Analysis of Parasitic Oscillations in Commutation Cells with High Voltage Power MOSFETs

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Abstract

The dynamic behavior of power semiconductor devices with decreasing area-specific on resistances is more and more influenced by parasitic characteristics of packages and PCBs. These parasitic characteristics can increase the switching times of power semiconductors and hence reduce the efficiency of power electronic circuits. Furthermore, during commutation the reliability of circuits can be compromised by parasitic oscillations with temporarily increasing amplitudes. Optimized parasitic characteristics of packages and PCBs are therefore necessary. This applies in particular, if fast power semiconductors are used. Using the example of a one quadrant buck converter topology with a high voltage power MOSFET and a SiC SCHOTTKY diode, in this work a methodology is developed that enables the prediction of parasitic oscillations with temporarily increasing amplitudes during commutation and the improvement of the stability of commutation cells. Thereto, suitable circuit models of the power semiconductors and the semiconductor's environment are required.

Large-signal models of power MOSFETs and SCHOTTKY diodes are deduced for the relevant operating conditions. The combination of curve tracer and short circuit measurements allows the static parameterization of the MOSFET model for the regarded operating range. It is shown that the MOSFET's capacitances can be determined from dynamic measurements. Compared to capacitances measured in accordance with DIN ICE 747, the dynamic capacitances result in an improved conformity of simulations and measurements.

The parasitic characteristics of the PCB and packages are modeled with coupling capacitances and effective resistances and inductances. The parameterization of the model is based on quasi-static field simulations of the 3D models of the PCB and packages.

The derived behavioral models of the power semiconductors and the electrical interconnections of the PCB and packages are combined with simple models of the DC voltage link, the driver and the load circuit to the model of the buck converter topology. The comparison of measured and simulated switching characteristics approves the proposed buck converter model and the determined parameterization.

For the relevant operating points of the buck converter topology, small-signal equivalent circuit models are deduced. It is shown that the stability analysis of the small-signal models enables the prediction of parasitic oscillations with temporarily increasing oscillations during commutation. From the stability analysis of the small-signal models with different parameterizations, measures for an improved stability of the commutation cell are concluded. Design iterations and development costs can be saved with the presented methodology.

Kurzfassung

Das dynamische Verhalten von Leistungshalbleitern mit immer kleineren flächenspezifischen Einschaltwiderständen wird stärker durch die parasitären Eigenschaften von Gehäusen und Leiterplatten beeinflusst. So können die Parasiten die Schaltzeiten der Halbleiter erhöhen und damit die Effizienz von leistungselektronischen Schaltungen verringern. Außerdem kann die Zuverlässigkeit von Schaltungen während der Kommutierung durch parasitäre Schwingungen mit zwischenzeitlich steigenden Amplituden beeinträchtigt werden. Insbesondere bei Verwendung von schnellen Leistungshalbleitern ist deshalb die Optimierung der parasitären Eigenschaften von Gehäusen und Leiterplatten notwendig. Am Beispiel eines Tiefsetzstellers mit einem Hochvolt-Leistungs-MOSFET und einer SiC Schottky-Diode wird in dieser Arbeit eine Methodik entwickelt, die die Vorhersage von parasitären Schwingungen mit zwischenzeitlich steigenden Amplituden während der Kommutierung und die Stabilitätsoptimierung von Kommutierungszellen ermöglicht. Dafür werden geeignete Modelle der Leistungshalbleiter und der Halbleiterumgebung benötigt.

Verhaltensmodelle von Leistungs-MOSFETs und Schottky-Dioden werden für die relevanten Betriebsbedingungen abgeleitet. Die Kombination von Curve-Tracer- und Kurzschlussmessungen ermöglicht die statische Parametrierung des MOSFET-Models für den betrachteten Betriebsbereich. Es wird gezeigt, dass die Kapazitäten des MOSFET-Models aus dynamischen Messungen extrahiert werden können und dass diese Kapazitäten zu einer besseren Übereinstimmung von Messungen und Simulationen führen als die Kapazitäten, die entsprechend der DIN IEC 747 gemessen wurden.

Die parasitären Eigenschaften von Gehäusen und Leiterplatten werden mit Koppelkapazitäten und effektiven Widerständen und Induktivitäten modelliert. Mit Hilfe der Finite-Elemente- und der Randelemente-Methode werden die Modellparameter bestimmt.

Die entwickelten Verhaltensmodelle der Halbleiter und der elektrischen Verbindungen sowie einfache Modelle des Zwischen-, Treiber- und Lastkreises werden zum Modell des Tiefsetzstellers zusammengefügt. Das Modell kann mit den gemessenen bzw. berechneten Kennlinienfeldern und Parametern das Schaltverhalten des MOSFETs nachbilden.

Für die relevanten Arbeitspunkte des Tiefsetzstellers werden Kleinsignalersatzschaltbilder ermittelt. Es wird gezeigt, dass die Stabilitätsanalyse der Kleinsignalersatzschaltbilder die Vorhersage von parasitären Schwingungen mit zwischenzeitlich steigenden Amplituden während der Kommutierung ermöglicht. Maßnahmen zur Stabilitätsoptimierung der Kommutierungszelle werden aus den Ergebnissen der Stabilitätsanalyse von verschiedenen Parametrierungen abgeleitet. Designiterationen und Entwicklungskosten können so reduziert werden.

Theses

- The stability analysis of commutation cells will further gain in importance.

...

- The static and dynamic characteristics of conventional and SJ power MOSFETs can be represented by different parameterizations of the same equivalent circuit elements.
- Interelectrode capacitances of behavioral MOSFET models can be parameterized by means of switching characteristics.
- The dynamic parameterization of behavioral MOSFET models on the basis of switching operations is superior to a parameterization with small-signal capacitances that are measured in accordance with the standard DIN IEC 747.
- A power MOSFET's gate charge during commutation can be simulated accurately even if a constant gate source capacitance is assumed.

...

- During commutation of high efficient power semiconductor devices, inductive voltage drops across electrical interconnections of packages and PCBs can be modeled sufficiently by constant self and mutual inductances.
- During commutation, resistive voltage drops across electrical interconnections of packages and PCBs can not be modeled by constant self and mutual resistances.
- Self and mutual resistances and inductances can be represented by effective inductances and resistances. The values of these effective resistances and inductances vary during turn-on and turn-off.

...

- The consideration of a possible gate source voltage dependency of a power MOSFET's drain source capacitance improves the simulation of the terminal behavior of single switching operations solely if the charging of the drain source capacitance limits the drain source voltage slope during commutation.

...

- Oscillations with temporarily increasing amplitudes can be predicted by means of the stability analysis of the small-signal equivalent circuit models of the power supplies' operating points - if the dwell time in areas with unstable operating points is large compared to the periods of the corresponding eigenfrequencies.
- The neglect of the chip-external coupling capacitances in the small-signal models of commutation cells reduces the value of the stability analysis.
- The stability analysis of a *single* operating point of a switching-mode power converter does not enable a reliable prediction of parasitic oscillations during commutation.
- The analysis of parasitic oscillations by means of resonant circuits can be deficient.
- The measurement of voltage and current characteristics of commutation cells has an impact on the stability of the commutation cells.
- Steeper switching slopes do not necessarily decrease the stability of commutation cells.

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- Oscillations in commutation cells that are caused by transit times of carriers can not be modeled with *lumped* circuit elements.

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1 Introduction

This chapter gives a general overview of the motivation of this work. Section **1.1** provides information on the background and the importance of the analysis of parasitic oscillations in commutation cells with high voltage power metal-oxide-semiconductor field-effect transistors (MOSFETs). The requirements for the analysis are discussed in section **1.2**. Subsequently, a brief summary of the state of the art of the determined requirements, and the concluded scope and objectives of this work are given in section **1.3** and **1.4** respectively.

1.1 Background and Importance of the Topic

Practically, all electronic devices require some kind of energy conversion since electric energy is usually not used in its produced or distributed form. Electronic circuits that convert electric energy from the given power input to an aimed power output are referred to as power supplies and power converters respectively. In power electronics, the energy flow is usually controlled with semiconductor devices that are switched on and off with relatively high frequencies. Advantages of power supplies with this switched-mode conversion include better power efficiency, lower heat generation as well as smaller size and weight compared to linear power supplies. ***Commutation cells*** are the centerpieces of power electronics. They consist of two semiconductor switches, which are alternatively conducting or blocking.

The development of the ***power MOSFET*** in the second half of the nineteen seventies replaced the bipolar junction transistor (BJT) almost completely in power electronics. Being a majority carrier device, a MOSFET can switch at higher frequencies then a comparable bipolar transistor. At the end of the eighties, high voltage transistors with the known metal-semiconductor-oxide (MOS) structure reached their limits regarding the reduction of their area-specific on-resistance due to the dependency of the blocking voltage on the on-resistance [Hu 79]. As an advantageous combination of BJT and MOSFET, the insulated gate bipolar transistor (IGBT) enabled a further reduction of the on-resistance without a cutback of the blocking voltage. The removal of stored minority charge carriers from the drift zone causes the IGBT's characteristic tail current during turn-off and thus, increased turn-off losses (e.g. [Blair 05]). Due to these additional losses, feasible switching frequencies of IGBTs are lower compared to MOSFETs (e.g. [Arlt 04] and [Blake 00]). Hence, MOSFETs are usually the preferred device in switched mode power supplies (SMPSs) as well as low voltage high current applications.[1] The market introduction of super junction (SJ) MOSFETs in the late nineties and their continuous enhancements increased the applicable voltage range of

[1] Junction field-effect-transistors (JFETs) are also unipolar devices. However, power JFETs are usually normally-on and, therewith, less accepted than MOSFETs (cp. [Kaminski 09] and [Treu 07]).

MOSFETs. Today, silicon carbide (SiC) MOSFETs are on the verge of being launched into the market [Richmond 09]. With respect to the SiC MOSFETs' potential operating voltage of up to 10 kV with on-resistances below 200 $^{m\Omega}/_{cm^2}$ (e.g. [Kaminski 09]), the usage of power MOSFETs will probably further broaden.[2]

The ***industry trend towards higher volume power density*** with the aim of miniaturization and system integration is one of the basic challenges facing future power supplies [Lorenz 99]. Additionally, there is a ***tendency towards stricter requirements*** regarding reliability, robustness, electromagnetic compatibility and power efficiency. The switching frequency of the semiconductors corresponds to the amount of energy that needs to be stored intermediately in inductor and capacitor material. Increasing frequencies reduce this energy. Thus, less material and smaller passive components respectively can be used for higher frequencies. However, miniaturization and high efficiency of power converters are competing objectives due to the increase of the semiconductor devices' average power dissipation with switching frequency.[3] The limitation on the frequency has been reduced by continual technology achievements that have mainly been focusing on the reduction of the on-resistance per silicon area. The reduction of the on-resistance enables not only the decrease of conduction losses but also of switching losses due to the usually involved chip area shrink and the resulting reduction of the semiconductor devices' capacitances.

Considering the more recent semiconductor technology achievements, the frequency limitation caused by the devices' switching losses has become much less important for a wide range of blocking voltages than it was a few years ago. However, the dynamic behavior of semiconductors with smaller chip-internal capacitances is stronger influenced by parasitics in commutation cells (see e.g. [Miller 10] and [Bayerer 10]). Parasitic circuit elements have an impact on the actual $^{dv}/_{dt}$ and $^{di}/_{dt}$ and on the occurrence of ***parasitic oscillations with temporarily increasing amplitudes*** during commutation. While decreasing $^{dv}/_{dt}$ and $^{di}/_{dt}$ prohibit the semiconductors' operation at their best dynamic behavior and electrical efficiency, parasitic oscillations with temporarily increasing amplitudes may compromise the reliability of the device itself and of the entire application system. The exceedance of the oxides' breakdown voltage during such oscillations could lead to a permanent device failure, and electromagnetic interference may interrupt, obstruct or otherwise degrade or limit the performance of the application system - and can result in expensive redesigns of printed circuit boards (PCBs), packages as well as semiconductors. The usage of modern semiconductor devices necessitates hence optimized parasitics in commutation cells. For the optimization, the influencing factors on the devices' dynamic behavior and the occurrence of parasitic oscillations with temporarily increasing amplitudes must be analyzed first.

Against this background, this dissertation was developed. Due to recent MOS technology achievements and assuming that the SiC and wide bandgap market will evolve similar to that of silicon (Si),[4] this work focuses its analyses on commutation cells with power MOSFETs.

[2] Even though the wide bandgap MOS devices still need to be optimized, they have already benefits over silicon insulated gate bipolar transistors (IGBTs) (see e.g. [Stalter 07]).

[3] The power devices' average power dissipation consists of forward, blocking, switching and driving losses.

[4] Initially, Si JFETs and BJTs dominated the market. Due to the ease of operation offered by a normally off voltage controlled transistor, sales dropped when a viable MOSFET was launched (e.g. [Richmond 09]).

1.2 Requirements for the Analysis of Parasitic Oscillations in Commutation Cells

Detailed analyses of the switching behavior of semiconductors and parasitic oscillations respectively that are *exclusively* based on dynamic measurements are little convenient. This is mainly due to the involved time, costs and effort, and the limited possibility to analyze the influence of single (parasitic) circuit elements and the therewith restricted revealing of coherences. Computer-aided analyses and simulations of switching operations in commutation cells can overcome the drawbacks of experimental analyses. However, without ...

- ... suitable behavioral models, ...
- ... an appropriate parameterization of the models and ...
- ... viable methods and procedures ...

... an effective and meaningful analysis can not be realized.

(I) Both ***large-signal and small-signal models*** of semiconductor devices and electrical interconnections in PCBs and packages are needed for the analyses of the dynamic behavior of commutation cells.[5] Suitable large-signal models enable the simulation and analysis of the semiconductors' current and voltage waveforms during commutation. Suitable small-signal models are necessary for the analysis of the circuit's stability.

(II) Just as important as suitable behavioral models is a reasonable ***parameterization*** of the models. The comparison of large-signal simulations and dynamic measurements imply the accuracy of the parameterization of equivalent circuit elements of semiconductor devices and electrical interconnections of PCBs and packages. The parameters of small-signal models are based on the linearization of accordant large-signal models in their operating points.

(III) Suitable circuit models and appropriate model parameterization can only be fully utilized with ***methods and procedures*** that reveal, explain and clearly visualize the considered variables' impact on the switching behavior of semiconductors and the occurrence of parasitic oscillations with temporarily increasing amplitudes in commutation cells.

1.3 State of the Art and Gaps in the Knowledge

(I) Behavioral Models

Behavioral modeling of power semiconductors for the computer-aided design of power electronic circuits is discussed in [Wintrich 97]. In standard literature of power electronics, the switching behavior of power MOSFETs is usually explained with a behavioral model, which consists of the output characteristics and the MOSFET's parasitic capacitances $C_{\mathrm{DG\,chip}}$,

[5] In this work, voltage and current sources, and passive components - such as resistors, capacitors and inductors - are assumed to be ideal. Accordingly, their modeling is not discuss.

$C_{\mathrm{GS\,chip}}$ and $C_{\mathrm{DS\,chip}}$ (see e.g. [Schröder 06], [Lutz 06] and [Mohan 03]). In [Xu 90], a comprehensive behavioral model of a power MOSFET is presented. Behavioral models of SCHOTTKY diodes are e.g. discussed in [Funaki 08] and [Pendharkar 95]. Lumped and distributed circuit models of electrical interconnections are e.g. presented in [Paul 08]. The behavioral models of the power semiconductors, the electrical interconnections of packages and PCBs, and the passive components can be combined to large-signal models of the power converter of interest. The necessary circuit elements depend on the aimed circuit analysis.

A relatively simple small-signal circuit model for the analysis of oscillations in commutation cells with power MOSFETs is published in [Severns 85], [Fujihira 08], [Kapels 09], [Kaindl 10] and [Höch 10]. The model does not include the MOSFET's output conductance g_{ds}, the chip-external capacitances $C_{\mathrm{dg\,ext}}$, $C_{\mathrm{gs\,ext}}$ and $C_{\mathrm{ds\,ext}}$ and parasitic resistances. Due to the lacking analytical description of more complex small-signal models, the impact of these equivalent circuit elements on the stability is not analyzed with stability theory.[6]

(II) Parameterization of Behavioral Models

Typical temperature dependent output characteristics up to a drain source voltage of 20 V are usually given in the application note of a high voltage power MOSFET (see e.g. [STM 08] and [Inf 10b]). The reason for this is not necessarily the simplifying assumption that the current of an output characteristic is almost constant in the saturation region, but rather the lack of appropriate measurement modes of commercial curve tracers for this region.[7] Information about the output characteristics at higher drain source voltages is lacking.

Application notes of power MOSFETs include the small-signal short circuit capacitance voltage characteristics C_{rss}, C_{iss} and C_{oss} that are measured in accordance with DIN IEC 747 at a gate source voltage of zero volt and a small-signal frequency of 1 MHz (see e.g. [STM 08], [Inf 10b] or [Wintrich 10]). The measurement conditions of these capacitance voltage characteristics do not represent typical switching conditions. For C_{rss} and C_{iss}, this is e.g. mentioned in [Stengl 92]. In [Elferich 05], C_{iss}, C_{rss} and C_{oss} of a low voltage power MOSFET are determined that depend on *both* the drain source voltage and the gate source voltage. The characteristics are obtained by a combination of impedance analyzer measurements (for capacitance characteristics below the threshold voltage V_{th}) and voltage ramp measurements (for capacitance characteristics above V_{th}). For gate source voltages above V_{th}, the voltage ramp measurement is limited by high drain currents (and the corresponding losses). In [Elferich 05], C_{oss} is not measured above V_{th}. The dependency of different high voltage power devices' gate capacitances on the drain source (collector emitter) voltage *and* the gate source (gate emitter) voltage is e.g. demonstrated in [Phankong 09] and [Funaki 09]. The gate source (gate emitter) voltage dependency of C_{oss} and the drain source (collector emitter) capacitance respectively are not measured in [Phankong 09] and [Funaki 09].

For the dynamic parameterization of behavioral MOSFET models, it should be kept in mind that the capacitance characteristics C_{iss}, C_{rss} and C_{oss} contain MOS capacitances, which are

[6] Stability theory analyses the stability of solutions of differential equations and of trajectories of dynamical systems under small perturbations of initial conditions. An introduction is e.g. given in [Merkin 97]).

[7] See e.g. [Agi 10a], [Tek 96] and [Tek 02]).

frequency dependent (see e.g. [Schröder 06]). During switching the slope of the drain source voltage and the gate source voltage vary significantly. Accordingly, the voltage ramp measurements or small-signal measurements may not represent typical conditions of switching operations, and the determined capacitance voltage characteristics may not represent the MOSFET's capacitances during turn-on and turn-off. Due to the drawbacks of small-signal and voltage ramp measurements, a method was developed, which enabled the determination of the feedback capacitance of a MOSFET from measured switching operations in a buck converter topology. The DUT was a low voltage trench gate MOSFET. The results are published in [Höch 07a], [Höch 07b] and [Höch 07c]. The output capacitance is not considered in these publications. For high efficient and fast switching power devices, the effects of the output capacitance can not be ignored (for details see e.g. [Gauen 89], [Int 04] and [Xiong 09]). For the parameterization of a behavioral MOSFET model, the drain gate capacitance, the gate source capacitance *and* the drain source capacitance during switching operations are of interest. Apart from publications in the course of this dissertation ([Höch 09b] and [Höch 09c]), capacitance voltage characteristics of high voltage devices, which are based on switching characteristics, are not discussed in literature.

Typical temperature dependent forward and reverse current vs. reverse voltage characteristics, and typical capacitance vs. reverse voltage characteristic of a SCHOTTKY diode are usually given in the application note (see e.g. [Inf 08b]). The static characteristics are usually measured with a curve tracer. The junction capacitance voltage characteristics are measured in accordance with the standard DIN IEC 747.

For the RLCG parameter extraction of packages and PCBs, electromagnetic field simulations are used (see e.g. [Gutsmann 07] and [Heeb 12]). For package and PCB structures that are small compared to the wavelength of the maximum frequency of interest, the couplings between the magnetic and the electric field can be neglected [Paul 09]. Frequency dependent material properties, skin and proximity effect can still be considered in field simulators that neglect these couplings. In literature, it is not discussed, how a reasonable application dependent frequency can be determined for the extraction of the RLCG parameters.

The parameterization of small-signal models is based on the linearization(s) of the parameters of large-signal models in the considered operating point(s). Linear circuit elements' parameterizations are equal in large-signal and small-signal models.

(III) Methods and Procedures

The impact of switching conditions (DC link voltage, driver voltage, load current, gate resistance and junction temperature) and parasitic circuit elements (loop inductance, source inductance, inductive couplings) on simulated (and measured) switching characteristics is e.g. presented in [Witcher 02] and [Gutsmann 07]. Such simulations (and measurements) are necessary for the determination of switching times and losses. The impact of switching conditions and parasitic circuit elements on the switching times and losses can be studied. An estimation of the stability that is solely based of the simulation (and measurement) of

switching characteristics is little convenient due to infinite combinations of switching conditions and parasitic circuit elements' parameterizations, as well as the involved time and effort for the simulations and measurements. Oscillations with temporarily increasing amplitudes during switching operations might be detected by luck or not at all.

A systematic approach for the stability analysis is presented in [Severns 85]. [Severns 85] recommends the analysis of selected operating points of commutation cells by means of stability theory. The impact of equivalent circuit elements on the stability can be estimated. However, the computing technology of the nineteen eighties limited a comprehensive analysis of the entire operating range of interest. The more recent analyses in [Kapels 09] and [Kaindl 10] are also based on stability theory, but they do not take advantage of the possibilities of nowadays computing technology. Only a not further specified operating point is analyzed in these publications. Apart from publications in the course of this dissertation ([Höch 10] and [Höch 11]), in literature, the methods of stability theory are not applied to the entire operating range of interest of a commutation cell.

1.4 Scope, Objectives and Structure of this Work

Parasitic oscillations with temporarily increasing amplitudes during commutation indicate a temporary instability of the commutation cell. The goal of this work is the development of a methodology that enables both the prediction of parasitic oscillations with temporarily increasing amplitudes in commutation cells and the optimization of the stability of commutation cells during switching operations. However, ...

- ... the derivation of condition of use specific large-signal behavioral models of all kinds of power semiconductor devices, ...
- ... the implementation of the semiconductor devices' large-signal models in the circuit models of all kinds of power supplies with switched-mode conversion, ...
- ... the derivation of the corresponding small-signal models, ...
- ... and the derivation of the corresponding differential equation systems and the subsequent stability analyses ...

... are far beyond the possibilities of a dissertation.

This work uses the example of a commutation cell in a one quadrant buck converter topology with a 650 V 16 A SJ MOSFET and a 600 V 4 A SiC SCHOTTKY diode. For this commutation cell, the behavioral model generation, parameterization and evaluation, as well as the derivations for the stability analysis, the stability analysis and its evaluation are described and discussed in detail. Thereby, the attempt is made to fill the gaps in knowledge, which are identified in the previous section. Although, the stability analysis *enables* the optimization of the stability and the damping, the optimization of the commutation cell is not an objective of this work. Due to the analysis of the sample commutation cell, the objectives

of this work are *apparently* limited to the development of a methodology that enables ...

- ... the prediction of parasitic oscillations with temporarily increasing amplitudes in commutation cells with a power MOSFET and a SCHOTTKY diode, and ...
- ... the optimization of the stability and the damping of commutation cells with a power MOSFET and a SCHOTTKY diode.

However, this work can be used as a starting point for the derivation and implementation of necessary adjustments for the analysis of other commutation cells.

The objectives can be assigned to four subtasks, which are represented by the four main chapters of this work. In chapter **2** on page 9 et seq., large-signal models of power MOSFETs and SCHOTTKY diodes are derived for conditions of use that are for example typical in power factor correction (PFC) circuits. The models' static and dynamic parameters are determined for a sample SJ MOSFET and a sample SiC SCHOTTKY diode. In chapter **3** on page 65 et seq., the modeling of electrical interconnections in packages and PCBs is discussed. A large-signal model of the interconnections of the packages and the PCB of the sample buck converter topology is derived and the circuit parameters are extracted by means of field simulations. The model of the interconnections is combined with the large-signal models of the power devices, ideal passive components and ideal voltage sources. The resulting equivalent circuit model of the buck converter topology is subsequently evaluated in chapter **4** on page 95 et seq. by comparison of some measured and simulated switching characteristics. In chapter **5** on page 111 et seq., the stability of the buck converter topology is analyzed in the entire operating range of interest by means of the eigenvalues of the small-signal equivalent circuit models of the buck converter's operating points. Conclusions on the occurrence of parasitic oscillations with temporarily increasing amplitudes during commutation are drawn. After the comparison of the stability analysis of different circuit parameterizations, measures for the optimization of the circuit elements are concluded. The results of the stability analysis are evaluated by means of simulated switching operations. Finally, a summary of the major results of this work, and a list of necessary continuing works is given in chapter **6** on page 171 et seq..

2 Modeling of Power MOSFETs and Schottky Diodes in Commutation Cells

In this chapter, the modeling of power MOSFETs and SCHOTTKY diodes in commutation circuits is discussed. In section **2.1**, advantages of behavioral models are briefly summarized. A behavioral model of a power MOSFET and a SCHOTTKY diode are derived in section **2.2**. The static and dynamic parameterization of the models are presented in section **2.3** and **2.4** respectively. In chapter **4** on page 95 et seq., the proposed modeling is evaluated.

2.1 Advantages of Behavioral Models

Both behavioral models and models based on semiconductor physics are used for the simulation of semiconductor devices in commutation circuits. As argued in [Wintrich 97], models based on semiconductor physics are particularly suitable for the analysis of the device itself. The semiconductor device is modeled by the calculation of internal physical processes (cp. e.g. [Kraus 96]). Due to the required device-specific technological information, physics-based models are usually designed by the device manufacturer. Because of the included technological information, these models are usually not available for application engineers of power electronics. However, an exact representation of the devices' internal behavior is not necessarily required for circuit analyses. Often, it is sufficient to simulate the terminal behavior of the device. The terminal behavior can often be represented by a convenient network of idealized equivalent circuit elements such as (voltage dependent) resistors, capacitors and inductors, as well as (controlled) current and voltage sources. Although behavioral models are only conditionally suitable for the analysis of the device itself, they provide several advantages for circuit analyses and therewith, for the analysis of parasitic oscillations in commutation cells of MOSFETs.

In particular, this work is based on behavioral modeling because behavioral models ...

- ... are generally valid for entire device families and do not depend on the device's generation or the semiconductor material. Thus, further device developments result solely in an altered parameterization of the behavioral model (cp. e.g. [Agi 08]).
- ... consist of lumped elements. This ensures relatively short simulation times.
- ... are descriptive. The network of the lumped circuit elements assures a familiar way of thinking for design and application engineers.
- ... represent most device characteristics independent of one another. This admits the analysis of the single circuit elements' influence on the dynamic behavior.

- ... enable the reduction of the semiconductor device to the relevant properties for the conditions of use that need to be analyzed.
- ... can be parameterized with data determined from measurements. Unpublished device-specific technological information is not needed.
- ... permit the integration of device characteristics as look-up tables. This is especially convenient for the modeling of non-linear dependencies.

2.2 Derivation of Conditions of Use Specific Large-Signal Behavioral Models

Knowledge about the *basic* structure and *fundamental* physical processes of the semiconductor enables a deeper understanding of the behavioral model itself and the device specific parameterization of the model. Therefore, based on the description of the basic structure of a power MOSFET and a SCHOTTKY diode, and the explanation of fundamental physical processes during the devices' operation, large-signal behavioral models of the semiconductors are derived in subsection **2.2.2** and **2.2.3** respectively. Thereby, the aim of this is section is *not* an exact physical description of the devices but the impartment of the origin the equivalent circuit elements and their characteristics.[1] Initially, assumptions for the behavioral modeling and disregarded conditions of use are summarized in the next subsection.

2.2.1 Assumptions and Disregarded Conditions of Use

Quasi-Static Operation Assumption

In accordance with [Tsividis 11], for the derivation of a conditions of a use specific large-signal behavioral model of a power MOSFET and a SCHOTTKY diode, it is assumed:

- The variation of currents during the dynamic operation of the semiconductor devices is slow enough for the neglect of magnetic fields inside the semiconductor chips. This assumption allows the use of electrostatic relations, in which constant charges and voltages are replaced by time-varying quantities.
- The dimension of the semiconductor chips is much smaller than the wavelength corresponding to the maximum frequency of interest. Therewith, the semiconductor chips remain overall electrically neutral and KIRCHHOFF's current law can be applied.
- Hot electron effects or leakage currents through insulators are not present.

[1] For a more exact description of the semiconductor physics, it is referred to the literature [Lutz 11], [Sze 07], [Schröder 06], etc..

Under these assumption, the transit times of carriers can be neglected: For varying terminal voltages, the charge distribution in the devices at any time are hence assumed to be identical to those that would be found if DC voltages were applied instead.[2] In the first instance, the thickness of the semiconductor chip would therewith limit the steepness of signal slopes during commutation and the oscillation frequencies that can be modeled with behavioral models. However, usually, the dimensions of the electrical interconnections of packages and PCBs are significantly larger than the dimensions of power semiconductors. Accordingly, the dimensions of packages and PCBs limit the steepness of signal slopes and oscillations frequencies that can be modeled with lumped circuit elements. This is discussed in more detail in chapter **3** on page 65 et seq..

Disregarded Conditions of Use of the Power Semiconductors

The anti-parallel body diode of the power MOSFET is not used. Furthermore, critical operation conditions that cause a turn-on of the MOSFET's parasitic bipolar transistor are disregarded.[3] It is also assumed that the MOSFET and the SCHOTTKY diode are well below their breakdown voltages during their dynamic operation. Accordingly, these functionalities of the power devices are not considered in the behavioral models.

2.2.2 Behavioral Model for Power MOSFETs

In this work, parasitic oscillations in a commutation cell with a high voltage super junction (SJ) MOSFET are analyzed by means of behavioral models. Compared to conventional power MOSFETs, the structure of SJ power MOSFETs differs by deep p-doped columns inside the n-doped drain region. This difference leads to static and dynamic characteristics of SJ MOSFETs, which can not be represented by physics-based models of conventional power MOSFETs (cp. [Kraus 96] and [Lagies 01a]). However, the static and dynamic characteristics of conventional and SJ power MOSFETs can be represented by different parameterizations of the same behavioral model. In **2.2.2.1**, the behavioral model of a power MOSFET is derived. Thereto, the basic structure and fundamental physical processes are explained for the older - the conventional - device concept.[4] In **2.2.2.2**, differences between conventional and SJ power MOSFETs are briefly discussed and it is concluded that these differences have only an impact on the parameterization of the behavioral model.

2.2.2.1 Conventional Power MOSFETs

In Fig. 2.1, the cross section of an enhancement mode n-channel MOSFET is shown with its p-type and n-type doping layers and its isolated gate. Geometric dimensions that are subsequently used are labeled. At first glance, it seems, that no current can flow between

[2] See [Tsividis 11] for details and limitations of quasi-static models.
[3] For a MOSFET behavioral model with these functionalities, see e.g. [Xu 90].
[4] An overview of the history of the conventional and the SJ MOSFET is e.g. given in [Deboy 04].

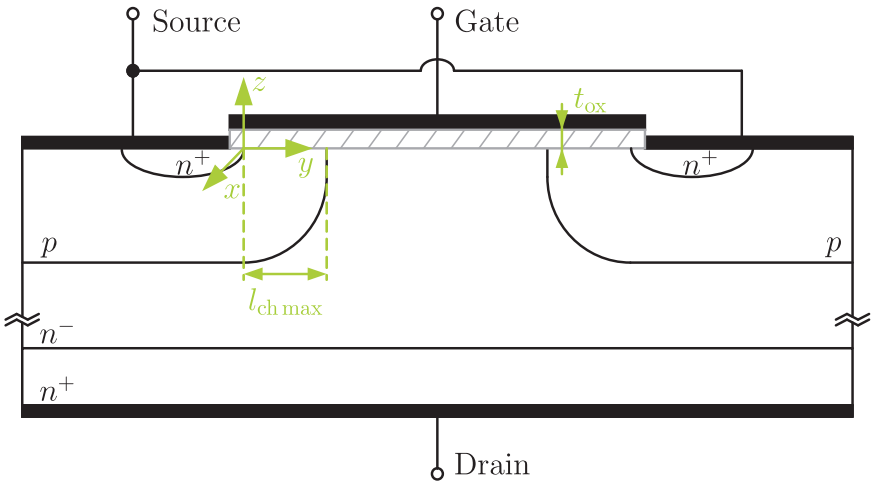


Figure 2.1: Cross section of an n-channel power MOSFET

a cell's drain and source terminals since one of the two pn-junctions is always blocked if a drain source voltage is applied. However, high enough positive gate source voltages will draw enough electrons towards the oxide for the development of an n-channel. Source and drain are connected through this channel and electrons can flow in between. Representing an MOS capacitance, the metal, oxide and p-type semiconductor layer sequence is quintessential for the MOSFET's functionality. Thus, it is discussed in more detail in the next paragraphs.

A MOSFET's n-Channel - A MOS Capacitance with a p-Type Semiconductor

As shown in Fig. 2.2, for a voltage dependent MOS capacitance, three basic conditions - accumulation, depletion and inversion - can be distinguished. The following explanations of the conditions assume an ideal MOS capacitance.[5]

(I) For negative gate source voltages, holes are drawn towards the oxide and form an ***accumulation*** layer. The accumulation layer is relatively thin and almost the entire gate source voltage drops across the insulator.[6] Thus, the effective MOS capacitance $C_{\mathrm{MOS\,p}}$ is represented by the oxide capacitance $C_{\mathrm{ox\,p}}$ and can be calculated with

$$C_{\mathrm{MOS\,p}} = C_{\mathrm{ox\,p}} = \varepsilon_0 \cdot \varepsilon_{\mathrm{ox}} \cdot \frac{A_{\mathrm{ox\,p}}}{t_{\mathrm{ox}}} \tag{2.1}$$

with the oxide's relative permittivity $\varepsilon_{\mathrm{ox}}$, the effective oxide area of the opposed surfaces between gate and the p-type semiconductor $A_{\mathrm{ox\,p}}$ (x-y area in Fig. 2.1) and the oxide thickness t_{ox} (z dimension in Fig. 2.1) (see e.g. [Thuselt 05]).

[5] Characteristic for an ideal MOS capacitance is: (i) The metal work function is equal to the semiconductor work function at zero bias, i.e. the Fermi level of the semiconductor is aligned with the Fermi level of the metal. The gate dielectric is assumed to be free of any charges. (ii) There is no carrier transport through the oxide. (iii) The semiconductor is uniformly doped.

[6] According to [Cooke 93], the voltage drop across the charge layers is negligible.

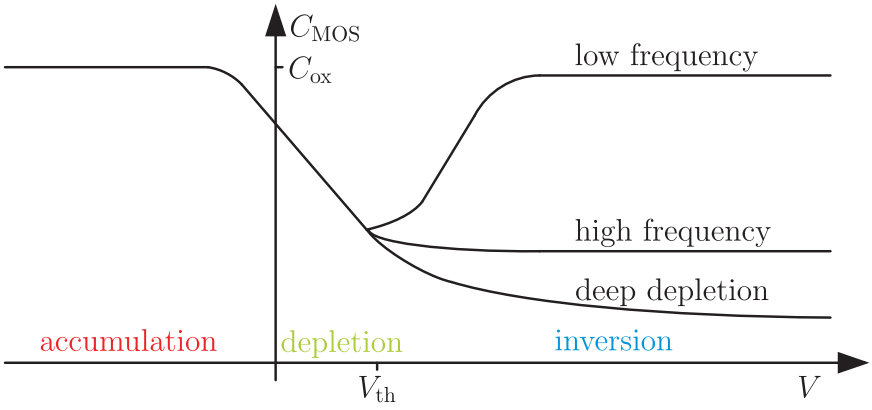


Figure 2.2: Qualitative small-signal capacitance voltage characteristics of a MOS capacitance with a p-type semiconductor (cp. e.g. [Schröder 06])

(II) For positive gate source voltages $V_{\mathrm{GS\,chip}}$, the holes are depleted beneath the gate oxide. During ***depletion***, the remaining ionized acceptor atoms form a space charge region with a gate source voltage dependent width $w_{\mathrm{scr\,p}}$. The gate source voltage dependent differential depletion layer capacitance can be expressed as

$$C_{\mathrm{scr\,p}}(v_{\mathrm{GS}}) = \varepsilon_0 \cdot \varepsilon_{\mathrm{p}} \cdot \frac{A_{\mathrm{ox\,p}}}{w_{\mathrm{scr\,p}}(V_{\mathrm{GS\,chip}})} \tag{2.2}$$

with the p-type semiconductor's relative permittivity ε_{p} (cp. e.g. [Porst 79]). The effective MOS capacitance during depletion results from a series connection of the depletion capacitance $C_{\mathrm{scr\,p}}$ and the oxide capacitance $C_{\mathrm{ox\,p}}$ (cp. e.g. [Schröder 06]), giving

$$C_{\mathrm{MOS\,p}}(V_{\mathrm{GS\,chip}}) = \frac{C_{\mathrm{ox\,p}} \cdot C_{\mathrm{scr\,p}}(V_{\mathrm{GS\,chip}})}{C_{\mathrm{ox\,p}} + C_{\mathrm{scr\,p}}(V_{\mathrm{GS\,chip}})}. \tag{2.3}$$

According to (2.2) and (2.3), $C_{\mathrm{scr\,p}}$ and $C_{\mathrm{MOS\,p}}$ decrease with rising gate source voltages.

(III) An increase of the gate source voltage above the threshold voltage V_{th} draws electrons towards the oxide. The minority carriers form an ***inversion*** layer. The capacitance depends on the ability of the electrons to follow the applied voltage signal. If the recombination-generation rates of the electrons are able to keep up with the applied voltage variation, the incremental charge at the semiconductor side is no longer at the edge of the space charge region as during depletion but at the inversion layer beneath the oxide. Hence, the MOS capacitance increases at the beginning of inversion and equals the oxide capacitance $C_{\mathrm{ox\,p}}$ during strong inversion. Fig. 2.3 depicts the placement of the incremental charge of the capacitance during strong inversion for different voltage signals with the location of the charge ρ (z dimension in Fig. 2.1) in the metal and the semiconductor as well as the acceptor concentration N_A. The frequency dependence of the capacitance is related to the carrier lifetime and the thermal generation rate in the semiconductor. As a consequence, capacitance voltage characteristics measured at high frequencies do not show the capacitance increase during strong inversion (see Fig. 2.2 and cp. [Grove 64] and [Hofstein 65]).

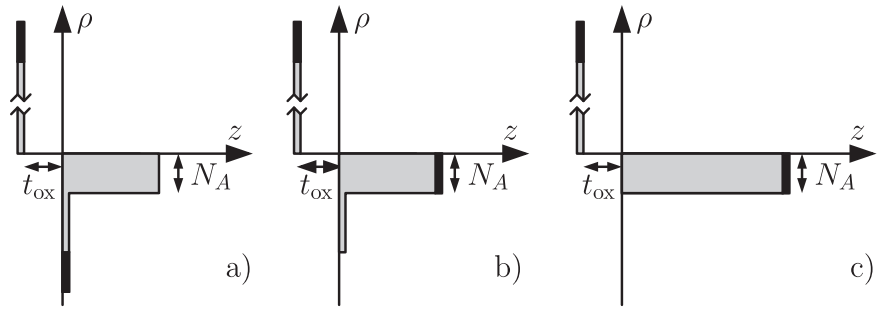


Figure 2.3: Location of the incremental displacement charge (black area) in a MOS layer during strong inversion in case of a) a relatively low small-signal frequency, b) a relatively high small-signal frequency and c) a deep depletion due to a relatively high small-signal frequency and a fast sweeping rate [Sze 07]

The described conditions of the MOS capacitance are not only key for understanding the functionality of a MOSFET but also for its dynamic behavior. Besides the described p-type MOS capacitance, there are two n-type MOS capacitances in the MOSFET's structure which need to be considered for the deduction of a MOSFET behavioral model. A MOS capacitance with a n-type semiconductor behaves as p-type MOS capacitance except the corresponding voltage is reversed biased for accumulation, depletion and inversion.

For a qualitative discussion of the MOSFET's physics of operation, important operation conditions are subsequently discussed and depicted in Fig. 2.4 and Fig. 2.5 respectively.

Considered Conditions of Operation of the Power MOSFET

(I) If both a gate source voltage that is large enough to cause an inversion layer beneath the oxide, and a small drain source voltage is applied to the MOSFET, electrons will flow from source to drain through the conducting channel (see Fig. 2.5 a)). As long as the voltage drop $V_{\mathrm{DS\,Ch}}$ caused by the current transportation through the channel is negligible, the channel charge Q_{Ch} is approximately given by

$$Q_{\mathrm{Ch}} = C_{\mathrm{ox\,p}} \cdot (V_{\mathrm{GS\,chip}} - V_{\mathrm{th}}) \tag{2.4}$$

with the threshold voltage V_{th} (cp. [Lutz 06]). The carriers that build the channel are available for the current flow. As long as the channel pinch-off is insignificant, the channel current is proportional to $V_{\mathrm{DS\,Ch}}$, and the channel resistance can be calculated with

$$R_{\mathrm{Ch}} = \frac{l_{\mathrm{Ch\,max}}}{\sigma_{\mathrm{Ch}} \cdot A_{\mathrm{Ch}}} = \frac{l_{\mathrm{Ch\,max}}}{q \cdot \mathrm{n} \cdot \mu_{\mathrm{e}} \cdot \mathrm{t_{Ch}} \cdot \mathrm{w_{Ch}}} = \frac{(l_{\mathrm{Ch\,max}})^2}{Q_{\mathrm{Ch}} \cdot \mu_{\mathrm{e}}} \tag{2.5}$$

with the maximum channel length $l_{\mathrm{Ch\,max}}$ (y dimension in Fig. 2.1), the specific channel conductance $\sigma_{\mathrm{Ch}} = q \cdot \mathrm{n} \cdot \mu_{\mathrm{e}}$, the channel cross-section A_{Ch} (x-z area in Fig. 2.1), the electron charge q, the electron density n, the electron mobility μ_{e}, the channel thickness t_{Ch} (z

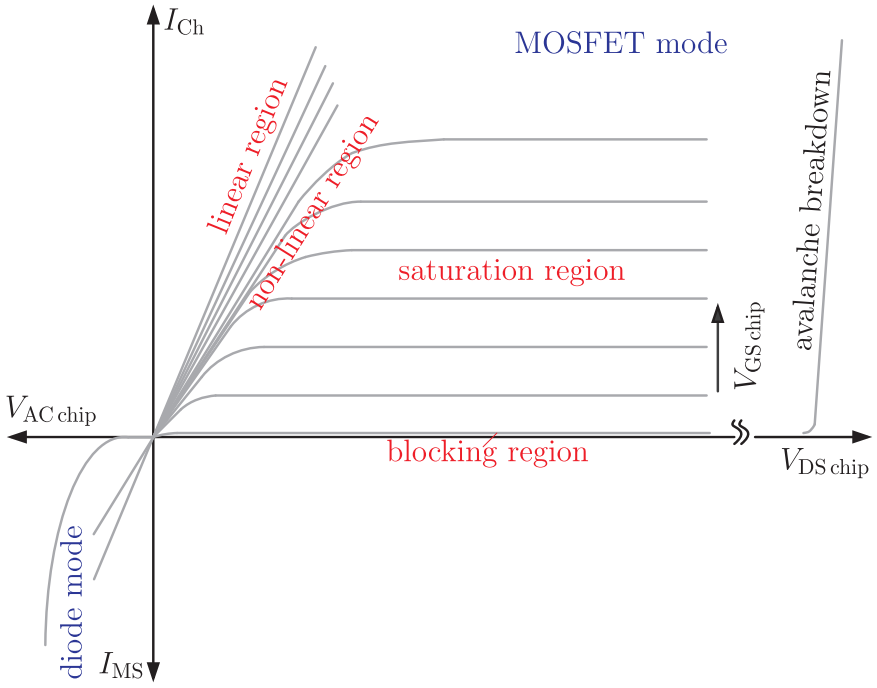


Figure 2.4: Current-voltage characteristics of a MOSFET (cp. with [Lutz 11])

dimension in Fig. 2.1) and the channel width w_{Ch} (x dimension in Fig. 2.1). Due to the proportionality of channel current and $V_{\mathrm{DS\,Ch}}$, this region is called the ***linear region***.

(II) For higher channel currents, the voltage drop $V_{\mathrm{DS\,Ch}}$ must be considered due to the location dependent potential difference between gate and channel:

$$Q_{\mathrm{Ch}}(y) = C_{\mathrm{ox\,p}} \cdot (V_{\mathrm{GS\,chip}} - V_{\mathrm{th}} - V_{\mathrm{DS\,Ch}}(y)) \tag{2.6}$$

The larger y gets, the higher the potential difference perpendicular to the channel and the smaller the corresponding channel thickness becomes. Therefore, the channel resistance increases and the current gain decreases with a rising drain source voltage. An increase of the drain source voltage, leads to $V_{\mathrm{DS\,Ch}} = V_{\mathrm{GS\,chip}} - V_{\mathrm{th}} = V_{\mathrm{DS\,sat}}$. The channel is pinched-off. The location where its inversion charge becomes approximately zero is called pinch-off point (see Fig. 2.5 b)). Due to the decreasing current gain, the operation area between the linear region and the pinch-off point at $l_{\mathrm{Ch\,max}}$ is named ***non-linear region***.

(III) If the drain source voltage continues to rise, the pinch-off point moves towards the source (see Fig. 2.5 c)). However, while the channel shortens, the voltage across the channel remains $V_{\mathrm{DS\,sat}}$, and the amount of electrons that arrive at the pinch-off point stay essentially the same.[7] Due to the current saturation, this region is called ***saturation region***.

(IV) Only leakage currents can flow from drain to source if the gate source voltage is beneath the threshold voltage and if the pn$^-$-junction is blocked due to applied drain source voltage (see Fig. 2.5). The conductance between the drain and the source terminal is almost

[7] For short channel effects, see e.g. [Sze 07].

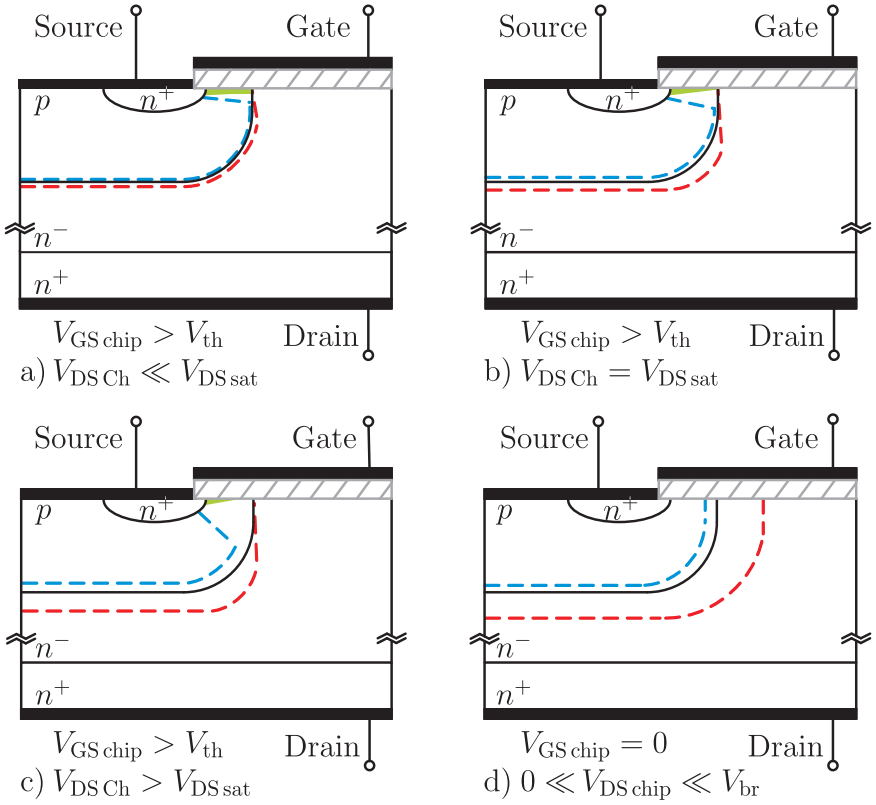


Figure 2.5: Cross sections of a power MOSFET if operated a) in the linear region, b) at the onset of saturation, c) in the saturation region and d) in the blocking region (cp. e.g. with [Schröder 06], [Mohan 03] and [Sze 07]) - The green plane represents the inversion layer beneath the oxide. The dashed lines typify the expansion of the depletion layer beneath the oxide and the space charge regions of the blocked pn-junction. The red line symbolizes the border of a positive and the blue line the border of a negative space charge region.

zero. In the ***blocking region***, the drain source voltage basically drops across the space charge region of the blocked pn$^-$-junction. According to [Lutz 11], for very abrupt junctions, whose doping transition occurs over a smaller length than a DEBYE length, the space charge capacitance $C_{\mathrm{scr\,pn^-}}$ can be calculated with the formula for a parallel plate capacitor

$$C_{\mathrm{scr\,pn^-}}(V_{\mathrm{DS\,chip}}) = \varepsilon_0 \cdot \varepsilon_{\mathrm{pn^-}} \cdot \frac{A_{\mathrm{pn^-}}}{w_{\mathrm{scr\,pn^-}}(V_{\mathrm{DS\,chip}})} \tag{2.7}$$

with the effective relative permittivity $\varepsilon_{\mathrm{pn^-}}$ of the pn$^-$-junction, the effective area of opposed surfaces $A_{\mathrm{pn^-}}$ of the space charge region of the pn$^-$-junction and the effective width of the space charge region $w_{\mathrm{scr\,pn^-}}$.[8] $C_{\mathrm{scr\,pn^-}}$ decreases with rising drain source voltages.

[8] For silicon devices, (2.7) overestimates the capacitance, because the doping transition is usually not very abrupt [Lutz 11]. For a more exact calculation of the junction capacitance, it is referred to [Lutz 11].

Large-Signal Circuit Model of a Power MOSFET

In the considered commutation cell, these four operation conditions must be represented by the behavioral model. A turned on MOSFET is operated in the linear region and a turned off MOSFET in the blocking region. The MOSFET's $i_{\mathrm{Ch}}(v_{\mathrm{DS\,chip}}, v_{\mathrm{GS\,chip}})$ locus curves of switching operations run additionally through the non-linear and the saturation region.

For the modeling of the ***MOSFET's static behavior***, the resistance between the drain and the source terminal must be considered the behavioral model. As shown in Fig. 2.6 a), the following resistances need to be considered:[9]

- the channel resistance R_{Ch} as well as
- the source region resistance $R_{\mathrm{n^+}}$,
- the accumulation layer resistance R_{acc},
- the JFET resistance R_{JFET}, which represents the pinching of the current due to the drain source voltage dependent space charge region of the $\mathrm{pn^-}$-junction,
- the epitaxial resistance R_{epi} and
- the substrate resistance R_{sub}

(e.g. [Barkhordarian 05], [Matocha 10] and [Baliga 08]). As R_{Ch} in (2.5), the listed resistances depend on the length of the current path, the amount of carriers and their mobility. The source region resistance $R_{\mathrm{n^+}}$ and the drain region resistance R_{sub} are effectively constant. R_{acc} alters with the voltage dependent amount of carriers in the $\mathrm{n^-}$-layer beneath the oxide. R_{epi} and R_{JFET} change due to the voltage dependent width of the space charge region of the $\mathrm{pn^-}$-junction. An increasing width of the space charge region reduces the amount of carriers of the epitaxy layer which results in an increased R_{epi}. For each operating point, the resistances add up to the resistance $R_{\mathrm{DS\,chip}}$ of the behavioral model in Fig. 2.7:

$$R_{\mathrm{DS\,chip}} = R_{\mathrm{n^+}} + R_{\mathrm{Ch}} + R_{\mathrm{acc}} + R_{\mathrm{JFET}} + R_{\mathrm{epi}} + R_{\mathrm{sub}}, \tag{2.8}$$

The ***MOSFET's dynamic behavior*** is represented by the device's chip-internal capacitances that are charged and discharged during (switching) operation. As shown in Fig. 2.6 b), the following capacitances need to be considered in the behavioral model:

- the space charge region capacitance $C_{\mathrm{scr\,pn^-}}$ and
- the channel capacitance $C_{\mathrm{MOS\,p}}$, as well as
- the MOS capacitance between gate and source $C_{\mathrm{MOS\,n^+}}$,
- the MOS capacitance between drain and gate $C_{\mathrm{MOS\,n^-}}$ and
- the metal-oxide-metal capacitance between gate and source C_{MOM}.

[9] The drain and source metal-semiconductor-contacts are ohmic contacts and have a negligible junction resistance compared to the total resistance of the semiconductor device (for more details see e.g. [Sze 07]).

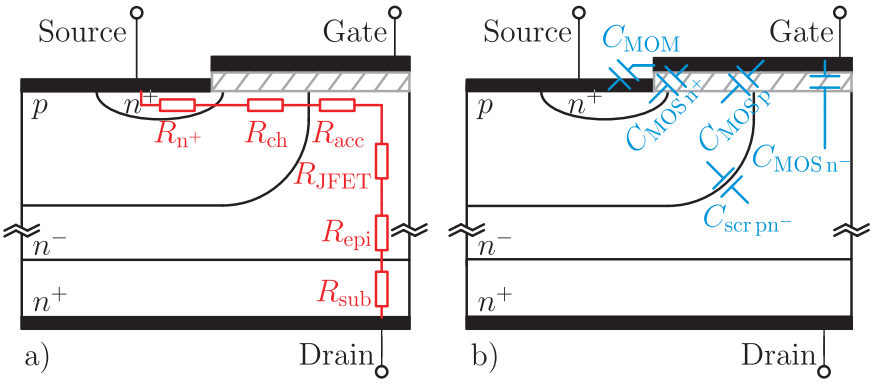


Figure 2.6: Cross section of a MOSFET cell with a) static and b) dynamic circuit elements of a MOSFET's behavioral model[10]

C_{MOM} is constant. $C_{MOS\,p}$, $C_{MOS\,n^+}$, $C_{MOS\,n^-}$ as well as $C_{scr\,pn^-}$ are voltage dependent. In circuit theory, the current i_C through a capacitance C is given by the derivation of the voltage across the capacitance $^{dv_C}/_{dt}$:

$$i_C = C \cdot {}^{dv_C}/_{dt} \tag{2.9}$$

$C_{MOS\,p}$, $C_{MOS\,n^-}$ and $C_{scr\,pn^-}$ depend on both $V_{DS\,chip}$ and $V_{GS\,chip}$. Hence, a connection of $C_{MOS\,p}$, $C_{MOS\,n^-}$ and $C_{scr\,pn^-}$ to the corresponding terminals in Fig. 2.7 would be incorrect.

The capacitances $C_{DS\,chip}$, $C_{DG\,chip}$ and $C_{GS\,chip}$ in Fig. 2.7 are represented by the charges

$$Q_{C_{DS\,chip}} = \mathbf{f}_{C_{DS\,chip}}(V_{DS\,chip}, V_{GS\,chip}, t), \tag{2.10}$$
$$Q_{C_{GS\,chip}} = \mathbf{f}_{C_{GS\,chip}}(V_{DS\,chip}, V_{GS\,chip}, t) \text{ and} \tag{2.11}$$
$$Q_{C_{DG\,chip}} = \mathbf{f}_{C_{DG\,chip}}(V_{DS\,chip}, V_{GS\,chip}, t). \tag{2.12}$$

The time-variance of the charges is assumed to be negligible. For the nonlinear, time-invariant capacitances, the corresponding currents are given by

$$i_{DS\,chip}(t) = \frac{dQ_{C_{DS\,chip}}}{dt} = \frac{\partial Q_{C_{DS\,chip}}}{\partial v_{DS\,chip}} \cdot \frac{dv_{DS\,chip}}{dt} + \frac{\partial Q_{C_{DS\,chip}}}{\partial v_{GS\,chip}} \cdot \frac{dv_{GS\,chip}}{dt}, \tag{2.13}$$
$$i_{GS\,chip}(t) = \frac{dQ_{C_{GS\,chip}}}{dt} = \frac{\partial Q_{C_{GS\,chip}}}{\partial v_{DS\,chip}} \cdot \frac{dv_{DS\,chip}}{dt} + \frac{\partial Q_{C_{GS\,chip}}}{\partial v_{GS\,chip}} \cdot \frac{dv_{GS\,chip}}{dt} \quad \text{and} \tag{2.14}$$
$$i_{DG\,chip}(t) = \frac{dQ_{C_{DG\,chip}}}{dt} = \frac{\partial Q_{C_{DG\,chip}}}{\partial v_{DS\,chip}} \cdot \frac{dv_{DS\,chip}}{dt} + \frac{\partial Q_{C_{DG\,chip}}}{\partial v_{GS\,chip}} \cdot \frac{dv_{GS\,chip}}{dt} \tag{2.15}$$

[10] The current paths from the electrodes through the semiconductor material towards the capacitances are disregarded. Thus, resistive voltage drops caused by the $^{dv}/_{dt}$ dependent charging and discharging currents of the capacitances are considered as a part of the voltage drop across the capacitances and the corresponding ohmic losses are neglected. As long as the resistive voltage drop is small compared to the voltage drop across the corresponding capacitance and as long as the ohmic losses in these resistances are small compared to the total losses of the device, this is a reasonable simplification. Continuative works could check the influence of this neglect on the capacitance determination by means of device simulations.

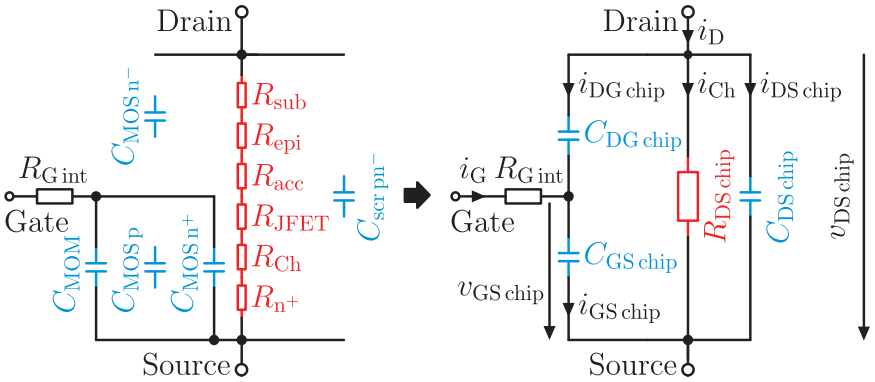


Figure 2.7: Behavioral model of a MOSFET (cp. e.g. with [Schröder 06] and [Michel 08]) - The index 'chip' is subsequently used for the equivalent circuit elements and the corresponding currents and voltages of the unpackaged transistor.

(cp. [Tsividis 11], [Lerch 07] and [Taylor 82]).

The following definitions are made:

$$C_{\mathrm{DS\,chip\,DS}} := \left.\frac{\partial Q_{C_{\mathrm{DS\,chip}}}}{\partial v_{\mathrm{DS\,chip}}}\right|_{V_{\mathrm{DS\,chip}}=v_{\mathrm{DS\,chip}}(t),\, V_{\mathrm{GS\,chip}}=v_{\mathrm{GS\,chip}}(t)} \tag{2.16}$$

$$C_{\mathrm{DS\,chip\,GS}} := \left.\frac{\partial Q_{C_{\mathrm{DS\,chip}}}}{\partial v_{\mathrm{GS\,chip}}}\right|_{V_{\mathrm{DS\,chip}}=v_{\mathrm{DS\,chip}}(t),\, V_{\mathrm{GS\,chip}}=v_{\mathrm{GS\,chip}}(t)} \tag{2.17}$$

$$C_{\mathrm{GS\,chip\,DS}} := \left.\frac{\partial Q_{C_{\mathrm{GS\,chip}}}}{\partial v_{\mathrm{DS\,chip}}}\right|_{V_{\mathrm{DS\,chip}}=v_{\mathrm{DS\,chip}}(t),\, V_{\mathrm{GS\,chip}}=v_{\mathrm{GS\,chip}}(t)} \tag{2.18}$$

$$C_{\mathrm{GS\,chip\,GS}} := \left.\frac{\partial Q_{C_{\mathrm{GS\,chip}}}}{\partial v_{\mathrm{GS\,chip}}}\right|_{V_{\mathrm{DS\,chip}}=v_{\mathrm{DS\,chip}}(t),\, V_{\mathrm{GS\,chip}}=v_{\mathrm{GS\,chip}}(t)} \tag{2.19}$$

$$C_{\mathrm{DG\,chip\,DS}} := \left.\frac{\partial Q_{C_{\mathrm{DG\,chip}}}}{\partial v_{\mathrm{DS\,chip}}}\right|_{V_{\mathrm{DS\,chip}}=v_{\mathrm{DS\,chip}}(t),\, V_{\mathrm{GS\,chip}}=v_{\mathrm{GS\,chip}}(t)} \tag{2.20}$$

$$C_{\mathrm{DG\,chip\,GS}} := \left.\frac{\partial Q_{C_{\mathrm{DG\,chip}}}}{\partial v_{\mathrm{GS\,chip}}}\right|_{V_{\mathrm{DS\,chip}}=v_{\mathrm{DS\,chip}}(t),\, V_{\mathrm{GS\,chip}}=v_{\mathrm{GS\,chip}}(t)} \tag{2.21}$$

Accordingly, (2.13) through (2.15) can be written as

$$i_{\mathrm{DS\,chip}}(t) = C_{\mathrm{DS\,chip\,DS}} \cdot \frac{\mathrm{d}v_{\mathrm{DS\,chip}}}{\mathrm{d}t} + C_{\mathrm{DS\,chip\,GS}} \cdot \frac{\mathrm{d}v_{\mathrm{GS\,chip}}}{\mathrm{d}t}, \tag{2.22}$$

$$i_{\mathrm{GS\,chip}}(t) = C_{\mathrm{GS\,chip\,DS}} \cdot \frac{\mathrm{d}v_{\mathrm{DS\,chip}}}{\mathrm{d}t} + C_{\mathrm{GS\,chip\,GS}} \cdot \frac{\mathrm{d}v_{\mathrm{GS\,chip}}}{\mathrm{d}t} \text{ and} \tag{2.23}$$

$$i_{\mathrm{DG\,chip}}(t) = C_{\mathrm{DG\,chip\,DS}} \cdot \frac{\mathrm{d}v_{\mathrm{DS\,chip}}}{\mathrm{d}t} + C_{\mathrm{DG\,chip\,GS}} \cdot \frac{\mathrm{d}v_{\mathrm{GS\,chip}}}{\mathrm{d}t}. \tag{2.24}$$

In accordance with (2.9), the currents through $C_{\mathrm{DS\,chip}}$, $C_{\mathrm{DG\,chip}}$ and $C_{\mathrm{GS\,chip}}$ of the behavioral

model in Fig. 2.7 are given by

$$i_{\mathrm{DS\,chip}}(t) = C_{\mathrm{DS\,chip}} \cdot \frac{\mathrm{d}v_{\mathrm{DS\,chip}}}{\mathrm{d}t}, \tag{2.25}$$

$$i_{\mathrm{GS\,chip}}(t) = C_{\mathrm{GS\,chip}} \cdot \frac{\mathrm{d}v_{\mathrm{GS\,chip}}}{\mathrm{d}t} \text{ and} \tag{2.26}$$

$$i_{\mathrm{DG\,chip}}(t) = C_{\mathrm{DG\,chip}} \cdot \frac{\mathrm{d}v_{\mathrm{DG\,chip}}}{\mathrm{d}t}. \tag{2.27}$$

The comparison of equation (2.22) through (2.24) with equation (2.25) through (2.27), results for each operating point in

$$C_{\mathrm{DS\,chip}} := C_{\mathrm{DS\,chip\,DS}} + C_{\mathrm{DS\,chip\,GS}} \cdot \frac{\mathrm{d}v_{\mathrm{GS\,chip}}}{\mathrm{d}v_{\mathrm{DS\,chip}}} \text{ with } \Delta v_{\mathrm{DS\,chip}} \neq 0, \tag{2.28}$$

$$C_{\mathrm{GS\,chip}} := C_{\mathrm{GS\,chip\,DS}} \cdot \frac{\mathrm{d}v_{\mathrm{DS\,chip}}}{\mathrm{d}v_{\mathrm{GS\,chip}}} + C_{\mathrm{GS\,chip\,GS}} \text{ with } \Delta v_{\mathrm{GS\,chip}} \neq 0 \text{ and} \tag{2.29}$$

$$C_{\mathrm{DG\,chip}} := C_{\mathrm{DG\,chip\,DS}} \cdot \frac{\mathrm{d}v_{\mathrm{DS\,chip}}}{\mathrm{d}v_{\mathrm{DG\,chip}}} + C_{\mathrm{DG\,chip\,GS}} \cdot \frac{\mathrm{d}v_{\mathrm{GS\,chip}}}{\mathrm{d}v_{\mathrm{DG\,chip}}} \text{ with } \Delta v_{\mathrm{DG\,chip}} \neq 0. \tag{2.30}$$

Accordingly, the characteristics $C_{\mathrm{ds\,chip}}(V_{\mathrm{DS\,chip}})$, $C_{\mathrm{gs\,chip}}(V_{\mathrm{GS\,chip}})$ as well as $C_{\mathrm{dg\,chip}}(V_{\mathrm{DG\,chip}})$ can depend on the operating conditions and the parasitic environment.[11] The stronger the variation of the model capacitances is, the more the measurement simulation conformance depends on the constitutive dynamic measurement (cp. [Agi 08]).

The proposed behavioral model in Fig. 2.7 contains the same 'elements' as the physical MOSFET model in [Kraus 96]. Additionally, an integrated gate resistance $R_{\mathrm{G\,int}}$ is considered. The model combines the device's numerous MOSFET cells to an equivalent MOSFET cell. Therefore, the model can only be applied if gate voltage propagation delays and the resulting inhomogeneous current distribution between the MOSFET cells are not of interest (see e.g. [Mawanda-Kibuule 87]). In this work, the impact of the gate voltage propagation delay on the switching characteristics is not considered.

2.2.2.2 SJ Power MOSFETs

For conventional high voltage power MOSFETs, the on-resistance is dominated by the drift region resistance R_{epi} [Lorenz 99], which is given by

$$R_{\mathrm{epi}} = \frac{t_{\mathrm{epi}}}{q \cdot \mu_{\mathrm{e}} \cdot N_D \cdot A_{\mathrm{act}}} \tag{2.31}$$

with the thickness of the epitaxial layer t_{epi}, the donor concentration N_D in the epitaxial layer and the active area of the chip A_{act} [Lutz 11]. For higher breakdown voltages V_{br}, t_{epi}

[11] On page 48 et seq., the model capacitances are determined from dynamic measurement data. The DUT's $C_{\mathrm{ds\,chip}}(V_{\mathrm{DS\,chip}})$ depends strongly on the operating conditions (see Fig. 2.29 on page 59).

is increased and N_D is decreased respectively. According to [Lutz 11], the lowest R_{epi} of a conventional power MOSFET is given by

$$R_{\mathrm{epi\,min}} = 0.9 \cdot \frac{2 \cdot B^{0.5} \cdot V_{\mathrm{br}}^{2.5}}{\mu_{\mathrm{e}} \cdot \varepsilon_0 \cdot \varepsilon_{\mathrm{n^-}} \cdot A_{\mathrm{act}}}. \tag{2.32}$$

with the FULOP constant B.[12] (2.32) and similar equations (see e.g. [Hu 79]) show $R_{\mathrm{epi}} \propto V_{\mathrm{br}}^{2.4\,..\,2.6}$ and are known in literature as silicon or unipolar limit. The compensation principle can overcome this limitation.

Charge Compensation Principle

The charge compensation principle is patented in [Chen 93]. According to [Deboy 04], SJ MOSFETs are based on the reduced surface field (RESURF) ideas of lateral semiconductor devices (see e.g. [Appels 79] and [Ludikhuize 00]). Compared to a conventional power MOSFET, the area-specific on-resistance is significantly reduced in SJ power MOSFETs due to p-columns, which are implemented into the drift region (see Fig. 2.8). According to [Silber 09], the super junction structure must fulfill the following conditions:

- ***Aspect Ratio:*** The n-column width is smaller than the column length.
- ***Compensation:*** The charges in the space charge regions in the n-columns are compensated by the charges in the space charge regions the p-columns.
- ***Limited Column Width or Doping:*** The integral of the space charge in y direction remains smaller than the material specific breakthrough charge.

With a SJ structure, as shown in Fig. 2.8, a horizontal field distribution can be achieved across the epitaxy layer. This results in a nearly linear relationship between the breakdown voltage V_{br} and the epitaxial resistance R_{epi} (see e.g. [Deboy 98], [Inf 08a] and [Lutz 11]). The compensation principle allows the increase of the doping of the n-columns inverse proportional to their width and thus, theoretically, a further reduction of area-specific resistance of the epitaxial layer [Fujihira 97]. However, without further semiconductor technology achievements, the reduction of R_{epi} is limited (for details, see e.g. [Kondekar 06]).

Comparison of Conventional and SJ Power MOSFETs

The operating modes and characteristics of SJ power MOSFETs are discussed in detail in [Lagies 01a] and [Lagies 01b]. Information on specific characteristics of SJ power MOSFETs can e.g. also be found in [Deboy 04]. Subsequently, a summary of the findings is given:

(I) For a given breakdown voltage, the SJ structure leads to the following differences in the ***static characteristics*** of conventional and SJ power MOSFETs:

[12] Information on the FULOP constant can be found in [Schröder 06]. For more details, see [Fulop 67].

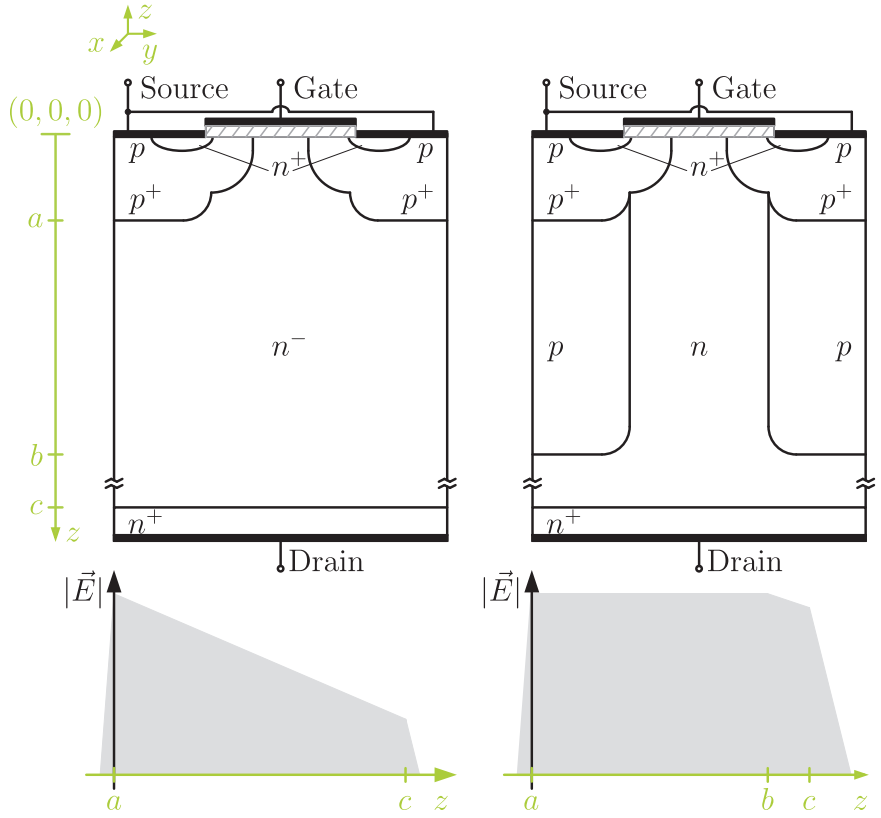


Figure 2.8: Comparison of a conventional power MOSFET (left) and a SJ power MOSFET (right) (cp. with [Lutz 11])

- For relatively small drain source voltages, the area-specific on-resistance of a SJ MOSFET is smaller than the area-specific on-resistance of a conventional MOSFETs.
- In conventional MOSFETs, the MOS channel resistance limits the current in the saturation region. When the quasi-saturation gate source voltage $V_{\mathrm{GS\,QS}}$ and the punch-through drain source voltage $V_{\mathrm{DS\,PT}}$ are reached,[13] the current in a SJ MOSFET is limited by the resistance of the current channel between the space charge regions of the SJ structure. As in [Lagies 01a], in **2.4.1.3** on page 55 et seq., this region is referred to as 'drain channel' and 'drain channel resistance' respectively.
- A conventional MOSFET shows a relatively low current increase in the saturation region, because the voltage across the remaining channel is almost constant for increasing drain source voltages. When the gate source voltage $V_{\mathrm{GS\,QS}}$ and drain source voltage $V_{\mathrm{DS\,PT}}$ are reached, the current increase in the saturation region of a SJ MOSFET is higher because the voltage across the current channel through the space charge regions of the pn-junctions of the columns keeps increasing.

[13] The space charge regions of the pn-junctions can not expand over half the width of the n columns. According to [Lagies 01a], a current channel remains between the space charge regions for $V_{\mathrm{GS}} > V_{\mathrm{th}}$. The current is not pinched-off as in JFETs. The drain source voltage for which the maximum space charge region width is reached (at one point in the n-column) is called punch-through voltage.

The reduction of the area-specific on-resistance $R_{\mathrm{DS\,chip\,on}}$ in SJ power MOSFETs, enables a chip area shrink, which has also an impact on the dynamic characteristics.

(II) For a given breakdown voltage, the SJ structure leads to the following differences between the ***dynamic characteristics*** of conventional and SJ power MOSFETs:

- Due to the enabled chip area shrink, the gate source capacitance of a SJ MOSFET is usually smaller than the gate source capacitance of a conventional power MOSFET.
- Due to implemented p-columns, the effective area of space charge region of the pn-junctions is increased significantly for the drain source voltages below $V_{\mathrm{DS\,PT}}$ and the drain source capacitance is relatively high. Above $V_{\mathrm{DS\,PT}}$, the space charge region expands only vertically and the drain source capacitances decreases significantly. Due to the enabled chip area shrink, the drain source capacitance of SJ power MOSFETs is usually larger for drain source voltages below $V_{\mathrm{DS\,PT}}$ and smaller for voltages above $V_{\mathrm{DS\,PT}}$ than the drain source capacitance of a conventional power MOSFET.
- The drain gate capacitance of a SJ MOSFET is also strongly non-linear because the space charge region expansion between the columns and the resulting reduction of the effective drain gate area overlap. For a certain voltage range above $V_{\mathrm{DS\,PT}}$, the effective drain gate area overlap and thus the drain gate capacitance increases. Due to the enabled chip shrink, the drain gate capacitance of a SJ power MOSFET is usually smaller than the drain gate capacitance of a conventional power MOSFET.

Impact of the SJ Structure on the Behavioral Modeling

The comparison of conventional and SJ power MOSFETs shows that their static and dynamic characteristics differ considerably. However, the differences in the characteristics can be represented by an accordant parameterization of $R_{\mathrm{DS\,chip}}$, $C_{\mathrm{ds\,chip}}$, $C_{\mathrm{dg\,chip}}$ and $C_{\mathrm{gs\,chip}}$ of the power MOSFET behavioral model in Fig. 2.7 on page 19. For the identified specifics, an adoption of the power MOSFET behavioral model is hence not necessary.

2.2.3 Behavioral Model for Schottky Diodes

Considered Conditions of Operation of the Schottky Diode

The basic structure of a SCHOTTKY diode is depicted in Fig. 2.9. The SCHOTTKY contact has a current voltage characteristic $I_{\mathrm{MS}}(V_{\mathrm{AC\,chip}})$ that is described with

$$I_{\mathrm{MS}}(V_{\mathrm{AC\,chip}}) = I_{\mathrm{MS\,sat}} \cdot \left(\mathrm{e}^{\frac{q \cdot V_{\mathrm{AC\,chip}}}{\mathrm{k} \cdot T_{\mathrm{J}}}} - 1 \right) \tag{2.33}$$

with the saturation current

$$I_{\mathrm{MS\,sat}} = A^* \cdot {T_{\mathrm{J}}}^2 \cdot \mathrm{e}^{-\frac{q \cdot \phi_{\mathrm{bn}}}{\mathrm{k} \cdot T_{\mathrm{J}}}}, \tag{2.34}$$

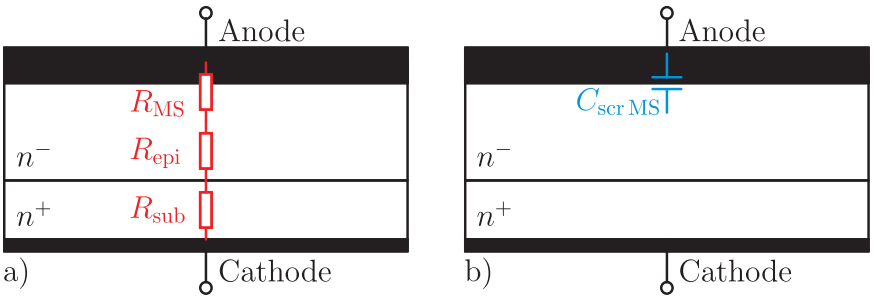


Figure 2.9: Cross section of a SCHOTTKY diode with a) static and b) dynamic circuit elements of the behavioral model (e.g. [Singh 00])[10]

the electron charge q, the BOLTZMANN constant k, the absolute junction temperature T_J, the effective RICHARDSON constant A^* and the barrier height between metal and semiconductor ϕ_{bn} (see e.g. [Lutz 06]).[14] The characteristic $I_{MS}(V_{AC\,chip})$ represents a voltage dependent junction resistance $R_{MS}(V_{AC\,chip})$. For positive junction voltages $V_{AC\,chip}$ above the threshold voltage, the junction current I_{MS} increases exponentially. The junction resistance becomes relatively small and the diode is conducting. For junction voltages beneath the threshold voltage, only a leakage current flows. The junction resistance is very high and the diode is blocked. $I_{MS}(V_{AC\,chip})$ characteristics of a SCHOTTKY diode are shown in Fig. 2.10.

In case the SCHOTTKY junction is blocked, a voltage dependent space charge region exists beneath the junction. According to [Lutz 11], for very abrupt junctions, the depletion capacitance $C_{scr\,MS}$ is given by

$$C_{scr\,MS}(V_{AC\,chip}) = \varepsilon_0 \cdot \varepsilon_{n^-} \cdot \frac{A_{MS}}{w_{scr\,MS}(V_{AC\,chip})} \tag{2.35}$$

with the semiconductor's effective relative permittivity ε_{n^-}, the effective area of the opposed metal and semiconductor surfaces A_{MS} and the width of the space charge region $w_{scr\,MS}$. For increasing reverse voltages, the space charge region widens and therefore, $C_{scr\,MS}$ diminishes. Positive anode cathode voltages minimize the space charge region's width $w_{scr\,MS}$ and maximize the capacitance $C_{scr\,MS}$ (see e.g. [Sze 07] for more details).

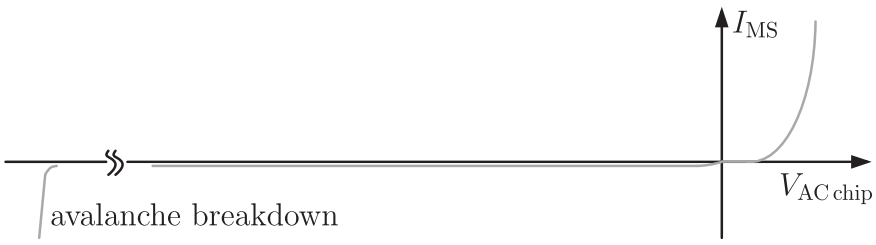


Figure 2.10: Current-voltage characteristics of a SCHOTTKY diode

[14] For the derivation of (2.33), see e.g. [Schröder 06]. Information on the RICHARDSON constant can be found in [Schröder 06]. For more details, see [Richardson 03].

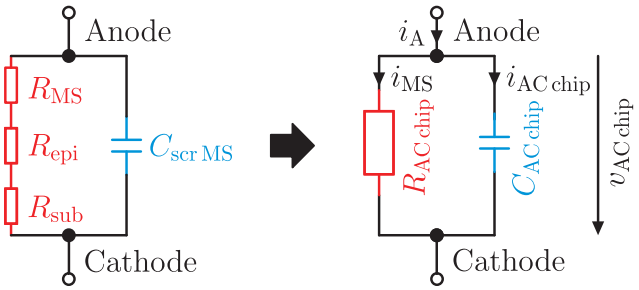


Figure 2.11: Behavioral model of a SCHOTTKY diode (cp. e.g. with [Funaki 08]) - The index 'chip' is subsequently used for the equivalent circuit elements and the corresponding voltage and currents of the unpackaged diode.

Large-Signal Circuit Model of a Schottky Diode

For the modeling of the ***Schottky diode's static behavior***, the resistance between the anode and the cathode terminal needs to be part of the behavioral model. As shown in Fig. 2.9 a), the following resistances are considered:

- the junction resistance R_{MS}
- the epitaxial resistance R_{epi} and
- the cathode region resistance R_{sub}

(cp. [Zhang 06]). As R_{Ch} in (2.5), the resistances depend on the length of the current path, the amount of carriers and their mobility. While R_{sub} is almost constant for non punch-through diodes, an increasing reverse voltage (a widening space charge region width) results in an increasing R_{epi} due to the reduction of carriers in this region. For each operating point, the resistances add up to the resistance $R_{\mathrm{AC\,chip}}$ of the behavioral model in Fig. 2.11:

$$R_{\mathrm{AC\,chip}} = R_{\mathrm{MS}} + R_{\mathrm{epi}} + R_{\mathrm{sub}} \tag{2.36}$$

The ***Schottky diode's dynamic behavior*** is represented by internal capacitances. As shown in Fig. 2.9 b), the voltage dependent capacitance $C_{\mathrm{scr\,MS}}$ of the space charge region is considered in the behavioral model.[15] For each operating point, the interelectrode capacitance $C_{\mathrm{AC\,chip}}$ of the behavioral model in Fig. 2.11 is given by:

$$C_{\mathrm{AC\,chip}} = C_{\mathrm{scr\,MS}}. \tag{2.37}$$

[15] A SCHOTTKY diode is a majority carrier device. Thus, contrary to pn and pin diodes, SCHOTTKY diodes have only of the depletion capacitance $C_{\mathrm{scr\,MS}}$ and no diffusion capacitance.

2.3 Determination of the Static Parameters of the Behavioral Models

Current voltage characteristics of the MOSFET and the SCHOTTKY diode are needed for the static parameterization of the operating point dependent resistances $R_{\mathrm{DS\,chip}}$ and $R_{\mathrm{AC\,chip}}$ of the behavioral models in Fig. 2.7 on page 19 and Fig. 2.11. For an optimized accuracy of the static characteristics, it must be ensured that ...

- ... the current through the device under test (DUT) is as constant as possible in the metering interval. Otherwise, voltage drops across parasitic inductances between semiconductor chip and probing points of the voltage measurements cause differences between measured voltages and chip voltages (see Fig. 3.9 on page 83).

- ... the voltage probing points are placed as close as possible to the DUT. This requirement reduces the differences between measured voltages and chip voltages due to parasitic equivalent circuit elements between chip and probing points.

- ... the voltages across the DUT are as constant as possible in the metering interval. Otherwise, currents through capacitances of the semiconductor chip and parasitic capacitances of the DUT's package and the used measurement setup cause alterations from the aimed static current (see Fig. 3.8 on page 81).

- ... the current probes are placed as close as possible to the DUT and are exposed as less as possible to voltage alterations during the measurement. This requirement reduces the differences between measured currents and currents that flow into the semiconductor chip. The differences are due to the charging of parasitic capacitances connected to the current path between the DUT and the placement of current probe.

- ... the measured voltages and currents are acquired from sufficiently short and sufficiently spaced pulses (see e.g. [Parker 95] and [Jenkins 95]). This approach ensures a relatively small self-heating during the static measurements and the same initial junction temperature for every measurement pulse.

- ... the operating range is characterized with a sufficient resolution.

Considering these requirements, the determination of temperature dependent current voltage characteristics of a 600 V super junction MOSFET and of a 600 V SiC SCHOTTKY diode are presented in subsection **2.3.1** and **2.3.2**. The MOSFET's static characteristics is are not only needed for the simulation of switching characteristics in section **4.1** on page 95 et seq. and in section **5.4** on page 156 et seq., and the stability analysis in chapter **5** on page 111 et seq. but also for the MOSFET's dynamic parameterization in subsection **2.4.1** on page 48 et seq.. The diode's static characteristics are needed for simulations of switching characteristics. The described static measurements are not limited to the considered DUTs but are applicable to any SCHOTTKY diode and any MOSFET as long as the devices' self-heating is within acceptable limits for the analyzed operating range.

2.3.1 Static Characterization of Power MOSFETs

The output characteristics $I_{\mathrm{Ch}}(V_{\mathrm{DS\,chip}},\, V_{\mathrm{GS\,chip}},\, T_{\mathrm{J}})$ represent with

$$R_{\mathrm{DS\,chip}}(V_{\mathrm{DS\,chip}},\, V_{\mathrm{GS\,chip}},\, T_{\mathrm{J}}) = \frac{I_{\mathrm{Ch}}(V_{\mathrm{DS\,chip}},\, V_{\mathrm{GS\,chip}},\, T_{\mathrm{J}})}{V_{\mathrm{DS\,chip}}} \tag{2.38}$$

the temperature dependent static behavior of a MOSFET. In this work, an operating range of $0\,\mathrm{A} \leq I_{\mathrm{Ch}} \leq 20\,\mathrm{A}$ and $0\,\mathrm{V} \leq V_{\mathrm{DS\,chip}} \leq 450\,\mathrm{V}$ is considered. In **2.3.1.1**, the curve tracer measurement of output characteristics is discussed. The measurement of transfer characteristics at higher drain source voltages is investigated in **2.3.1.2**. In **2.3.1.3**, both measurements are combined to output characteristics that cover the considered operating range. Systematic error sources of the static characterization and their impact on the measurement results are discussed in **2.3.1.4**.

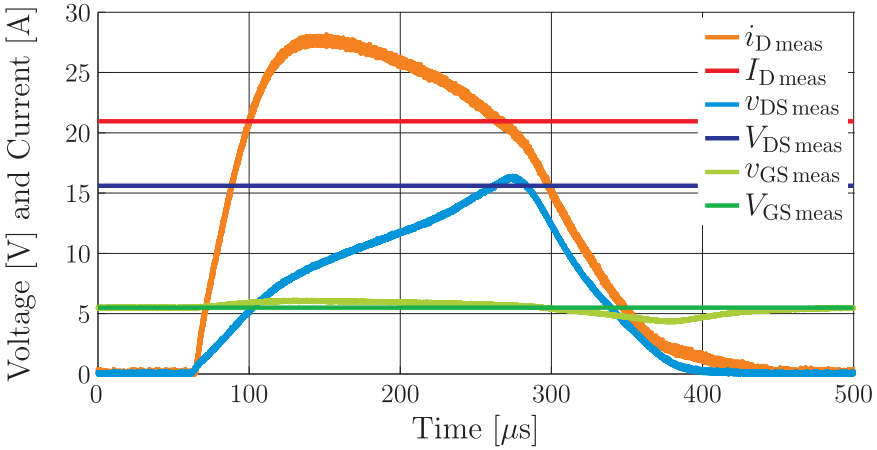
2.3.1.1 Curve Tracer Output Characteristics

For the measurement of output characteristics, the curve tracer applies different drain source and gate sources voltages to the DUT. The used curve tracer has a fixed pulse width t_{pu} of approximately $250\,\mu\mathrm{s}$. The maximum drain source voltage supply in high current mode ($i \gg 40\,\mathrm{mA}$) is approximately $30\,\mathrm{V}$ [Tek 96]. Hence, $I_{\mathrm{Ch}}(V_{\mathrm{DS\,chip}} = 30\,\mathrm{V},\ V_{\mathrm{GS\,chip}}) = 20\,\mathrm{A}$ is the most lossy point of the operating range of interest that can be measured. For a $250\,\mu\mathrm{s}$ pulse, a duty cycle of zero and $\vartheta_{\mathrm{J}} = 25\,^{\circ}\mathrm{C}$, this point is within the save operating area [Inf 07b]. A suitable gate resistance $R_{\mathrm{G\,ext}}$ needs to be chosen for the measurements. As shown in Fig. 2.12, $R_{\mathrm{G\,ext}}$ must be high enough to prevent parasitic oscillations and low enough to ensure the static operation in the metering interval. The initial junction temperature of the measurement can be adjusted with a heating plate.

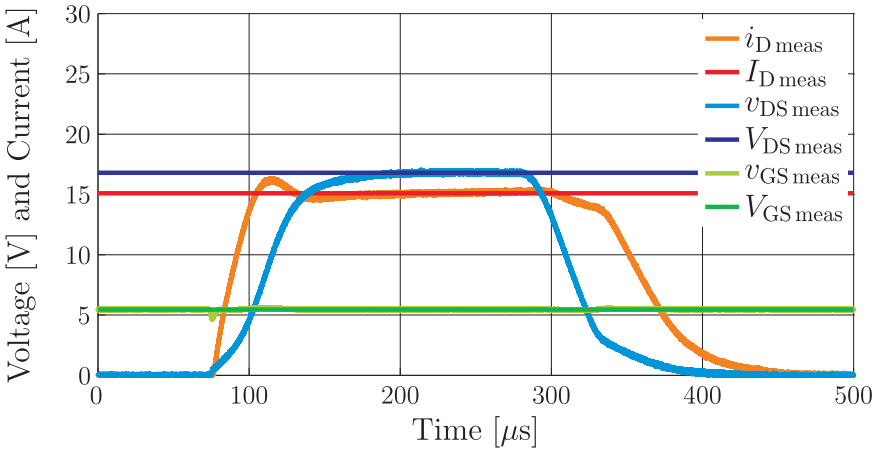
For the aimed oscillation analysis, a relatively high resolution of the output characteristics is required. The curve tracer provides a mode that enables the simultaneous sweeping of $I_{\mathrm{Ch}}(V_{\mathrm{DS\,meas}})$ characteristics for up to ten gate source voltages. However, this mode is not convenient because of the suboptimal resolution of the characteristics with lower gate source voltages and a relatively high self-heating of the DUT due to the relatively short pulse repetition time and the relatively long pulse width. Therefore, instead of the sweeping mode, a sequence of single pulses is recommended for the measurement. Even though, the pulse width is often fixed, the pulse repetition time $\mathcal{T}_{\mathrm{pu}}$ can be defined with a programmed break between single pulses. Due to the dependency of the effective transient thermal junction case impedance $Z_{th\,\mathrm{JC}}$ on the duty cycle $\mathrm{D} = {}^{t_{\mathrm{pu}}}/_{\mathcal{T}_{\mathrm{pu}}}$, and due to the dependency of average power P_{avg} on $\mathcal{T}_{\mathrm{pu}}$, the user can influence both $T_{\mathrm{J\,max}}$ and $T_{\mathrm{J\,avg}}$. The maximum junction temperature at the end of a relatively long power pulse ($>100\,\mu\mathrm{s}$) is roughly given by

$$T_{\mathrm{J\,max}} = T_{\mathrm{C}} + P_{\mathrm{pu}} \cdot Z_{th\,\mathrm{JC}} \tag{2.39}$$

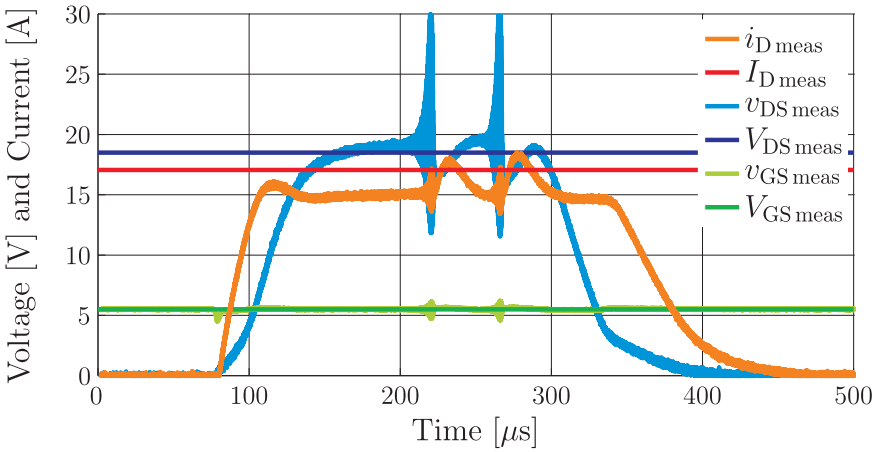
with the case temperature T_{C} and the average power during the measurement pulse P_{pu}



(a) If $R_{\mathrm{G\,ext}}$ is too high (here: $R_{\mathrm{G\,ext}} = 10\,\mathrm{k\Omega}$), the aimed operating points may not be reached.



(b) If a suitable $R_{\mathrm{G\,ext}}$ is used (here: $R_{\mathrm{G\,ext}} = 100\,\Omega$), the static operation is enabled and accurate operating points are measured.



(c) If $R_{\mathrm{G\,ext}}$ is too low (here: $R_{\mathrm{G\,ext}} = 10\,\Omega$), parasitic oscillations may occur which might result in incorrect operating points.

Figure 2.12: Impact of the serial gate resistance $R_{\mathrm{G\,ext}}$ on the determined operating point

(e.g. [Nicolai 98]).[16] The average junction temperature during a single pulse cycle roughly indicates the initial junction temperature of the next pulse and can be calculated with

$$T_{\mathrm{J\,avg}} = T_{\mathrm{C}} + P_{\mathrm{avg}} \cdot R_{th\,\mathrm{JC}} \tag{2.40}$$

with the thermal junction case resistance $R_{th\,\mathrm{JC}}$ of the DUT (e.g. [Nicolai 98]).[16]

According to the DUT's application note [Inf 07b], the maximum thermal resistance $R_{th\,\mathrm{JC}}$ equals $0.9\,^{K}/\mathrm{W}$. With $t_{\mathrm{pu}} = 250\,\mu\mathrm{s}$ and $\mathcal{T}_{\mathrm{pu}} = 1\,\mathrm{s}$, the implemented duty cycle is approximately zero. The corresponding maximum transient thermal impedance $Z_{th\,\mathrm{JC}}$ is $0.125\,^{K}/\mathrm{W}$ [Inf 07b]. For $I_{\mathrm{Ch}} = 20\,\mathrm{A}$ and $V_{\mathrm{DS\,chip}} = 30\,\mathrm{V}$, the DUT's self-heating is characterized by

$$\Delta T_{\mathrm{J\,max}} = T_{\mathrm{J\,max}} - T_{\mathrm{C}} = P_{\mathrm{pu}} \cdot Z_{th\,\mathrm{JC}} = 20\,\mathrm{A} \cdot 30\,\mathrm{V} \cdot 0.125\,^{K}/\mathrm{W} = 75\,\mathrm{K} \text{ and}$$
$$\Delta T_{\mathrm{J\,avg}} = T_{\mathrm{J\,avg}} - T_{\mathrm{C}} = P_{\mathrm{avg}} \cdot R_{th\,\mathrm{JC}} = \frac{20\,\mathrm{A} \cdot 30\,\mathrm{V} \cdot 250\,\mu\mathrm{s}}{1\,\mathrm{s}} \cdot 0.9\,^{K}/\mathrm{W} = 0.135\,\mathrm{K}.$$

The previous calculation shows that $\mathcal{T}_{\mathrm{pu}} = 1\,\mathrm{s}$ limits the self-heating significantly. The calculation of $\Delta T_{\mathrm{J\,max}}$ is confirmed by the simulation results in Fig. 2.13.[17]

The measurement of curve tracer output characteristics of the DUT in Fig. 2.14 was based on these considerations. For a further reduced self-heating, the measurement range was limited to $0\,\mathrm{V} \leq V_{\mathrm{DS\,chip}} \leq 15\,\mathrm{V}$. The used measurement routine is based on the routine for curve tracer output characteristics in [Brocke 10]. The measurement program ...

- ... allows the alteration of the pulse repetition time.
- ... enables the definition of the maximum drain current and drain source voltage, and prevents the exceedance of these values.
- ... enables the measurement of specific gate source voltages and the measurement of gate source voltage ranges and increments.
- ... ensures that the output characteristics are subsequently measured and in ascending order with respect of the applied gate source voltages.
- ... ensures a longer break between the measurement of two output characteristics.[18]
- ... ensures the highest possible resolution for each operating point.
- ... saves of the measured currents and voltages for further processing.

[16] The equation assumes a constant case temperature T_{C}.
[17] The simulation was done by *A. Willmeroth* from *Infineon Technologies*.
[18] The self-heating of the DUT increases at the end of an output characteristic. A longer hold time reduces the self-heating during the entire measurement [Agi 10b].

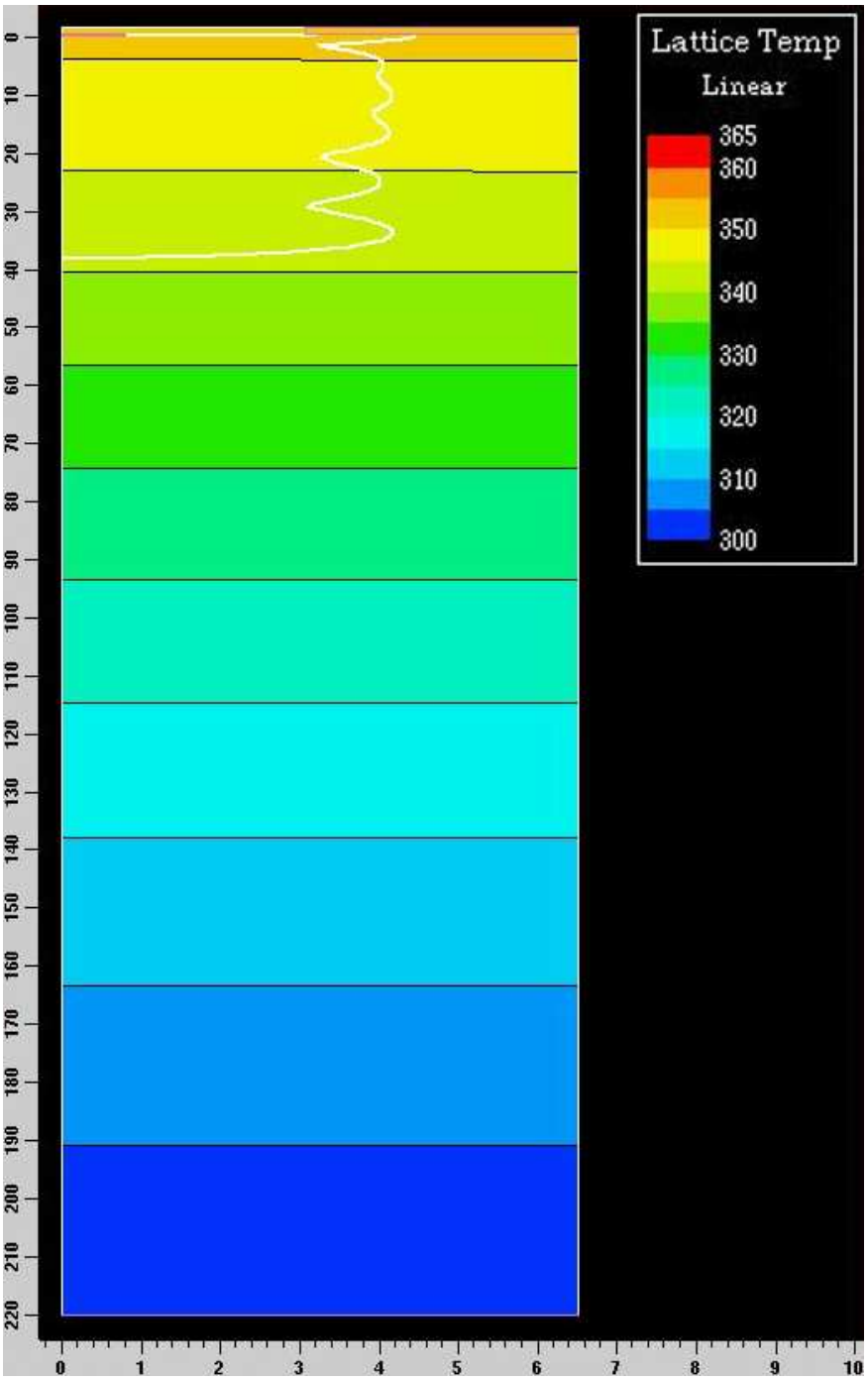
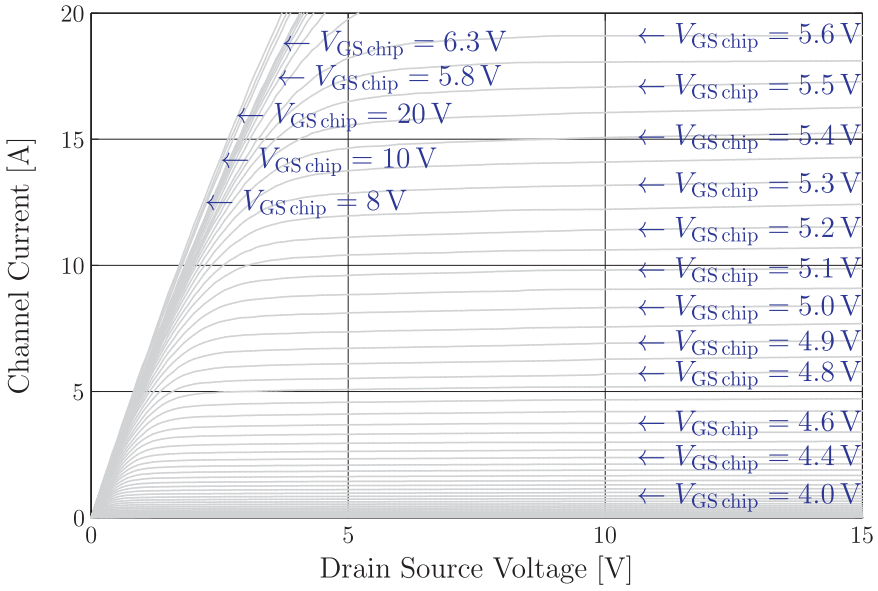
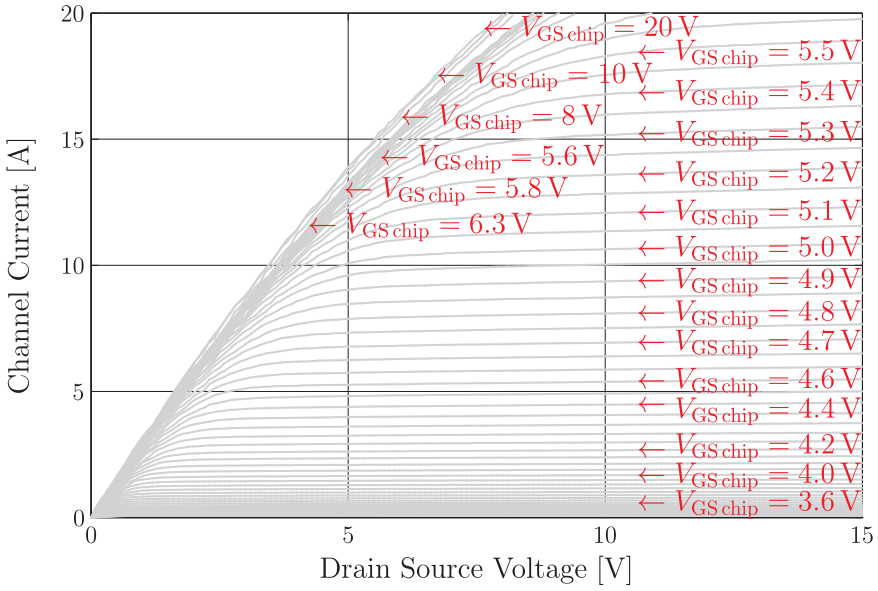


Figure 2.13: *Medici* simulation of the temperature distribution in the SJ MOSFET cell at the end of a single pulse measurement with $t_{\mathrm{pu}} = 250\,\mu\mathrm{s}$, $V_{\mathrm{DS\,chip}} = 400\,\mathrm{V}$, $I_{\mathrm{Ch}} = 20\,\mathrm{A}$ and a constant temperature of 300 K at the backside of the chip (temperature in $[K]$ and geometric data in $[\mu m]$)



(a) Output characteristics with $\vartheta_J = 25\,°C$



(b) Output characteristics with $\vartheta_J = 125\,°C$

Figure 2.14: Output characteristics of the 600 V SJ MOSFET

2.3.1.2 High Voltage Transfer Characteristics

For increasing drain source voltages (and high channel currents), the self-heating of the DUT rises significantly. For the measurement of high voltage transfer characteristics, the pulse length is hence reduced to $t_{\mathrm{pu}} = 10\,\mu\mathrm{s}$. For such a small pulse length, the maximum junction temperature $T_{\mathrm{J\,max}}$ is usually significantly overestimated by (2.39) on page 27. A volume-based calculation, which is based on the assumption that no heat is dissipated through conductance, radiation and convection to the chip's ambiance during relatively short pulses (cp. e.g. [Dyn 02]), results in a better estimation of maximum junction temperature.

The thermal energy $\mathcal{Q}_{\mathrm{pu}}$ during a short circuit measurement can be approximated with

$$\mathcal{Q}_{\mathrm{pu}} = P_{\mathrm{pu}} \cdot t_{\mathrm{pu}} = V_{\mathrm{DS\,chip}} \cdot I_{\mathrm{Ch}} \cdot t_{\mathrm{pu}} \tag{2.41}$$

(e.g. [Stöcker 07]). The thermal energy is also given by

$$\mathcal{Q}_{\mathrm{pu}} = \mathrm{c}_{\mathrm{Si}} \cdot m_{\mathrm{Si}} \cdot \Delta T_{\mathrm{pu}} \tag{2.42}$$

with the temperature rise during the measurement ΔT_{pu}, the specific heat capacity of silicon $\mathrm{c}_{\mathrm{Si}} = 703\,{}^{J}/_{\mathrm{kg\cdot K}}$, and silicon chip's mass m_{Si} (e.g. [Stöcker 07]). The mass m_{Si} equals

$$m_{\mathrm{Si}} = V_{\mathrm{Si}} \cdot \varrho_{\mathrm{Si}} \tag{2.43}$$

with the density of silicon $\varrho_{\mathrm{Si}} = 2.336\,{}^{g}/_{\mathrm{cm}^3}$, and the volume of the silicon chip V_{Si}. The maximum temperature rise is therewith given by

$$\Delta T_{\mathrm{J\,max}} = \Delta T_{\mathrm{pu}} = \frac{P_{\mathrm{pu}} \cdot t_{\mathrm{pu}}}{\mathrm{c}_{\mathrm{Si}} \cdot V_{\mathrm{Si}} \cdot \varrho_{\mathrm{Si}}}. \tag{2.44}$$

The highest dissipation losses occur if the DUT is operated in the upper limits of the considered operating range. According to *Infineon Technologies*, the DUT's chip volume approximately equals $3.78\,\mathrm{mm}^3$. As shown in Fig. 2.15, the heat is mainly generated in the DUT's n-type columns and disperses even in horizontal direction within the n- and p-type columns during a $10\,\mu\mathrm{s}$ pulse. Considering the DUT's specific column depth and its active chip area, the effectively heated silicon volume during the measurement is estimated with $0.76\,\mathrm{mm}^3$. Thus, the maximum temperature rise can approximately be calculated with

$$\Delta T_{\mathrm{J\,max}} = \frac{20\,\mathrm{A} \cdot 450\,\mathrm{V} \cdot 10\,\mu\mathrm{s}}{703\,{}^{J}/_{\mathrm{kg\cdot K}} \cdot 0.00076\,\mathrm{cm}^3 \cdot 2.336 \cdot 10^{-3}\,{}^{kg}/_{\mathrm{cm}^3}} \approx 72\,\mathrm{K},$$

which corresponds well with the result in Fig. 2.15.[17] According to the previous calculation, the considered operating range can be characterized without destroying the DUT.[19]

[19] At a certain doping dependent intrinsic temperature T_{i}, the thermal generation of carriers and the intrinsic carrier density $\mathrm{n_i}$ respectively becomes as high as the carriers in the epitaxy layer in which the losses are mainly generated during the aimed measurement. The intrinsic carrier density exponentially increases with temperature and above T_{i} the resulting temperature rise acts as a positive feedback, which eventually leads to the destruction of the device (e.g. [Lutz 06]). The used SJ device has a relatively high-doped epitaxy layer. Thus, the DUT should withstand junction temperatures well above 150 °C.

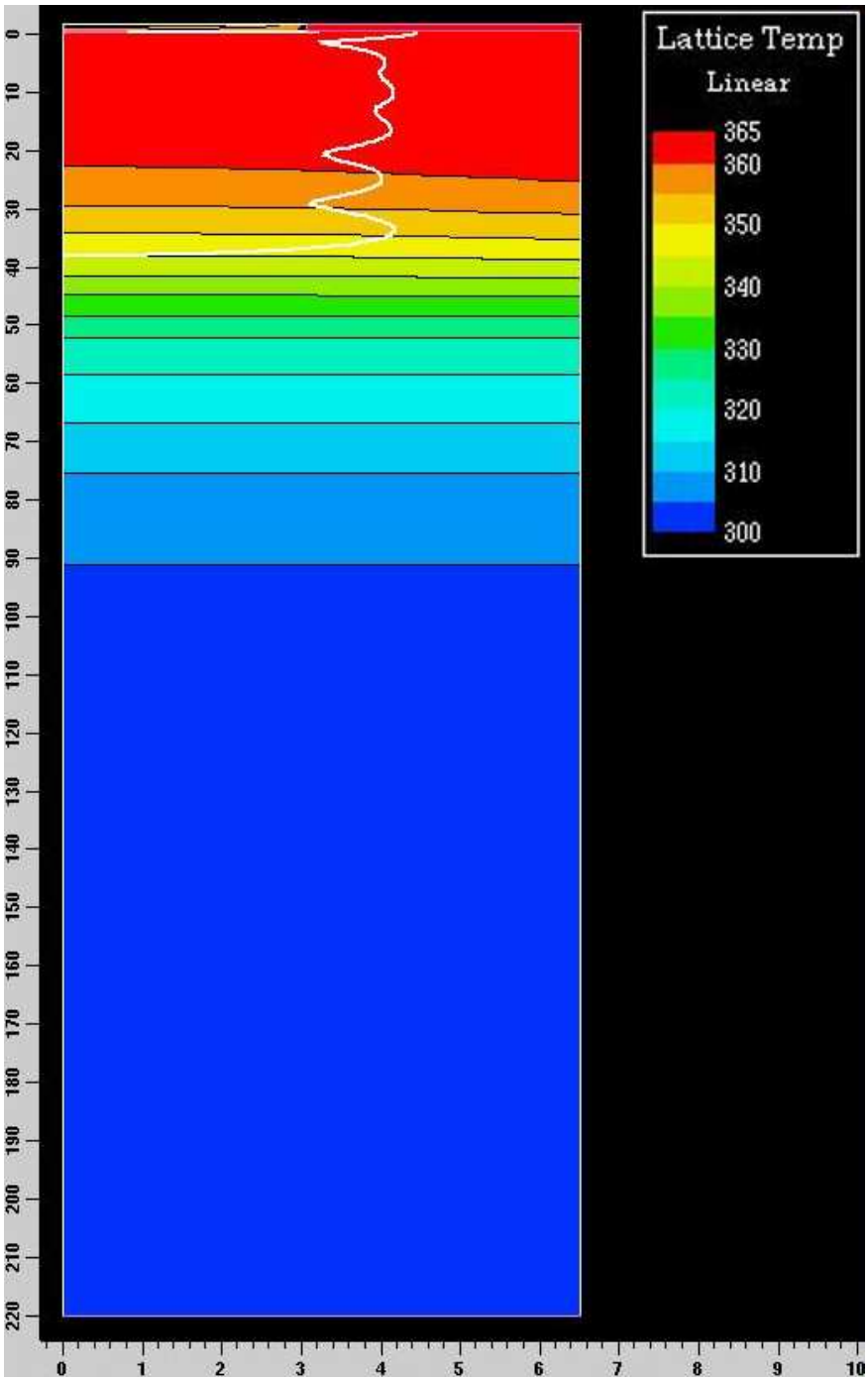
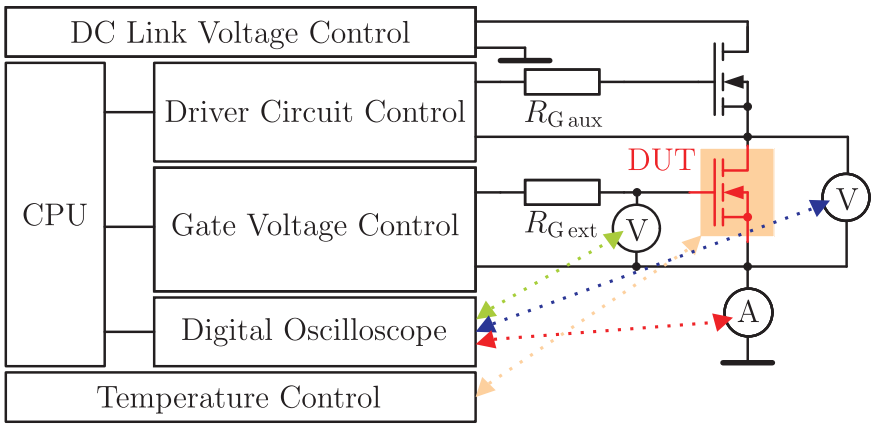
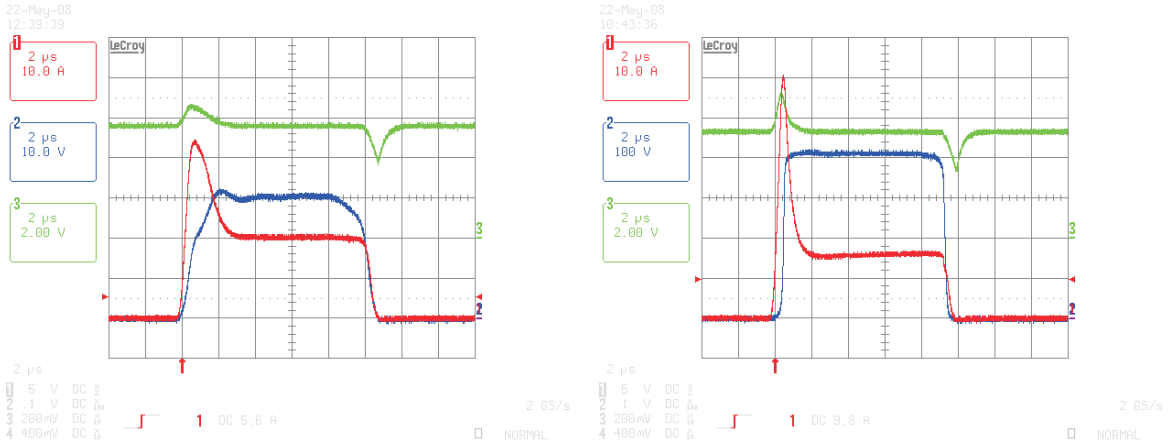


Figure 2.15: *Medici* simulation of the temperature distribution in the SJ MOSFET cell at the end of a single pulse measurement with $t_{\mathrm{pu}} = 10\,\mu\mathrm{s}$, $V_{\mathrm{DS\,chip}} = 400\,\mathrm{V}$, $I_{\mathrm{Ch}} = 20\,\mathrm{A}$ and a constant temperature of 300 K at the backside of the chip (temperature in $[K]$ and geometric data in $[\mu m]$)

Fig. 2.16(a) shows the principle setup for the static characterization of the saturation region. For the measurement of a transfer characteristic, the DC link voltage V_{DClink} and the initial junction temperature are set to the aimed values. The resistances $R_{\mathrm{G\,aux}}$ and $R_{\mathrm{G\,ext}}$ must ensure that the operating points are reached relatively fast with minimized oscillations after the current and voltage slopes (see Fig. 2.16(b)).[20] The gate source voltage of the DUT is varied for every turn-on of the auxiliary MOSFET. After a transition time, the DUT is operated in the defined operating point. The channel current and the chip voltages can be determined from the data recorded with the oscilloscope. The measured operating points are joined to the transfer characteristics. Sample characteristics are shown in Fig. 2.17.



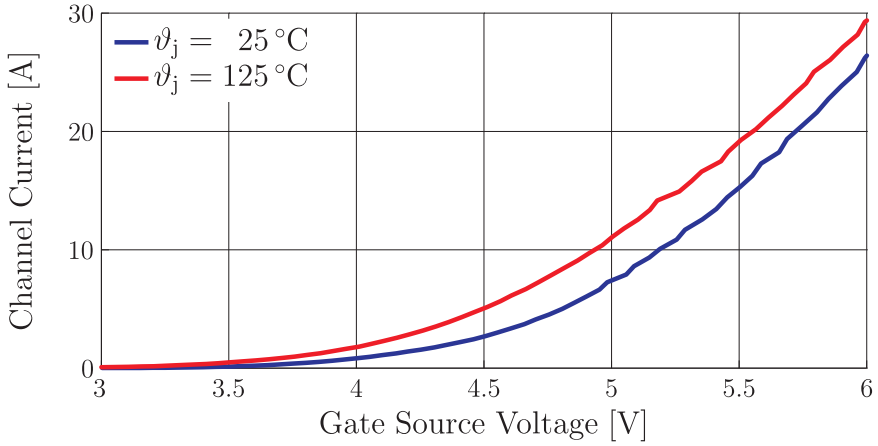
(a) Principle setup for the measurement of transfer characteristics



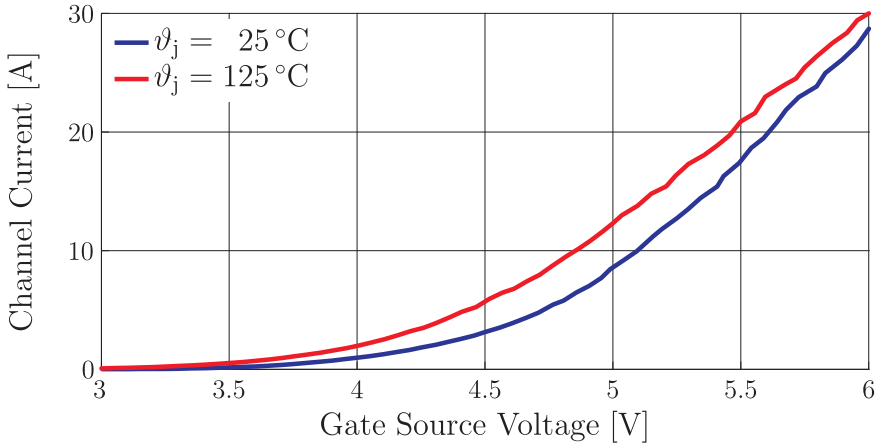
(b) Oscillograms of sample measurements: $V_{\mathrm{DClink}} = 30\,\mathrm{V}$, $V_{\mathrm{GS}} = 5.6\,\mathrm{V}$ and $\vartheta_{\mathrm{J}} = 125\,^{\circ}\mathrm{C}$ (left) as well as $V_{\mathrm{DClink}} = 400\,\mathrm{V}$, $V_{\mathrm{GS}} = 5.2\,\mathrm{V}$ and $\vartheta_{\mathrm{J}} = 125\,^{\circ}\mathrm{C}$ (right) - the color code of the measured signals is indicated in Fig. 2.16(a)

Figure 2.16: Measurement of transfer characteristics (cp. in contrast [López 07])

[20] The optimization of the gate resistances enables the minimization of the transition times and thus, the optimization of the width of the measurement pulse and the minimization of the DUT's self-heating.



(a) Transfer characteristics at $V_{DClink} = 45\,V$



(b) Transfer characteristics at $V_{DClink} = 400\,V$

Figure 2.17: Temperature dependent transfer characteristics of the 600 V SJ MOSFET

The automated ***short circuit measurement*** and the ***interpretation of the measurement data***, which are used for the measurements, are based on the routine in [Brocke 10].

(I) The ***measurement routine*** ensures that ...

- ... the DC link voltage, the pulse width, the gate source voltage range and increment to be measured, and the maximum static current allowed are set in the user interface.
- ... the measurement range of the oscilloscope is as small as possible for each measurement in order to ensure the oscilloscope's maximum accuracy.[21] For small gate source or high drain source voltages, this is particularly important for the drain current measurement due to the relatively large current peak during the transition time.[22] Since

[21] The maximum measurement accuracy refers to the step size, which equals the quotient of the set measurement range and the resolution of the used oscilloscope.

[22] The current peak is induced by the dynamic feedback into the gate circuit: The current $i_{DG\,chip} = C_{DG\,chip} \cdot {}^{dv_{DG\,chip}}/_{dt}$ causes a voltage drop across $R_{G\,ext}$, which results in a gate source voltage above the applied gate source voltage and a channel current above the aimed channel current.

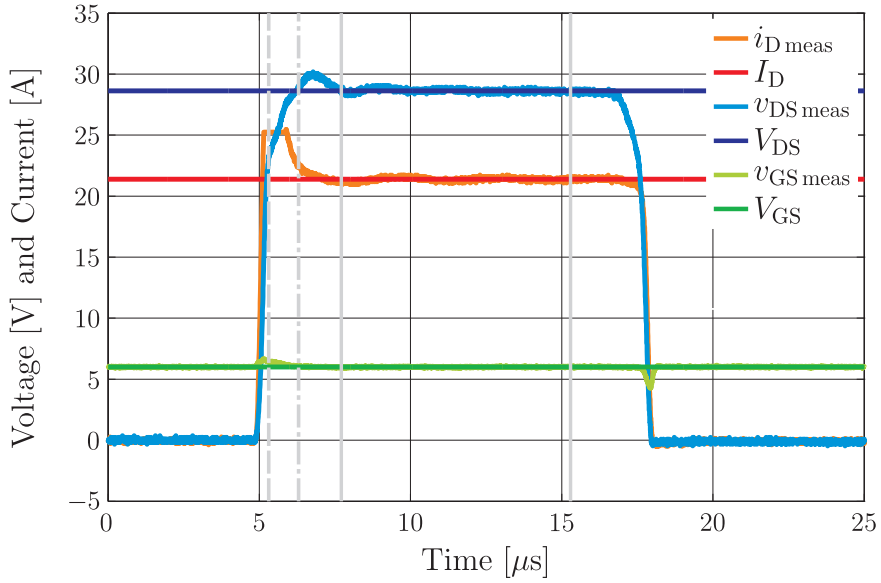


Figure 2.18: Measurement of an operating point in the saturation region - The operating point is determined from the time range between the solid gray lines.

the current measurement range needs to be as small as possible in the range, in which the DUT is statically operated, the current peak can not be part of the measurement range. This results in a cut off signal (see e.g. Fig. 2.18).

- ... the measurement is discontinued if the maximum allowed static drain current is exceeded or if oscillations with temporarily increasing amplitudes occur.

(II) Due to thermal effects, I_{D} should be calculated from a preferably short period time at the beginning of the DUT's static operation. The relevant time segment of the signals can be determined by means of the signals' mean values, derivations, and the DC link voltage and the applied pulse width. This is subsequently shown using the example of the measurement in Fig. 2.18. The used ***data interpretation*** routine implements the following steps:

- The time before the drain source voltage signal reaches 50 % of the DC link voltage and the time of the remaining time range that exceeds the pulse width are deleted.[23] The remaining time range is between the dashed and the right solid line in Fig. 2.18.

- Subsequently, the mean value of the remaining gate source voltage signal $\overline{v_{\mathrm{GS\,meas}}}$ is calculated and the signals are shortened by the time, in which the gate source voltage signal differs more than 2 % from $\overline{v_{\mathrm{GS\,meas}}}$. Then, the mean value of the remaining drain source voltage signal $\overline{v_{\mathrm{DS\,meas}}}$ is determined and the time before the drain source voltage signal reaches 99 % of $\overline{v_{\mathrm{DS\,meas}}}$ is cut off. The remaining time range is between the dashed-dotted and the right solid line in Fig. 2.18.

[23] Due to the charging and discharging of chip-internal capacitances, the applied pulse width is usually shorter than the pulse width of the measured signals.

- Afterwards, the time range for the data interpretation is further limited by means of the derivations of the remaining drain source voltage and drain current signal. A period, in which the derivations are close to zero, is used. The resulting time range is between the solid gray lines in Fig. 2.18.

Enabling the minimization of thermal effects and the mean value determination in case of oscillations, the user interface admits an interval selection of the determined time range for the data interpretation. The interval's mean values of the voltage and current signals represent the operation point. The resulting operating point is also shown in Fig. 2.18.

2.3.1.3 Combined Measurement Data

The data of the curve tracer and the short circuit measurements are combined and integrated in a lookup table. The look up table of the output characteristics is defined by ...

- ... the row index input values, which represent the considered drain source voltage range, as an $1 \times m$ vector, ...
- the column index input values, which represent the considered gate source voltage range, as an $1 \times n$ vector, and ...
- the page index, which represents the considered junction temperature.

For each junction temperature, a $m \times n$ matrix includes the corresponding channel current data. For the calculation of the matrix, first, $V_{\mathrm{DS\,chip}}$ and $V_{\mathrm{GS\,chip}}$ are calculated from measured voltages $V_{\mathrm{DS\,meas}}$ and $V_{\mathrm{GS\,meas}}$ according to subsection **3.3.1** on page 82 et seq.. The matrix is then generated by interpolating the scattered measurement data triples.

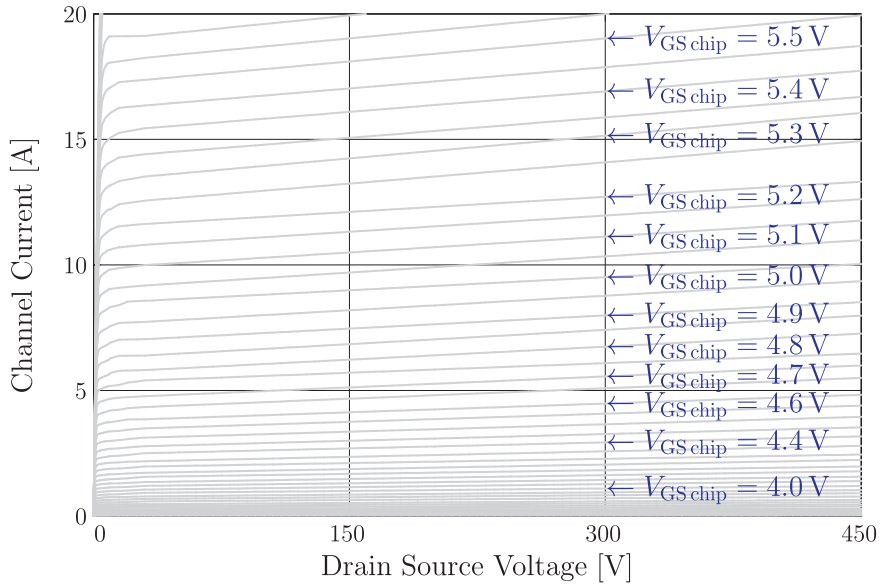
Output characteristics of the combined measurement data are shown in Fig. 2.19 for two junction temperatures. The output characteristics represent the voltage and temperature dependent resistance $R_{\mathrm{DS\,chip}}$ of the behavioral model in Fig. 2.7 on page 19.

2.3.1.4 Discussion of Systematic Error Sources and Evaluation of the Static Parameterization of the Power MOSFET

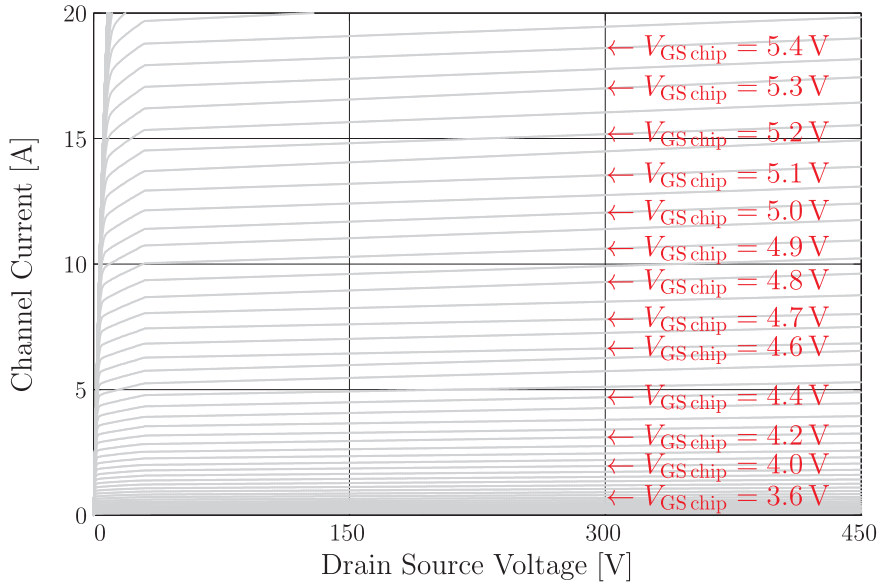
Systematic Error Sources of the Curve Tracer and the Short Circuit Measurements

Considered systematic error sources that apply to both the curve tracer measurements and the measurement of high voltage transfer characteristics are ...

- ... parasitic circuit elements between voltage probing points and the contact points of the semiconductor chip, ...
- ... capacitive currents measured along with the channel current caused by altering voltages across parasitic device and circuit capacitances, ...
- ... the DUT's self-heating during the measurement.



(a) Output characteristics with $\vartheta_J = 25\,°C$



(b) Output characteristics with $\vartheta_J = 125\,°C$

Figure 2.19: Output characteristics up to 450 V of the 600 V SJ MOSFET

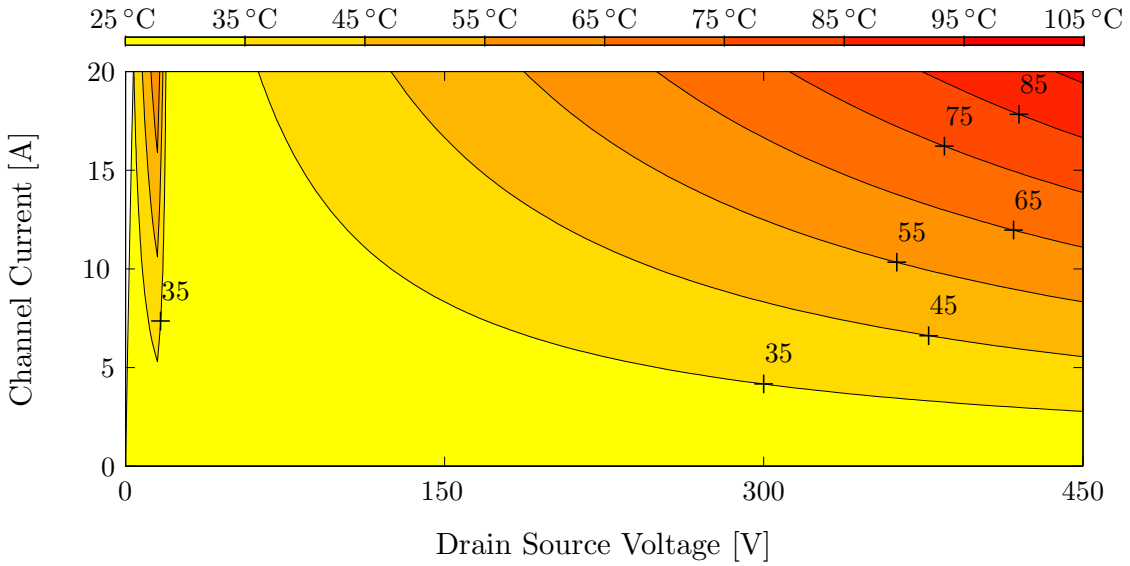


Figure 2.20: $T_{\mathrm{J\,max}}$ according to (2.44) during the static characterization of the DUT's operating range with $V_{\mathrm{Si}} = 0.76\,\mathrm{mm}^3$ and $t_{\mathrm{pu}} = 10\,\mu\mathrm{s}$ for the 'short circuit' and with $V_{\mathrm{Si}} = 1.21\,\mathrm{mm}^3$ and $t_{\mathrm{pu}} = 250\,\mu\mathrm{s}$ for the 'curve tracer' measurements[24]

Subsequently, the impact of the different sources of error is estimated:

(I) Voltage drops across ***parasitic inductances*** are insignificant in the operating point. ***Parasitic resistances*** between the voltage probing points and the semiconductor chip cause differences between the measured voltages $V_{\mathrm{DS\,meas}}$ and $V_{\mathrm{GS\,meas}}$, and the chip voltages $V_{\mathrm{DS\,chip}}$ and $V_{\mathrm{GS\,chip}}$. The chip voltages are calculated according to subsection **3.3.1** on page 82. Hence, the parasitic voltage drops are eliminated as an error source.

(II) The used gate resistance for the curve tracer measurements and the $\mathrm{d}v_{\mathrm{DS\,meas}}/\mathrm{d}t$ limitation of time range for the data interpretation of the high voltage transfer characteristics ensure that remaining ***capacitive currents*** are irrelevant.

(III) Due to the ***DUT's self-heating***, the measured channel current differs from the aimed channel current $I_{\mathrm{Ch}}(V_{\mathrm{DS\,chip}}, V_{\mathrm{GS\,chip}}, T_{\mathrm{J0}})$ with the initial junction temperature T_{J0}. The maximum junction temperature during the measurement of operating points in the considered operating range of the DUT is shown in Fig. 2.20 as a contour plot in the $I_{\mathrm{Ch}}(V_{\mathrm{DS\,chip}})$ plane. The variation of the channel current with temperature is due to the temperature dependence of both the ***threshold voltage*** and the ***electron mobility***:

(a) The ***threshold voltage*** is given by

$$V_{\mathrm{th}} = \phi_{\mathrm{MS\,p}} - \frac{Q_{\mathrm{ox\,p\,fix}}}{C_{\mathrm{ox\,p}}} + 2 \cdot \phi_{\mathrm{F\,p}}(T_{\mathrm{J}}) + \frac{\sqrt{4 \cdot q \cdot \varepsilon_{\mathrm{Si}} \cdot N_A \cdot \phi_{\mathrm{F\,p}}(T_{\mathrm{J}})}}{C_{\mathrm{ox\,p}}} \tag{2.45}$$

[24] Due to the increased pulse width during the curve tracer measurements, the heat dissipation is not only horizontal but also vertical (see Fig. 2.13 on page 30).

with the work-function difference between metal and p-type semiconductor $\phi_{\mathrm{MS\,p}}$, the fixed oxide charge $Q_{\mathrm{ox\,p\,fix}}$, the oxide capacitance $C_{\mathrm{ox\,p}}$, the non-linear temperature dependent FERMI potential of the p-region $\phi_{\mathrm{F\,p}}$ and the impurity concentration of the p-region N_A (more details are given in [Vadasz 66] or [Sze 07]). Therewith, the threshold voltage shift $^{\mathrm{d}V_{\mathrm{th}}}/_{\mathrm{d}T_{\mathrm{J}}}$ during the measurement pulse depends on the initial temperature, the doping of the p-region as well as the oxide thickness. Considering the DUT's physical properties, the temperature dependency of V_{th} according to (2.45) is presented in Fig. 2.21.[25] V_{th} can also be measured for different T_{J} with the constant current method (see e.g. [Jeppson 98] and [Barkhordarian 05]). The results of such measurements - with $I_{\mathrm{Ch}} = 2\,\mathrm{mA}$ and $V_{\mathrm{DS\,chip}} = 200\,\mathrm{V}$ - are also presented in Fig. 2.21. Measurements and calculations correlate well and show a decrease of V_{th} with temperature. As also shown in Fig. 2.21, this correlation is sufficiently described with

$$\begin{aligned} V_{\mathrm{th\,approx}}(T_{\mathrm{J}}) &= V_{\mathrm{th}}(273.15\,\mathrm{K}) - (T_{\mathrm{J}} - 273.15\,\mathrm{K}) \cdot \mathrm{m} \\ &= V_{\mathrm{th}}(0\,^{\circ}\mathrm{C}) - \vartheta_{\mathrm{J}} \cdot \mathrm{m} \end{aligned} \tag{2.46}$$

with the DUT dependent slope m (see e.g. [Lagies 01a], [Kraus 96] and [Reisch 07]). The change of the MOSFET's channel current due to the temperature dependence of the threshold voltage can roughly be estimated with

$$I_{\mathrm{Ch}} \propto V_{\mathrm{GS\,chip}} - V_{\mathrm{th}}(T_{\mathrm{J}}) \quad \text{for } V_{\mathrm{DS\,chip}} \ll V_{\mathrm{GS\,chip}} - V_{\mathrm{th}} \text{ and} \tag{2.47}$$

$$I_{\mathrm{Ch}} \propto \left(V_{\mathrm{GS\,chip}} - V_{\mathrm{th}}(T_{\mathrm{J}})\right)^2 \quad \text{for } V_{\mathrm{DS\,chip}} \geq V_{\mathrm{DS\,sat}} \tag{2.48}$$

(e.g. [Schröder 06]).[26] The reduction of the threshold voltage with temperature results in an increased channel current. Simplifying, the maximum channel current error due to the temperature dependence of V_{th} is calculated for each operating point with

$$e_{\mathrm{thv}} = \left(\frac{V_{\mathrm{GS\,chip}} - V_{\mathrm{th}}(T_{\mathrm{J\,max}})}{V_{\mathrm{GS\,chip}} - V_{\mathrm{th}}(T_{\mathrm{J0}})} - 1\right) \cdot 100\,\% \quad \text{for } V_{\mathrm{DS\,chip}} < V_{\mathrm{DS\,sat}} \text{ and} \tag{2.49}$$

$$e_{\mathrm{thv}} = \left(\frac{\left(V_{\mathrm{GS\,chip}} - V_{\mathrm{th}}(T_{\mathrm{J\,max}})\right)^2}{\left(V_{\mathrm{GS\,chip}} - V_{\mathrm{th}}(T_{\mathrm{J0}})\right)^2} - 1\right) \cdot 100\,\% \quad \text{for } V_{\mathrm{DS\,chip}} \geq V_{\mathrm{DS\,sat}} \tag{2.50}$$

with the initial junction temperature T_{J0}. The operating point dependent error e_{thv} is presented in Fig. 2.22(a) for the 25 °C output characteristics in Fig. 2.14. The maximum derivation e_{thv} is below +30 % of the aimed channel current $I_{\mathrm{Ch}}(V_{\mathrm{DS\,chip}}, V_{\mathrm{GS\,chip}}, T_{\mathrm{J0}})$. In the output characteristics' nonlinear region, e_{thv} is overrated due to the application of (2.47). Higher initial junction temperature increase the e_{thv} values. Hence, deviations from the aimed current $I_{\mathrm{Ch}}(V_{\mathrm{DS\,chip}}, V_{\mathrm{GS\,chip}}, T_{\mathrm{J0}})$ due to the temperature dependence of the threshold voltage are more critical at high junction temperatures.

(b) In the considered operating range, the longitudinal fields along the current flow in the DUT are relatively low.[27] In non-polar semiconductors, such as silicon, the electron mobility at low electric fields is affected by electron scattering due to the presence of acoustic phonons

[25] The physical parameters of the DUT are provided by *Infineon Technologies*.
[26] For a more exact calculation of the channel current it is referred to [Lutz 11] or [Grant 89].
[27] This information was obtained in a personal conversation with *P. Türkes* from *Infineon Technologies*.

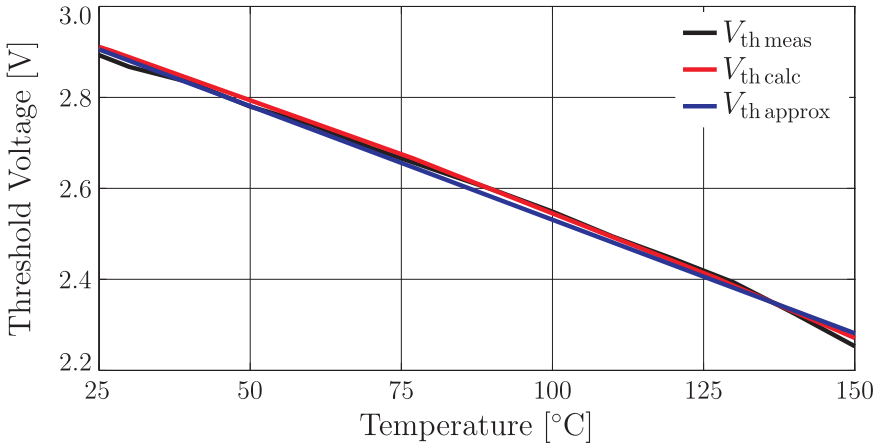


Figure 2.21: Temperature dependence of the threshold voltage of the 600 V SJ MOSFET

and ionized impurities (e.g. [Sze 07]). The temperature dependence of the mobility, which is limited by interactions with acoustical vibrations of the lattice, is characterized by

$$\mu_{\text{ap}} \propto T_{\text{J}}^{-1.5} \tag{2.51}$$

([Bardeen 50] and see e.g. [Heywang 76]). The temperature dependence of the mobility affected by interactions with ionized impurities can be described with

$$\mu_{\text{ii}} \propto T_{\text{J}}^{1.5} \tag{2.52}$$

(cp. [Conwell 50] and [Heywang 76]). The simplifying assumption that acoustic phonon and impurity scattering do not interact allows the application of the MATTHIESSEN rule. Accordingly, the electron mobility is given by

$$\mu_{\text{e}}(T_{\text{J}}) = \left(\frac{1}{\mu_{\text{ap}}(T_{\text{J}})} + \frac{1}{\mu_{\text{ii}}(T_{\text{J}})} \right)^{-1} \tag{2.53}$$

(e.g. [Sze 07]). For relatively low doping densities, the mobility μ_{ap} dominates the electron mobility. According to [Conwell 50] and [Sze 07], μ_{ii} is also proportional to the ionized impurity density. Due to the relatively high doping densities in SJ devices, μ_{ii} increases the effective temperature coefficient. The transfer characteristics in Fig. 2.17 on page 35 indicate a positive temperature coefficient. For smaller values than -1.1, a positive temperature coefficient can not be achieved in the measured saturation region. Therefore, the temperature dependency of the electron mobility μ_{e} is approximated with

$$\mu_{\text{e}} \propto T_{\text{J}}^{-1.1}. \tag{2.54}$$

The electron mobility decreases with rising temperatures. The change of the channel current due to the temperature dependent electron mobility can be estimated by means of

$$I_{\text{Ch}} \propto \mu_{\text{e}}. \tag{2.55}$$

The effective electron mobility of the maximum junction temperature $T_{\mathrm{J\,max}}$ during the measurement of an operating point can be approximated with

$$\mu_{\mathrm{e}}(T_{\mathrm{J\,max}}) \approx \mu_{\mathrm{e}}(T_{\mathrm{J0}}) \cdot \left(\frac{T_{\mathrm{J\,max}}}{T_{\mathrm{J0}}}\right)^{-1.1} \tag{2.56}$$

with the junction temperature T_{J0} at the beginning of the measurement (see e.g. [Lagies 01a], [Kraus 96] and [Reisch 07]). Accordingly, the maximum current error due to the temperature dependence of the electron mobility e_{em} is calculated for each operating point with

$$e_{\mathrm{em}} = \left(\left(\frac{T_{\mathrm{J\,max}}}{T_{\mathrm{J0}}}\right)^{-1.1} - 1\right) \cdot 100\,\%. \tag{2.57}$$

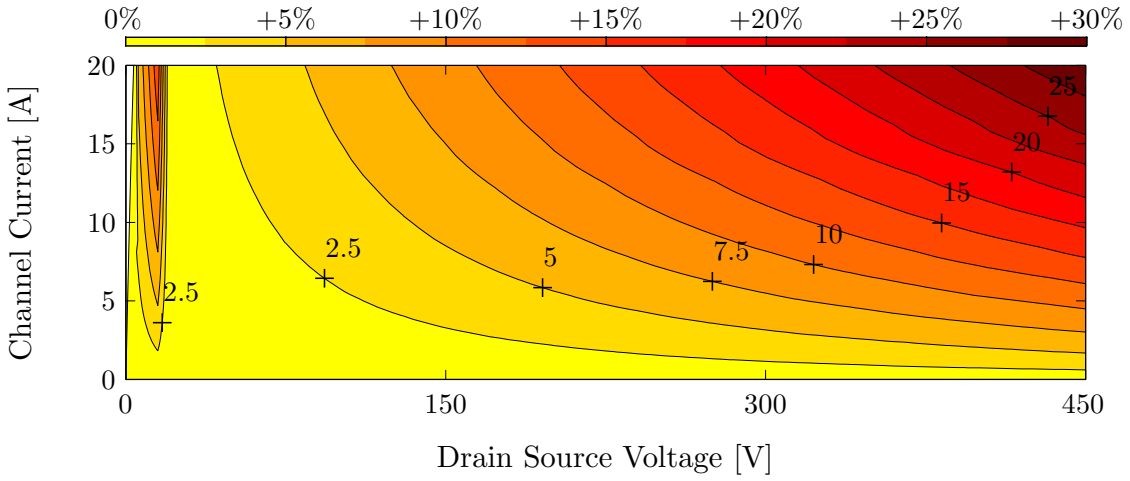
The estimated operating point dependent error e_{em} is presented in Fig. 2.22(b) for the 25 °C output characteristics in Fig. 2.14. The maximum derivation is below −27.5 % of the aimed channel current $I_{\mathrm{Ch}}(V_{\mathrm{DS\,chip}}, V_{\mathrm{GS\,chip}}, T_{\mathrm{J0}})$. Higher T_{J0}, reduce the e_{em} values. Hence, deviations from the aimed channel current $I_{\mathrm{Ch}}(V_{\mathrm{DS\,chip}}, V_{\mathrm{GS\,chip}}, T_{\mathrm{J0}})$ due to the temperature dependence of the electron mobility are more critical at low temperatures.

The impact of the temperature dependent threshold voltage and the temperature dependent electron mobility compensate partially. The total channel current error due to the MOSFET's self heating e_{tot} is approximated with

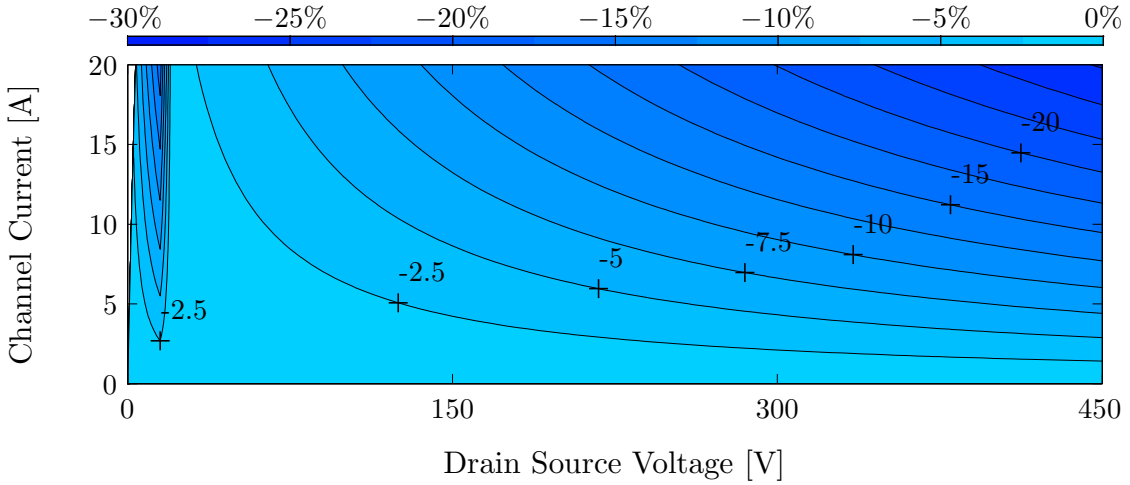
$$e_{\mathrm{tot}} = \left(\left(\frac{T_{\mathrm{J\,max}}}{T_{\mathrm{J0}}}\right)^{-1.1} + \frac{v_{\mathrm{GS\,chip}} - V_{\mathrm{th}}(T_{\mathrm{J\,max}})}{v_{\mathrm{GS\,chip}} - V_{\mathrm{th}}(T_{\mathrm{J0}})} - 2\right) \cdot 100\,\% \quad \text{for } V_{\mathrm{DS\,chip}} < V_{\mathrm{DS\,sat}} \text{ and} \tag{2.58}$$

$$e_{\mathrm{tot}} = \left(\left(\frac{T_{\mathrm{J\,max}}}{T_{\mathrm{J0}}}\right)^{-1.1} + \frac{(v_{\mathrm{GS\,chip}} - V_{\mathrm{th}}(T_{\mathrm{J\,max}}))^2}{(v_{\mathrm{GS\,chip}} - V_{\mathrm{th}}(T_{\mathrm{J0}}))^2} - 2\right) \cdot 100\,\% \quad \text{for } V_{\mathrm{DS\,chip}} \geq V_{\mathrm{DS\,sat}}. \tag{2.59}$$

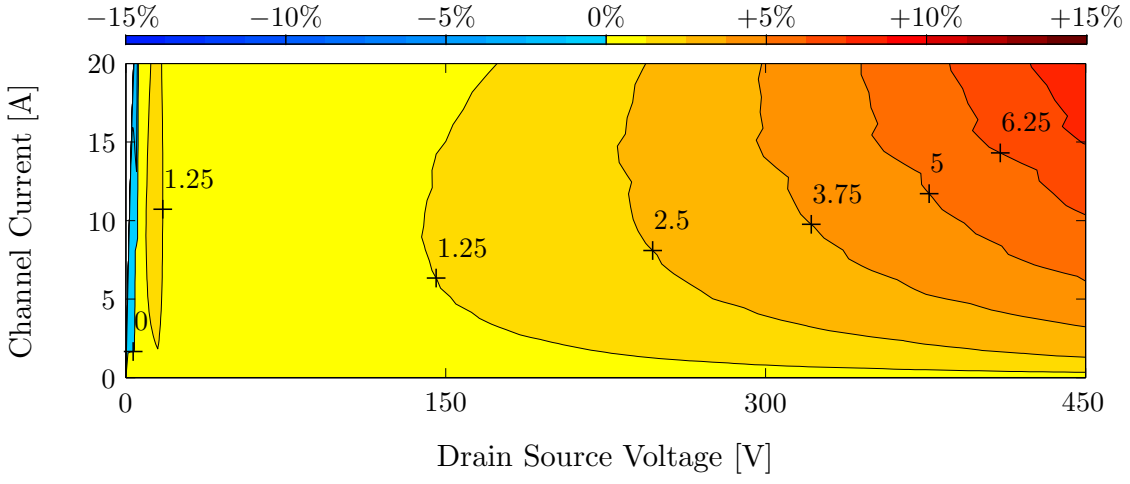
The results are shown in Fig. 2.22(c). The self-heating of the DUT during the static measurements results in an operating point dependent error between −2.5 % and +8.75 % of the aimed channel current $I_{\mathrm{Ch}}(V_{\mathrm{DS\,chip}}, V_{\mathrm{GS\,chip}}, T_{\mathrm{J0}})$. In the linear region of the DUT's output characteristics, the impact of the temperature dependent electron mobility dominates the impact of temperature dependent threshold voltage and the measured channel currents are too low. In the nonlinear and the saturation region, the impact of the temperature dependent threshold voltage outweighs the impact of the temperature dependent electron mobility. The measured channel currents are accordingly too high. The percental derivations of the aimed channel currents at higher drain source voltages are below the calculated values, because the voltages and currents are measured before the end of the measurement pulse and thus, before the maximum junction temperature $T_{\mathrm{J\,max}}$ is reached (see Fig. 2.18 on page 36). The current slope of the measured output characteristics is too high in regions with a positive temperature coefficient, and too low in regions with a negative temperature coefficient. For the 125 °C characteristics, similar results are expected.



(a) Impact of the temperature dependent threshold voltage: Contour plot of e_{thv}



(b) Impact of the temperature dependent electron mobility: Contour plot of e_{em}



(c) Impact of the DUT's self-heating: Contour plot of e_{tot}

Figure 2.22: Channel current error in typical output characteristics at 25 °C

Additional Systematic Error Source of the Curve Tracer Measurements

A systematic error source of the curve tracer measurements is the ***curve tracer's resolution***. The resolution has an impact on the accuracy of the measured I_{Ch} and $V_{\mathrm{DS\,chip}}$. The used measurement routine sets the measurement range for both the drain current and the drain source voltage to the lowest possible values. With respect to the curve tracer's vertical and horizontal ranges as well as its accuracy of ± 0.1 division [Tek 96], the curve tracer's resolution causes a maximum error of $\pm 2\,\%$ of the measured channel currents and drain source voltages in the range of $2.5\,\mathrm{A} \leq I_{\mathrm{Ch}} \leq 20\,\mathrm{A}$ and $0.5\,\mathrm{V} \leq V_{\mathrm{DS\,chip}} \leq 20\,\mathrm{V}$. Below this range the absolute error is within $\pm 50\,\mathrm{mA}$ and $\pm 10\,\mathrm{mV}$ respectively [Tek 96]. The values confirm a sufficient accuracy for the dynamic analysis.

Additional Systematic Error Sources of the Short Circuit Measurements

Considered systematic error sources that apply solely to the measurement of high voltage transfer characteristics are ...

- ... the vertical resolution of the used oscilloscope, ...
- ... offsets in the measured current and voltage signals, and ...
- ... the accuracy of the programmable voltage source in the DUT's gate circuit.

Subsequently, the impact of the different sources of error is estimated:

(I) The ***vertical resolution of the oscilloscope*** is critical for the accuracy of the measurement of the channel current. The implemented measurement routine adjusts the measurement range of the current for each measured operating point which results in an error below $\pm 0.5\,\%$ of the actual channel current. The vertical resolution has also an impact on the accuracy of the measured drain source voltage. The implemented measurement routine adapts the measurement range of the drain source voltage to the preset V_{DClink}. Considering actual drain source voltage variations during the measurement of transfer characteristics, the vertical resolution of the drain source voltage channel causes an error smaller than $\pm 1\,\%$ of the actual chip voltage. This error is insignificant due to the small slope of the DUT's output characteristics in the saturation region.

(II) ***Signal offsets*** in the time dependent current and voltage characteristics are eliminated with an offset correction. An offset correction of measured gate source voltage is not possible since the signal has no zero voltage range during the measurement. However, as the voltage probing points, the gate circuit is connected as close as possible to the DUT. Thus, the applied gate source voltage equals the potential differences between the probing points and only the accuracy of the voltage source needs to be considered.

(III) The appointed gate source voltage value of the programmable voltage source is directly used for temperature dependent data triple of the measured operating points. The ***accuracy of the programmable voltage source*** varies between $\pm 0.5\,\%$ of its output

for gate source voltages near the DUT's threshold voltages and ±0.15 % of its output for gate source voltages near the driver voltage [Agi 07].

Based on the previous considerations, it is concluded that the maximum channel current error is below 10 % of $I_{\mathrm{Ch}}(V_{\mathrm{DS\,chip}}, V_{\mathrm{GS\,chip}}, T_{\mathrm{J0}})$ in the considered operating range. Therewith, the static characterization of the DUT has a sufficient accuracy for the simulation of switching characteristics and the aimed stability analysis.

2.3.2 Static Characterization of Schottky Diodes

Corresponding to the considered operating range of the SJ MOSFET, the static parameterization of the used 600 V SiC SCHOTTKY diode should include a forward characteristic up to 15 A and a blocking characteristic up to 450 V for the aimed junction temperatures. Both characteristics are can be determined by means of curve tracer measurements.

(I) The ***forward characteristics*** are determined by applying a sequence of measurement pulses to the diode. A sample pulse is shown in the oscillogram in Fig. 2.23. Forward characteristics of the diode are presented in Fig. 2.24(a).

(II) Due to the minor losses in the ***reverse characteristics***, the curve tracer's collector supply is not pulsed in the applied leakage measurement mode. Blocking characteristics of the SCHOTTKY diode are presented in Fig. 2.24(b).

The characteristics represent the voltage and temperature dependent resistance $R_{\mathrm{AC\,chip}}$ of the SCHOTTKY diode's behavioral model in Fig. 2.11 on page 25. Considered systematic error sources in the characteristics are ...

- ... the curve tracers' vertical resolution, ...
- ... voltage drops across parasitic circuit elements between voltage probing points and the contact points of the semiconductor chip, ...
- ... capacitive currents measured along with the diode's forward current, ...
- ... the DUT's self-heating during the measurement.

Subsequently, the impact of the different sources of error is estimated:

(I) Errors in the blocking characteristics due to the ***curve tracer's resolution*** are not relevant for this work. The implemented measurement routine for forward characteristics sets the measurement range for the current and the voltage to the smallest possible values. With respect to the measurement ranges and the accuracy of ±0.1 division of used curve tracer [Tek 96], a maximum error of ±2 % of the measured currents and voltages is caused in the range of $2.5\,\mathrm{A} \leq I_{\mathrm{MS}} \leq 20\,\mathrm{A}$ and $0.5\,\mathrm{V} \leq V_{\mathrm{AC\,chip}} \leq 6\,\mathrm{V}$. Below this range, the absulute error in the forward characteristics is within ±50 mA and ±10 mV respectively [Tek 96].

(II) Voltage drops across ***parasitic inductances*** are insignificant in the operating point. ***Parasitic resistances*** between the voltage probing points and the chip cause differences

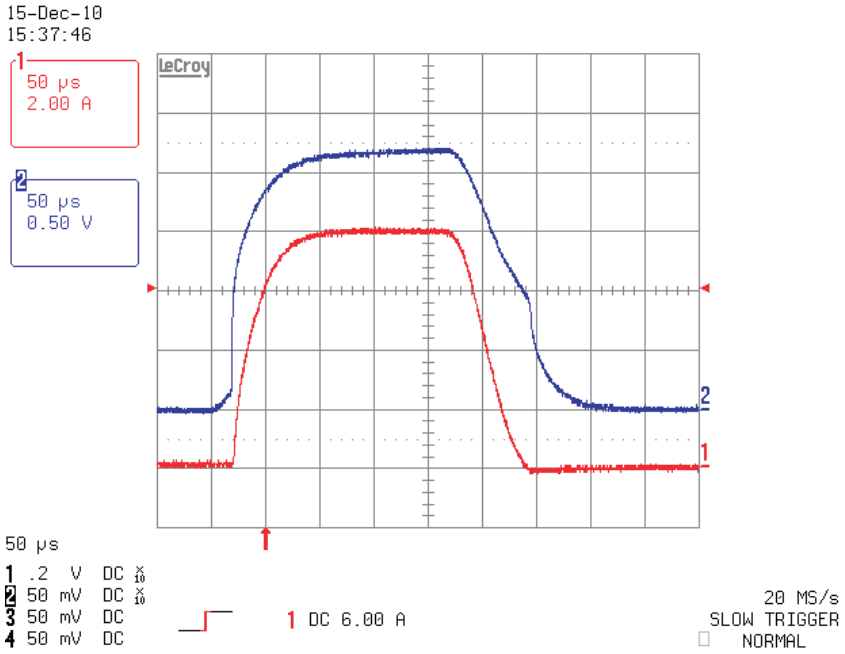


Figure 2.23: Measurement of a forward operating point of the 600 V SiC SCHOTTKY diode - Channel two represents the voltage across the diode and channel one the current through the diode during the measurement.

between $V_{\mathrm{AC\,meas}}$ and $V_{\mathrm{AC\,chip}}$. $V_{\mathrm{AC\,chip}}$ is calculated as described in subsection **3.3.1** on page 82 et seq.. Hence, the parasitic voltage drops are eliminated as an error source.

(III) Almost constant cathode anode voltages are given in the metering interval of the operating points (see Fig. 2.23). Thus, remaining ***capacitive currents*** are irrelevant.

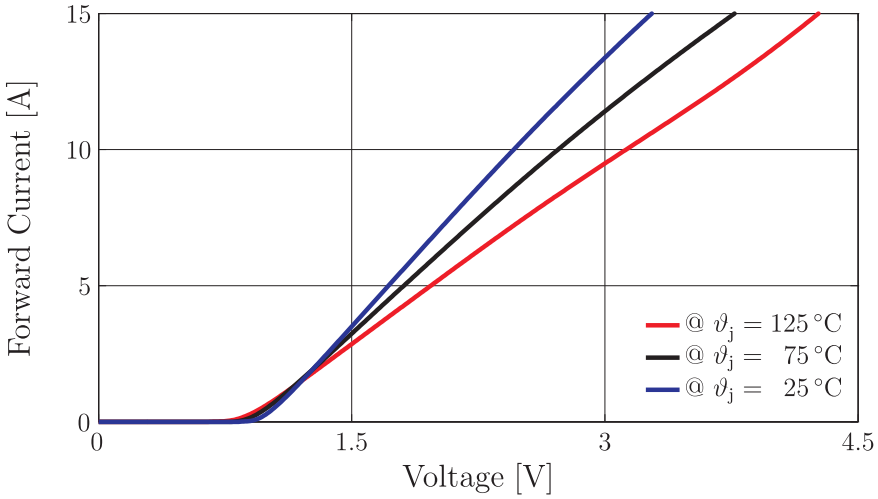
(IV) Since the curve tracer's collector supply is not pulsed during the measurement of the blocking characteristics, (2.40) on page 27 is used for the estimation of the DUT's ***self-heating***. According to [Inf 08b], the maximum thermal resistance $R_{th\,\mathrm{JC}}$ equals 3.6 ^{K}/W. For a worst case calculation, the junction temperature increase of the most lossy operating point of the measured blocking characteristics is calculated with

$$\Delta T_{\mathrm{J}} = \Delta T_{\mathrm{J\,max}} = \Delta T_{\mathrm{J\,avg}} = P_{\mathrm{avg}} \cdot R_{th\,\mathrm{JC}} = 1\,\mu\mathrm{A} \cdot 720\,\mathrm{V} \cdot 3.6\,{}^{K}/\mathrm{W} \approx 2.6\,\mathrm{mK}.$$

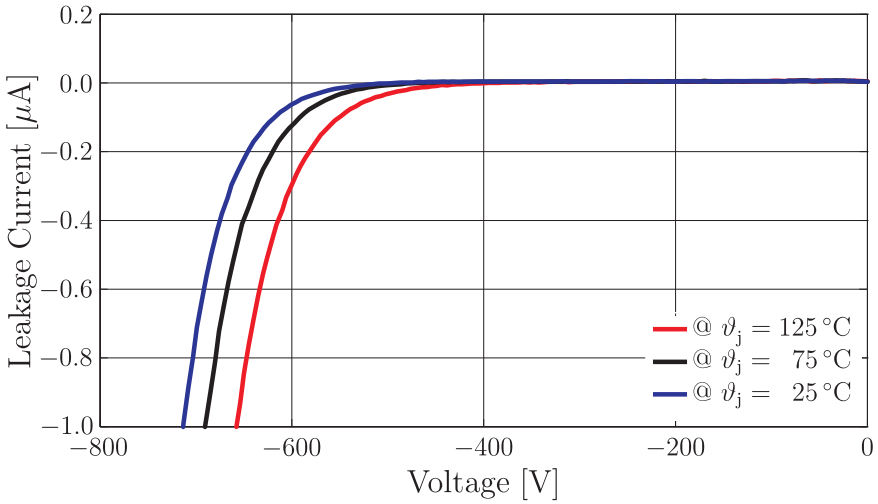
Thus, the self-heating during the measurement of the blocking characteristics is insignificant. According to [Inf 08b], the effective transient thermal junction case impedance $Z_{th\,\mathrm{JC}}$ equals 0.5 ^{K}/W for a pulse width of 250 μs. With (2.39) and (2.40) and a pulse repetition time $\mathcal{T}_{\mathrm{pu}}$ of one second, the measurement cycle's self-heating of the most lossy operating point of the measured 25 °C forward characteristic is described with

$$\Delta T_{\mathrm{J\,max}} = T_{\mathrm{J\,max}} - T_{\mathrm{C}} = P_{\mathrm{pu}} \cdot Z_{th\,\mathrm{JC}} = 15\,\mathrm{A} \cdot 3.3\,\mathrm{V} \cdot 0.5\,{}^{K}/\mathrm{W} = 24.75\,\mathrm{K} \text{ and}$$

$$\Delta T_{\mathrm{J\,avg}} = T_{\mathrm{J\,avg}} - T_{\mathrm{C}} = P_{\mathrm{avg}} \cdot R_{th\,\mathrm{JC}} = \frac{15\,\mathrm{A} \cdot 3.3\,\mathrm{V} \cdot 250\,\mu\mathrm{s}}{1\,\mathrm{s}} \cdot 3.6\,{}^{K}/\mathrm{W} \approx 0.045\,\mathrm{K}.$$



(a) Forward characteristics



(b) Blocking characteristics

Figure 2.24: Static characteristics of the 600 V SiC SCHOTTKY diode

According to the characteristics in Fig. 2.24(a), the DUT's self-heating is insignificant for relatively small forward voltages. For higher forward voltages, the previous calculations and the characteristics in Fig. 2.24(a) indicate an error below -10 % of $I_{MS}(V_{AC\,chip}, T_{J0})$.

Therewith, the presented static characteristics of SiC SCHOTTKY diode have a sufficient accuracy for the simulation of switching characteristics in section **4.1** on page 95 et seq. and chapter **5.4** on page 156 et seq..

2.4 Determination of the Dynamic Parameters of the Behavioral Models

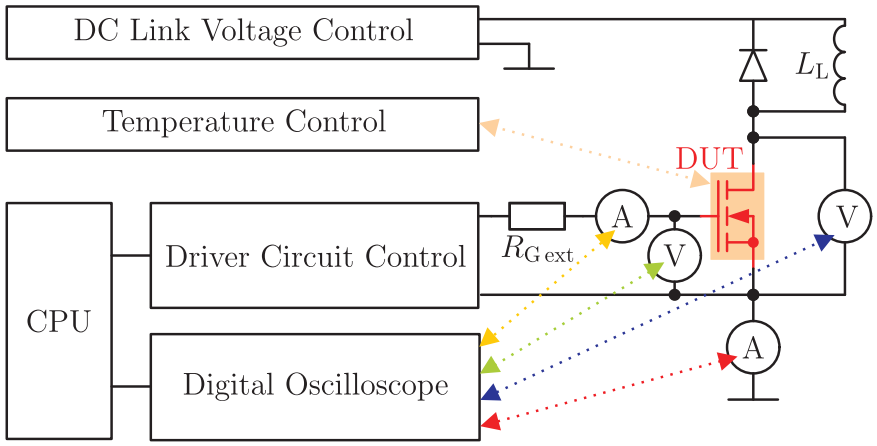
Capacitance voltage characteristics of the MOSFET and the SCHOTTKY diode are needed for the dynamic parameterization of the operating point dependent capacitances $C_{\mathrm{DS\,chip}}$, $C_{\mathrm{DG\,chip}}$, $C_{\mathrm{GS\,chip}}$ and $C_{\mathrm{AC\,chip}}$ of the behavioral models in Fig. 2.7 on page 19 and Fig. 2.11 on page 25. The capacitance voltage characteristics of power MOSFETs depend on the voltages $v_{\mathrm{DS\,chip}}$ and $v_{\mathrm{GS\,chip}}$ during commutation. Therefore, in subsection **2.4.1**, the capacitance voltage characteristics of the 650 V super junction MOSFET are determined from dynamic measurements. The capacitance voltage characteristic of SCHOTTKY diodes are independent of the switching conditions. Therefore, the capacitance voltage characteristics of the 600 V SCHOTTKY diode is measured in accordance with the standard DIN IEC 747. The result of this measurement is presented in **2.4.2**.

2.4.1 Dynamic Characterization of Power MOSFETs

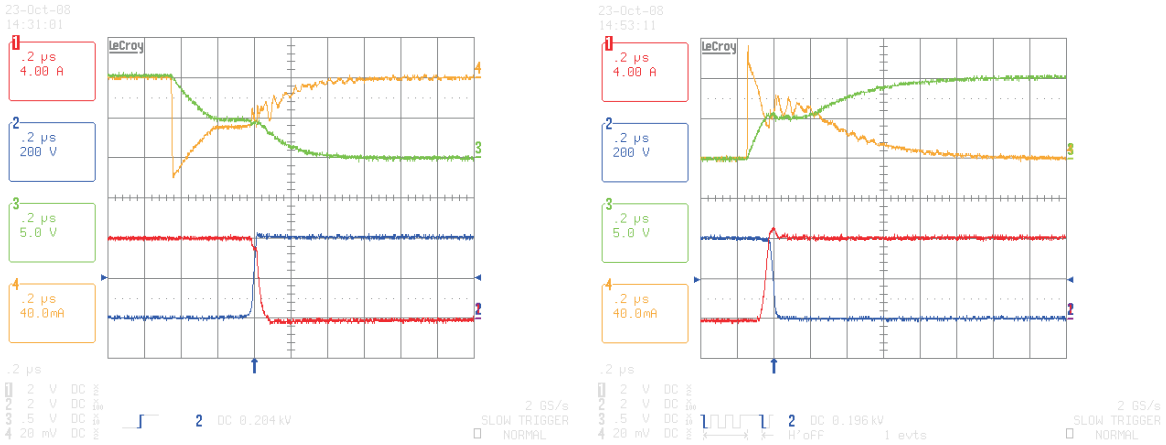
During switching operations, the nonlinear capacitances $C_{\mathrm{DS\,chip}}$, $C_{\mathrm{DG\,chip}}$ and $C_{\mathrm{GS\,chip}}$ can not be measured. However, if capacitance voltage characteristics can be determined from the corresponding switching characteristics for different switching conditions, the MOSFET's dynamic behavior can be represented for a certain range of switching conditions. This subsection investigates how the MOSFET's capacitance voltage characteristics can be determined from dynamic measurements. The measurement setup and the determinability of the capacitances are discussed in **2.4.1.1**. As a result of this discussion, the gate source capacitance $C_{\mathrm{GS\,chip}}$ is approximated in **2.4.1.2**, and the drain gate capacitance $C_{\mathrm{DG\,chip}}$ and the drain source capacitance $C_{\mathrm{DS\,chip}}$ are calculated in **2.4.1.3**. In **2.4.1.4**, systematic error sources are discussed and the defined MOSFET capacitances are evaluated. The described dynamic characterization is not limited to the DUT but applicable to any MOSFET as long as no parasitic oscillations occur during the voltage commutation.

2.4.1.1 Measurement Setup and Capacitance Determinability

Application relevant switching characteristics can be measured in a commutation circuit with an inductive load. A typical commutation circuit with an inductive load is a buck converter. A buck converter topology is often used for the measurement of switching characteristics (see e.g. [Witcher 02] and [Chen 09]). The principle setup and sample dynamic measurements of the used topology are shown in Fig. 2.25. The gate current $i_{\mathrm{G\,meas}}(t)$ and the drain current $i_{\mathrm{D\,meas}}(t)$ are both captured with a 1:1 PEARSON probe [Pea 99]. 100 : 1 and 10 : 1 voltage probes are used for the measurement of the drain source voltage $v_{\mathrm{DS\,meas}}(t)$ and the gate source voltage $v_{\mathrm{GS\,meas}}(t)$. The MOSFET is switched by a double pulse at its gate. At the end of the first pulse and at the beginning of the second pulse the switching transients are measured for a set DC link voltage and load current. For a given DC link voltage, the turn-off



(a) Principle setup for dynamic measurements



(b) Oscillograms of sample measurements: turn-off (left) and turn-on (right) with $V_{DClink} = 400\,V$, $v_{Dr} = 10\,V$, $i_L = 8\,A$, $R_{G\,ext} = 100\,\Omega$ and $\vartheta_J = 25\,°C$ - the color code of the measured signals is indicated in Fig. 2.25(a)

Figure 2.25: Measurement of switching characteristics

current can be adjusted with the load inductance L_L and the length of the first pulse. The turn-on current equals approximately the turn-off current, if the break in between the two pulses is small with respect to the load current ripple $^{di_L}/_{dt} = {}^{V_L}/_{L_L}$ of the free wheeling loop. The transistor's junction temperature can be varied by means of a heating plate and its switching speed can be modified with the series gate resistance $R_{G\,ext}$. The 600 V SiC SCHOTTKY diode is used as freewheeling diode [Inf 08b].

In order to obtain switching characteristics suitable for the determination of capacitance voltage characteristics, it must be ensured that ...

- ... parasitic capacitances and inductances in the commutation circuit are as small as possible. Parasitic capacitances and inductances can increase switching times and have - as discussed in chapter **5** on page 111 et seq. - a significant impact on the

occurrence of parasitic oscillations during commutation. Oscillations can limit the measurable switching conditions and affect the determinability of capacitance voltage characteristics from the measurement data.

- ... the voltage probing points are placed as close to the DUT as possible. This requirement reduces differences between measured and chip voltages due to parasitic circuit elements between chip and probing points (see Fig. 3.11 on page 86).
- ... the current probes are placed as close to the DUT as possible, and are exposed as less to voltage alterations as possible. This decreases differences between measured currents and the currents that flow into the contacts of the chip. The differences are caused by the charging of chip-external capacitances, that are connected to the current paths between the DUT and the currents' probing points (see Fig. 3.8 on page 81).
- ... the characteristics are acquired from sufficiently short double pulses. The electrical characteristics of any semiconductor device are affected by temperature. This approach ensures a minimal self-heating during the dynamic measurements.
- ... the bandwidth of the measurement system is relatively high compared to the equivalent frequencies of the DUT's switching waveforms (see e.g. [Tek 08] and [Tek 09]).[28] Otherwise, the switching slopes are not measured with a sufficient accuracy.
- ... the probes have well-matched delay characteristics. Otherwise, the time dependent switching characteristics need to be adjusted to one another (see e.g. [Laimer 02]).
- ... the switching characteristics have a sufficient resolution. This necessitates a relatively high sampling rate of the used oscilloscope.

Considering these requirements, the switching characteristics of the 600V SJ MOSFET are measured. For the determination of the capacitances, the chip-internal voltages $v_{\mathrm{DS\,chip}}(t)$, $v_{\mathrm{DG\,chip}}(t)$ and $v_{\mathrm{GS\,chip}}(t)$ need to be calculated. The electrical interconnections between the DUT and the voltage probing points are modeled in subsection **3.2.2** on page 70 et seq.. In subsection **3.3.2** on page 85 et seq., the correction of the measured voltages is presented. If the currents $i_{\mathrm{GS\,chip}}(t)$, $i_{\mathrm{DS\,chip}}(t)$ and $i_{\mathrm{DG\,chip}}(t)$ in Fig. 2.7 on page 19 were measurable, the capacitances could be calculated with $C_{\mathrm{GS\,chip}} = {}^{i_{\mathrm{GS\,chip}}(t)}\!/_{\mathrm{d}v_{\mathrm{GS\,chip}}/\mathrm{d}t}$, $C_{\mathrm{DS\,chip}} = {}^{i_{\mathrm{DS\,chip}}(t)}\!/_{\mathrm{d}v_{\mathrm{DS\,chip}}/\mathrm{d}t}$ and $C_{\mathrm{DG\,chip}} = {}^{i_{\mathrm{DG\,chip}}(t)}\!/_{\mathrm{d}v_{\mathrm{DG\,chip}}/\mathrm{d}t}$. For the determination of the currents $i_{\mathrm{GS\,chip}}(t)$, $i_{\mathrm{DS\,chip}}(t)$ and $i_{\mathrm{DG\,chip}}(t)$, a system of equations is set up using KIRCHHOFF's circuit laws for the branch point equations

$$i_{\mathrm{GS\,chip}}(t) - i_{\mathrm{DG\,chip}}(t) = i_{\mathrm{G\,meas}}(t) \text{ and} \tag{2.60}$$

$$i_{\mathrm{DS\,chip}}(t) + i_{\mathrm{DG\,chip}}(t) = i_{\mathrm{D\,meas}}(t) - i_{\mathrm{Ch}}(t), \tag{2.61}$$

and for the differentiated mesh equation

$$\frac{i_{\mathrm{GS\,chip}}(t)}{C_{\mathrm{GS\,chip}}} - \frac{i_{\mathrm{DS\,chip}}(t)}{C_{\mathrm{DS\,chip}}} + \frac{i_{\mathrm{DG\,chip}}(t)}{C_{\mathrm{DG\,chip}}} = 0. \tag{2.62}$$

[28] The estimation of a switching waveform's equivalent frequency is e.g. described in [Witcher 02].

The points in time, in which the currents and voltages are measured, are indicated by '(t)'. With respect to [Bronstein 08], if the capacitances $C_{\mathrm{DS\,chip}}$, $C_{\mathrm{GS\,chip}}$ and $C_{\mathrm{DG\,chip}}$ are known in each point in time, the inhomogeneous system of linear equations

$$\begin{pmatrix} 1 & 0 & -1 \\ 0 & 1 & 1 \\ \frac{1}{C_{\mathrm{GS\,chip}}} & -\frac{1}{C_{\mathrm{DS\,chip}}} & \frac{1}{C_{\mathrm{DG\,chip}}} \end{pmatrix} \cdot \begin{pmatrix} i_{\mathrm{GS\,chip}}(t) \\ i_{\mathrm{DS\,chip}}(t) \\ i_{\mathrm{DG\,chip}}(t) \end{pmatrix} = \begin{pmatrix} i_{\mathrm{G\,meas}}(t) \\ i_{\mathrm{D\,meas}}(t) - i_{\mathrm{Ch}}(t) \\ 0 \end{pmatrix} \tag{2.63}$$

has a unique solution for each point in time, since the rank of the system's coefficient matrix is equal to the rank of its augmented matrix and the number of unknowns. With $v_{\mathrm{DS\,chip}}(t)$ and $v_{\mathrm{GS\,chip}}(t)$, the channel current $i_{\mathrm{Ch}}(t)$ can be calculated by means of the measured output characteristics.[29] Since the capacitances in (2.63) are sought not given, the displacement currents are substituted with $i_C(t) = C \cdot {}^{\mathrm{d}v_C}/_{\mathrm{d}t}$, and the equation system is transposed accordingly. Although the rank of the systems coefficient matrix is equal to the rank of its augmented matrix, the resulting system of equations

$$\begin{pmatrix} \frac{\mathrm{d}v_{\mathrm{GS\,chip}}}{\mathrm{d}t} & 0 & -\frac{\mathrm{d}v_{\mathrm{DG\,chip}}}{\mathrm{d}t} \\ 0 & \frac{\mathrm{d}v_{\mathrm{DS\,chip}}}{\mathrm{d}t} & \frac{\mathrm{d}v_{\mathrm{DG\,chip}}}{\mathrm{d}t} \\ \frac{\frac{\mathrm{d}v_{\mathrm{GS\,chip}}}{\mathrm{d}t}}{C_{\mathrm{GS\,chip}}} & -\frac{\frac{\mathrm{d}v_{\mathrm{DS\,chip}}}{\mathrm{d}t}}{C_{\mathrm{DS\,chip}}} & \frac{\frac{\mathrm{d}v_{\mathrm{DG\,chip}}}{\mathrm{d}t}}{C_{\mathrm{DG\,chip}}} \end{pmatrix} \cdot \begin{pmatrix} C_{\mathrm{GS\,chip}} \\ C_{\mathrm{DS\,chip}} \\ C_{\mathrm{DG\,chip}} \end{pmatrix} = \begin{pmatrix} i_{\mathrm{G\,meas}}(t) \\ i_{\mathrm{D\,meas}}(t) - i_{\mathrm{Ch}}(t) \\ 0 \end{pmatrix} \tag{2.64}$$

has no unique solution, since the rank of its coefficient matrix and its augmented matrix is less than the number of unknowns. Therewith, the solution depends on an arbitrary capacitance. A third linearly independent equation does not exist for the given network. Thus, it is not possible to determine $C_{\mathrm{GS\,chip}}$, $C_{\mathrm{DS\,chip}}$ and $C_{\mathrm{DG\,chip}}$ uniquely from dynamic measurement data unless one of the three transistor capacitances is known.

2.4.1.2 Approximation of the Gate Source Capacitance

Due to its relatively low voltage dependency, the gate source capacitance $C_{\mathrm{GS\,chip}}$ is often approximated by a constant capacitance value in behavioral models (cp. e.g. [Schröder 06] or [Mohan 03]). For the determination of a suitable constant $C_{\mathrm{GS\,chip}}$ value, the dynamic input capacitance C_{in}

$$C_{\mathrm{in}} := \frac{\mathrm{d}Q_{\mathrm{in}}}{\mathrm{d}v_{\mathrm{GS\,chip}}} = \frac{\mathrm{d}\int i_{\mathrm{G\,meas}}\,\mathrm{dt}}{\mathrm{d}v_{\mathrm{GS\,chip}}} \tag{2.65}$$

with $\mathrm{dv}_{\mathrm{GS\,chip}} \neq 0$ is defined. With respect to

$$i_{\mathrm{G\,meas}}(t) = C_{\mathrm{GS\,chip}} \cdot \frac{\mathrm{d}v_{\mathrm{GS\,chip}}}{\mathrm{d}t} - C_{\mathrm{DG\,chip}} \cdot \frac{\mathrm{d}v_{\mathrm{DG\,chip}}}{\mathrm{d}t}, \tag{2.66}$$

C_{in} equals the sum of $C_{\mathrm{DG\,chip}}$ and $C_{\mathrm{GS\,chip}}$, if the drain source voltage does not alter with time. Constant drain source voltages are assumed ...

[29] See **2.3.1** on page 27 et seq. for details on the measurement.

- ... *during turn-on* before the current commutates and - in case the drain source voltage is not oscillating - after the voltage commutation, as well as ...

- ... *during turn-off* before voltages commutates and - in case the drain source voltage is not oscillating - after the current commutation.

Fig. 2.26 shows gate charge curves of different turn-on and turn-off operations of the DUT. The MOSFET's threshold voltage, which represents the beginning of the current commutation during turn-on and the end of the current commutation during turn-off, is approximately at 3.2 V. The voltage commutation corresponds to the nearly vertical part - the MILLER plateau - of the gate charge curves in Fig. 2.26.[30] The MILLER plateau voltage depends on the load current. The input capacitance before and after the MILLER plateau is approximately given by the slopes of the linear functions in Fig. 2.26. The black and the gray slopes represent two different conditions of the DUT:

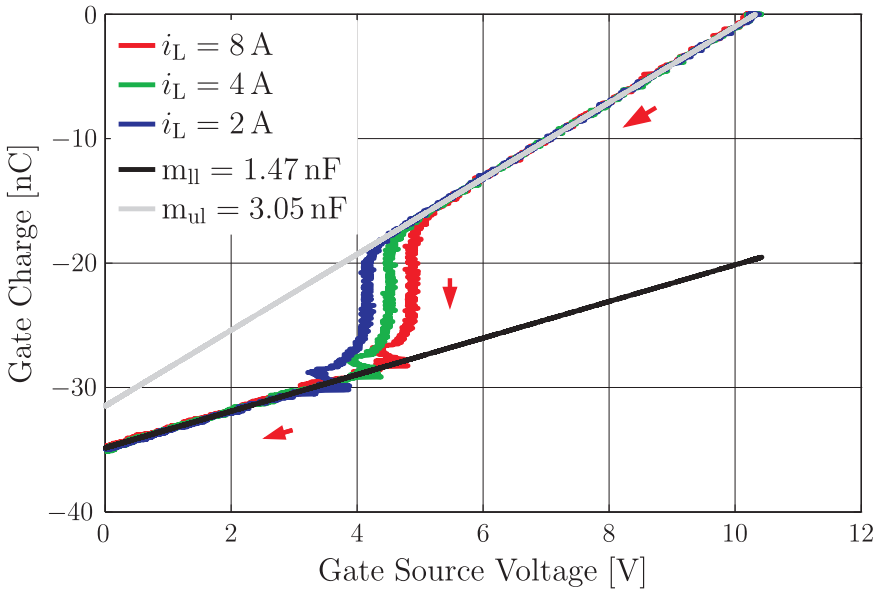
(I) The ***black line*** corresponds to gate source voltages below the threshold voltage and a constant drain source voltage of 400 V. The input capacitance C_{in} is represented by the sum of four capacitances - the capacitance C_{MOM} and the metal-oxide-semiconductor capacitances $C_{\text{MOS n}^+}$, $C_{\text{MOS p}}$ and $C_{\text{MOS n}^-}$ (see Fig. 2.7 on page 19 for details). C_{MOM} is voltage independent. It mainly depends on the transistor's material and geometric properties. For positive gate source voltages, $C_{\text{MOS n}^+}$ is in accumulation mode. Apart from a relatively small voltage range at the beginning of accumulation, $C_{\text{MOS n}^+}$ is constant and equals its oxide capacitance.[31] $C_{\text{MOS p}}$ is in depletion mode between $v_{\text{GS chip}}(t) = 0\,\text{V}$ and $v_{\text{GS chip}}(t) = V_{\text{th}}$. During depletion $C_{\text{MOS p}}$ results from the series connection of the space charge region capacitance $C_{\text{scr p}}$ and the oxide capacitance $C_{\text{ox p}}$. With rising $v_{\text{GS chip}}$, $C_{\text{scr p}}$ and $C_{\text{MOS p}}$ decrease. The alteration of $C_{\text{MOS n}^+}$ and $C_{\text{MOS p}}$ at low gate source voltages compensate partly. For the gate source voltages below the MILLER plateau voltage, almost the entire DC link voltage drops between the gate and drain contact. Thus, $C_{\text{MOS n}^-}$ is in depletion, and $C_{\text{DG chip}}$ is substantially smaller than $C_{\text{GS chip}}$. This can also be seen in the DUT's data sheet capacitance characteristics in Fig. 2.27: For drain source voltages above 50 V, C_{rss} is more than two orders of magnitude smaller than C_{iss}.[32]

(II) The ***gray line*** corresponds to gate source voltages well above V_{th} and drain source voltages within the linear region of the MOSFET's output characteristics. For two of the four capacitances different conditions apply compared to the previous paragraph. $C_{\text{MOS p}}$ is in inversion and $C_{\text{MOS n}^-}$ is represented by its oxide capacitance due to the accumulation layer below the oxide. Under these conditions, $C_{\text{DG chip}}$ and $C_{\text{GS chip}}$ have a similar order of magnitude. This can be seen in Fig. 2.27. C_{rss} increases more than two orders of magnitude

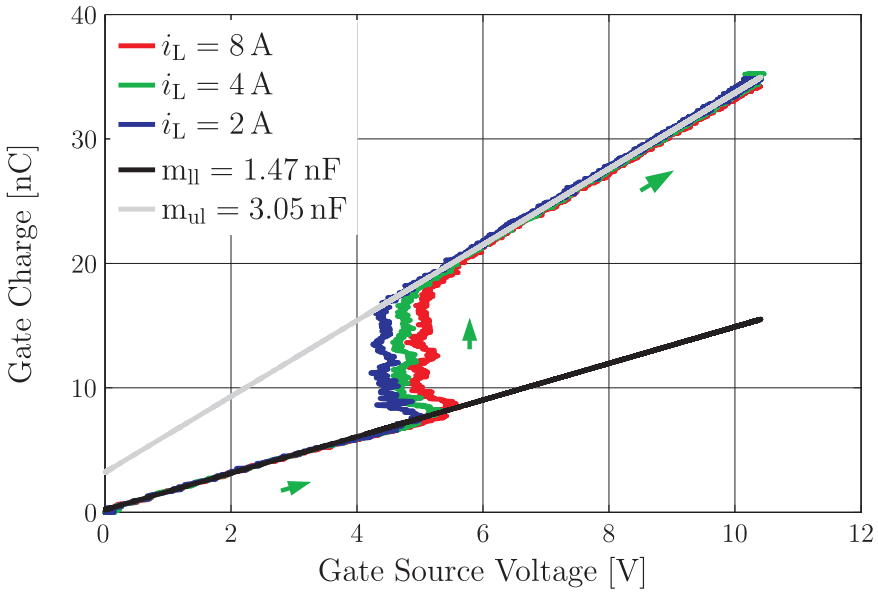
[30] The different commutation phases during turn-on and turn-off and the Miller plateau effect are e.g. described in [Brown 04] and [Jaunay 02].

[31] MOS capacitance with a n-type semiconductor has qualitatively the same characteristics as the p-type MOS capacitance shown in Fig. 2.2 on page 13 - but the voltage is reversed biased.

[32] The data sheet capacitances are measured in accordance with the standard DIN IEC 747. Thus, C_{rss} equals $C_{\text{dg chip}}$, C_{iss} is the sum of $C_{\text{gs chip}}$ and $C_{\text{dg chip}}$, and C_{oss} is the sum of $C_{\text{dg chip}}$ and $C_{\text{ds chip}}$ (cp. e.g. [Sattar 02] or [Consentino 08]). The presented measurement data has been generated with a small-signal capacitance measurement setups at *Infineon Technologies* in Munich.



(a) Gate charge characteristics $Q_{in}(v_{GS\,chip})$ of turn-off operations with different load currents i_L, $V_{DClink} = 400\,V$, $\vartheta_J = 25\,°C$ and an external gate resistance $R_{G\,ext}$ of $100\,\Omega$



(b) Gate charge characteristics $Q_{in}(v_{GS\,chip})$ of turn-on operations with different load currents i_L, $V_{DClink} = 400\,V$, $\vartheta_J = 25\,°C$ and an external gate resistance $R_{G\,ext}$ of $100\,\Omega$

Figure 2.26: Gate charge characteristics and gate source capacitance approximation with the slope m of the linear functions (black and gray lines) - The red and green arrows indicate how the curves are run through during commutation.

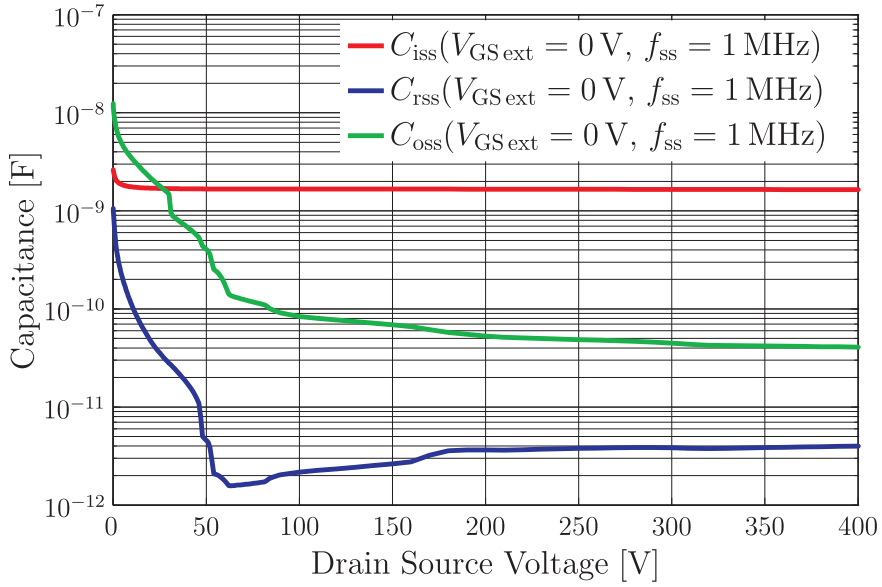


Figure 2.27: Data sheet capacitances of the DUT

from 50 V to 0 V.[33] The increase is due to the reduced space charge region width. Since the gate source voltage in the measurements is set to zero, the data sheet characteristics do not include the impact of the accumulation layer.

The difference between the black and the gray slopes in Fig. 2.26 is caused by the alteration of $C_{\mathrm{MOS\,p}}$ and $C_{\mathrm{MOS\,n^-}}$. In condition (II), the gate source capacitance $C_{\mathrm{GS\,chip}}$ can not be determined because $C_{\mathrm{DG\,chip}}$ has a similar order of magnitude as $C_{\mathrm{GS\,chip}}$. In condition (I), is more than two orders of magnitude smaller than $C_{\mathrm{GS\,chip}}$ and thus negligible. Therefore, $C_{\mathrm{GS\,chip}}$ of the MOSFET behavioral model is parameterized with the input capacitance C_{in} in condition (I) - the slope of the black line Fig. 2.26.[34]

The external gate resistance has no influence on the defined capacitance value. Gate charge characteristics of turn-off operations with $R_{\mathrm{G\,ext}} = 10\,\Omega$ have the same slope as the gray line in Fig. 2.26(a) for $v_{\mathrm{GS\,chip}}$ above the MILLER plateau voltage. Below the MILLER plateau voltage, oscillations of $v_{\mathrm{GS\,chip}}$ disable the determination of the input capacitance. Gate charge characteristics of turn-on operations with $R_{\mathrm{G\,ext}} = 10\,\Omega$ have the same slope as the black line in Fig. 2.26(b) for $v_{\mathrm{GS\,chip}}$ below the threshold voltage. Above the Miller plateau voltage, oscillations of $v_{\mathrm{GS\,chip}}$ disable the determination of the input capacitance.

An alteration of the junction temperature leads to an altered V_{th}.[35] The defined $C_{\mathrm{GS\,chip}}$ value is not affected by a shift of V_{th} as long as this shift is considered. The alteration of T_{J} also changes the electron mobility.[35] For gate source voltages between 0 V and V_{th}, this has no impact on the space charge regions and the corresponding capacitances. Therefore, it can be assumed that the proposed $C_{\mathrm{GS\,chip}}$ value is independent of temperature.

[33] This is also the reason for the increased C_{iss} values near zero volt.

[34] The determined gate source capacitance value of 1.47 nF is similar to the value 1.63 nF which results from $C_{\mathrm{iss}}(v_{\mathrm{DS}} = 400\,\mathrm{V}) - C_{\mathrm{rss}}(v_{\mathrm{DS}} = 400\,\mathrm{V})$.

[35] Details on the temperature dependency are given in **2.3.1.4** on page 37 et seq..

2.4.1.3 Determination of the Drain Gate and the Drain Source Capacitance

According to equation (2.64) on page 51, the approximated gate source capacitance $C_{\mathrm{GS\,chip}}$ is used for the calculation of the voltage dependent capacitances $C_{\mathrm{DG\,chip}}$ and $C_{\mathrm{DS\,chip}}$ with

$$C_{\mathrm{DG\,chip}} = \frac{i_{\mathrm{DG\,chip}}(t)}{\frac{\mathrm{d}v_{\mathrm{DG\,chip}}}{\mathrm{d}t}} = \frac{-i_{\mathrm{G\,meas}}(t) + C_{\mathrm{GS\,chip}} \cdot \frac{\mathrm{d}v_{\mathrm{GS\,chip}}}{\mathrm{d}t}}{\frac{\mathrm{d}v_{\mathrm{DG\,chip}}}{\mathrm{d}t}} \quad \text{and} \tag{2.67}$$

$$C_{\mathrm{DS\,chip}} = \frac{i_{\mathrm{DS\,chip}}(t)}{\frac{\mathrm{d}v_{\mathrm{DS\,chip}}}{\mathrm{d}t}} = \frac{i_{\mathrm{D\,meas}}(t) - i_{\mathrm{Ch}}(t) - C_{\mathrm{DG\,chip}} \cdot \frac{\mathrm{d}v_{\mathrm{DG\,chip}}}{\mathrm{d}t}}{\frac{\mathrm{d}v_{\mathrm{DS\,chip}}}{\mathrm{d}t}}. \tag{2.68}$$

Results of such calculations are depicted in Fig. 2.28 and Fig. 2.29.

Drain Gate Capacitance

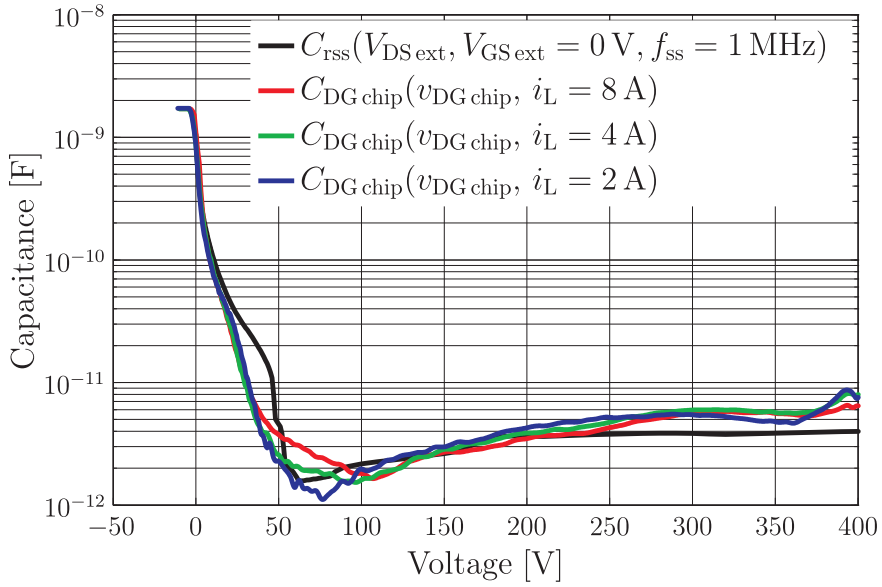
In Fig. 2.28(a), dynamic drain gate capacitance characteristics are shown as a function of the drain gate voltage, and in Fig. 2.28(b) as a function of the drain source voltage. As reference, C_{rss} is also depicted in Fig. 2.28. The comparison of C_{rss} and the different $C_{\mathrm{DG\,chip}}$ reveals the impact of the accumulation layer beneath the oxide on the capacitance for drain source voltages beneath 20 V, and that the space charge regions in the DUT widen differently if a channel current is flowing or not (see [Lagies 01a] or [Lagies 01b]). However, both diagrams show that different load currents and therewith, different gate source voltages have little impact on the drain gate capacitance during the voltage commutation.[36] In the voltage range, in which the smallest $C_{\mathrm{DG\,chip}}$ values occur, the current dependent cross sectional areas long the drain channel have a relatively small impact on $C_{\mathrm{DG\,chip}}$ (for details on the cross sectional areas, see [Lagies 01a] or [Lagies 01b]). With respect to the $C_{\mathrm{DG\,chip}}$ characteristics in Fig. 2.28(a), it is concluded that the drain gate capacitance of the MOSFET is sufficiently represented by a two-dimensional characteristics. Thereby, for the DUT, either the dependency on the drain gate voltage or the dependency of the drain source voltage may be implemented in the behavioral model.[37]

As mentioned in **2.4.1.1** on page 48 et seq., high demands exist regarding the measurement setup and equipment. The DUT - a super fast SJ MOSFET - brings the used measurement setup and equipment to their limits. The measurement data of turn-on operations of the MOSFET can not be evaluated because of gate current and gate source voltage oscillations.[38] Due to oscillations, the drain gate capacitance of relatively fast turn-off operations with $R_{\mathrm{G\,ext}} = 10\,\Omega$ can also not be analyzed. Up to a drain source voltage of approximately 30 V, the drain gate capacitances equal the drain gate capacitances in Fig. 2.28. For higher drain source voltages, the calculated capacitance characteristics are not reasonable. Furthermore, due to the measured signals' noise, no single capacitance characteristic can be determined without filtering the measurement data. The filtering, however, is challenging

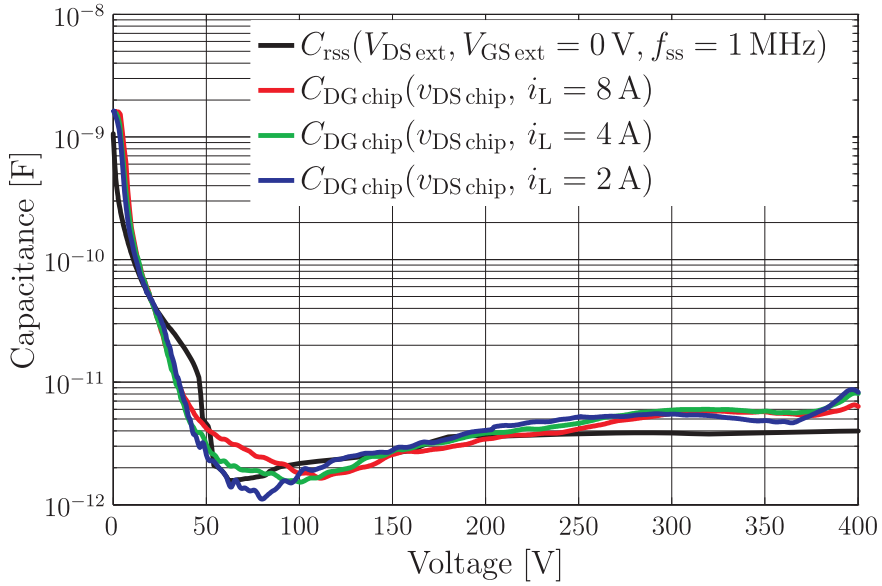
[36] The Miller plateau voltages during the voltage commutations are shown in Fig. 2.26 on page 53.

[37] A zoom in Fig. 2.28(b) would show a slight shift in the $C_{\mathrm{DG\,chip}}(v_{\mathrm{DS\,chip}})$ characteristics. Due to the high transconductance of the DUT, the neglect of this shift hardly affects the models accuracy.

[38] See e.g. the altering gate source voltage in Fig. 2.26(b) on page 37 in the Miller plateau region.



(a) $C_{\mathrm{DG\,chip}}(v_{\mathrm{DG\,chip}})$ characteristics of turn-off operations with different load currents i_{L}, $V_{\mathrm{DClink}} = 400\,\mathrm{V}$, $\vartheta_{\mathrm{J}} = 25\,^{\circ}\mathrm{C}$ and an external gate resistance $R_{\mathrm{G\,ext}}$ of $100\,\Omega$ compared to C_{rss}



(b) $C_{\mathrm{DG\,chip}}(v_{\mathrm{DS\,chip}})$ characteristics of turn-off operations with different load currents i_{L}, $V_{\mathrm{DClink}} = 400\,\mathrm{V}$, $\vartheta_{\mathrm{J}} = 25\,^{\circ}\mathrm{C}$ and an external gate resistance $R_{\mathrm{G\,ext}}$ of $100\,\Omega$ compared to C_{rss}

Figure 2.28: Comparison of the DUT's small-signal feedback capacitance C_{rss} and drain gate capacitances $C_{\mathrm{DG\,chip}}$ determined from switching characteristics

itself. The slopes of the drain source and gate source voltage vary orders of magnitude during the different phases of switching. The measurement data of each switching operation is hence filtered and evaluated for different filter parameters. Afterwards, the determined capacitance characteristics are put together in sections. For higher drain source voltages and especially in the voltage range where the minimum capacitance values occur, the determined drain gate capacitance values depend on the applied filter parameters. Minimal oscillation amplitudes on the gate current and the gate source voltage further increase the sensitivity at higher voltages. An improved measurement setup and improved measurement equipment will probably overcome these obstacles. In this work, based on the observation that the $C_{\mathrm{DG\,chip}}$ characteristics in Fig. 2.28(b) vary little for the different switching conditions and match relatively well with the C_{rss} characteristics for higher drain source voltages, the following workaround is proposed for the DUT:

A typical $C_{\mathrm{DG\,chip}}$ characteristic is determined from the characteristics in Fig. 2.28(b). The first intersection point with C_{rss} is determined. For drain source voltages smaller than the intersection point voltage, the dynamic drain gate capacitance values are considered, and for drain source voltages bigger than the intersection point voltage, the feedback capacitance values are used. The resulting characteristics $C_{\mathrm{DG\,dyn}}$ is shown in Fig. 4.2 on page 100. $C_{\mathrm{DG\,dyn}}$ is used for the parameterization of $C_{\mathrm{DG\,chip}}$ of the MOSFET behavioral model. Therewith, the advantages of the dynamic drain gate capacitance characteristics at lower voltages are implemented in the model. The impact of the gate source voltage and the channel current respectively at higher drain source voltages is disregarded with this approach.

$C_{\mathrm{DG\,chip}}$ is a MOS capacitance and, thus, composed of a series connection of the corresponding depletion and oxide capacitance. For specified operating temperatures, the number and place of the corresponding ionized impurities in the n^- region should not alter. A temperature dependency of $C_{\mathrm{DG\,chip}}$ is hence not expected. However, the drain current is temperature dependent and Fig. 2.28 shows: The channel current has an impact on the how the space charge regions spread between the columns and on the cross sectional areas long the drain channel respectively. Accordingly, $C_{\mathrm{DG\,chip}}$ can be influenced by T_{J}. Continuative works could analyze the impact of a temperature dependent channel current on the DUT's space charge regions by means of device simulations. For the stability analysis in section **5** on page 111 et seq., a temperature independent $C_{\mathrm{DG\,chip}}$ characteristic is assumed.

Drain Source Capacitance

In Fig. 2.29(a), drain source capacitance characteristics are shown for relatively slow switching operations with $R_{\mathrm{G\,ext}} = 100\,\Omega$. In Fig. 2.29(b), drain source capacitance characteristics of relatively fast switching operations with $R_{\mathrm{G\,ext}} = 10\,\Omega$ are depicted. As reference, the small-signal capacitance C_{oss} is also shown.[39] The comparison of C_{oss} and the different $C_{\mathrm{DS\,chip}}$ shows also that the space charge regions in the DUT widen differently if a channel current is flowing or not (see [Lagies 01a] or [Lagies 01b]). The dynamic characteristics in

[39] According to [Sattar 02], the C_{DS} equals the difference of C_{oss} and C_{rss}. C_{rss} is over an order of magnitude smaller than C_{oss}. Thus, the impact of C_{rss} on the C_{DS} is almost negligible.

Fig. 2.29(a) reveal a strong dependency of $C_{\mathrm{DS\,chip}}$ on the gate source voltage during the voltage commutation. In contrast, the characteristics in Fig. 2.29(b) seem to be almost independent of the switching conditions. In Fig. 2.29(a), the dynamic drain source capacitances exceed C_{oss} considerably. With decreasing external gate resistances, the $C_{\mathrm{DS\,chip}}$ characteristics approach the C_{oss} characteristic - probably because the measurement conditions of C_{oss} and $C_{\mathrm{DS\,chip}}$ become more and more similar: For relatively fast switching operations, the channel channel current is close to zero or zero during the turn-off voltage commutation (see Fig. 4.3(a) and Fig. 4.3(c) on page 102 and 104) - as in the C_{oss} measurement.

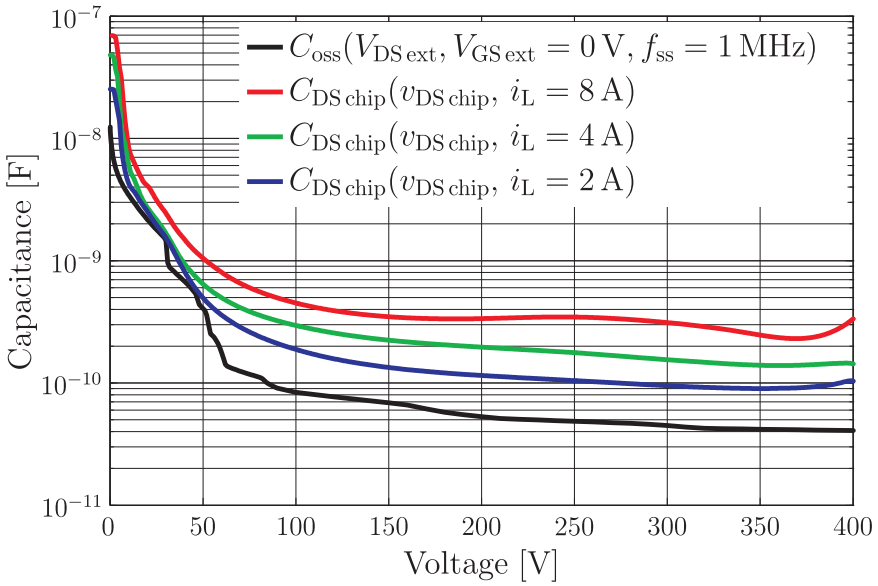
The small-signal capacitance C_{iss} and C_{rss} have the same order of magnitude as the determined dynamic capacitances $C_{\mathrm{GS\,chip}}$ and $C_{\mathrm{DG\,chip}}$. The different orders of magnitude between C_{oss} and the dynamic drain source capacitances $C_{\mathrm{DS\,chip}}$ in Fig. 2.29(a) are surprising. There are two possibilities: either the increase of the capacitance is real or it is due to a systematic error in the determination routine. The major difference between the determination of the dynamic gate capacitances $C_{\mathrm{GS\,chip}}$ and $C_{\mathrm{DG\,chip}}$ and the dynamic drain source capacitance $C_{\mathrm{DS\,chip}}$ is that $C_{\mathrm{GS\,chip}}$ and $C_{\mathrm{DG\,chip}}$ are solely based on dynamic measurement data and that $C_{\mathrm{DS\,chip}}$ is based on both dynamic and static measurement data. A possible cause for the increased $C_{\mathrm{DS\,chip}}$ could be a mismatch of the used static characteristics and the dynamic measurement data. As discussed in **2.3.1.4** on page 37 et seq., the self-heating during the static measurements results in a measured channel current that corresponds to a junction temperature that is higher than the initial junction temperature. With respect to Fig. 2.17 on page 35 and Fig. 2.22 on page 43, for operating points beyond the output characteristics' linear region, it is concluded that the calculated channel current is higher than the actual channel current during the dynamic measurement. Accordingly, $i_{\mathrm{DS\,chip}}$ would be underestimated in equation (2.68), and the actual drain source capacitance would exceed the calculated drain source capacitance. However, the space charge capacitance of a pn-junction is also temperature dependent due to the temperature dependent built-in voltage $V_{\mathrm{bi}}(T_{\mathrm{J}})$ [Lagies 01a]. For a pn-junction in thermal equilibrium, $V_{\mathrm{bi}}(T_{\mathrm{J}})$ is approximately given by

$$V_{\mathrm{bi}}(T_{\mathrm{J}}) \approx \frac{\mathrm{k} \cdot T_{\mathrm{J}}}{q} \cdot \ln\left(\frac{N_A \cdot N_D}{\mathrm{n_i}(T_{\mathrm{J}})^2}\right) \tag{2.69}$$

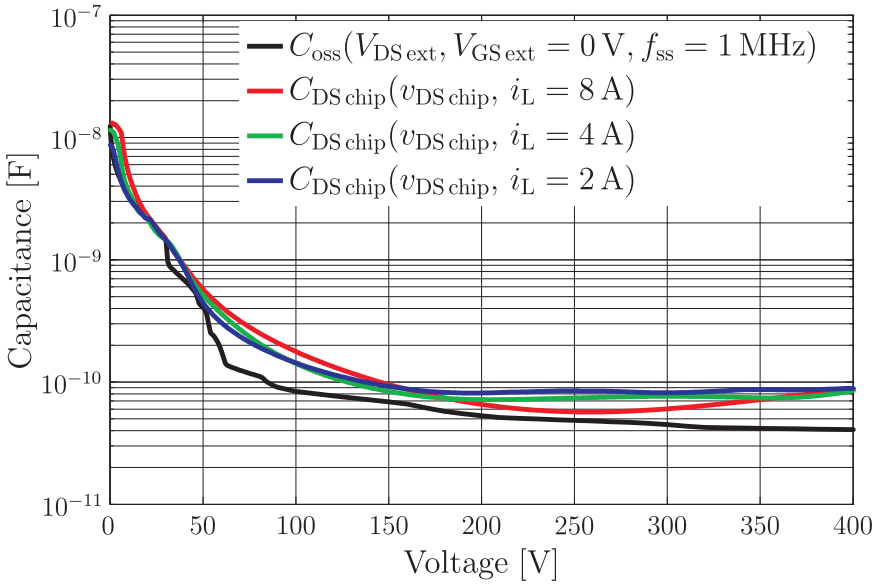
with the temperature dependent intrinsic density $\mathrm{n_i}(T_{\mathrm{J}})$ (for details, see e.g. [Lutz 11]). Therewith, the built-in voltage of the pn-junction's space charge region and, thus, the space charge region itself, could be different in the static measurements and the corresponding points in time of the dynamic measurements. The different space charge region may correspond to different MOS and drain channel resistances and, therefore, the channel current could be different in the static measurements and the corresponding points in time of the dynamic measurements. However, since $C_{\mathrm{DS\,chip}}$ is significantly increased at high *and* low drain source voltages, this seems to be unlikely.[40] Future works could quantify this effect by means of device simulations. If the increase of the capacitance is real, device simulations could also help to explain the effect.[41] In [Brocke 10], it is shown, that the same effect can

[40] The temperature increase during the static measurements is relatively small in the linear region of the MOSFET's output characteristics. See Fig. 2.20 on page 39.

[41] However, geometric device models are also simplified reflections of the reality and may not be able to



(a) Drain source capacitance characteristics of turn-off operations with different load currents i_L, $V_{DClink} = 400\,V$, $\vartheta_J = 25\,°C$ and an external gate resistance $R_{G\,ext}$ of $100\,\Omega$



(b) Drain source capacitance characteristics of turn-off operations with different load currents i_L, $V_{DClink} = 400\,V$, $\vartheta_J = 25\,°C$ and an external gate resistance $R_{G\,ext}$ of $10\,\Omega$

Figure 2.29: Comparison of the DUT's data sheet small-signal output capacitance C_{oss} and drain source capacitances $C_{DS\,chip}$ determined from switching characteristics

be observed in a conventional power MOSFET. In this work, the cause of the increased $C_{\mathrm{ds\,chip}}$ is not further analyzed. At present, a systematic error in the determination routine of $C_{\mathrm{DS\,chip}}$ can not entirely be excluded. The operating point dependent $C_{\mathrm{DS\,chip}}$ of the behavioral MOSFET model is hence parameterized - as usually - with

$$C_{\mathrm{DS\,chip}} = C_{\mathrm{oss}} - C_{\mathrm{rss}}. \tag{2.70}$$

Therewith, the impact of the channel current and the gate source voltage respectively on the drain source capacitance is meanwhile neglected. However, the variation of the parameterization of $C_{\mathrm{DS\,chip}}$ during the stability analysis of the commutation cell enables conclusions on the stability of commutation cells in case $C_{\mathrm{DS\,chip}}$ is in fact greater than C_{oss}.[42]

As $C_{\mathrm{DG\,chip}}$, $C_{\mathrm{DS\,chip}}$ can be influenced by T_{J}. The drain current is temperature dependent and the channel current has an impact on the how the space charge regions spread between the columns and on the cross sectional areas long the drain channel respectively. Additionally as discussed in the previous paragraph, the build-in voltage of the pn-junction is temperature dependent. Continuative works could analyze the impact of a temperature on the DUT's space charge regions by means of device simulations. For the stability analysis in chapter **5** on page 111 et seq., a temperature independent $C_{\mathrm{DS\,chip}}$ characteristic is assumed.

2.4.1.4 Discussion of Systematic Error Sources and Evaluation of the Dynamic Parameterization of the Power MOSFET

The data sheet capacitances in Fig. 2.27 on page 54 represent the DUT's capacitances in the blocking region. Due to the given reasons in **2.4.1.3** on page 55 et seq., the C_{oss} characteristic and parts of the C_{rss} characteristic are used for the parameterization of the dynamic capacitances of the MOSFET's behavioral model. The C_{rss} measurement and the C_{oss} measurement are standard measurements. Their accuracy is not discussed in this work. It is assumed that parasitic capacitances of the measurement setups can be neglected for the determined characteristics and that the difference between the measured and chip-internal drain source voltage is insignificant.

Considered systematic error sources in the dynamic measurement data are ...

- ... the resolution of the used oscilloscope, ...
- ... the probes delay times, ...
- ... offsets in the measured current and voltage characteristics, ...
- ... parasitic circuit elements between the voltage probing points and the contact points of the semiconductor chip, ...

model the cause. 2D device models might be insufficient.

[42] If future works verify the determined gate source voltage dependency of the $C_{\mathrm{DS\,chip}}$, the switching loss calculation needs to be reconsidered. The locus curves $i_{\mathrm{Ch}}(v_{\mathrm{DS\,chip}})$ during turn-on and -off differ. Therewith, different drain source capacitance characteristics may apply to the turn-on and -off. An exact loss calculation is then only possible if the drain current distribution between channel current and output capacitance current is considered (see [Höch 09b] for details and compare [Höch 09b] with [Xiong 09]).

- ... parasitic chip-external capacitances, and ...
- ... the self-heating of the DUT during the dynamic measurement.

Subsequently, the impact of the different sources of error is estimated:

(I) The ***limited resolution of the used oscilloscope*** causes errors in the dynamic measurement data. The oscilloscope's resolution does not affect the average slope of $Q_{\mathrm{in}}(v_{\mathrm{GS\,chip}})$. Therewith, it has no impact on the determined input capacitance C_{in} in Fig. 2.26 on page 53. The ***horizontal resolution of the oscilloscope*** enables the sampling of sufficient points in time during voltage commutation. Due to the ***vertical resolution of the used oscilloscope***, low drain source voltages have the highest absolute measurement error. Therefore, each switching condition is measured twice. The first measurement senses the entire drain source voltage range with the highest possible resolution, the second measurement records only a zoom of the lower drain source voltage. Before the calculation of the dynamic capacitances the two characteristics are put together. The variation of the gate source voltage is significantly smaller than the variation of the drain source voltage. Hence, no zoomed gate source measurement is necessary. Remaining voltage errors average out because not absolute voltages but voltage differences are used for the capacitance calculation in (2.67) and (2.68) on page 55. (2.67) and (2.68) contain absolute current values. However, the error in $i_{\mathrm{D\,meas}}(t)$ and $i_{\mathrm{G\,meas}}(t)$ is below 1 % of $\max|i_{\mathrm{D\,meas}}(t)|$ and $\max|i_{\mathrm{G\,meas}}(t)|$ respectively. Therewith, the limited resolution of the used oscilloscope has no noteworthy impact on the accurracy of the capacitance characteristics.

(II) The ***probes' delay times*** are another error source. The presented measurements in section **4.1** on page 95 et seq. show that the delay times of current and voltage probes are well matched. Thus, the delay times do not influence the accuracy of the defined capacitances.

(III) ***Offsets in the measured current and voltage signals*** cause also errors in the dynamic measurement data. Before the capacitance calculation, an offset correction is carried out for the current and gate source voltage characteristics. The offset of the measured drain source voltage is corrected by means of the linear region of the output characteristics. Therewith, the impact of signal offsets is minimized.

(IV) ***Parasitic inductances and resistances*** between the voltage probing points and the semiconductor chip cause differences between the measured and the chip-internal voltages. The chip voltages are calculated as described in subsection **3.3.2** on page 85 et seq.. Accordingly, parasitic voltage drops are eliminated as an error source.

(V) ***Parasitic chip-external capacitances*** cause differences between the measured currents and the currents that flows into the chip contacts. The parasitic capacitances of the transistor's package and the PCB of buck converter topology have a magnitude of a few picofarad (see subsection **3.2.3** on page 75 et seq. for details). While $C_{\mathrm{DS\,chip}}$ and $C_{\mathrm{GS\,chip}}$ are over one order of magnitude bigger than the parasitic chip-external capacitances, $C_{\mathrm{DG\,chip}}$ has the same order of magnitude at higher drain source voltages as the parasitic chip-internal capacitances. Due to the former, it can be assumed that $i_{\mathrm{D\,meas}}$ sufficiently represent the current that flows into the drain contact and that the impact of parasitic

chip-external capacitances on the determined $C_{\mathrm{GS\,chip}}$ is insignificant.[43] However, during the drain source voltage commutation at higher drain source voltages, a significant proportion of the gate current flows through the parasitic chip-external drain gate capacitance $C_{\mathrm{DG\,ext}}$. Hence, during voltage commutation, the current that flows into the gate contact *and* the current that flows through the chip-external drain gate capacitance is represented by $i_{\mathrm{G\,meas}}$. As a result, the calculated chip-internal drain gate capacitance is increased by $C_{\mathrm{DG\,ext}}$. The difference of the chip-external drain gate capacitance and the calculated chip-internal drain gate capacitance represents the actual $C_{\mathrm{DG\,chip}}$. For the DUT and the used dynamic measurement setup, $C_{\mathrm{DG\,ext}}$ is only relevant for drain source voltages above 40 V. Due to the given reasons in **2.4.1.3** on page 55 et seq., this part of the dynamic drain gate capacitance is not used for the parameterization of $C_{\mathrm{DG\,chip}}$. The impact of the chip-external capacitances on the dynamic part of the $C_{\mathrm{DG\,chip}}$ characteristic is insignificant.

(VI) The maximum junction temperature increase due to the DUT's ***self-heating*** during the realized double pulse measurements is estimated - in accordance with the calculation and assumptions on page 32 - with 2 K. Hence, the impact of temperature on the dynamic measurement data is negligible.

Therewith, it is assumed that the defined dynamic capacitances are determined with a sufficient accuracy. The estimation of a maximum relative error of the determined dynamic capacitance characteristics is not possible. Thereto, a reference measurement, which determines the capacitance characteristics over the considered operating range of the DUT, or an analytic description of the defined capacitances is needed. By comparing sample simulations of switching characteristics with the corresponding measurement data, an exemplary evaluation of the modeled MOSFET with the defined capacitances is presented in subsection **4.1** on page 95 et seq.. The comparison shows simulated and measured switching characteristics match relatively well as long as $C_{\mathrm{DS\,chip}}$ is not limiting the $\mathrm{d}v_{\mathrm{DS\,chip}}/\mathrm{d}t$.

Due to the defined $C_{\mathrm{GS\,chip}}$ value in **2.4.1.2** on page 51 et seq., both the difference between $C_{\mathrm{MOS\,n^-}}$ during depletion and accumulation, and the difference between $C_{\mathrm{MOS\,p}}$ during depletion and inversion are dedicated to $C_{\mathrm{DG\,chip}}$. The approximation of $C_{\mathrm{GS\,chip}}$ with a constant value results in overestimated $C_{\mathrm{DG\,chip}}$ values in time ranges with too small $C_{\mathrm{GS\,chip}}$ values, and underestimated $C_{\mathrm{DG\,chip}}$ values in time ranges with too high $C_{\mathrm{GS\,chip}}$ values.[44] In accordingly parameterized switching behavioral models, the gate charge is accurately modeled and the drain source voltage slopes are hardly affected. However, the simulated gate source voltage might differ from the measured gate source voltage due to an inaccurately modeled capacitive voltage divider.[45] Despite this disadvantage, the proposed parameterization

[43] Due to the difference in magnitude of the parasitic chip-external capacitances and $C_{\mathrm{DS\,chip}}$, the impact of the chip-external capacitances on the $C_{\mathrm{DS\,chip}}$ characteristics in Fig. 2.29 on page 59 can also be neglected.

[44] A reasonable variation of the determined gate source capacitance value has only an observable influence on $C_{\mathrm{DG\,chip}}$ of negative and low drain gate voltages. During the steep part of the voltage commutation, the slope of $v_{\mathrm{DG\,chip}}$ is significantly larger than the slope of $v_{\mathrm{GS\,chip}}$. Thus, the fraction of the calculated $C_{\mathrm{DG\,chip}}$ that corresponds to the alteration of the actual gate source capacitance is considerably smaller than the absolute alteration of the actual gate source capacitance. Therefore, the impact of $C_{\mathrm{GS\,chip}}$ on $C_{\mathrm{DG\,chip}}$ at higher drain gate voltages is insignificant.

[45] The usage of C_{iss} and C_{rss} in Fig. 2.27 results also in an inaccurately modeled voltage divider so that no disadvantage arises compared to the usage of data sheet capacitances.

of $C_{\mathrm{GS\,chip}}$ and $C_{\mathrm{DG\,chip}}$ is superior to a parameterization with $C_{\mathrm{GS\,chip}} = C_{\mathrm{iss}} - C_{\mathrm{rss}}$ and $C_{\mathrm{DG\,chip}}) = C_{\mathrm{rss}}$, because the data sheet capacitances do not consider ...

- ... the impact of the accumulation layer on $C_{\mathrm{MOS\,n^+}}$ for positive gate source voltages.
- ... the impact of alteration of the space charge region width corresponding to $C_{\mathrm{MOS\,p}}$ for positive gate sources voltages between zero volt and the threshold voltage.
- ... the impact of the electron inversion layer on the gate charge.
- ... the impact of the accumulation layer on $C_{\mathrm{MOS\,n^-}}$.

Fig. 4.1 on page 98 shows that the consideration of the accumulation and inversion layers at low drain source voltages and gate source voltages above the threshold voltage is necessary for an accurate modeling of the gate circuit's time constants and the gate charge. The charge in the accumulation and inversion layers belongs partly to the gate source capacitance. However, on the basis of gate charge characteristics, it is not possible to distinguish the capacitive effects of the accumulation and the inversion layer beneath the gate. Therewith, it is not possible to assign the exact charge to $C_{\mathrm{GS\,chip}}$.[46]

2.4.2 Dynamic Characterization of Schottky Diodes

This subsection discusses briefly the determination of the capacitance voltage characteristic for the SCHOTTKY diode behavioral model in Fig. 2.11 on page 25. The $C_{\mathrm{AC\,chip}}(v_{\mathrm{AC\,chip}})$ characteristic is needed for the simulation of switching characteristics in chapter **4** on page 95 et seq. and chapter **5** on page 111 et seq..

A dependency of the anode cathode capacitance $C_{\mathrm{AC\,chip}}$ on the switching conditions is not expected due to the following reasons:

- Minority charge carriers are negligible in a SCHOTTKY diode. Therewith, the diode has no reverse and no forward recovery [Inf 08b].
- $C_{\mathrm{AC\,ss}}(V_{\mathrm{AC\,ext}})$ represents the space charge region in the $\mathrm{n^-}$ region beneath the SCHOTTKY contact. For specified operating temperatures, the number and place of the corresponding ionized donor atoms should not alter. A temperature dependency of $C_{\mathrm{AC\,ss}}(V_{\mathrm{AC\,ext}})$ is hence not expected [Inf 08b].

A setup for the measurement of the small-signal capacitance voltage characteristic at *Infineon Technologies* is used for the determination of the anode cathode capacitance characteristic. The result of the small-signal measurement is presented in Fig. 2.30.

The measurement of a diode's small-signal capacitance versus its reverse voltage is a standardized measurement. The accuracy of the capacitance characteristic in Fig. 2.30 is not discussed in this work. It is assumed that parasitic capacitances of the measurement setup

[46] With the aid of the charge partitioning described in [Ward 78] and device simulations, a methodology for a reasonable charge splitting on $C_{\mathrm{GS\,chip}}$ and $C_{\mathrm{DG\,chip}}$ may be found in continuative works.

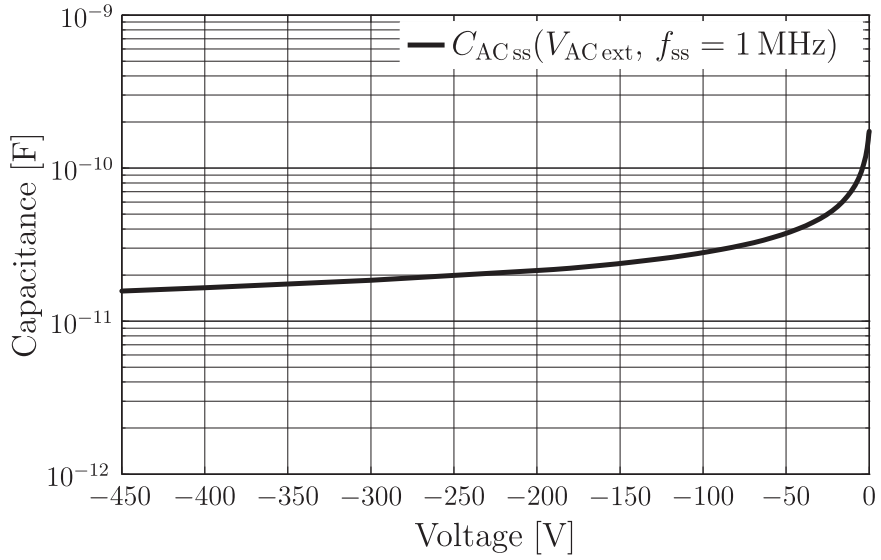


Figure 2.30: Data sheet capacitance of the used SiC SCHOTTKY diode (cp. [Inf 08b])

have no significant impact on the capacitance characteristic and that the differences between the measured and the chip-internal anode cathode voltages are negligible.

$C_{\mathrm{AC\,chip}}$ of the SCHOTTKY diode behavioral model is parameterized with $C_{\mathrm{AC\,ss}}$ in Fig. 2.30. $C_{\mathrm{AC\,chip}}$ influences the reduction of the drain current during the turn-off voltage commutation, and the increase of the drain current during the turn-on voltage commutation. An inaccurate $C_{\mathrm{AC\,chip}}$ characteristic can lead to differences between the measured and the simulated $\mathrm{d}v_{\mathrm{DS\,chip}}/\mathrm{d}t$ and the measured and the simulated MILLER plateau. Since $C_{\mathrm{AC\,chip}}$ is not included in the small-signal equivalent circuit model in Fig. 5.2 on page 114, $C_{\mathrm{AC\,chip}}$ has no impact on the stability analysis presented in chapter **5** on page 111 et seq..

3 Modeling of Electrical Interconnections of Packages and PCBs in Commutation Cells

In this chapter, the modeling of the electrical interconnections of packages and PCBs is regarded. As shown in section **3.1**, the interconnections of the considered packages and PCB are electrically small compared to the wavelength that corresponds to the highest relevant frequency of the considered voltage and current signals' harmonic content. Therefore, the interconnections can be modeled with lumped circuit elements. A circuit model with lumped circuit elements is described in **3.1**. The equivalent circuit element extraction of the packages and the PCB is presented in section **3.2**. Application dependent simplifications and parameterizations of the equivalent circuit model are discussed in section **3.3**. In chapter **4** on page 95 et seq., the proposed modeling is evaluated.

3.1 Equivalent Circuit Model of Electrical Interconnections

Electromagnetic phenomena in electrical interconnections can be calculated with MAXWELL's equations [Maxwell 65]. For materials that are described by their electric permittivity ε, their electric conductivity σ and their magnetic permeability μ, MAXWELL's equations relate the electric field to the magnetic field and show that both fields are coupled. MAXWELL's equations can be solved by an iterative process (see e.g. [Fano 63]). The disregard of all time derivatives gives the zero-order solution - the DC solution - of MAXWELL's equations. The DC solution is then used for the first-order solution. Subsequently, the first-order solution is used for the second-order solution, and so forth. The sum of the partial solutions converges to the solution of MAXWELL's equations.

In case the size of the considered structure is electrically small, the couplings between the magnetic and the electric field can be neglected. Provided that the structure does not have a long internal path length, a rough estimate of the structure's size limit is given by one tenth of the wavelength that corresponds to the highest relevant frequency of the considered signals' harmonic content (see e.g. [Paul 09]).

The electromagnetic wave length λ is proportional to the wave's propagation velocity v and inversely proportional to the wave's frequency f (see e.g. [Stöcker 07]):

$$\lambda = \frac{1}{f \cdot \sqrt{\varepsilon \cdot \mu}} = \frac{c_0}{f \cdot \sqrt{\varepsilon_r \cdot \mu_r}} = \frac{v}{f} \tag{3.1}$$

with the velocity of light c_0, the relative permittivity ε_r and the relative permeability μ_r.

Table 3.1: Frequency dependent wave length in different materials

Material	ε_r	μ_r	v $[10^6 \cdot {}^m/_s]$	λ(200 MHz) [cm]	λ(1 GHz) [cm]
aluminum	1.00	1.00	≈ 299.79	≈ 150	≈ 30.0
brass	1.00	1.00	≈ 299.79	≈ 150	≈ 30.0
copper	1.00	1.00	≈ 299.79	≈ 150	≈ 30.0
FR-4	4.40	1.00	≈ 142.92	≈ 71	≈ 14.2
MP-195	4.50	1.00	≈ 141.32	≈ 71	≈ 14.2
silicon	11.90	1.00	≈ 86.91	≈ 43	≈ 8.6
silicon carbide	9.70	1.00	≈ 96.26	≈ 48	≈ 9.6
solder	1.00	1.00	≈ 299.79	≈ 150	≈ 30.0

For switching operations, the maximum frequency of interest is usually in the range of three to five times the switching slopes' maximum equivalent frequency $f_{\text{equ max}}$ [Tek 08]. For analysis of parasitic oscillations during commutation, the maximum frequency of interest is given by the maximum of the switching slopes' maximum equivalent frequency and the maximum oscillation frequency during commutation:

(I) Different signal dependent definitions for the calculation of a slope's equivalent frequency exist in literature (see e.g. [Tek 08] and [Witcher 02]). For this work, the steep parts of the considered switching slopes are sufficiently described by linear functions. Hence, the signals' maximum equivalent frequency is defined with

$$f_{\text{equ max}} := \max\left\{\frac{0.25}{t_{\text{r min}}}, \frac{0.25}{t_{\text{f min}}}\right\} \tag{3.2}$$

with the minimum rise and fall times $t_{\text{r min}}$ and $t_{\text{f min}}$. The equation assumes that the signals' rise and fall times represent 80 % of their slopes (see e.g. [Witcher 02]). The ***maximum equivalent frequency of the considered switching characteristics*** in chapter **4.1** on page 95 is below 50 MHz. Therewith, the maximum frequency of interest would be in a range of 200 MHz. In Table 3.1, the wave length of 200 MHz is calculated for PCB and packaging materials. If the surrounding medium of the conductive PCB and packaging materials is free space, the length of electromagnetic waves propagating along the connectors is approximately 1.5 m. In PCBs, the wave length is about 60 % of that value [Paul 09]. Therewith, with respect to the switching slopes' maximum equivalent frequency, the PCB and package structures in Fig. 3.2 on page 71 and Fig. 3.6(a) on page 76 can be considered as electrically small. Accordingly, the couplings between the magnetic and the electric field could be neglected for the approximation of the structures' parameters. For structures that are not electrically small, full-wave solvers, which consider the two-way coupling between electric and magnetic fields, should be used.

(II) The ***maximum oscillation frequency*** in the considered commutation cell during commutation is not known. In [Fujihira 08], frequencies between 20 MHz and 150 MHz are

mentioned for SMPSs with fast switching power MOSFETs. Similar (and higher) oscillation frequencies occur in the original dynamic measurement setup (see section **4.1** on page 95 for details) and in boost converter topologies with comparable power MOSFETs in the laboratories of *Infineon Technologies*. However, oscillations with much higher frequencies might occur during commutation. According to Table 3.1 and according to the assumption in the previous paragraph, the PCB and package structures in Fig. 3.2 and Fig. 3.6(a) can be assumed to be electrically small for oscillation frequencies of up to 1 GHz. Thus, the proposed large-signal modeling in subsection **3.3.3** on page 90 et seq. can be applied for the simulation and analysis of oscillations with frequencies up to 1 GHz.

Electrically small structures can be represented by lumped circuit elements [Aatre 80]. A common equivalent circuit model of electrically small interconnections is the T-model (see e.g. [Paul 08]). In Fig. 3.1(a), the T-model is illustrated for n coupled electrical interconnect sections. The model has n source and n sink terminals, and consists of a grounded capacitance conductance sub-circuit and a pair of serial resistance inductance sub-circuits. The capacitance conductance sub-circuit is shown in Fig. 3.1(b). The resistance inductance sub-circuit is shown in Fig. 3.1(c). With respect to NORTON's theorem,[1] instead of inductive coupling elements, current-controlled current sources are used for the modeling of mutual inductances. The self and mutual resistances are modeled accordingly.[2]

3.2 Extraction of Equivalent Circuit Elements

It is not possible to parameterize all RLCG parameters of the T-model by means of measurements. Field simulations enable the extraction of the RLCG parameters. In subsection **3.2.1**, the used simulation software is introduced and the simulation settings are given. The extracted parameters of the regarded packages and the regarded PCB are presented in subsection **3.2.2** and **3.2.3** respectively.

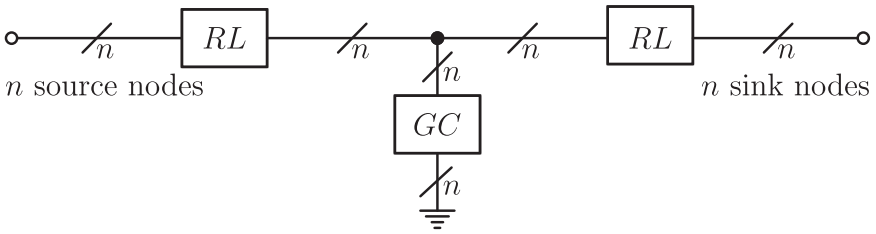
3.2.1 Computer Aided Parameter Extraction

The field simulation software *Q3D Extractor 10.0* of *ANSYS* is used for the extraction of the RLCG parameters of the considered interconnect sections. The software's solver neglects the couplings between the magnetic and the electric field.[3] The algorithm for the calculation of CG matrices considers frequency dependent material properties - such as permittivity and

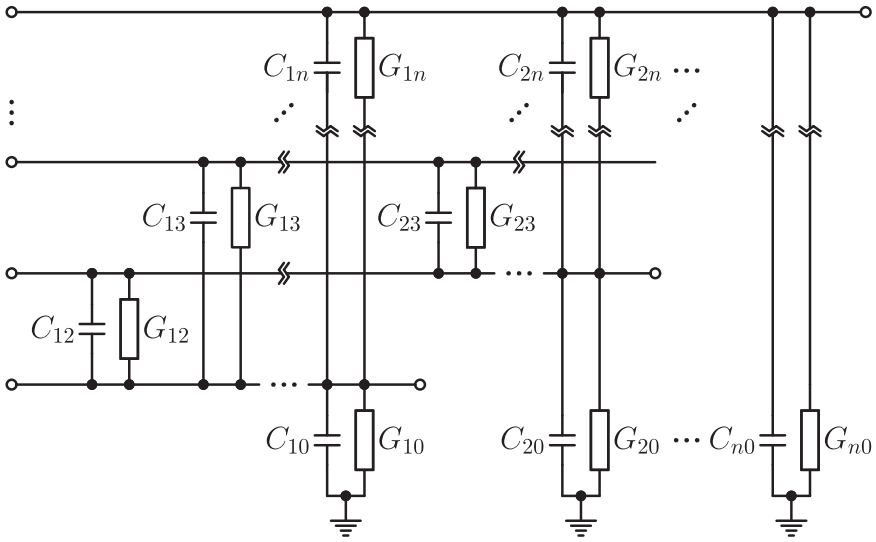
[1] NORTON's theorem states that from the viewpoint of any pair of terminals any linear circuit is electrically equivalent to an ideal current source in parallel with an impedance. See e.g. [Johnson 01] for details.

[2] The mutual resistance between two conductors represents the conductors' power dissipation through induced eddy currents. See e.g. [Bracken 00] for details.

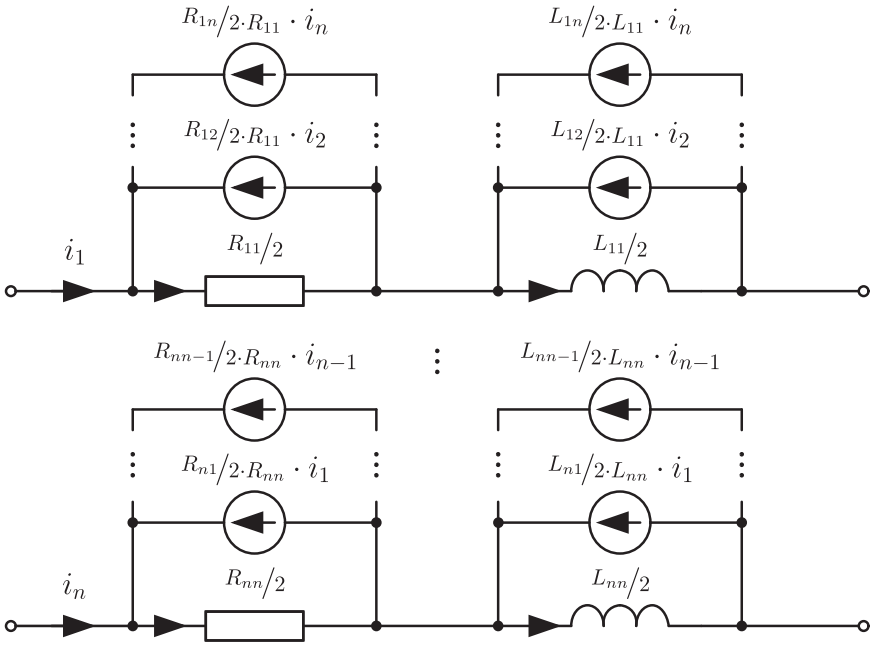
[3] This means that displacement currents are disregarded when the inductances and resistances are calculated, and that inductive voltage drops are neglected when capacitances and conductances are calculated.



(a) T-model of electrical interconnections (see e.g. [Bracken 05])



(b) Grounded CG sub-circuit (see e.g. [Bracken 05])



(c) Serial RL sub-circuit (see e.g. [Ans 99] and [Bracken 00])

Figure 3.1: Equivalent circuit model of electrical interconnections

loss tangent[4]; and the algorithm for the calculation of AC RL matrices considers the skin and proximity effect. Therewith, *Q3D Extractor* enables the determination of ...

- ... frequency dependent CG matrices, ...
- ... a DC RL matrix and ...
- ... frequency dependent AC RL matrices ...

of interconnect structures.[5] The extraction of the lumped RLCG parameters is based on the finite element method (FEM) and the boundary element method (BEM) (or method of moments) with a fast multipole method (FMM).[6] Information on partial and loop inductance concepts are for instance given in [Paul 09] and [Gutsmann 07]. The circuit models of self and mutual resistances and inductances in Fig. 3.1(c) indicate the transferability of the partial and loop inductance concepts to resistances.

The grounded CG sub-circuit in Fig. 3.1(b) is represented by the *Q3D Extractor* CG matrix. Since the capacitance solver is based on BEM, the ground represents a location infinitely far away from the modeled structure.[7] The equivalent circuit elements in Fig. 3.1(b) do not correspond directly to the entries of the *Q3D Extractor*'s MAXWELL matrices $\boldsymbol{M}_C$ and $\boldsymbol{M}_G$. For a design with three interconnect section, the MAXWELL matrices are given by

$$\boldsymbol{M}_C = \begin{pmatrix} C_{10}+C_{12}+C_{13} & -C_{12} & -C_{13} \\ -C_{21} & C_{20}+C_{21}+C_{23} & -C_{23} \\ -C_{31} & -C_{32} & C_{30}+C_{31}+C_{32} \end{pmatrix} \text{ and}$$

$$\boldsymbol{M}_G = \begin{pmatrix} G_{10}+G_{12}+G_{13} & -G_{12} & -G_{13} \\ -G_{21} & G_{20}+G_{21}+G_{23} & -G_{23} \\ -G_{31} & -G_{32} & G_{30}+G_{31}+G_{32} \end{pmatrix}.$$

Accordingly, the coupling capacitances and conductances in Fig. 3.1(b) are the same as the corresponding off-diagonal entries of the *Q3D Extractor* matrices, but the negative signs are ignored. The grounded capacitances C_{i0} and conductances G_{i0} in Fig. 3.1(b) are the sums of the accordant column entries of the MAXWELL matrices:

$$C_{i0} = \sum_{j=1}^{n} C_{ij}^{M} \text{ and} \tag{3.3}$$

$$G_{i0} = \sum_{j=1}^{n} G_{ij}^{M}. \tag{3.4}$$

[4] The term refers to the tangent of the angle δ in a impedance plane between the resistive (lossy) component and the reactive (lossless) component. For details, see e.g. [Kories 08].

[5] Parameter extraction details are given in the *Q3D Extractor* help menu entries 'Capacitance and Conduction Solution', 'DC Resistance and Inductance Solution' and 'AC Resistance and Inductance Solution'.

[6] See e.g. [Kost 94] for details on FEM and BEM; and e.g. [Greengard 88], [Nabors 91], [Nabors 92] and [Kamon 94] for details on FMM.

[7] BEM uses a GREEN's function to model the electrostatic potential $\phi(r)$ due to a charge at the distance r. Accordingly, as r goes to infinity, the potential goes to zero. For details see e.g. [Nabors 91].

The RL sub-circuits are represented by the *Q3D Extractor* resistance inductance matrix. The total RL matrix is divided by two. One half is put on each side of the CG sub-circuit.

The accuracy of the simulation results depends on the mesh. The finer the mesh the more accurate are the simulation results. The presented simulation results are based on an adaptive analysis. According to the help menu entry 'The Adaptive Analysis Process', *Q3D Extractor* generates an initial mesh first. With this initial mesh *Q3D Extractor* computes the electromagnetic field that exists inside the structure when the structure is excited with the regarded frequency. Based on the current finite element solution, the regions with the highest errors are estimated and the tetrahedra in these regions are refined (see [Sun 00] for details). Afterwards, *Q3D Extractor* generates another solution using the refined mesh and recomputes the error. The iterative process repeats until the convergence criteria are met or the stopping criterion - the maximum number of passes - is reached. In this work, the following settings are used for the parameter extraction:

- The ***percent error*** is set to 0.1 %. Accordingly, the convergence criteria are not met before the relative change between the previous and the current matrix is below 0.1 %.
- The ***percent refinement per pass*** is set to 15 %. Therewith, the actual current mesh has approximately 15 % more tetrahedra than the previous mesh.
- Five is used as ***minimum number of passes***.
- Two is used as ***minimum number of converged passes***.
- The ***maximum number of passes*** is set to 30.

Due to the chosen percent error, a further mesh refinement does not enhance the accuracy of the solution considerably. All presented simulations converged well before 30 passes. Therefore, it can be assumed that the accuracy of the results is very high.

3.2.2 Parameter Extraction of TO-220 Packages

Fig. 3.2 shows the models of the TO-220 packages of the MOSFET and the SCHOTTKY diode.[8] For the voltage corrections described in subsection **3.3.1** on page 82 et seq. and **3.3.2** on page 85 et seq., the pin length is reduced. The ends of the pins represent the positions of the voltage probes. Thus, the RL parameters of the package models represent the equivalent circuit elements between the contacting surfaces of the dies and the position of the voltage probes. The models include lead frame, solder layer, bond wires, mold compound and a homogeneous plate with silicon or silicon carbide properties. The device-specific metalization layers are not considered as a part of the package and are hence not modeled.

The sinks and sources of the models' interconnections are defined as follows:

- The cross-sections at the ends of the shorted drain, gate, source, cathode and anode pin are defined as ***sources***.

[8] The models of the TO-220 packages are provided by *Infineon Technologies*.

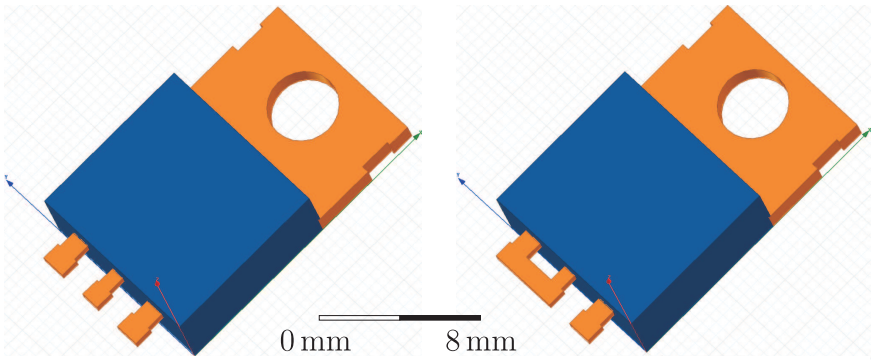


Figure 3.2: *Q3D Extractor* models of the TO-220 package of the SJ MOSFET (left) and the SiC SCHOTTKY diode (right)

- The contacting areas of the source, the gate and the anode bond wire on the top of the dies, as well as the solder layer faces, which are connected to the drain and the cathode side of the semiconductor chips, are defined as ***sinks***.

Q3D Extractor simulation results for the models in Fig. 3.2 are shown in Table 3.2 through Table 3.4, as well as in Fig. 3.3 and Fig. 3.4. The models assume frequency independent capacitances and ideal isolation materials. Thus, the conductances are zero.

If objects without a large metal enclosure are modeled, the connection to infinity ground is usually not necessary.[9] During the static and dynamic measurements the MOSFET and the SCHOTTKY diode are not within a metal enclosure. Therefore, the 'floating at infinity' operation is carried out for the packages (for details see [Bracken 99]). The 'floating at infinity' capacitance values are shown in Table 3.5. The circuit model with the remaining capacitances and the frequency dependent resistances and inductances is shown in Fig. 3.5.

If the DUTs are mounted to heat sink(s) during static or dynamic measurements, the consideration of heat sink(s) could be of interest. The impact of coupling capacitances to heat sink(s) is disregarded in this work.

[9] This information is obtained from personal correspondence with *J. E. Bracken* from *ANSYS*.

Table 3.2: Extracted DC RL matrix of the MOSFET's TO-220 package*

	Drain		Gate		Source	
	R [mΩ]	L [nH]	R [mΩ]	L [nH]	R [mΩ]	L [nH]
Drain	0.18	2.96	0.00	1.21	0.00	1.26
Gate	0.00	1.21	27.57	5.99	0.00	0.90
Source	0.00	1.26	0.00	0.90	0.81	4.79

* The designation of the matrix entries corresponds to the accordant die contact.

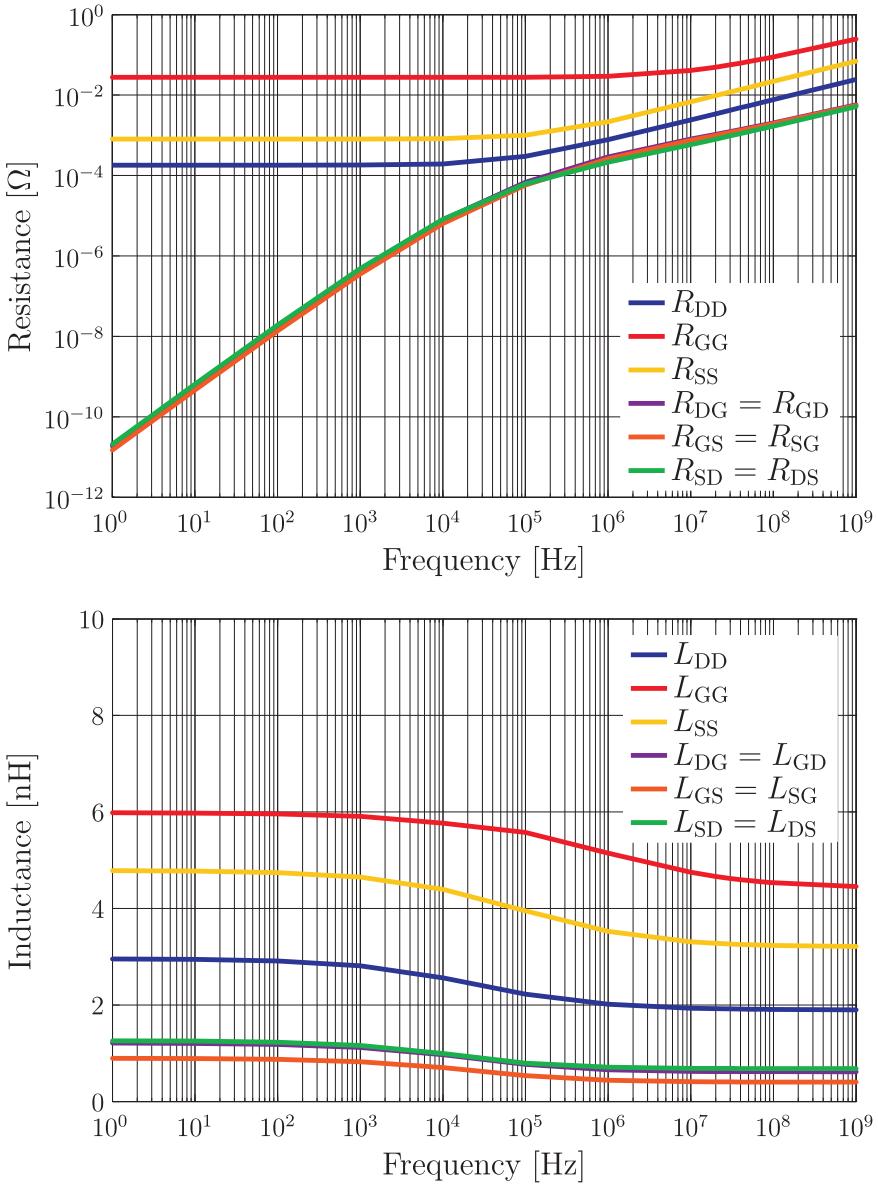


Figure 3.3: Extracted AC RL matrix elements of the SJ MOSFET's TO-220 package - The index 'D' represents the drain related net, the index 'G' represents the gate related net, and the index 'S' represents the source related net.

Table 3.3: Extracted CG matrix of the MOSFET's TO-220 package*

	Drain		Gate		Source	
	C [pF]	G [mS]	C [pF]	G [mS]	C [pF]	G [mS]
Drain	2.54	0.00	−0.65	0.00	−1.40	0.00
Gate	−0.65	0.00	0.75	0.00	−0.03	0.00
Source	−1.40	0.00	−0.03	0.00	1.50	0.00

* The designation of the matrix entries corresponds to the accordant die contact.

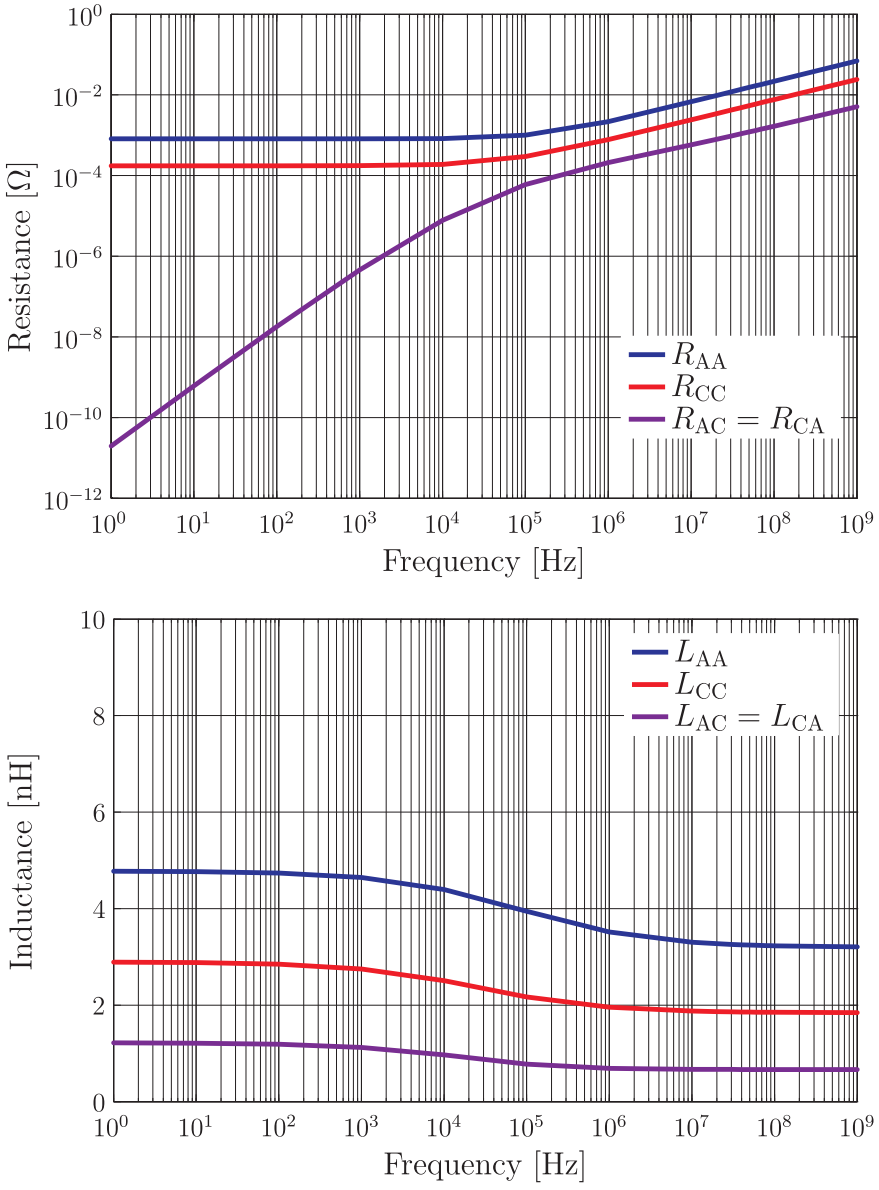


Figure 3.4: Extracted AC RL matrix elements of the SCHOTTKY diode's TO-220 package - The index 'C' represents the cathode related net, and the index 'A' represents the anode related net.

Table 3.4: Extracted DC RL and CG matrix of the diode's TO-220 package*

	Cathode				Anode			
	R [mΩ]	L [nH]	C [pF]	G [mS]	R [mΩ]	L [nH]	C [pF]	G [mS]
Cathode	0.81	4.78	1.42	0.00	0.00	1.22	−1.35	0.00
Anode	0.00	1.22	−1.35	0.00	0.17	2.90	1.90	0.00

* The designation of the matrix entries corresponds to the accordant die contact.

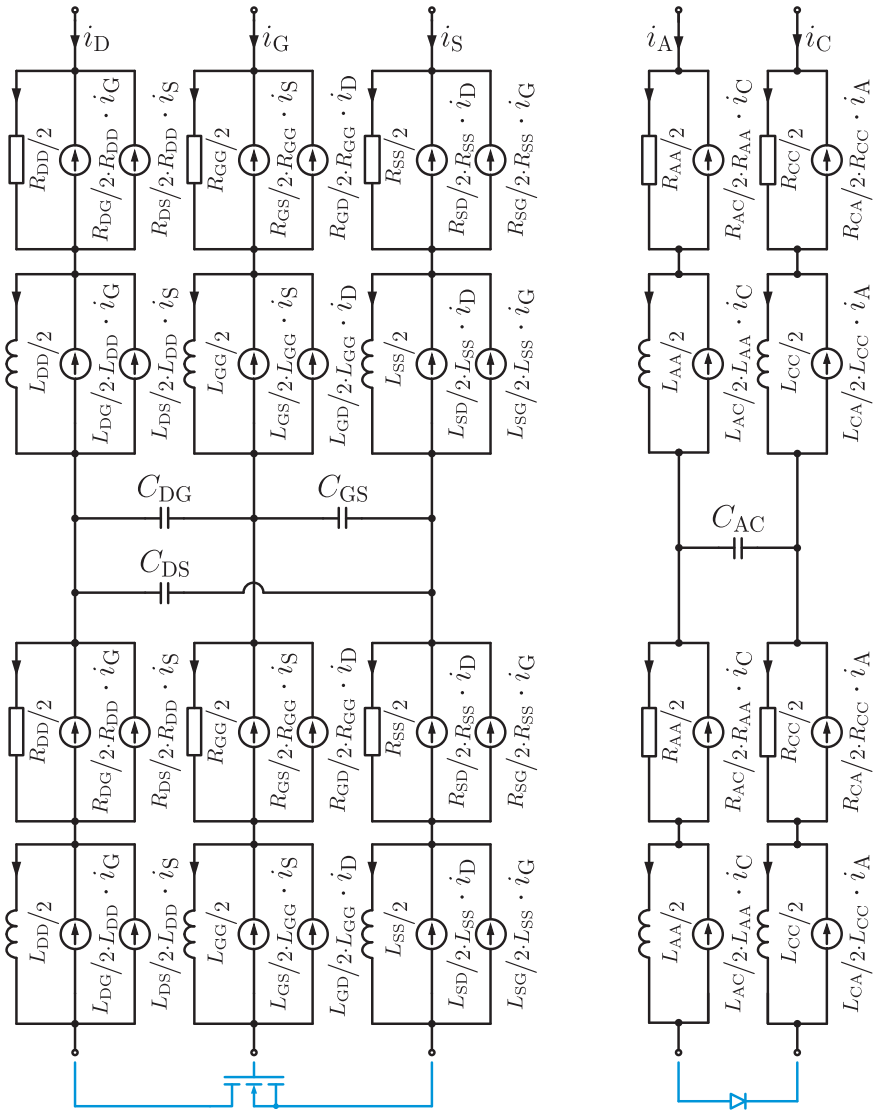


Figure 3.5: Equivalent circuit models of the TO-220 package of the SJ MOSFET (left) and the SiC SCHOTTKY diode (right) - The blue symbols represent the connecting points of the device models in Fig. 2.7 on page 19 and Fig. 2.11 on page 25.

Table 3.5: 'Floating at infinity' capacitance values of the TO-220 packages*

	Drain C [pF]	**Gate** C [pF]	**Source** C [pF]		**Cathode** C [pF]	**Anode** C [pF]
Drain	2.16	−0.71	−1.46	**Cathode**	1.41	−1.41
Gate	−0.71	0.75	−0.04	**Anode**	−1.41	1.41
Source	−1.46	−0.04	1.50			

* The designation of the matrix entries corresponds to the accordant die contact.

3.2.3 Parameter Extraction of a PCB with TO-220 Packages

Fig. 3.6(a) shows the *Q3D Extractor* model of the dynamic measurement setup.[10] The considered PCB detail is modeled with its four 0.2 mm thick copper traces, its three 0.5 mm thick FR-4 isolation layers in between and its vertical interconnect accesses (vias). The TO-220 packages are modeled with their actual pin length. Between the packages and the PCB 0.5 mm thick solder layers are designed and the via holes beneath the combining solder layers are filled with solder. The model considers the current path for the drain current measurement with the PEARSON probe, as well as the connections of the load and the gate driver circuit. The load and the gate driver circuit are not considered.[11] The placement vias of the DC link capacitor closest to the semiconductor devices are included in the model. The placement area of the other DC link capacitors is disregarded.[12] According to the explanations in [Paul 09], the current path with the lowest loop resistance and the current path with the lowest loop inductance should be represented by the model.

As indicated in Fig. 3.6(b), the sinks and sources of the model are defined as follows:

- The cross-section at the end of the gate pin, the placement vias of the DC link capacitor, the face of the solder layer connected to the cathode side of the SiC chip, and the cross-sections at the end of the load and the source connector are defined as ***sources***.

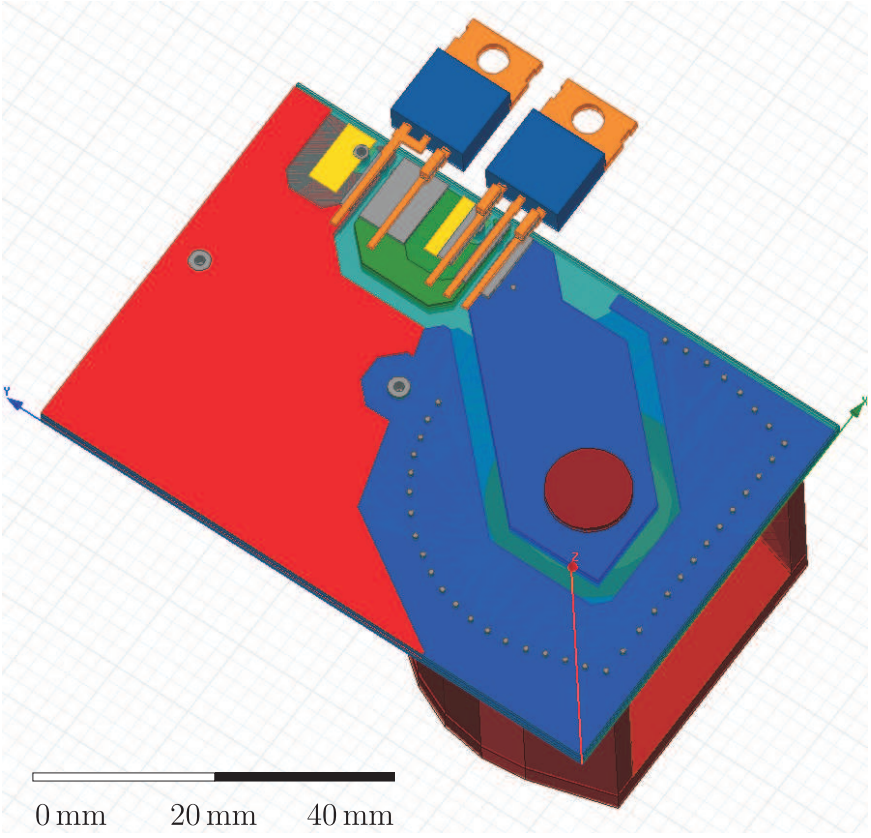
- The contacting areas of the source, the gate bond and the anode bond wire at the top of the dies, as well as the face of the solder layer, which is connected to the drain side of the silicon chip, are defined as ***sinks***.

Therewith, two multiple source connectors are defined in the *Q3D Extractor* model. Details on the equivalent circuit model of multiple source connectors are given in [Bracken 05].

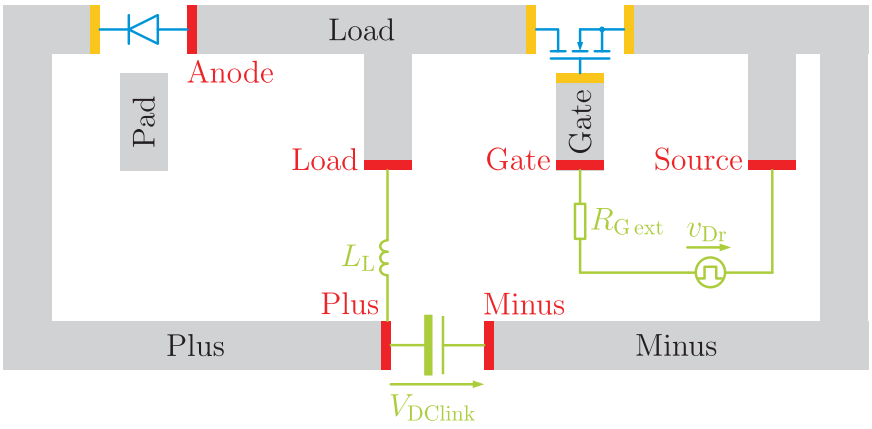
[10] The model is built on the models in [Hiller 09].

[11] The load circuit has probably little impact on the stability. Future works could verify this assumption. The parameter variation in subsection **5.2.4** on page 119 et seq. shows a significant impact of the equivalent circuit elements in the gate driver circuit on the stability. The neglect of significant parts of the input circuit results in reduced values of the equivalent circuit elements.

[12] The impact of the design of DC voltage link on the stability is not regarded in this work. For reasonable designs, the DC voltage link has probably little impact. Future works could verify this assumption.



(a) *Q3D Extractor* model



(b) Designation of the model's interconnect structures - The interconnect structures are represented by gray bars with yellow sinks and red sources. The blue and green symbols represent the connection points of the models in Fig. 2.7 on page 19, Fig. 2.11 on page 25 and simplified parts of the buck converter respectively.

Figure 3.6: Modeled buck converter topology's PCB detail with device packages

The *Q3D Extractor* simulation results are shown in Table 3.6 through Table 3.8, as well as in Fig. 3.7. The model assumes frequency independent capacitances and ideal isolation materials. The not shown conductance matrix elements are zero.

Table 3.6: Extracted DC R matrix of the buck converter model (R in [mΩ])*

	Plus	**Load**	**Anode**	**Gate**	**Source**	**Minus**
Plus	0.58	0.00	0.00	0.00	0.00	0.00
Load	0.00	0.57	0.54	0.00	0.00	0.00
Anode	0.00	0.54	1.37	0.00	0.00	0.00
Gate	0.00	0.00	0.00	27.86	0.00	0.00
Source	0.00	0.00	0.00	0.00	0.85	0.82
Minus	0.00	0.00	0.00	0.00	0.82	1.22

* For designation of the matrix entries, the red labels of the sources in Fig. 3.6(b) are used.

Table 3.7: Extracted DC L matrix of the buck converter model (L in [nH])*

	Plus	**Load**	**Anode**	**Gate**	**Source**	**Minus**
Plus	18.81	0.80	−2.12	1.64	1.13	3.00
Load	0.80	12.18	11.78	2.30	2.23	3.84
Anode	−2.12	11.78	17.78	1.29	1.60	2.31
Gate	1.64	2.30	1.29	7.56	1.52	2.59
Source	1.13	2.23	1.60	1.52	6.40	7.75
Minus	3.00	3.84	2.31	2.59	7.75	37.95

* For designation of the matrix entries, the red labels of the sources in Fig. 3.6(b) are used.

Table 3.8: Extracted C matrix of the buck converter model (C in [pF])*

	Plus	**Pad**	**Load**	**Gate**	**Minus**
Plus	292.72	−3.33	−2.48	−0.05	−286.91
Pad	−3.33	3.42	−0.03	−0.00	−0.04
Load	−2.48	−0.03	10.75	−5.49	−2.58
Gate	−0.05	−0.00	−5.49	5.68	−0.11
Minus	−286.91	−0.04	−2.58	−0.11	292.67

* For designation of the matrix entries, the black labels of the nets in Fig. 3.6(b) are used.

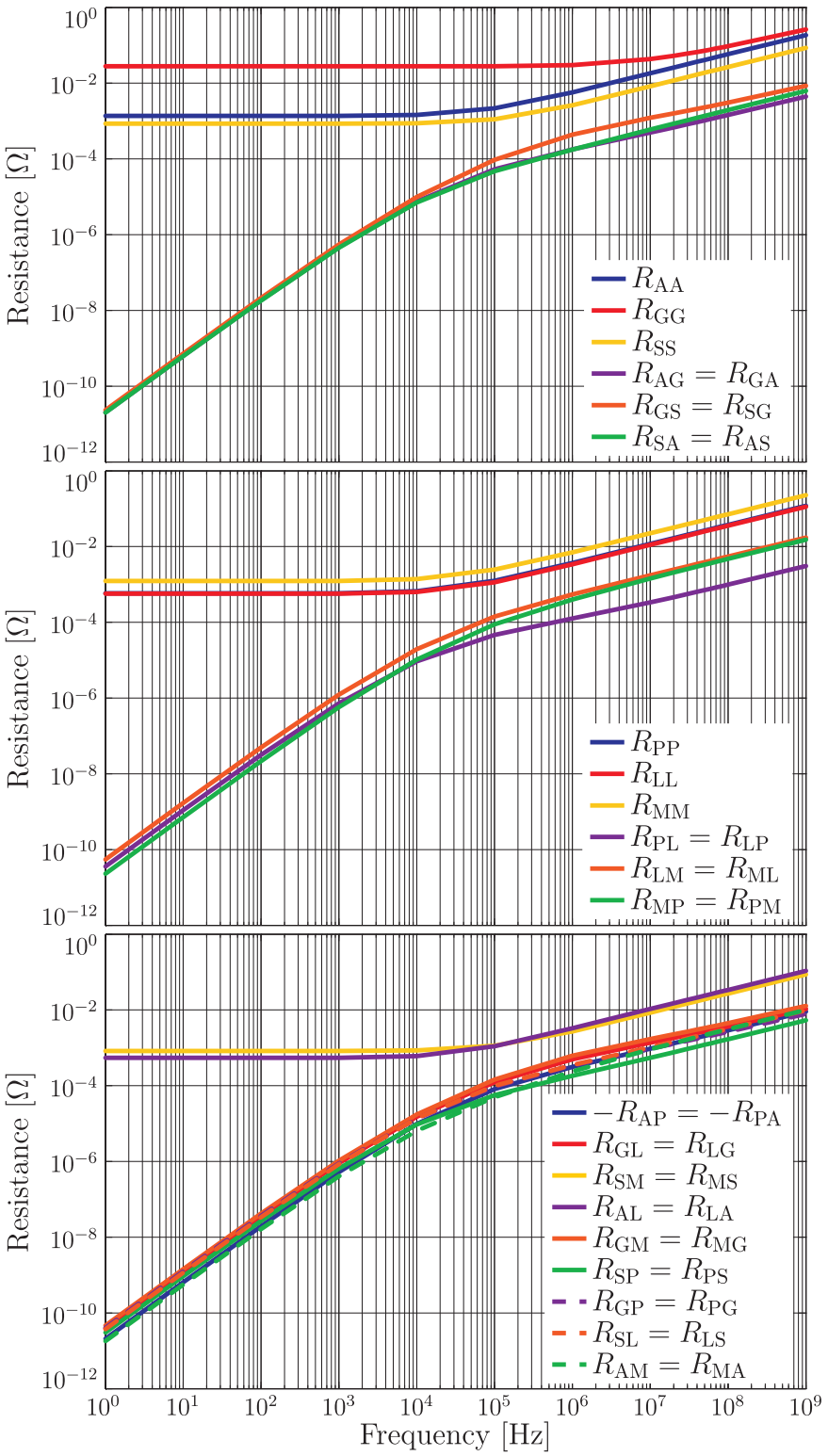


Figure 3.7: Extracted AC RL matrix elements of the buck converter topology - The index 'P' corresponds to the source 'Plus', 'G' to the source 'Gate', 'A' to the source 'Anode', 'L' to the source 'Load', 'S' to the source 'Source' and 'M' to the source 'Minus' in Fig. 3.6(b) on page 76.

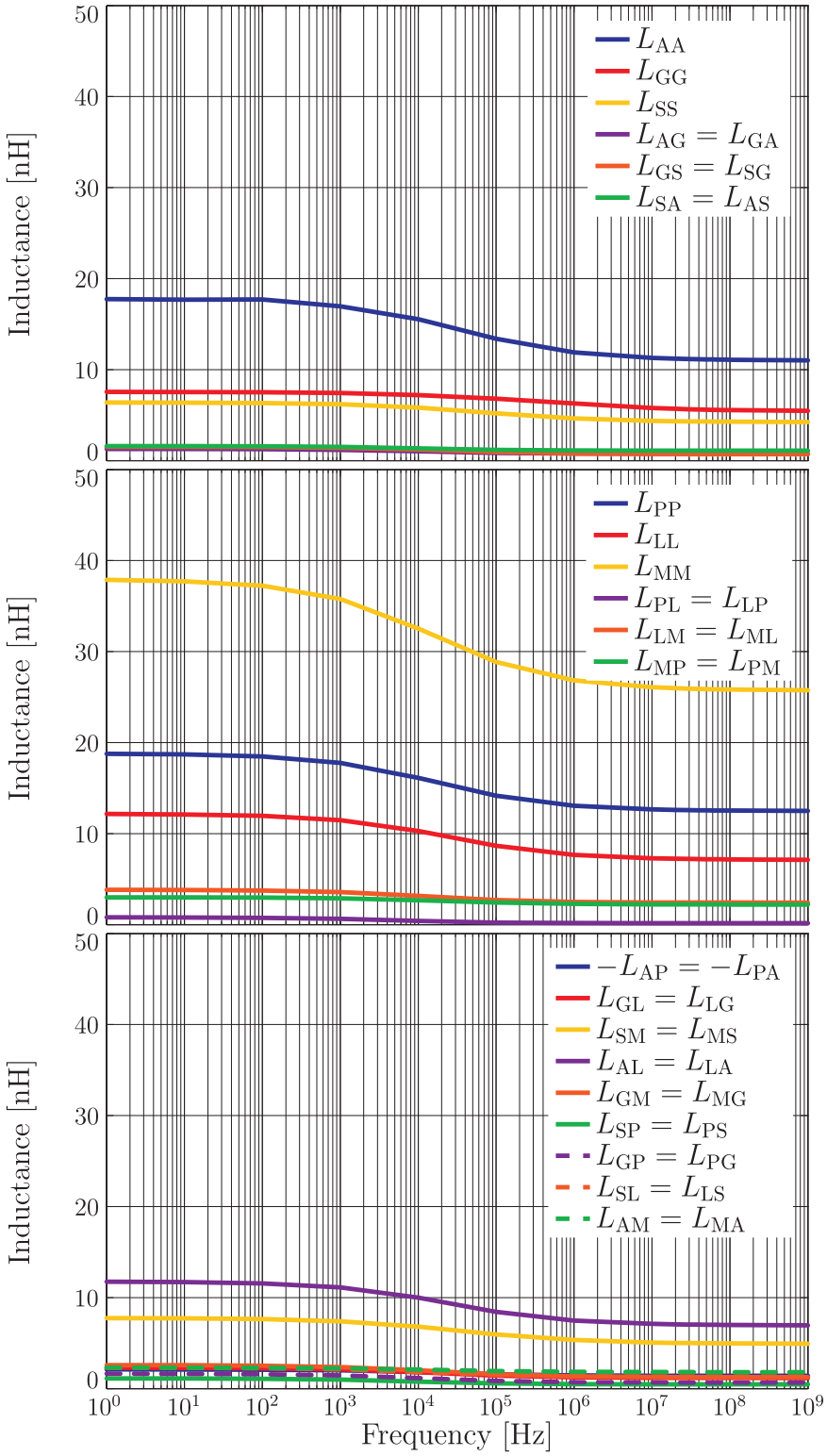


Figure 3.7: Extracted AC RL matrix elements of the buck converter topology (cont.) - The index 'P' corresponds to the source 'Plus', 'G' to the source 'Gate', 'A' to the source 'Anode', 'L' to the source 'Load', 'S' to the source 'Source' and 'M' to the source 'Minus' in Fig. 3.6(b) on page 76.

Since the net 'Pad' is not used in the buck converter, it has no sinks and sources.[13] Accordingly, the net 'Pad' has no entry in the RL matrices. For the determination of the CG matrix, sinks and sources are not necessary. The post-processing operating 'floating a connector', which is described in [Bracken 99], results in a reduced capacitance matrix. The reduced matrix for the floating 'Pad' is presented in Table 3.9. The 'floating pad' matrix is further reduced by the 'floating at infinity' operation. The result is shown in Table 3.10. The circuit model with the remaining capacitances and the frequency dependent inductances and resistances is shown in Fig. 3.8.

If the devices are mounted to heat sink(s) during switching operation, the consideration of the heat sink(s) in the *Q3D Extractor* model and the equivalent circuit model might be necessary. The impact of coupling capacitances to heat sink(s) is disregarded in this work.

Table 3.9: 'Floating pad' C matrix of the buck converter model (C in [pF])*

	Plus	**Load**	**Gate**	**Minus**
Plus	289.47	−2.51	−0.06	−286.95
Load	−2.51	10.75	−5.49	−2.58
Gate	−0.06	−5.49	5.68	−0.11
Minus	−286.95	−2.58	−0.11	292.67

* For designation of the matrix entries, the black labels of the nets in Fig. 3.6(b) are used.

Table 3.10: 'Floating at infinity' C matrix of the buck converter model (C in [pF])*

	Plus	**Load**	**Gate**	**Minus**
Plus	289.47	−2.51	−0.06	−286.91
Load	−2.51	10.74	−5.49	−2.74
Gate	−0.06	−5.49	5.68	−0.14
Minus	−286.91	−2.74	−0.14	289.78

* For designation of the matrix entries, the black labels of the nets in Fig. 3.6(b) are used.

[13] If the sinks and sources would have been defined, the application of the operation 'floating a connector' on the net 'Pad' would have resulted in RL matrices that would be identical to the results presented in Table 3.6, Table 3.7 and Fig. 3.7 on page 77 et seq. See [Bracken 99] for details.

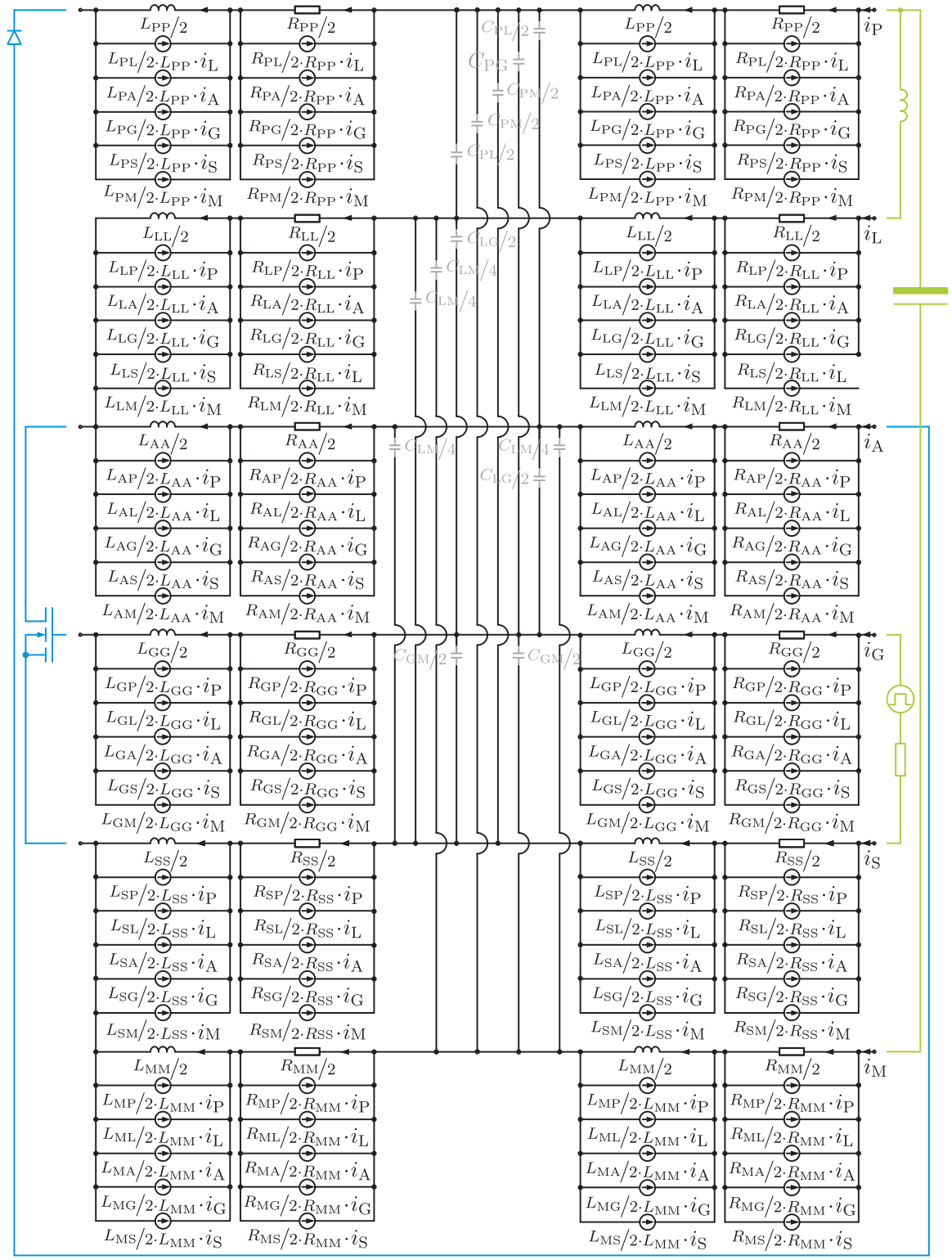


Figure 3.8: Equivalent circuit model of the measurement setup - The blue device symbols in Fig. 3.5 represent the connecting points of the semiconductor models in Fig. 2.7 on page 19 and Fig. 2.11 on page 25. The green circuit elements represent the connection points of the simplified parts of the buck converter.

3.3 Application Dependent Model Simplifications and Parameterizations

This section addresses the application of the extracted circuit elements for the calculation of chip voltages from measured DC voltages (as mentioned in **2.3.1.4** on page 37 et seq.), for the calculation of chip voltages from measured time-varying voltages (as mentioned in **2.4.1.4** on page 60 et seq.), and for the simulation and analysis of switching operations in section **4.1** on page 95 et seq. and section **5.4** on page 156 et seq..

3.3.1 Calculation of Chip Voltages from Measured DC Voltages

Fig. 3.5 on page 74 shows the equivalent circuits between the voltage measuring points and the semiconductor chips with their frequency dependent self and mutual resistances and inductances. An accurate parameterization of these circuit elements enables the calculation of the chip voltages. Constant voltages and currents can be assumed in the metering intervals of the measurements for the static characterization of the DUT. Therewith, self and mutual inductances have no impact on the measured DC voltages. Accordingly, the self inductances in Fig. 3.5 are represented by short circuits, and the parallel connected current sources are represented by open circuits. For a constant voltage, the capacitive reactance is infinite (see e.g. [Kories 08]). Hence, the coupling capacitances in Fig. 3.5 can be regarded as open circuits. Constant voltages imply a nonexistent gate current and thus, identical drain and source currents, as well as the insignificance of the gate resistances. The remaining circuit elements are shown in Fig. 3.9. The resistances in Fig. 3.9 are frequency dependent and the applied pulse width for the static characterization has an impact on the resistive voltage drop between the voltage measuring points and the connecting points of the semiconductor chip. This is exemplified in Fig. 3.10 for the voltage drop, which corresponds to the self resistance $R_{\mathrm{SS}}(f)$ of the MOSFET's package. Simplifying, two periodic rectangular source current signals $i_{\mathrm{S}}(t)$ with a duty cycle of 50 % with different pulse widths t_{pu} are assumed and represented by the first fifteen elements of their FOURIER series. For the regarded elements of the FOURIER series, the corresponding resistive voltage drops are calculated and then superposed.[14] The resulting voltage is $v_{R_{\mathrm{SS}}(f)}$. Additionally, the voltage drop is calculated for two constant resistances - the DC resistance $R_{\mathrm{SS\,DC}}$ and the resistance $R_{\mathrm{SS}}(f_0)$, which corresponds to the fundamental frequency f_0 of the source current signal i_{S}.[15]

The pulse width of 250 μs in Fig. 3.10(a) represents the pulse width of the curve tracer (see e.g. Fig. 2.12 on page 28 and Fig. 2.23 on page 46). Fig. 3.10(a) shows the voltage $v_{R_{\mathrm{SS}}(f)}$ can be approximated with $v_{R_{\mathrm{SS\,DC}}}$ and $v_{R_{\mathrm{SS}}(f_0)}$. For the curve tracer measurements,

[14] The *Q3D Extractor*'s resistance calculation is based on a loss calculation. The calculation of losses in conductors with periodic non sinusoidal current waveforms with the aid of the FOURIER series analysis is shown in [Venkatramen 84] and [Carsten 86]. The Fourier analysis can be used due to the fact that the losses at different frequencies are orthogonal, which means that the losses, which are caused by a sinusoidal current with a certain frequency, have no impact on the losses that are caused by a sinusoidal current with another frequency (see e.g. [Morrison 06]).

[15] The fundamental frequencies f_0 of the periodic signals $i_{\mathrm{S}}(t)$ are given by $f_0 = 1/2 \cdot t_{\mathrm{pu}}$.

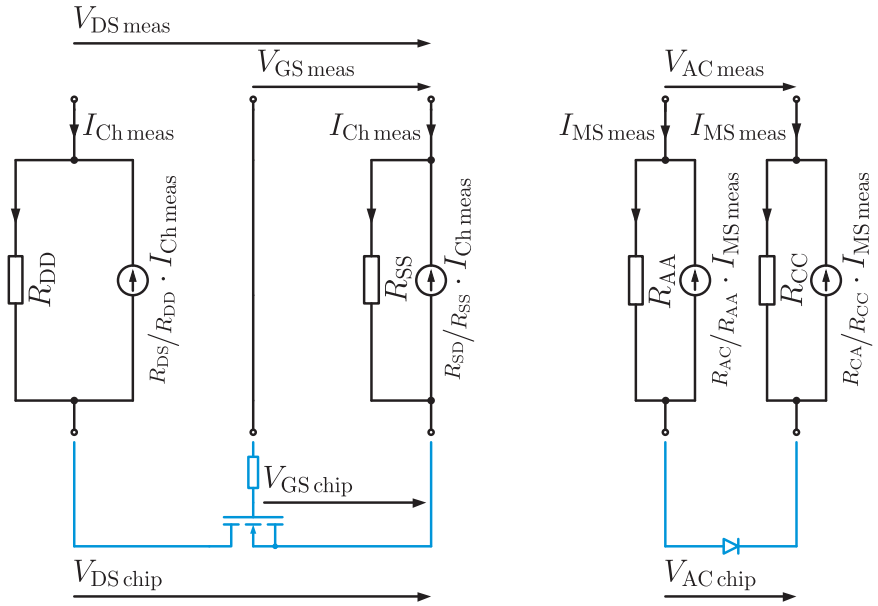


Figure 3.9: Equivalent circuit models of the MOSFET's and the diode's TO-220 package for the calculation of chip voltages from measured DC voltages - The blue device symbols represent the connecting points of the models in Fig. 2.7 on page 19 and Fig. 2.11 on page 25. For the accurate representation of $V_{\mathrm{GS\,chip}}$, $R_{\mathrm{G\,int}}$ is depicted separately.

the DC resistances are a very good approximation in the middle of the current pulse - where the static voltages and currents are determined. Accordingly, the voltage correction of the operating points of the MOSFET $I_{\mathrm{Ch\,meas}}(V_{\mathrm{DS\,meas}}, V_{\mathrm{GS\,meas}})$ and the SCHOTTKY diode $I_{\mathrm{Dio\,meas}}(V_{\mathrm{AC\,meas}})$ can be estimated with

$$V_{\mathrm{DS\,chip}} \approx V_{\mathrm{DS\,meas}} - (R_{\mathrm{DD\,DC}} + R_{\mathrm{SS\,DC}}) \cdot I_{\mathrm{Ch\,meas}}, \tag{3.5}$$

$$V_{\mathrm{GS\,chip}} \approx V_{\mathrm{GS\,meas}} - R_{\mathrm{SS\,DC}} \cdot I_{\mathrm{Ch\,meas}} \text{ and} \tag{3.6}$$

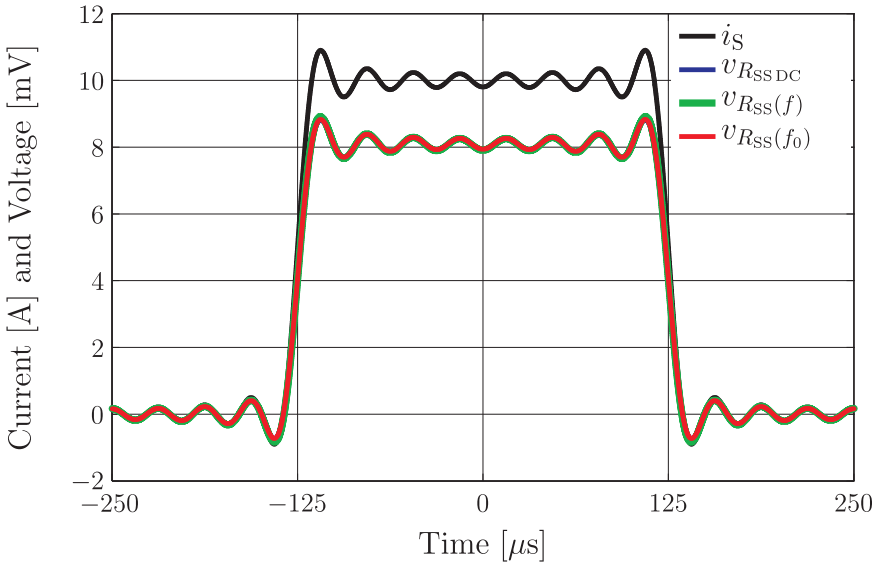
$$V_{\mathrm{AC\,chip}} \approx V_{\mathrm{AC\,meas}} - (R_{\mathrm{AA\,DC}} + R_{\mathrm{CC\,DC}}) \cdot I_{\mathrm{Dio\,meas}} \tag{3.7}$$

with the DC self resistances $R_{\mathrm{DD\,DC}}$ and $R_{\mathrm{SS\,DC}}$ of the MOSFET's package in Table 3.2 on page 72, and $R_{\mathrm{AA\,DC}}$ and $R_{\mathrm{CC\,DC}}$ of the diode's package in Table 3.4 on page 74. For the measurement of high voltage transfer characteristics, pulse widths in a range of 10 μs are used (see e.g. Fig. 2.18 on page 36). Fig. 3.10(b) shows that the actual voltage drop $v_{R_{\mathrm{SS}}(f)}$ in the middle part of a 10 μs pulse is between the approximations with the DC resistance $R_{\mathrm{SS\,DC}}$ and the resistance of current signal's first harmonic $R_{\mathrm{SS}}(f_0)$. Accordingly, for the operating points of the measured high voltage transfer characteristics, (3.5) and (3.6) calculate the upper limits of $V_{\mathrm{DS\,chip}}$ and $V_{\mathrm{GS\,chip}}$. The lower limit is given by

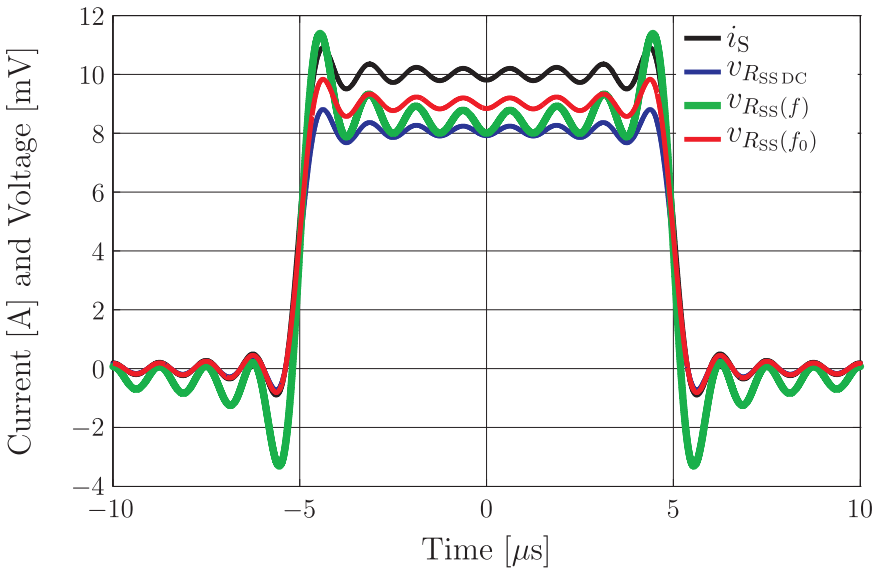
$$V_{\mathrm{DS\,chip}} \approx V_{\mathrm{DS\,meas}} - (R_{\mathrm{DD}}(f_0) + R_{\mathrm{SS}}(f_0) - 2 \cdot R_{\mathrm{DS}}(f_0)) \cdot I_{\mathrm{Ch\,meas}} \text{ and} \tag{3.8}$$

$$V_{\mathrm{GS\,chip}} \approx V_{\mathrm{GS\,meas}} - (R_{\mathrm{SS}}(f_0) - R_{\mathrm{DS}}(f_0)) \cdot I_{\mathrm{Ch\,meas}} \tag{3.9}$$

with the current signal's fundamental frequency f_0 and the resistances $R_{\mathrm{DD}}(f_0)$, $R_{\mathrm{SS}}(f_0)$ and



(a) Voltage $v_{R_{SS}(f)}$ across the source connector caused by the connector's self resistance $R_{SS}(f)$ and different voltage approximations in case the DUT is operated approximately ***250*** μs in an operating point with a channel current of 10 A



(b) Voltage $v_{R_{SS}(f)}$ across the source connector caused by the connector's self resistance $R_{SS}(f)$ and different voltage approximations in case the DUT is operated approximately ***10*** μs in an operating point with a channel current of 10 A

Figure 3.10: Impact of the source current pulse width on the voltage across the self resistance of the source connector of modeled MOSFET package in Fig. 3.2 - Two periodic rectangular source current signals are assumed and represented by the first fifteen elements of their Fourier series.

$R_{\mathrm{DS}}(f_0)$ of the MOSFET's package model in Fig. 3.3 on page 72 (cp. [Bracken 00]). Mutual resistances that are not located between the voltage measuring points and the contacts of the semiconductor chip are disregarded in the lower limit calculation.

With respect to Fig. 3.10(a) and according to the DC resistances in Table 3.4 on page 74, the difference between $V_{\mathrm{AC\,meas}}(I_{\mathrm{Dio\,meas}})$ and $V_{\mathrm{AC\,chip}}(I_{\mathrm{Dio\,meas}})$ is below 20 mV in the regarded forward region. In the blocking region, the difference between $V_{\mathrm{AC\,meas}}(I_{\mathrm{Dio\,meas}})$ and $V_{\mathrm{AC\,chip}}(I_{\mathrm{Dio\,meas}})$ is negligible. With respect to Fig. 3.10, and according to the DC resistance values in Table 3.2 on page 72 and the 50 kHz resistance values in Fig. 3.3 on page 72, the difference between $V_{\mathrm{DS\,meas}}$ and $V_{\mathrm{DS\,chip}}$ is below 20 mV in the regarded operating range. Therewith, the error in the drain source voltage measurement is very small and the drain source voltage correction could be omitted for the considered placement of the drain source voltage probe and the regarded package. However, beyond the linear region of the output characteristics a difference between $V_{\mathrm{GS\,meas}}$ and $V_{\mathrm{GS\,chip}}$ of up to 20 mV is not negligible due to the high transconductance of the DUT. Hence, a DC voltage correction is recommended for an accurate static characterization.

3.3.2 Calculation of Chip Voltages from Measured Dynamic Voltages

Fig. 3.5 on page 74 shows the equivalent circuit between the voltage measuring points and the MOSFET with its frequency dependent resistances and inductances. For the transient voltage correction, the parasitic capacitances in Fig. 3.5 are neglected. The resulting circuit model is shown in Fig. 3.11. An appropriate parameterization of the model enables the determination of the chip voltages of the power MOSFET. For the determination of an appropriate parameterization, sampled current characteristics of switching operations are analyzed. Thereto, each regarded current characteristic is mirrored along the abscissa. The resulting characteristic represents the period $\mathcal{T}$ of the current $i_{\mathrm{j}}(t)$ through the connector j. The periodic current $i_{\mathrm{j}}(t)$ can be transformed into the discrete Fourier series

$$i_{\mathrm{j}}(t) = \sum_{k\in\mathbb{Z}} c_k \cdot \mathrm{e}^{\mathrm{i}\cdot\omega_k\cdot t} \text{ with } \omega_k = 2\cdot\pi\cdot f_0\cdot k \text{ and } f_0 = {}^1\!/\!_{\mathcal{T}} \tag{3.10}$$

[Bronstein 08]. The complex Fourier coefficients c_k are given by

$$c_k = \frac{1}{\mathcal{T}} \cdot \int_0^{\mathcal{T}} i_{\mathrm{j}}(t) \cdot \mathrm{e}^{-\mathrm{i}\cdot\omega_k\cdot t}\mathrm{d}t \tag{3.11}$$

For the real signals, c_k and c_{-k} are conjugate-complex. Thus, (3.10) can be simplified to

$$i_{\mathrm{j}}(t) = c_0 + \sum_{k=1}^{\infty} 2\cdot\Re\left\{c_k\cdot\mathrm{e}^{\mathrm{i}\cdot\omega_k\cdot t}\right\} = c_0 + \sum_{k=1}^{\infty} 2\cdot|c_k|\cdot\cos\left(\omega_k\cdot t + \arctan\left(\frac{\Im\{c_k\}}{\Re\{c_k\}}\right)\right) \tag{3.12}$$

with the real part of the Fourier series elements $\Re\left\{c_k\cdot\mathrm{e}^{\mathrm{i}\cdot\omega_k\cdot t}\right\}$, as well as the real and imaginary part of the complex Fourier coefficients $\Re\{c_k\}$ and $\Im\{c_k\}$.

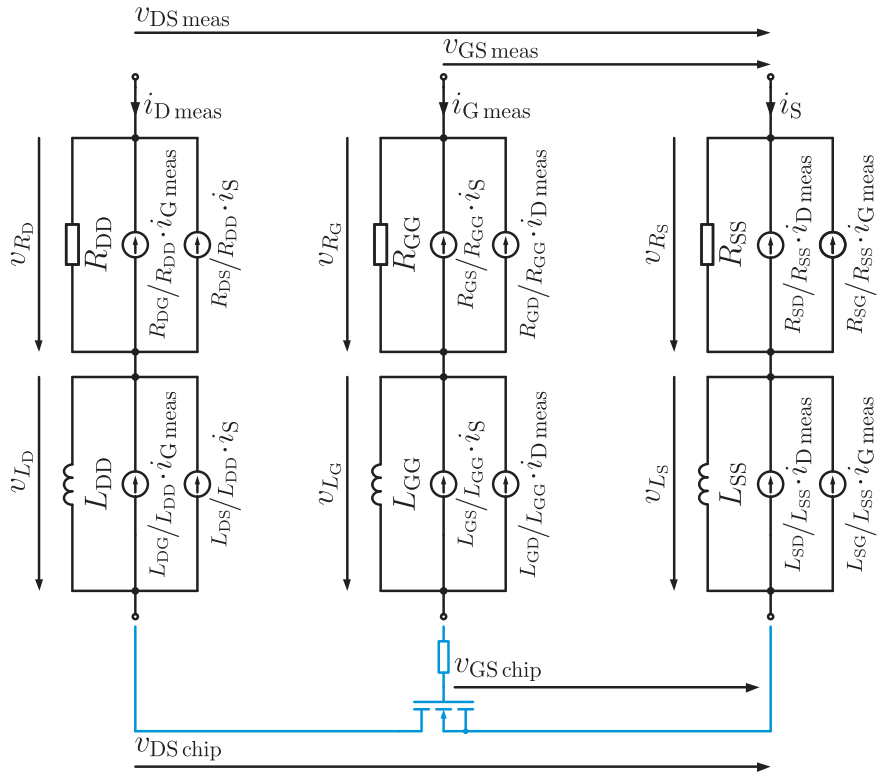


Figure 3.11: Equivalent circuit models of the MOSFET's TO-220 package for the calculation of chip voltages from measured transient voltages - The blue device symbols represent the connecting points of the MOSFET model in Fig. 2.7 on page 19. For the accurate illustration of $v_{\mathrm{GS\,chip}}$, the integrated gate resistance is depicted separately. All currents and voltages are time dependent, and all resistances and inductances are frequency dependent.

According to the NYQUIST-SHANNON sampling theorem, a signal that has been sampled can be reconstructed if the sampling rate f_s exceeds two times the highest frequency of the original signal [Shannon 98].[16] Accordingly, it is assumed that the current signal $i(t)$ is given by the finite FOURIER series

$$i_{\mathrm{j}}(t) = c_0 + \sum_{k=1}^{\lfloor f_s/2 \cdot f_0 \rfloor} 2 \cdot |c_k| \cdot \cos\left(\omega_k \cdot t + \arctan\left(\frac{\Im\{c_k\}}{\Re\{c_k\}}\right)\right). \tag{3.13}$$

According to the OHM's law, the voltage across the connector i caused by the current through the connector j and the frequency dependent resistance $R_{\mathrm{ij}}(f)$ can be calculated with

$$v_{R_{\mathrm{ij}}}(t) = c_0 \cdot R_{\mathrm{ij}}(0\,\mathrm{Hz}) + \sum_{k=1}^{\lfloor f_s/2 \cdot f_0 \rfloor} 2 \cdot |c_k \cdot R_{\mathrm{ij}}(f_k)| \cdot \cos\left(\omega_k \cdot t + \arctan\left(\frac{\Im\{c_k \cdot R_{\mathrm{ij}}(f_k)\}}{\Re\{c_k \cdot R_{\mathrm{ij}}(f_k)\}}\right)\right) \tag{3.14}$$

[16] The measurement data analyzed in this work is sampled with 2 GHz.

with $f_k = f_0 \cdot k$. The impedance of an inductance L is given by $Z = \mathrm{i} \cdot \omega \cdot L$. Hence, the voltage across the connector i caused by the altering current through the connector j and the frequency dependent inductance $L_{\mathrm{ij}}(f)$ is given by

$$v_{L_{\mathrm{ij}}}(t) = \sum_{k=1}^{\lfloor f_s/2 \cdot f_0 \rfloor} 2 \cdot |c_k \cdot \mathrm{i} \cdot \omega_k \cdot L_{\mathrm{ij}}(f_k)| \cdot \cos\left(\omega_k \cdot t + \arctan\left(\frac{\Im\{c_k \cdot \mathrm{i} \cdot \omega_k \cdot L_{\mathrm{ij}}(f_k)\}}{\Re\{c_k \cdot \mathrm{i} \cdot \omega_k \cdot L_{\mathrm{ij}}(f_k)\}}\right)\right). \quad (3.15)$$

In Fig. 3.12, results of such calculations are shown for sample turn-off source current characteristics with different gate resistances $R_{\mathrm{G\,ext}}$. The voltages $v_{R_{\mathrm{SS}}}$ and $v_{L_{\mathrm{SS}}}$ are depicted in green. The approximation of $v_{R_{\mathrm{SS}}}$ and $v_{L_{\mathrm{SS}}}$ with constant resistances and inductances is tested with the DC resistance $R_{\mathrm{SS\,DC}}$ and the DC inductance $L_{\mathrm{SS\,DC}}$, as well as the resistance $R_{\mathrm{SS}}(f_{\mathrm{equ}})$ and the inductance $L_{\mathrm{SS}}(f_{\mathrm{equ}})$ of the source current slope's equivalent frequency f_{equ}.[17] In Fig. 3.12, the resulting characteristics $v_{R_{\mathrm{SS\,DC}}}$ and $v_{L_{\mathrm{SS\,DC}}}$, as well as $v_{R_{\mathrm{SS}}(f_{\mathrm{equ}})}$ and $v_{L_{\mathrm{SS}}(f_{\mathrm{equ}})}$ are shown in blue and red respectively. The following conclusions can be drawn:

- Inductive voltage drops are represented by the inductances, which correlate to the current slope's equivalent frequency.[18] The usage of DC inductances results in a considerable overestimation of inductive voltages during commutation.
- For the estimation of resistive voltage drops, the frequency dependency of the resistances needs to be regarded. Frequency independent resistances are not suitable.

Therewith and with respect to Fig. 3.11, the transient voltage correction of the measured voltage characteristics of the MOSFET are approximately given by

$$\begin{aligned} v_{\mathrm{DS\,chip}}(t) \approx\ & v_{\mathrm{DS\,meas}}(t) - (L_{\mathrm{DD}}(f_{\mathrm{equ}}) + L_{\mathrm{SS}}(f_{\mathrm{equ}}) - 2 \cdot L_{\mathrm{DS}}(f_{\mathrm{equ}})) \cdot \frac{\mathrm{d}i_{\mathrm{D\,meas}}(t)}{\mathrm{d}t} \\ & - (L_{\mathrm{DG}}(f_{\mathrm{equ}}) + L_{\mathrm{SS}}(f_{\mathrm{equ}}) - L_{\mathrm{SG}}(f_{\mathrm{equ}}) - L_{\mathrm{DS}}(f_{\mathrm{equ}})) \cdot \frac{\mathrm{d}i_{\mathrm{G\,meas}}(t)}{\mathrm{d}t} \\ & - v_{R_{\mathrm{DD}}}(t) - v_{R_{\mathrm{DG}}}(t) - v_{R_{\mathrm{DS}}}(t) + v_{R_{\mathrm{SD}}}(t) + v_{R_{\mathrm{SG}}}(t) + v_{R_{\mathrm{SS}}}(t) \end{aligned} \quad (3.16)$$

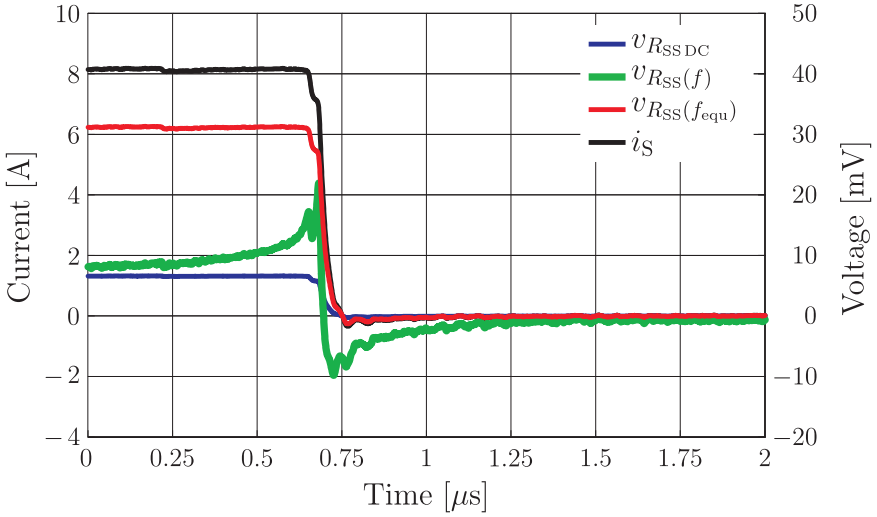
as well as

$$\begin{aligned} v_{\mathrm{GS\,chip}}(t) \approx\ & v_{\mathrm{GS\,meas}}(t) - (L_{\mathrm{GG}}(f_{\mathrm{equ}}) + L_{\mathrm{SS}}(f_{\mathrm{equ}}) - 2 \cdot L_{\mathrm{GS}}(f_{\mathrm{equ}})) \cdot \frac{\mathrm{d}i_{\mathrm{G\,meas}}(t)}{\mathrm{d}t} \\ & - (L_{\mathrm{GD}}(f_{\mathrm{equ}}) + L_{\mathrm{SS}}(f_{\mathrm{equ}}) - L_{\mathrm{SD}}(f_{\mathrm{equ}}) - L_{\mathrm{GS}}(f_{\mathrm{equ}})) \cdot \frac{\mathrm{d}i_{\mathrm{D\,meas}}(t)}{\mathrm{d}t} \\ & - R_{\mathrm{G\,int}} \cdot i_{\mathrm{G\,meas}}(t) - v_{R_{\mathrm{GD}}}(t) - v_{R_{\mathrm{GG}}}(t) - v_{R_{\mathrm{GS}}}(t) \\ & + v_{R_{\mathrm{SD}}}(t) + v_{R_{\mathrm{SG}}}(t) + v_{R_{\mathrm{SS}}}(t) \end{aligned} \quad (3.17)$$

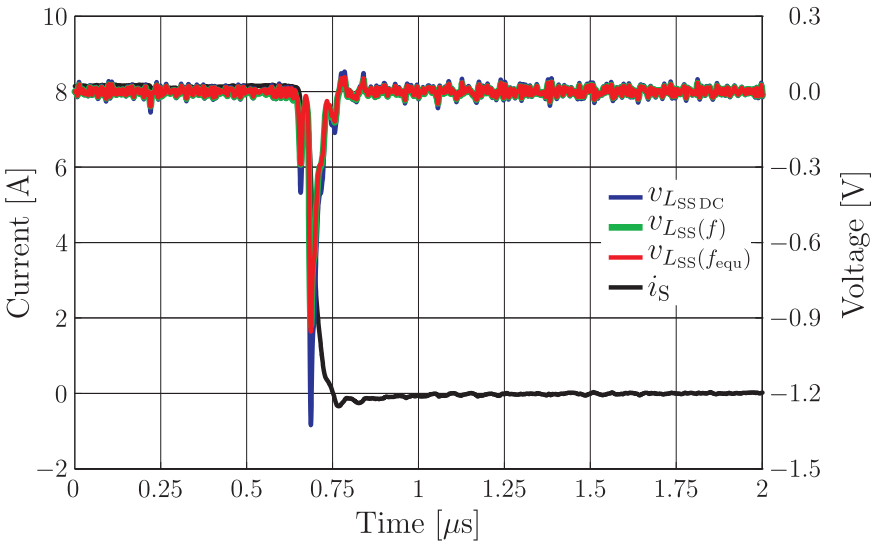
with $i_{\mathrm{S}}(t) = -i_{\mathrm{D\,meas}}(t) - i_{\mathrm{G\,meas}}(t)$, the current slopes' equivalent frequencies f_{equ}, the corresponding inductances in Fig. 3.3 on page 72. In Fig. 3.11, the resistive and inductive voltage drops of the connectors are represented by $v_{L_{\mathrm{G}}}$, $v_{R_{\mathrm{G}}}$, $v_{L_{\mathrm{D}}}$, $v_{R_{\mathrm{D}}}$, $v_{L_{\mathrm{S}}}$ and $v_{R_{\mathrm{S}}}$.

[17] The equivalent frequency of a slope is defined in (3.2) on page 66.

[18] The usage of the inductance of the current slope's equivalent frequency was also proposed in [Höch 09a] after the comparison of the drain source overvoltage and voltage reduction during current commutation of simulated and measured switching characteristics.

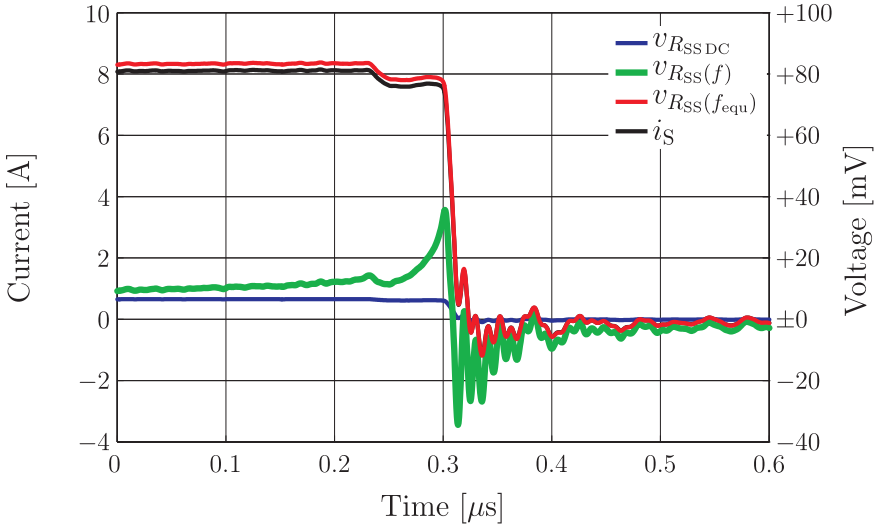


(a) Voltage $v_{R_{SS}(f)}$ across the source connector caused by the connector's self resistance $R_{SS}(f)$ and different voltage approximations during a turn-off of the DUT with $i_L = 8\,A$, $V_{DClink} = 400\,V$, $R_{G\,ext} = \mathbf{100}\,\Omega$ and $\vartheta_J = 25\,°C$

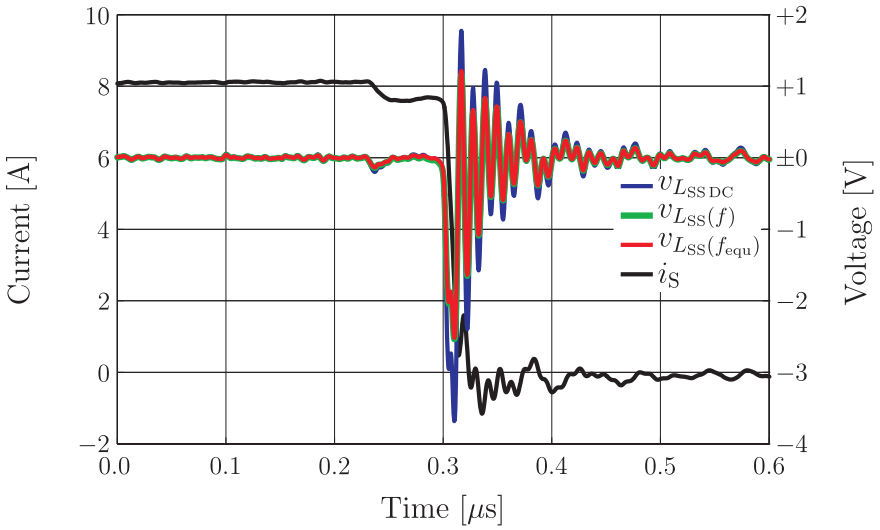


(b) Voltage $v_{L_{SS}(f)}$ across the source connector caused by the connector's self inductance $L_{SS}(f)$ and different voltage approximations during a turn-off of the DUT with $i_L = 8\,A$, $V_{DClink} = 400\,V$, $R_{G\,ext} = \mathbf{100}\,\Omega$ and $\vartheta_J = 25\,°C$

Figure 3.12: Voltages across the source connector during switching caused by the frequency dependent resistance $R_{SS}(f)$ and inductance $L_{SS}(f)$



(c) Voltage $v_{R_{SS}(f)}$ across the source connector caused by the connector's self resistance $R_{SS}(f)$ and different voltage approximations during a turn-off of the DUT with $i_L = 8\,A$, $V_{DClink} = 400\,V$, $R_{G\,ext} = \mathbf{10}\,\Omega$ and $\vartheta_J = 25\,°C$



(d) Voltage $v_{L_{SS}(f)}$ across the source connector caused by the connector's self inductance $L_{SS}(f)$ and different voltage approximations during a turn-off of the DUT with $i_L = 8\,A$, $V_{DClink} = 400\,V$, $R_{G\,ext} = \mathbf{10}\,\Omega$ and $\vartheta_J = 25\,°C$

Figure 3.12: Voltages across the source connector during switching caused by the frequency dependent resistance $R_{SS}(f)$ and inductance $L_{SS}(f)$ (cont.)

Mutual resistances and inductances that are not located between the voltage measuring points and the chip contacts are disregarded in the previous equations. Furthermore, displacement currents, which corresponds to the coupling capacitances in Fig. 3.8 on page 81, and thus, differences between the measured currents and the currents, which flow into the die, are not considered. The ratio of C_{MP} and chip capacitances, and the ratio of C_{GP} and the chip capacitances allow the conclusion that the corresponding differences are very small. Accordingly, the impact of these capacitances on the dynamic characterization results is negligible. The disregard of displacement currents charging the chip-external coupling capacitances C_{GM}, C_{LG}, C_{LM} and C_{PL} results in an increase of the calculated chip capacitances $C_{\mathrm{GS\,chip}}$, $C_{\mathrm{DG\,chip}}$ and $C_{\mathrm{DS\,chip}}$ in **2.4.1.2** on page 51 et seq. and in **2.4.1.3** on page 55 et seq.. With C_{GM}, C_{LG}, C_{LM} and C_{PL} in Table 3.10 on page 80 the upper limits, and with C_{DG}, C_{DS}, C_{GS} and C_{AC} in Table 3.5 on page 75 the lower limits of this increase are given.

With respect to Fig. 3.12, and according to the resistance and inductance values in Fig. 3.4 on page 73, it is concluded that the difference between the measured drain source voltage $v_{\mathrm{DS\,meas}}$ and the chip voltage $v_{\mathrm{DS\,chip}}$ is below 120 mV in the regarded operating range. The difference between the measured voltage $v_{\mathrm{GS\,meas}}$ and the chip voltage $v_{\mathrm{GS\,chip}}$ is up to 80 mV in the regarded operating range. For an accurate determination of the channel current i_{Ch}, the difference between the measured gate source voltages $v_{\mathrm{GS\,meas}}$ and the chip voltage $v_{\mathrm{GS\,chip}}$ must be considered because of the MOSFET's high transconductance. Therefore, a voltage correction of transient voltages is necessary for an accurate dynamic characterization.

3.3.3 Large-Signal Model for the Simulation of Switching Characteristics

Since simulation times correlate with the circuit complexity, an as complex model as necessary and an as simple model as possible is needed for the simulation of switching characteristics. In Fig. 3.13, the circuit model, which is proposed for the simulation of switching operations, is shown. The DC link circuit is modeled with an ideal voltage source, which supplies a constant voltage V_{DClink}. The load current branch consists of an ideal inductance L_{L}, and the integrated driver circuit is represented by an ideal voltage source, which provides a PT2 delayed square wave voltage signal v_{Dr}.[19]

Measurements have shown an impact of coupling capacitances between the MOSFET's contacts on the occurrence of parasitic oscillations in commutation cells (see e.g. [Kapels 09] or [Inf 07a]). Thus, the chip-external capacitances $C_{\mathrm{DS\,ext}}$, $C_{\mathrm{DG\,ext}}$ and $C_{\mathrm{GS\,ext}}$ are included in the buck converter model. Referring to Table 3.10 on page 80, they are parameterized with the maximum possible values between the nets 'Load', 'Gate' and 'Minus':

$$C_{\mathrm{DS\,ext}} := C_{\mathrm{LM}}, \tag{3.18}$$

$$C_{\mathrm{DG\,ext}} := C_{\mathrm{LG}} \text{ and} \tag{3.19}$$

$$C_{\mathrm{GS\,ext}} := C_{\mathrm{GM}}. \tag{3.20}$$

[19] For details on PT2 elements, see e.g. [Lutz 07].

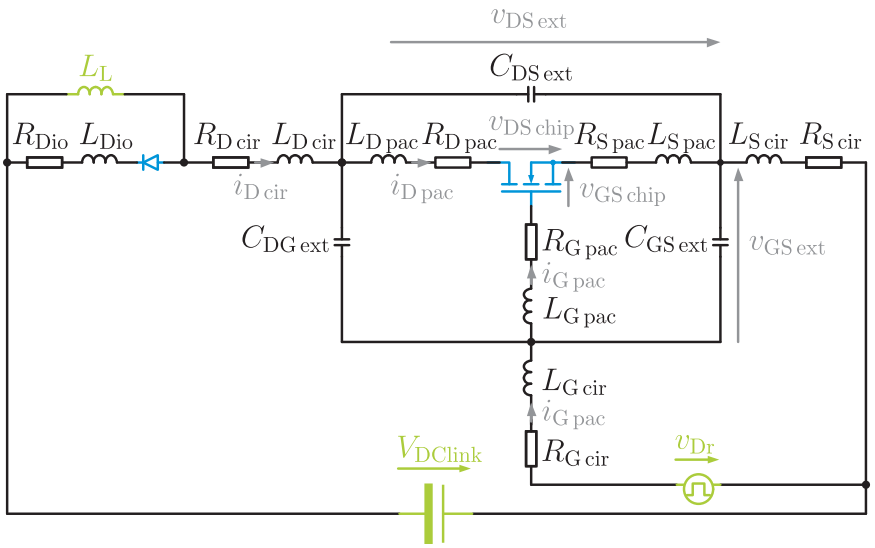


Figure 3.13: Switching behavioral model of a buck converter topology - The blue semiconductor symbols represent the behavioral models in Fig. 2.7 on page 19 and Fig. 2.11 on page 25 respectively. The green circuit elements represent simplified parts of the buck converter topology.

All other capacitances in Table 3.10 are disregarded.

Mutual inductances and resistances are not considered in the circuit model. The subsequent equations and their transpositions show that self and mutual inductances and resistances can be summarized in time dependent effective resistances $R_{\mathrm{i}}(t)$ and inductances $L_{\mathrm{i}}(t)$ if displacement currents through the CG sub-circuit are disregarded.

For the 'first' connector of an n-connector problem, the resistive voltage drop can be described by

$$\begin{aligned} v_{R_1}(t) &= R_{11} \cdot i_1(t) + R_{12} \cdot i_2(t) + \cdots + R_{1n} \cdot i_n(t) \\ &= i_1(t) \cdot \left(R_{11} + R_{12} \cdot \frac{i_2(t)}{i_1(t)} + \cdots + R_{1n} \cdot \frac{i_n(t)}{i_1(t)} \right) \\ &= i_1(t) \cdot R_1(t) \end{aligned} \tag{3.21}$$

and the inductive voltage drop can be described by

$$\begin{aligned} v_{L_1}(t) &= L_{11} \cdot \frac{\mathrm{d}i_1(t)}{\mathrm{d}t} + L_{12} \cdot \frac{\mathrm{d}i_2(t)}{\mathrm{d}t} + \cdots + L_{1n} \cdot \frac{\mathrm{d}i_n(t)}{\mathrm{d}t} \\ &= \frac{\mathrm{d}i_1(t)}{\mathrm{d}t} \cdot \left(L_{11} + L_{12} \cdot \frac{\mathrm{d}i_2(t)}{\mathrm{d}i_1(t)} + \cdots + L_{1n} \cdot \frac{\mathrm{d}i_n(t)}{\mathrm{d}i_1(t)} \right) \\ &= \frac{\mathrm{d}i_1(t)}{\mathrm{d}t} \cdot L_1(t) \end{aligned} \tag{3.22}$$

(for the derivation of the equations see Fig. 3.1(c) on page 68 or cp. with [Ans 99]).

According to Fig. 3.12(a) and Fig. 3.12(c) on page 88 et seq., the frequency dependency of parasitic resistances must be considered for the modeling of the corresponding voltage drops. However, the frequency dependency of the resistances is disregarded. The resistances in Fig. 3.13 are defined with the DC values in Table 3.6 on page 77:

$$R_{\mathrm{Dio}} := R_{\mathrm{PP\,DC}} + (R_{\mathrm{AA\,DC}} - R_{\mathrm{AL\,DC}}), \tag{3.23}$$

$$R_{\mathrm{D\,pac}} = R_{\mathrm{D\,cir}} = \frac{R_{\mathrm{D}}}{2} := \frac{R_{\mathrm{AL\,DC}}}{2} + \frac{R_{\mathrm{MM\,DC}} - R_{\mathrm{MS\,DC}}}{2}, \tag{3.24}$$

$$R_{\mathrm{G\,pac}} = R_{\mathrm{G\,int}} + \frac{R_{\mathrm{G}}}{2} := R_{\mathrm{G\,int}} + \frac{R_{\mathrm{GG\,DC}}}{2} + \frac{R_{\mathrm{SS\,DC}} - R_{\mathrm{MS\,DC}}}{2}, \tag{3.25}$$

$$R_{\mathrm{G\,cir}} = R_{\mathrm{G\,ext}} + \frac{R_{\mathrm{G}}}{2} := R_{\mathrm{G\,ext}} + \frac{R_{\mathrm{GG\,DC}}}{2} + \frac{R_{\mathrm{SS\,DC}} - R_{\mathrm{MS\,DC}}}{2} \text{ and} \tag{3.26}$$

$$R_{\mathrm{S\,pac}} = R_{\mathrm{S\,cir}} = \frac{R_{\mathrm{S}}}{2} := \frac{R_{\mathrm{MS\,DC}}}{2}. \tag{3.27}$$

Thereby, the T-network model in [Bracken 00] for the modeling of the self and mutual resistance between two conduction paths within the same conductor is applied. The usage of DC resistances means that the resistances are either over- or underestimated at different points in time during commutation.[20] However, related to the resistances $R_{\mathrm{G\,ext}}$, $R_{\mathrm{G\,int}}$ and $R_{\mathrm{DS\,chip}}$, the impact of the parasitic PCB and package resistances is usually negligible. The impact of different parasitic resistance values on the stability of commutation circuits is analyzed in section **5.2.4** on page 119 et seq.

Fig. 3.12(b) and Fig. 3.12(d) on page 88 et seq. show that inductances, which correspond to the accordant current slopes' equivalent frequency, enable the approximations of inductive voltage drops. Fig. 3.7 on page 78 shows that the inductance characteristics can roughly be distinguished in three regions - a DC, an AC and a transition region. In the DC and the AC region, the inductances change little with frequency. According to the parameters in Fig. 3.7, the DC region ends in the range of 100 Hz, and the AC region begins in the range of 10 MHz for the analyzed buck converter model. Equivalent frequencies of the current slopes during current commutation are in a range of ten to fifty megahertz. Due to the low frequency dependency of the inductances in this range, it is randomized that the inductances of 50 MHz in Fig. 3.7 are used for the determination of the effective inductances. The parameterization of effective inductances in Fig. 3.13 is defined with

$$L_{\mathrm{Dio}} := (L_{\mathrm{PP}}(f) + L_{\mathrm{PA}}(f) - L_{\mathrm{PM}}(f)) + (L_{\mathrm{AA}}(f) - L_{\mathrm{AL}}(f)), \tag{3.28}$$

$$L_{\mathrm{D\,pac}} = L_{\mathrm{D\,cir}} = \frac{L_{\mathrm{D}}}{2} := \frac{L_{\mathrm{AL}}(f)}{2} + \frac{L_{\mathrm{MM}}(f) - L_{\mathrm{MS}}(f)}{2}, \tag{3.29}$$

$$L_{\mathrm{G\,pac}} = L_{\mathrm{G\,cir}} = \frac{L_{\mathrm{G}}}{2} := \frac{L_{\mathrm{GG}}(f) - L_{\mathrm{GS}}(f)}{2} + \frac{L_{\mathrm{SS}}(f) - L_{\mathrm{MS}}(f)}{2} \text{ and} \tag{3.30}$$

$$L_{\mathrm{S\,pac}} = L_{\mathrm{S\,cir}} = \frac{L_{\mathrm{S}}}{2} := \frac{L_{\mathrm{MS}}(f)}{2}. \tag{3.31}$$

[20] Fig. 3.12(a) and Fig. 3.12(c) on page 88 et seq. allow the conclusion that the effective resistances may change their signs during current commutation.

For double source conductors, only the mutual inductance between the two conduction paths within the same conductor is regarded (cp. Fig. 3.8 on page 81 and Fig. 3.13 with (3.28) through (3.31)). Thereby, the T-network model in [Bracken 00] for the modeling of the self and mutual resistance between two conduction paths within the same conductor is accordingly applied. For single source connectors, only the mutual inductances L_{ij} with $L_{ij} = L_{ij} \cdot {}^{di_j}/_{di_i}$ are regarded in the calculation of the effective self inductances. Both results in too high loop inductance values in the circuit model. The impact of reduced circuit inductances on the occurrence of parasitic oscillations with temporarily increasing amplitudes is discussed in section **5.2.4** on page 119 et seq..

The indices 'cir' and 'pac' in (3.24) through (3.27) and in (3.29) through (3.31) are used to distinguish RL elements close to and further away from the MOSFET.[21] They do *not* refer to RL proportions that are caused by the TO-220 package and the PCB respectively. The calculation of the parasitic circuit elements of the sample buck converter topology is presented in Table 3.11. As defined in (3.24) through (3.27) and in (3.29) through (3.31), one half of the drain, gate and source inductance and resistance is dedicated to the corresponding 'circuit' and 'package' inductance and resistance respectively.

Table 3.11: Calculation of the parasitic parameters of the buck converter model in Fig. 3.13 with the resistances in Table 3.6 and the $f = 50\,\mathrm{MHz}$ inductances in Fig. 3.7

Parameter	**Calculation**	**Result**
L_D	$L_\mathrm{AL}(f) + L_\mathrm{MM}(f) - L_\mathrm{MS}(f)$	27.91 nH
R_D	$R_\mathrm{AL\,DC} + R_\mathrm{MM\,DC} - R_\mathrm{MS\,DC}$	0.94 mΩ
L_G	$L_\mathrm{GG}(f) - L_\mathrm{GS}(f) + L_\mathrm{SS}(f) - L_\mathrm{MS}(f)$	4.18 nH
R_G	$R_\mathrm{GG\,DC} + R_\mathrm{SS\,DC} - R_\mathrm{MS\,DC}$	27.89 mΩ
L_S	$L_\mathrm{MS}(f)$	4.99 nH
R_S	$R_\mathrm{MS\,DC}$	0.82 mΩ
L_Dio	$L_\mathrm{PP}(f) + L_\mathrm{PA}(f) - L_\mathrm{PM}(f) + L_\mathrm{AA}(f) - L_\mathrm{AL}(f)$	13.05 nH
R_Dio	$R_\mathrm{PP\,DC} + R_\mathrm{AA\,DC} - R_\mathrm{AL\,DC}$	1.41 mΩ
$C_\mathrm{DS\,ext}$	C_LM	2.74 pF
$C_\mathrm{DG\,ext}$	C_LG	5.49 pF
$C_\mathrm{GS\,ext}$	C_GM	0.14 pF

[21] In (3.26), $R_\mathrm{G\,ext}$ is assigned to $R_\mathrm{G\,cir}$. Depending on the location of $R_\mathrm{G\,ext}$ in the commutation cell, $R_\mathrm{G\,ext}$ could also be allocated between $R_\mathrm{G\,cir}$ and $R_\mathrm{G\,pac}$.

4 Evaluation of the Behavioral Modeling of Commutation Cells

Large-signal models of the semiconductor devices, the packages and the PCB, and the parameterization of these large-signal models are discussed in chapter **2** and chapter **3**. The applicability of the parameterized large-signal models for the modeling of switching operations is a precondition for the stability analysis in chapter **5**. The proposed modeling is evaluated in this chapter. Using the example of the buck converter topology of the previous chapters, simulated and measured switching characteristics of the SJ MOSFET are compared in section **4.1**. In section **4.2**, conclusions are drawn on the applicability of the proposed behavioral model for the stability analysis.

4.1 Comparison of Measured and Simulated Switching Characteristics

The measurement setup of the switching characteristics, which are subsequently presented, is shown in principle in Fig. 2.25 on page 49. The setup is modeled and parameterized in subsection **3.2.3** on page 75 et seq.. In subsection **3.3.3** on page 90 et seq., a simplified behavioral model of the measurement setup is deduced for the simulation of switching characteristics. The model is shown in Fig. 3.13 on page 91.[1] For the simulation of switching characteristics, the semiconductor device models are parameterized according to section **2.3** on page 26 et seq.[2] and section **2.4** on page 48 et seq. unless it is stated otherwise. The PCB model is parameterized - with the exception of the chip-external drain gate capacitance $C_{\mathrm{DG\,ext}}$ - according to equations (3.23) through (3.31) and Table 3.11 on page 92 et seq.. $C_{\mathrm{DG\,ext}}$ is reduced to 0.5 pF. The reduction is due to a difference of the modeled (original) measurement setup in Fig. 3.6(a) on page 75 and the setup used for the dynamic measurements. In the original measurement setup, parasitic oscillations occur. In order to diminish the capacitive coupling between gate and drain, the gate pin is not connected to the gate pad of the PCB but bend up ninety degrees in the used measurement setup. The impact of this modification on the parameterization of the other circuit elements is disregarded.

The different circuit parameters can not be verified independently of one another. However, conclusions on the accuracy of some parameters can be drawn by comparison of measured and simulated switching characteristics with respect to ...

[1] The simulations of switching characteristics in this and the following chapter are performed in *MATLAB* & *Simulink*. Thereto, the circuit model in Fig. 3.13 was implemented in *MATLAB* & *Simulink*.

[2] The channel current range of the output characteristics is extended to 40 A by means of interpolation.

- ... their gate current characteristics, ...
- ... their gate source voltage slopes, and their MILLER plateau voltage and length, ...
- ... their drain source voltage and drain current slopes, ...
- ... their drain source overvoltage during the turn-off current commutation and their drain source voltage drop during the turn-on current commutation, ...
- ... their drain current reduction during the turn-off voltage commutation and their drain current increase during the turn-on voltage commutation, and ...
- ... occurring oscillations.

Switching operations with relatively high gate resistances are characterized by a reduced impact of parasitic couplings compared to switching operations with relatively low gate resistances. This is advantageous for a first evaluation of the circuit model in Fig. 3.13 on page 91. The comparison of measured and simulated switching characteristics with relatively low gate resistances enables the evaluation of the proposed modeling of couplings. Due to these reasons, measured and simulated switching operations with $R_{\mathrm{G\,ext}} = 100\,\Omega$ and with $R_{\mathrm{G\,ext}} = 10\,\Omega$ are compared subsequently.

For the comparison of simulated and measured switching characteristics, ...

- ... the indexes of the simulated switching characteristics correspond to the labeled currents and voltages in Fig. 3.13 and Fig. 2.7 on page 19 respectively. The simulated characteristics are labeled with the index 'sim'.
- ... possible offsets in the measured voltage and current signals are corrected in the presented characteristics.
- ... only chip voltages are shown. From the measured voltages, the chip voltages are calculated according to subsection **3.3.2** on page 85 et seq..
- ... the measured characteristics are labeled with the index 'meas'.
- ... the coefficients of the PT2 element, which delays the rectangular gate driver signal, are used for the fitting of the gate current and the gate source voltage signals.

Comparison of Switching Characteristics with Different Capacitances

Fig. 4.1 shows measured and simulated switching characteristics with $R_{\mathrm{G\,ext}} = 100\,\Omega$. A comparison of Fig. 4.1(a) and Fig. 4.1(c), and Fig. 4.1(b) and Fig. 4.1(d) illustrate the disadvantages of a parameterization that is based on the data sheet capacitances C_{iss}, C_{rss} and C_{oss}. The circuit model of the simulated characteristics in Fig. 4.1(a) and Fig. 4.1(b), and the simulated characteristics in Fig. 4.1(c) and Fig. 4.1(d) is exactly the same - solely $C_{\mathrm{DG\,chip}}$ and $C_{\mathrm{GS\,chip}}$ are slightly different. $C_{\mathrm{DS\,chip}}$ is identical. The capacitance parameterization in Fig. 4.1(a) and Fig. 4.1(b) is given by

$$C_{\mathrm{DS\,chip}}(V_{\mathrm{DS\,chip}}) = C_{\mathrm{oss}}(V_{\mathrm{DS\,chip}}) - C_{\mathrm{rss}}(V_{\mathrm{DS\,chip}}), \tag{4.1}$$

$$C_{\mathrm{DG\,chip}}(V_{\mathrm{DS\,chip}}) = C_{\mathrm{rss}}(V_{\mathrm{DS\,chip}}) \text{ and} \tag{4.2}$$
$$C_{\mathrm{GS\,chip}}(V_{\mathrm{DS\,chip}}) = C_{\mathrm{iss}}(V_{\mathrm{DS\,chip}}) - C_{\mathrm{rss}}(V_{\mathrm{DS\,chip}}). \tag{4.3}$$

The resulting characteristics are shown in Fig. 4.2 with the index 'ss'. In Fig. 4.1(c) and Fig. 4.1(d), the dynamic capacitances, which are proposed in subsection **2.4.1**, are used. In Fig. 4.2, these capacitances are labeled with the index 'dyn'. Even though the small-signal and the dynamic capacitances are quite similar, the differences between the MILLER plateau lengths, the gate charges and the gate source voltage slopes in Fig. 4.1 are significant. The switching characteristics, which correspond to the dynamic capacitances, correlate well with the measurement data. In some time ranges, the switching characteristics, which correspond to the small-signal capacitances, differ significantly from the measurement data. This is because the small-signal capacitances are measured with a gate source voltage of zero volt. Accordingly, the impact of the accumulation and the inversion layer beneath the gate oxide is neglected. Fig. 4.1 proves that the parameterization with the dynamic capacitances results in a more accurate modeling of the MOSFET's switching behavior than the parameterization with small-signal capacitances that are measured according to DIN IEC 747.

Switching Characteristics with a Relatively High Gate Resistance

The comparison of measured and simulated characteristics in Fig. 4.1(c) and Fig. 4.1(d) with the relatively high gate resistance $R_{\mathrm{G\,ext}} = 100\,\Omega$ allows the following conclusions:

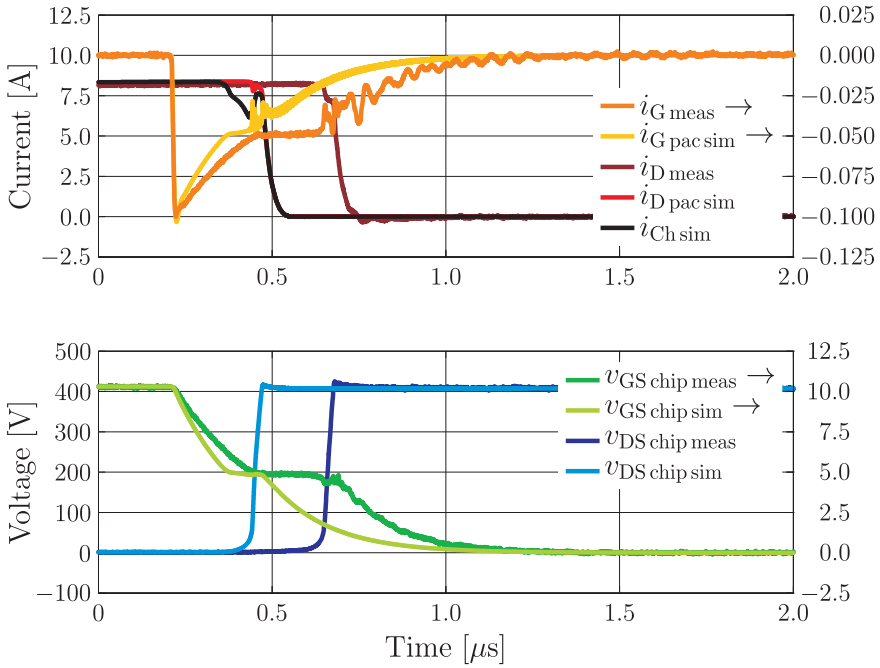
- Apart from the time ranges with oscillations, the differences between the simulated and the measured ***gate currents*** are below 5 %. The gate current charges mainly the gate capacitances $C_{\mathrm{GS\,chip}}$ and $C_{\mathrm{DG\,chip}}$. Thus, the good consistency of the measured and the simulated gate currents indicates a relatively high accuracy of the input capacitance C_{in} in the buck converter model.[3]

- The differences between the simulated and measured ***drain source voltage slopes*** are below 10 %. Due to the relatively high gate resistance, the charging of the drain gate capacitances $C_{\mathrm{DG\,chip}}$ and $C_{\mathrm{DG\,ext}}$ limits the steep part of the drain source voltage slope. Therewith, the comparision of the simulated and measured drain source voltage slopes indicates a relatively high accuracy of the sum of $C_{\mathrm{DG\,chip}}$ and $C_{\mathrm{DG\,ext}}$ at higher drain source voltages in the circuit model.
  The difference between the simulated and measured ***drain current slopes*** is below 10 %. The drain current slope is mainly given by the gate capacitances $C_{\mathrm{GS\,chip}}$ and $C_{\mathrm{DG\,chip}}$, the gate resistances, the source inductances and the commutation circuit inductance.[4] The good consistency of the measured and simulated drain current slopes indicates a relatively high accuracy of these parameters in the buck converter model.

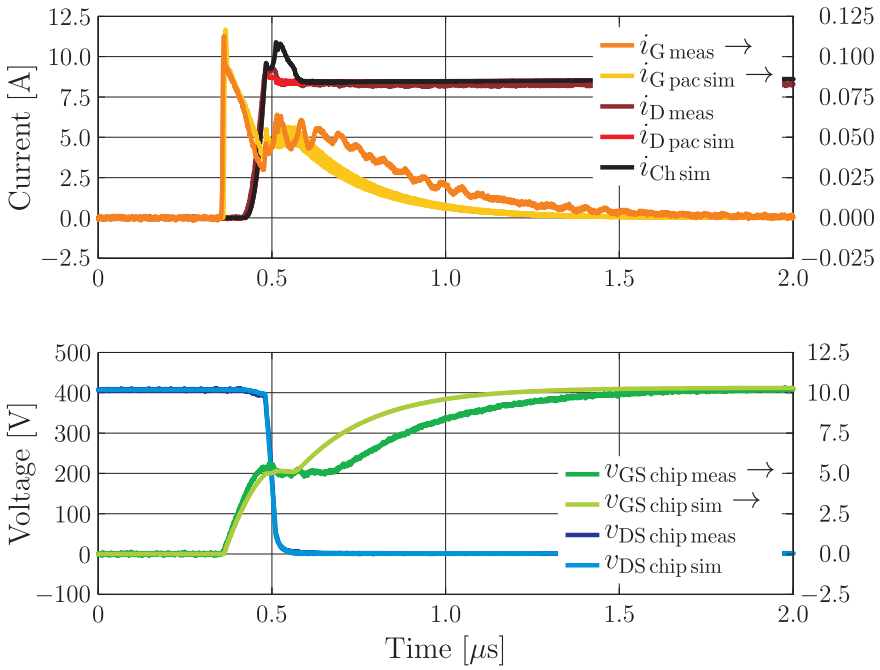
- The difference between simulated and the measured ***gate source voltage slopes*** before and after the MILLER plateau is below 5 %. The gate source voltage slopes

[3] The input capacitance is defined in **2.4.1.2** on page 51.

[4] In the buck converter circuit in Fig. 3.13 on page 91, the commutation circuit inductance is given by the sum of the inductances L_{Dio}, $L_{\mathrm{D\,cir}}$, $L_{\mathrm{D\,pac}}$, $L_{\mathrm{S\,pac}}$ and $L_{\mathrm{S\,cir}}$.

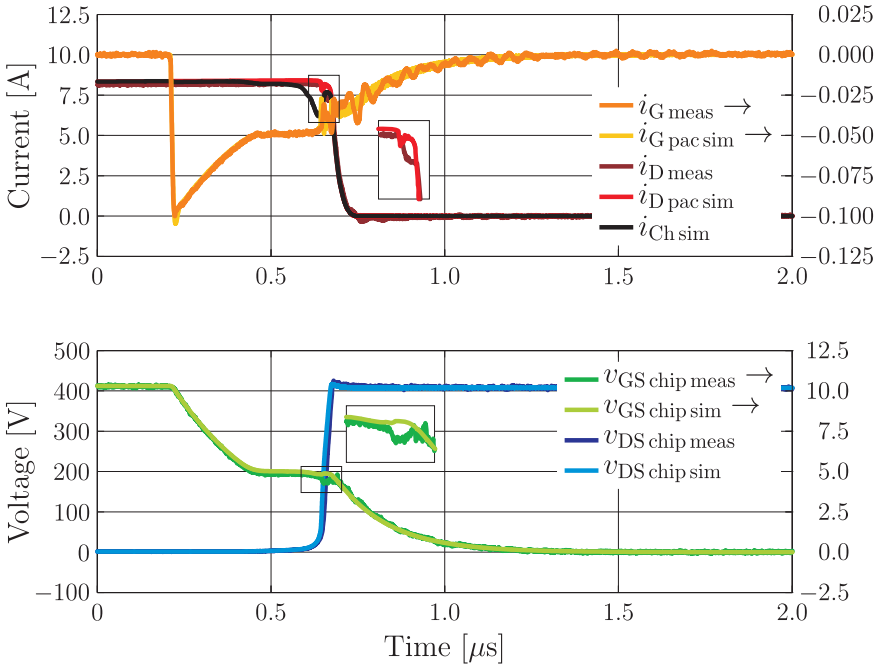


(a) Turn-off characteristics with $R_{G\,ext} = 100\,\Omega$, $V_{DClink} = 400\,V$, $i_L = 8\,A$ and $\vartheta_J = 25\,°C$ - parameterization of the simulation model with $C_{DG\,ss}$, $C_{GS\,ss}$ & $C_{DS\,ss}$ in Fig. 4.2

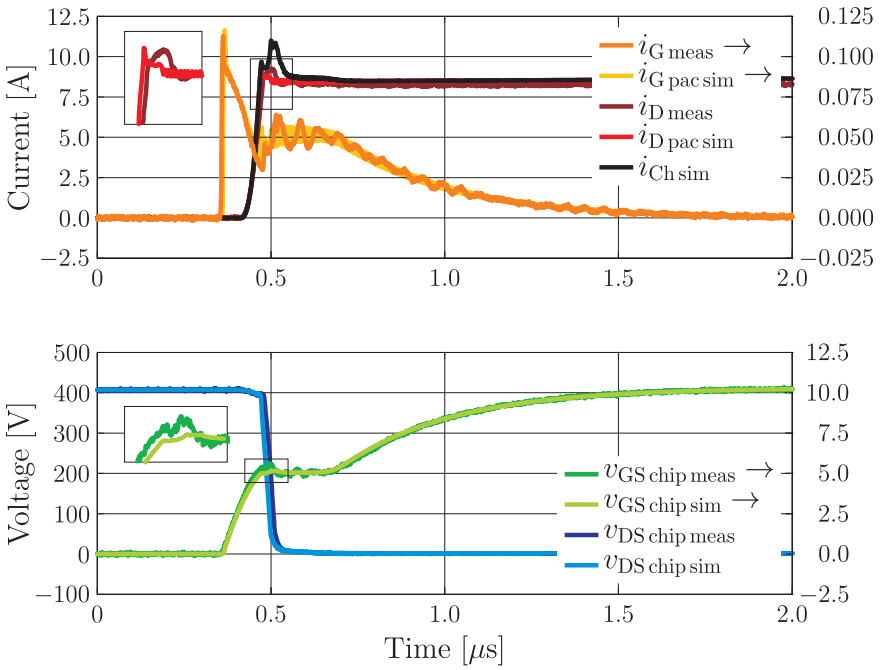


(b) Turn-on characteristics with $R_{G\,ext} = 100\,\Omega$, $V_{DClink} = 400\,V$, $i_L = 8\,A$ and $\vartheta_J = 25\,°C$ - parameterization of the simulation model with $C_{DG\,ss}$, $C_{GS\,ss}$ & $C_{DS\,ss}$ in Fig. 4.2

Figure 4.1: Comparison of switching characteristics - measurements vs. simulations with small-signal or dynamic capacitances as chip-internal capacitances



(c) Turn-off characteristics with $R_{G\,ext} = 100\,\Omega$, $V_{DClink} = 400\,V$, $i_L = 8\,A$ and $\vartheta_J = 25\,°C$ - parameterization of the simulation model with $C_{DG\,dyn}$, $C_{GS\,dyn}$ & $C_{DS\,dyn}$ in Fig. 4.2



(d) Turn-on characteristics with $R_{G\,ext} = 100\,\Omega$, $V_{DClink} = 400\,V$, $i_L = 8\,A$ and $\vartheta_J = 25\,°C$ - parameterization of the simulation model with $C_{DG\,dyn}$, $C_{GS\,dyn}$ & $C_{DS\,dyn}$ in Fig. 4.2

Figure 4.1: Comparison of switching characteristics - measurements vs. simulations with small-signal or dynamic capacitances as chip-internal capacitances (cont.)

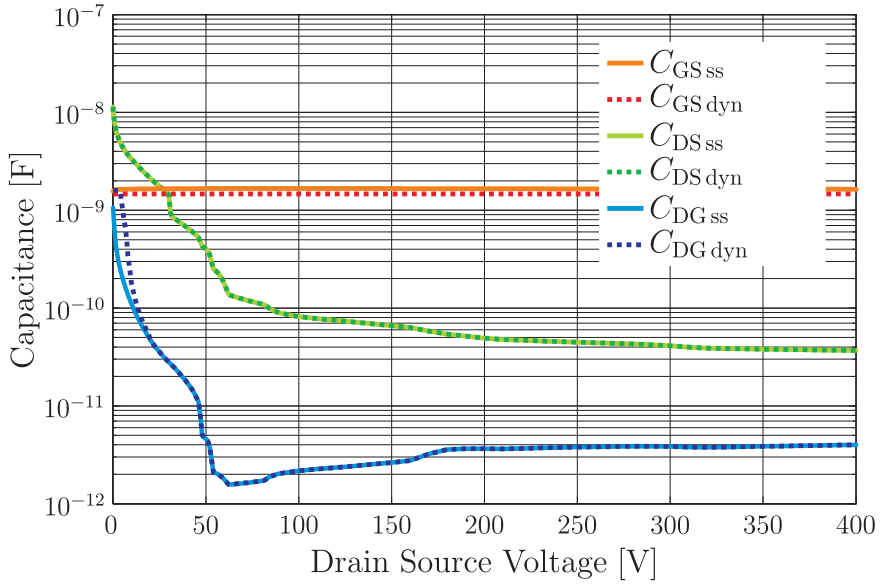


Figure 4.2: Comparison of small-signal and dynamic capacitances

are mainly given by the gate resistances and the input capacitance C_{in}. Accordingly, the comparison of the simulated and measured gate source voltage slopes indicates a relatively high accuracy of these parameters in the circuit model.

Apart from the oscillations on the measured MILLER plateau, the differences between the measured and the simulated ***Miller plateau voltages*** are below 5 %.[5] The MILLER plateau voltage represents the channel current during voltage commutation. Due to the DUT's high transconductance, minor deviations in the MILLER plateau voltage represent considerable differences between the actual and simulated channel currents. In the simulated characteristics, during the steep part of the drain source voltage slope, the missing gate source voltage drop in Fig. 4.1(c) and the missing gate source voltage increase in Fig. 4.1(d) indicate a too large channel current during the turn-off voltage commutation and a too small channel current during the turn-on voltage commutation. The remaining discrepancies can be explained by the differences between $C_{\mathrm{DS\,chip}}(v_{\mathrm{DS\,chip}},\, i_{\mathrm{L}} = 8\,\mathrm{A})$ in Fig. 2.29(a) and $C_{\mathrm{DS\,dyn}}$ in Fig. 4.2.[6]

The difference between the measured and simulated ***Miller plateau length*** is also below 5 %. The MILLER plateau length is mainly given by the duration of the voltage commutation. Thereby, the steep part of the DUT's drain source voltage slope constitutes at most half of the MILLER plateau length. The rest of the plateau correlates to the charging of $C_{\mathrm{DG\,chip}}$ at low drain source voltages (see Fig. 4.2 and cp. Fig. 4.1(c) and Fig. 4.1(a), as well as Fig. 4.1(d) and Fig. 4.1(b)). Since the difference between the steep part of the measured and simulated drain source voltage slopes is below

[5] The term 'MILLER plateau' is only to a limited extent suitable for the DUT. During voltage commutation, the channel current is considerably decreased or increased by $i_{\mathrm{DS\,chip}} = C_{\mathrm{DS\,chip}} \cdot {}^{\mathrm{d}v_{\mathrm{DS\,chip}}}/_{\mathrm{d}t}$. This results in an increasing or decreasing $v_{\mathrm{GS\,chip}}$. The lower the gate resistances, the stronger is the alteration.

[6] In [Höch 09c], the circuit model is parameterized with the characteristic $C_{\mathrm{DS\,chip}}(v_{\mathrm{DS\,chip}},\, i_{\mathrm{L}} = 8\,\mathrm{A})$ in Fig. 2.29(a) on page 59. The usage of $C_{\mathrm{DS\,chip}}(v_{\mathrm{DS\,chip}},\, i_{\mathrm{L}} = 8\,\mathrm{A})$ results in reduced differences between the simulated and measured MILLER plateau voltage during the MOSFET's turn-off.

10 %, the Miller plateau length indicates a high accuracy of drain gate capacitance characteristic in the buck converter circuit model at low drain source voltages.

- The difference between the measured and the simulated drain source overvoltage during the turn-off current commutation is below 5 %. The ***drain source overvoltage and voltage drop*** during the turn-off and the turn-on current commutation are mainly caused by the changing current through the commutation circuit inductance. The good consistency of measurement and simulation indicates a relatively high accuracy of the commutation circuit inductance in the buck converter model.
- In the simulation, the ***drain current reduction*** and the ***drain current increase*** during the turn-off and turn-on voltage commutation is slightly smaller than in the measurement. The drain current reduction and increase during the voltage commutation is mainly caused by the depletion capacitance of the SCHOTTKY diode and parasitic coupling capacitances connected to the drain and the diode's current path.[7] The differences between simulation and measurement indicate that the actual capacitances in the measurement setup are not completely considered in the model.
- The measured gate source voltage and the measured current characteristics show ***oscillations***. In the simulated gate source voltage characteristics no oscillations can be observed. The simulated current characteristics shows oscillations with higher frequencies than in the measured characteristics. Possible reasons for the differences are a too low band width of the used PEARSON probes [Pea 99], and the superposition of measured and interfering signals.

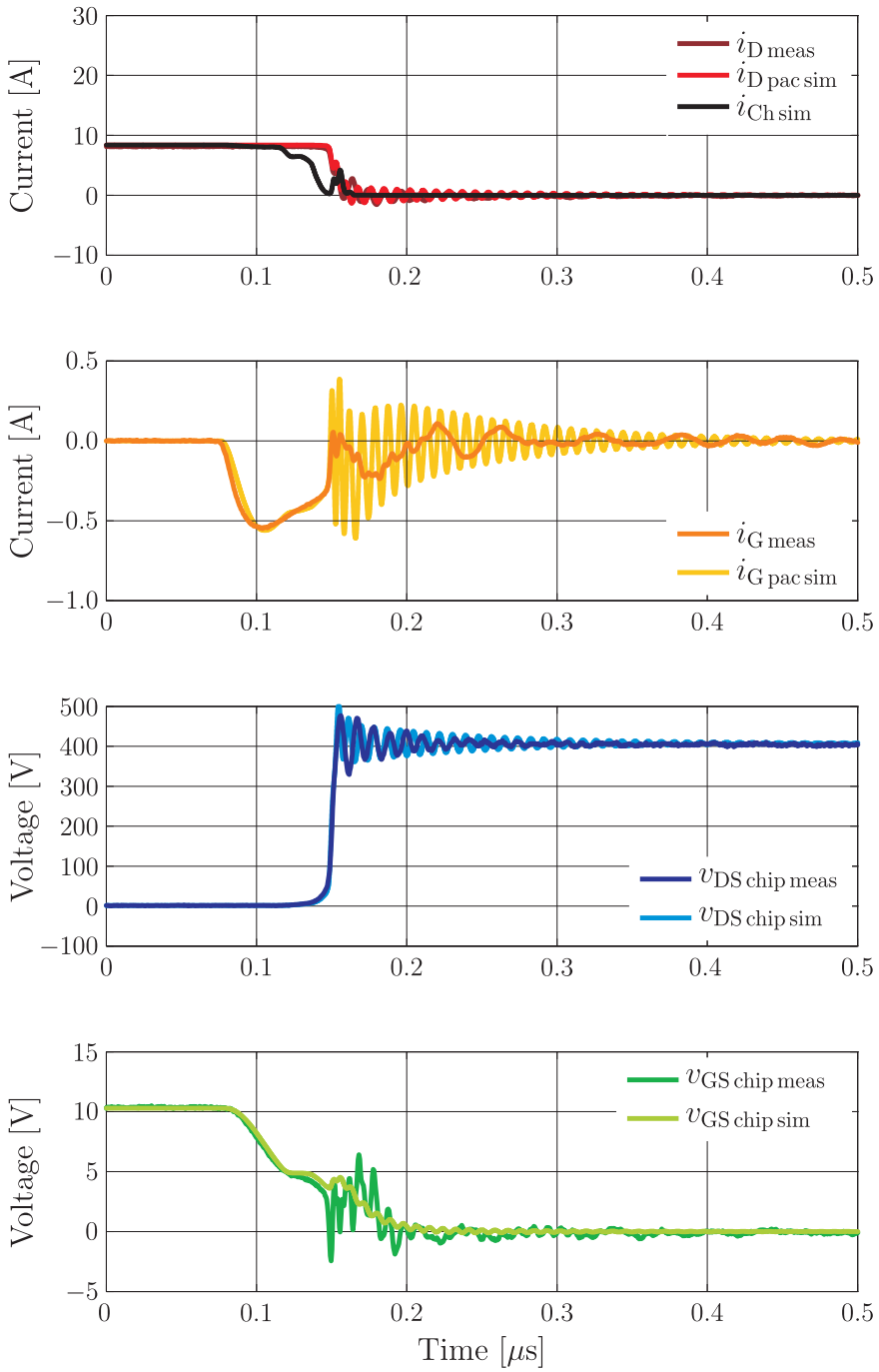
Fig. 4.1(c) and Fig. 4.1(d) validate the circuit model's ability to simulate the MOSFET's terminal behavior for relatively slow switching operations with a relatively high accuracy.

Switching Characteristics with a Relatively Low Gate Resistance

The evaluation of simulated switching characteristics with an application-relevant gate resistance is of particular interest for the stability analysis in chapter **5**. Measurements and simulations of switching operations with the relatively low gate resistance $R_{\mathrm{G\,ext}} = 10\,\Omega$ are compared in Fig. 4.3. The comparison allows the following conclusions:

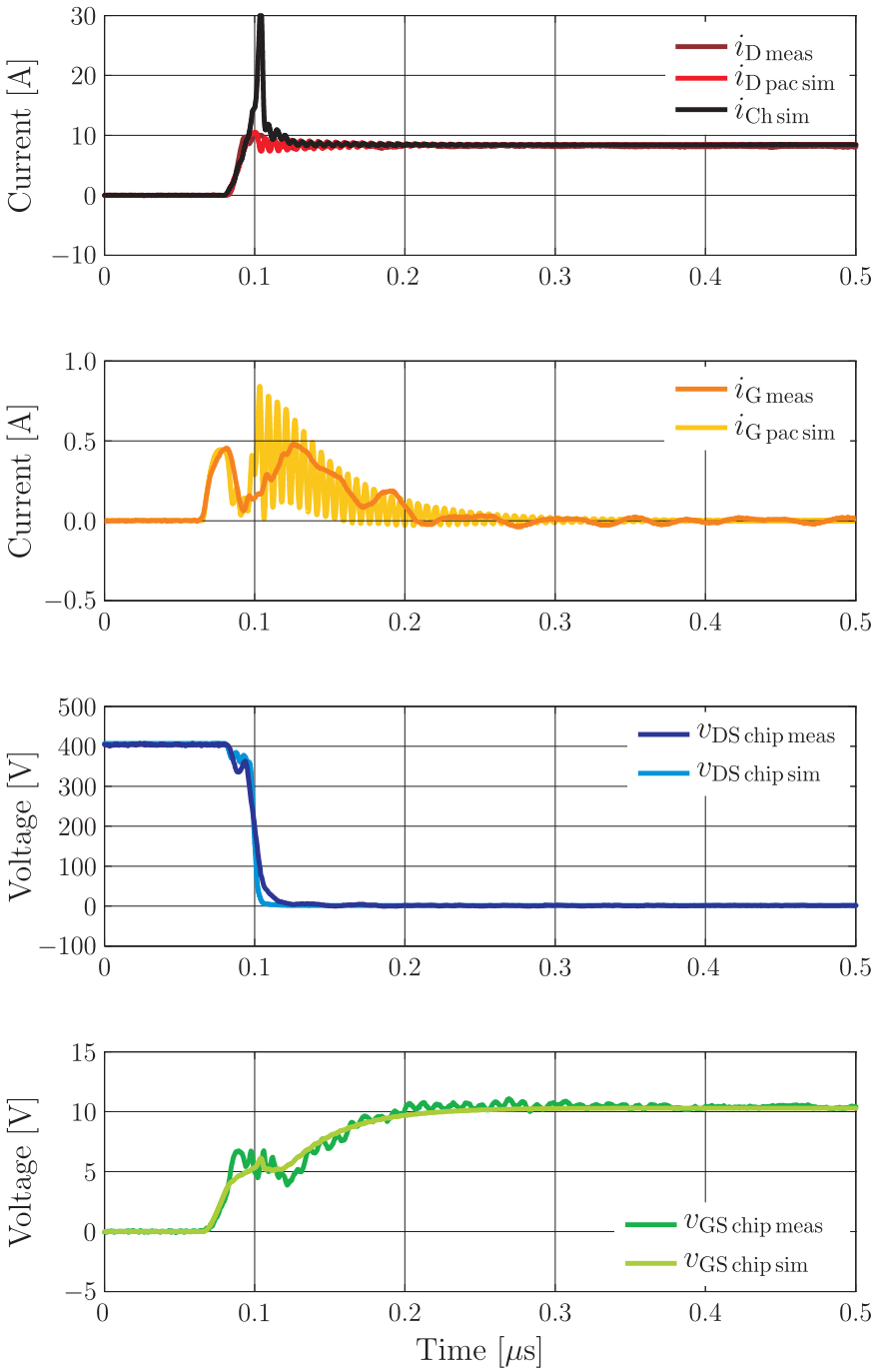
- Apart from time ranges with oscillations, the difference between the simulated and measured ***gate currents*** is below 10 %. This indicates a relatively accurately modeled input capacitance C_{in} in the circuit model.
- The difference between the simulated and the measured ***drain source voltage slopes*** in Fig. 4.3(a) is below 5 %. Despite the relatively low gate resistance, the charging of $C_{\mathrm{DG\,chip}}$ and $C_{\mathrm{DG\,ext}}$ still limits the drain source voltage slope. This is confirmed by the simulated channel current, which is above zero during the steep part of the drain source voltage slope. Hence, the characteristics indicate a relatively high accuracy of the drain gate capacitances' sum at higher drain source voltages. In Fig. 4.3(c), the

[7] The capacitances are connected to the i_{A} and i_{L} current paths in the model in Fig. 3.8 on page 81.



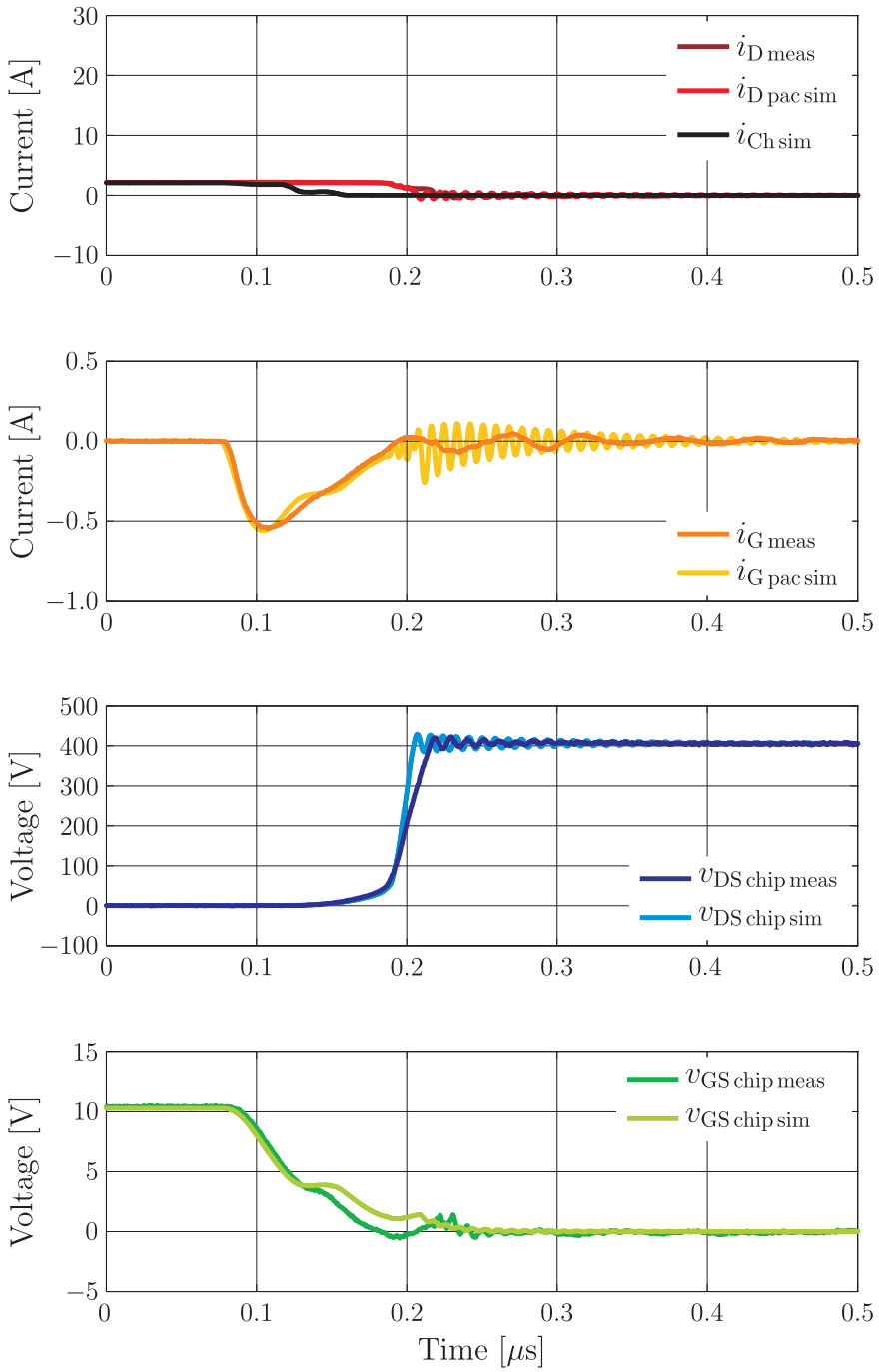
(a) Turn-off characteristics with $R_{\mathrm{G\,ext}} = 10\,\Omega$, $V_{\mathrm{DClink}} = 400\,\mathrm{V}$, $i_{\mathrm{L}} = 8\,\mathrm{A}$ and $\vartheta_{\mathrm{J}} = 25\,^{\circ}\mathrm{C}$

Figure 4.3: Measurements vs. simulations with dynamic capacitances



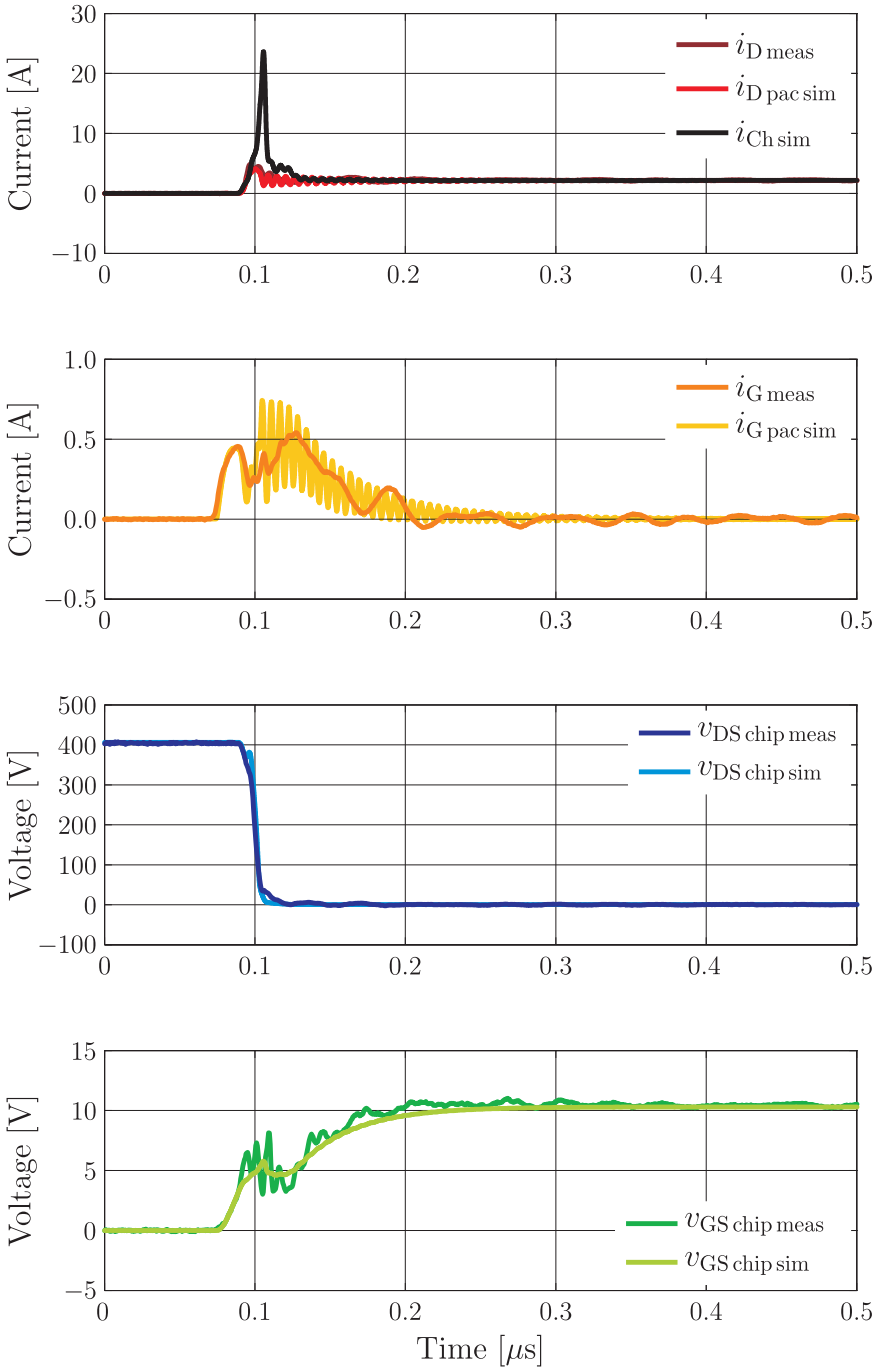
(b) Turn-on characteristics with $R_{\mathrm{G\,ext}} = 10\,\Omega$, $V_{\mathrm{DClink}} = 400\,\mathrm{V}$, $i_{\mathrm{L}} = 8\,\mathrm{A}$ and $\vartheta_{\mathrm{J}} = 25\,^{\circ}\mathrm{C}$

Figure 4.3: Measurements vs. simulations with dynamic capacitances (cont.)



(c) Turn-off characteristics with $R_{\mathrm{G\,ext}} = 10\,\Omega$, $V_{\mathrm{DClink}} = 400\,\mathrm{V}$, $i_{\mathrm{L}} = 2\,\mathrm{A}$ and $\vartheta_{\mathrm{J}} = 25\,^{\circ}\mathrm{C}$

Figure 4.3: Measurements vs. simulations with dynamic capacitances (cont.)



(d) Turn-on characteristics with $R_{\mathrm{G\,ext}} = 10\,\Omega$, $V_{\mathrm{DClink}} = 400\,\mathrm{V}$, $i_{\mathrm{L}} = 2\,\mathrm{A}$ and $\vartheta_{\mathrm{J}} = 25\,^{\circ}\mathrm{C}$

Figure 4.3: Measurements vs. simulations with dynamic capacitances (cont.)

charging of $C_{\mathrm{DS\,chip}}$ limits the drain source voltage slope, because the channel current is zero during significant parts the voltage commutation. The differences between the measured and the simulated drain source voltage slope indicate that the modeled $C_{\mathrm{DS\,chip}}$ is too small. For the simulation in Fig. 4.4, $C_{\mathrm{DS\,chip}}(v_{\mathrm{DS\,chip}}, i_{\mathrm{L}} = 2\,\mathrm{A})$ in Fig. 2.29 on page 59 and $C_{\mathrm{DG\,chip}}(v_{\mathrm{DG\,chip}}, i_{\mathrm{L}} = 2\,\mathrm{A})$ in Fig. 2.28 on page 56 are used. In Fig. 4.4, the difference between the simulated and the measured drain source voltage slopes is below 5 %. A too small $C_{\mathrm{DS\,chip}}$ is also the reasons for the differences in the drain source voltage slopes in Fig. 4.3(c) and Fig. 4.3(d).[8]
The slight differences between the measured and the simulated ***drain current slopes*** in Fig. 4.3(b) and Fig. 4.3(d) are probably due to the neglect of the gate related couplings in the definition of the effective source inductances in (3.31). Due to oscillations during the current commutation, the simulated and measured drain current slopes in Fig. 4.3(a) and Fig. 4.3(c) can not be compared.

- In Fig. 4.3, the differences between the simulated and the measured ***gate source voltage slopes*** before the drain current and the drain source voltage commutation are below 5 %. This indicate a relatively high accuracy of the gate resistances and the input capacitance C_{in} in the circuit model in this time range.
  During the ***turn-off commutation*** in Fig. 4.3(a), apart from the oscillations, the differences between the simulated and the measured gate source voltages are below 10 %. The simulated gate source voltage is slightly too high. In Fig. 4.3(c), the simulated and the measured gate source voltages differ significantly. The comparison of Fig. 4.3(c) and Fig. 4.4 allows the conclusion that the differences are due to the parameterization of the drain capacitances.
  During the ***turn-on commutation***, apart from the oscillations, the simulated and measured gate source voltage characteristics match relatively well. In the simulation, the too slow drain current and the too fast drain source voltage commutation result in a horizontal offset to the measured gate source voltage characteristics.

- The simulated ***drain source voltage reduction*** during the turn-on current commutation in Fig. 4.3(b) and Fig. 4.3(d) is less distinct than in the corresponding measurements. Since the drain current slope is slightly too flat during simulated current commutation, a direct conclusion on the commutation circuit inductance's parameterization is not possible. In Fig. 4.3(a) and Fig. 4.3(c), the difference between the simulated and the measured ***drain source overvoltage*** during the turn-off current commutation is below 10 %. Taking the corresponding drain current slopes into account, this indicates a relatively high accuracy of the sum of commutation circuit inductances in the simulation circuit.

- The ***drain current reduction*** and the ***drain current increase*** during the simulated and the measured voltage commutations differ. In Fig. 4.3(b) through Fig. 4.3(d)

[8] $C_{\mathrm{DG\,chip}}$ and $C_{\mathrm{DS\,chip}}$ could not be determined from turn-on operations due to parasitic oscillations. During voltage commutation, $v_{\mathrm{GS\,chip}}$ of turn-on operations is higher than $v_{\mathrm{GS\,chip}}$ of the corresponding turn-off operations (see e.g. Fig. 5.1 on page 112). With respect to Fig. 2.29 on page 59 and the channel currents in Fig. 4.3, it is assumed that the turn-on $C_{\mathrm{DS\,chip}}(V_{\mathrm{DS\,chip}})$ is higher than the corresponding turn-off $C_{\mathrm{DS\,chip}}(V_{\mathrm{DS\,chip}})$ - especially at low drain source voltages.

the simulated drain current reduction and the simulated drain current increase is more distinct than in the corresponding measurements. However, the simulated drain source voltage slopes are steeper than the measured slopes. Therefore, a direct conclusion on the parameterization of the depletion capacitance of the SCHOTTKY diode and the modeling of the parasitic coupling capacitances, which are connected to the drain and the diode's current path, is not possible. In Fig. 4.3(a), the difference between the simulated and the measured drain source voltage slope is below 5 %. The slightly reduced drain current reduction during the simulated voltage commutation indicates that the mentioned capacitances are not completely considered in the circuit model.

- The simulated gate current is oscillating with a higher frequency than the measured gate current. As the ***oscillation*** frequencies of the measured gate source voltage signals are similar to the oscillation frequency on the simulated gate current, it is assumed that the used PEARSON probe does not capture the oscillations accurately. In comparison to the simulated gate source voltage characteristics, the measured gate source voltage characteristics have more distinct oscillations amplitudes. The measured drain source voltage characteristics show low frequency oscillations. The simulated drain source voltage is not oscillating. Possible reasons for the differences are the neglect of mutual inductances in the defined effective inductances in equation (3.28) through (3.31) on page 92 and the superposition of measured and interfering signals.[9]
- For relatively small gate resistance, differences between the measured and simulated switching characteristics could also be caused by the ***neglect of properties of the driver IC***. In [Petzoldt 01], it is shown that the consideration of the internal driver resistance and inductance as well as an equivalent capacitance reduces differences between simulations and measurements. However, these circuit elements could be considered in $R_{\mathrm{G\,cir}}$, $L_{\mathrm{G\,cir}}$ and $C_{\mathrm{GS\,ext}}$ of the equivalent circuit model in Fig. 3.13.
- For relatively small gate resistance, differences between the measured and simulated switching characteristics could also be due to the ***distributed chip-internal gate resistance*** on the silicon chip. Due the distributed gate resistance, the chip's MOSFET cells do not switch homogeneously. The impact of a distributed chip-internal gate resistance is not considered in this work. Future works could analyze the impact of a distributed gate resistance by connecting several MOSFET models accordingly.

Therewith, the comparison of the switching operations with $R_{\mathrm{G\,ext}} = 10\,\Omega$ confirms most of the findings of the switching operations with $R_{\mathrm{G\,ext}} = 100\,\Omega$. Even though measured and simulated switching characteristics differ in parts, the characteristics in Fig. 4.3 validate the proposed circuit model's ability to simulate the MOSFET's terminal behavior for relatively fast switching operations with a relatively good accuracy.

For a more comprehensive evaluation of the modeling, a wider operating range could be compared. However, the comparison has revealed the major shortcomings of the proposed parameterization. More findings are not expected from an extended comparison.

[9] In Fig. A.1 on page 178 et seq., the simulated chip characteristics i_{Ch}, $i_{\mathrm{D\,pac}}$, $i_{\mathrm{G\,pac}}$, $v_{\mathrm{DS\,chip}}$ and $v_{\mathrm{GS\,chip}}$ are compared to the simulated chip-external characteristics $i_{\mathrm{D\,cir}}$, $i_{\mathrm{G\,cir}}$, $v_{\mathrm{DS\,ext}}$ and $v_{\mathrm{GS\,ext}}$. The comparison shows e.g. that the oscillation amplitudes of $v_{\mathrm{GS\,ext}}$ are higher than the oscillation amplitudes of $v_{\mathrm{GS\,chip}}$.

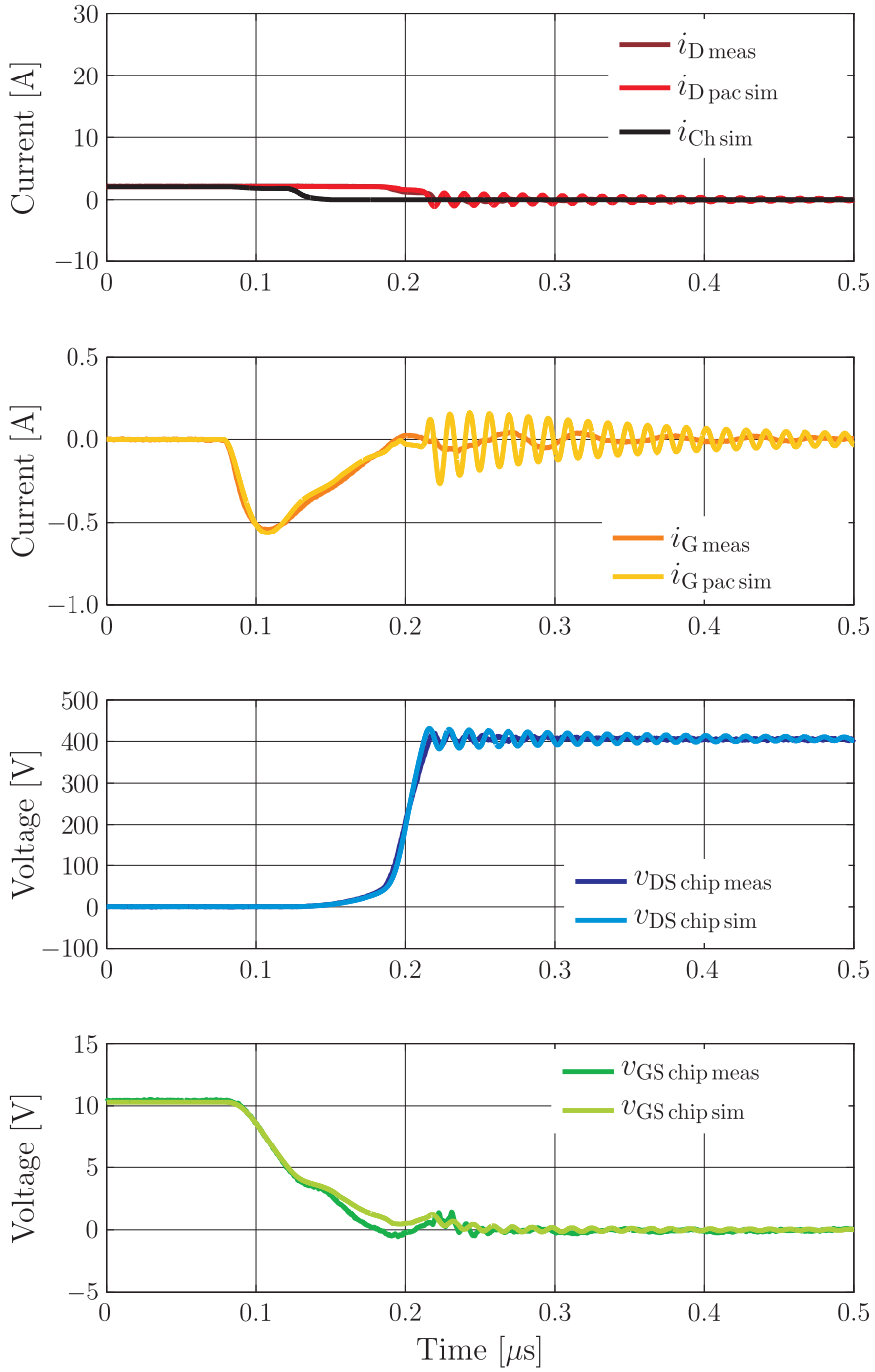


Figure 4.4: Measurements vs. simulations: Turn-off characteristics with $R_{\mathrm{G\,ext}} = 10\,\Omega$, $V_{\mathrm{DClink}} = 400\,\mathrm{V}$, $i_{\mathrm{L}} = 2\,\mathrm{A}$ and $\vartheta_{\mathrm{J}} = 25\,^{\circ}\mathrm{C}$ with $C_{\mathrm{DS\,chip}}(v_{\mathrm{DS\,chip}}, i_{\mathrm{L}} = 2\,\mathrm{A})$ in Fig. 2.29 on page 59 and $C_{\mathrm{DG\,chip}}(v_{\mathrm{DG\,chip}}, i_{\mathrm{L}} = 2\,\mathrm{A})$ in Fig. 2.28 on page 56

Conclusions Regarding the Parameterization of the Drain Capacitances

The proposed modeling can simulate the SJ MOSFET's terminal behavior with a relatively good accuracy. However, dependent on the applied $R_{\mathrm{G\,ext}}$ and the switched load current i_{L}, especially the simplified modeling of the drain source capacitance causes differences between simulations and measurements. *In all its particulars*, the terminal behavior of the DUT can only be simulated over a wide range of operating conditions if the drain source *and* the gate source voltage dependence of the drain source capacitance $C_{\mathrm{DS\,chip}}$ (and the drain gate capacitance $C_{\mathrm{DS\,chip}}$) are accurately modeled. On the basis of the determined capacitance characteristics in Fig. 2.29 on page 59 (and Fig. 2.28 on page 56), 2D look-up tables can not be generated for $C_{\mathrm{DS\,chip}}$ (and $C_{\mathrm{DG\,chip}}$) for the considered operating range of the SJ MOSFET. Thereto, further evaluable measurement data (without parasitic oscillations) and, hence, an optimized dynamic measurement setup would be necessary. Due to the involved effort, first, the (physical) cause of the gate source voltage dependency of $C_{\mathrm{DS\,chip}}$ should be analyzed for example by means of 3D device simulations. Such an analysis is beyond the scope and possibilities in this work. Thus, it is left for future works. Meanwhile, the proposed parameterization of $C_{\mathrm{DG\,chip}}$ and $C_{\mathrm{DS\,chip}}$ in **2.4.1.3** on page 55 et seq. is used for the stability analysis - despite the detected shortcomings.

4.2 Model Applicability for the Stability Analysis

The comparison of measured and simulated switching characteristics in section **4.1** demonstrates the performance of the proposed large-signal buck converter model and reveals the shortcomings of the proposed parameterization. The causes - in descending order of the assumed importance - for the differences between measurements and simulations are ...

- ... the simplified parameterization of $C_{\mathrm{DS\,chip}}$ of the MOSFET behavioral model, ...
- ... the simplified parameterization of $C_{\mathrm{DG\,chip}}$ of the MOSFET behavioral model, ...
- ... the simplified modeling of the gate driver circuit, ...
- ... the neglect of the mutual inductances L_{ij} with $L_{\mathrm{ij}} \neq L_{\mathrm{ij}} \cdot {}^{\mathrm{d}i_{\mathrm{j}}}/_{\mathrm{d}i_{\mathrm{i}}}$ in the calculation of the effective inductances of the single source connectors, and the neglect of the mutual inductances, which are not between the conductors' two conduction paths, in the calculation of the effective inductances of the double source connectors,[10] ...
- ... the simplified modeling of the DC voltage link, ...
- ... the usage of DC resistances in the calculation of the effective resistances according to equation (3.23) through (3.27) on page 92, and ...
- ... the simplified modeling of the load circuit.

[10] The effective inductances are defined in equation (3.28) through (3.31) on page 92.

Subsequently, the impact of the simplifications on the stability analysis is discussed:

The ***consideration of a drain source voltage and gate source voltage dependent drain capacitances*** $C_{\mathrm{DS\,chip}}$ and $C_{\mathrm{DG\,chip}}$ would improve the simulation results, and, thus, the significance of the stability analysis. The disregard of the gate source voltage dependence does not necessarily reduce the informational value of the stability analysis if the gate source voltage dependent codomain of the drain capacitances is regarded. An estimation of the capacitance's variation in the MOSFET's operating range is enabled with the dynamic drain source capacitance characteristics in Fig. 2.29 on page 59 and Fig. 2.28 on page 56.

The ***disregarded mutual inductances*** may cause differences between the measured and the simulated switching characteristics. However, the disregarded mutual inductances do not necessarily reduce the significance of the stability analysis. This is due to the fact that self and mutual inductances can be summarized in effective inductances (see (3.22) on page 91). The impact of the variation of the effective inductances during commutation on the stability can be detected if the possible range of the effective inductances is considered.

According to (3.13) and (3.14) on page 86 and (3.21) on page 91, the ***frequency dependent self and mutual resistances*** can also be summarized in effective resistances. The impact of the variation of the effective resistances during commutation on the stability can be detected if the possible range of the effective resistances is considered.[11]

The ***DC voltage link***, the ***load circuit*** and the ***gate driver circuit*** may influence the stability of the buck converter circuit during switching operation. Some parasitics of the DC voltage link and the gate driver circuit can for example be considered in the drain inductance $L_{\mathrm{D\,cir}}$ and the drain resistance $R_{\mathrm{D\,cir}}$, and the gate inductance $L_{\mathrm{G\,cir}}$ and the gate resistance $R_{\mathrm{g\,cir}}$ as well as the chip-external gate source capacitance $C_{\mathrm{GS\,ext}}$. The impact of these parasitics on the stability can also be analyzed by the variation of the corresponding circuit parameters. For the consideration of additional parasitics, the large-signal model of the buck converter must be adapted accordingly.

The stability analysis itself and the underlying equations are not affected by most of the mentioned simplifications. Often, a consideration would sorely result in a more accurate parameterization of the circuit model: In case of the drain capacitances, instead of 1D characteristics, 2D characteristics would be implemented, and neglected parasitics can - to a certain extent - be considered in the existing circuit elements. Therefore, the variation of the elements' parameterization enables conclusions on the impact of most of the neglected characteristics on the stability. The proposed modeling of the buck converter circuit is therewith suitable for the stability analysis - despite the detected shortcomings.

[11] In subsection **5.2.4** on page 146 et seq., it is shown that lower resistances do not always correlate with lower cosine phi's (higher damping ratios). Therewith, the usage of DC resistances is not necessarily a worst case consideration.

5 Stability of Commutation Cells with Power MOSFETs during Switching Operations

The stability analysis of commutation cells enables the prediction of oscillations (with temporarily increasing amplitudes) during switching operations. This is shown in this chapter using the example of the buck converter model in Fig. 3.13 on page 91. Section **5.1** explains why information about the dynamic behavior of non-linear systems is revealed by the analysis of their linearized operating points. In section **5.2**, the small-signal equivalent circuit model of the operating points of the buck converter model is derived, and the analysis of circuit's stability and its ability to oscillate is explained by means of eigenvalues. Subsequently, operating points are analyzed with respect to their stability. Thereby, the impact of different circuit parameterizations is investigated. In section **5.3**, the stability analysis of a simplified circuit model is presented. In section **5.4**, the results of the analyses are compared with simulations of switching operations, and the stability analysis is evaluated. Finally, the optimization of the damping in commutation cells is discussed in section **5.5**.

5.1 Analysis of a Non-Linear System

As shown in Fig. 5.1, the channel current i_{Ch} and the drain source voltage $v_{\mathrm{DS\,chip}}$ of a MOSFET during switching can be depicted as a locus curve in the MOSFET's output characteristics. Along the locus curves, the equivalent circuit elements $R_{\mathrm{DS\,chip}}$, $C_{\mathrm{DS\,chip}}$ and $C_{\mathrm{DG\,chip}}$ change their values according to their voltage dependency. The locus curves change with altered switching conditions and altered circuit parameters.

The explanations in the previous paragraph demonstrate that commutation cells in general and buck converters in specific are non-linear systems. The principle of linearity - i.e. the principle of amplification and superposition - can not be applied for non-linear systems. For analyzing non-linear systems, generally valid methods do not exist [Lutz 06]. For small excursions from a DC bias point, the behavior of the non-linear system can be approximated by the system's linearization in the operating point. Therewith, to some extend, information about a non-linear system can be obtained from a stability analysis of its operating points.

In the following sections, it is shown, that oscillations with temporarily increasing amplitudes during commutation in a buck converter topology can be predicted by means of a stability analysis of the small-signal equivalent circuit models of the buck converter's operating points - as long as the dwell time in areas with unstable operating points is large compared to the periods of the corresponding eigenfrequencies of the unstable operating points.

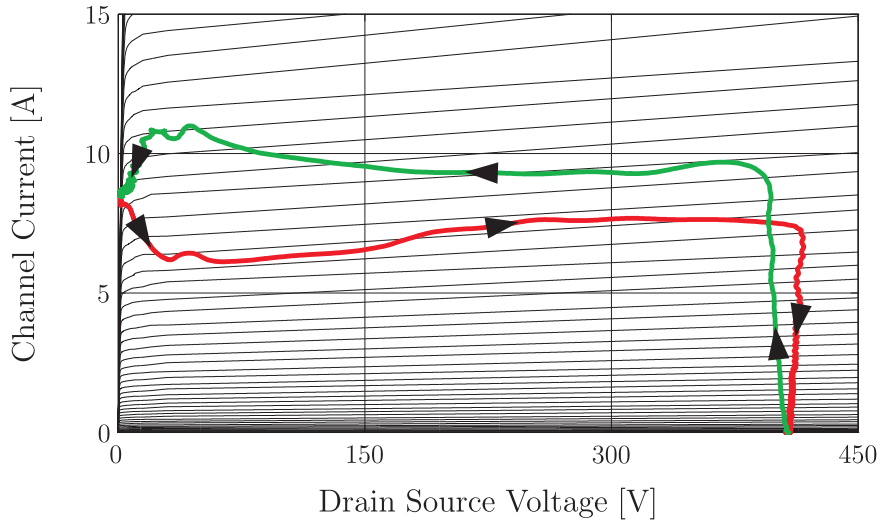


Figure 5.1: $I_{\mathrm{Ch}}(V_{\mathrm{DS\,chip}})$ locus curves of the simulated turn-off (red) and turn-on (green) in Fig. 4.1(c) and Fig. 4.1(d) on page 99

5.2 Analysis of a Buck Converter

5.2.1 Derivation of a Small-Signal Equivalent Circuit Model

Strictly speaking, in a buck converter topology, DC bias points exist only in the zero current state. During continuous current mode operation of the buck converter, the load current either increases or decreases. This results in increasing drain source voltages and decreasing blocking voltages of the diode while the MOSFET is turned on, as well as in decreasing forward voltages of the diode and increasing drain source voltages while the MOSFET is turned off. However, for short enough periods of time, the load current can be regarded as constant. Accordingly, static voltages across the devices can be assumed, and the term 'operating point' can be used. In this work, operating points of the buck converter model are defined by $V_{\mathrm{DS\,chip}}$ and $V_{\mathrm{GS\,chip}}$. For small-signals, DC voltage sources and high capacitances behave as shorts and DC current sources and high inductances behave as open circuits. The diode is represented as a short (as e.g. in [Severns 85] and [Fujihira 08]). The remaining circuit elements are represented by their linearization in the operating points. An operating point's channel current I_{Ch} is a function of $V_{\mathrm{DS\,chip}}$ and $V_{\mathrm{GS\,chip}}$. Accordingly, I_{Ch} can change due to an alteration of $V_{\mathrm{DS\,chip}}$ and $V_{\mathrm{GS\,chip}}$. Small derivations from I_{Ch} are given by

$$\begin{aligned}\Delta I_{\mathrm{Ch}} &= \left.\frac{\partial \mathbf{f}(V_{\mathrm{DS\,chip}}, V_{\mathrm{GS\,chip}})}{\partial V_{\mathrm{DS\,chip}}}\right|_{V_{\mathrm{GS\,chip}}} \cdot \Delta V_{\mathrm{DS\,chip}} \\ &+ \left.\frac{\partial \mathbf{f}(V_{\mathrm{DS\,chip}}, V_{\mathrm{GS\,chip}})}{\partial V_{\mathrm{GS\,chip}}}\right|_{V_{\mathrm{DS\,chip}}} \cdot \Delta V_{\mathrm{GS\,chip}} \\ &= g_{\mathrm{ds}}|_{V_{\mathrm{GS\,chip}}} \cdot \Delta V_{\mathrm{DS\,chip}} + g_{\mathrm{m}}|_{V_{\mathrm{DS\,chip}}} \cdot \Delta V_{\mathrm{GS\,chip}}\end{aligned} \tag{5.1}$$

with the output conductance g_{ds} and the gate transconductance g_{m} (cp. e.g. [Tille 04]). The MOSFET's absolute junction temperature T_{J} is considered constant in the operating points. The bias dependent small-signal capacitances are given by

$$C_{\mathrm{dg\,chip}}(V_{\mathrm{DS\,chip}}) = C_{\mathrm{DG\,chip}}(V_{\mathrm{DS\,chip}}) = C_{\mathrm{DG\,dyn}}(V_{\mathrm{DS\,chip}}) \text{ and} \tag{5.2}$$
$$C_{\mathrm{ds\,chip}}(V_{\mathrm{DS\,chip}}) = C_{\mathrm{DS\,chip}}(V_{\mathrm{DS\,chip}}) = C_{\mathrm{DS\,dyn}}(V_{\mathrm{DS\,chip}}). \tag{5.3}$$

The capacitances $C_{\mathrm{DG\,dyn}}(V_{\mathrm{DS\,chip}})$ and $C_{\mathrm{DS\,dyn}}(V_{\mathrm{DS\,chip}})$ are shown in Fig. 4.2 on page 100. $C_{\mathrm{GS\,chip}}$, the external capacitances $C_{\mathrm{DG\,ext}}$, $C_{\mathrm{DS\,ext}}$ and $C_{\mathrm{GS\,ext}}$, as well as the parasitic inductances and resistances of the large-signal model are constant in the regarded buck converter model. Thus, the corresponding small-signal equivalent circuit elements are given by

$$C_{\mathrm{gs\,chip}} = C_{\mathrm{GS\,chip}}, \tag{5.4}$$
$$C_{\mathrm{dg\,ext}} = C_{\mathrm{DG\,ext}},\ C_{\mathrm{ds\,ext}} = C_{\mathrm{DS\,ext}} \text{ and } C_{\mathrm{gs\,ext}} = C_{\mathrm{GS\,ext}}, \tag{5.5}$$
$$L_{\mathrm{d\,cir}} = L_{\mathrm{D\,cir}} + L_{\mathrm{Dio}},\ L_{\mathrm{g\,cir}} = L_{\mathrm{G\,cir}} \text{ and } L_{\mathrm{s\,cir}} = L_{\mathrm{S\,cir}}, \tag{5.6}$$
$$L_{\mathrm{d\,pac}} = L_{\mathrm{D\,pac}},\ L_{\mathrm{g\,pac}} = L_{\mathrm{G\,pac}} \text{ and } L_{\mathrm{s\,pac}} = L_{\mathrm{S\,pac}}, \tag{5.7}$$
$$R_{\mathrm{d\,cir}} = R_{\mathrm{D\,cir}} + R_{\mathrm{Dio}},\ R_{\mathrm{g\,cir}} = R_{\mathrm{G\,cir}} \text{ and } R_{\mathrm{s\,cir}} = R_{\mathrm{S\,cir}} \text{ as well as} \tag{5.8}$$
$$R_{\mathrm{d\,pac}} = R_{\mathrm{D\,pac}},\ R_{\mathrm{g\,pac}} = R_{\mathrm{G\,pac}} \text{ and } R_{\mathrm{s\,pac}} = R_{\mathrm{S\,pac}}. \tag{5.9}$$

The large-signal circuit elements in the previous equations correspond to (3.23) through (3.31) on page 92. The small-signal equivalent circuit model of the buck converter's operating points is shown in Fig. 5.2. $C_{\mathrm{dg\,chip}}$, $C_{\mathrm{ds\,chip}}$, g_{m} and g_{ds} depend on the operating point.

5.2.2 Stability Analysis with the Small-Signal Equivalent Circuit Model

The small-signal equivalent circuit model of the buck converter's operating points in Fig. 5.2 is described by the linear homogeneous differential state-space equation system

$$\dot{\vec{x}} = \boldsymbol{A} \cdot \vec{x} \tag{5.10}$$

with the state space vector

$$\vec{x} = \left[\Delta I_{\mathrm{D\,pac}},\ \Delta I_{\mathrm{G\,pac}},\ \Delta I_{\mathrm{D\,cir}},\ \Delta I_{\mathrm{G\,cir}},\ \Delta V_{\mathrm{DS\,chip}},\ \Delta V_{\mathrm{GS\,chip}},\ \Delta V_{\mathrm{DS\,ext}},\ \Delta V_{\mathrm{GS\,ext}}\right]^{\mathrm{T}}, \tag{5.11}$$

the time-derived state space vector

$$\dot{\vec{x}} = \left[\Delta \dot{I}_{\mathrm{D\,pac}},\ \Delta \dot{I}_{\mathrm{G\,pac}},\ \Delta \dot{I}_{\mathrm{D\,cir}},\ \Delta \dot{I}_{\mathrm{G\,cir}},\ \Delta \dot{V}_{\mathrm{DS\,chip}},\ \Delta \dot{V}_{\mathrm{GS\,chip}},\ \Delta \dot{V}_{\mathrm{DS\,ext}},\ \Delta \dot{V}_{\mathrm{GS\,ext}}\right]^{\mathrm{T}} \tag{5.12}$$

and the system matrix $\boldsymbol{A}$. The matrix elements a_{ij} are presented in Table 5.1 with

$$LL_{\mathrm{cir}} = L_{\mathrm{g\,cir}} \cdot L_{\mathrm{s\,cir}} + L_{\mathrm{d\,cir}} \cdot L_{\mathrm{g\,cir}} + L_{\mathrm{s\,cir}} \cdot L_{\mathrm{d\,cir}}, \tag{5.13}$$
$$LL_{\mathrm{pac}} = L_{\mathrm{g\,pac}} \cdot L_{\mathrm{s\,pac}} + L_{\mathrm{d\,pac}} \cdot L_{\mathrm{g\,pac}} + L_{\mathrm{s\,pac}} \cdot L_{\mathrm{d\,pac}}, \tag{5.14}$$
$$CC_{\mathrm{chip}} = C_{\mathrm{dg\,chip}} \cdot C_{\mathrm{ds\,chip}} + C_{\mathrm{gs\,chip}} \cdot C_{\mathrm{dg\,chip}} + C_{\mathrm{ds\,chip}} \cdot C_{\mathrm{gs\,chip}} \text{ and} \tag{5.15}$$

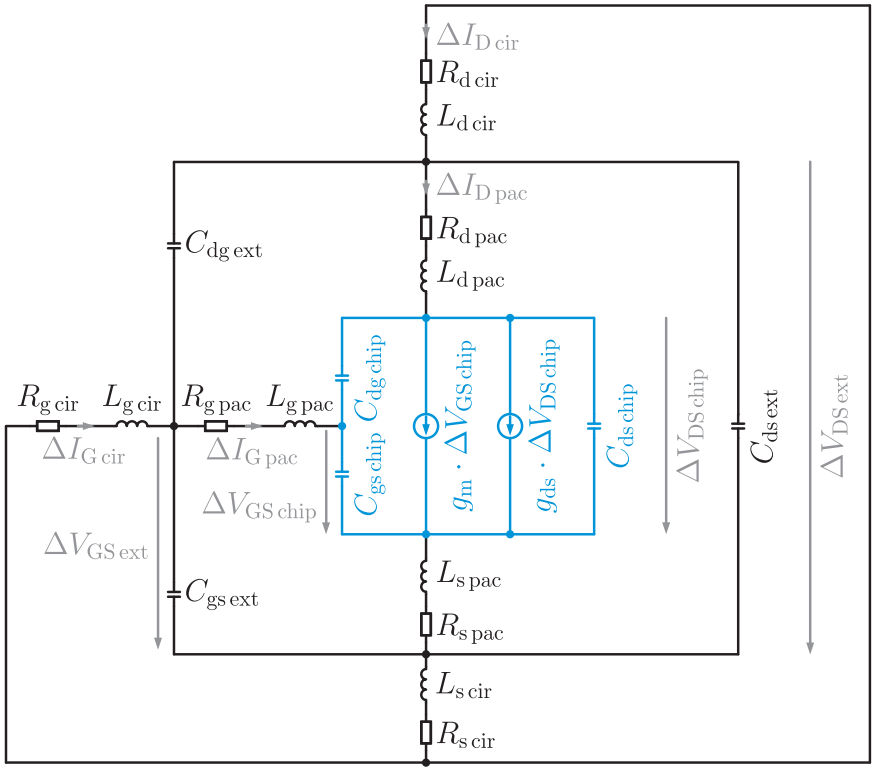


Figure 5.2: Small-signal equivalent circuit model of a buck converter topology's operating points on the basis of the buck converter model in Fig. 3.13 on page 91

$$CC_{\mathrm{ext}} = C_{\mathrm{dg\,ext}} \cdot C_{\mathrm{ds\,ext}} + C_{\mathrm{gs\,ext}} \cdot C_{\mathrm{dg\,ext}} + C_{\mathrm{ds\,ext}} \cdot C_{\mathrm{gs\,ext}}. \tag{5.16}$$

The determination of $\boldsymbol{A}$ is described in the appendix in section **B.1** on page 183 et seq..

The solution of the differential equation system represents the change of small derivations from the operating point over time. The operating point is stable, if

$$\lim_{t \to \infty} \vec{x} = \vec{0} \tag{5.17}$$

after *any* small excursion from the operating point. Else the operating point is unstable.

For the general solution of the linear differential equation system in (5.10), the solutions of the characteristic polynomial of the system matrix $\boldsymbol{A}$ are needed (see e.g. [Bronstein 08]). The characteristic polynomial of $\boldsymbol{A}$ is given by

$$|\boldsymbol{A} - \lambda \cdot \boldsymbol{I}| = 0. \tag{5.18}$$

The solutions are the eigenvalues λ_{i} of the system matrix $\boldsymbol{A}$. Since $\boldsymbol{A}$ is an 8×8 matrix, eight solutions of the characteristic polynomial exist. The eight solutions can only be determined numerically [Bronstein 08]. The unit of the eigenvalues is s^{-1}.

Table 5.1: Elements of the system matrix of the model in Fig. 5.2

a_{ij}	**Calculation of** a_{ij}	a_{ij}	**Calculation of** a_{ij}
$a_{1\,1}$	$L_{\mathrm{g\,pac}} \cdot R_{\mathrm{s\,pac}} - (L_{\mathrm{g\,pac}} + L_{\mathrm{s\,pac}}) \cdot R_{\mathrm{d\,pac}} / LL_{\mathrm{pac}}$	$a_{5\,1}$	$-C_{\mathrm{dg\,chip}} - C_{\mathrm{gs\,chip}} / CC_{\mathrm{chip}}$
$a_{1\,2}$	$L_{\mathrm{S\,pac}} \cdot R_{\mathrm{g\,pac}} - L_{\mathrm{G\,pac}} \cdot R_{\mathrm{s\,pac}} / LL_{\mathrm{pac}}$	$a_{5\,2}$	$-C_{\mathrm{dg\,chip}} / CC_{\mathrm{chip}}$
$a_{1\,3}$	0	$a_{5\,3}$	0
$a_{1\,4}$	0	$a_{5\,4}$	0
$a_{1\,5}$	$L_{\mathrm{g\,pac}} + L_{\mathrm{s\,pac}} / LL_{\mathrm{pac}}$	$a_{5\,5}$	$-(C_{\mathrm{dg\,chip}} + C_{\mathrm{gs\,chip}}) \cdot g_{\mathrm{ds}} / CC_{\mathrm{chip}}$
$a_{1\,6}$	$-L_{\mathrm{s\,pac}} / LL_{\mathrm{pac}}$	$a_{5\,6}$	$-(C_{\mathrm{dg\,chip}} + C_{\mathrm{gs\,chip}}) \cdot g_{\mathrm{m}} / CC_{\mathrm{chip}}$
$a_{1\,7}$	$-L_{\mathrm{g\,pac}} - L_{\mathrm{s\,pac}} / LL_{\mathrm{pac}}$	$a_{5\,7}$	0
$a_{1\,8}$	$L_{\mathrm{s\,pac}} / LL_{\mathrm{pac}}$	$a_{5\,8}$	0
$a_{2\,1}$	$L_{\mathrm{s\,pac}} \cdot R_{\mathrm{d\,pac}} - L_{\mathrm{d\,pac}} \cdot R_{\mathrm{s\,pac}} / LL_{\mathrm{pac}}$	$a_{6\,1}$	$-C_{\mathrm{dg\,chip}} / CC_{\mathrm{chip}}$
$a_{2\,2}$	$L_{\mathrm{d\,pac}} R_{\mathrm{s\,pac}} - (L_{\mathrm{d\,pac}} + L_{\mathrm{s\,pac}}) \cdot R_{\mathrm{g\,pac}} / LL_{\mathrm{pac}}$	$a_{6\,2}$	$-C_{\mathrm{dg\,chip}} - C_{\mathrm{ds\,chip}} / CC_{\mathrm{chip}}$
$a_{2\,3}$	0	$a_{6\,3}$	0
$a_{2\,4}$	0	$a_{6\,4}$	0
$a_{2\,5}$	$-L_{\mathrm{s\,pac}} / LL_{\mathrm{pac}}$	$a_{6\,5}$	$-C_{\mathrm{DG\,chip}} \cdot g_{\mathrm{ds}} / CC_{\mathrm{chip}}$
$a_{2\,6}$	$L_{\mathrm{d\,pac}} + L_{\mathrm{s\,pac}} / LL_{\mathrm{pac}}$	$a_{6\,6}$	$-C_{\mathrm{dg\,chip}} \cdot g_{\mathrm{m}} / CC_{\mathrm{chip}}$
$a_{2\,7}$	$L_{\mathrm{s\,pac}} / LL_{\mathrm{pac}}$	$a_{6\,7}$	0
$a_{2\,8}$	$-(L_{\mathrm{d\,pac}} + L_{\mathrm{s\,pac}}) / LL_{\mathrm{pac}}$	$a_{6\,8}$	0
$a_{3\,1}$	0	$a_{7\,1}$	$C_{\mathrm{dg\,ext}} + C_{\mathrm{gs\,ext}} / CC_{\mathrm{ext}}$
$a_{3\,2}$	0	$a_{7\,2}$	$C_{\mathrm{dg\,ext}} / CC_{\mathrm{ext}}$
$a_{3\,3}$	$L_{\mathrm{g\,cir}} \cdot R_{\mathrm{s\,cir}} - (L_{\mathrm{g\,cir}} + L_{\mathrm{s\,cir}}) \cdot R_{\mathrm{d\,cir}} / LL_{\mathrm{cir}}$	$a_{7\,3}$	$-C_{\mathrm{dg\,ext}} - C_{\mathrm{gs\,ext}} / CC_{\mathrm{ext}}$
$a_{3\,4}$	$L_{\mathrm{s\,cir}} \cdot R_{\mathrm{g\,cir}} - L_{\mathrm{g\,cir}} \cdot R_{\mathrm{s\,cir}} / LL_{\mathrm{cir}}$	$a_{7\,4}$	$-C_{\mathrm{dg\,ext}} / CC_{\mathrm{ext}}$
$a_{3\,5}$	0	$a_{7\,5}$	0
$a_{3\,6}$	0	$a_{7\,6}$	0
$a_{3\,7}$	$L_{\mathrm{g\,cir}} + L_{\mathrm{s\,cir}} / LL_{\mathrm{cir}}$	$a_{7\,7}$	0
$a_{3\,8}$	$-L_{\mathrm{s\,cir}} / LL_{\mathrm{cir}}$	$a_{7\,8}$	0
$a_{4\,1}$	0	$a_{8\,1}$	$C_{\mathrm{dg\,ext}} / CC_{\mathrm{ext}}$
$a_{4\,2}$	0	$a_{8\,2}$	$C_{\mathrm{dg\,ext}} + C_{\mathrm{ds\,ext}} / CC_{\mathrm{ext}}$
$a_{4\,3}$	$L_{\mathrm{s\,cir}} \cdot R_{\mathrm{d\,cir}} - L_{\mathrm{d\,cir}} \cdot R_{\mathrm{s\,cir}} / LL_{\mathrm{cir}}$	$a_{8\,3}$	$-C_{\mathrm{dg\,ext}} / CC_{\mathrm{ext}}$
$a_{4\,4}$	$L_{\mathrm{d\,cir}} \cdot R_{\mathrm{s\,cir}} - (L_{\mathrm{d\,cir}} + L_{\mathrm{s\,cir}}) \cdot R_{\mathrm{g\,cir}} / LL_{\mathrm{cir}}$	$a_{8\,4}$	$-C_{\mathrm{dg\,ext}} - C_{\mathrm{ds\,ext}} / CC_{\mathrm{ext}}$
$a_{4\,5}$	0	$a_{8\,5}$	0
$a_{4\,6}$	0	$a_{8\,6}$	0
$a_{4\,7}$	$-L_{\mathrm{s\,cir}} / LL_{\mathrm{cir}}$	$a_{8\,7}$	0
$a_{4\,8}$	$L_{\mathrm{d\,cir}} + L_{\mathrm{s\,cir}} / LL_{\mathrm{cir}}$	$a_{8\,8}$	0

Each *single* eigenvalue λ_i corresponds to a particular solution vector

$$\vec{x_\mathrm{i}} = [K_\mathrm{i1},\ K_\mathrm{i2},\ K_\mathrm{i3},\ K_\mathrm{i4},\ K_\mathrm{i5},\ K_\mathrm{i6},\ K_\mathrm{i7},\ K_\mathrm{i8}]^\mathrm{T} \cdot \mathrm{e}^{\lambda_\mathrm{i} \cdot t} \tag{5.19}$$

with the coefficients K_ik. The determination of coefficients is e.g. described in [Bronstein 08]. Only ratios of the coefficients K_ik can be determined. Therefore, for each single eigenvalue an arbitrary constant exists.

Each *multiple* eigenvalues λ_i corresponds also to a particular solution vector

$$\vec{x_\mathrm{i}} = [K_\mathrm{i1}(t),\ K_\mathrm{i2}(t),\ K_\mathrm{i3}(t),\ K_\mathrm{i4}(t),\ K_\mathrm{i5}(t),\ K_\mathrm{i6}(t),\ K_\mathrm{i7}(t),\ K_\mathrm{i8}(t)]^\mathrm{T} \cdot \mathrm{e}^{\lambda_\mathrm{i} \cdot t} \tag{5.20}$$

with the polynomials $K_\mathrm{ik}(t)$. The maximum degree of the polynomials is given by $m - 1$ with the multiplicity m. The determination of the coefficients in the polynomials $K_\mathrm{ik}(t)$ is e.g. described in [Bronstein 08]. Only ratios of the coefficients can be determined. Therefore, for each eigenvalue with the multiplicity m, m arbitrary constants exist.

Since the sum of particular solution vectors of the eigenvalues of the system matrix $\boldsymbol{A}$ contain eight arbitrary constants, the particular solution vectors are linear independent. Therefore, the general solution of the linear homogeneous differential equation system is given by the sum of all the particular solution vectors [Bronstein 08].

(5.19) and (5.20) show that information about the stability of the system is available *without* solving its differential equation system explicitly. The eigenvalues are in the exponential part of the solution of a differential equation system. Thus, they indicate if the system is stable or unstable, and if the system is able to oscillate or not. The system is stable if the real parts of *all* eigenvalues are smaller than zero. Complex eigenvalues of real linear differential equation systems with constant coefficients occur always as conjugate-complex eigenvalues (see e.g. [Bronstein 08]). With respect to Euler's formula

$$\mathrm{e}^{(\alpha + \mathrm{i} \cdot \beta) \cdot t} = \mathrm{e}^{\alpha \cdot t} \cdot \mathrm{e}^{\mathrm{i} \cdot \beta \cdot t} = \mathrm{e}^{\alpha \cdot t} \cdot (\cos(\beta \cdot t) + \mathrm{i} \cdot \sin(\beta \cdot t)), \tag{5.21}$$

the system is able to oscillate in case conjugate-complex eigenvalues $\lambda_\mathrm{i} = \alpha_\mathrm{i} + \mathrm{i} \cdot \beta_\mathrm{i}$ and $\overline{\lambda_\mathrm{i}} = \alpha_\mathrm{i} - \mathrm{i} \cdot \beta_\mathrm{i}$ occur. The particular solution vectors of conjugate-complex eigenvalues are also conjugate-complex. The two complex particular solution vectors can be represented by two real particular solution vectors, which are given by the real and the imaginary part of one of the conjugate-complex particular solution vectors (see e.g. [Goldhorn 07]).

Conclusions that can be drawn from the eigenvalues of a linear system are summarized in Table 5.2. After a single disturbance, oscillations in the linear system are characterized by the ***cosine phi*** and the ***eigenfrequencies*** of conjugate-complex eigenvalues:

(I) The ***cosine phi*** $\cos\varphi$ is a dimensionless measure which describes how oscillations in a system decay after a disturbance. The cosine phi of an eigenvalue λ_i is given by

$$\cos\varphi(\lambda_\mathrm{i}) = \Re(\lambda_\mathrm{i}) / \sqrt{\Re(\lambda_\mathrm{i})^2 + \Im(\lambda_\mathrm{i})^2} \tag{5.22}$$

with the imaginary part $\Im(\lambda_\mathrm{i})$ and the real part $\Re(\lambda_\mathrm{i})$ of λ_i. The more negative the cosine phi the fewer periods are needed for the decay of the oscillation (see Fig. 5.29 on page 168).

Table 5.2: Evaluation of the stability of a system by means of its eigenvalues

Eigenvalues $[\mathrm{s}^{-1}]$ $\lambda_\mathrm{i} = \alpha_\mathrm{i} + \mathrm{i} \cdot \beta_\mathrm{i}$	**Effect on state space variables (SSVs) after an excursion from the operating point (OP)**
$\max_\mathrm{i}\{\alpha_\mathrm{i} > 0\}$, $\beta_\mathrm{i} = 0$	SSVs are driven further away from the OP.
$\max_\mathrm{i}\{\alpha_\mathrm{i} < 0\}$, $\beta_\mathrm{i} = 0$	SSVs are driven back to the OP.
$\alpha_\mathrm{i} = 0$, $\beta_\mathrm{i} = 0$	SSVs remain in the position to which they were moved.
$\max_\mathrm{i}\{\alpha_\mathrm{i} > 0\}$, $\beta_\mathrm{i} \neq 0$	SSVs oscillate and are driven away from the OP.
$\max_\mathrm{i}\{\alpha_\mathrm{i} < 0\}$, $\beta_\mathrm{i} \neq 0$	SSVs oscillate and are driven back to the OP.
$\alpha_\mathrm{i} = 0$, $\beta_\mathrm{i} \neq 0$	SSVs oscillate around the position to which they were moved.

The cosine phi of a negative real eigenvalue is -1 . The cosine phi of an imaginary eigenvalue is 0 , and the cosine phi of a positive real eigenvalue is 1 . As summarized in Table 5.2, oscillations with increasing amplitudes occur for $\cos\varphi(\lambda_\mathrm{i}) > 0$. Oscillations with constant amplitudes occur for $\cos\varphi(\lambda_\mathrm{i}) = 0$. For $\cos\varphi(\lambda_\mathrm{i}) < 0$, the amplitudes decrease.

(II) A system is able to oscillate with its ***eigenfrequency*** f_0 after a single excitation. The eigenfrequency of an eigenvalue λ_i is given by

$$f_0(\lambda_\mathrm{i}) = |\Im(\lambda_\mathrm{i})| \,/ (2 \cdot \pi). \tag{5.23}$$

For the same cosine phi, oscillations with higher eigenfrequencies decline or increase faster than oscillations with smaller eigenfrequencies (see Fig. 5.29 on page 168).

5.2.3 Analysis of Operating Points of a Buck Converter Topology

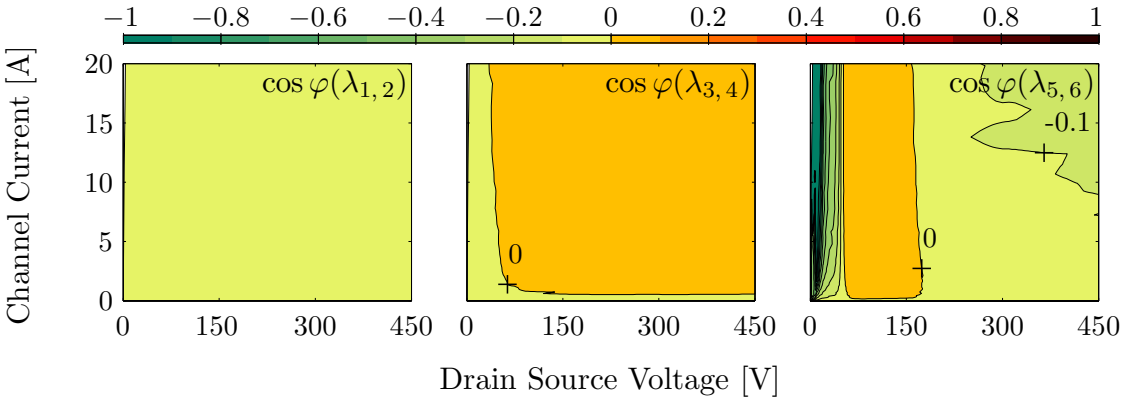
The eigenvalues of the operating points of a buck converter topology are determined in the operating range of the SJ MOSFET by means of the *MATLAB & Simulink* function 'eig'. Thereby, the values in Table 5.3 are used for the parameterization of the operating point independent circuit elements in Fig. 5.2. The operating point dependent circuit elements are based on the 25 °C output characteristics in Fig. 2.19 on page 38 and the 'dynamic' capacitances in Fig. 4.2 on page 100. Three conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$, as well as two negative real eigenvalues exist in the regarded operating range.

For the determined conjugate-complex eigenvalues, the cosine phi's and the eigenfrequencies are calculated according to (5.22) and (5.23). The results are shown as contour plots in Fig. 5.3. The contour plots display isolines of the cosine phi's and the eigenfrequencies in the considered operating range and can be interpreted as heights with respect to the $I_\mathrm{Ch}(V_\mathrm{DS\,chip})$ plane.[1] The contour plot of the cosine phi's of the conjugate-complex eigenvalue pair $\lambda_{1,2}$

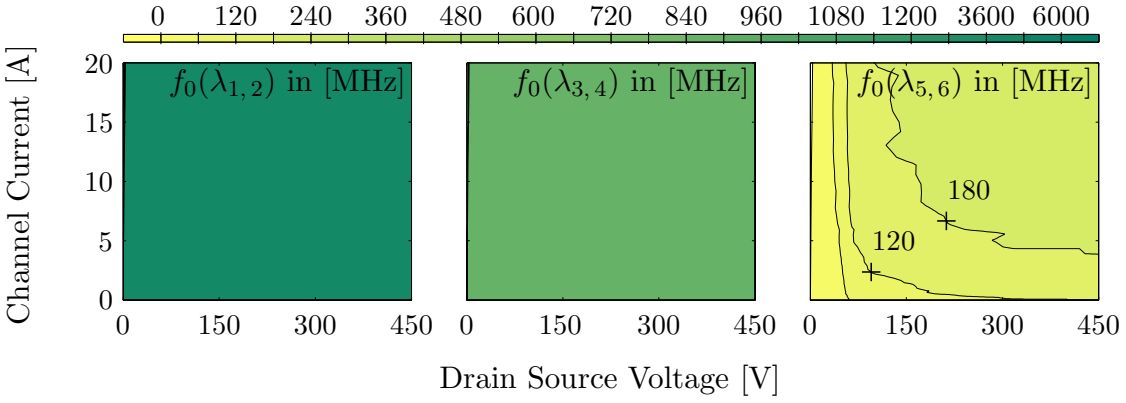
[1] An alternative plane for the contour plots is the $V_\mathrm{GS\,chip}(V_\mathrm{DS\,chip})$ plane, which is advantageous in MOSFET's subthreshold and linear region. The $I_\mathrm{Ch}(V_\mathrm{DS\,chip})$ plane refers to the MOSFET's output characteristics and, thus, supports the thinking in $i_\mathrm{Ch}(v_\mathrm{DS\,chip})$ locus curves through the output characteristics.

Table 5.3: Parameterization of operating point independent circuit elements of the buck converter's small-signal equivalent circuit model

Inductance	Value	Resistance	Value	Capacitance	Value
$L_{\mathrm{d\,pac}}$	13.96 nH	$R_{\mathrm{d\,pac}}$	0.47 mΩ	$C_{\mathrm{gs\,chip}}$	1.47 nF
$L_{\mathrm{d\,cir}}$	27.01 nH	$R_{\mathrm{d\,cir}}$	1.88 mΩ	$C_{\mathrm{gs\,ext}}$	0.14 pF
$L_{\mathrm{g\,pac}}$	2.09 nH	$R_{\mathrm{g\,pac}}$	2.16 Ω	$C_{\mathrm{dg\,ext}}$	5.49 pF
$L_{\mathrm{g\,cir}}$	2.09 nH	$R_{\mathrm{g\,cir}}$	10.01 Ω	$C_{\mathrm{ds\,ext}}$	2.74 pF
$L_{\mathrm{s\,pac}}$	2.50 nH	$R_{\mathrm{s\,pac}}$	0.41 mΩ		
$L_{\mathrm{s\,cir}}$	2.50 nH	$R_{\mathrm{s\,cir}}$	0.41 mΩ		



(a) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with unstable operating areas in orange



(b) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$

Figure 5.3: Results of the stability analysis of the buck converter topology's operating points in the MOSFET's operating range

in Fig. 5.3(a) has no unstable area in the regarded operating range. The orange areas in the contour plots of the cosine phi's of $\lambda_{3,4}$ and $\lambda_{5,6}$ represent unstable areas. Fig. 5.3(b) shows that the eigenfrequencies of the different eigenvalues differ significantly. The eigenvalue pair $\lambda_{5,6}$ has the lowest eigenfrequencies. Its eigenfrequencies depend on the considered operating point. The eigenfrequencies of the other eigenvalues are relatively constant in the regarded operating range. The eigenfrequencies of $\lambda_{3,4}$ is in the range of 890 MHz, and the eigenfrequencies of $\lambda_{1,2}$ is in a range of 4.5 GHz.[2] The simulated characteristics in Fig. 4.3 on page 102 et seq. are based on the same parameterization as the results of the stability analysis in Fig. 5.3. In Fig. A.1 on page 178 et seq., the simulated switching characteristics $i_{\mathrm{D\,cir}}$, $i_{\mathrm{G\,cir}}$, $v_{\mathrm{DS\,ext}}$ and $v_{\mathrm{GS\,ext}}$ are shown additionally to the characteristics i_{Ch}, $i_{\mathrm{D\,pac}}$, $i_{\mathrm{G\,pac}}$, $v_{\mathrm{DS\,chip}}$ and $v_{\mathrm{GS\,chip}}$. The frequencies of the oscillating part of the $v_{\mathrm{DS\,ext}}$ in Fig. A.1(a) and Fig. A.1(b) are determined by means of a FOURIER analysis. The results are depicted in Fig. A.2 on page 182. The determined frequencies correspond well with the eigenfrequencies in Fig. 5.3(b) and validate the application of the presented stability analysis for the analysis of switching operations. However, due to the unstable areas in the contour plots of $\cos\phi(\lambda_{3,4})$ and $\cos\phi(\lambda_{5,6})$, oscillations with increasing amplitudes are expected during commutation. If at all, oscillations with temporarily increasing amplitudes can only be detected in some gate current characteristics. This indicates that positive cosine phi's in the contour plots of the conjugate-complex eigenvalues are probably only a necessary condition for oscillations with temporarily increasing amplitudes. The way of the $i_{\mathrm{Ch}}(v_{\mathrm{DS\,chip}})$ locus curves through areas with positive cosine phi's and the dwell time in these areas determine if a sufficient condition for oscillations with temporarily increasing amplitudes during commutation is satisfied or not. Oscillations with temporarily increasing amplitudes can only be predicted by means of the presented stability analysis as long as the dwell time in unstable areas of the $I_{\mathrm{Ch}}(V_{\mathrm{DS\,chip}})$ plane is large compared to the periods of the eigenfrequencies of the corresponding subsidiary systems.

5.2.4 Impact of the Circuit Elements on the Stability

In this work, the focus of the stability analysis lays on the analysis of the determined necessary condition for oscillations with temporarily increasing amplitudes during turn-on and turn-off of power MOSFETs in commutation cells. Thus, the impact of the circuit elements on the cosine phi's of the conjugate-complex eigenvalues is considered in this subsection. The real eigenvalues are not shown. They remain negative for all presented parameterizations.

The switching characteristics in Fig. 4.3 on page 102 et seq. correspond to the results of the stability analysis in Fig. 5.3. They show no oscillations with temporarily increasing amplitudes even though unstable areas exist in the $I_{\mathrm{Ch}}(V_{\mathrm{DS\,chip}})$ plane. For the analysis of the circuit elements' impact on the stability, an initial parameterization is used, which shows oscillations with temporarily increasing amplitudes during switching operations. Thereto, the values of the chip-external inductances and capacitances in Table 5.3 are altered accordingly. The resulting initial parameterization of the operating point independent circuit

[2] According to the assumptions made in section **3.1** on page 65 et seq., frequencies above 1 GHz can not be analyzed with the behavioral model of the considered buck converter topology.

elements is shown in Table 5.4. The corresponding 'L_s' characteristics in Fig. 5.26(a) and Fig. 5.26(b) on page 157 et seq. show oscillations with temporarily increasing amplitudes. As in the previous subsection, the calculation of the initial operating point dependent circuit elements is based on the 25 °C output characteristics in Fig. 2.19 on page 38 and the 'dynamic' capacitances in Fig. 4.2 on page 100.

Subsequently, unless it is stated otherwise, the values of all circuit elements in Fig. 5.2 on page 114 are varied one ofter another while all other parameters are kept at their initial values. ***Interdependencies between the circuit parameters are not regarded.***[3] The most important results of the stability analysis are beforehand summarized. Therewith, the reader could only look at the following figures and skip their more detailed explanations.

Summary of the Most Important Results of the Stability Analysis

For the considered parameterizations of the circuit elements in Fig. 5.2 on page 114, the following list summarizes the results of the stability analysis. The conclusions assume: The smaller the area in the $I_{\mathrm{Ch}}(V_{\mathrm{DS\,chip}})$ plane with positive cosine phi's and the smaller the (positive) cosine phi's, the less unstable/the more stable is the buck converter.

- The power MOSFET's junction temperature T_{J} is not the most critical factor on the stability of the considered buck converter topology.
- The circuit is less unstable/more stable for smaller transconductances g_{m}.
- The circuit is less unstable/more stable for higher output conductances g_{ds}.
- A clear trend on the stability of the considered buck converter topology can not be observed for the increase or the decrease of the chip-internal capacitance $C_{\mathrm{ds\,chip}}$. For different initial parameters, the stability is often improved for lower $C_{\mathrm{ds\,chip}}$.
- The circuit is less unstable/more stable for higher chip-internal capacitances $C_{\mathrm{dg\,chip}}$.
- The circuit is more unstable/less stable for lower chip-internal capacitances $C_{\mathrm{gs\,chip}}$.
- A clear trend on the stability of the considered buck converter topology can not be observed for the increase or the decrease of the chip-external capacitances $C_{\mathrm{ds\,ext}}$.
- The chip-external capacitance $C_{\mathrm{dg\,ext}}$ is one of the most critical parameters on the stability. A clear trend on the stability of the considered buck converter topology can not be observed for the increase or the decrease of $C_{\mathrm{dg\,ext}}$.
- A clear trend on the stability of the considered buck converter topology can not be observed for the increase or the decrease of the chip-external capacitance $C_{\mathrm{gs\,ext}}$.
- A clear trend on the stability of the considered buck converter topology can not be observed for the increase or the decrease of the drain inductances $L_{\mathrm{d\,pac}}$ and $L_{\mathrm{d\,cir}}$.

[3] The variation of more than one circuit parameter may improve or degrade the stability much stronger, weaker or in a different direction than one would expect due to the separate variation of the circuit parameters. Compare e.g. Fig. 5.17 and Fig. 5.18 with Fig. 5.19 on page 143 et seq..

- The circuit is less unstable/more stable for lower gate inductances $L_{\mathrm{g\,pac}}$ and $L_{\mathrm{g\,cir}}$.
- The circuit is less unstable/more stable for lower source inductances $L_{\mathrm{s\,pac}}$ and $L_{\mathrm{s\,cir}}$.
- The impact of the drain resistances $R_{\mathrm{d\,pac}}$ and $R_{\mathrm{d\,cir}}$, and the source resistances $R_{\mathrm{s\,pac}}$ and $R_{\mathrm{s\,cir}}$ on the stability of the considered buck converter is insignificant.
- The circuit is more unstable/less stable for lower gate resistances $R_{\mathrm{g\,pac}}$ and $R_{\mathrm{g\,cir}}$.

In general, the analysis of the circuit elements' impact on the stability shows ...

- ... that the stability of commutation cells can be optimized by altered PCB, package and semiconductor chip designs.
- ... that the variation of some parameters results in increased cosine phi's of at least one conjugate-complex eigenvalue pair and decreased cosine phi's of at least one other conjugate-complex eigenvalue pair in parts of the regarded operating range.
- ... that the increase of the stability is a complex optimization problem - especially for boundary conditions like efficiency and power density.
- ... that the optimization of the inductances and resistances of interconnections, which are close to the semiconductor chip, is sometimes more effective than the optimization of inductances and resistances, which are further away from the semiconductor chip.
- ... that the ongoing trend towards higher current densities will probably further increase the significance of stability analysis of commutation cells.
- ... that the measurement of voltage and current characteristics of switching operations influences the stability because parasitic circuit elements are additionally implemented in the circuit for the measurement.
- ... that all capacitances and inductances and most resistances and conductances of the small-signal equivalent circuit model in Fig. 5.2 on page 114 can influence the cosine phi's of all conjugate-complex eigenvalues. Thus, the analysis of parasitic oscillations with temporarily increasing amplitudes by means of oscillating meshes within the circuit might be insufficient.[4]

[4] Resonant circuits (meshes) in commutation cells with power MOSFETs are for example shown in [Inf 11].

Impact of the MOSFET's Junction Temperature

The contour plots of the cosine phi's of the conjugate-complex eigenvalues for different junction temperatures T_J are shown in Fig. 5.4. The corresponding contour plots of the eigenfrequencies are shown in Fig. C.1 on page 191. In Fig. 5.4(a), the contour plots of the cosine phi's of the initial parameterization are depicted. Fig. 5.4(b) shows the contour plots of the cosine phi's of the parameterization with the 125 °C output characteristics in Fig. 2.19(b) on page 38. The different output characteristics, have an impact on both the MOSFET's transconductance and the MOSFET's conductance characteristic.[5]

Compared to the corresponding contour plot in Fig. 5.4(a), the increased junction temperature results in increase cosine phi's of $\lambda_{5,6}$ in the MOSFET's saturation region. The contour plot of $\cos\varphi(\lambda_{1,2})$ in Fig. 5.4(b) has decreased cosine phi's in the MOSFET's saturation region in comparison to the corresponding contour plot in Fig. 5.4(a). The contour plot of $\cos\varphi(\lambda_{3,4})$ is hardly affected by the alteration of the junction temperature.

According to Fig. 5.4, the cosine phi's are little affected by T_J. Due to an increased T_J, a significant alteration of the oscillations during switching operations is thus not expected for the regarded parameterizations. The junction temperature of a power MOSFET is hence not the most critical factor on the stability of the commutation cell.

Impact of the MOSFET's Transconductance

The contour plots of the cosine phi's of the conjugate-complex eigenvalues for different transconductance characteristics $g_\mathrm{m}(V_{\mathrm{DS\,chip}}, V_{\mathrm{GS\,chip}})$ are shown in Fig. 5.5. The corresponding contour plots of the eigenfrequencies are shown in Fig. C.2 on page 192. In Fig. 5.5(b), the contour plots of the cosine phi's of the initial parameterization are depicted. Fig. 5.5(a) and Fig. 5.5(c) show the contour plots of the cosine phi's of the parameterizations with the fifth part and the fivefold of the initial transconductance characteristic.

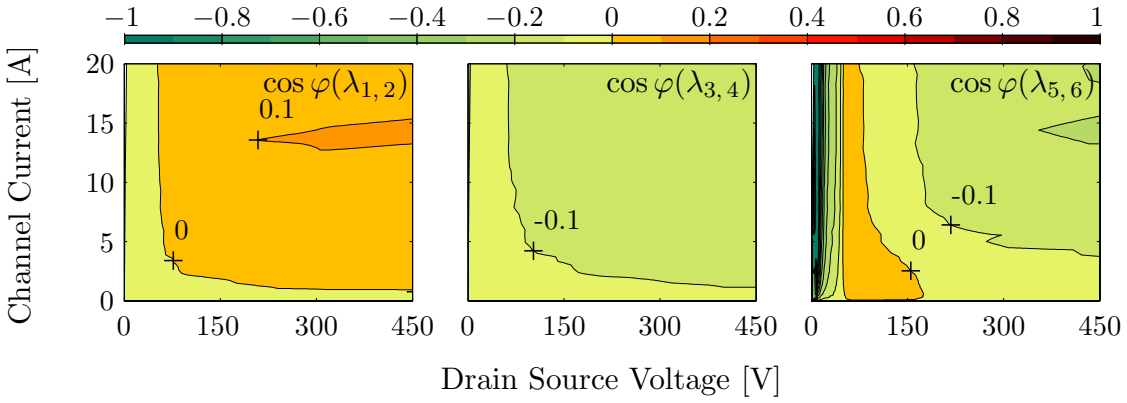
In comparison to the corresponding contour plot in Fig. 5.5(b), the areas with positive cosine phi's in the contour plot of $\cos\varphi(\lambda_{1,2})$ are reduced and the cosine phi's in the contour plots of $\cos\varphi(\lambda_{3,4})$ and $\cos\varphi(\lambda_{5,6})$ are increased in the MOSFET's saturation region in Fig. 5.5(a). Compared to the corresponding contour plot in Fig. 5.5(b), the increase of the transconductance leads to an increased unstable operating area in the contour plot of $\cos\varphi(\lambda_{1,2})$ in Fig. 5.5(c). The contour plots of $\cos\varphi(\lambda_{3,4})$ and $\cos\varphi(\lambda_{5,6})$ in Fig. 5.5(c) show decreased cosine phi's compared to the corresponding plots in Fig. 5.5(b).

According to Fig. 5.5, the cosine phi's are significantly influenced by the MOSFET's transconductance characteristic. The increase of the $g_\mathrm{m}(V_{\mathrm{DS\,chip}}, V_{\mathrm{GS\,chip}})$ results in an increased unstable area in the transistor's operating range. Compared to the initial parameterization, higher oscillation amplitudes are therefore expected during switching operations for the increased transconductance characteristic. The higher the current density in a power MOSFET, the more unstable/the less stable is the commutation cell.

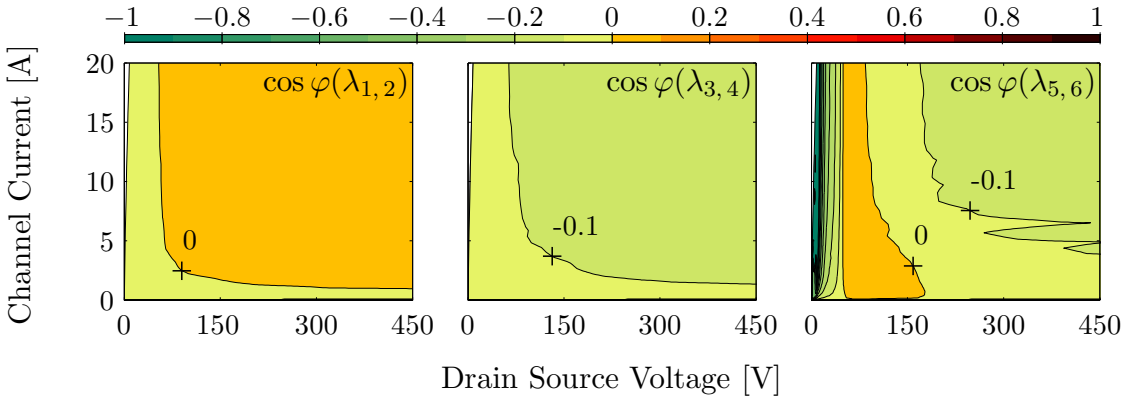
[5] See Fig. 2.17 on page 35, and compare Fig. 2.14(a) with Fig. 2.14(b) on page 31 and Fig. 2.19(a) with Fig. 2.19(b) on page 38.

Table 5.4: Initial parameterization of operating point independent circuit elements of the buck converter's small-signal equivalent circuit model in Fig. 5.2 on page 114

Inductance	Value	Resistance	Value	Capacitance	Value
$L_{\mathrm{d\,pac}}$	2.0 nH	$R_{\mathrm{d\,pac}}$	0.47 mΩ	$C_{\mathrm{gs\,chip}}$	1.47 nF
$L_{\mathrm{d\,cir}}$	35.0 nH	$R_{\mathrm{d\,cir}}$	1.88 mΩ	$C_{\mathrm{gs\,ext}}$	15.00 pF
$L_{\mathrm{g\,pac}}$	4.7 nH	$R_{\mathrm{g\,pac}}$	2.16 Ω	$C_{\mathrm{dg\,ext}}$	5.00 pF
$L_{\mathrm{g\,cir}}$	6.0 nH	$R_{\mathrm{g\,cir}}$	10.01 Ω	$C_{\mathrm{ds\,ext}}$	15.00 pF
$L_{\mathrm{s\,pac}}$	4.1 nH	$R_{\mathrm{s\,pac}}$	0.41 mΩ		
$L_{\mathrm{s\,cir}}$	3.0 nH	$R_{\mathrm{s\,cir}}$	0.41 mΩ		

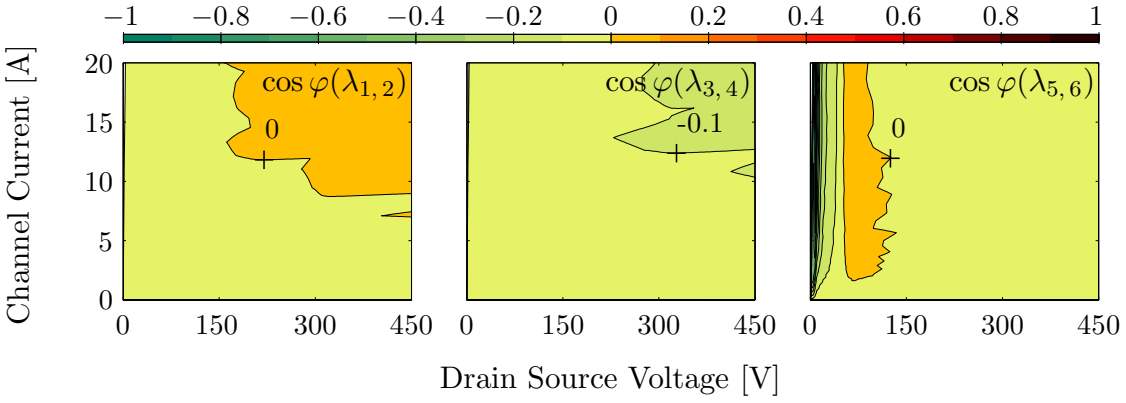


(a) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ of the initial parameterization with unstable areas in orange

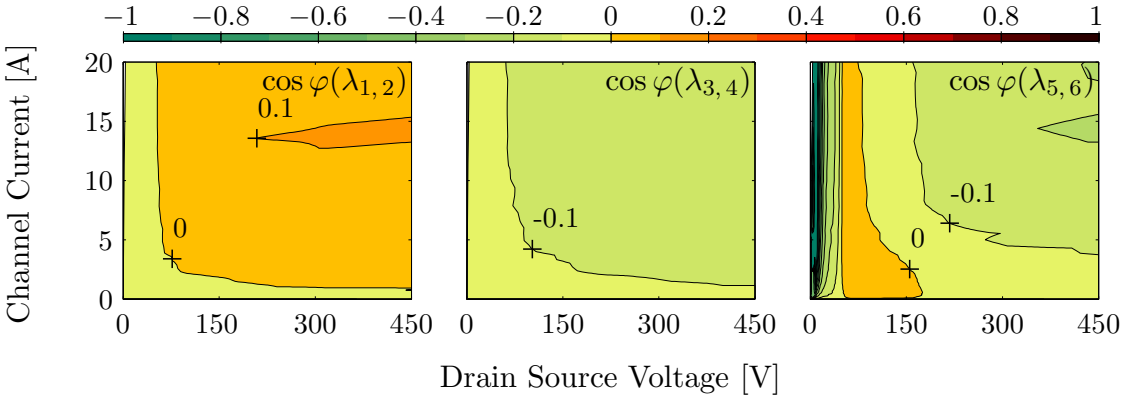


(b) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $\vartheta_{\mathrm{J}} = 125\,^{\circ}\mathrm{C}$ with unstable areas in orange

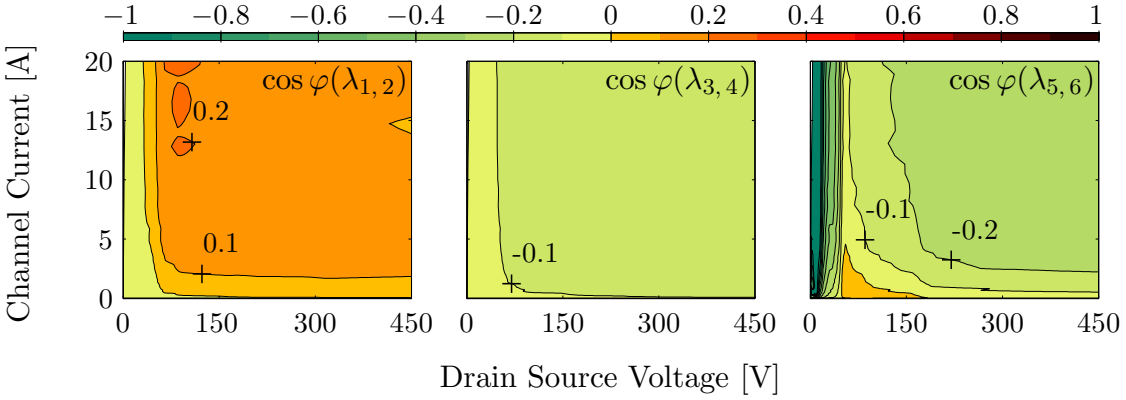
Figure 5.4: Impact of the MOSFET's junction temperature T_{J} on the cosine phi's of the conjugate-complex eigenvalues of a buck converter topology's operating points in the MOSFET's operating range



(a) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $0.2 \cdot g_{\mathrm{m}}(V_{\mathrm{DS\,chip}}, V_{\mathrm{GS\,chip}})$ with unstable areas in orange



(b) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ of the initial parameterization with unstable areas in orange



(c) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $5 \cdot g_{\mathrm{m}}(V_{\mathrm{DS\,chip}}, V_{\mathrm{GS\,chip}})$ with unstable areas in orange

Figure 5.5: Impact of the MOSFET's transconductance characteristic $g_{\mathrm{m}}(V_{\mathrm{DS\,chip}}, V_{\mathrm{GS\,chip}})$ on the cosine phi's of the conjugate-complex eigenvalues of a buck converter topology's operating points in the MOSFET's operating range

Impact of the MOSFET's Output Conductance

The contour plots of the cosine phi's of the conjugate-complex eigenvalues for different output conductance characteristics $g_{\mathrm{ds}}(V_{\mathrm{DS\,chip}}, V_{\mathrm{GS\,chip}})$ are shown in Fig. 5.6. The corresponding contour plots of the eigenfrequencies are shown in Fig. C.3 on page 193. In Fig. 5.6(b), the contour plots of the cosine phi's of the initial parameterization are depicted. Fig. 5.6(a) and Fig. 5.6(c) show the contour plots of the cosine phi's of the parameterizations with the fifth part and the fivefold of the initial output conductance $g_{\mathrm{ds}}(V_{\mathrm{DS\,chip}}, V_{\mathrm{GS\,chip}})$.

Compared to the contour plots in Fig. 5.6(b), the cosine phi's in the contour plots of $\cos\phi(\lambda_{1,2})$ and $\cos\phi(\lambda_{5,6})$ are reduced in Fig. 5.6(c). In comparison to the corresponding contour plots in Fig. 5.6(b), the decrease of the conductance leads to increased cosine phi's in the contour plots of $\cos\phi(\lambda_{1,2})$ and $\cos\phi(\lambda_{5,6})$ in Fig. 5.5(a). The contour plot of $\cos\phi(\lambda_{3,4})$ is not or hardly affected by the alteration of the output conductance.

According to Fig. 5.6, the cosine phi's increase with lower conductance values and vice versa. Compared to the initial parameterization, lower oscillation amplitudes are therefore expected during switching for the increased transconductance characteristic. The commutation cell is hence less unstable/the more stable for higher output conductance values.

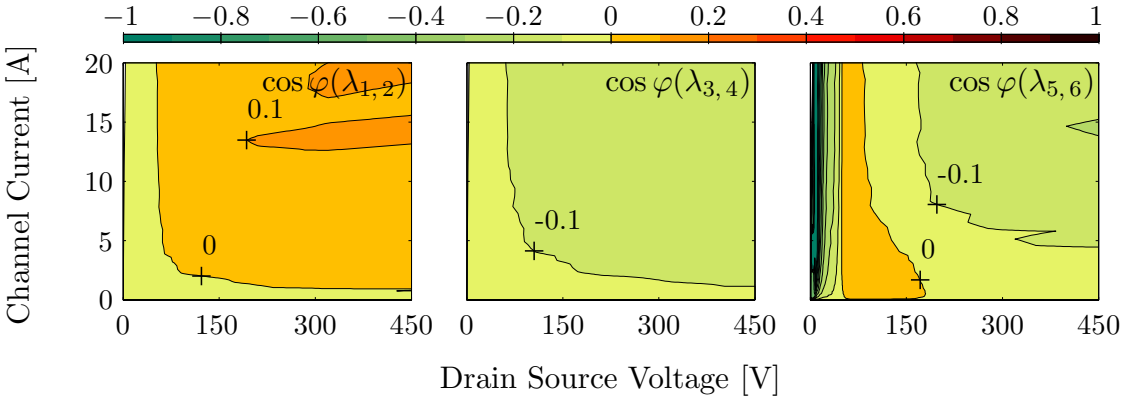
Impact of the MOSFET's Drain Source Capacitance Characteristic

The contour plots of the cosine phi's of the conjugate-complex eigenvalues for different drain source capacitance characteristics $C_{\mathrm{ds\,chip}}(V_{\mathrm{DS\,chip}})$ are shown in Fig. 5.7. The corresponding contour plots of the eigenfrequencies are shown in Fig. C.4 on page 194. In Fig. 5.7(b), the contour plots of the cosine phi's of the initial parameterization are depicted. Fig. 5.7(a) and Fig. 5.7(c) show the contour plots of the cosine phi's of the parameterizations with the fifth part and the fivefold of the initial drain source capacitance characteristic.

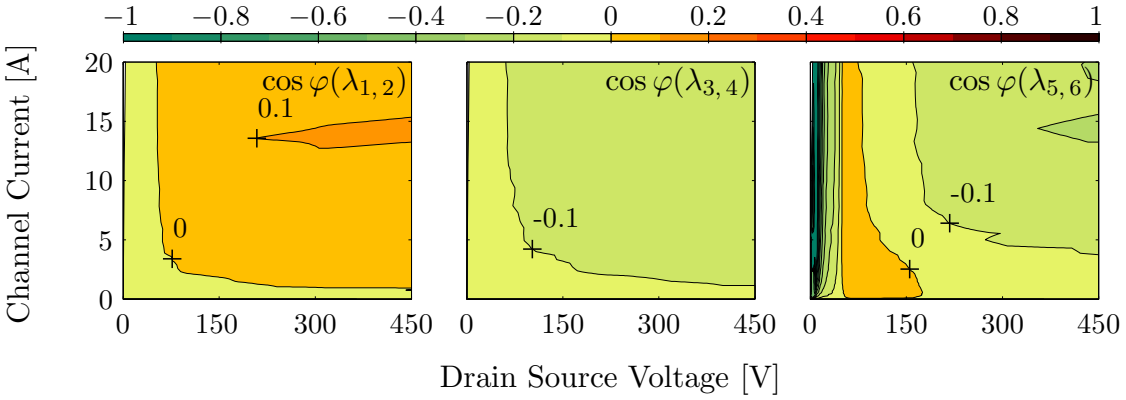
Compared to the contour plots in Fig. 5.7(b), the cosine phi's in the contour plots of $\cos\phi(\lambda_{3,4})$ and $\cos\phi(\lambda_{5,6})$ are reduced in Fig. 5.7(a) and increased in Fig. 5.7(c). In comparison to the corresponding contour plot in Fig. 5.7(b), the increase of $C_{\mathrm{ds\,chip}}(V_{\mathrm{DS\,chip}})$ results in a reduction of the unstable area in the contour plot of $\cos\phi(\lambda_{1,2})$ in Fig. 5.7(c). Compared to the corresponding contour plot in Fig. 5.7(b), the cosine phi's of the contour plot $\cos\phi(\lambda_{1,2})$ are increased in Fig. 5.7(a).

According to Fig. 5.7, the cosine phi's are significantly influenced by the MOSFET's drain source capacitance characteristic.[6] Based on the results in Fig. 5.7, an optimization approach of $C_{\mathrm{ds\,chip}}(V_{\mathrm{DS\,chip}})$ can not be made for the regarded initial parameterization. In case the parameters in Table 5.3 on page 118 are used instead of the parameters in Table 5.4 on page 123, the same variation of $C_{\mathrm{ds\,chip}}(V_{\mathrm{DS\,chip}})$ shows that the reduced $C_{\mathrm{ds\,chip}}(V_{\mathrm{DS\,chip}})$ characteristic improves the stability of the commutation cell significantly.

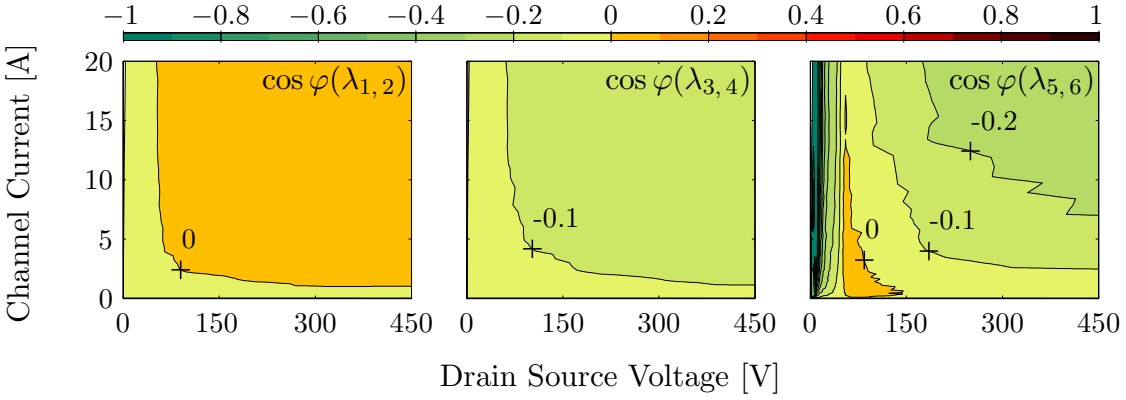
[6] With respect to the $C_{\mathrm{ds\,chip}}$ characteristics in Fig. 2.29 on page 59, the $V_{\mathrm{GS\,chip}}$ dependence of $C_{\mathrm{ds\,chip}}$ should be further analyzed for the stability analysis.



(a) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $0.2 \cdot g_{\mathrm{ds}}(V_{\mathrm{DS\,chip}}, V_{\mathrm{GS\,chip}})$ with unstable areas in orange

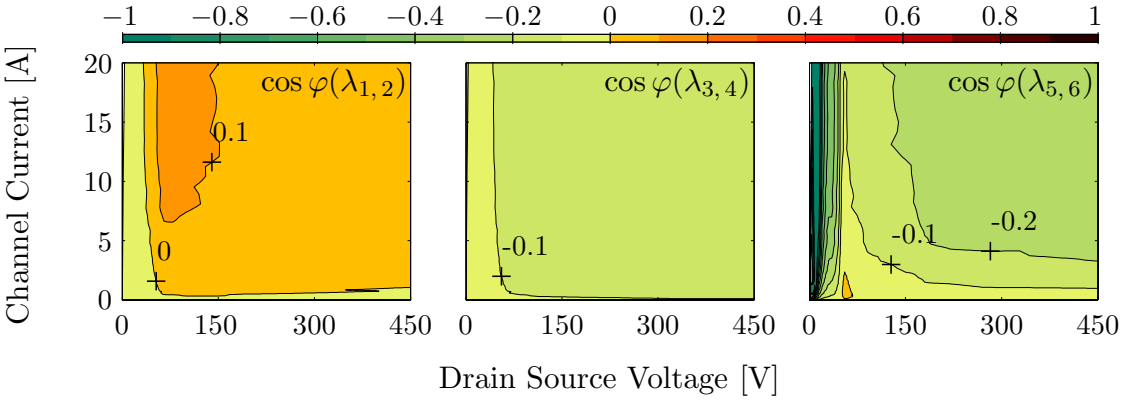


(b) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ of the initial parameterization with unstable areas in orange

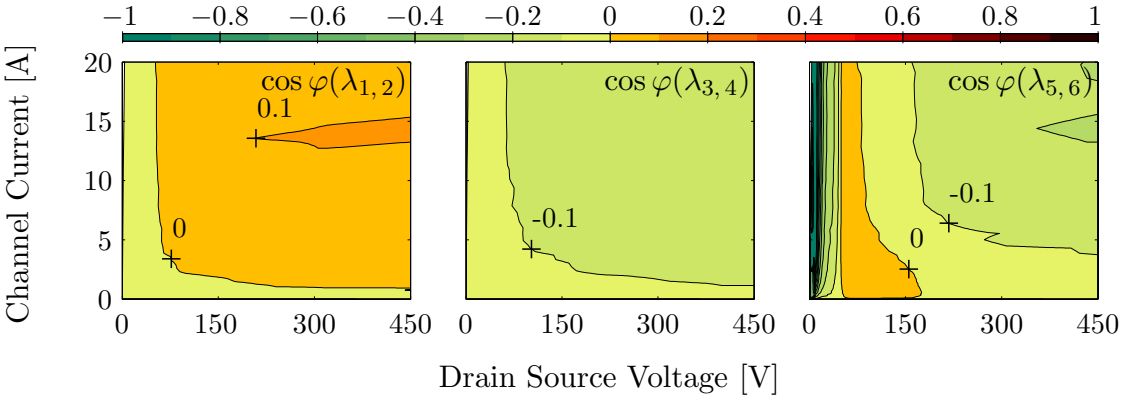


(c) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $5 \cdot g_{\mathrm{ds}}(V_{\mathrm{DS\,chip}}, V_{\mathrm{GS\,chip}})$ with unstable areas in orange

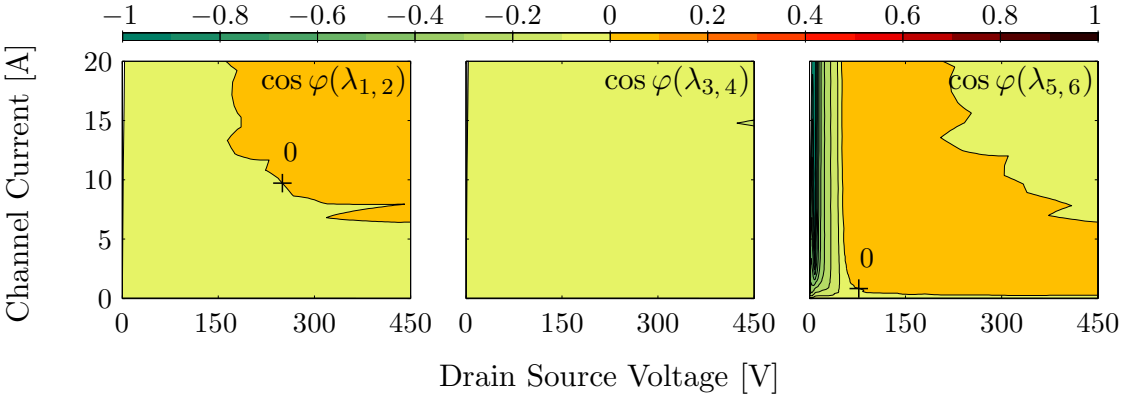
Figure 5.6: Impact of the MOSFET's conductance characteristic $g_{\mathrm{ds}}(V_{\mathrm{DS\,chip}}, V_{\mathrm{GS\,chip}})$ on the cosine phi's of the conjugate-complex eigenvalues of a buck converter topology's operating points in the MOSFET's operating range



(a) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $0.2 \cdot C_{\mathrm{ds\,chip}}(V_{\mathrm{DS\,chip}})$ with unstable areas in orange



(b) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ of the initial parameterization with unstable areas in orange



(c) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $5 \cdot C_{\mathrm{ds\,chip}}(V_{\mathrm{DS\,chip}})$ with unstable areas in orange

Figure 5.7: Impact of the drain source capacitance characteristic $C_{\mathrm{ds\,chip}}(V_{\mathrm{DS\,chip}})$ on the cosine phi's of the conjugate-complex eigenvalues of a buck converter topology's operating points in the MOSFET's operating range

Impact of the MOSFET's Drain Gate Capacitance Characteristic

The contour plots of the cosine phi's of the conjugate-complex eigenvalues for different drain gate capacitance characteristics $C_{\mathrm{dg\,chip}}(V_{\mathrm{DS\,chip}})$ are shown in Fig. 5.8. The corresponding contour plots of the eigenfrequencies are shown in Fig. C.5 on page 195. In Fig. 5.8(b), the contour plots of the cosine phi's of the initial parameterization are depicted. Fig. 5.8(a) and Fig. 5.8(c) show the contour plots of the cosine phi's of the parameterizations with the fifth part and the fivefold of the initial drain gate capacitance characteristic.

In Fig. 5.8(c), no areas with a positive cosine phi exist in the contour plot of $\cos\phi(\lambda_{5,6})$. Compared to the corresponding contour plot in Fig. 5.8(b), the area with a positive cosine phi is reduced in the contour plot of $\cos\phi(\lambda_{1,2})$ in Fig. 5.8(c). In the contour plots of $\cos\phi(\lambda_{1,2})$ and $\cos\phi(\lambda_{5,6})$ in Fig. 5.8(a), the cosine phi's have increased compared to the corresponding contour plots in Fig. 5.8(b). The contour plots of $\cos\phi(\lambda_{3,4})$ are not or hardly affected by the alteration of $C_{\mathrm{dg\,chip}}(V_{\mathrm{DS\,chip}})$.

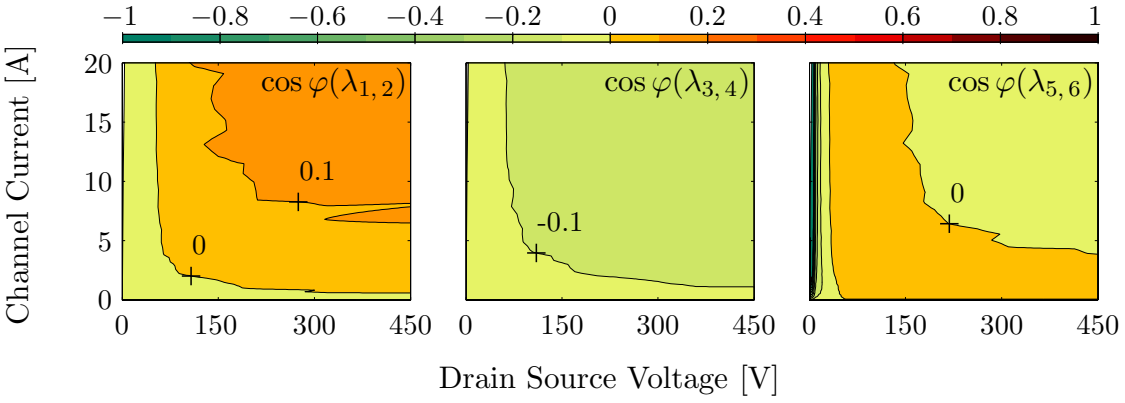
According to Fig. 5.8, the unstable areas increase with a lower $C_{\mathrm{dg\,chip}}(V_{\mathrm{DS\,chip}})$. Compared to the initial parameterization, higher oscillation amplitudes are therefore expected during switching for the decreased $C_{\mathrm{dg\,chip}}(V_{\mathrm{DS\,chip}})$ characteristic. The higher the chip-internal feedback capacitance, the less unstable/the more stable is the commutation cell. However, the MOSFET's switching losses increase with higher $C_{\mathrm{dg\,chip}}(V_{\mathrm{DS\,chip}})$.

Impact of the MOSFET's Gate Source Capacitance Characteristic

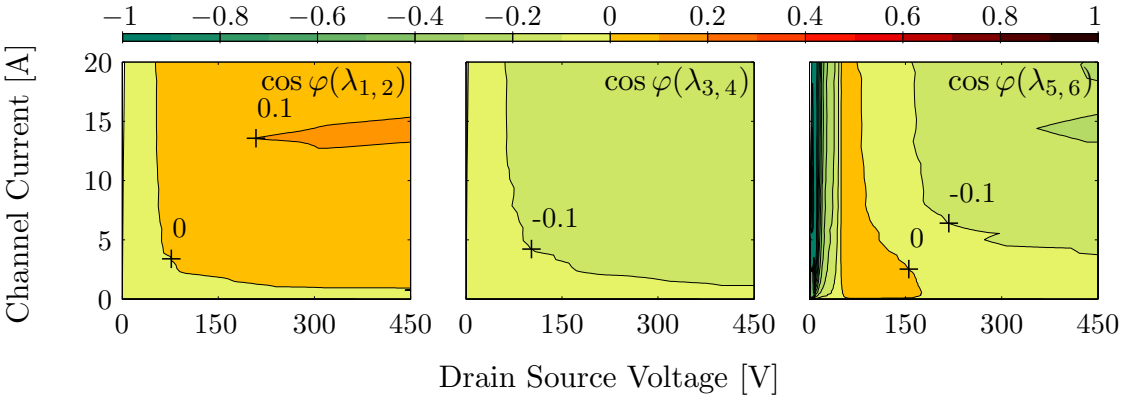
The contour plots of the cosine phi's of the conjugate-complex eigenvalues for different gate source capacitances $C_{\mathrm{gs\,chip}}$ are shown in Fig. 5.9. The corresponding contour plots of the eigenfrequencies are shown in Fig. C.6 on page 196. In Fig. 5.9(b), the contour plots of the cosine phi's of the initial parameterization are depicted. Fig. 5.9(a) and Fig. 5.9(c) show the contour plots of the cosine phi's of the parameterizations with the fifth part and the fivefold of the initial gate source capacitance.

In comparison to the corresponding contour plots in Fig. 5.9(b), the increase of $C_{\mathrm{gs\,chip}}$ results a reduction of the areas with positive cosine phi's in the contour plot of $\cos\phi(\lambda_{1,2})$ in Fig. 5.9(c). Compared to the corresponding plots in Fig. 5.9(b), the cosine phi's in the contour plots of $\cos\phi(\lambda_{3,4})$ and $\cos\phi(\lambda_{5,6})$ are mainly increased in Fig. 5.9(c). In Fig. 5.9(a), compared to the corresponding plots in Fig. 5.9(b), the cosine phi's of $\lambda_{3,4}$ and $\lambda_{5,6}$ are decreased, but the cosine phi's in the contour plot $\cos\phi(\lambda_{1,2})$ are increased.

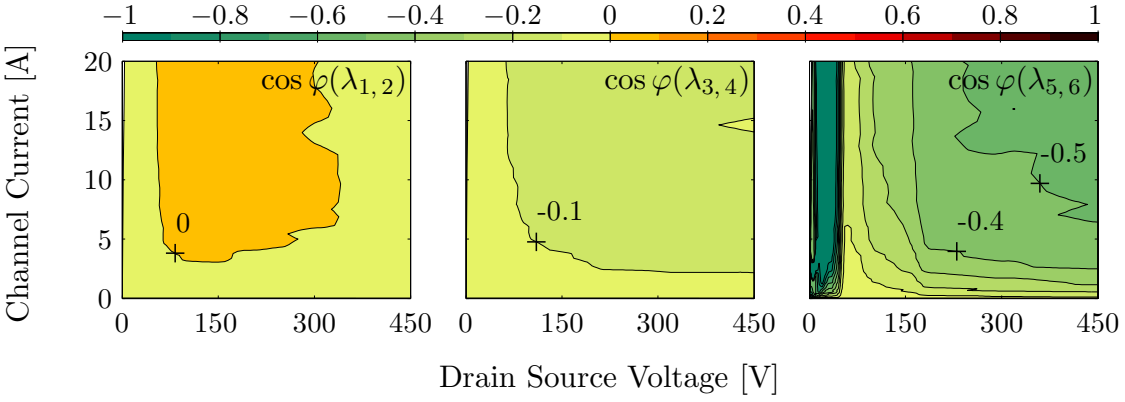
According to Fig. 5.9, the cosine phi's are significantly influenced by the MOSFET's gate source capacitance. For the regarded parameterizations, an increase of $C_{\mathrm{gs\,chip}}$ seems to be advantageous for the stability. Compared to the initial parameterization, reduced oscillations are therefore expected during switching for the increased $C_{\mathrm{gs\,chip}}$. The lower $C_{\mathrm{gs\,chip}}$, the more unstable/the less unstable is the commutation cell. However, for an unaltered driver configuration, higher $C_{\mathrm{gs\,chip}}$ increase the switching times.



(a) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $0.2 \cdot C_{\mathrm{dg\,chip}}(V_{\mathrm{DS\,chip}})$ with unstable areas in orange

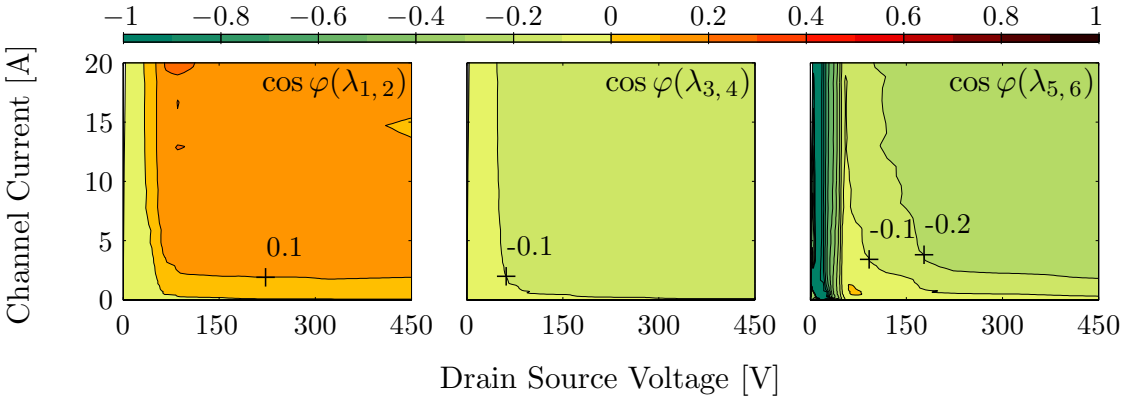


(b) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ of the initial parameterization with unstable areas in orange

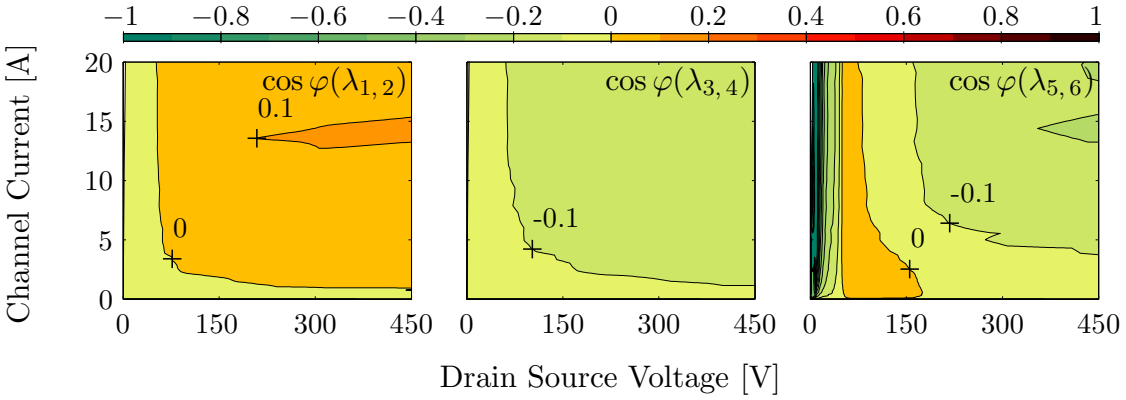


(c) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $5 \cdot C_{\mathrm{dg\,chip}}(V_{\mathrm{DS\,chip}})$ with unstable areas in orange

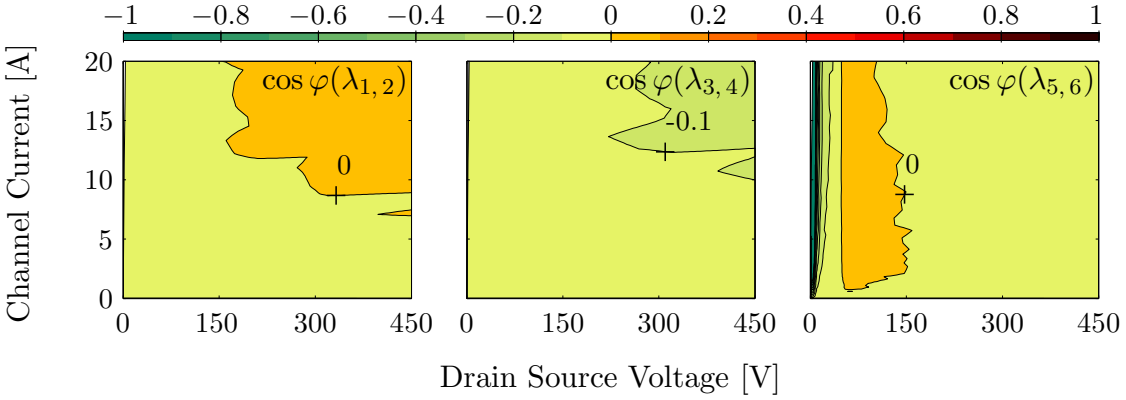
Figure 5.8: Impact of the MOSFET's drain gate capacitance characteristic $C_{\mathrm{dg\,chip}}(V_{\mathrm{DS\,chip}})$ on the cosine phi's of the conjugate-complex eigenvalues of a buck converter topology's operating points in the MOSFET's operating range



(a) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $0.2 \cdot C_{\text{gs chip}} = 0.294\,\text{nF}$ with unstable areas in orange



(b) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ of the initial parameterization with unstable areas in orange



(c) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $5 \cdot C_{\text{gs chip}} = 7.35\,\text{nF}$ with unstable areas in orange

Figure 5.9: Impact of the MOSFET's gate source capacitance $C_{\text{gs chip}}$ on the cosine phi's of the conjugate-complex eigenvalues of a buck converter topology's operating points in the MOSFET's operating range

Impact of the Chip-External Drain Source Capacitance

The contour plots of of $\cos\phi(\lambda_{1,2})$, $\cos\phi(\lambda_{3,4})$ and $\cos\phi(\lambda_{5,6})$ for different $C_{\mathrm{ds\,ext}}$ are shown in Fig. 5.10. The corresponding contour plots of the eigenfrequencies are shown in Fig. C.7 on page 197. Fig. 5.10(b) depicts the contour plots of the cosine phi's of the initial parameterization. Fig. 5.10(a) and Fig. 5.10(c) show the contour plots of the cosine phi's of the parameterizations with the fifth part and the fivefold of the initial $C_{\mathrm{ds\,ext}}$.

Compared to the corresponding contour plots in Fig. 5.10(b), the reduced $C_{\mathrm{ds\,ext}}$ results in decreased cosine phi's in the saturation region in the contour plots of $\cos\phi(\lambda_{1,2})$ and $\cos\phi(\lambda_{5,6})$ in Fig. 5.10(a). In comparison to the corresponding contour plot in Fig. 5.10(b), the cosine phi's of $\lambda_{3,4}$ in Fig. 5.10(a) are increased. The cosine phi's in the contour plots of $\cos\phi(\lambda_{1,2})$, $\cos\phi(\lambda_{3,4})$ and $\cos\phi(\lambda_{5,6})$ in Fig. 5.10(c) are partly reduced and partly increased compared to the corresponding contour plots in Fig. 5.10(b).

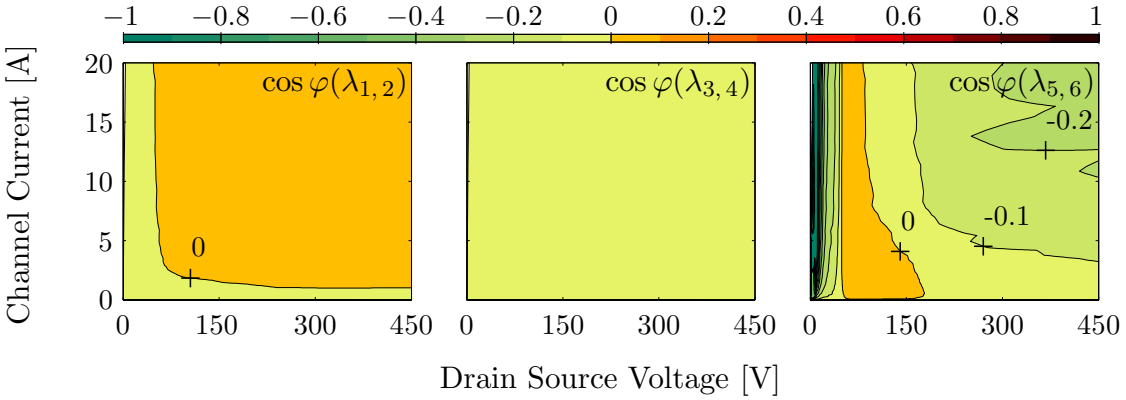
According to Fig. 5.10, the cosine phi's are influenced by the chip-external drain source capacitance. Based on the results in Fig. 5.10, an optimization approach of $C_{\mathrm{ds\,ext}}$ can not be made for the initial parameterization. Input capacitances of voltage probes are easily in a range of 10 pF. Fig. 5.10 shows that the measurement of the drain source voltage can influence the stability of the commutation cell.

Impact of the Chip-External Drain Gate Capacitance

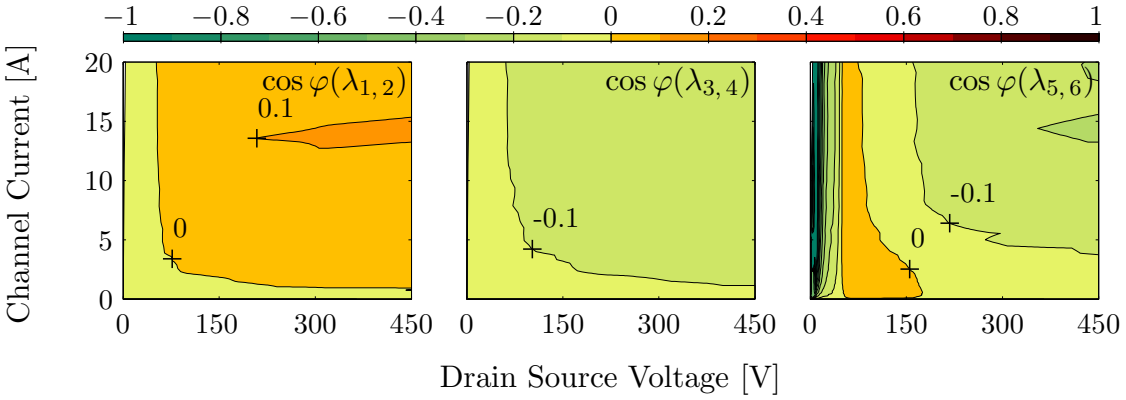
The contour plots of $\cos\phi(\lambda_{1,2})$, $\cos\phi(\lambda_{3,4})$ and $\cos\phi(\lambda_{5,6})$ for different $C_{\mathrm{dg\,ext}}$ are shown in Fig. 5.11. The corresponding contour plots of the eigenfrequencies are shown in Fig. C.8 on page 198. Fig. 5.11(b) depicts the contour plots of the cosine phi's of on the initial parameterization. Fig. 5.11(a) and Fig. 5.11(c) show the contour plots of the cosine phi's of the parameterizations with the fifth part and the fivefold of the initial $C_{\mathrm{dg\,ext}}$. Compared to $C_{\mathrm{dg\,chip}}$ at higher drain source voltages, a $C_{\mathrm{dg\,ext}}$ of 10 pF is very high.

The contour plot of $\cos\phi(\lambda_{5,6})$ in Fig. 5.11(c) has no unstable area. In Fig. 5.11(c), in comparison to the corresponding contour plots in Fig. 5.11(b), the contour plot of $\cos\phi(\lambda_{3,4})$ has areas with increased and decreased cosine phi's, and the contour plot of $\cos\phi(\lambda_{1,2})$ has increased cosine phi's. In Fig. 5.11(a), compared to the corresponding contour plots in Fig. 5.11(b), the unstable area in the contour plot of $\cos\phi(\lambda_{1,2})$ is reduced, but the contour plots of $\cos\phi(\lambda_{3,4})$ and $\cos\phi(\lambda_{5,6})$ show increased cosine phi's.

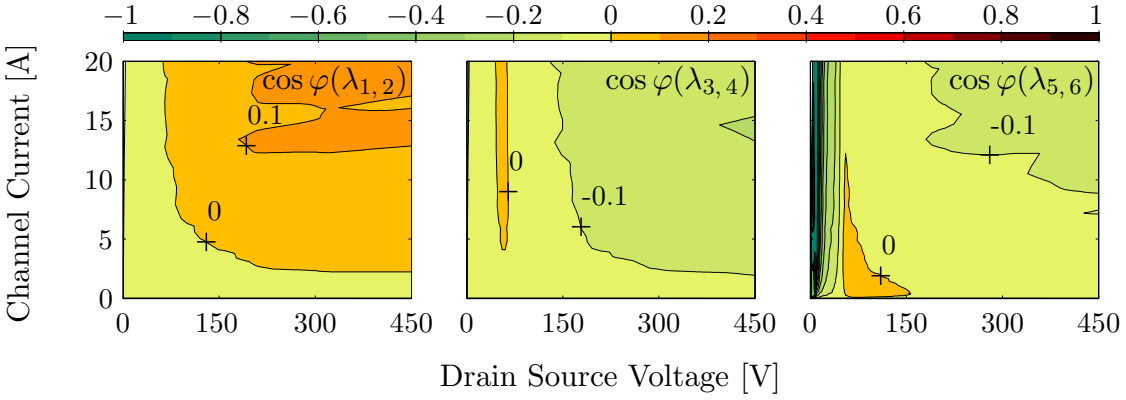
According to Fig. 5.11, the cosine phi's are significantly influenced by the chip-external drain gate capacitance. Based on the results in Fig. 5.11, an optimization approach of $C_{\mathrm{dg\,ext}}$ can not be made for the initial parameterization. Compared to the initial parameterization, higher oscillation amplitudes can be expected during switching for both a decrease and an increase of $C_{\mathrm{dg\,ext}}$. With respect to the stability, the $C_{\mathrm{dg\,ext}}$ is one of the most critical parameters in commutation cells with SJ MOSFETs [Kapels 09]. A careful optimization of the PCB layout is thus necessary (cp. with [Inf 07a]).



(a) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $0.2 \cdot C_{\mathrm{ds\,ext}} = 3\,\mathrm{pF}$ with unstable areas in orange

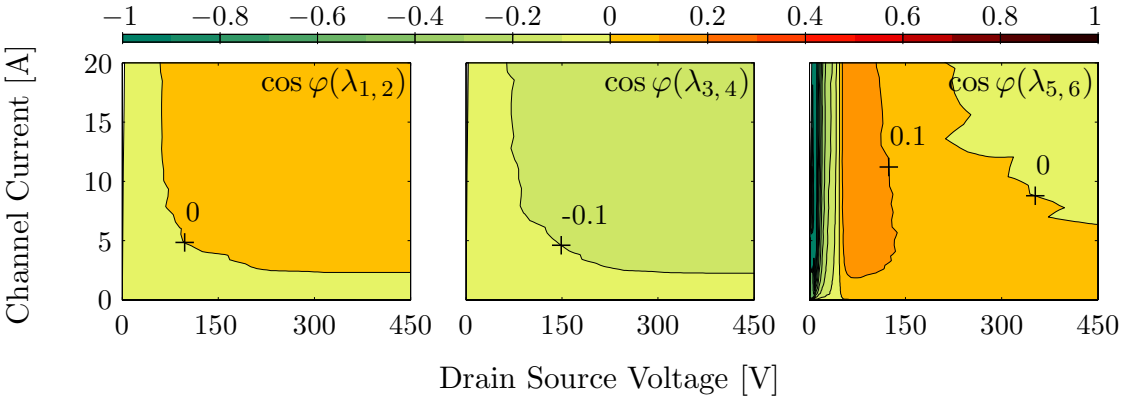


(b) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ of the initial parameterization with unstable areas in orange

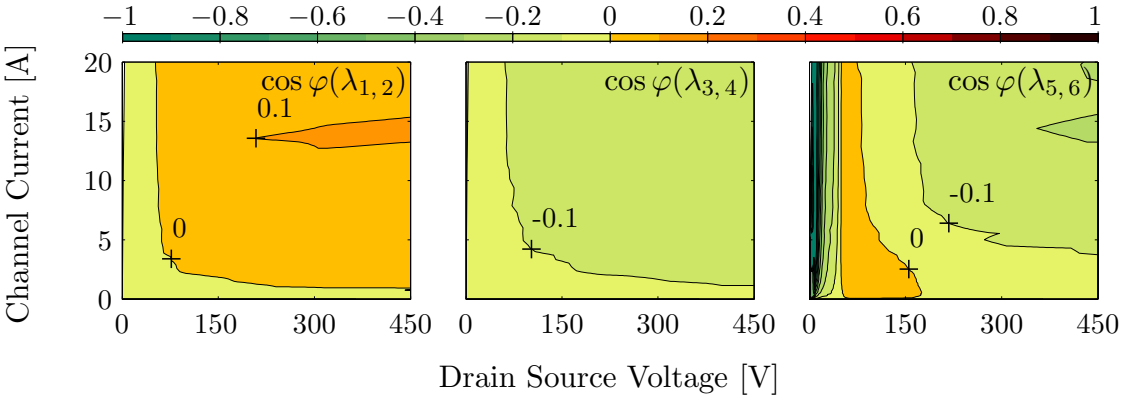


(c) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $5 \cdot C_{\mathrm{ds\,ext}} = 75\,\mathrm{pF}$ with unstable areas in orange

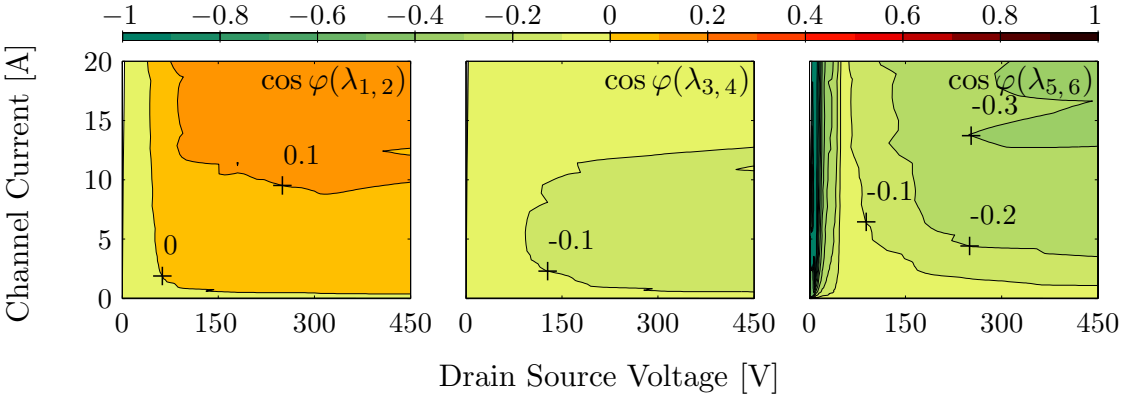
Figure 5.10: Impact of the chip-external drain gate capacitance $C_{\mathrm{ds\,ext}}$ on the cosine phi's of the conjugate-complex eigenvalues of a buck converter topology's operating points in the MOSFET's operating range



(a) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $0.02 \cdot C_{\mathrm{dg\,ext}} = 0.1\,\mathrm{pF}$ with unstable areas in orange



(b) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ of the initial parameterization with unstable areas in orange



(c) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $2 \cdot C_{\mathrm{dg\,ext}} = 10\,\mathrm{pF}$ with unstable areas in orange

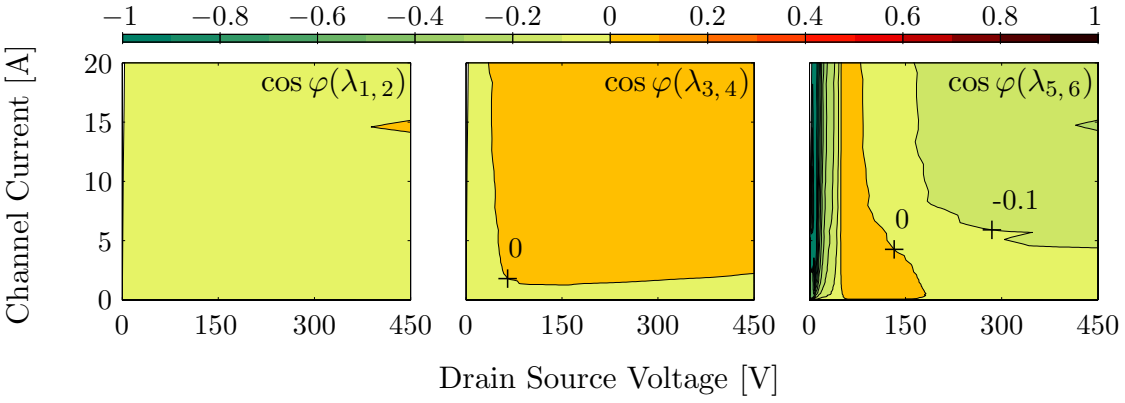
Figure 5.11: Impact of the chip-external drain gate capacitance $C_{\mathrm{dg\,ext}}$ on the cosine phi's of the conjugate-complex eigenvalues of a buck converter topology's operating points in the MOSFET's operating range

Impact of the Chip-External Gate Source Capacitance

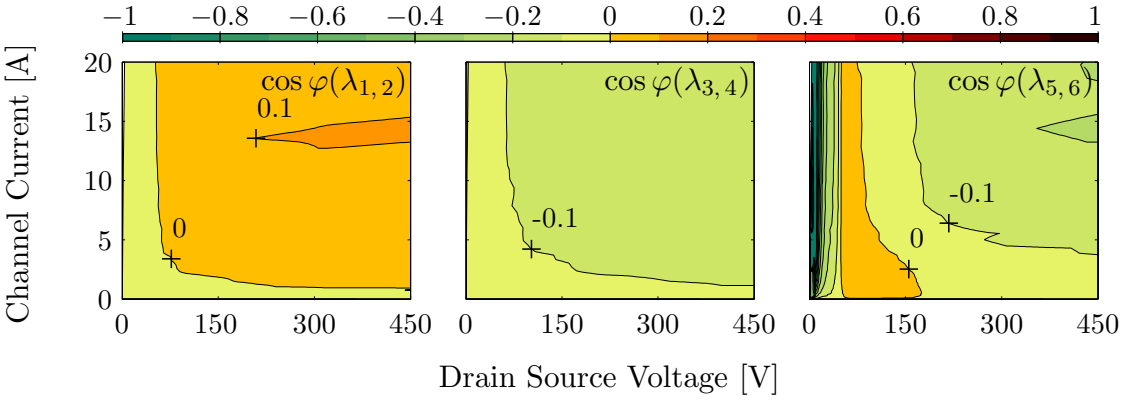
The contour plots of the cosine phi's of $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ for different $C_{\mathrm{gs\,ext}}$ are shown in Fig. 5.12. The corresponding contour plots of the eigenfrequencies are shown in Fig. C.9 on page 199. Fig. 5.12(b) depicts the contour plots of the cosine phi's of the initial parameterization. Fig. 5.12(a) and Fig. 5.12(c) show the contour plots of the cosine phi's of the parameterizations with the fifth part and the fivefold of the initial $C_{\mathrm{gs\,ext}}$. Compared to the chip-internal gate source capacitance $C_{\mathrm{gs\,chip}}$ of 1.47 nF, the considered values of chip-external capacitance $C_{\mathrm{gs\,ext}}$ are relatively small.

In comparison to the corresponding contour plots in Fig. 5.12(b), the cosine phi's in the contour plots of $\cos\phi(\lambda_{3,4})$ and $\cos\phi(\lambda_{5,6})$ in Fig. 5.12(c) are decreased and the cosine phi's in the contour plots of $\cos\phi(\lambda_{3,4})$ and $\cos\phi(\lambda_{5,6})$ in Fig. 5.12(a) are increased. Compared to the corresponding contour plot in Fig. 5.12(b), the cosine phi's of the contour plot of $\cos\phi(\lambda_{1,2})$ are increased in Fig. 5.12(c) and decreased in Fig. 5.12(a).

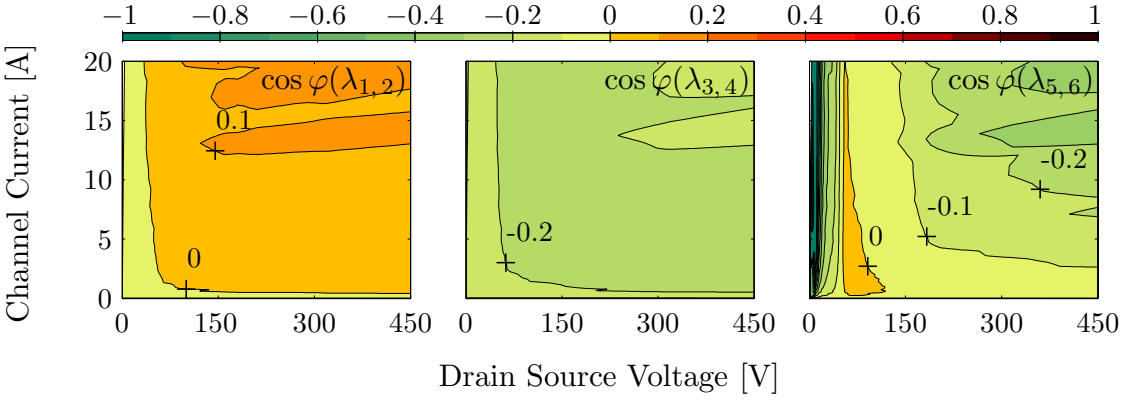
According to Fig. 5.12, the cosine phi's are influenced by the chip-external gate source capacitance. The unstable area in the $I_{\mathrm{Ch}}(V_{\mathrm{DS\,chip}})$ plane minimizes probably between the initial $C_{\mathrm{gs\,ext}}$ and the fifth part of the initial $C_{\mathrm{gs\,ext}}$. Thus, a slight reduction of the initial $C_{\mathrm{gs\,ext}}$ seems to be advantageous for the stability of the commutation cell. Input capacitances of voltage probes are easily in a range of 10 pF. Fig. 5.12 shows that the measurement of the gate source voltage can influence the stability of the commutation cell.



(a) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $0.2 \cdot C_{\mathrm{gs\,ext}} = 3\,\mathrm{pF}$ with unstable areas in orange



(b) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ of the initial parameterization with unstable areas in orange



(c) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $5 \cdot C_{\mathrm{gs\,ext}} = 75\,\mathrm{pF}$ with unstable areas in orange

Figure 5.12: Impact of the chip-external gate source capacitance $C_{\mathrm{gs\,ext}}$ on the cosine phi's of the conjugate-complex eigenvalues of a buck converter topology's operating points in the MOSFET's operating range

Impact of the Drain Inductances

The contour plots of the cosine phi's of the conjugate-complex eigenvalues for different $L_{\mathrm{d\,pac}}$ are shown in Fig. 5.13. The corresponding contour plots of the eigenfrequencies are shown in Fig. C.10 on page 200. Fig. 5.13(b) depicts the contour plots of the cosine phi's of the initial parameterization. Fig. 5.13(a) and Fig. 5.13(c) show the contour plots of the cosine phi's of the parameterizations with the fifth part and the fivefold of the initial $L_{\mathrm{d\,pac}}$.

In comparison to the corresponding contour plots in Fig. 5.13(b), the contour plots of $\cos\phi(\lambda_{3,4})$ and $\cos\phi(\lambda_{5,6})$ in Fig. 5.13(a) are hardly affected by the reduction of $L_{\mathrm{d\,pac}}$. Compared to the corresponding contour plot in Fig. 5.13(b), the cosine phi's of $\cos\phi(\lambda_{5,6})$ in Fig. 5.13(a) are slightly reduced. In Fig. 5.13(c), the contour plots of $\cos\phi(\lambda_{1,2})$ and $\cos\phi(\lambda_{5,6})$ show reduced cosine phi's compared to the corresponding plots in Fig. 5.13(b), but the cosine phi's in the contour plot of $\cos\phi(\lambda_{3,4})$ are significantly increased in comparison to the corresponding contour plot in Fig. 5.13(b).

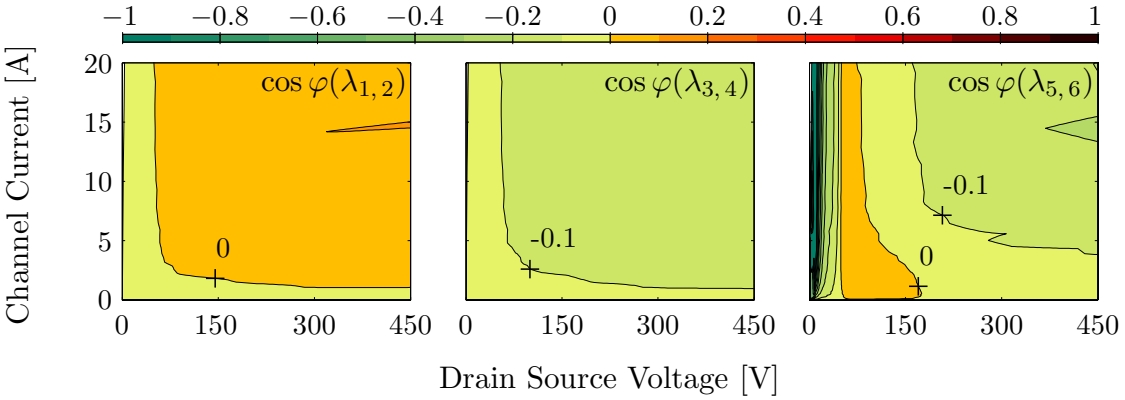
According to Fig. 5.13, the cosine phi's of the conjugate-complex eigenvalues are influenced by $L_{\mathrm{d\,pac}}$. Based on the results in Fig. 5.13, an optimization approach of $L_{\mathrm{d\,pac}}$ can not be made for the initial parameterization. However, the MOSFET's switching times would increase with higher $L_{\mathrm{d\,pac}}$.

The contour plots of the cosine phi's of the conjugate-complex eigenvalues for different $L_{\mathrm{d\,cir}}$ are shown in Fig. 5.14. The corresponding contour plots of the eigenfrequencies are shown in Fig. C.11 on page 201. Fig. 5.14(b) depicts the contour plots of the cosine phi's of the initial parameterization. Fig. 5.14(a) and Fig. 5.14(c) show the contour plots of the cosine phi's of the parameterizations with the fifth part and the fivefold of the initial $L_{\mathrm{d\,cir}}$.

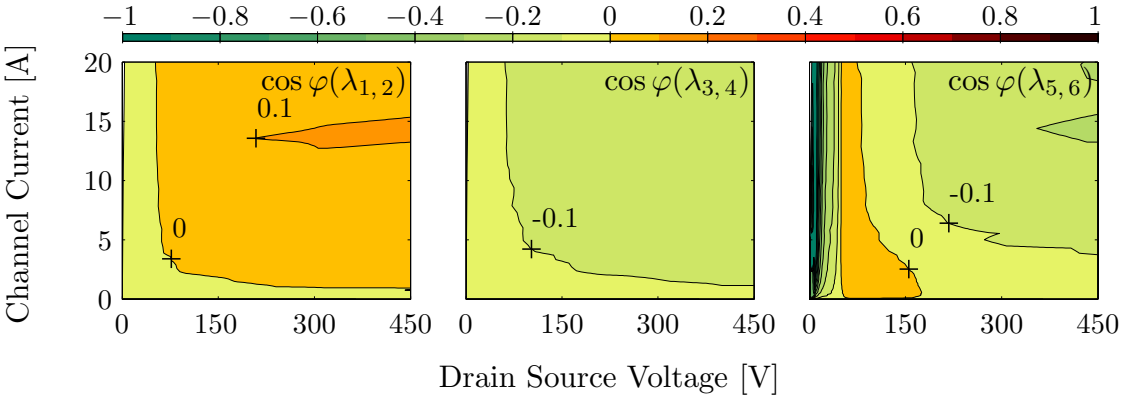
Compared to the corresponding contour plot in Fig. 5.14(b), the cosine phi's of $\cos\phi(\lambda_{1,2})$ in Fig. 5.14(c) are increased and the cosine phi's of $\cos\phi(\lambda_{1,2})$ in Fig. 5.14(a) are decreased. In comparison to the corresponding contour plot in Fig. 5.14(b), the cosine phi's are significantly increased in the contour plot of $\lambda_{5,6}$ in Fig. 5.14(a). Positive cosine phi's do not exist in the contour plot of $\lambda_{5,6}$ in Fig. 5.14(c). The contour plots of $\cos\phi(\lambda_{3,4})$ are little affected by the alteration of $L_{\mathrm{d\,cir}}$.

According to Fig. 5.14, the cosine phi's of the conjugate-complex eigenvalues are influenced by $L_{\mathrm{d\,cir}}$. Based on the results in Fig. 5.14, an optimization approach of $L_{\mathrm{d\,cir}}$ can not be made for the initial parameterization. However, the MOSFET's switching times would increase with higher $L_{\mathrm{d\,cir}}$.

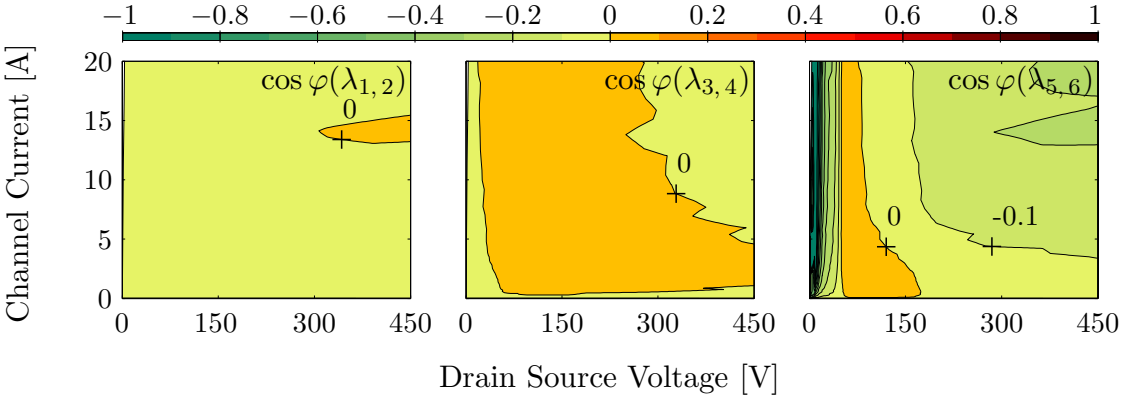
Fig. 5.13 and Fig. 5.14 show that the increase (or the decrease) of $L_{\mathrm{d\,pac}}$ and the increase (or the decrease) of $L_{\mathrm{d\,cir}}$ might have an opposing effect on the cosine phi's of the different eigenvalue pairs. The implementation of a PEARSON probe into the drain current path causes easily 15 nH additional drain inductance. Fig. 5.13 and Fig. 5.14 show that the drain current measurement has an impact on the stability of the commutation cell.



(a) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $0.2 \cdot L_{\mathrm{d\,pac}} = 0.4\,\mathrm{nH}$ with unstable areas in orange

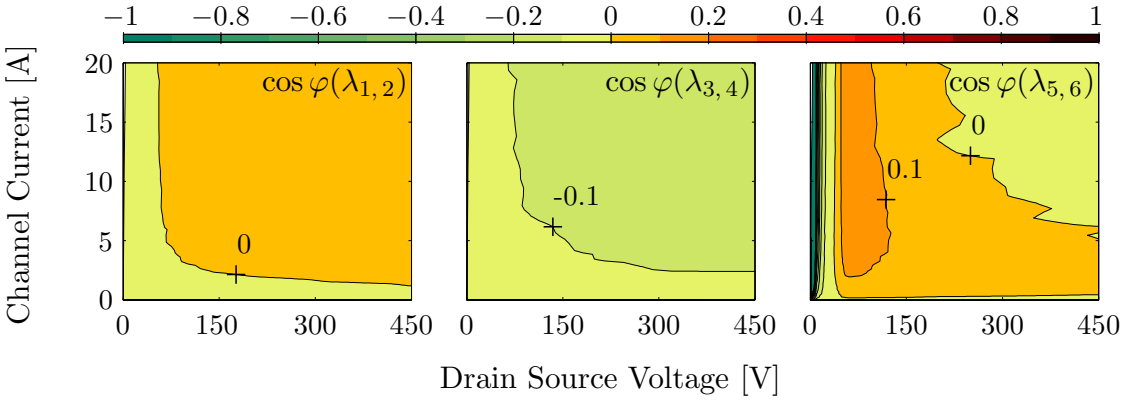


(b) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ of the initial parameterization with unstable areas in orange

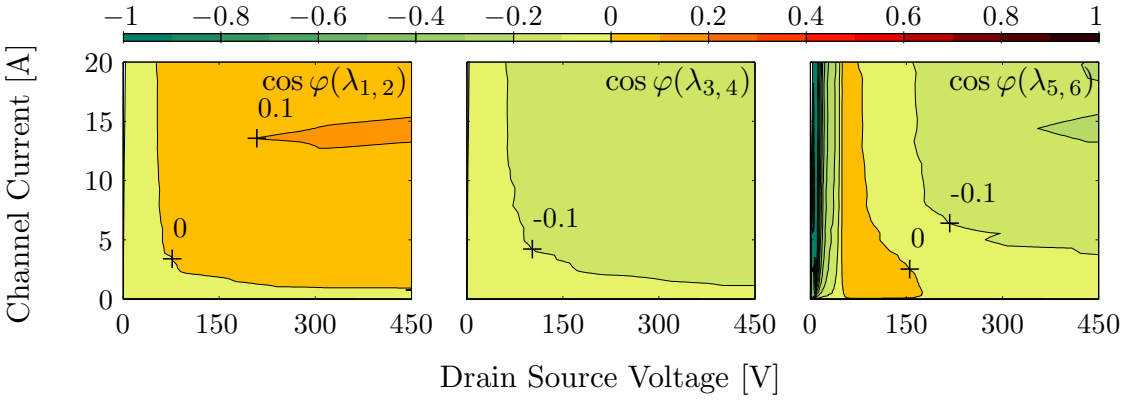


(c) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $5 \cdot L_{\mathrm{d\,pac}} = 10\,\mathrm{nH}$ with unstable areas in orange

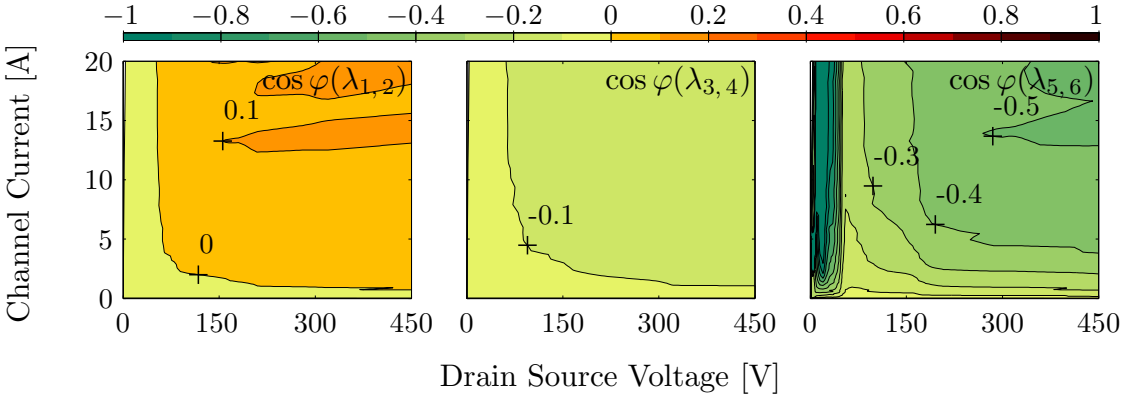
Figure 5.13: Impact of the drain inductance $L_{\mathrm{d\,pac}}$ on the cosine phi's of the conjugate-complex eigenvalues of a buck converter topology's operating points in the MOSFET's operating range



(a) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $0.2 \cdot L_{\mathrm{d\,cir}} = 7\,\mathrm{nH}$ with unstable areas in orange



(b) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ of the initial parameterization with unstable areas in orange



(c) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $5 \cdot L_{\mathrm{d\,cir}} = 175\,\mathrm{nH}$ with unstable areas in orange

Figure 5.14: Impact of the drain inductance $L_{\mathrm{d\,cir}}$ on the cosine phi's of the conjugate-complex eigenvalues of a buck converter topology's operating points in the MOSFET's operating range

Impact of the Gate Inductances

The contour plots of the cosine phi's of the conjugate-complex eigenvalues for different $L_{\mathrm{g\,pac}}$ are shown in Fig. 5.15. The corresponding contour plots of the eigenfrequencies are shown in Fig. C.12 on page 202. Fig. 5.15(b) depicts the contour plots of the cosine phi's of the initial parameterization. Fig. 5.15(a) and Fig. 5.15(c) show the contour plots of the cosine phi's of the parameterizations with the fifth part and the fivefold of the initial $L_{\mathrm{g\,pac}}$.

In comparison to the corresponding contour plots in Fig. 5.15(b), the cosine phi's are increased in the contour plot of $\cos\phi(\lambda_{5,6})$ in Fig. 5.15(c) and decreased in the contour plot of $\cos\phi(\lambda_{3,4})$ in Fig. 5.15(c). Compared to the corresponding contour plots in Fig. 5.15(b), areas with increased and areas with decreased cosine phi's exist in the contour plot of $\cos\phi(\lambda_{1,2})$ in Fig. 5.15(c). In comparison to the corresponding contour plots in Fig. 5.15(b), the cosine phi's are decreased in the contour plots of $\cos\phi(\lambda_{1,2})$ and $\cos\phi(\lambda_{5,6})$ in Fig. 5.15(a) and increased in the contour plot of $\cos\phi(\lambda_{3,4})$ in Fig. 5.15(a).

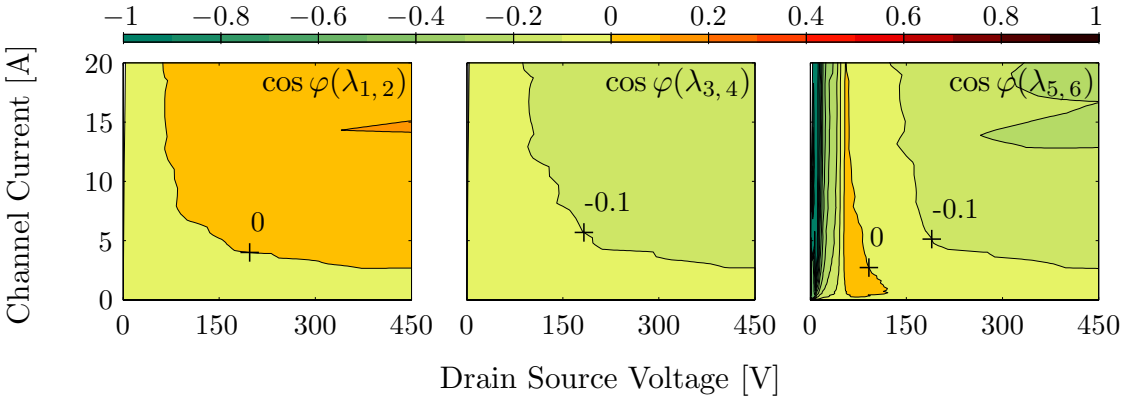
Fig. 5.15 shows that the increase (or the decrease) of $L_{\mathrm{g\,pac}}$ might have an opposing effect on the cosine phi's of the different conjugate-complex eigenvalues. According to Fig. 5.15, the unstable areas decrease with decreasing $L_{\mathrm{g\,pac}}$ and vice versa. Compared to the initial parameterization, for the decreased $L_{\mathrm{g\,pac}}$, lower oscillation amplitudes are thus expected during switching. The commutation cell is less unstable/more stable for lower $L_{\mathrm{g\,pac}}$.

The contour plots of the cosine phi's of the conjugate-complex eigenvalues for different $L_{\mathrm{g\,cir}}$ are shown in Fig. 5.16. The corresponding contour plots of the eigenfrequencies are shown in Fig. C.13 on page 203. Fig. 5.16(b) depicts the contour plots of the cosine phi's of the initial parameterization. Fig. 5.16(a) and Fig. 5.16(c) show the contour plots of the cosine phi's of the parameterizations with the half and the double value of the initial $L_{\mathrm{g\,cir}}$.

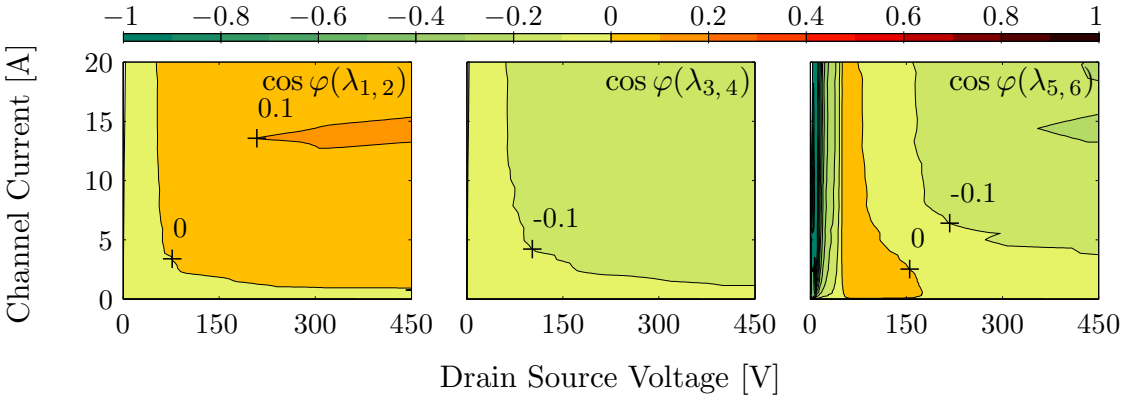
Compared to the corresponding contour plots in Fig. 5.16(b), the cosine phi's in the contour plots of $\cos\phi(\lambda_{1,2})$, $\cos\phi(\lambda_{3,4})$ and $\cos\phi(\lambda_{5,6})$ in Fig. 5.16(a) are decreased. In comparison corresponding contour plots in Fig. 5.16(b), the cosine phi's in the contour plot of $\cos\phi(\lambda_{1,2})$, $\cos\phi(\lambda_{3,4})$ and $\cos\phi(\lambda_{5,6})$ in Fig. 5.16(c) are increased.

According to Fig. 5.16, the cosine phi's decrease with decreasing $L_{\mathrm{g\,cir}}$. Compared to the initial parameterization, for the decreased $L_{\mathrm{g\,cir}}$, lower oscillation amplitudes are thus expected during switching. The commutation cells is less unstable/more stable for lower $L_{\mathrm{g\,cir}}$.

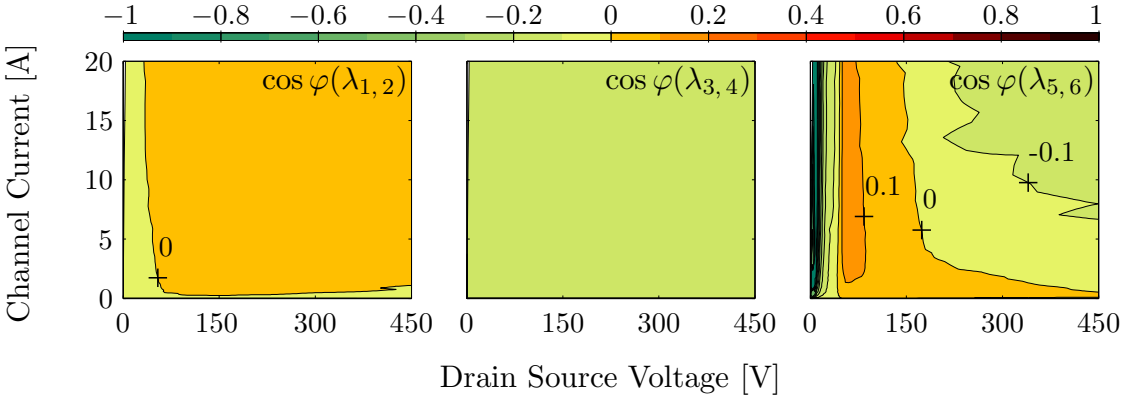
Fig. 5.15 and Fig. 5.16 show that - with respect to the stability - a reduction of $L_{\mathrm{g\,pac}}$ is more effective than a comparable reduction of $L_{\mathrm{g\,cir}}$. The implementation of a PEARSON probe into the gate current path causes easily 15 nH additional gate inductance. Fig. 5.15 and Fig. 5.16 show that the gate current measurement has an impact on the stability.



(a) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $0.2 \cdot L_{\mathrm{g\,pac}} = 0.94\,\mathrm{nH}$ with unstable areas in orange

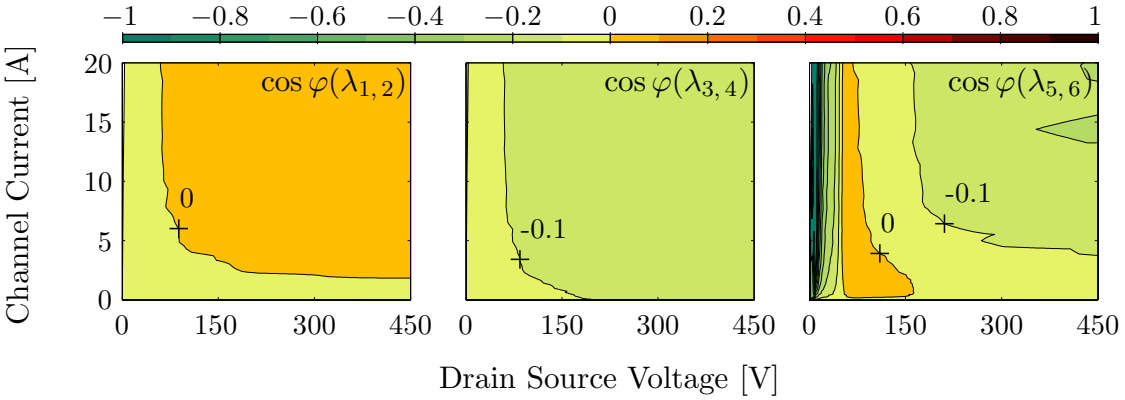


(b) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ of the initial parameterization with unstable areas in orange

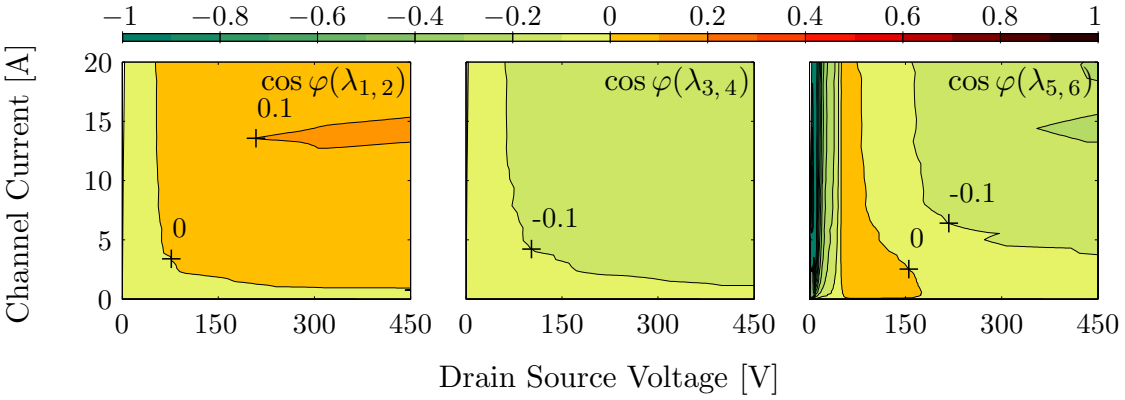


(c) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $5 \cdot L_{\mathrm{g\,pac}} = 23.5\,\mathrm{nH}$ with unstable areas in orange

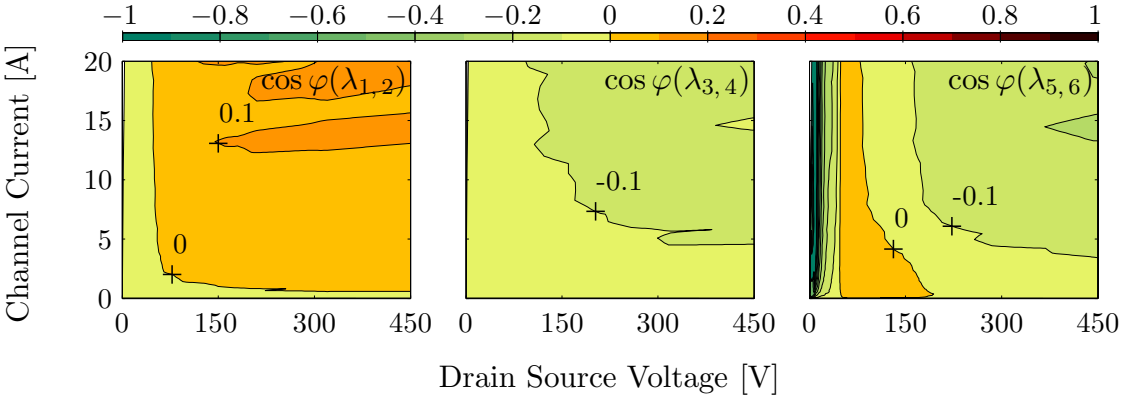
Figure 5.15: Impact of the gate inductance $L_{\mathrm{g\,pac}}$ on the cosine phi's of the conjugate-complex eigenvalues of a buck converter topology's operating points in the MOSFET's operating range



(a) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $0.5 \cdot L_{\mathrm{g\,cir}} = 3\,\mathrm{nH}$ with unstable areas in orange



(b) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ of the initial parameterization with unstable areas in orange



(c) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $2 \cdot L_{\mathrm{g\,cir}} = 12\,\mathrm{nH}$ with unstable areas in orange

Figure 5.16: Impact of the gate inductance $L_{\mathrm{g\,cir}}$ on the cosine phi's of the conjugate-complex eigenvalues of a buck converter topology's operating points in the MOSFET's operating range

Impact of the Source Inductances

The contour plots of the cosine phi's of the conjugate-complex eigenvalues for different $L_{\mathrm{s\,pac}}$ are shown in Fig. 5.17. The corresponding contour plots of the eigenfrequencies are shown in Fig. C.14 on page 204. Fig. 5.17(b) depicts the contour plots of the cosine phi's of the initial parameterization. Fig. 5.17(a) and Fig. 5.17(c) show the contour plots of the cosine phi's of the parameterizations wiht the fifth part and the fivefold of the initial $L_{\mathrm{s\,pac}}$.

Compared to the corresponding contour plots in Fig. 5.17(b), the cosine phi's in the contour plots of $\cos\phi(\lambda_{1,2})$ and $\cos\phi(\lambda_{5,6})$ are significantly reduced in Fig. 5.17(a). In the contour plot of $\cos\phi(\lambda_{5,6})$ in Fig. 5.17(a) an area with positive cosine phi's does not exist. In comparison to the corresponding contour plot in Fig. 5.17(b), the cosine phi's in the contour plot of $\cos\phi(\lambda_{3,4})$ are increased in Fig. 5.17(a) and decreased in Fig. 5.17(c). Compared to the corresponding contour plot in Fig. 5.17(b), the unstable area in the contour plot of $\cos\phi(\lambda_{5,6})$ in Fig. 5.17(c) is significantly increased. In comparison to the corresponding contour plot in Fig. 5.17(b), the cosine phi's are partly increased and partly decrease in the contour plot of $\cos\phi(\lambda_{1,2})$ in Fig. 5.17(c).

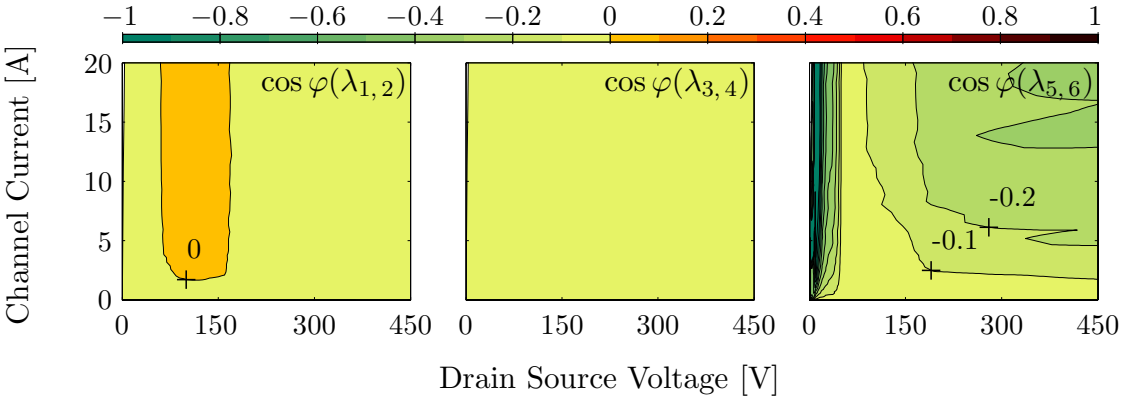
According to Fig. 5.17, the unstable areas decrease with decreasing $L_{\mathrm{s\,pac}}$. Compared to the initial parameterization, for the decreased $L_{\mathrm{s\,pac}}$, lower oscillation amplitudes are expected during switching. The commutation cells is less unstable/more stable for lower $L_{\mathrm{s\,pac}}$.

The contour plots of the cosine phi's of the conjugate-complex eigenvalues for different $L_{\mathrm{s\,cir}}$ are shown in Fig. 5.18. The corresponding contour plots of the eigenfrequencies are shown in Fig. C.15 on page 205. Fig. 5.18(b) depicts the contour plots of the cosine phi's of the initial parameterization. Fig. 5.18(a) and Fig. 5.18(c) show the contour plots of the cosine phi's of the parameterizations with the fifth part and the fivefold of the initial $L_{\mathrm{s\,cir}}$.

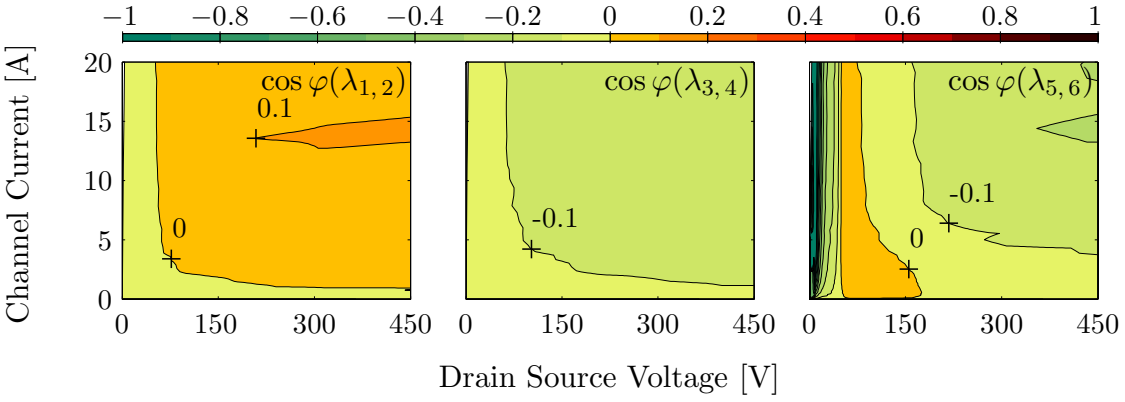
Compared to the corresponding contour plot in Fig. 5.18(b), the cosine phi's in the contour plot of $\cos\phi(\lambda_{1,2})$ in Fig. 5.18(a) is slightly reduced. In the contour plot of $\cos\phi(\lambda_{5,6})$ in Fig. 5.18(a) an area with positive cosine phi's does not exist. In comparison to the corresponding contour plot in Fig. 5.18(b), the cosine phi's are decreased in the contour plot of $\cos\phi(\lambda_{3,4})$ in Fig. 5.18(a). Compared to the corresponding contour plot in Fig. 5.18(b), the unstable area in the contour plot of $\cos\phi(\lambda_{5,6})$ in Fig. 5.18(c) are significantly increased. In comparison to the corresponding plots in Fig. 5.18(b), the cosine phi's are increased in the contour plots of $\cos\phi(\lambda_{1,2})$ and $\cos\phi(\lambda_{3,4})$ in Fig. 5.18(c).

According to Fig. 5.18, the cosine phi's decrease with decreasing $L_{\mathrm{s\,cir}}$ and vice versa. Compared to the initial parameterization, for the decreased $L_{\mathrm{s\,cir}}$, lower oscillation amplitudes are therefore expected during switching operations. The commutation cell is less unstable/more stable for lower $L_{\mathrm{s\,cir}}$.

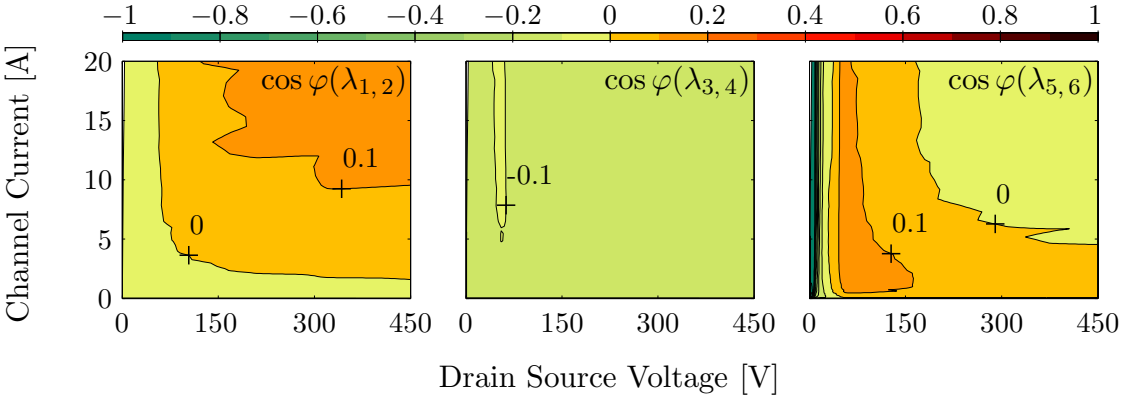
The contour plots of the cosine phi's of the conjugate-complex eigenvalues for the combined alteration of the source inductances are shown in Fig. 5.19. The corresponding contour plots of the eigenfrequencies are shown in Fig. C.16 on page 206. Fig. 5.19(b) depicts the contour plots of the cosine phi's of the initial parameterization. Fig. 5.19(a) and Fig. 5.19(c) show the contour plots of the cosine phi's of the parameterizations with the fifth part and the fivefold of the initial source inductances.



(a) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $0.2 \cdot L_{\mathrm{s\,pac}} = 0.82\,\mathrm{nH}$ with unstable areas in orange

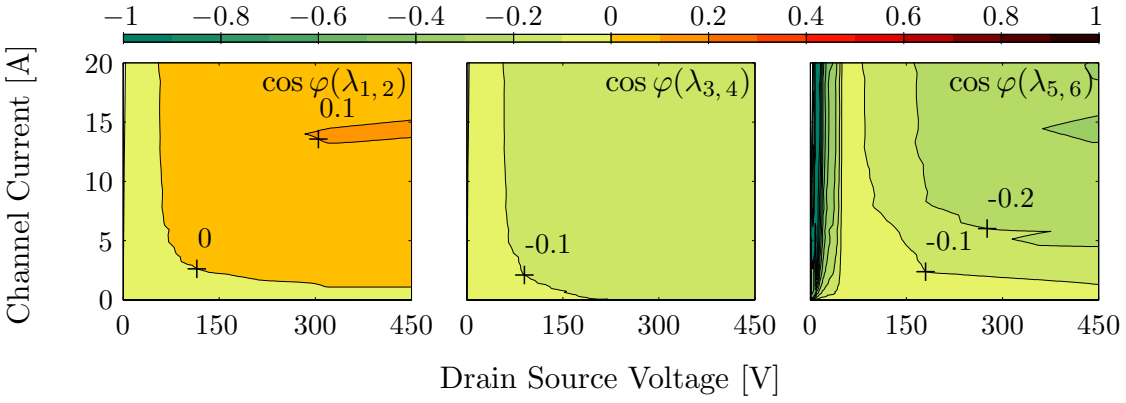


(b) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ of the initial parameterization with unstable areas in orange

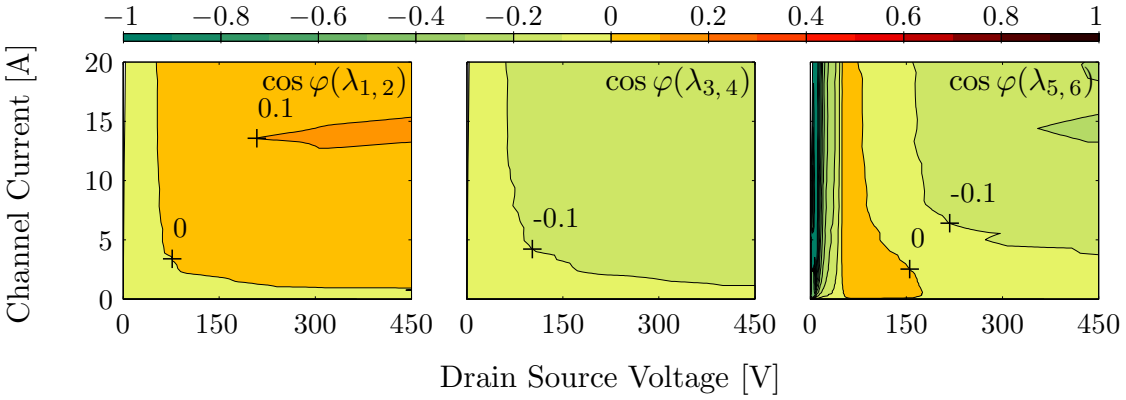


(c) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $5 \cdot L_{\mathrm{s\,pac}} = 20.5\,\mathrm{nH}$ with unstable areas in orange

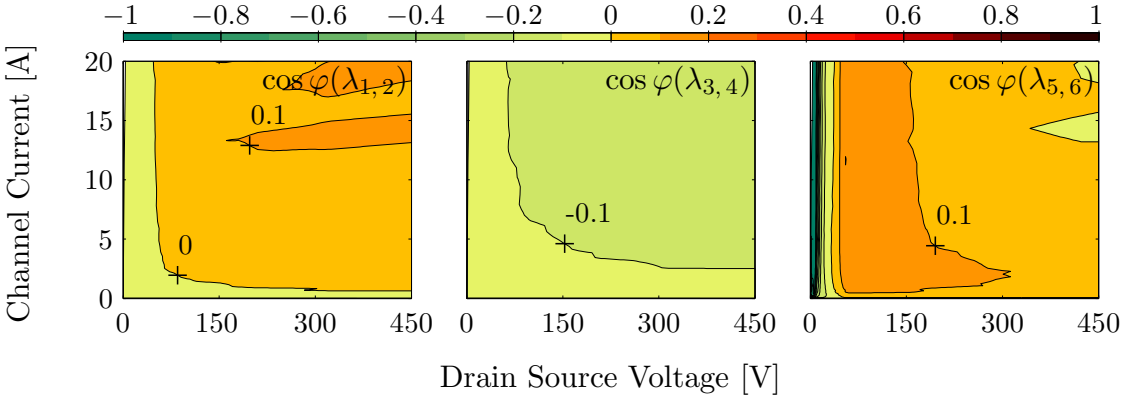
Figure 5.17: Impact of the source inductance $L_{\mathrm{s\,pac}}$ on the cosine phi's of the conjugate-complex eigenvalues of a buck converter topology's operating points in the MOSFET's operating range



(a) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $0.2 \cdot L_{\mathrm{s\,cir}} = 0.6\,\mathrm{nH}$ with unstable areas in orange

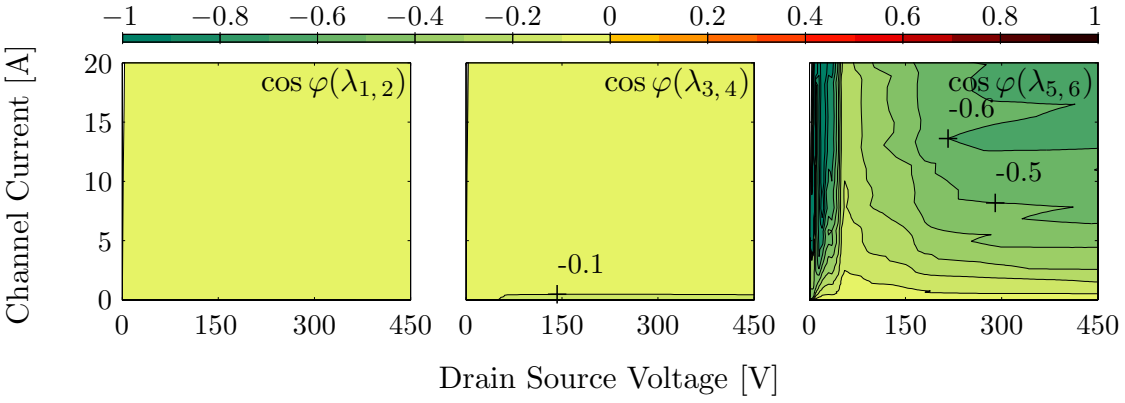


(b) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ of the initial parameterization with unstable areas in orange

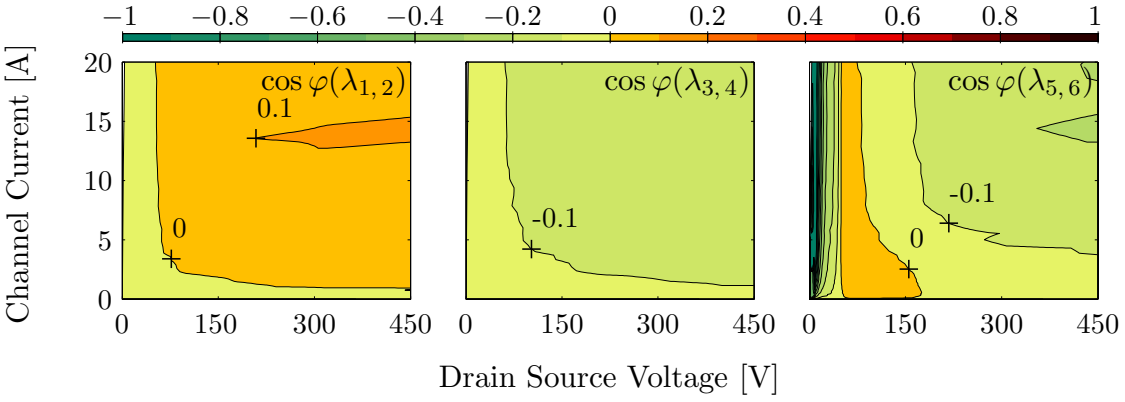


(c) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $5 \cdot L_{\mathrm{s\,cir}} = 15\,\mathrm{nH}$ with unstable areas in orange

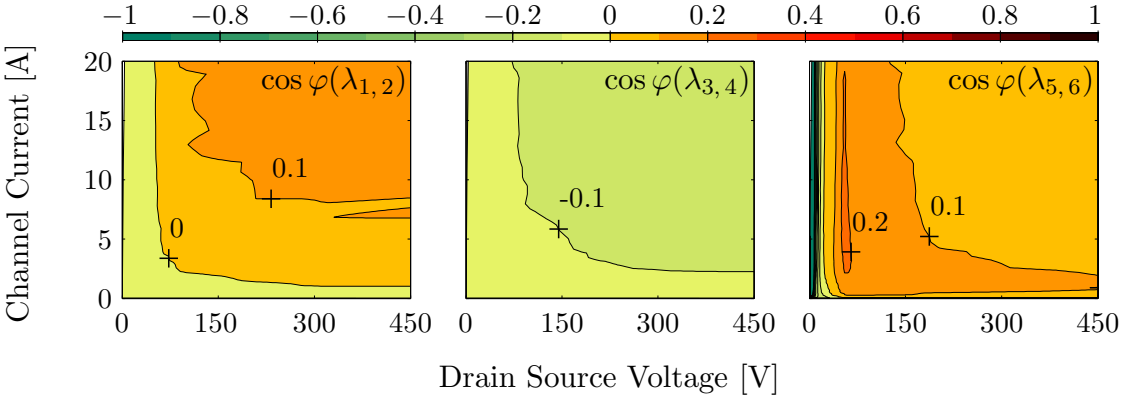
Figure 5.18: Impact of the source inductance $L_{\mathrm{s\,cir}}$ on the cosine phi's of the conjugate-complex eigenvalues of a buck converter topology's operating points in the MOSFET's operating range



(a) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $0.2 \cdot L_{\mathrm{s\,pac}} = 0.82\,\mathrm{nH}$ and $0.2 \cdot L_{\mathrm{s\,cir}} = 0.6\,\mathrm{nH}$



(b) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ of the initial parameterization with unstable areas in orange



(c) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $5 \cdot L_{\mathrm{s\,pac}} = 20.5\,\mathrm{nH}$ and $5 \cdot L_{\mathrm{s\,cir}} = 15\,\mathrm{nH}$

Figure 5.19: Impact of the source inductances $L_{\mathrm{s\,pac}}$ and $L_{\mathrm{s\,cir}}$ on the cosine phi's of the conjugate-complex eigenvalues of a buck converter topology's operating points in the MOSFET's operating range

In the contour plot of $\cos\phi(\lambda_{1,2})$, $\cos\phi(\lambda_{3,4})$ and $\cos\phi(\lambda_{5,6})$ in Fig. 5.19(a), no area with positive cosine phi's exist. In comparison to the corresponding contour plots in Fig. 5.19(b), the cosine phi's of $\cos\phi(\lambda_{1,2})$, $\cos\phi(\lambda_{3,4})$ and $\cos\phi(\lambda_{5,6})$ in Fig. 5.19(c) are increased.

According to Fig. 5.19, the unstable areas decrease with decreasing source inductances and vice versa. Compared to the initial parameterization, for the decreased source inductances, lower oscillation amplitudes are thus expected in the commutation cell during switching. The stability of commutation cells is improved for lower source inductances.

The reduction of the inductance $L_{\mathrm{s\,pac}}$ decreases the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$ and $\lambda_{5,6}$ more severely than the reduction of the inductance $L_{\mathrm{s\,cir}}$. Fig. 5.19 shows that the combination of two circuit optimizations results in a further reduced cosine phi's the conjugate-complex eigenvalues $\lambda_{1,2}$ and $\lambda_{5,6}$. The reduction of the inductance $L_{\mathrm{s\,cir}}$ decreases the cosine phi's of the conjugate-complex eigenvalue pair $\lambda_{3,4}$ more severely than the reduction of the inductance $L_{\mathrm{s\,pac}}$. However, the combination of the two circuit optimizations results only in slightly better cosine phi's of the conjugate-complex eigenvalue pair $\lambda_{3,4}$ than in the corresponding contour plot in Fig. 5.17(a).

Impact of the Drain Resistances

The contour plots of the cosine phi's of $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ for different $R_{\mathrm{d\,pac}}$ are shown in Fig. 5.20. The corresponding contour plots of the eigenfrequencies are shown in Fig. C.17 on page 207. Fig. 5.20(b) depicts the contour plots of the initial parameterization. Fig. 5.20(a) and Fig. 5.20(c) show the contour plots of the cosine phi's of the parameterizations with the minus five hundredfold and the five hundredfold of the initial $R_{\mathrm{d\,pac}}$.[7]

Compared to the corresponding contour plot in Fig. 5.20(b), the cosine phi's in the contour plot of $\lambda_{1,2}$ are decreased in Fig. 5.20(a) and increased in Fig. 5.20(c). The contour plots of $\cos\phi(\lambda_{3,4})$ and $\cos\phi(\lambda_{5,6})$ are not affected by the alteration of $R_{\mathrm{d\,pac}}$.

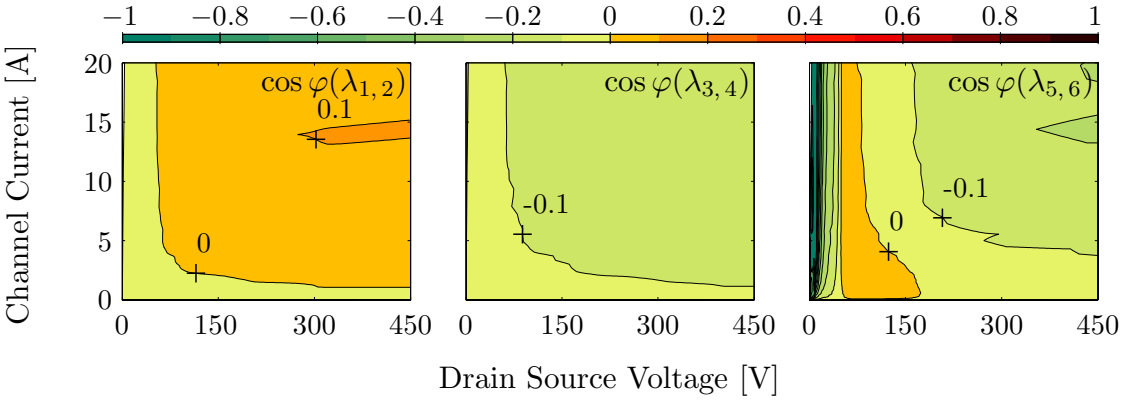
Fig. 3.12(a) and Fig. 3.12(c) on page 88 et seq. show that the absolute values of the chosen multipliers are unrealistic high. For more realistic values, an impact on the contour plots of the conjugate-complex eigenvalues' cosine phi's can not be observed. The impact of $R_{\mathrm{d\,pac}}$ is usually negligible for the stability of commutation cells.

In Fig. 5.21, the contour plots of the cosine phi's of the conjugate-complex eigenvalues for different $R_{\mathrm{d\,cir}}$ are shown. The corresponding contour plots of the eigenfrequencies are shown in Fig. C.18 on page 208. Fig. 5.21(b) depicts the contour plots of the initial parameterization. Fig. 5.21(a) and Fig. 5.21(c) show the contour plots of the cosine phi's of the parameterizations with the minus five and the five hundredfold of the initial $R_{\mathrm{d\,cir}}$.[7]

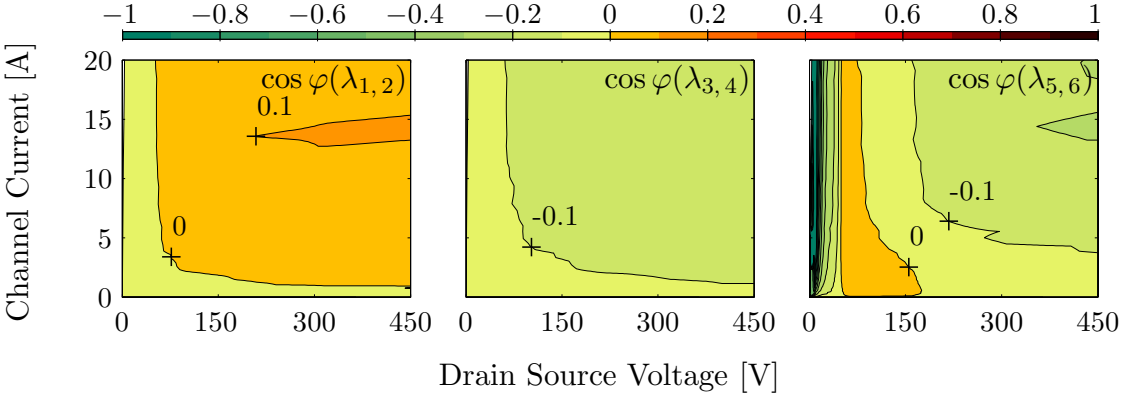
Compared to the corresponding contour plot in Fig. 5.21(b), the cosine phi's in the contour plot of $\lambda_{5,6}$ are decreased in Fig. 5.21(a) and increased in Fig. 5.21(c). The contour plots of $\cos\phi(\lambda_{3,4})$ and $\cos\phi(\lambda_{5,6})$ are not affected by the alteration of $R_{\mathrm{d\,cir}}$.

The chosen multipliers are unrealistic high. For more realistic values, the impact of $R_{\mathrm{d\,cir}}$ is usually negligible for the stability of commutation cells.

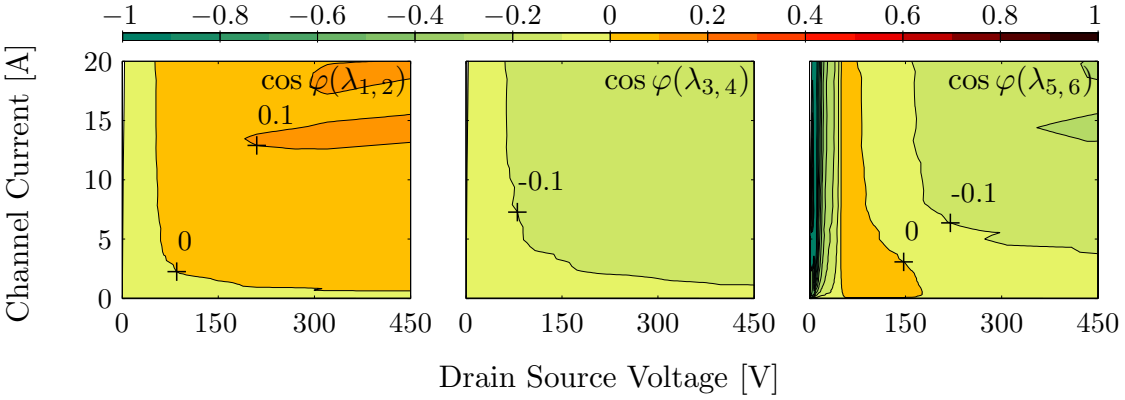
[7] The negative multiplier considers the changing sign of the effective resistance during switching operations. See subsection **3.3.2** on page 85 et seq. for details.



(a) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $-500 \cdot R_{\mathrm{d\,pac}} = -0.235\,\Omega$ with unstable areas in orange

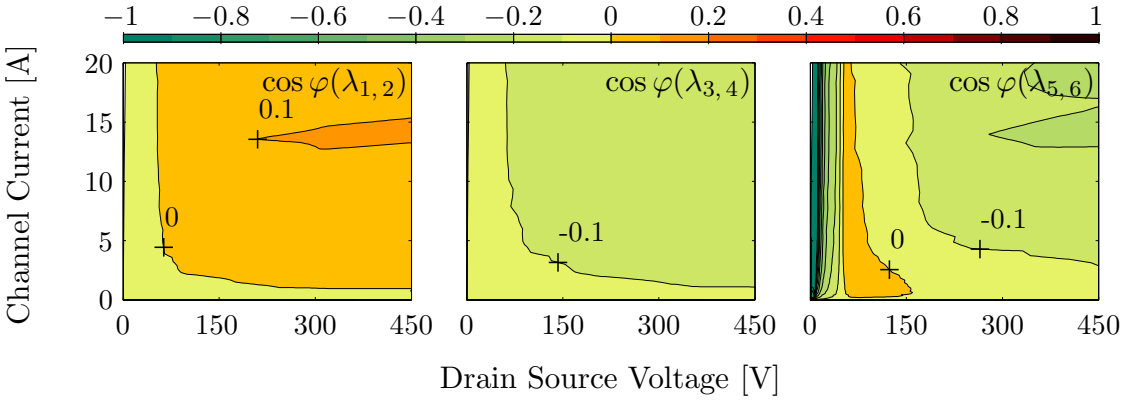


(b) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ of the initial parameterization with unstable areas in orange

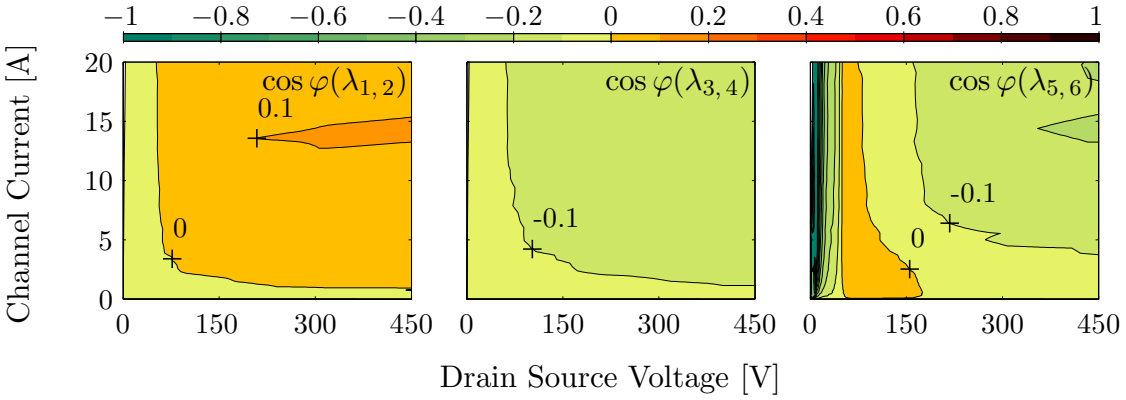


(c) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $500 \cdot R_{\mathrm{d\,pac}} = 0.235\,\Omega$ with unstable areas in orange

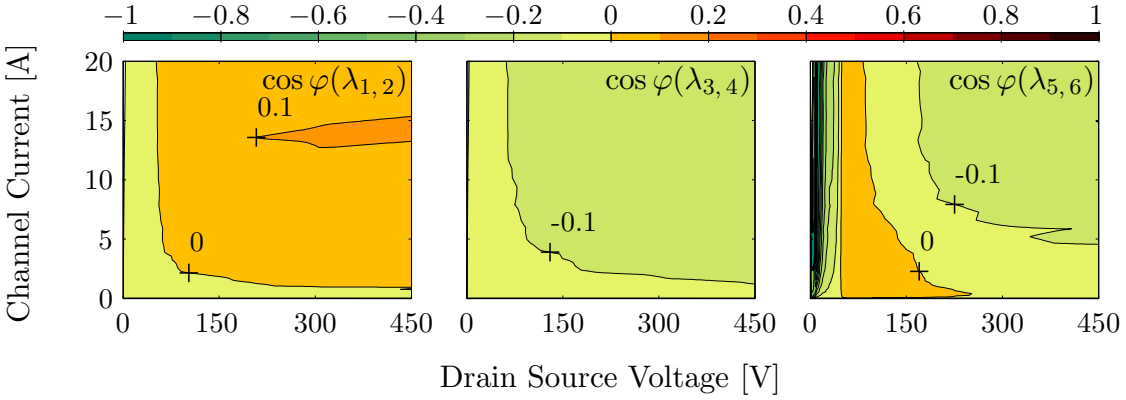
Figure 5.20: Impact of the drain resistance $R_{\mathrm{d\,pac}}$ on the cosine phi's of the conjugate-complex eigenvalues of a buck converter topology's operating points in the MOSFET's operating range



(a) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $-500 \cdot R_{\mathrm{d\,cir}} = -0.94\,\Omega$ with unstable areas in orange



(b) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ of the initial parameterization with unstable areas in orange



(c) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $500 \cdot R_{\mathrm{d\,cir}} = 0.94\,\Omega$ with unstable areas in orange

Figure 5.21: Impact of the drain resistance $R_{\mathrm{d\,cir}}$ on the cosine phi's of the conjugate-complex eigenvalues of a buck converter topology's operating points in the MOSFET's operating range

Impact of the Gate Resistances

The contour plots of the cosine phi's of the conjugate-complex eigenvalues for different $R_{\mathrm{g\,pac}}$ are shown in Fig. 5.22. The corresponding contour plots of the eigenfrequencies are shown in Fig. C.19 on page 209. Fig. 5.22(b) depicts the contour plots of the cosine phi's of the initial parameterization. Fig. 5.22(a) and Fig. 5.22(c) show the contour plots of the cosine phi's of the parameterizations with the fifth part and the fivefold of the initial $R_{\mathrm{g\,pac}}$.[8]

Compared to the corresponding contour plot in Fig. 5.22(b), the unstable area in the contour plot of $\cos\phi(\lambda_{1,2})$ in Fig. 5.22(c) is reduced. In Fig. 5.22(c), the contour plot of $\cos\phi(\lambda_{5,6})$ has no unstable area. Compared to the corresponding plot in Fig. 5.22(b), the cosine phi's in the contour plot of $\cos\phi(\lambda_{3,4})$ are decreased in Fig. 5.22(c) and increased in Fig. 5.22(a). In comparison to the corresponding plots in Fig. 5.22(b), the cosine phi's in the contour plots of $\cos\phi(\lambda_{1,2})$ and $\cos\phi(\lambda_{5,6})$ in Fig. 5.22(a) are increased.

According to Fig. 5.22, the cosine phi's are significantly influenced by $R_{\mathrm{g\,pac}}$. An increase of $R_{\mathrm{g\,pac}}$ improves the stability. Compared to the initial parameterization, for the increased $R_{\mathrm{g\,pac}}$, lower oscillation amplitudes, but increased losses are expected during switching. The higher $R_{\mathrm{g\,pac}}$, the less unstable/the more stable is the commutation cell.

The contour plots of the cosine phi's of the conjugate-complex eigenvalues for different $R_{\mathrm{g\,cir}}$ are shown in Fig. 5.23. The corresponding contour plots of the eigenfrequencies are shown in Fig. C.20 on page 210. Fig. 5.23(b) depicts the contour plots of the cosine phi's of the initial parameterization. Fig. 5.23(a) and Fig. 5.23(c) show the contour plots of the cosine phi's of the parameterizations with the fifth part and the fivefold of the initial $R_{\mathrm{g\,cir}}$.[9]

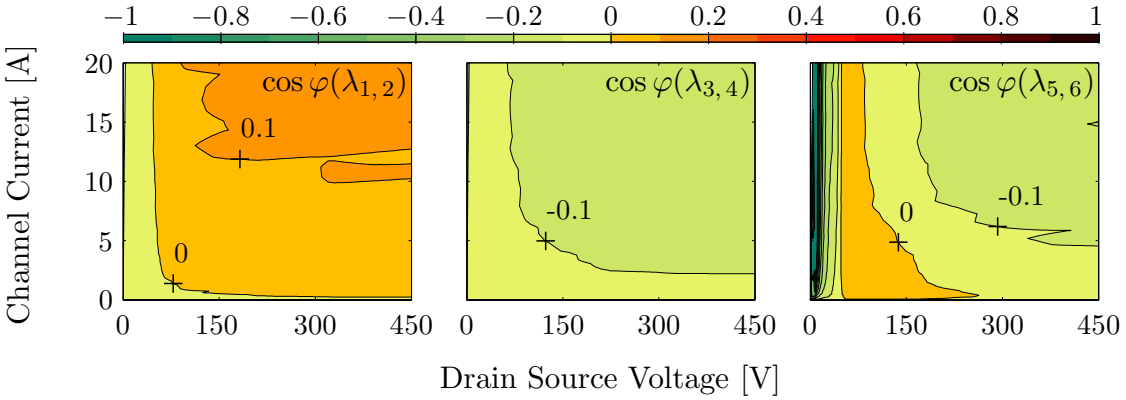
Compared to the corresponding plots in Fig. 5.23(b), the cosine phi's in the contour plots of $\cos\phi(\lambda_{3,4})$ and $\cos\phi(\lambda_{5,6})$ are decreased in Fig. 5.23(c) and increased in Fig. 5.23(a). In Fig. 5.23(c), the contour plot of $\cos\phi(\lambda_{5,6})$ has no unstable area. In comparison to the corresponding plot in Fig. 5.23(b), both the increase and decrease of $R_{\mathrm{g\,cir}}$ result in increased cosine phi's in some areas of the plot of $\cos\phi(\lambda_{1,2})$ in Fig. 5.23(a) and Fig. 5.23(c).

According to Fig. 5.23, the cosine phi's are significantly influenced by $R_{\mathrm{g\,cir}}$. An decrease of the initial $R_{\mathrm{g\,cir}}$ increases the instability of the commutation cell. Compared to the initial parameterization, higher oscillation amplitudes are therefore expected during switching. The lower $R_{\mathrm{g\,cir}}$, the more unstable/the less stable is hence the commutation cell.

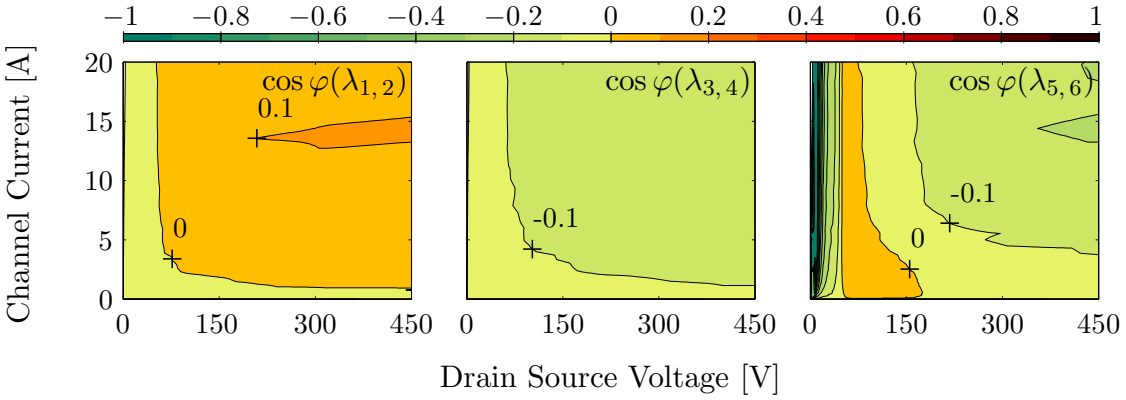
With respect to the stability of commutation cells, an increase of $R_{\mathrm{g\,pac}}$ is more effective than a comparable increase of $R_{\mathrm{g\,cir}}$. For this reason some SJ MOSFETs are in two versions available - one version with a relatively low $R_{\mathrm{G\,int}}$ in order to support applications where highest efficiency and power density are key requirements and another version with a relatively high $R_{\mathrm{G\,int}}$ in order to achieve self-limiting $^{\mathrm{d}i}/_{\mathrm{d}t}$ and $^{\mathrm{d}v}/_{\mathrm{d}t}$ characteristics [Inf 10a].

[8] The effective gate resistance of the interconnections of the PCB and the TO-220 package changes also its sign during switching operation. Due to a $R_{\mathrm{G\,int}}$ of 2.15 Ω, the effective gate resistance $R_{\mathrm{g\,pac}}$ can not become negative during the MOSFET's switching operation.

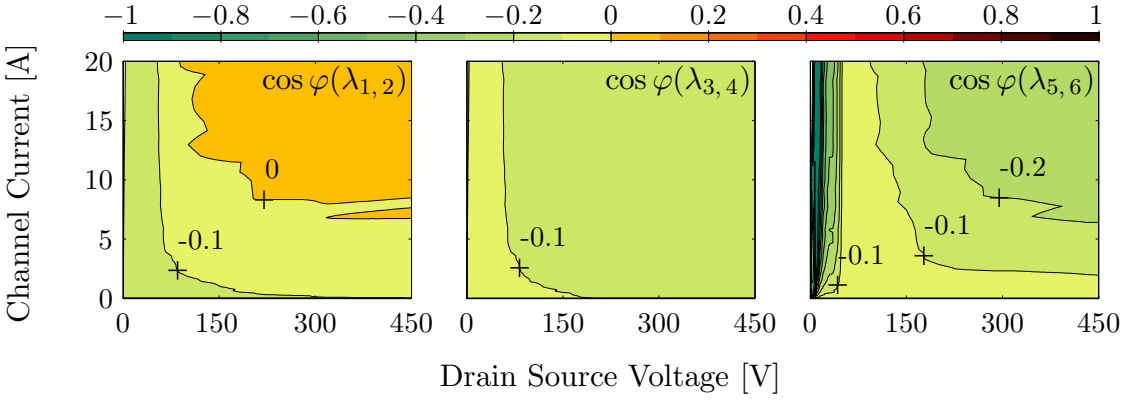
[9] The effective gate resistance of the interconnections of the PCB and the TO-220 package changes also its sign during switching operation. Due to a $R_{\mathrm{G\,ext}}$ of 10 Ω, the effective gate resistance $R_{\mathrm{g\,cir}}$ can not become negative during the MOSFET's switching operation.



(a) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $0.2 \cdot R_{\mathrm{g\,pac}} = 0.432\,\Omega$ with unstable areas in orange

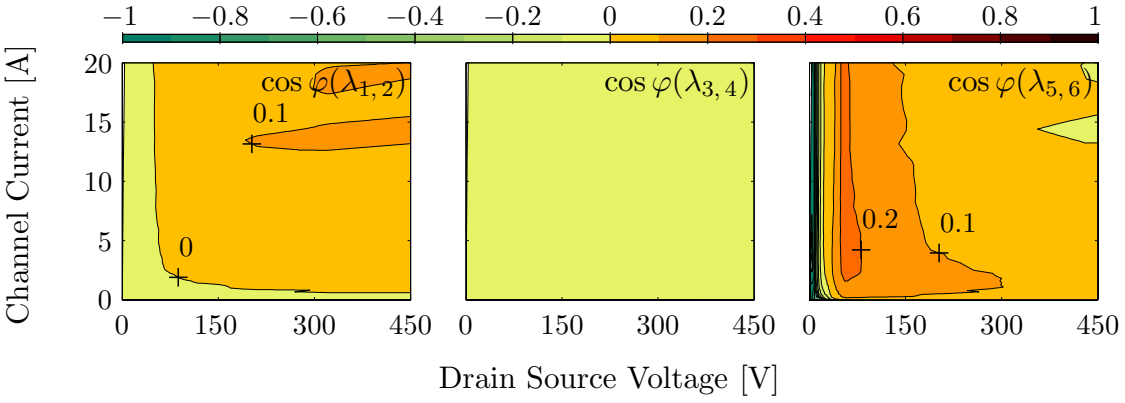


(b) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ of the initial parameterization with unstable areas in orange

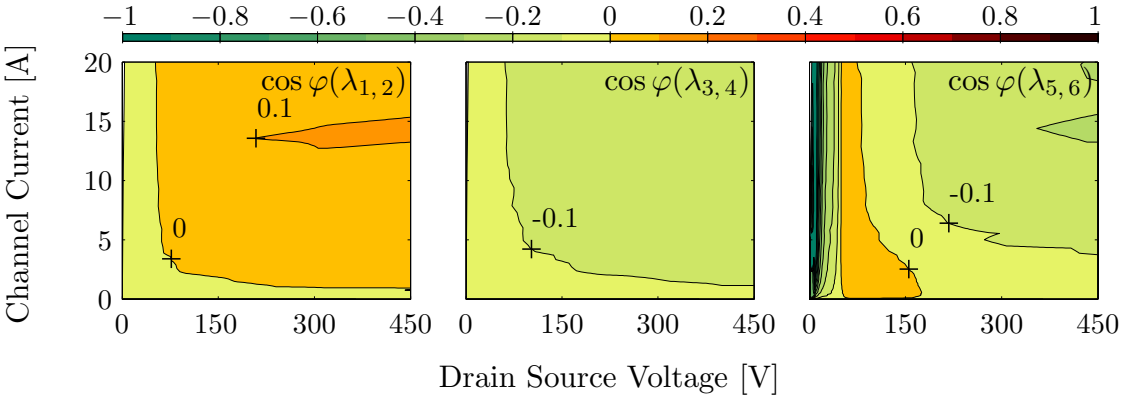


(c) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $5 \cdot R_{\mathrm{g\,pac}} = 10.8\,\Omega$ with unstable areas in orange

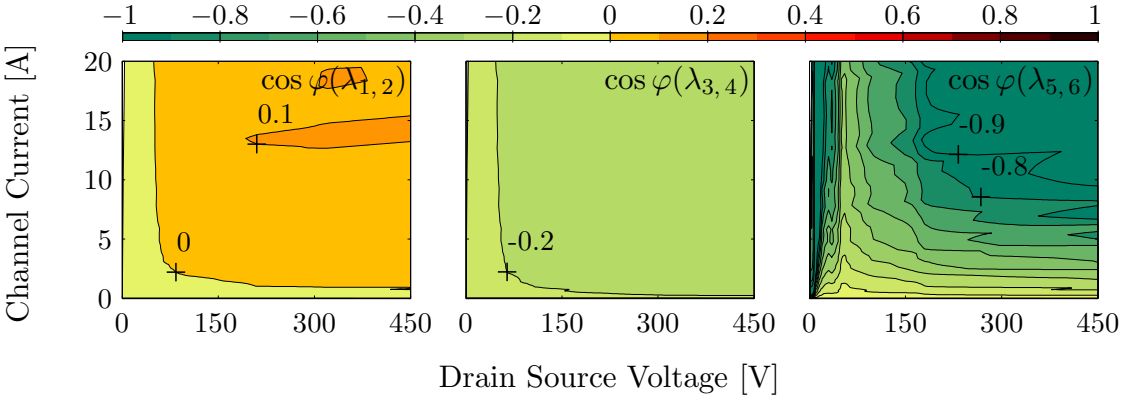
Figure 5.22: Impact of the gate resistance $R_{\mathrm{g\,pac}}$ on the cosine phi's of the conjugate-complex eigenvalues of a buck converter topology's operating points in the MOSFET's operating range



(a) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $0.2 \cdot R_{\mathrm{g\,cir}} = 2.02\,\Omega$ with unstable areas in orange



(b) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ of the initial parameterization with unstable areas in orange



(c) Contour plots of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $5 \cdot R_{\mathrm{g\,cir}} = 50.5\,\Omega$ with unstable areas in orange

Figure 5.23: Impact of the gate resistance $R_{\mathrm{g\,cir}}$ on the cosine phi's of the conjugate-complex eigenvalues of a buck converter topology's operating points in the MOSFET's operating range

Impact of the Source Resistances

The contour plots of the cosine phi's of the conjugate-complex eigenvalues for different $R_{\mathrm{s\,pac}}$ and $R_{\mathrm{s\,cir}}$ are not shown, because the contour plots are not affected by the minus one millionfold and the one millionfold of the initial $R_{\mathrm{s\,pac}}$ and $R_{\mathrm{s\,cir}}$ values. Therewith, the impact of the source resistances on the cosine phi's is found to be insignificant.

5.3 Stability Analysis with a Simplified Small-Signal Equivalent Circuit Model

5.3.1 Simplified Small-Signal Equivalent Circuit Model

The neglect of chip-external capacitances, the neglect of the resistances in the drain and the source current path, and the neglect of the MOSFET's output conductance g_{ds} in Fig. 5.2 on page 114 results in the simplified small-signal equivalent circuit model in Fig. 5.24. This circuit was already known in the nineteen eighties [Severns 85], but the computing technology back then limited a comprehensive analysis. Due to nonlinearity of circuit topologies with power MOSFET, [Severns 85] recommends the analysis of selected operating points. The more recent publications [Fujihira 08] and [Kapels 09] consider also the circuit model in Fig. 5.24, but do not take advantage of the possibilities of nowadays computing technology. [Fujihira 08] and [Kapels 09] analyze solely a not further specified operating point.

The MOSFET's transconductance g_{m} and its capacitances $C_{\mathrm{dg\,chip}}$, $C_{\mathrm{ds\,chip}}$ and $C_{\mathrm{gs\,chip}}$ of the simplified circuit model are defined according to (5.1) through (5.4) on page 112 et seq.. The inductances and the gate resistance are given by

$$L_{\mathrm{d}} = L_{\mathrm{d\,pac}} + L_{\mathrm{d\,cir}}, \tag{5.24}$$

$$L_{\mathrm{g}} = L_{\mathrm{g\,pac}} + L_{\mathrm{g\,cir}} \text{ and} \tag{5.25}$$

$$L_{\mathrm{s}} = L_{\mathrm{s\,pac}} + L_{\mathrm{s\,cir}}, \tag{5.26}$$

$$R_{\mathrm{g}} = R_{\mathrm{g\,pac}} + R_{\mathrm{g\,cir}}. \tag{5.27}$$

The simplified equivalent circuit model is described by the equation system

$$\dot{\vec{x}} = \boldsymbol{A} \cdot \vec{x} \tag{5.28}$$

with the state space vector

$$\vec{x} = \left[\Delta I_{\mathrm{D}},\ \Delta I_{\mathrm{G}},\ \Delta V_{\mathrm{DS\,chip}},\ \Delta V_{\mathrm{GS\,chip}}\right]^{\mathrm{T}}, \tag{5.29}$$

the time-derived state space vector

$$\dot{\vec{x}} = \left[\Delta \dot{I}_{\mathrm{D}},\ \Delta \dot{I}_{\mathrm{G}},\ \Delta \dot{V}_{\mathrm{DS\,chip}},\ \Delta \dot{V}_{\mathrm{GS\,chip}}\right]^{\mathrm{T}} \tag{5.30}$$

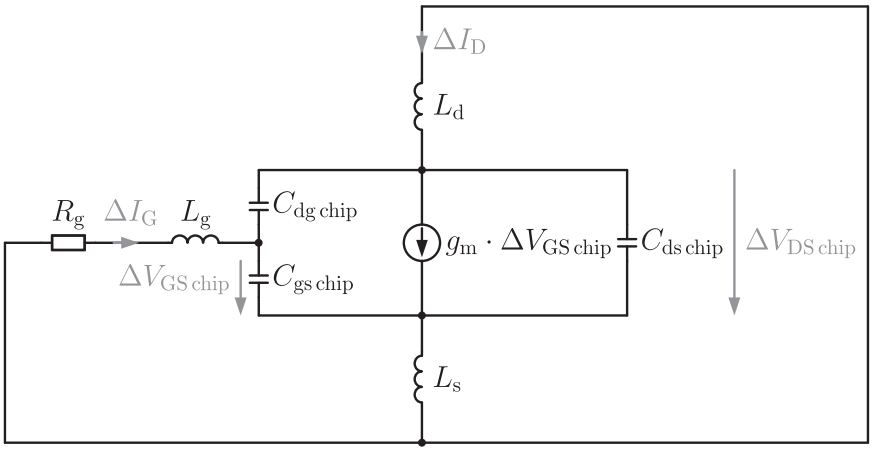


Figure 5.24: Simplified small-signal equivalent circuit model of a buck converter topology's operating points

Table 5.5: Elements of the system matrix of the simplified small-signal equivalent circuit model in Fig. 5.24

a_{ij}	**Calculation of** a_{ij}	a_{ij}	**Calculation of** a_{ij}
$a_{1\,1}$	0	$a_{3\,1}$	$-C_\mathrm{dg\,chip}/CC_\mathrm{chip}$
$a_{1\,2}$	$L_\mathrm{s} \cdot R_\mathrm{g}/LL$	$a_{3\,2}$	$-(C_\mathrm{dg\,chip}+C_\mathrm{ds\,chip})/CC_\mathrm{chip}$
$a_{1\,3}$	$L_\mathrm{g}+L_\mathrm{s}/LL$	$a_{3\,3}$	0
$a_{1\,4}$	$-L_\mathrm{s}/LL$	$a_{3\,4}$	$-C_\mathrm{dg\,chip} \cdot g_\mathrm{m}/CC_\mathrm{chip}$
$a_{2\,1}$	0	$a_{4\,1}$	$-(C_\mathrm{dg\,chip}+C_\mathrm{ds\,chip})/CC_\mathrm{chip}$
$a_{2\,2}$	$-R_\mathrm{g} \cdot (L_\mathrm{d}+L_\mathrm{s})/LL$	$a_{4\,2}$	$-C_\mathrm{dg\,chip}/CC_\mathrm{chip}$
$a_{2\,3}$	$-L_\mathrm{s}/LL$	$a_{4\,3}$	0
$a_{2\,4}$	$L_\mathrm{d}+L_\mathrm{s}/LL$	$a_{4\,4}$	$-(C_\mathrm{dg\,chip}+C_\mathrm{gs\,chip}) \cdot g_\mathrm{m}/CC_\mathrm{chip}$

and the system matrix $\boldsymbol{A}$. The matrix elements a_{ij} are presented in Table 5.5 with

$$LL = L_\mathrm{g} \cdot L_\mathrm{s} + L_\mathrm{d} \cdot L_\mathrm{g} + L_\mathrm{s} \cdot L_\mathrm{d} \text{ and} \tag{5.31}$$

$$CC_\mathrm{chip} = C_\mathrm{dg\,chip} \cdot C_\mathrm{ds\,chip} + C_\mathrm{gs\,chip} \cdot C_\mathrm{dg\,chip} + C_\mathrm{ds\,chip} \cdot C_\mathrm{gs\,chip}. \tag{5.32}$$

The determination of $\boldsymbol{A}$ is described in the appendix in section **B.2** on page 188 et seq..

The four solutions of $|\boldsymbol{A} - \lambda \cdot \boldsymbol{I}| = 0$ are the eigenvalues of $\boldsymbol{A}$. Conclusions that can be drawn from the eigenvalues of a linear system are in summarized in Table 5.2 on page 117.

5.3.2 Analysis of Operating Points of a Buck Converter Topology

The eigenvalues of the operating points of a buck converter topology are determined in the operating range of the regarded SJ MOSFET by means of the *MATLAB* & *Simulink* function 'eig'. Thereby, the values in Table 5.6 are used for the parameterization of the operating point independent circuit elements in Fig. 5.24. The calculation of the operating point dependent circuit elements is based on the 25 °C output characteristics in Fig. 2.19 on page 38 and the 'dynamic' capacitances in Fig. 4.2 on page 100. One conjugate-complex eigenvalue pair and two negative real eigenvalues exist in the regarded operating range.

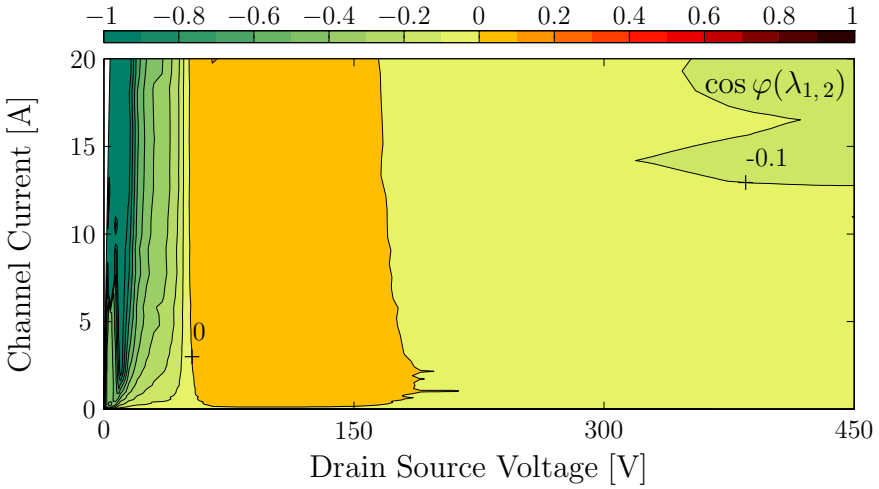
For the conjugate-complex eigenvalues, the cosine phi's and the eigenfrequencies are calculated according to (5.22) and (5.23) on page 116 et seq.. The results are shown in Fig. 5.25. The contour plots of $\cos\phi(\lambda_{1,2})$ and $f_0(\lambda_{1,2})$ in Fig. 5.25 are very similar to the contour plots of $\cos\phi(\lambda_{5,6})$ and $f_0(\lambda_{5,6})$ in Fig. 5.3 on page 118. The simulated switching characteristics in Fig. 4.3 on page 102 et seq. correspond to the results of the simplified stability analysis in Fig. 5.25. In Fig. A.1 on page 178, the simulated characteristics $i_{\mathrm{D\,cir}}$, $i_{\mathrm{G\,cir}}$, $v_{\mathrm{DS\,ext}}$ and $v_{\mathrm{GS\,ext}}$ are shown additionally to i_{Ch}, $i_{\mathrm{D\,pac}}$, $i_{\mathrm{G\,pac}}$, $v_{\mathrm{DS\,chip}}$ and $v_{\mathrm{GS\,chip}}$. The frequencies of the oscillating part of the $v_{\mathrm{DS\,ext}}$ in Fig. A.1(a) and Fig. A.1(b) are determined by means of a FOURIER analysis. The results are depicted in Fig. A.2 on page 182. The lower frequency band in Fig. A.2 correspond well with the eigenfrequencies in Fig. 5.25(b). However, oscillations corresponding to the other conjugate-complex eigenvalues can also occur in the buck converter topology. In Fig. A.2, the amplitudes, which correspond to the frequencies of the conjugate-complex eigenvalues $\lambda_{3,4}$ in Fig. 5.3, are small compared to the amplitudes, which correspond to the frequencies of the conjugate-complex eigenvalues $\lambda_{5,6}$ in Fig. 5.3. This is because the dwell time in areas with positive $\cos\phi(\lambda_{3,4})$ is small compared to the periods of the corresponding eigenfrequencies $f_0(\lambda_{3,4})$.

In Fig. 5.28 on page 164, the FOURIER analysis of switching characteristics in Fig. 5.26 on page 157 et seq. shows that higher eigenfrequencies can become dominant. The dwell time in areas with positive cosine phi's $\cos\phi(\lambda_{1,2})$ is large compared to the periods of the eigenfrequencies $f_0(\lambda_{1,2})$. With the simplified model in Fig. 5.24, not all frequency ranges of parasitic oscillations can be predicted. Therefore, the analysis of the stability of commutation cells is not reliable with the simplified circuit model.

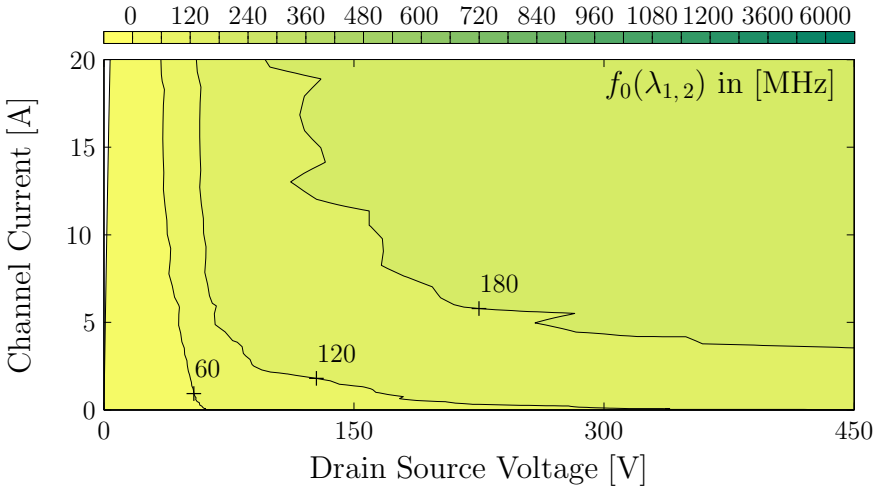
As the contour plots in subsection **5.2.3** on page 117 et seq. and in subsection **5.2.4** on page 119 et seq., the contour plots in Fig. 5.25 make clear that the analysis of a single operating point - as in [Fujihira 08] and [Kapels 09] - is not sufficient for the analysis of the stability of commutation cells. Even the analysis of selected operating points - as proposed in [Severns 85] - might be insufficient. For a meaningful stability analysis, the MOSFET's operating range of interest needs to be analyzed.

Table 5.6: Parameterization of operating point independent circuit elements of the buck converter's simplified small-signal equivalent circuit model

Inductance	Value	Resistance	Value	Capacitance	Value
L_d	40.97 nH	R_g	12.17 Ω	$C_{\mathrm{gs\,chip}}$	1.47 nF
L_g	4.18 nH				
L_s	4.99 nH				



(a) Contour plot of the cosine phi's of the conjugate-complex eigenvalues $\lambda_{1,2}$



(b) Contour plot of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$

Figure 5.25: Results of the simplified stability analysis of a buck converter topology's operating points in the MOSFET's operating range

5.4 Stability Analysis versus Switching Behavior

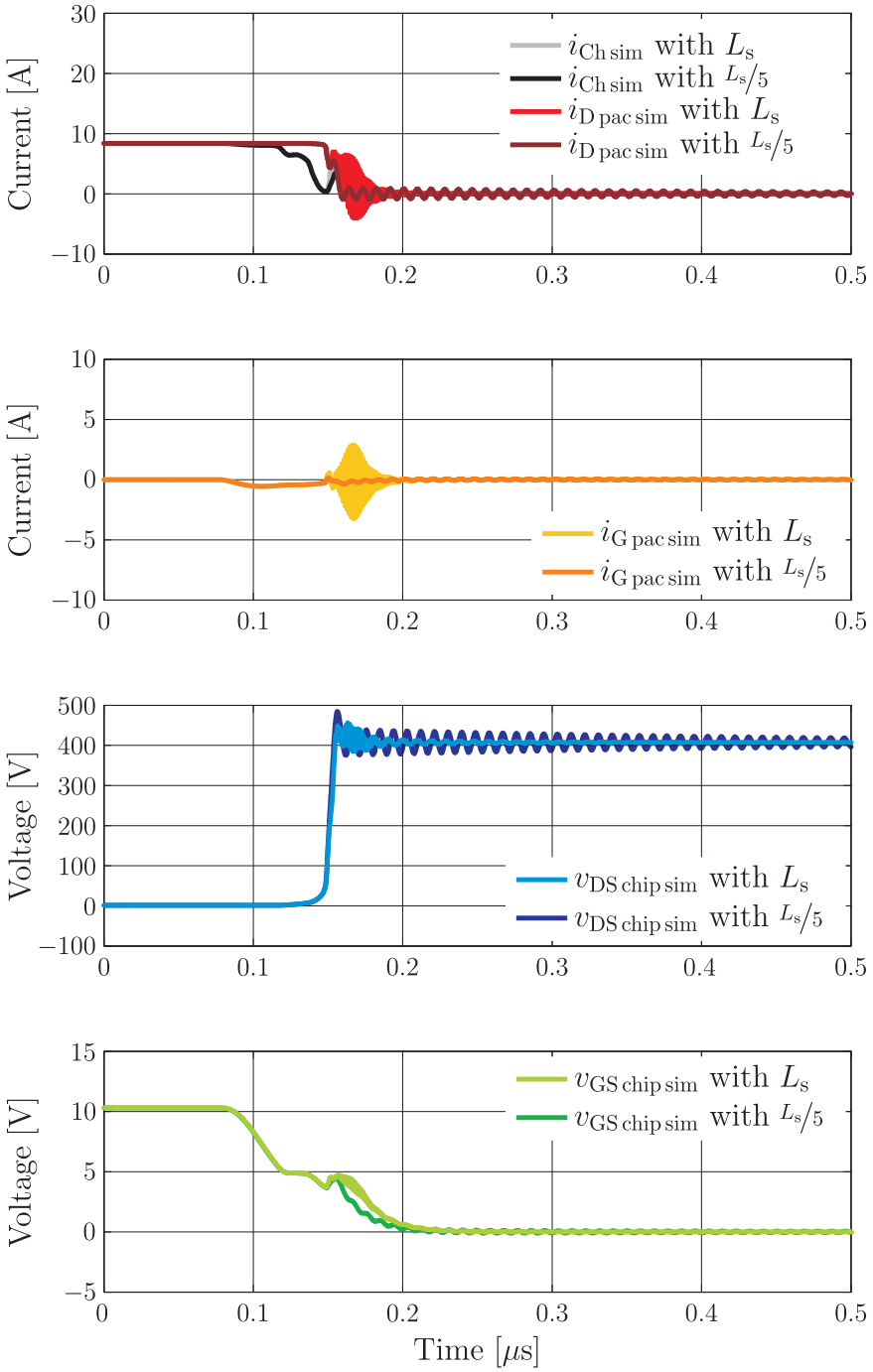
5.4.1 Prediction of Oscillations with Temporarily Increasing Amplitudes

As discussed at the end of subsection **5.2.3** on page 119, the positive cosine phi's in the contour plots of the conjugate-complex eigenvalues are probably only the necessary condition for oscillations with temporarily increasing amplitudes. The way of the $i_{\mathrm{Ch}}(v_{\mathrm{DS\,chip}})$ locus curves through areas with positive cosine phi's and the dwell time in these areas determine if the sufficient condition for oscillations with temporarily increasing amplitudes is satisfied or not. For a given buck converter circuit, infinite locus curves through the $I_{\mathrm{Ch}}(V_{\mathrm{DS\,chip}})$ plane exist due to infinite possibilities for the parameterization of the DC link voltage, the driver voltage and the load current. It is not possible to analyze the correlation of the switching behavior and the stability analysis for all possible trajectories. Parameters, which determine if the sufficient condition for oscillations with temporarily increasing amplitudes is satisfied or not, are also not further investigated in this work. Instead, the significance of stability analysis is exemplified with a few switching characteristics:

The switching characteristics are shown in Fig. 5.26. They are simulated with the circuit in Fig. 3.13 on page 91. L_{Dio} and R_{Dio} are parameterized with the values in Table 3.11 on page 93. $L_{\mathrm{d\,cir}}$ and $R_{\mathrm{d\,cir}}$ in Table 5.4 on page 123 are accordingly reduced for the parameterization of $L_{\mathrm{D\,cir}}$ and $R_{\mathrm{D\,cir}}$. The 'L_{s}' characteristics correspond to the circuit parameters used for the contour plots in Fig. 5.19(b) on page 145 and Fig. C.16(b) on page 206. The '$L_{\mathrm{s}}/5$' characteristics correspond to the circuit parameters used for the contour plots in Fig. 5.19(a) on page 145 and Fig. C.16(a) on page 206.

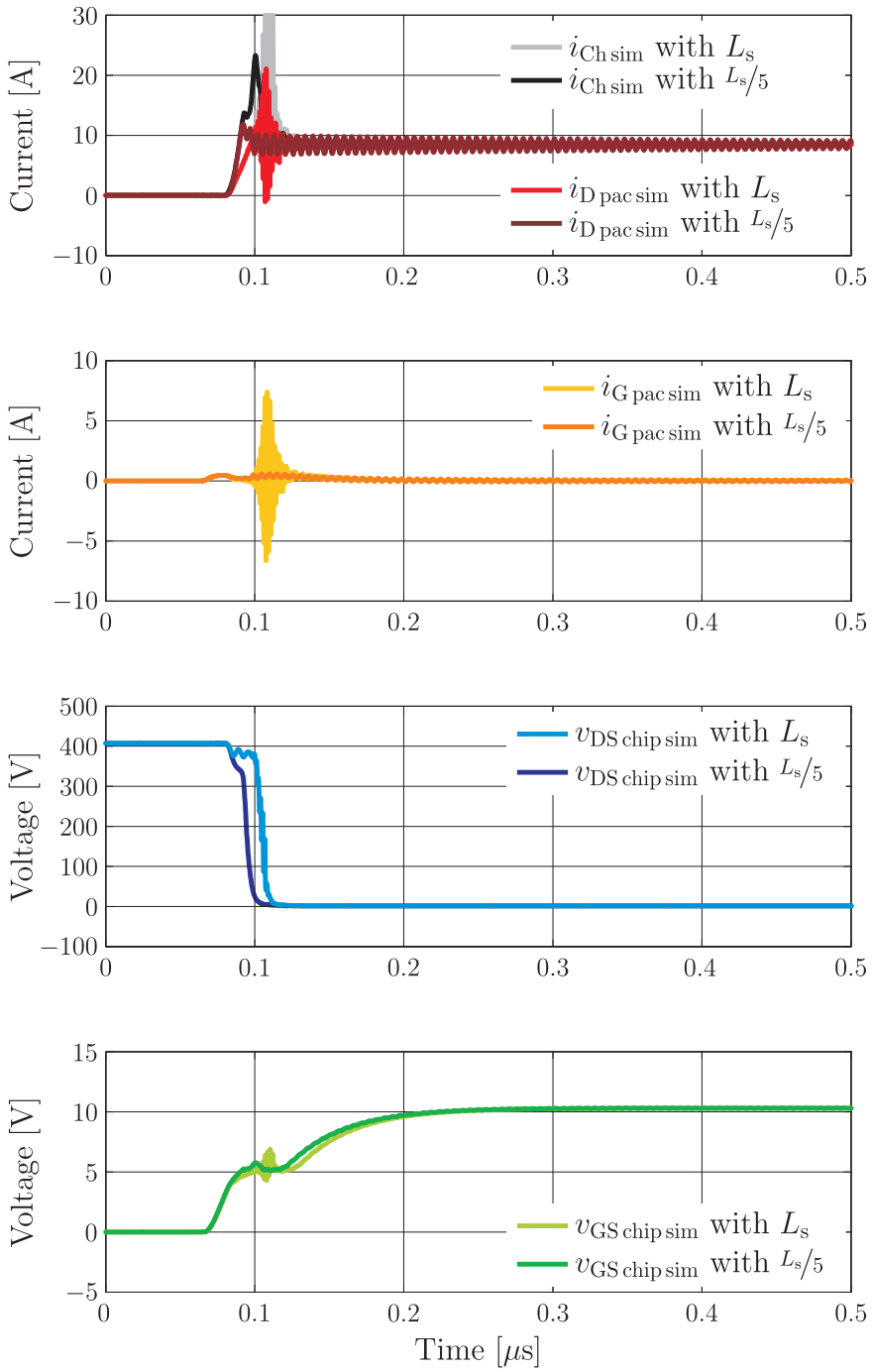
Due to the results in Fig. 5.19(a), oscillations with temporarily increasing amplitudes are not expected in the '$L_{\mathrm{s}}/5$' characteristics. The oscillation amplitudes, which correspond to the contour plots of $f_0(\lambda_{3,4})$ and $f_0(\lambda_{5,6})$ in Fig. C.16(a) are expected to be small compared to the oscillation amplitudes, which correspond to the contour plot of $f_0(\lambda_{1,2})$. Due to the results in Fig. 5.19(b), oscillations with temporarily increasing amplitudes are expected in the 'L_{s}' characteristics. The oscillation amplitudes, which correspond to the contour plot of $f_0(\lambda_{1,2})$ in Fig. C.16(b) are expected to be high compared to the oscillation amplitudes, which correspond to the contour plot of $f_0(\lambda_{5,6})$. Furthermore, the smaller source inductances decrease the feedback in the gate circuit during source current alterations. Hence, an increased drain current slope and decreased switching times and losses are expected for the parameterization with reduced $L_{\mathrm{S\,pac}}$ and $L_{\mathrm{S\,cir}}$.

The characteristics in Fig. 5.26(a) and Fig. 5.26(b) confirm the expectations. The 'L_{s}' characteristics have oscillations with temporarily increasing amplitudes. The oscillations in the '$L_{\mathrm{s}}/5$' characteristics have solely decreasing oscillation amplitudes. In Fig. 5.26(a) and Fig. 5.26(b), the oscillation amplitudes of the 'L_{s}' characteristics are relatively small. In Fig. 5.27, the corresponding characteristics $i_{\mathrm{D\,cir}}$, $i_{\mathrm{G\,cir}}$, $v_{\mathrm{DS\,ext}}$ and $v_{\mathrm{GS\,ext}}$ are depicted. The 'probing points' of the different currents and voltages are indicated in Fig. 3.13 on page 91 and Fig. 2.7 on page 19. Fig. 5.27 shows that the oscillation amplitudes of the voltage



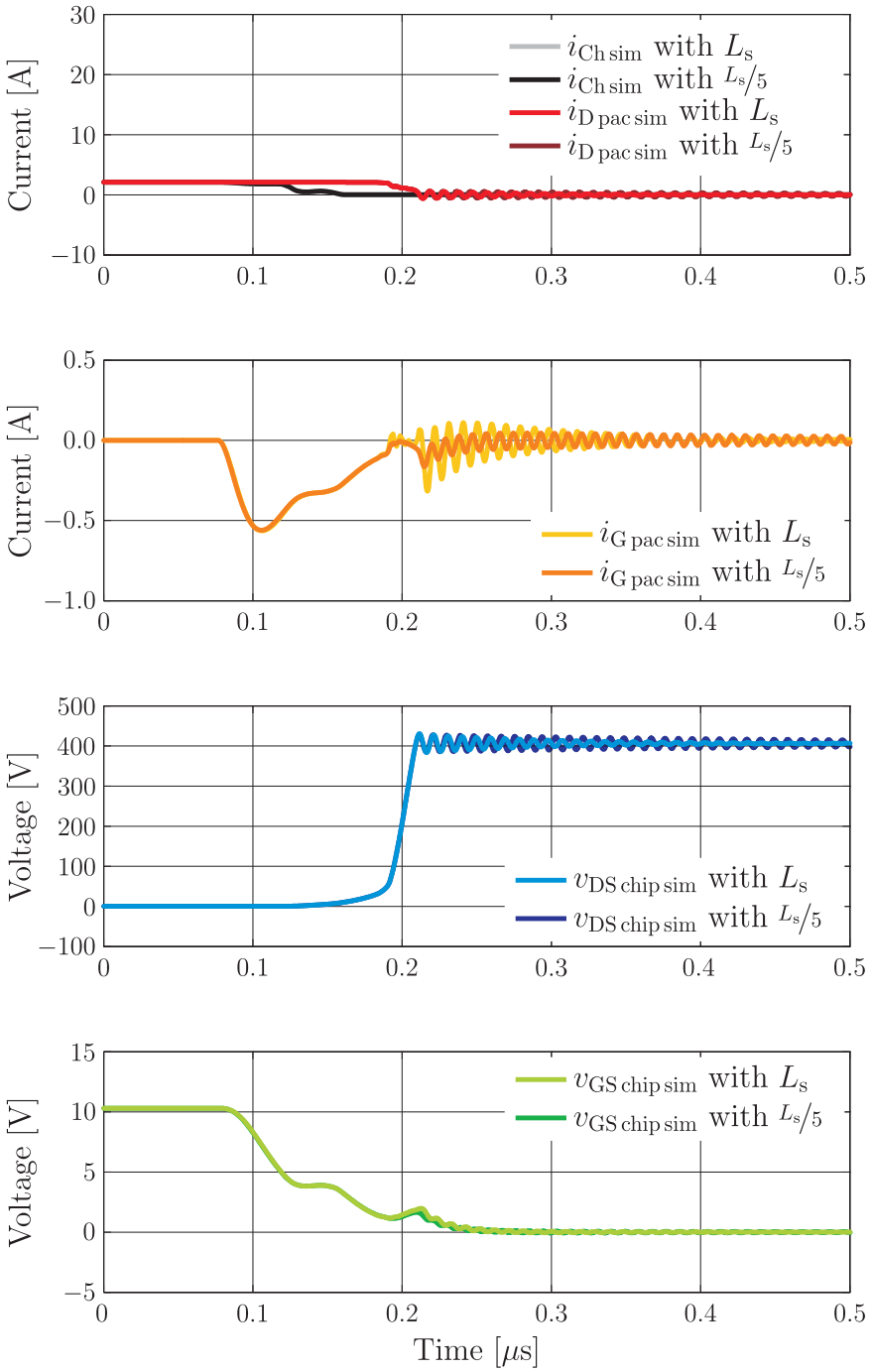
(a) Turn-off characteristics with $R_{\mathrm{G\,ext}} = 10\,\Omega$, $V_{\mathrm{DClink}} = 400\,\mathrm{V}$, $i_{\mathrm{L}} = 8\,\mathrm{A}$ and $\vartheta_{\mathrm{J}} = 25\,^{\circ}\mathrm{C}$

Figure 5.26: Impact of the source inductances $L_{\mathrm{s\,pac}}$ and $L_{\mathrm{s\,cir}}$ on simulated switching characteristics



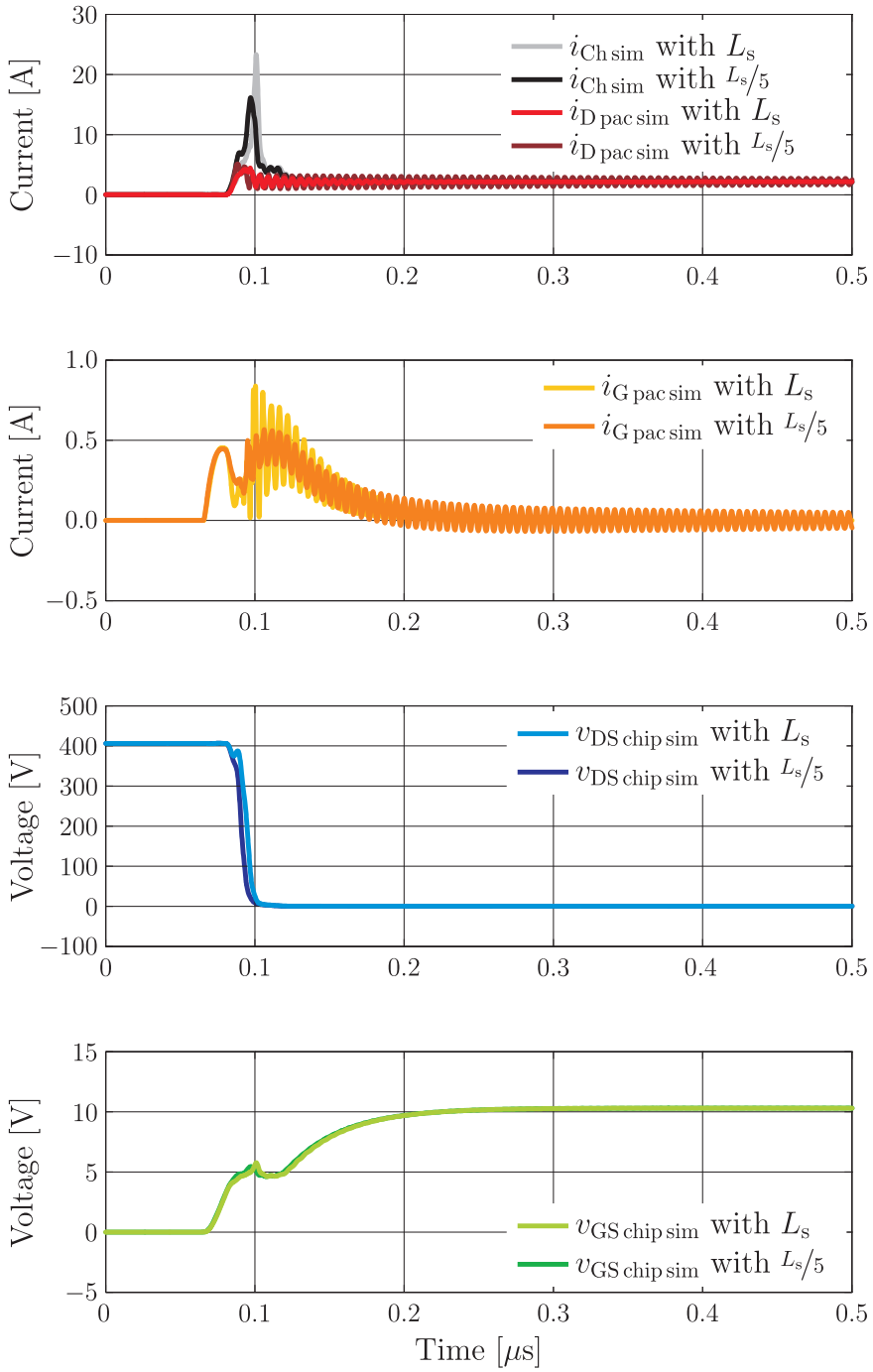
(b) Turn-on characteristics with $R_{\mathrm{G\,ext}} = 10\,\Omega$, $V_{\mathrm{DClink}} = 400\,\mathrm{V}$, $i_{\mathrm{L}} = 8\,\mathrm{A}$ and $\vartheta_{\mathrm{J}} = 25\,^{\circ}\mathrm{C}$

Figure 5.26: Impact of the source inductances $L_{\mathrm{s\,pac}}$ and $L_{\mathrm{s\,cir}}$ on simulated switching characteristics (cont.)



(c) Turn-off characteristics with $R_{\mathrm{G\,ext}} = 10\,\Omega$, $V_{\mathrm{DClink}} = 400\,\mathrm{V}$, $i_{\mathrm{L}} = 2\,\mathrm{A}$ and $\vartheta_{\mathrm{J}} = 25\,^{\circ}\mathrm{C}$

Figure 5.26: Impact of the source inductances $L_{\mathrm{s\,pac}}$ and $L_{\mathrm{s\,cir}}$ on simulated switching characteristics (cont.)



(d) Turn-on characteristics with $R_{\mathrm{G\,ext}} = 10\,\Omega$, $V_{\mathrm{DClink}} = 400\,\mathrm{V}$, $i_{\mathrm{L}} = 2\,\mathrm{A}$ and $\vartheta_{\mathrm{J}} = 25\,^{\circ}\mathrm{C}$

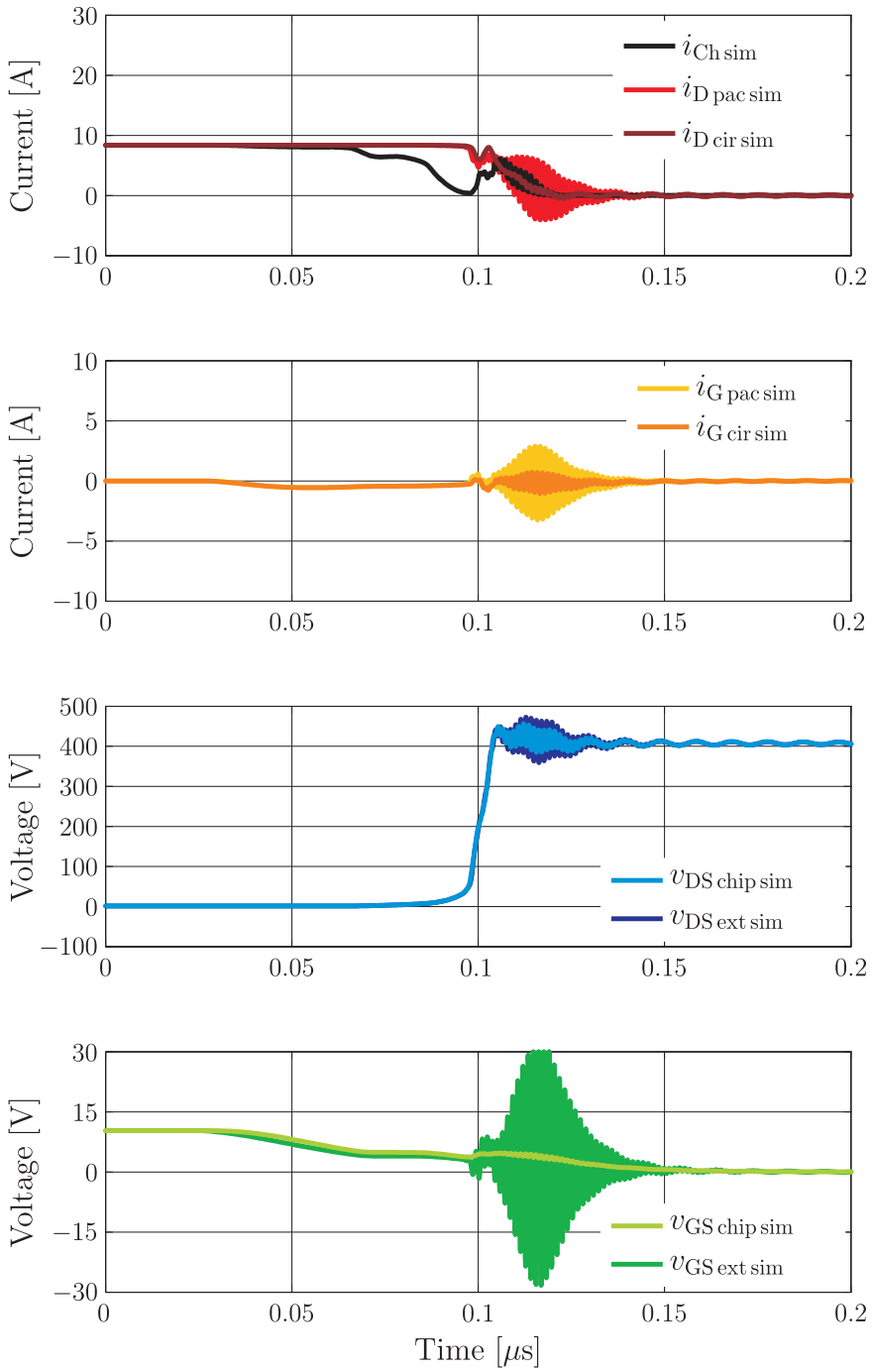
Figure 5.26: Impact of the source inductances $L_{\mathrm{s\,pac}}$ and $L_{\mathrm{s\,cir}}$ on simulated switching characteristics (cont.)

signals increase significantly with distance to the semiconductor chip while the oscillation amplitudes of the current signals decrease with distance to the chip. The results of a frequency analysis of the oscillating part of the gate current characteristics in Fig. 5.26(a) and Fig. 5.26(b) are shown in Fig. 5.28. The spectra correlate well with the eigenfrequencies in the contour plots in Fig. C.16(a) and Fig. C.16(b). Differences are probably due to the restricted resolution of the subthreshold region and the linear region in the $I_{\mathrm{Ch}}(V_{\mathrm{DS\,chip}})$ plane. The expectations regarding the oscillation amplitudes of the different frequency components are also met. As predicted, the reduction of $L_{\mathrm{S\,pac}}$ and $L_{\mathrm{S\,cir}}$ results in reduced switching times and losses.

Compared to the switching characteristics with $i_{\mathrm{L}} = 8\,\mathrm{A}$ in Fig. 5.26(a) and Fig. 5.26(b), the differences between the 'L_{s}' and the '$L_{\mathrm{s}}/5$' characteristics with $i_{\mathrm{L}} = 2\,\mathrm{A}$ in Fig. 5.26(c) and Fig. 5.26(d) are marginal. In the 'L_{s}' characteristics, the expected oscillations with temporarily increasing amplitudes are not or hardly visible. In Fig. 5.26(c), most of the commutation time, the gate source voltage is below or only slightly above the threshold voltage. Hence, the channel current is very small or zero during voltage and current commutation. The unstable areas in the contour plots of $\cos\phi(\lambda_{1,2})$ and $\cos\phi(\lambda_{5,6})$ in Fig. 5.19(b) are not run through by the $i_{\mathrm{Ch}}(v_{\mathrm{DS\,chip}}, /, v_{\mathrm{GS\,chip}})$ locus curves. The 'L_{s}' characteristics in Fig. 5.26(c) have therefore no oscillations with temporarily increasing amplitudes. In Fig. 5.26(d), oscillations with temporarily increasing amplitudes occur only briefly in the gate current characteristics. Before the oscillation amplitudes could build up, the unstable areas in the contour plots of $\cos\phi(\lambda_{1,2})$ and $\cos\phi(\lambda_{5,6})$ in Fig. 5.19(b) are left.

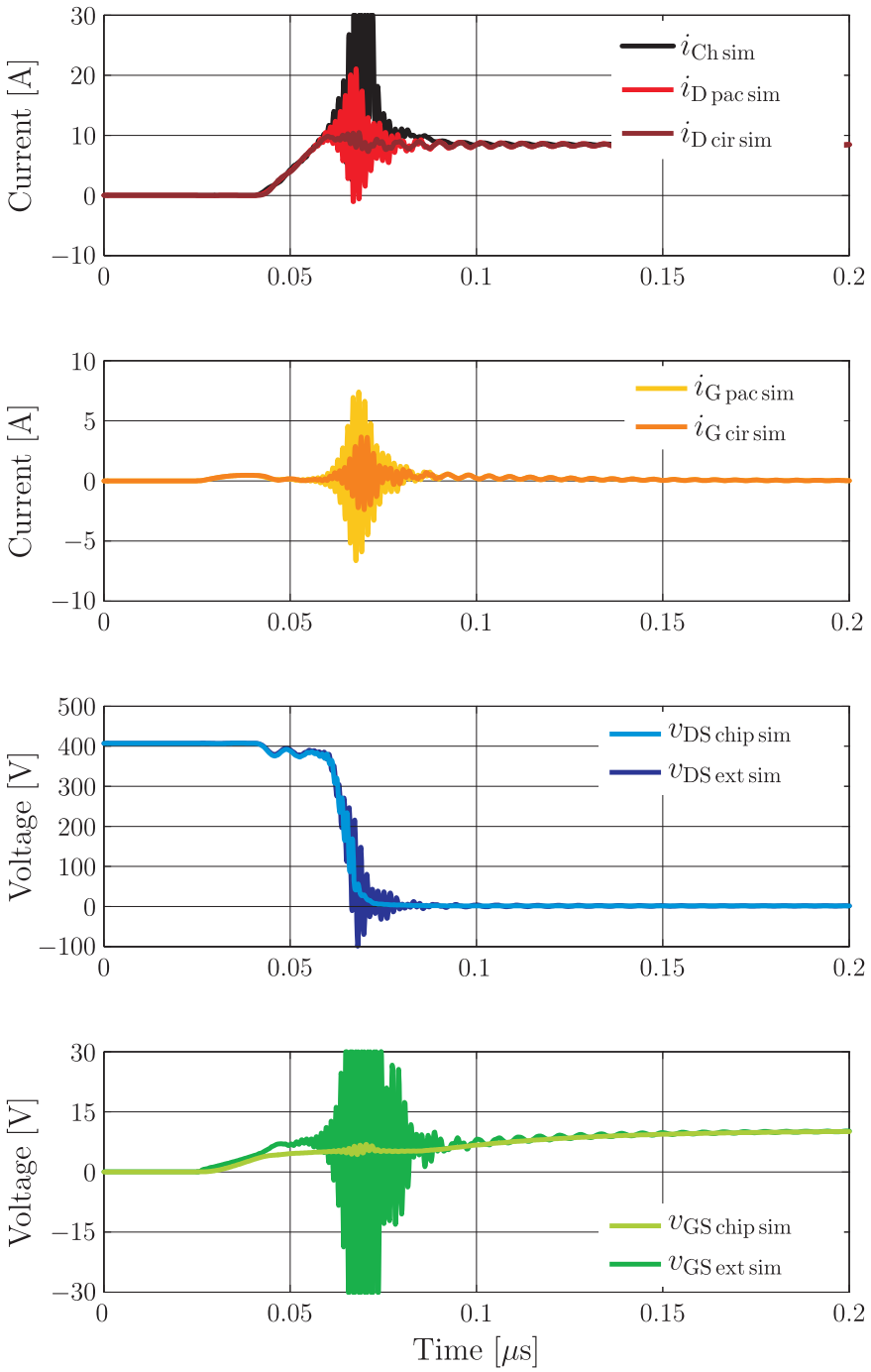
In summary, the switching characteristics in Fig. 5.26 exemplify ...

- ... that the results of the oscillation analysis on the basis of the small-signal equivalent circuit model in Fig. 5.2 on page 114 represent the stability of the nonlinear commutation circuit, ...
- ... that $i_{\mathrm{Ch}}(v_{\mathrm{DS\,chip}})$ locus curves must be considered additionally to the stability analysis in order to predict oscillations with temporarily increasing amplitudes, ...
- ... that the dwell time in unstable areas influences the development of oscillations with temporarily increasing amplitudes, ...
- ... that - independent from the circuit parameterization - the stability is given for zero voltage and zero current switching operations, ...
- ... that the optimization of some circuit parameters improve both the efficiency and the stability of commutation cells, and ...
- ... that both an optimized circuit topology and optimized power devices are required in order to achieve highest efficiency of power conversion.



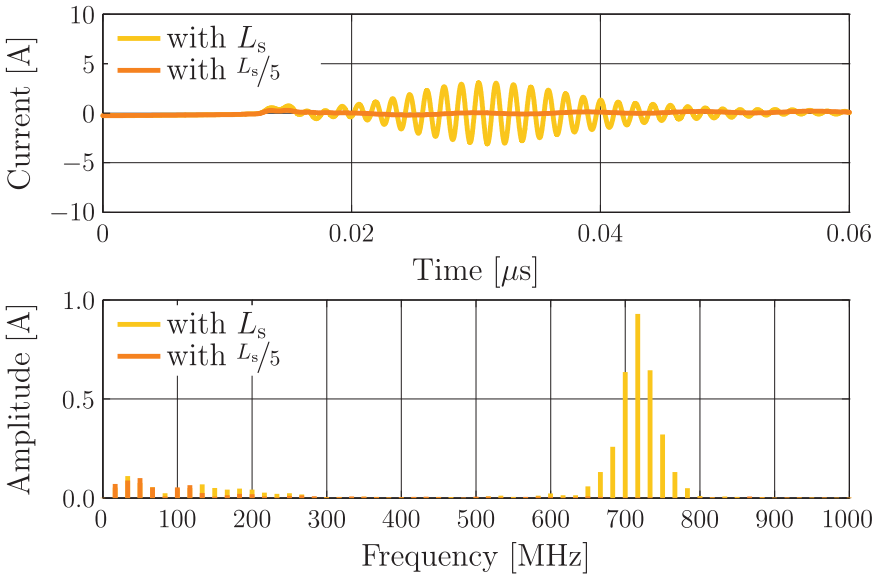
(a) Turn-off characteristics with $R_{\mathrm{G\,ext}} = 10\,\Omega$, $V_{\mathrm{DClink}} = 400\,\mathrm{V}$, $i_{\mathrm{L}} = 8\,\mathrm{A}$ and $\vartheta_{\mathrm{J}} = 25\,^{\circ}\mathrm{C}$

Figure 5.27: Comparison of the 'L_{s}' chip characteristics in Fig. 5.26(a) and Fig. 5.26(b) with the corresponding circuit characteristics

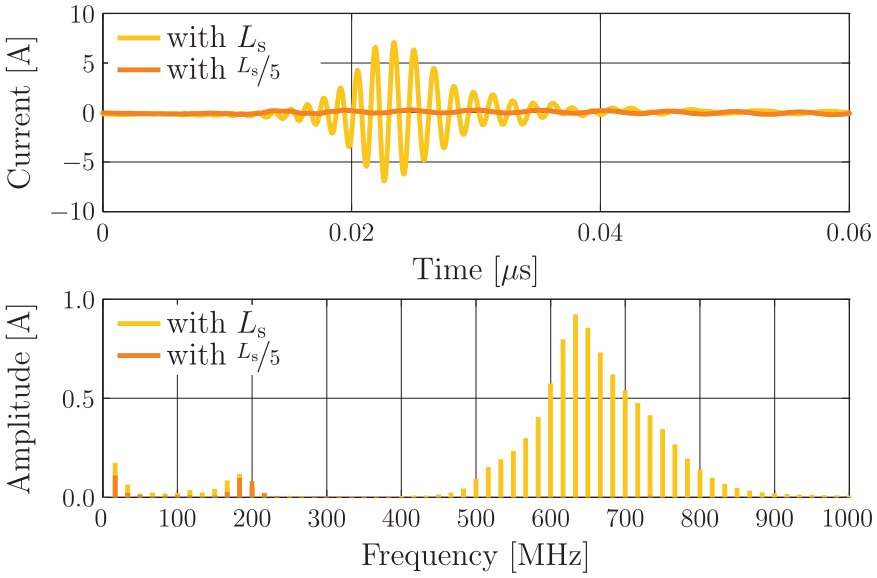


(b) Turn-on characteristics with $R_{\mathrm{G\,ext}} = 10\,\Omega$, $V_{\mathrm{DClink}} = 400\,\mathrm{V}$, $i_{\mathrm{L}} = 8\,\mathrm{A}$ and $\vartheta_{\mathrm{J}} = 25\,^{\circ}\mathrm{C}$

Figure 5.27: Comparison of the 'L_{s}' chip characteristics in Fig. 5.26(a) and Fig. 5.26(b) with the corresponding circuit characteristics (cont.)



(a) AC component of a detail of the simulated gate currents in Fig. 5.26(a) (top) and the accordant frequency spectra (bottom)



(b) AC component of a detail of the simulated gate currents in Fig. 5.26(b) (top) and the accordant frequency spectra (bottom)

Figure 5.28: Frequency spectra of the oscillating part of the gate current characteristics in Fig. 5.26(a) and Fig. 5.26(b)

5.4.2 Evaluation of the Stability Analysis

The previous subsection exemplifies that the results of the stability analysis of the buck converter's subsidiary systems enable conclusions on large-signals and switching characteristics respectively. Oscillations with temporarily increasing amplitudes can be predicted by means of the presented stability analysis as long as the dwell time in unstable areas of the $I_{\mathrm{Ch}}(V_{\mathrm{DS\,chip}})$ plane is large compared to the periods of the eigenfrequencies of the corresponding subsidiary systems. Thereby, the stability analysis itself does not contain any information about typical $i_{\mathrm{Ch}}(v_{\mathrm{DS\,chip}})$ locus curves, which are not only determined by the equivalent circuit elements but also by the DC link voltage, the driver voltage and the load current. Hence, additionally to the stability analysis, the simulation of typical switching characteristics can be helpful. The presented analysis is based on simplifications. Some are subsequently discussed:

A behavioral model of a ***Schottky diode*** is shown in Fig. 2.11 on page 25. In Fig. 5.2 on page 114, the SCHOTTKY diode is represented by a short circuit. Measurements have shown, the oscillation behavior during switching operations depends on the used freewheeling diode. The equivalent circuit elements of a SCHOTTKY diode have an impact on the $i_{\mathrm{Ch}}(v_{\mathrm{DS\,chip}})$ locus curve. This is one reason why the freewheeling diode may influence the oscillation behavior during switching. The simulation of switching characteristics with differently parameterized $C_{\mathrm{AC\,chip}}$ and $R_{\mathrm{AC\,chip}}$ enable the analysis of this aspect. The consideration of $C_{\mathrm{AC\,chip}}$ and $R_{\mathrm{AC\,chip}}$ in the small-signal equivalent circuit model in Fig. 5.2 would result in an additional eigenvalue. With the additional eigenvalue, up to four conjugate-complex eigenvalues and thus, up to four eigenfrequencies are possible. Future works should analyze the impact of the additional eigenvalue on the conjugate-complex eigenvalues.

The ***junction temperature*** is disregarded in (5.1) on page 112. For the consideration of the temperature, the circuit model in Fig. 5.2 on page 114 would be coupled with a thermal circuit. For the temperature calculation, the dissipated power must be determined by a multiplication of $\Delta V_{\mathrm{DS\,chip}}$ and $\Delta I_{\mathrm{Ch}}(V_{\mathrm{DS\,chip}}, V_{\mathrm{GS\,chip}})$. Due to the multiplication, it is not possible to convert the system into $\dot{\vec{x}} = \boldsymbol{A} \cdot \vec{x}$, and the presented methodology can not be applied to the extended circuit model. However, the influence of a single switching period on the mean junction temperature is negligible. Accordingly, the neglect of T_{J} should be a reasonable simplification for the analysis of the stability during switching operations.

In subsection **5.3** on page 152 et seq., it is concluded that the simplified circuit model in Fig. 5.24 on page 153 is not sufficient for the analysis of the stability. Compared to the circuit model in Fig. 5.2 on page 114, ***more complex circuit models*** might enhance stability analysis. However, the small-signal equivalent circuit model in Fig. 5.2 is based on the circuit model in Fig. 3.13 on page 91. The circuit in Fig. 3.13 is a result of various simplifications of the circuit in Fig. 3.8 on page 81. The comparison of measured and simulated switching characteristics in section **4.1** on page 95 et seq. shows that the terminal behavior is well represented by the simulation circuit Fig. 3.13. Therefore, it is assumed that a more complex circuit model does not significantly enhance the simulation results in section **4.1** and the results of the stability analysis in this chapter.

Although the presented stability analysis is based on various simplification, it provides a basis to diminish oscillations with temporarily increasing amplitudes during switching operations by means of optimized PCBs, packages and power MOSFETs. The approach has a strong saving potential with respect to design iterations and development costs, because the stability can be analyzed during virtual prototyping processes.[10] Thereby, the stability analysis is not restricted to buck converter topologies. It can be applied to different kinds of commutation cells. The small-signal equivalent circuit model and the circuit parameter definitions must possibly be adopted.[11]

5.5 Optimization of the Stability and the Damping of Commutation Cells

For the considered commutation cell, infinite locus curves of switching operations exist due to infinite possibilities for the parameterization of the driver voltage, the switched DC link voltage and load current. Various trajectories are also found during normal operation of a power converter. The optimization of the stability or the damping of operating points along the locus curve of single turn-off and a single turn-on is hence not sufficient. The entire operating range of interest must be regarded.

Different parameterizations of the circuit elements represent different designs of semiconductor chips, packages and PCBs. As shown in subsection **5.2.4** on page 119 et seq., the circuit parameters can be optimized with respect to the stability of the linearized subsidiary systems. Measures for an improved stability of the *analyzed* commutation cell are summarized in Table 5.7. '↓' in front of an circuit elements means that a parameter decrease tends to increase the stability. '↑' in front of an circuit elements means that a parameter increase tends to increase the stability. '↓↑' means that a clear trend could not be observed. It is indicated how the alteration can be implemented in the commutation cell. However, interdependencies between the circuit parameters have not been analyzed in subsection **5.2.4**. The variation of more than one circuit parameter may improve or degrade the stability much stronger, weaker or in a different direction than one would expect due to the separate variation of the circuit parameters. Furthermore, it must be kept in mind that a change in the design of a semiconductor, a package or a PCB affect usually more than one circuit parameter. With respect to the stability, the improvement of one circuit parameter can therewith lead to a worsening of an other circuit parameter. Process and semiconductor device simulations as well as electromagnetic field simulations for the extraction of resistance, inductance, conductance and capacitance parameters from PCB and package designs are useful for gaining a sense of how design alterations affect the equivalent circuit elements of semiconductors, packages and PCBs.

[10] Virtual prototyping is a technique, which is used during product development. The product's design is tested by computer-aided engineering software before a physical prototype of the product is made.

[11] In [Höch 10], it is e.g. shown that buck and boost converters have the same small-signal equivalent circuit model, but the circuit parameters are defined differently.

Table 5.7: Concluded alteration of parameters in the equivalent circuit model in Fig. 5.2 on page 114 for an improved stability of the considered commutation cell and the corresponding implementation possibilities

Parameter change		**Alteration can be realized through an adopted ...**			
		... PCB design.	... package (design).	... chip (design).	... chip size.
↓	g_{m}			x	↓
↑	g_{ds}			x	↑
↓↑	$C_{\mathrm{ds\,chip}}$			x	↓↑
↑	$C_{\mathrm{dg\,chip}}$			x	↑
↑	$C_{\mathrm{gs\,chip}}$			x	↑
↓↑	$C_{\mathrm{ds\,ext}}$	x	x		
↓↑	$C_{\mathrm{dg\,ext}}$	x	x		
↓↑	$C_{\mathrm{gs\,ext}}$	x	x		
↓↑	$L_{\mathrm{d\,pac}}{}^{*}$	x	x		
↓↑	$L_{\mathrm{d\,cir}}$	x			
↓	$L_{\mathrm{g\,pac}}{}^{*}$	x	x		
↓	$L_{\mathrm{g\,cir}}$	x			
↓	$L_{\mathrm{s\,pac}}{}^{*}$	x	x		
↓	$L_{\mathrm{s\,cir}}$	x			
↑	$R_{\mathrm{g\,pac}}{}^{*}$	x	x	x	
↑	$R_{\mathrm{g\,cir}}$	x			

* As stated on page 93, indices 'cir' and 'pac' are used to distinguish RL elements close to and further away from the MOSFET. They do *not* refer to package and PCB.

The optimization of the stability and the damping of commutation cells is not part of this work. The following list of optimization criteria is intended as a suggestion:

- One optimization criterion is the ***maximization of the stability degree*** d_0, which is a measure for the decrease of the system's energy (see e.g. [Cox 97] and [Cox 98]):

$$\max_i\{\Re(\lambda_{\mathrm{i}})\} = -d_0 \rightarrow \min \tag{5.33}$$

  The degree of stability is the distance of the imaginary axis from the nearest eigenvalue, which is given by the maximum real part of the system's eigenvalues (see Fig. 5.29).

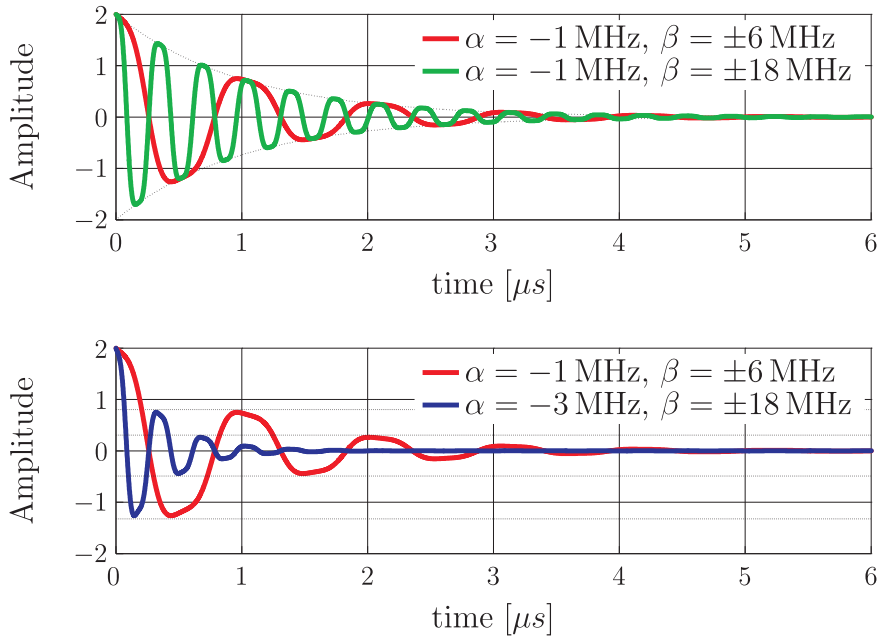


Figure 5.29: Comparison of stability degree and damping ratio for systems with a 2×2 system matrix and the eigenvalues $\lambda_{1,2} = \alpha \pm \mathrm{i} \cdot \beta$ - The upper plot shows oscillations in systems with the same stability degree. The lower plot shows oscillations in systems with the same damping ratio. The 'green' system has a lower damping ratio than the 'red' (and the 'blue') system. The 'blue' system has a higher stability degree than the 'red' (and the 'green') system.

- The ***maximization of the damping ratio*** D_0:

$$\max_i \left\{ \frac{\Re(\lambda_\mathrm{i})}{|\lambda_\mathrm{i}|} \right\} = \max_i \{\cos \varphi(\lambda_\mathrm{i})\} = -D_0 \rightarrow \min \tag{5.34}$$

  is another optimization criterion (see e.g. [Müller 91]). The smaller the damping ratio the fewer oscillation periods are needed for the decline of an initial displacement to a certain fraction of the initial displacement. This criterion minimizes the number of oscillations before the system comes to rest (see Fig. 5.29).

- A third optimization criterion is the ***minimization of the total energy of the system*** (see e.g. [Brabender 98] and [Narkić 03]):

$$\int_0^\infty E(t)\ \mathrm{dt} \rightarrow \min \tag{5.35}$$

The references in the previous list contain examples for the different optimization approaches of the stability of oscillating systems. Continuative works could apply the different optimization approaches to small-signal equivalent circuit models of commutation cells. Thereby, the impact of the different criteria on sample switching characteristics should also be analyzed.

The (statistical) design of experiments (DoE) might also be of interest for the optimization of the stability of commutation cells.[12] Statistical methodologies are of particular interest for the analysis of the interactions between the circuit elements with respect to the oscillatory stability of commutation cells. For the considered $I_{\mathrm{Ch}}(V_{\mathrm{DS\,chip}})$ plane, a cumulated or averaged optimization criterion could be defined, and analyzed with the methods of DoE.

[12] DoE is a method for the analysis of systems. The method is universal and applicable for the optimization of products and processes. For details, see e.g. [Fisher 90] and [Siebertz 10].

6 Summary and Outlook

In this chapter, the results of this work are summarized in section **6.1**, and topics for necessary and recommended continuing works are pointed out in section **6.2**.

6.1 Major Results of this Work

The main goal of this work was the development of a methodology that enables ...

- ... the prediction of parasitic oscillations with temporarily increasing amplitudes in commutation cells with a power MOSFET and a SCHOTTKY diode and ...
- ... the optimization of the stability and the damping of commutation cells with a power MOSFET and a SCHOTTKY diode ...

during switching operations. This goal was achieved by deriving a large-signal behavioral model and the corresponding small-signal equivalent behavioral models of the commutation cell in a sample one quadrant buck converter topology, and the subsequent stability analysis of the small-signal equivalent behavioral models.

Large-signal models of power MOSFETs and SCHOTTKY diodes are derived for conditions of use that are for example typical in PFC circuits. The MOSFET's behavioral model consists of the output characteristics and the capacitances $C_{\mathrm{DG\,chip}}$, $C_{\mathrm{GS\,chip}}$ and $C_{\mathrm{DS\,chip}}$. The model of the SCHOTTKY diode includes the forward and the blocking characteristics of the diode and the junction capacitance $C_{\mathrm{AC\,chip}}$. Restrictions for the application of the large-signal behavioral models are discussed. The combination of curve tracer measurements and short circuit measurements allow the MOSFETs' static characterization for the *entire* operating range of interest. The estimation of the current error in the MOSFETs' static characteristics is explained. The power MOSFETs' dynamic parameters can be approximated by means of switching characteristics. A gate source voltage dependency of the defined drain source capacitance $C_{\mathrm{DS\,chip}}$ is revealed for the considered SJ MOSFET.

A large-signal model of the electrical interconnections of the considered buck converter's packages and PCB is derived with inductances the $L_{\mathrm{D\,cir}}$, $L_{\mathrm{D\,pac}}$, $L_{\mathrm{G\,cir}}$, $L_{\mathrm{G\,pac}}$, $L_{\mathrm{S\,cir}}$ and $L_{\mathrm{S\,pac}}$, the resistances $R_{\mathrm{D\,cir}}$, $R_{\mathrm{D\,pac}}$, $R_{\mathrm{G\,cir}}$, $R_{\mathrm{G\,pac}}$, $R_{\mathrm{S\,cir}}$ and $R_{\mathrm{S\,pac}}$, as well as the coupling capacitances $C_{\mathrm{DG\,ext}}$, $C_{\mathrm{GS\,ext}}$ and $C_{\mathrm{DS\,ext}}$. Thereby, the concept of *effective* resistances and inductances is introduced. Effective resistances and inductances enable the consideration of mutual and self resistances and inductances of an electrical interconnection in a single resistance and inductance. Some mutual inductances and resistances are disregarded in the calculation of the effective inductances and resistances in order to obtain constant circuit

parameters. The parameterization of the behavioral model is based on quasi-static field simulations of the 3D models of the PCB and packages. The proposed large-signal model of the considered interconnections limits the maximum equivalent frequency of the switching slopes, which can be modeled, to approximately 200 MHz and the maximum oscillation frequencies, which can be analyzed, to approximately 1 GHz.

The behavioral models of the power semiconductors, the electrical interconnections of packages and PCBs, and the simplified DC voltage link, input and load circuit are combined. The comparison of measured and simulated switching characteristics approves the proposed modeling of the considered buck converter topology. It is shown that the parameterization of the MOSFET's capacitances $C_{\mathrm{DG\,chip}}$, $C_{\mathrm{GS\,chip}}$ and $C_{\mathrm{DS\,chip}}$ on the basis of dynamic measurements is superior to the parameterization on the basis of C_{rss}, C_{iss} and C_{oss}, which are given in the MOSFETs' data sheets. The modeling of the gate source voltage dependency of the defined drain source capacitance $C_{\mathrm{DS\,chip}}$ improves the simulation results for switching operations, in which the drain source voltage slope is limited by the charging of $C_{\mathrm{DS\,chip}}$.

The derived small-signal equivalent circuit model considers the MOSFET's output conductance g_{ds}, gate transconductance g_{m} and capacitances $C_{\mathrm{dg\,chip}}$, $C_{\mathrm{gs\,chip}}$ and $C_{\mathrm{ds\,chip}}$, as well as the chip-external capacitances $C_{\mathrm{dg\,ext}}$, $C_{\mathrm{gs\,ext}}$ and $C_{\mathrm{ds\,ext}}$, the inductances $L_{\mathrm{d\,cir}}$, $L_{\mathrm{d\,pac}}$, $L_{\mathrm{g\,cir}}$, $L_{\mathrm{g\,pac}}$, $L_{\mathrm{s\,cir}}$ and $L_{\mathrm{s\,pac}}$ of the electrical interconnections of packages and PCB, and the resistances $R_{\mathrm{d\,cir}}$, $R_{\mathrm{d\,pac}}$, $R_{\mathrm{g\,cir}}$, $R_{\mathrm{g\,pac}}$, $R_{\mathrm{s\,cir}}$ and $R_{\mathrm{s\,pac}}$. It is revealed that both a simplified small-signal equivalent circuit model (without the MOSFET's output conductance g_{ds} and the chip-external capacitances $C_{\mathrm{dg\,ext}}$, $C_{\mathrm{gs\,ext}}$ and $C_{\mathrm{ds\,ext}}$) and the analysis of single operating points are usually not sufficient for the analysis of the stability of commutation cells. Results of the stability analysis and corresponding switching characteristics show: The proposed stability analysis of the buck converter's subsidiary systems enables conclusions on occurring oscillations during switching operations. Oscillations with temporarily increasing amplitudes can be predicted as long as the dwell time in areas with unstable operating points is large compared to the periods of the corresponding eigenfrequencies. The comparison of the stability analysis of different circuit parameterizations enables conclusions on an optimized stability of the commutation cell. The efficiency of the commutation cell can also be improved if the circuit elements' impact on the switching losses is considered.

If the presented approach enables also the derivation and implementation of necessary adjustments for the stability analysis of other commutation cells - for example with other semiconductor devices - remains to be shown.

6.2 Necessary and Recommended Continuing Works

With this dissertation the analysis of the stability of commutation cells during switching operations is not completed. Especially against the background of the more recent semiconductor technology achievements and developments, future works are needed. Below, a proposal for necessary and recommended continuing works is given.

Continuing Works Regarding the Modeling of High Voltage Power MOSFETs in Commutation Cells

The switching operations that are suitable for the determination of the dynamic parameters of the MOSFET's behavioral model are restricted. The ***optimization of the stability of the dynamic measurement setup*** would improve the dynamic characterization and the dynamic parameterization of the MOSFET's behavioral model respectively.

The determined drain source capacitance of the MOSFET's behavioral model shows a strong dependency on the operating conditions (see Fig. 2.29 on page 59). The ***physical cause of the dependency of the drain source capacitance on the operating conditions*** must be analyzed and understood. The implementation of the dependency in the parameterization of the MOSFET model will enhance the simulation of switching operations.

Continuing Works Regarding the Modeling of Electrical Interconnections of Packages and PCBs in Commutation Cells

The used circuit models in this work are based on the assumption that the considered commutation cell is electrically small compared to the wavelength that corresponds to the maximum frequency of interest of the considered voltage and current signals' harmonic content. Electrically small circuits can be approximated with lumped circuit elements. Not all commutation cells are electrically small compared to the maximum frequency of interest.[1] The ***implantation of transmission lines in the large-signal circuit models of electrical interconnections*** could enhance the simulation of the dynamic behavior of commutation cells that are not electrically small.[2]

The stability analysis in subsection **5.2.4** on page 119 et seq. shows that the design of the MOSFET's input circuit has a significant impact on the stability of commutation cells. In this work, significant parts of the interconnections of the MOSFET's gate driver circuit are not modeled. Ideal circuit elements are assumed for these parts. Due to the significance of the driver circuit, future works should ***implement the electrical interconnections to the driving IC in the field simulation model***. This enables a better parameterization of the input circuit elements $L_{\mathrm{G\,pac}}$, $L_{\mathrm{G\,cir}}$, $L_{\mathrm{S\,pac}}$, $L_{\mathrm{S\,cir}}$, $C_{\mathrm{GS\,ext}}$ and $C_{\mathrm{DG\,ext}}$ of the large-signal model of the buck converter topology, and the input circuit elements $L_{\mathrm{g\,pac}}$, $L_{\mathrm{g\,cir}}$, $L_{\mathrm{s\,pac}}$, $L_{\mathrm{s\,cir}}$, $C_{\mathrm{gs\,ext}}$ and $C_{\mathrm{dg\,ext}}$ of the corresponding small-signal models.

[1] In power electronics, the 'electrically small' assumption is probably true for most semiconductor devices.
[2] Thereby, it must be kept in mind that the computing time correlates with the circuit models' complexity.

As shown in [Petzoldt 01], the ***consideration of equivalent circuit elements of the driver IC*** could further improve the simulation of switching operations.

The ***consideration of the heat sink(s)*** in the Q3D Extractor model enables the analysis of the impact of the coupling capacitances to heat sink(s) on parasitic oscillations.

The derived large-signal model of electrical interconnections in PCBs and packages for the simulation of switching operations in Fig. 3.13 on page 91 considers *effective* inductances and resistances. Some mutual inductances and resistances are disregarded in the defining equations. The ***implementation of mutual inductances and resistances in the large-signal model*** could enhance the simulation of switching operations.

Continuing Works Regarding the Stability Analysis of Commutation Cells

In the small-signal equivalent circuit model for the stability analysis, the SCHOTTKY diode is represented by a short circuit. Measurements have shown, the oscillation behavior during switching operations depends on the used freewheeling diode. Thus, the ***consideration of the Schottky diode in the small-signal equivalent circuit model*** would enhance the stability analysis. However, as discussed in subsection **5.2.1** on page 112, for the stability analysis operating points are necessary. The points in time during commutation could be *defined* as operating points, and eigenvalues of the accordant small-signal equivalent circuit models - with the SCHOTTKY diode's conductance $g_{\mathrm{ac}}(V_{\mathrm{AC\,chip}}) = {}^{\Delta I_{\mathrm{MS}}}/_{\Delta V_{\mathrm{AC\,chip}}}$ and capacitance $C_{\mathrm{ac\,chip}}(V_{\mathrm{AC\,chip}}) = C_{\mathrm{AC\,chip}}(V_{\mathrm{AC\,chip}})$ - could be derived for trajectories of switching operations. However, infinite trajectories exist for the commutation cell. Instead of the analysis of trajectories, the considered operating range of the MOSFET could be investigated for sample operating conditions of the SCHOTTKY diode.

The ***implantation of transmission lines in the small-signal circuit models of electrical interconnections*** could be necessary for a meaningful stability analysis of commutation cells that are not electrically small.

The ***implementation of equivalent circuit elements of the driver IC*** could further enhance the stability analysis of commutation cells.

In subsection **5.2.4** on page 119 et seq., the impact of circuit element(s) on the stability is analyzed. Based on this analysis, conclusions are drawn for the optimization of the circuit element(s) with respect to the stability of the commutation cell. Thereby, it is assumed that all but the altered circuit element(s) remain(s) constant. Conclusions on the stability for the combined optimization of two or more circuit elements can only conditionally be drawn on basis of the results, because interactions between the circuit elements can not be observed in exclusive parameter alterations. The stability analysis would be significantly enhanced by an ***analysis of interactions of the circuit elements***. Such interactions can for example be detected with the statistical methodology DoE.

The small-signal equivalent circuit models in Fig. 5.2 on page 114 and Fig. 5.24 on page 153 enable the analysis of oscillations, which were known as common mode oscillations in the nineteen eighties [Severns 85]. Similar to the simplified small-signal equivalent circuit

model in Fig. 5.24, a small-signal equivalent circuit model for the ***analysis of differential mode oscillations*** is presented in [Severns 85] and [Kassakian 84]. It enables the analysis of oscillations due to the parallel connection of power MOSFETs. Future works could derive a small-signal equivalent circuit model for differential mode oscillations, which considers chip-external capacitances as well as the MOSFET's output conductance. In accordance with the analysis in section **5.2** on page 112 et seq., the operating range of the paralleled power MOSFETs could be analyzed with such a model.

This dissertation assumes that positive cosine phi's of the conjugate-complex eigenvalues are a necessary condition for oscillations with temporarily increasing amplitudes during commutation (see subsection **5.2.3** on page 117 et seq. and **5.4.1** on page 156 et seq.). During switching operations, the way of the $i_{\mathrm{Ch}}(v_{\mathrm{DS\,chip}})$ locus curves through areas with positive cosine phi's and the dwell time in these areas determine if a sufficient condition for oscillations with temporarily increasing amplitudes is satisfied or not. A ***better understanding of the sufficient condition(s) of oscillations with temporarily increasing amplitudes*** would enhance the stability analysis. At present, oscillations with temporarily increasing amplitudes can be predicted by means of the presented stability analysis as long as the dwell time in unstable areas is large compared to the periods of the eigenfrequencies of the corresponding subsidiary systems. A more specific measure for 'large compared to' would be of interest. The measure seems to depend on the positive cosine phi values.

Different approaches of the ***optimization of the stability and the damping of commutation cells*** are suggested in subsection **5.5** on page 167 et seq.. The implementation of these approaches for a sample commutation cell and a comparison of the resulting dynamic behavior - for example with respect to the efficiency and the EMI behavior - would support the application dependent design optimization of commutation cells.

The detection of the (used) commutation cells in power converters is the precondition for the analysis of their stability. Once the commutation cells are detected and modeled, the ***the stability of other power converters*** can be analyzed.

The ***application of the stability analysis to commutation cells with other semiconductor devices*** is also an interesting research topic. The derivation of appropriate behavioral models of bipolar devices and their parameterization are the keys to a successful application of the presented methodology. Oscillations in commutation cells with bipolar power devices can correlate with transit times of carriers. The oscillation frequencies are relatively high and the dimensions of the semiconductor chips are not small enough compared to the corresponding wavelengths. In this case, lumped circuit elements are not sufficient for the modeling of the semiconductor devices. The derivation of distributed behavioral models that enable the analysis of such oscillations and the parameterization of such models could be interesting. However, process and device simulation tools might be more sufficient for the analysis of such oscillations.

A Additional Simulations of Switching Characteristics

Comparison of Chip Characteristics with Circuit Characteristics

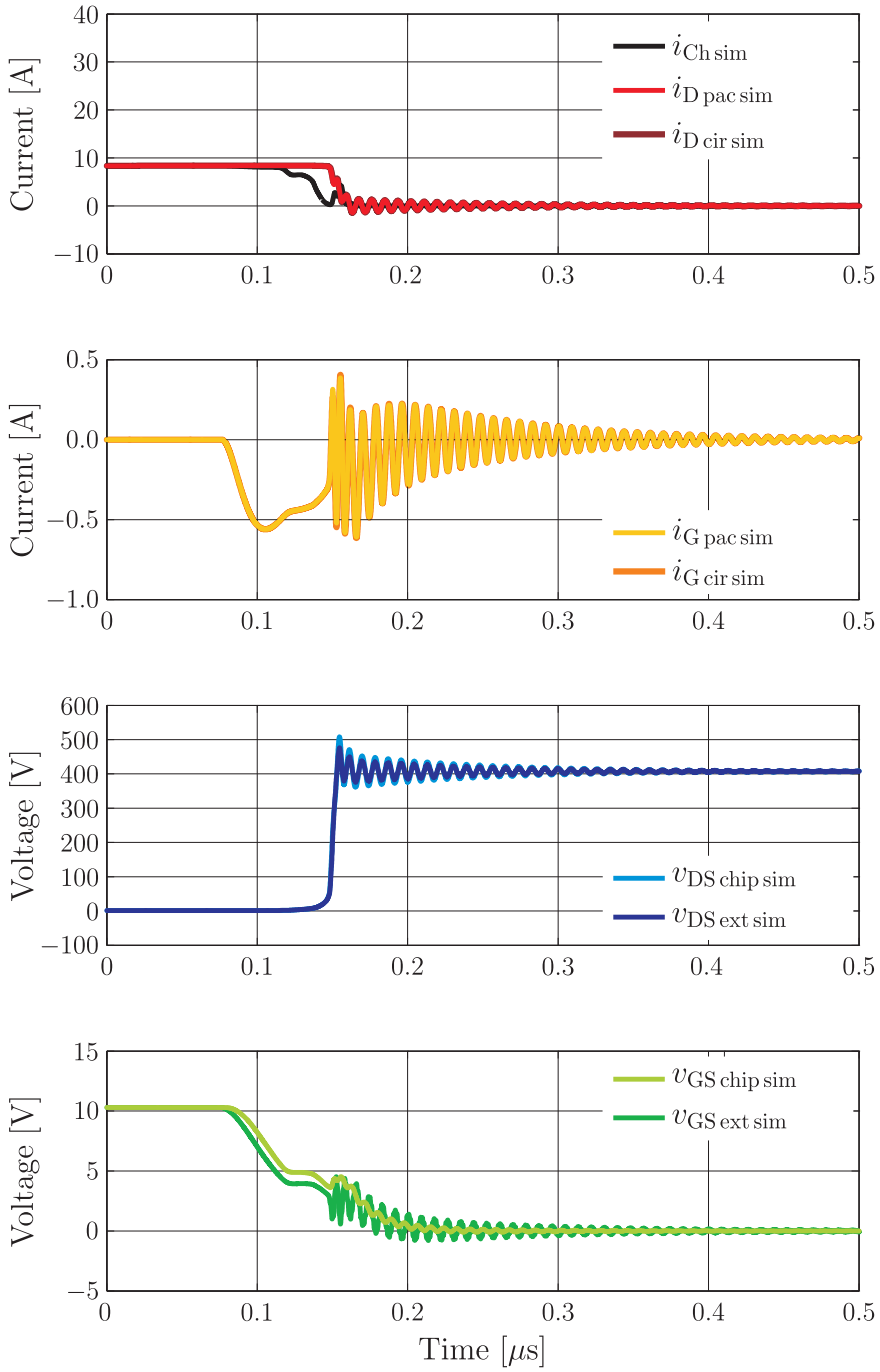
In Fig. A.1, simulated chip characteristics i_{Ch}, $i_{\mathrm{D\,pac}}$, $i_{\mathrm{G\,pac}}$, $v_{\mathrm{DS\,chip}}$ and $v_{\mathrm{GS\,chip}}$ are compared to simulated chip-external characteristics $i_{\mathrm{D\,cir}}$, $i_{\mathrm{G\,cir}}$, $v_{\mathrm{DS\,ext}}$ and $v_{\mathrm{GS\,ext}}$. The 'probing points' of the different currents and voltages are indicated in Fig. 3.13 and Fig. 2.7. Fig. A.1 corresponds to Fig. 4.3 in section **4.1**. The currents $i_{\mathrm{D\,pac}}$ and $i_{\mathrm{D\,cir}}$, $i_{\mathrm{G\,pac}}$ and $i_{\mathrm{G\,cir}}$, as well as the voltages $v_{\mathrm{DS\,chip}}$ and $v_{\mathrm{DS\,ext}}$ are almost identical. The voltages $v_{\mathrm{GS\,chip}}$ and $v_{\mathrm{GS\,ext}}$ have different oscillation amplitudes and partly different absolute voltage levels.

Frequency Analysis of Simulated Switching Characteristics

For a frequency analysis, signals with high oscillation amplitudes and signals, which oscillate around an as constant value as possible, are preferred.

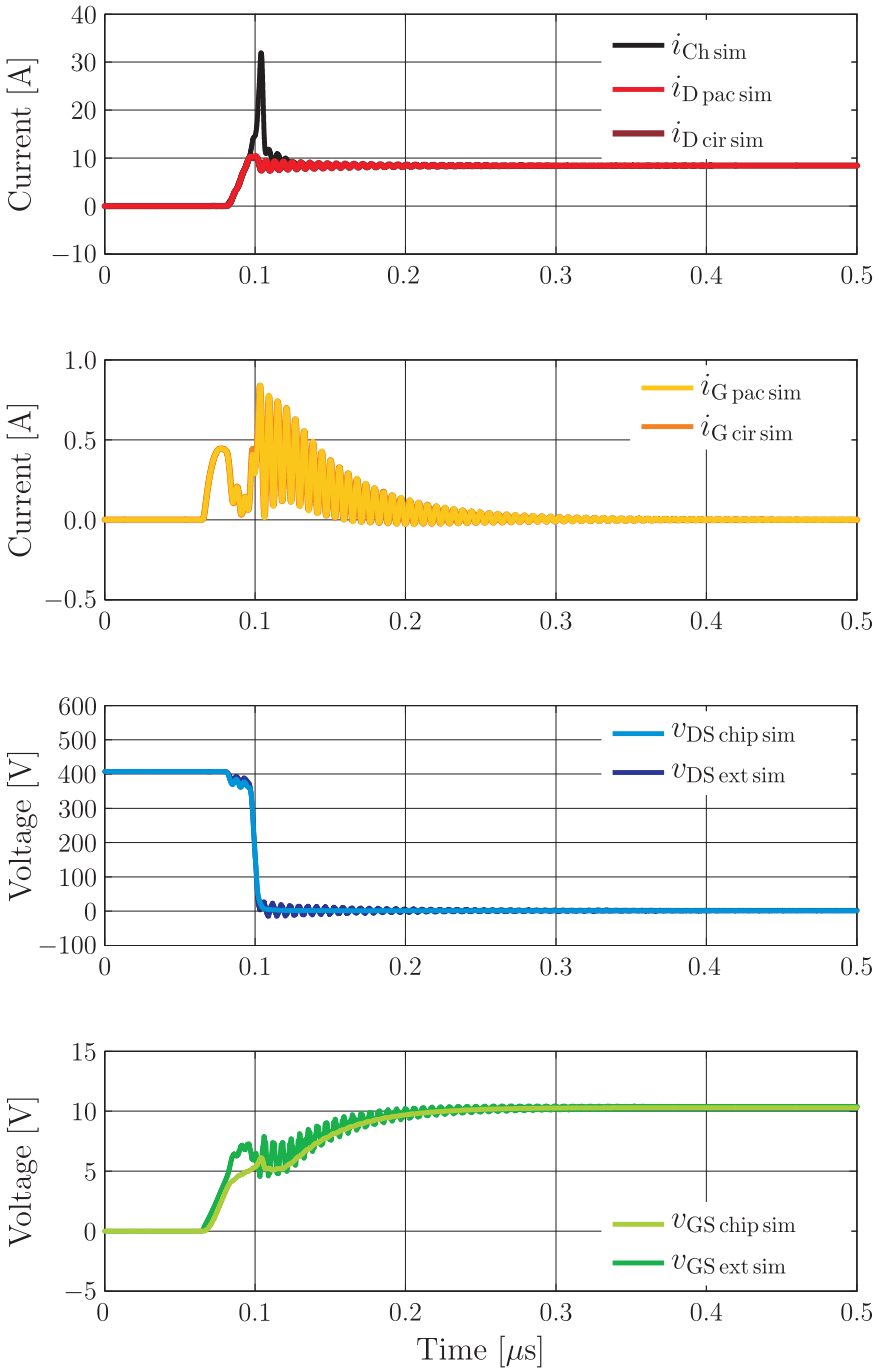
Accordingly, the gate current and the gate source voltage characteristics in Fig. A.1 are less suitable for the frequency analysis, because the oscillations superpose non-constant signals. The drain source voltage characteristics oscillate around almost constant values. However, during turn-on, the oscillation amplitudes of the $v_{\mathrm{DS\,chip}}$ characteristics are too small. Thus, Fig. A.2 shows the results of a FOURIER analysis of oscillating sections of the $v_{\mathrm{DS\,ext}}$ characteristics. The $v_{\mathrm{DS\,ext}}$ characteristics in Fig. 5.27 are based on the same parameterization as the results of the stability analysis in Fig. 5.3. The eigenfrequencies of different operating points of the buck converter topology are depicted in Fig. 5.3(b). The eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{3,4}$ and $\lambda_{5,6}$ are visible in the frequency spectra in Fig. A.2. The step width in the simulation characteristics is too small for the eigenfrequencies of the conjugate-complex eigenvalue pair $\lambda_{1,2}$, but even for an adopted step width, the oscillation amplitudes would probably be too small to stand out against the amplitudes of the eigenfrequencies of $\lambda_{3,4}$ and $\lambda_{5,6}$.[1]

[1] With the used dynamic measurement setup, oscillation with a frequency of 4.5 GHz can not be measured.



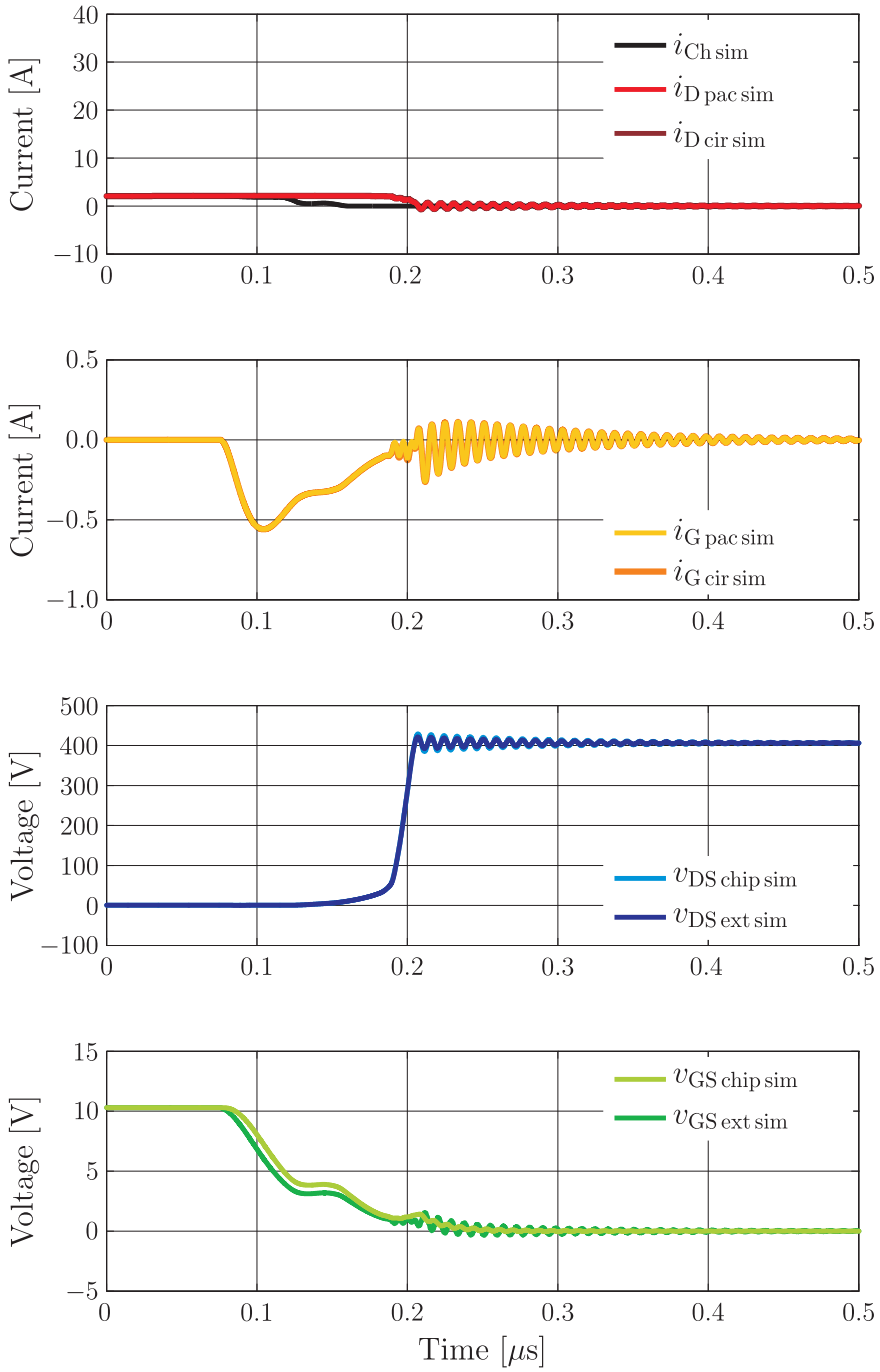
(a) Turn-off characteristics with $R_{\mathrm{G\,ext}} = 10\,\Omega$, $V_{\mathrm{DClink}} = 400\,\mathrm{V}$, $i_{\mathrm{L}} = 8\,\mathrm{A}$ and $\vartheta_{\mathrm{J}} = 25\,^{\circ}\mathrm{C}$

Figure A.1: Comparison of the chip characteristics in Fig. 4.3 with the corresponding circuit characteristics



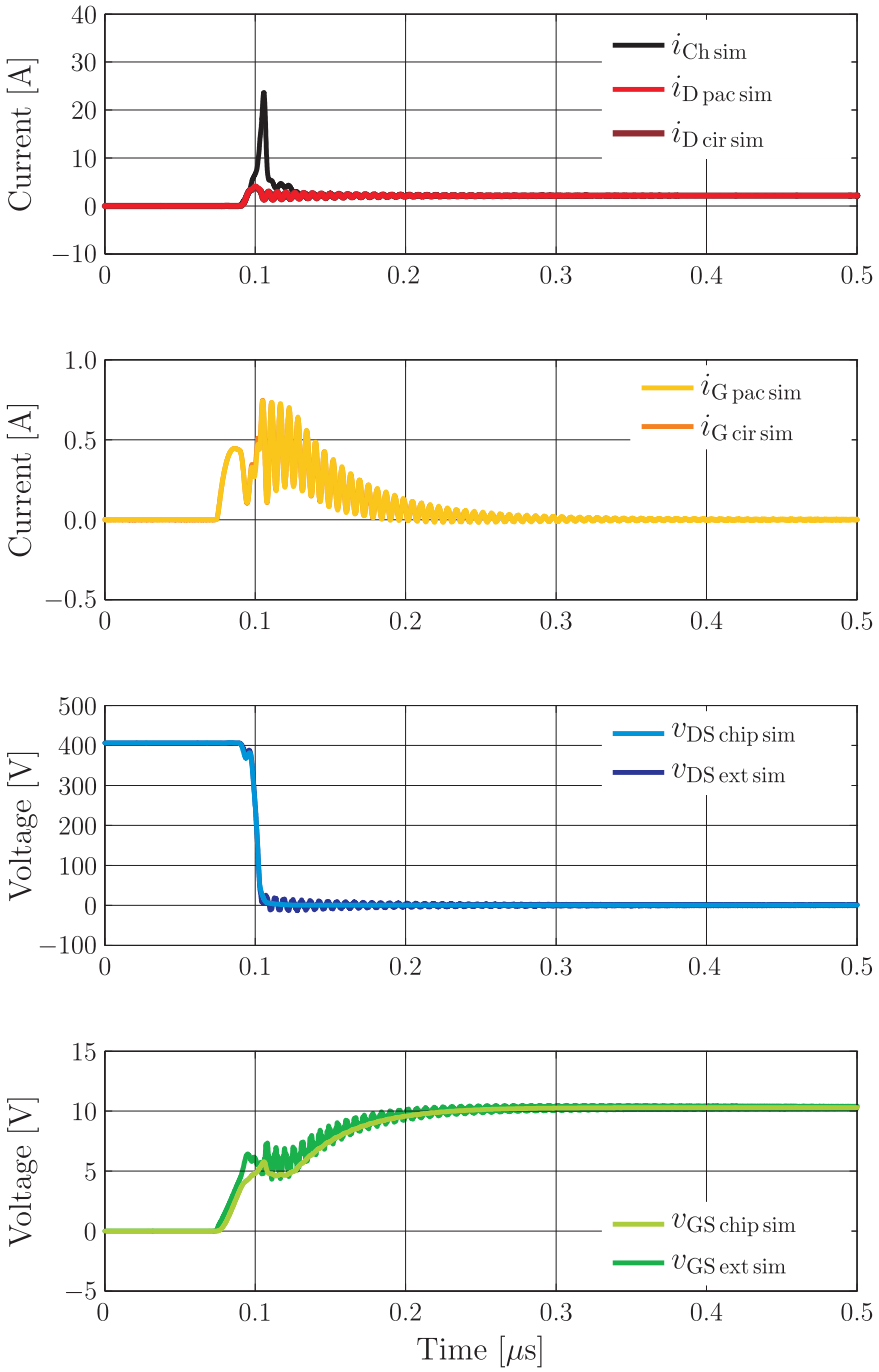
(b) Turn-on characteristics with $R_{\mathrm{G\,ext}} = 10\,\Omega$, $V_{\mathrm{DClink}} = 400\,\mathrm{V}$, $i_{\mathrm{L}} = 8\,\mathrm{A}$ and $\vartheta_{\mathrm{J}} = 25\,^{\circ}\mathrm{C}$

Figure A.1: Comparison of the chip characteristics in Fig. 4.3 with the corresponding circuit characteristics (cont.)



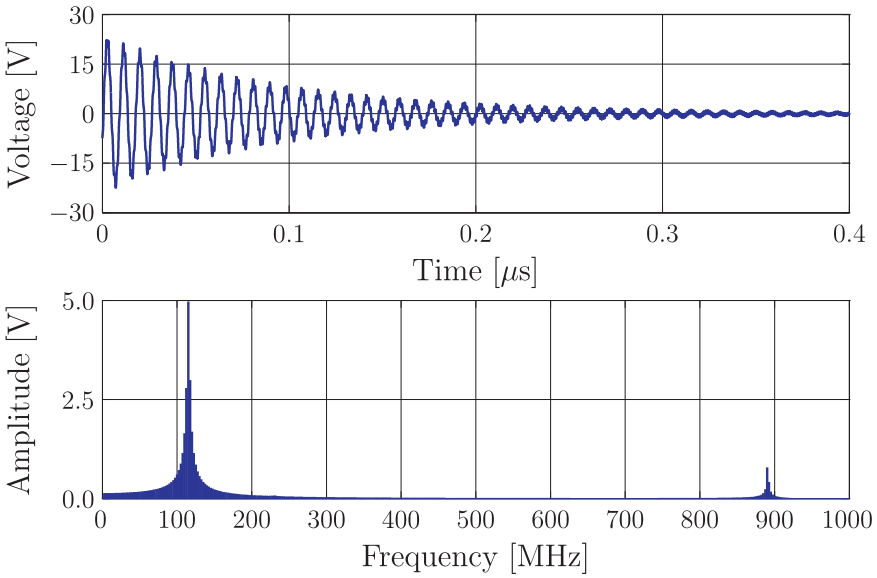
(c) Turn-off characteristics with $R_{\mathrm{G\,ext}} = 10\,\Omega$, $V_{\mathrm{DClink}} = 400\,\mathrm{V}$, $i_{\mathrm{L}} = 2\,\mathrm{A}$ and $\vartheta_{\mathrm{J}} = 25\,^{\circ}\mathrm{C}$

Figure A.1: Comparison of the chip characteristics in Fig. 4.3 with the corresponding circuit characteristics (cont.)

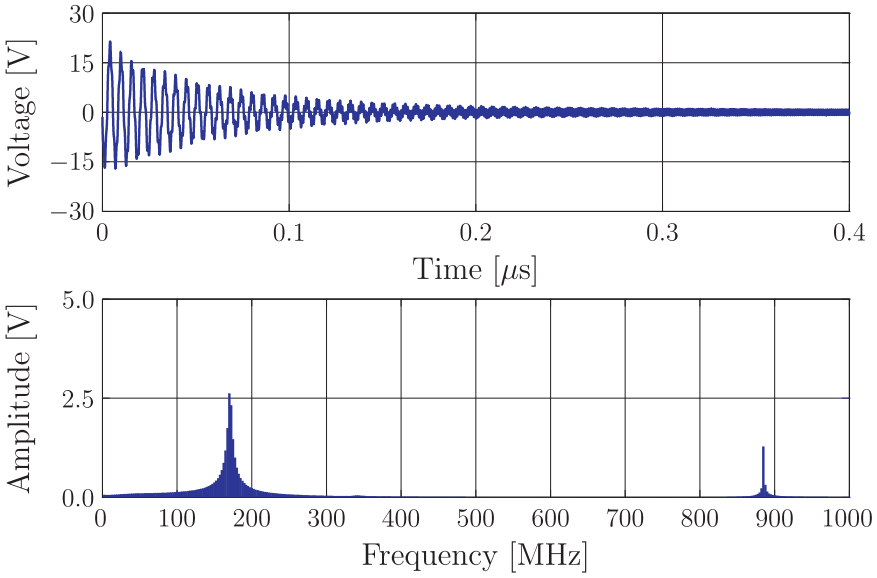


(d) Turn-on characteristics with $R_{\mathrm{G\,ext}} = 10\,\Omega$, $V_{\mathrm{DClink}} = 400\,\mathrm{V}$, $i_{\mathrm{L}} = 2\,\mathrm{A}$ and $\vartheta_{\mathrm{J}} = 25\,^{\circ}\mathrm{C}$

Figure A.1: Comparison of the chip characteristics in Fig. 4.3 with the corresponding circuit characteristics (cont.)



(a) AC component of a detail of the simulated $v_{\mathrm{DS\,ext}}$ signal in Fig. A.1(a) (top) and the accordant frequency spectra (bottom)



(b) AC component of a detail of the simulated $v_{\mathrm{DS\,ext}}$ signal in Fig. A.1(b) (top) and the accordant frequency spectra (bottom)

Figure A.2: Frequency analysis of simulated switching characteristics in Fig. A.1(a) and Fig. A.1(b)

B Derivations for the Stability Analysis

B.1 System Matrix of the Small-Signal Equivalent Circuit Model

In Fig. B.1, the small-signal equivalent circuit of the regarded buck converter topology is shown.[1] For the determination of the circuit's system matrix $\boldsymbol{A}$, the corresponding differential state space equation system $\dot{\vec{x}} = \boldsymbol{A} \cdot \vec{x}$ is needed. Subsequently, the state space equation system is derived. Thereby, the following definitions are used:

$$
\begin{aligned}
CC_{\text{chip}} &= C_{\text{dg chip}} \cdot C_{\text{ds chip}} + C_{\text{gs chip}} \cdot C_{\text{dg chip}} + C_{\text{ds chip}} \cdot C_{\text{gs chip}}, \\
CC_{\text{ext}} &= C_{\text{dg ext}} \cdot C_{\text{ds ext}} + C_{\text{gs ext}} \cdot C_{\text{dg ext}} + C_{\text{ds ext}} \cdot C_{\text{gs ext}}, \\
LL_{\text{pac}} &= L_{\text{g pac}} \cdot L_{\text{s pac}} + L_{\text{d pac}} \cdot L_{\text{g pac}} + L_{\text{s pac}} \cdot L_{\text{d pac}} \text{ and} \\
LL_{\text{cir}} &= L_{\text{g cir}} \cdot L_{\text{s cir}} + L_{\text{d cir}} \cdot L_{\text{g cir}} + L_{\text{s cir}} \cdot L_{\text{d cir}}.
\end{aligned}
$$

For the small-signal circuit in Fig. B.1, the time derivatives of the currents through the inductances are given by

$$\Delta\dot{I}_{\text{D pac}} = \frac{\Delta V_{\text{DS chip}} - \Delta V_{\text{DS ext}} - \Delta V_{n1} - R_{\text{d pac}} \cdot \Delta I_{\text{D pac}}}{L_{\text{d pac}}}, \tag{B.1}$$

$$\Delta\dot{I}_{\text{G pac}} = \frac{\Delta V_{\text{GS chip}} - \Delta V_{\text{GS ext}} - \Delta V_{n1} - R_{\text{g pac}} \cdot \Delta I_{\text{G pac}}}{L_{\text{g pac}}} \text{ and} \tag{B.2}$$

$$\Delta\dot{I}_{\text{S pac}} = \frac{\Delta V_{n1} - R_{\text{s pac}} \cdot \Delta I_{\text{S pac}}}{L_{\text{s pac}}} \text{ as well as} \tag{B.3}$$

$$\Delta\dot{I}_{\text{D cir}} = \frac{\Delta V_{\text{DS ext}} - \Delta V_{n2} - R_{\text{d cir}} \cdot \Delta I_{\text{D cir}}}{L_{\text{d cir}}}, \tag{B.4}$$

$$\Delta\dot{I}_{\text{G cir}} = \frac{\Delta V_{\text{GS ext}} - \Delta V_{n2} - R_{\text{g cir}} \cdot \Delta I_{\text{G cir}}}{L_{\text{g cir}}} \text{ and} \tag{B.5}$$

$$\Delta\dot{I}_{\text{S cir}} = \frac{\Delta V_{n2} - R_{\text{s cir}} \cdot \Delta I_{\text{S cir}}}{L_{\text{s cir}}}. \tag{B.6}$$

[1] The derivation of the small-signal equivalent circuit model is described in subsection **5.2.1** on page 112 et seq.. For small-signals, DC voltage sources and high capacitances behave as shorts and DC current sources and high inductances behave as open circuits. The diode is represented as a short.

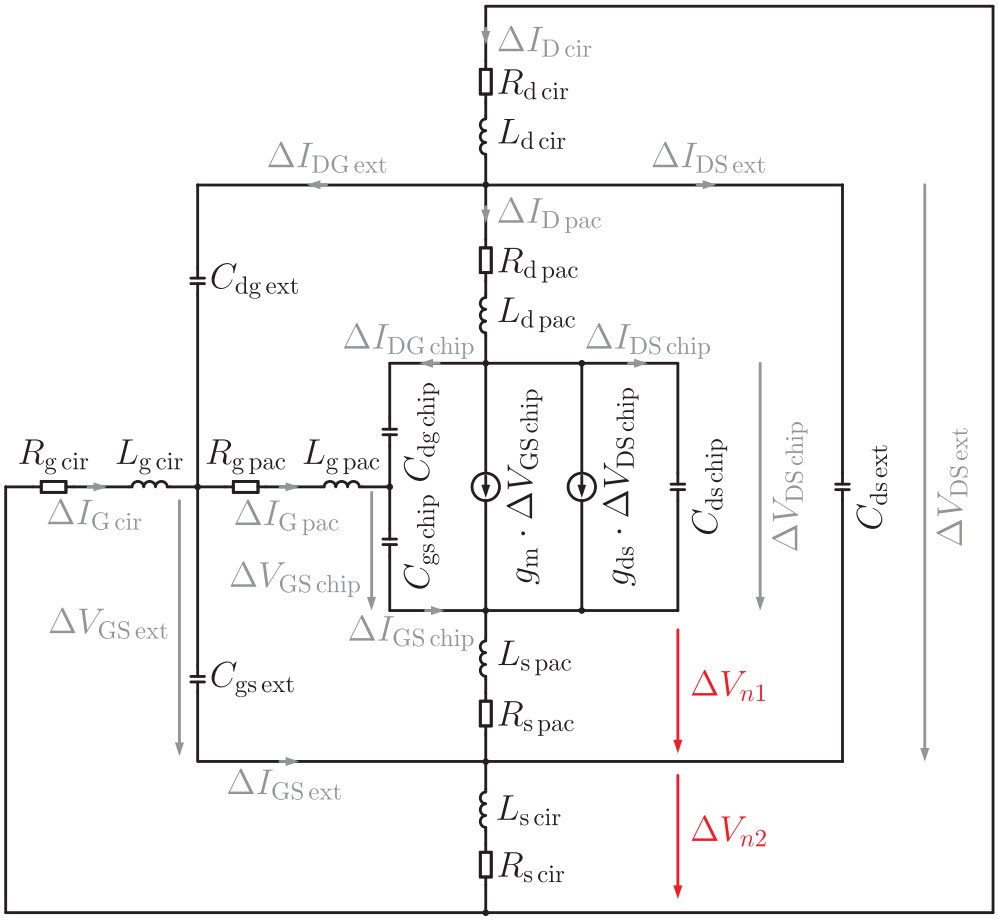


Figure B.1: Small-signal equivalent circuit model of a buck converter topology's operating points on the basis of the buck converter model in Fig. 3.13 on page 91

The application of KIRCHHOFF's current law results in

$$\begin{aligned} 0 =& \frac{\Delta V_{\mathrm{DS\,chip}} - \Delta V_{\mathrm{DS\,ext}} - \Delta V_{n1} - R_{\mathrm{d\,pac}} \cdot \Delta I_{\mathrm{D\,pac}}}{L_{\mathrm{d\,pac}}} - \frac{\Delta V_{n1} - R_{\mathrm{s\,pac}} \cdot \Delta I_{\mathrm{S\,pac}}}{L_{\mathrm{s\,pac}}} \\ &+ \frac{\Delta V_{\mathrm{GS\,chip}} - \Delta V_{\mathrm{GS\,ext}} - \Delta V_{n1} - R_{\mathrm{g\,pac}} \cdot \Delta I_{\mathrm{G\,pac}}}{L_{\mathrm{g\,pac}}} \end{aligned} \tag{B.7}$$

as well as

$$\begin{aligned} 0 =& \frac{\Delta V_{\mathrm{DS\,ext}} - \Delta V_{n2} - R_{\mathrm{d\,cir}} \cdot \Delta I_{\mathrm{D\,cir}}}{L_{\mathrm{d\,cir}}} - \frac{\Delta V_{n2} - R_{\mathrm{s\,cir}} \cdot \Delta I_{\mathrm{S\,cir}}}{L_{\mathrm{s\,cir}}} \\ &+ \frac{\Delta V_{\mathrm{GS\,ext}} - \Delta V_{n2} - R_{\mathrm{g\,cir}} \cdot \Delta I_{\mathrm{G\,cir}}}{L_{\mathrm{g\,cir}}} \end{aligned} \tag{B.8}$$

which is solved - with $\Delta I_{\mathrm{S\,pac}} = \Delta I_{\mathrm{D\,pac}} + \Delta I_{\mathrm{G\,pac}}$ and $\Delta I_{\mathrm{S\,cir}} = \Delta I_{\mathrm{D\,cir}} + \Delta I_{\mathrm{G\,cir}}$ - with

$$\begin{aligned}
\Delta V_{n1} =& \frac{L_{\mathrm{g\,pac}} \cdot (L_{\mathrm{d\,pac}} \cdot R_{\mathrm{s\,pac}} - L_{\mathrm{s\,pac}} \cdot R_{\mathrm{d\,pac}}) \cdot \Delta I_{\mathrm{D\,pac}}}{LL_{\mathrm{pac}}} \\
&+ \frac{L_{\mathrm{d\,pac}} \cdot (L_{\mathrm{g\,pac}} \cdot R_{\mathrm{s\,pac}} - L_{\mathrm{s\,pac}} \cdot R_{\mathrm{g\,pac}}) \cdot \Delta I_{\mathrm{G\,pac}}}{LL_{\mathrm{pac}}} \\
&+ \frac{L_{\mathrm{g\,pac}} \cdot L_{\mathrm{s\,pac}} \cdot (\Delta V_{\mathrm{DS\,chip}} - \Delta V_{\mathrm{DS\,ext}})}{LL_{\mathrm{pac}}} \\
&+ \frac{L_{\mathrm{d\,pac}} \cdot L_{\mathrm{s\,pac}} \cdot (\Delta V_{\mathrm{GS\,chip}} - \Delta V_{\mathrm{GS\,ext}})}{LL_{\mathrm{pac}}} \\
\Delta V_{n2} =& \frac{L_{\mathrm{g\,cir}} \cdot (L_{\mathrm{d\,cir}} \cdot R_{\mathrm{s\,cir}} - L_{\mathrm{s\,cir}} \cdot R_{\mathrm{d\,cir}}) \cdot \Delta I_{\mathrm{D\,cir}}}{LL_{\mathrm{cir}}} \\
&+ \frac{L_{\mathrm{d\,cir}} \cdot (L_{\mathrm{g\,cir}} \cdot R_{\mathrm{s\,cir}} - L_{\mathrm{s\,cir}} \cdot R_{\mathrm{g\,cir}}) \cdot \Delta I_{\mathrm{G\,cir}}}{LL_{\mathrm{cir}}} \\
&+ \frac{L_{\mathrm{g\,cir}} \cdot L_{\mathrm{s\,cir}} \cdot \Delta V_{\mathrm{DS\,ext}}}{LL_{\mathrm{cir}}} + \frac{L_{\mathrm{d\,cir}} \cdot L_{\mathrm{s\,cir}} \cdot \Delta V_{\mathrm{GS\,ext}}}{LL_{\mathrm{cir}}}
\end{aligned} \quad \text{and} \quad \text{(B.9)}$$

$$\text{(B.10)}$$

This results in

$$\begin{aligned}
\Delta \dot{I}_{\mathrm{D\,pac}} =& -\frac{(L_{\mathrm{g\,pac}} + L_{\mathrm{s\,pac}}) \cdot R_{\mathrm{d\,pac}} - L_{\mathrm{g\,pac}} \cdot R_{\mathrm{s\,pac}}}{LL_{\mathrm{pac}}} \cdot \Delta I_{\mathrm{D\,pac}} \\
&- \frac{L_{\mathrm{g\,pac}} \cdot R_{\mathrm{s\,pac}} - L_{\mathrm{s\,pac}} \cdot R_{\mathrm{g\,pac}}}{LL_{\mathrm{pac}}} \cdot \Delta I_{\mathrm{G\,pac}} \\
&+ \frac{L_{\mathrm{g\,pac}} + L_{\mathrm{s\,pac}}}{LL_{\mathrm{pac}}} \cdot \Delta V_{\mathrm{DS\,chip}} - \frac{L_{\mathrm{s\,pac}}}{LL_{\mathrm{pac}}} \cdot \Delta V_{\mathrm{GS\,chip}} \\
&- \frac{L_{\mathrm{g\,pac}} + L_{\mathrm{s\,pac}}}{LL_{\mathrm{pac}}} \cdot \Delta V_{\mathrm{DS\,ext}} + \frac{L_{\mathrm{s\,pac}}}{LL_{\mathrm{pac}}} \cdot \Delta V_{\mathrm{GS\,ext}} \\
\Delta \dot{I}_{\mathrm{G\,pac}} =& -\frac{L_{\mathrm{d\,pac}} \cdot R_{\mathrm{s\,pac}} - L_{\mathrm{s\,pac}} \cdot R_{\mathrm{d\,pac}}}{LL_{\mathrm{pac}}} \cdot \Delta I_{\mathrm{D\,pac}} \\
&- \frac{(L_{\mathrm{d\,pac}} + L_{\mathrm{s\,pac}}) \cdot R_{\mathrm{g\,pac}} - L_{\mathrm{d\,pac}} \cdot R_{\mathrm{s\,pac}}}{LL_{\mathrm{pac}}} \cdot \Delta I_{\mathrm{G\,pac}} \\
&- \frac{L_{\mathrm{s\,pac}}}{LL_{\mathrm{pac}}} \cdot \Delta V_{\mathrm{DS\,chip}} + \frac{L_{\mathrm{d\,pac}} + L_{\mathrm{s\,pac}}}{LL_{\mathrm{pac}}} \cdot \Delta V_{\mathrm{GS\,chip}} \\
&+ \frac{L_{\mathrm{s\,pac}}}{LL_{\mathrm{pac}}} \cdot \Delta V_{\mathrm{DS\,ext}} - \frac{L_{\mathrm{d\,pac}} + L_{\mathrm{s\,pac}}}{LL_{\mathrm{pac}}} \cdot \Delta V_{\mathrm{GS\,ext}}
\end{aligned} \quad \text{and} \quad \text{(B.11)}$$

$$\text{(B.12)}$$

as well as

$$\begin{aligned}
\Delta \dot{I}_{\mathrm{D\,cir}} =& -\frac{(L_{\mathrm{g\,cir}} + L_{\mathrm{s\,cir}}) \cdot R_{\mathrm{d\,cir}} - L_{\mathrm{g\,cir}} \cdot R_{\mathrm{s\,cir}}}{LL_{\mathrm{cir}}} \cdot \Delta I_{\mathrm{D\,cir}} \\
&- \frac{L_{\mathrm{g\,cir}} \cdot R_{\mathrm{s\,cir}} - L_{\mathrm{s\,cir}} \cdot R_{\mathrm{g\,cir}}}{LL_{\mathrm{cir}}} \cdot \Delta I_{\mathrm{G\,cir}} \\
&+ \frac{L_{\mathrm{g\,cir}} + L_{\mathrm{s\,cir}}}{LL} \cdot \Delta V_{\mathrm{DS\,ext}} - \frac{L_{\mathrm{s\,cir}}}{LL_{\mathrm{cir}}} \cdot \Delta V_{\mathrm{GS\,ext}}
\end{aligned} \quad \text{and} \quad \text{(B.13)}$$

$$\begin{aligned}\dot{\Delta I}_{\mathrm{G\,cir}} = &- \frac{L_{\mathrm{d\,cir}} \cdot R_{\mathrm{s\,cir}} - L_{\mathrm{s\,cir}} \cdot R_{\mathrm{d\,cir}}}{LL_{\mathrm{cir}}} \cdot \Delta I_{\mathrm{D\,cir}} \\ &- \frac{(L_{\mathrm{d\,cir}} + L_{\mathrm{s\,cir}}) \cdot R_{\mathrm{g\,cir}} - L_{\mathrm{d\,cir}} \cdot R_{\mathrm{s\,cir}}}{LL_{\mathrm{cir}}} \cdot \Delta I_{\mathrm{G\,cir}}. \\ &- \frac{L_{\mathrm{s\,cir}}}{LL_{\mathrm{cir}}} \cdot \Delta V_{\mathrm{DS\,ext}} + \frac{L_{\mathrm{d\,cir}} + L_{\mathrm{s\,cir}}}{LL_{\mathrm{cir}}} \cdot \Delta V_{\mathrm{GS\,ext}}\end{aligned} \tag{B.14}$$

According to Fig. B.1, the application of KIRCHHOFF's laws results in

$$g_{\mathrm{ds}} \cdot \Delta V_{\mathrm{DS\,chip}} + g_{\mathrm{m}} \cdot \Delta V_{\mathrm{GS\,chip}} + \Delta I_{\mathrm{DS\,chip}} + \Delta I_{\mathrm{D\,pac}} + \Delta I_{\mathrm{DG\,chip}} = 0, \tag{B.15}$$

$$\Delta I_{\mathrm{DG\,chip}} - \Delta I_{\mathrm{G\,pac}} - \Delta I_{\mathrm{GS\,chip}} = 0 \text{ and} \tag{B.16}$$

$$\frac{\Delta I_{\mathrm{DS\,chip}}}{C_{\mathrm{ds\,chip}}} - \frac{\Delta I_{\mathrm{DG\,chip}}}{C_{\mathrm{dg\,chip}}} - \frac{\Delta i_{\mathrm{GS\,chip}}}{C_{\mathrm{gs\,chip}}} = 0 \tag{B.17}$$

as well as

$$\Delta I_{\mathrm{DS\,ext}} + \Delta I_{\mathrm{D\,cir}} + \Delta I_{\mathrm{DG\,ext}} - \Delta I_{\mathrm{D\,pac}} = 0, \tag{B.18}$$

$$\Delta I_{\mathrm{DG\,ext}} + \Delta I_{\mathrm{G\,pac}} - \Delta I_{\mathrm{G\,cir}} - \Delta I_{\mathrm{GS\,ext}} = 0 \text{ and} \tag{B.19}$$

$$\frac{\Delta I_{\mathrm{DS\,ext}}}{C_{\mathrm{ds\,ext}}} - \frac{\Delta I_{\mathrm{DG\,ext}}}{C_{\mathrm{dg\,ext}}} - \frac{\Delta I_{\mathrm{GS\,ext}}}{C_{\mathrm{gs\,ext}}} = 0. \tag{B.20}$$

The equations are solved with

$$\begin{aligned}\Delta I_{\mathrm{DS\,chip}} = &- \frac{C_{\mathrm{ds\,chip}} \cdot (C_{\mathrm{dg\,chip}} + C_{\mathrm{gs\,chip}})}{CC_{\mathrm{chip}}} \cdot \Delta I_{\mathrm{D\,pac}} \\ &- \frac{C_{\mathrm{ds\,chip}} \cdot C_{\mathrm{dg\,chip}}}{CC_{\mathrm{chip}}} \cdot \Delta I_{\mathrm{G\,pac}} \\ &- \frac{C_{\mathrm{ds\,chip}} \cdot (C_{\mathrm{dg\,chip}} + C_{\mathrm{gs\,chip}}) \cdot g_{\mathrm{ds}}}{CC_{\mathrm{chip}}} \cdot \Delta V_{\mathrm{DS\,chip}} \\ &- \frac{C_{\mathrm{ds\,chip}} \cdot (C_{\mathrm{dg\,chip}} + C_{\mathrm{gs\,chip}}) \cdot g_{\mathrm{m}}}{CC_{\mathrm{chip}}} \cdot \Delta V_{\mathrm{GS\,chip}}\end{aligned} \quad \text{and} \tag{B.21}$$

$$\begin{aligned}\Delta I_{\mathrm{GS\,chip}} = &- \frac{C_{\mathrm{gs\,chip}} \cdot C_{\mathrm{dg\,chip}}}{CC_{\mathrm{chip}}} \cdot \Delta I_{\mathrm{D\,pac}} \\ &- \frac{C_{\mathrm{gs\,chip}} \cdot (C_{\mathrm{dg\,chip}} + C_{\mathrm{ds\,chip}})}{CC_{\mathrm{chip}}} \cdot \Delta I_{\mathrm{G\,pac}} \\ &- \frac{C_{\mathrm{gs\,chip}} \cdot C_{\mathrm{dg\,chip}} \cdot g_{\mathrm{ds}}}{CC_{\mathrm{chip}}} \cdot \Delta V_{\mathrm{DS\,chip}} \\ &- \frac{C_{\mathrm{gs\,chip}} \cdot C_{\mathrm{dg\,chip}} \cdot g_{\mathrm{m}}}{CC_{\mathrm{chip}}} \cdot \Delta V_{\mathrm{GS\,chip}}\end{aligned} \tag{B.22}$$

as well as

$$\begin{aligned}\Delta I_{\mathrm{DS\,ext}} =& \frac{C_{\mathrm{ds\,ext}} \cdot (C_{\mathrm{dg\,ext}} + C_{\mathrm{gs\,ext}})}{CC_{\mathrm{ext}}} \cdot \Delta I_{\mathrm{D\,pac}} + \frac{C_{\mathrm{ds\,ext}} \cdot C_{\mathrm{dg\,ext}}}{CC_{\mathrm{ext}}} \cdot \Delta I_{\mathrm{G\,pac}} \\ & - \frac{C_{\mathrm{ds\,ext}} \cdot (C_{\mathrm{dg\,ext}} + C_{\mathrm{gs\,ext}})}{CC_{\mathrm{ext}}} \cdot \Delta I_{\mathrm{D\,cir}} - \frac{C_{\mathrm{ds\,ext}} \cdot C_{\mathrm{dg\,ext}}}{CC_{\mathrm{ext}}} \cdot \Delta I_{\mathrm{G\,cir}}\end{aligned} \quad \text{and} \tag{B.23}$$

$$\begin{aligned}\Delta I_{\mathrm{GS\,ext}} =& \frac{C_{\mathrm{gs\,ext}} \cdot C_{\mathrm{dg\,ext}}}{CC_{\mathrm{ext}}} \cdot \Delta I_{\mathrm{D\,pac}} + \frac{(C_{\mathrm{dg\,ext}} + C_{\mathrm{ds\,ext}}) \cdot C_{\mathrm{gs\,ext}}}{CC_{\mathrm{ext}}} \cdot \Delta I_{\mathrm{G\,pac}} \\ & - \frac{C_{\mathrm{gs\,ext}} \cdot C_{\mathrm{dg\,ext}}}{CC_{\mathrm{ext}}} \cdot \Delta I_{\mathrm{D\,cir}} - \frac{(C_{\mathrm{dg\,ext}} + C_{\mathrm{ds\,ext}}) \cdot C_{\mathrm{gs\,ext}}}{CC_{\mathrm{ext}}} \cdot \Delta I_{\mathrm{G\,cir}}\end{aligned} . \tag{B.24}$$

The time derivatives of the voltages across the capacitances are given by

$$\begin{aligned}\dot{\Delta V}_{\mathrm{DS\,chip}} =& - \frac{C_{\mathrm{dg\,chip}} + C_{\mathrm{gs\,chip}}}{CC_{\mathrm{chip}}} \cdot \Delta I_{\mathrm{D\,pac}} - \frac{C_{\mathrm{dg\,chip}}}{CC_{\mathrm{chip}}} \cdot \Delta I_{\mathrm{G\,pac}} \\ & - \frac{(C_{\mathrm{dg\,chip}} + C_{\mathrm{gs\,chip}}) \cdot g_{\mathrm{ds}}}{CC_{\mathrm{chip}}} \cdot \Delta V_{\mathrm{DS\,chip}} \\ & - \frac{(C_{\mathrm{dg\,chip}} + C_{\mathrm{gs\,chip}}) \cdot g_{\mathrm{m}}}{CC_{\mathrm{chip}}} \cdot \Delta V_{\mathrm{GS\,chip}}\end{aligned} \quad \text{and} \tag{B.25}$$

$$\begin{aligned}\dot{\Delta V}_{\mathrm{GS\,chip}} =& - \frac{C_{\mathrm{dg\,chip}}}{CC_{\mathrm{chip}}} \cdot \Delta I_{\mathrm{D\,pac}} - \frac{C_{\mathrm{dg\,chip}} + C_{\mathrm{ds\,chip}}}{CC_{\mathrm{chip}}} \cdot \Delta I_{\mathrm{G\,pac}} \\ & - \frac{C_{\mathrm{dg\,chip}} \cdot g_{\mathrm{ds}}}{CC_{\mathrm{chip}}} \cdot \Delta V_{\mathrm{DS\,chip}} - \frac{C_{\mathrm{dg\,chip}} \cdot g_{\mathrm{m}}}{CC_{\mathrm{chip}}} \cdot \Delta V_{\mathrm{GS\,chip}}\end{aligned} \tag{B.26}$$

as well as

$$\begin{aligned}\dot{\Delta V}_{\mathrm{DS\,ext}} =& \frac{C_{\mathrm{dg\,ext}} + C_{\mathrm{gs\,ext}}}{CC_{\mathrm{ext}}} \cdot \Delta I_{\mathrm{D\,pac}} + \frac{C_{\mathrm{dg\,ext}}}{CC_{\mathrm{ext}}} \cdot \Delta I_{\mathrm{G\,pac}} \\ & - \frac{C_{\mathrm{dg\,ext}} + C_{\mathrm{gs\,ext}}}{CC_{\mathrm{ext}}} \cdot \Delta I_{\mathrm{D\,cir}} - \frac{C_{\mathrm{dg\,ext}}}{CC_{\mathrm{ext}}} \cdot \Delta I_{\mathrm{G\,cir}}\end{aligned} \quad \text{and} \tag{B.27}$$

$$\begin{aligned}\dot{\Delta V}_{\mathrm{GS\,ext}} =& \frac{C_{\mathrm{dg\,ext}}}{CC_{\mathrm{ext}}} \cdot \Delta I_{\mathrm{D\,pac}} + \frac{C_{\mathrm{dg\,ext}} + C_{\mathrm{ds\,ext}}}{CC_{\mathrm{ext}}} \cdot \Delta I_{\mathrm{G\,pac}} \\ & - \frac{C_{\mathrm{dg\,ext}}}{CC_{\mathrm{ext}}} \cdot \Delta I_{\mathrm{D\,cir}} - \frac{C_{\mathrm{dg\,ext}} + C_{\mathrm{ds\,ext}}}{CC_{\mathrm{ext}}} \cdot \Delta I_{\mathrm{G\,cir}}\end{aligned} . \tag{B.28}$$

With it, the elements of the model's system matrix $\boldsymbol{A}$ are determined (cp. the coefficients in (B.11) through (B.14) and in (B.25) through (B.28) with the matrix elements in Table 5.1).

B.2 System Matrix of the Simplified Small-Signal Equivalent Circuit Model

In Fig. B.2, the simplified small-signal equivalent circuit of the regarded buck converter topology is shown.[1] For the determination of the circuit's system matrix $\boldsymbol{A}$, the corresponding differential state space equation system $\dot{\vec{x}} = \boldsymbol{A} \cdot \vec{x}$ is needed. Subsequently, the state space equation system is derived. Thereby, the following definitions are used:

$$CC_{\text{chip}} = C_{\text{dg chip}} \cdot C_{\text{ds chip}} + C_{\text{gs chip}} \cdot C_{\text{dg chip}} + C_{\text{ds chip}} \cdot C_{\text{gs chip}} \text{ and}$$
$$LL = L_{\text{g}} \cdot L_{\text{s}} + L_{\text{d}} \cdot L_{\text{g}} + L_{\text{s}} \cdot L_{\text{d}}.$$

With respect to the small-signal circuit in Fig. B.2, the time derivatives of currents through the inductances are given by

$$\Delta\dot{I}_{\text{D}} = \frac{\Delta V_{\text{DS chip}} - \Delta V_n}{L_{\text{d}}}, \tag{B.29}$$

$$\Delta\dot{I}_{\text{G}} = \frac{\Delta V_{\text{GS chip}} - \Delta V_n - R_{\text{g}} \cdot \Delta I_{\text{G}}}{L_{\text{g}}} \text{ and} \tag{B.30}$$

$$\Delta\dot{I}_{\text{S}} = \frac{\Delta V_n}{L_{\text{s}}}. \tag{B.31}$$

The application of KIRCHHOFF's current law results in

$$\frac{\Delta V_{\text{DS chip}} - \Delta V_n}{L_{\text{d}}} + \frac{\Delta V_{\text{GS chip}} - \Delta V_n - R_{\text{g}} \cdot \Delta I_{\text{G}}}{L_{\text{g}}} - \frac{\Delta V_n}{L_{\text{s}}} = 0 \tag{B.32}$$

which is solved with

$$\Delta V_n = -\frac{L_{\text{d}} \cdot L_{\text{s}} \cdot R_{\text{g}} \cdot \Delta I_{\text{G}}}{LL} + \frac{L_{\text{d}} \cdot L_{\text{s}} \cdot \Delta V_{\text{GS chip}}}{LL} + \frac{L_{\text{g}} \cdot L_{\text{s}} \cdot \Delta V_{\text{DS chip}}}{LL} \tag{B.33}$$

and therewith leads to

$$\Delta\dot{I}_{\text{D}} = \frac{L_{\text{s}} \cdot R_{\text{g}}}{LL} \cdot \Delta I_{\text{G}} + \frac{L_{\text{g}} + L_{\text{s}}}{LL} \cdot \Delta V_{\text{DS chip}} - \frac{L_{\text{s}}}{LL} \cdot \Delta V_{\text{GS chip}} \text{ and} \tag{B.34}$$

$$\Delta\dot{I}_{\text{G}} = -\frac{(L_{\text{d}} + L_{\text{s}}) \cdot R_{\text{g}}}{LL} \cdot \Delta I_{\text{G}} - \frac{L_{\text{s}}}{LL} \cdot \Delta V_{\text{DS chip}} + \frac{L_{\text{d}} + L_{\text{s}}}{LL} \cdot \Delta V_{\text{GS chip}}. \tag{B.35}$$

According to Fig. B.2, the application of KIRCHHOFF's laws results in

$$g_{\text{m}} \cdot \Delta V_{\text{GS chip}} + \Delta I_{\text{DS chip}} + \Delta I_{\text{D}} + \Delta I_{\text{DG chip}} = 0, \tag{B.36}$$

$$\Delta I_{\text{DG chip}} - \Delta I_{\text{G}} - \Delta I_{\text{GS chip}} = 0 \text{ and} \tag{B.37}$$

$$\frac{\Delta I_{\text{DS chip}}}{C_{\text{ds chip}}} - \frac{\Delta I_{\text{DG chip}}}{C_{\text{dg chip}}} - \frac{\Delta I_{\text{GS chip}}}{C_{\text{gs chip}}} = 0. \tag{B.38}$$

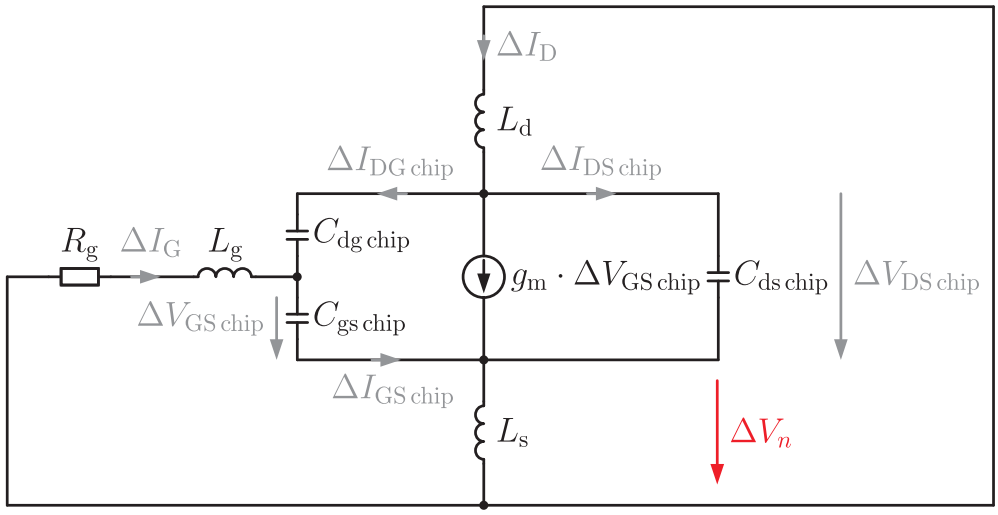


Figure B.2: Simplified small-signal equivalent circuit model of a buck converter topology's operating points

The equations are solved with

$$\begin{aligned}\Delta I_{\mathrm{DS\,chip}} = &- \frac{C_{\mathrm{ds\,chip}} \cdot (C_{\mathrm{dg\,chip}} + C_{\mathrm{gs\,chip}}) \cdot \Delta I_\mathrm{D}}{CC_\mathrm{chip}} + \frac{C_{\mathrm{ds\,chip}} \cdot C_{\mathrm{dg\,chip}} \cdot \Delta I_\mathrm{G}}{CC_\mathrm{chip}} \\ &+ \frac{C_{\mathrm{ds\,chip}} \cdot (C_{\mathrm{dg\,chip}} + C_{\mathrm{gs\,chip}}) \cdot g_\mathrm{m} \cdot \Delta V_{\mathrm{GS\,chip}}}{CC_\mathrm{chip}}\end{aligned} \tag{B.39}$$

and

$$\begin{aligned}\Delta I_{\mathrm{GS\,chip}} = &- \frac{C_{\mathrm{gs\,chip}} \cdot C_{\mathrm{dg\,chip}}}{CC_\mathrm{chip}} \cdot \Delta I_\mathrm{D} + \frac{C_{\mathrm{gs\,chip}} \cdot (C_{\mathrm{dg\,chip}} + C_{\mathrm{ds\,chip}})}{CC_\mathrm{chip}} \cdot \Delta I_\mathrm{G} \\ &+ \frac{C_{\mathrm{gs\,chip}} \cdot C_{\mathrm{dg\,chip}} \cdot g_\mathrm{m}}{CC_\mathrm{chip}} \cdot \Delta V_{\mathrm{GS\,chip}}\end{aligned} . \tag{B.40}$$

The time derivatives of the voltages across the capacitances are given by

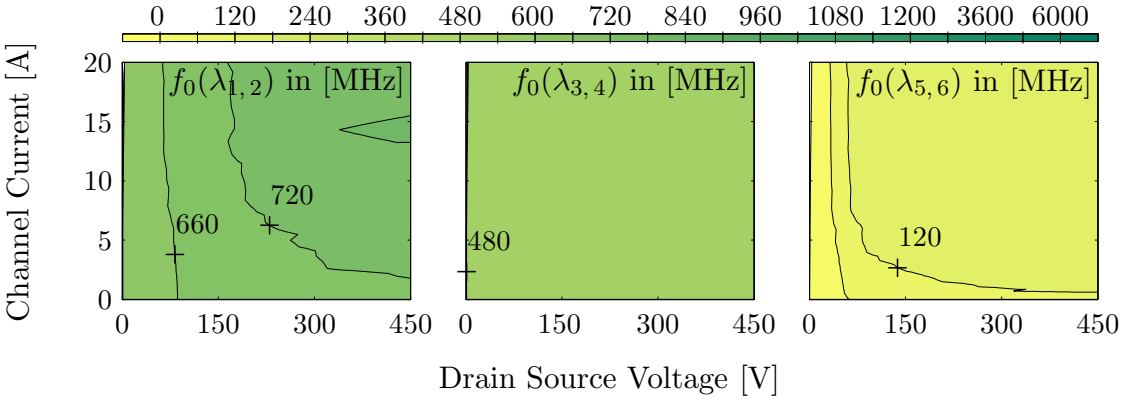
$$\begin{aligned}\dot{\Delta V}_{\mathrm{DS\,chip}} = &- \frac{C_{\mathrm{dg\,chip}} + C_{\mathrm{gs\,chip}}}{CC_\mathrm{chip}} \cdot \Delta I_\mathrm{D} - \frac{C_{\mathrm{dg\,chip}}}{CC_\mathrm{chip}} \cdot \Delta I_\mathrm{G} \\ &- \frac{(C_{\mathrm{dg\,chip}} + C_{\mathrm{gs\,chip}}) \cdot g_\mathrm{m}}{CC_\mathrm{chip}} \cdot \Delta V_{\mathrm{GS\,chip}}\end{aligned} \quad \text{and} \tag{B.41}$$

$$\begin{aligned}\dot{\Delta V}_{\mathrm{GS\,chip}} = &- \frac{C_{\mathrm{dg\,chip}}}{CC_\mathrm{chip}} \cdot \Delta I_\mathrm{D} - \frac{C_{\mathrm{dg\,chip}} + C_{\mathrm{ds\,chip}}}{CC_\mathrm{chip}} \cdot \Delta I_\mathrm{G} \\ &- \frac{C_{\mathrm{dg\,chip}} \cdot g_\mathrm{m}}{CC_\mathrm{chip}} \cdot \Delta V_{\mathrm{GS\,chip}}\end{aligned} . \tag{B.42}$$

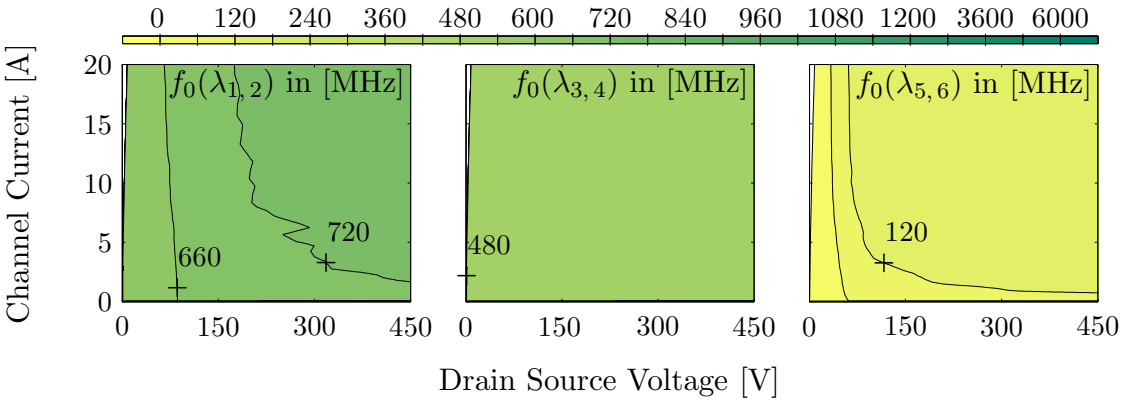
With it, the elements of the model's system matrix $\boldsymbol{A}$ are determined (cp. the coefficients in (B.34) and (B.35) and in (B.41) and (B.42) with the matrix elements in Table 5.5).

C Impact of the Circuit Elements on the Eigenfrequencies

The following figures correspond to Fig. 5.4 through Fig. 5.23 in subsection **5.2.4**, in which the impact of the small-signal equivalent circuit elements on the cosine phi's is analyzed.

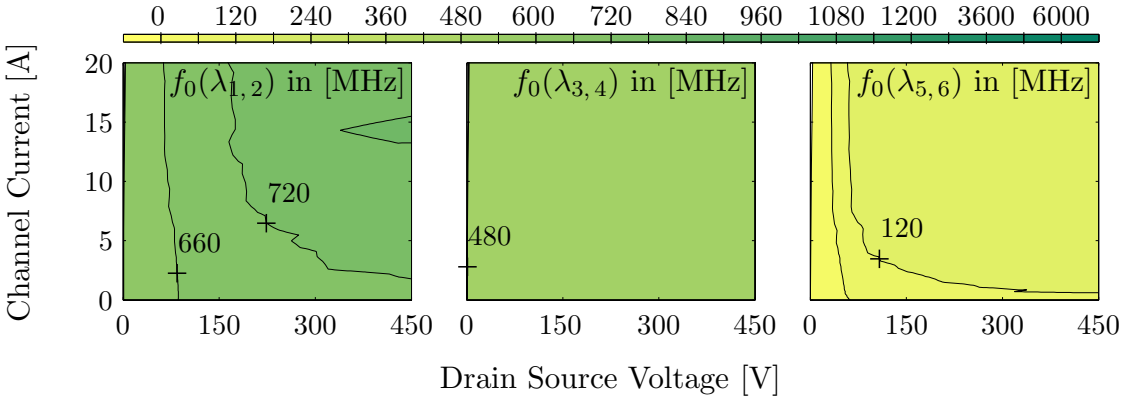


(a) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ of the initial parameterization

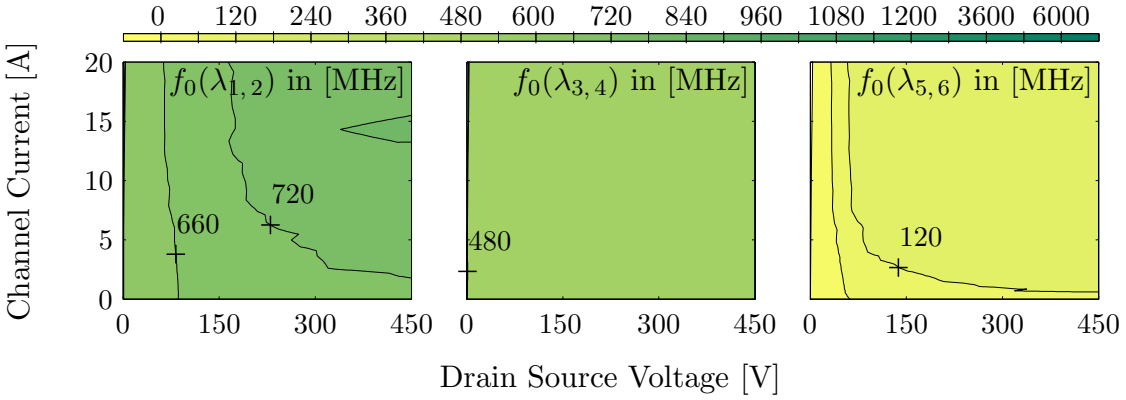


(b) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $\vartheta_J = 125\,°C$

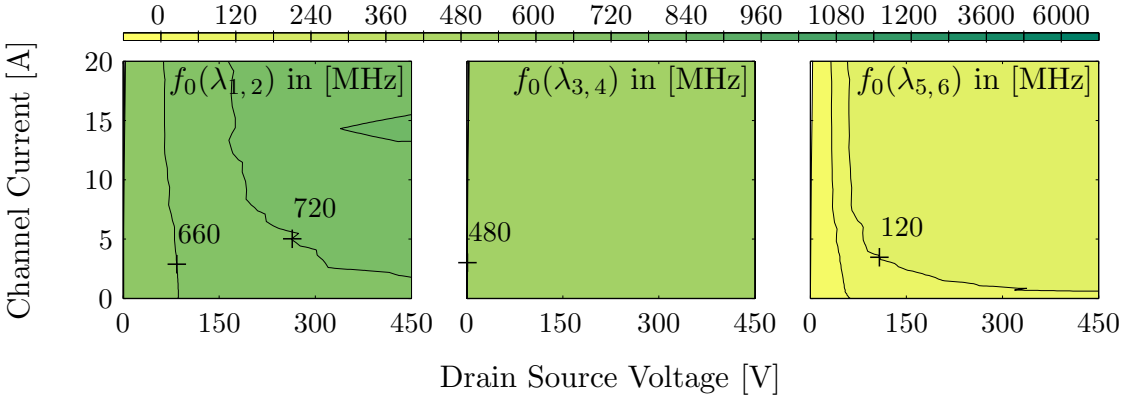
Figure C.1: Impact of the MOSFET's junction temperature T_J on the eigenfrequencies of the conjugate-complex eigenvalues of a buck converter topology's operating points in the MOSFET's operating range



(a) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $0.2 \cdot g_\mathrm{m}(V_\mathrm{DS\,chip}, V_\mathrm{GS\,chip})$

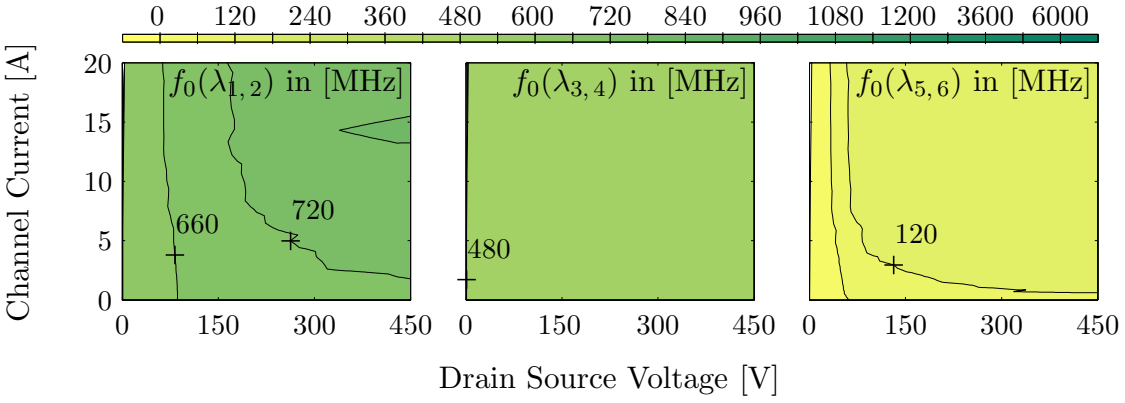


(b) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ of the initial parameterization

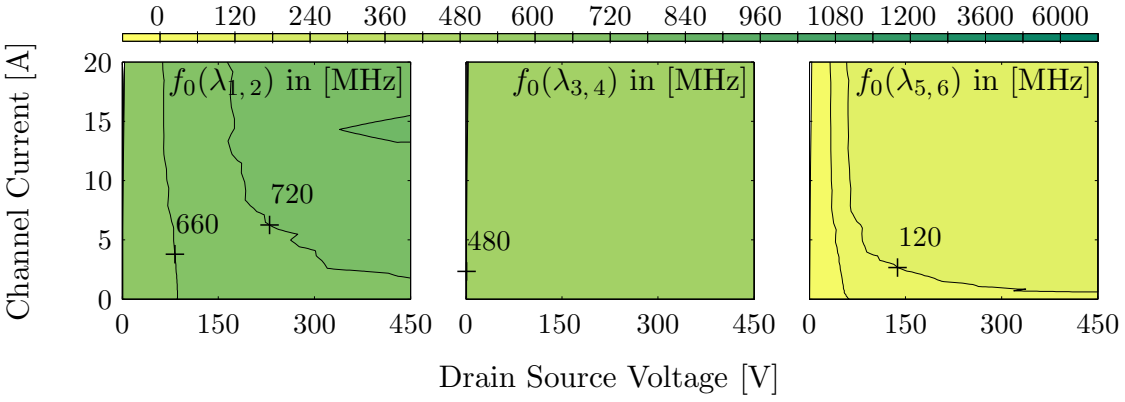


(c) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $5 \cdot g_\mathrm{m}(V_\mathrm{DS\,chip}, V_\mathrm{GS\,chip})$

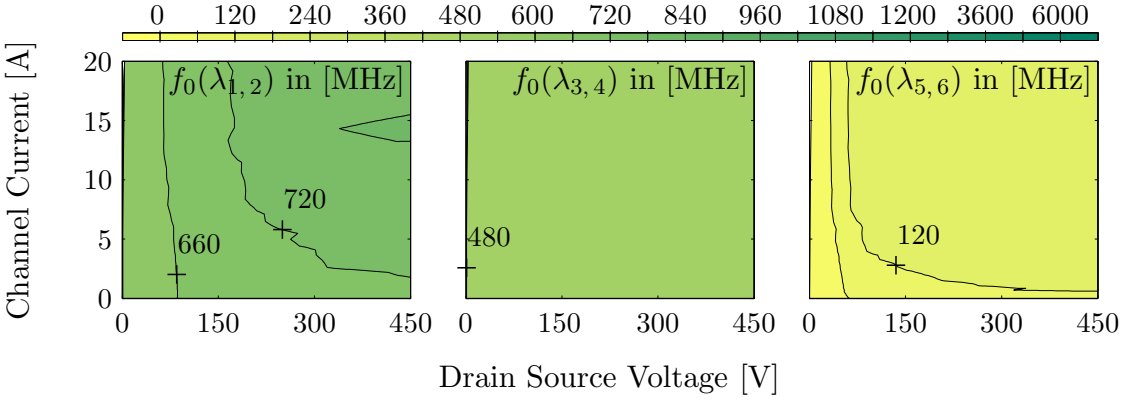
Figure C.2: Impact of the MOSFET's transconductance characteristic $g_\mathrm{m}(V_\mathrm{DS\,chip}, V_\mathrm{GS\,chip})$ on the eigenfrequencies of the conjugate-complex eigenvalues of a buck converter topology's operating points in the MOSFET's operating range



(a) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $0.2 \cdot g_{\mathrm{ds}}(V_{\mathrm{DS\,chip}}, V_{\mathrm{GS\,chip}})$

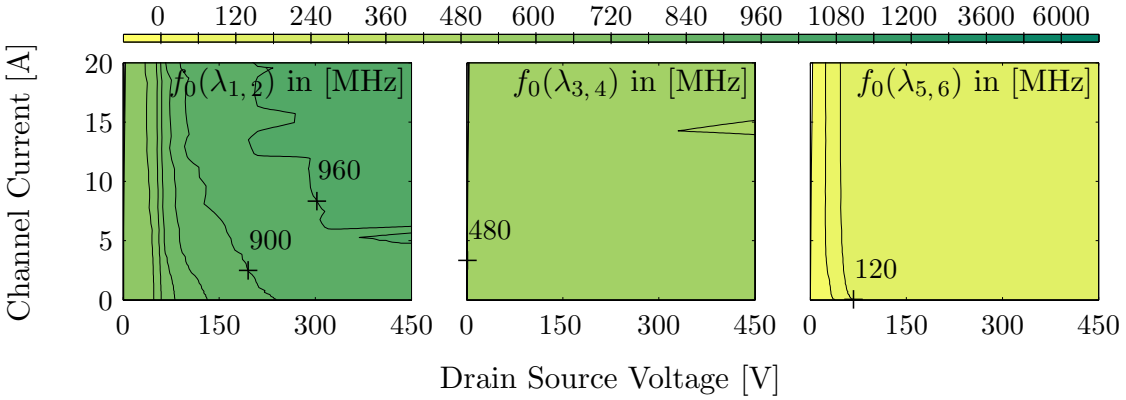


(b) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ of the initial parameterization

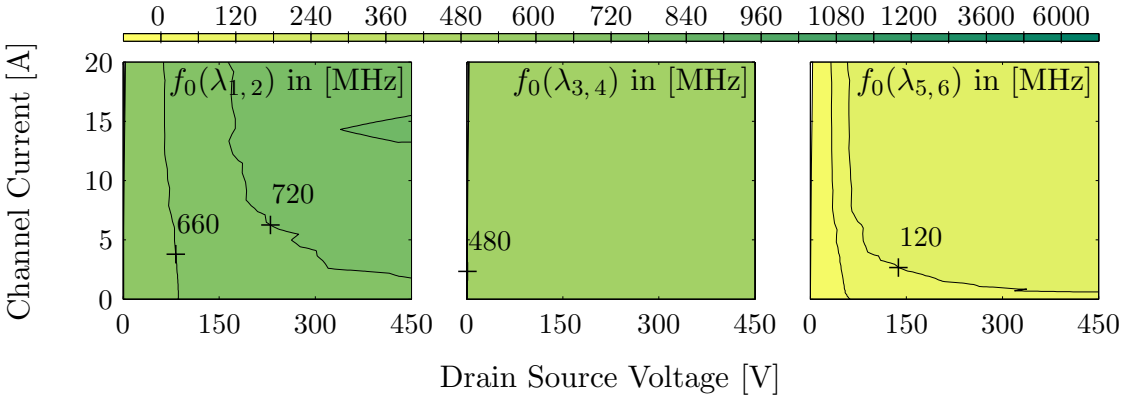


(c) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $5 \cdot g_{\mathrm{ds}}(V_{\mathrm{DS\,chip}}, V_{\mathrm{GS\,chip}})$

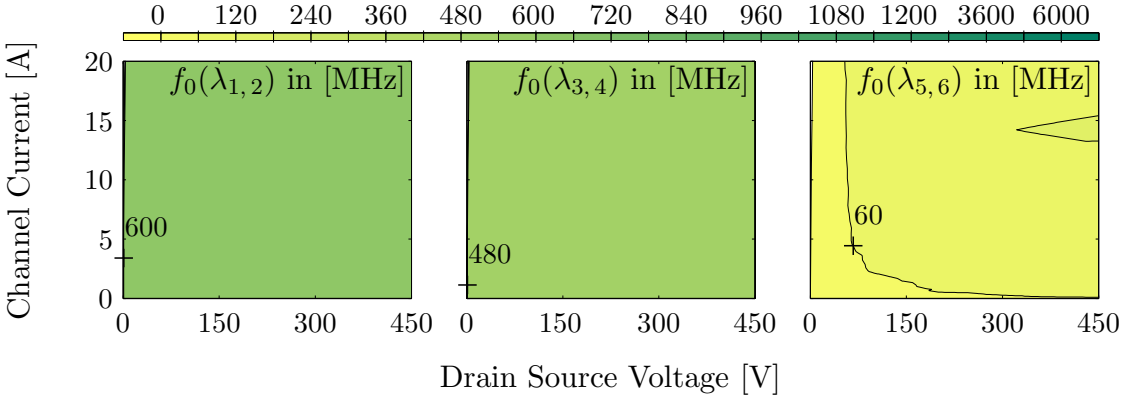
Figure C.3: Impact of the MOSFET's conductance characteristic $g_{\mathrm{ds}}(V_{\mathrm{DS\,chip}}, V_{\mathrm{GS\,chip}})$ on the eigenfrequencies of the conjugate-complex eigenvalues of a buck converter topology's operating points in the MOSFET's operating range



(a) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $0.2 \cdot C_{\mathrm{ds\,chip}}(V_{\mathrm{DS\,chip}})$

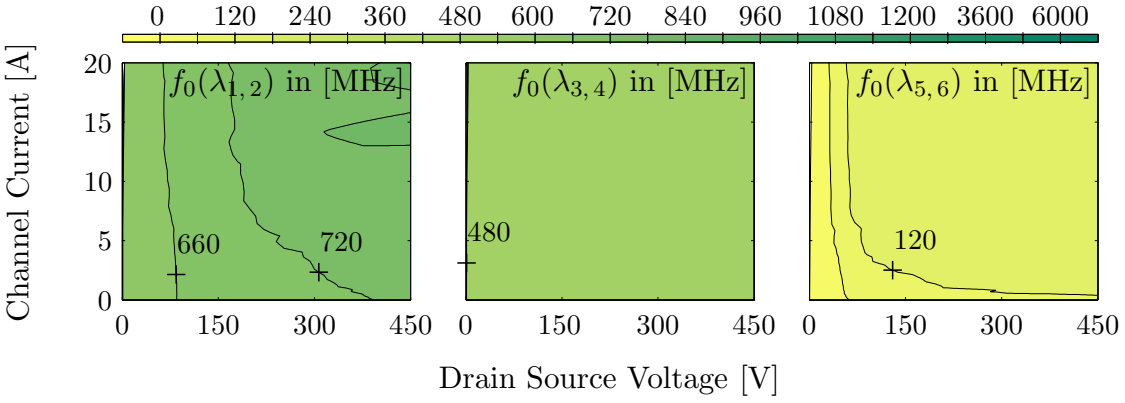


(b) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ of the initial parameterization

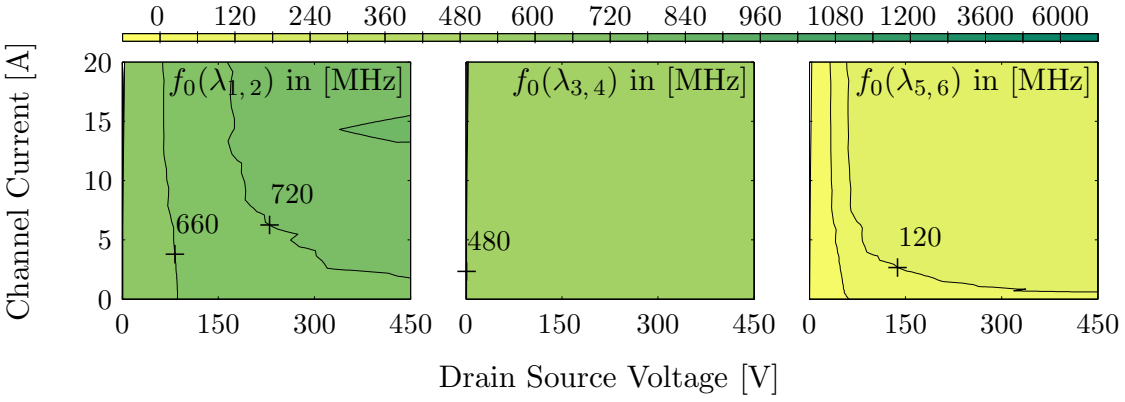


(c) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $5 \cdot C_{\mathrm{ds\,chip}}(V_{\mathrm{DS\,chip}})$

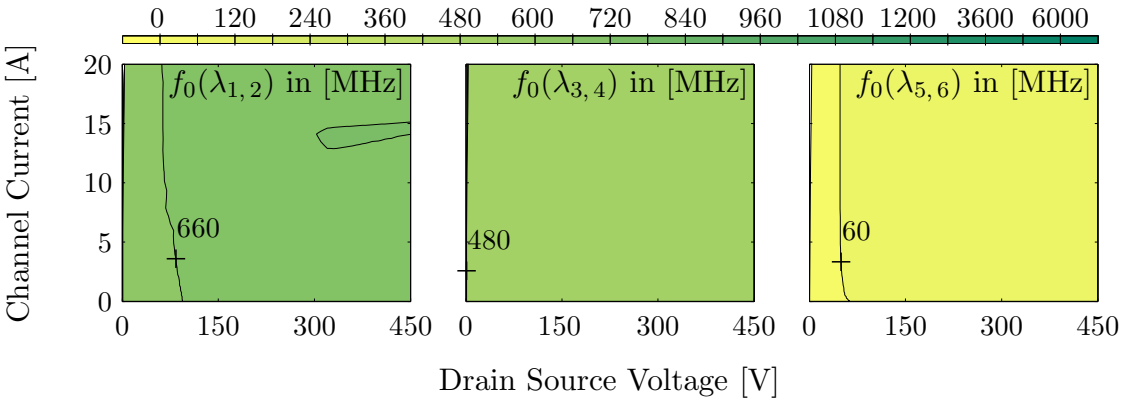
Figure C.4: Impact of the drain source capacitance characteristic $C_{\mathrm{ds\,chip}}(V_{\mathrm{DS\,chip}})$ on the eigenfrequencies of the conjugate-complex eigenvalues of a buck converter topology's operating points in the MOSFET's operating range



(a) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $0.2 \cdot C_{\mathrm{dg\,chip}}(V_{\mathrm{DS\,chip}})$

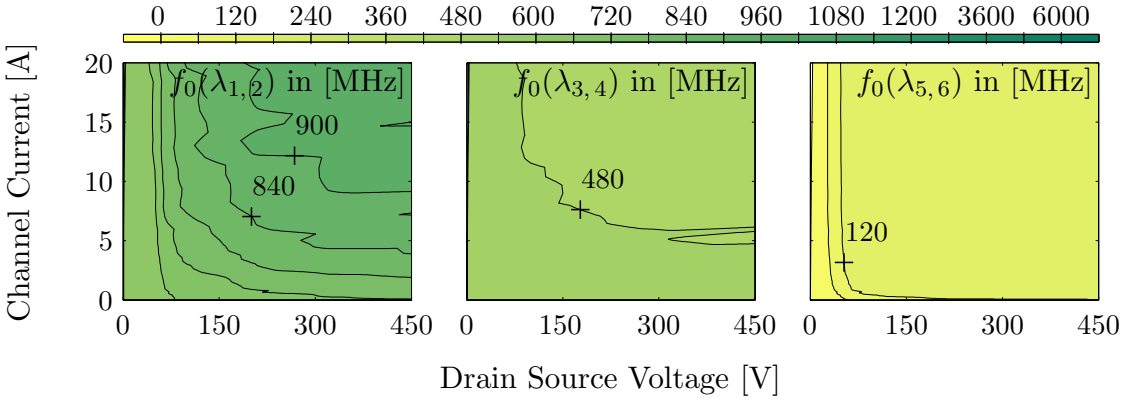


(b) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ of the initial parameterization

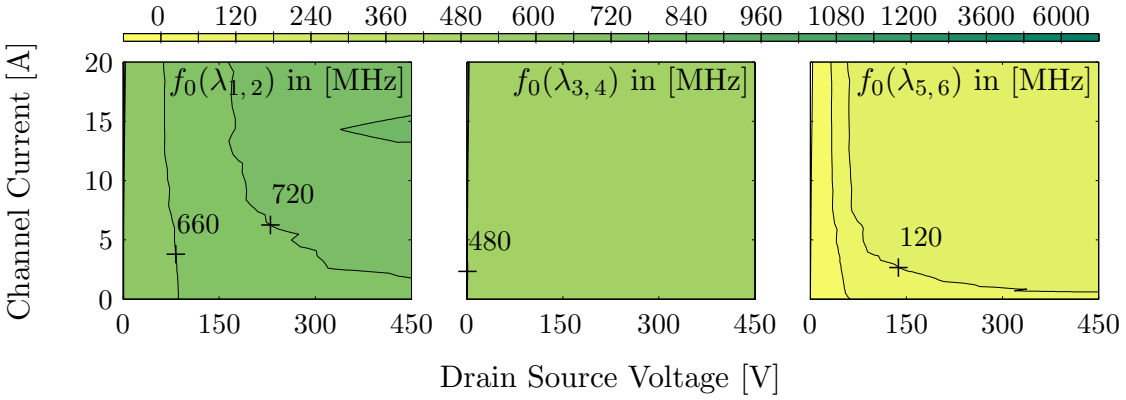


(c) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $5 \cdot C_{\mathrm{dg\,chip}}(V_{\mathrm{DS\,chip}})$

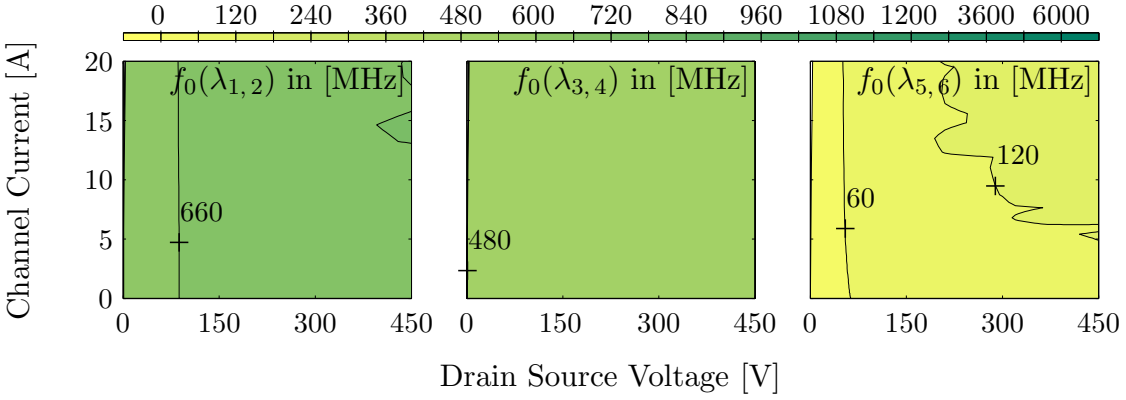
Figure C.5: Impact of the drain gate capacitance characteristic $C_{\mathrm{dg\,chip}}(V_{\mathrm{DS\,chip}})$ on the eigenfrequencies of the conjugate-complex eigenvalues of a buck converter topology's operating points in the MOSFET's operating range



(a) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $0.2 \cdot C_{\text{gs chip}} = 0.294\,\text{nF}$

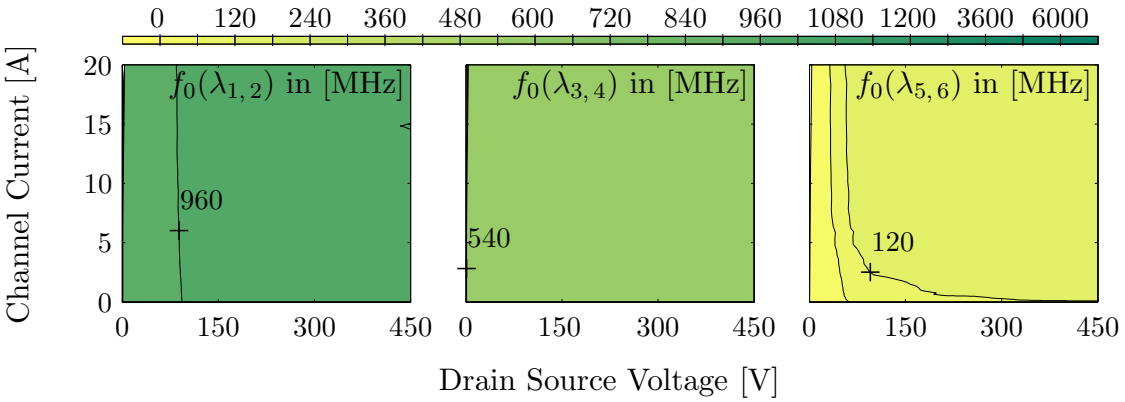


(b) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ of the initial parameterization

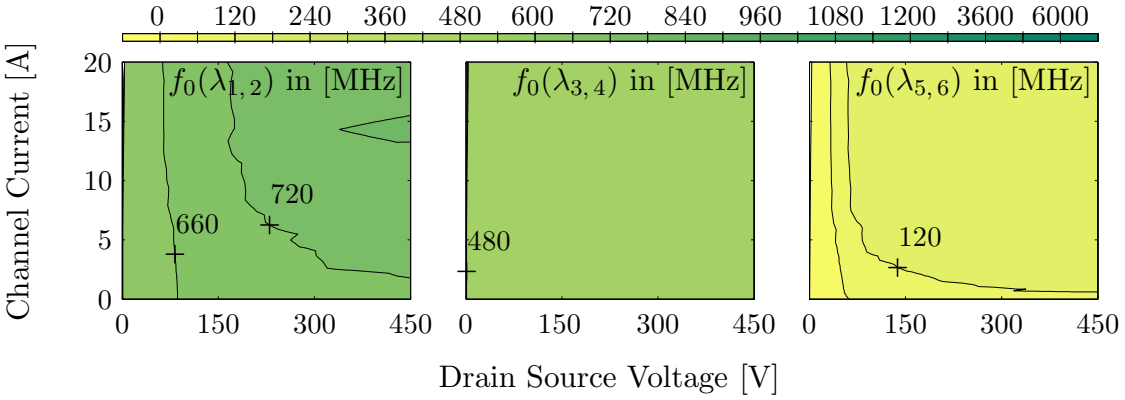


(c) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $5 \cdot C_{\text{gs chip}} = 7.35\,\text{nF}$

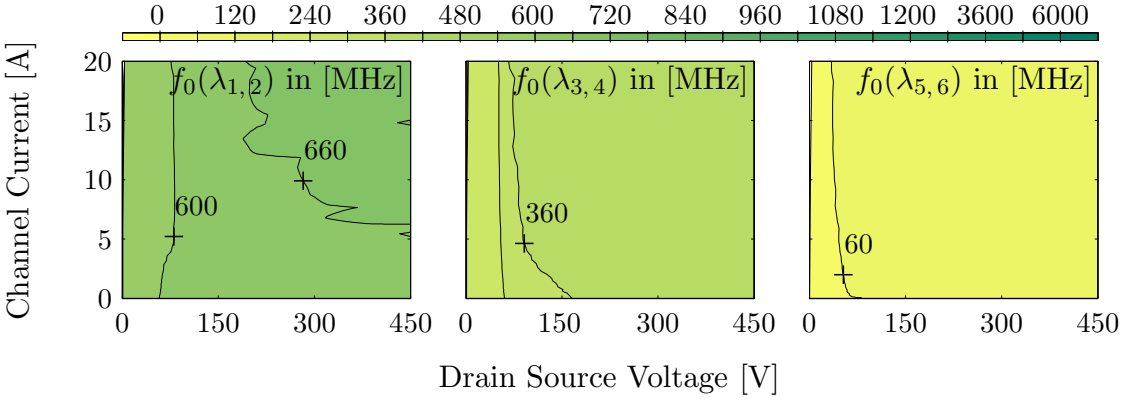
Figure C.6: Impact of the MOSFET's gate source capacitance $C_{\text{gs chip}}$ on the eigenfrequencies of the conjugate-complex eigenvalues of a buck converter topology's operating points in the MOSFET's operating range



(a) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $0.2 \cdot C_{\mathrm{ds\,ext}} = 3\,\mathrm{pF}$

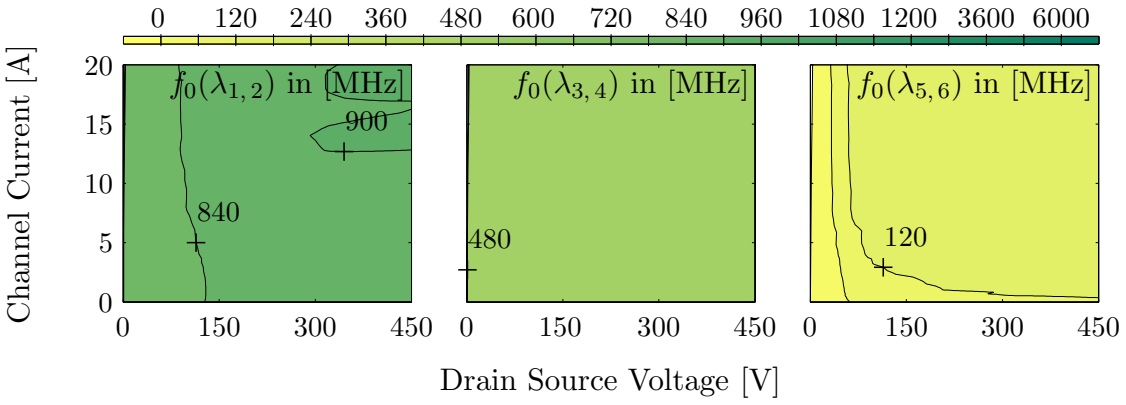


(b) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ of the initial parameterization

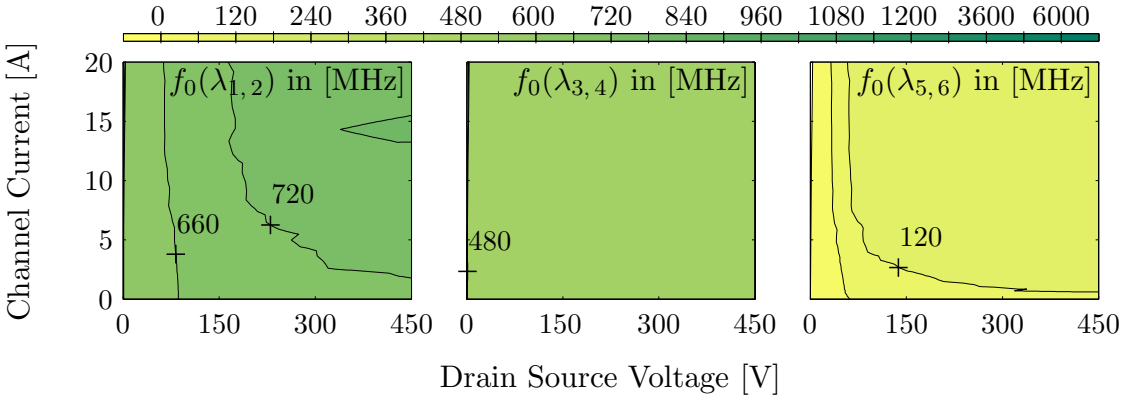


(c) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $5 \cdot C_{\mathrm{ds\,ext}} = 75\,\mathrm{pF}$

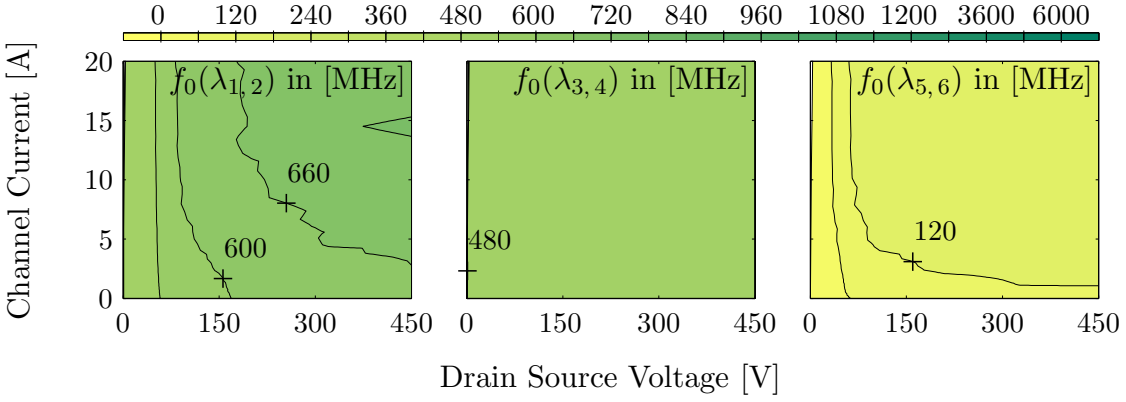
Figure C.7: Impact of the chip-external drain source capacitance $C_{\mathrm{ds\,ext}}$ on the eigenfrequencies of the conjugate-complex eigenvalues of a buck converter topology's operating points in the MOSFET's operating range



(a) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $0.02 \cdot C_{\mathrm{dg\,ext}} = 0.1\,\mathrm{pF}$

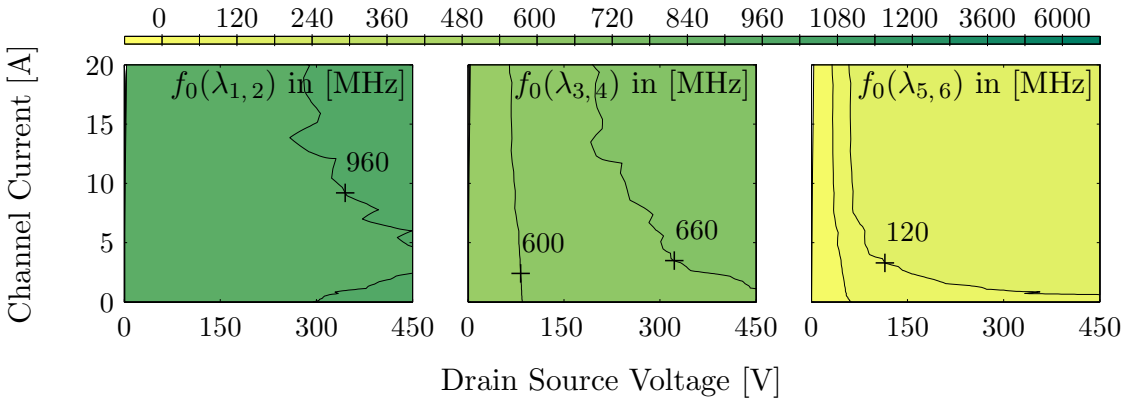


(b) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ of the initial parameterization

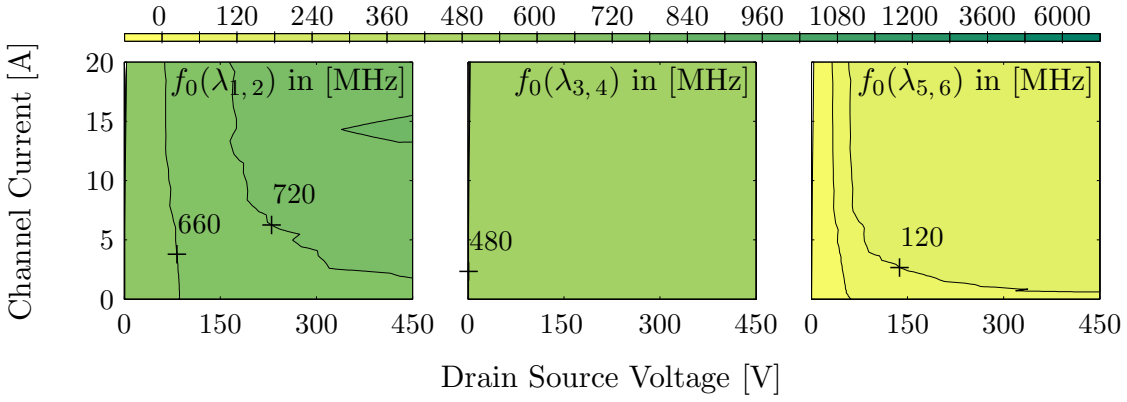


(c) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $2 \cdot C_{\mathrm{dg\,ext}} = 10\,\mathrm{pF}$

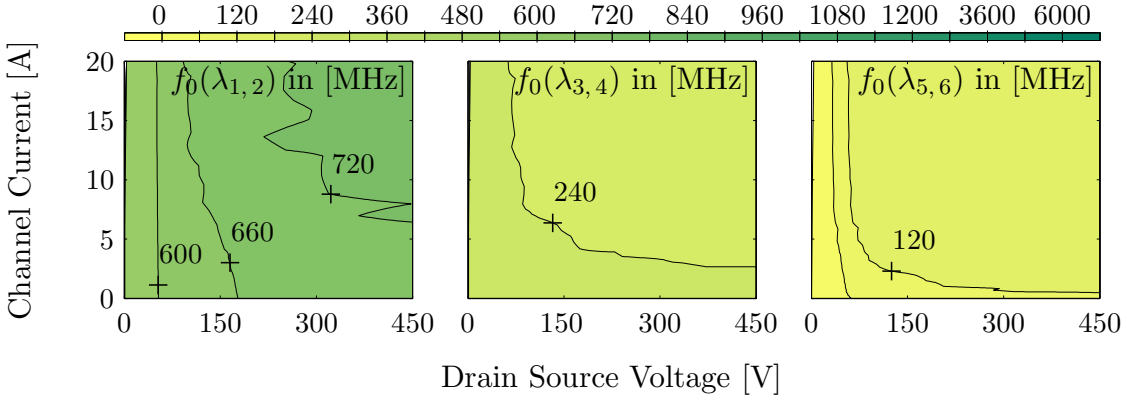
Figure C.8: Impact of the chip-external drain gate capacitance $C_{\mathrm{dg\,ext}}$ on the eigenfrequencies of the conjugate-complex eigenvalues of a buck converter topology's operating points in the MOSFET's operating range



(a) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $0.2 \cdot C_{\mathrm{gs\,ext}} = 3\,\mathrm{pF}$

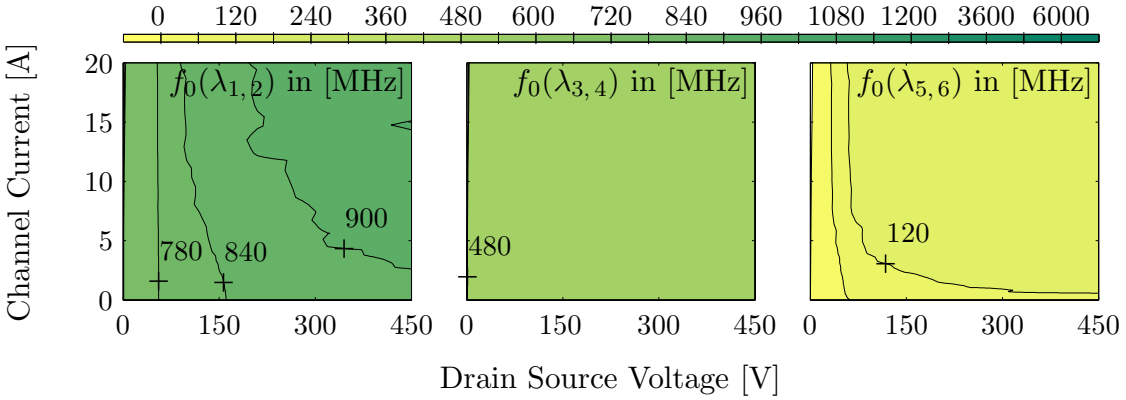


(b) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ of the initial parameterization

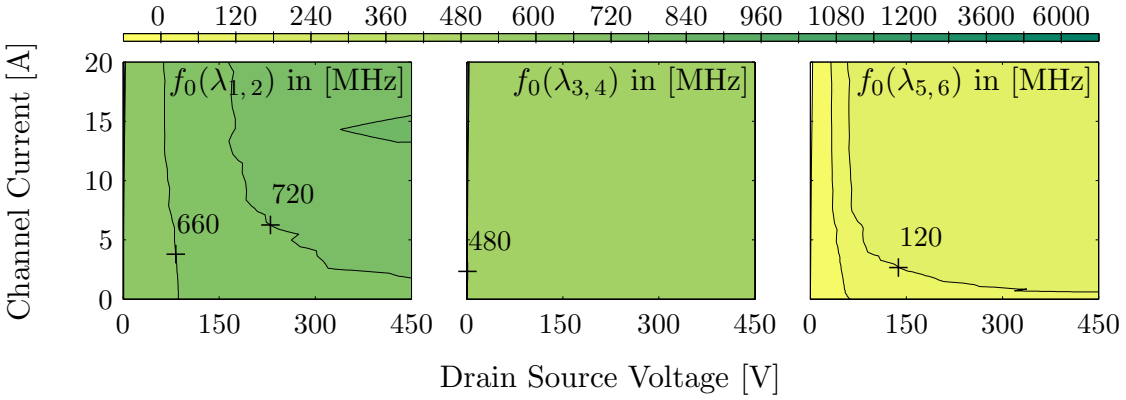


(c) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $5 \cdot C_{\mathrm{gs\,ext}} = 75\,\mathrm{pF}$

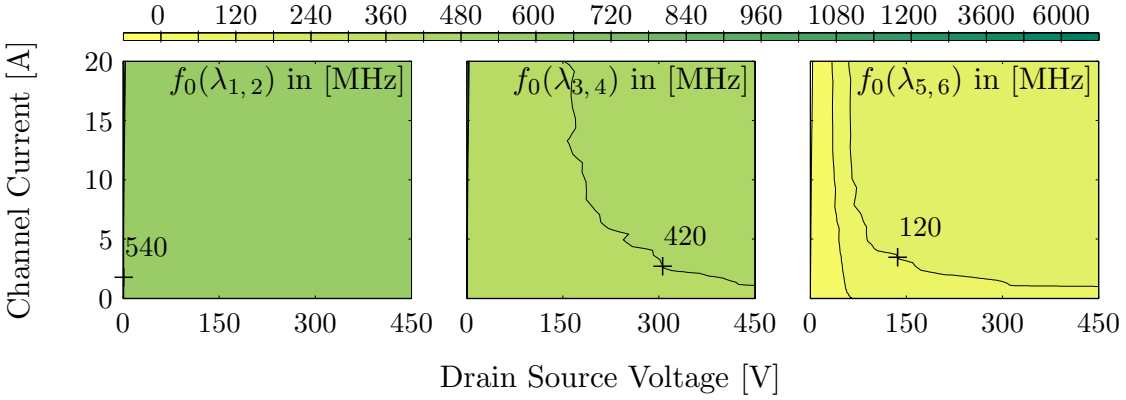
Figure C.9: Impact of the chip-external gate source capacitance $C_{\mathrm{gs\,ext}}$ on the eigenfrequencies of the conjugate-complex eigenvalues of a buck converter topology's operating points in the MOSFET's operating range



(a) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $0.2 \cdot L_{\mathrm{d\,pac}} = 0.4\,\mathrm{nH}$

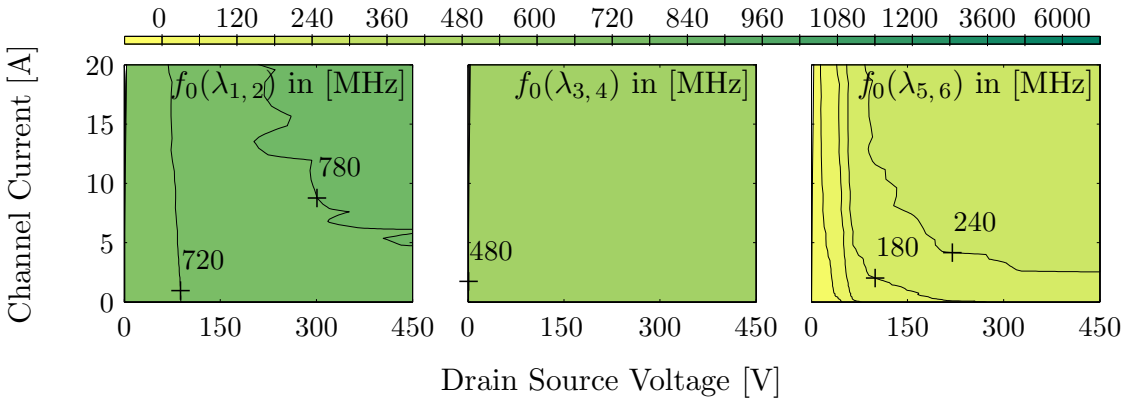


(b) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ of the initial parameterization

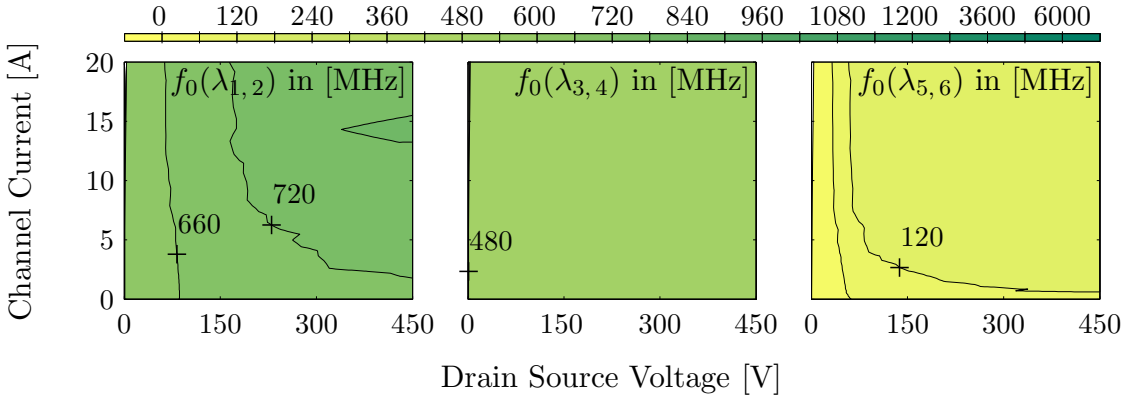


(c) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $5 \cdot L_{\mathrm{d\,pac}} = 10\,\mathrm{nH}$

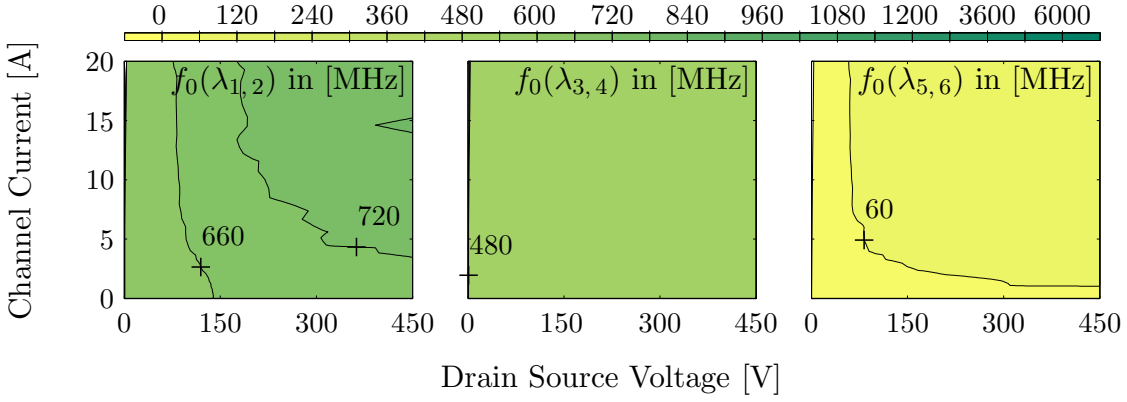
Figure C.10: Impact of the drain inductance $L_{\mathrm{d\,pac}}$ on the eigenfrequencies of the conjugate-complex eigenvalues of a buck converter topology's operating points in the MOSFET's operating range



(a) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $0.2 \cdot L_{\mathrm{d\,cir}} = 7\,\mathrm{nH}$

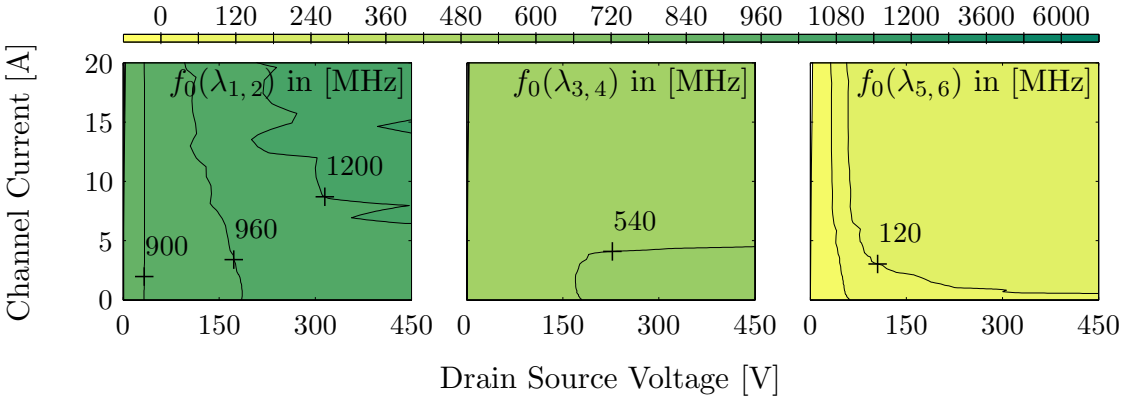


(b) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ of the initial parameterization

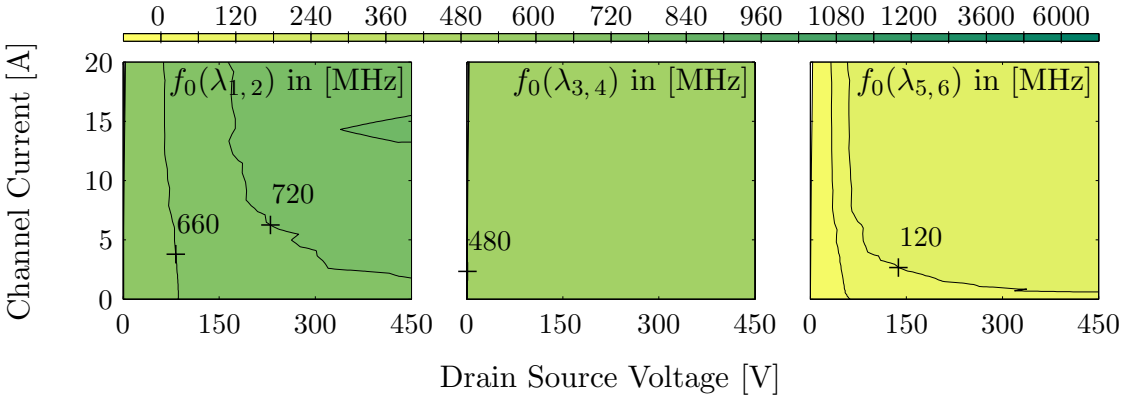


(c) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $5 \cdot L_{\mathrm{d\,cir}} = 175\,\mathrm{nH}$

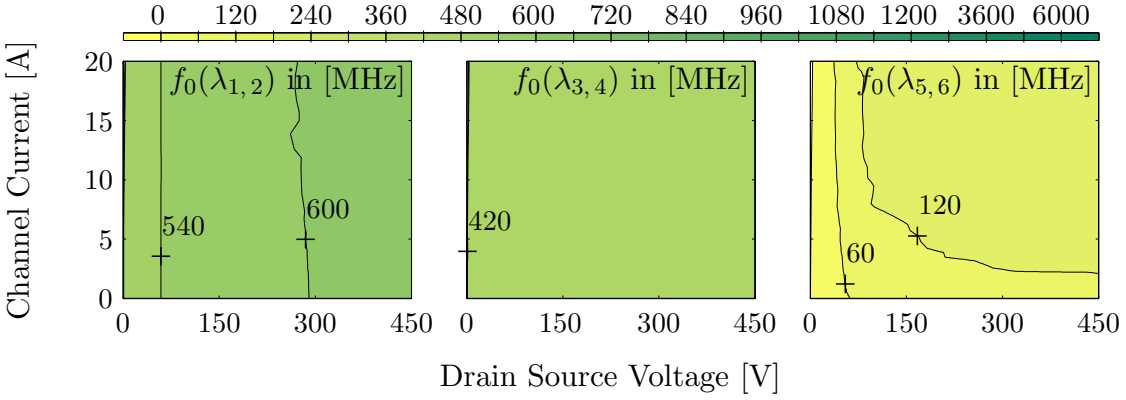
Figure C.11: Impact of the drain inductance $L_{\mathrm{d\,cir}}$ on the eigenfrequencies of the conjugate-complex eigenvalues of a buck converter topology's operating points in the MOSFET's operating range



(a) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $0.2 \cdot L_{\mathrm{g\,pac}} = 0.94\,\mathrm{nH}$

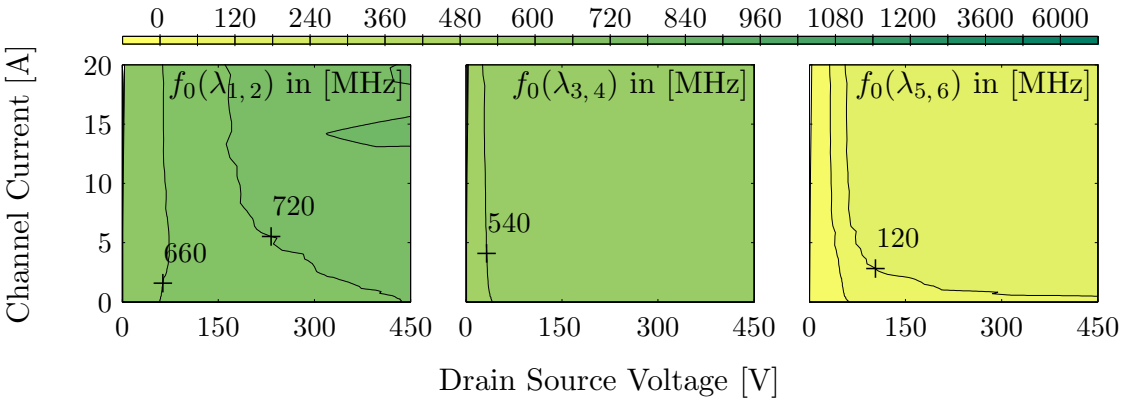


(b) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ of the initial parameterization

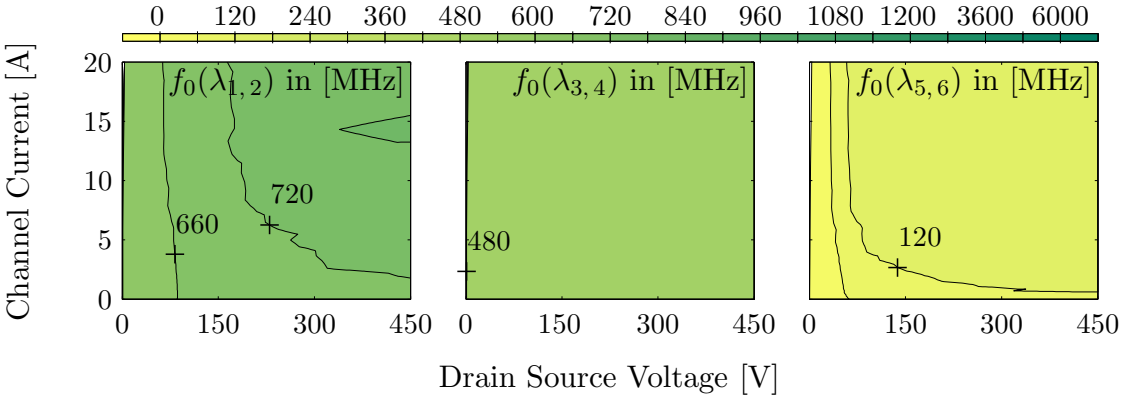


(c) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $5 \cdot L_{\mathrm{g\,pac}} = 23.5\,\mathrm{nH}$

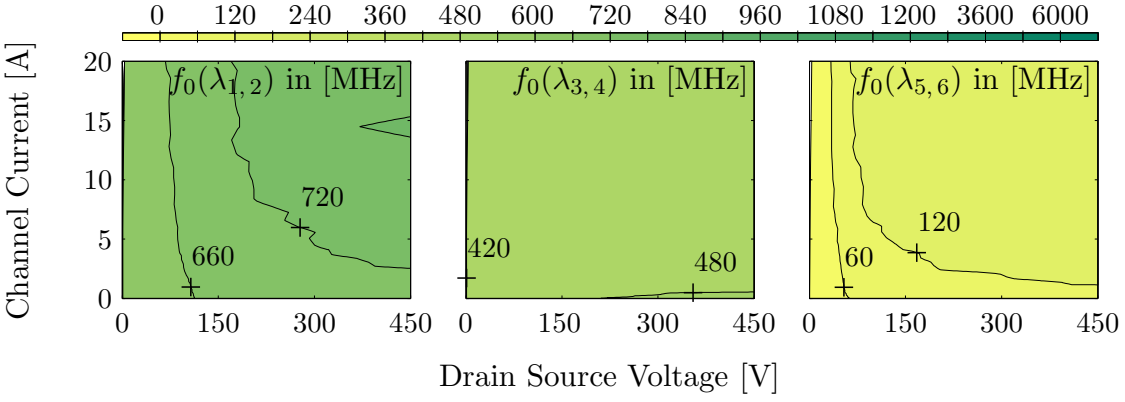
Figure C.12: Impact of the gate inductance $L_{\mathrm{g\,pac}}$ on the eigenfrequencies of the conjugate-complex eigenvalues of a buck converter topology's operating points in the MOSFET's operating range



(a) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $0.5 \cdot L_{\mathrm{g\,cir}} = 3\,\mathrm{nH}$

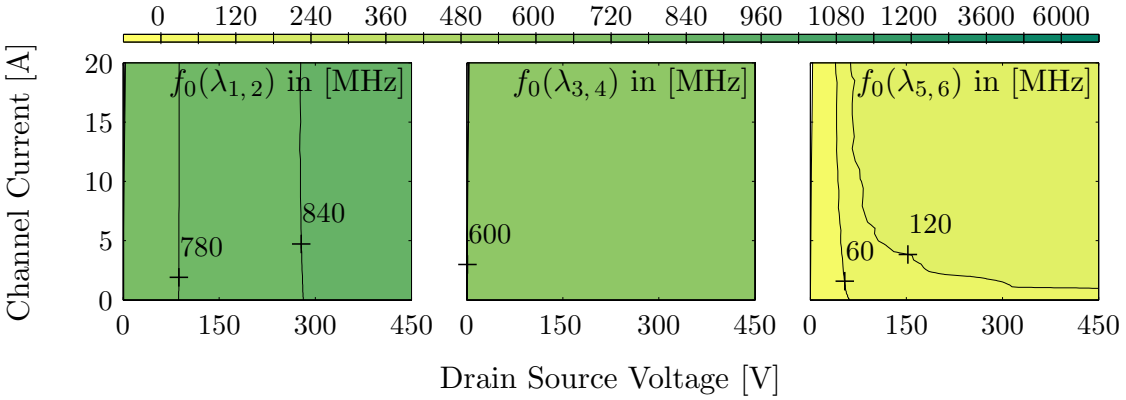


(b) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ of the initial parameterization

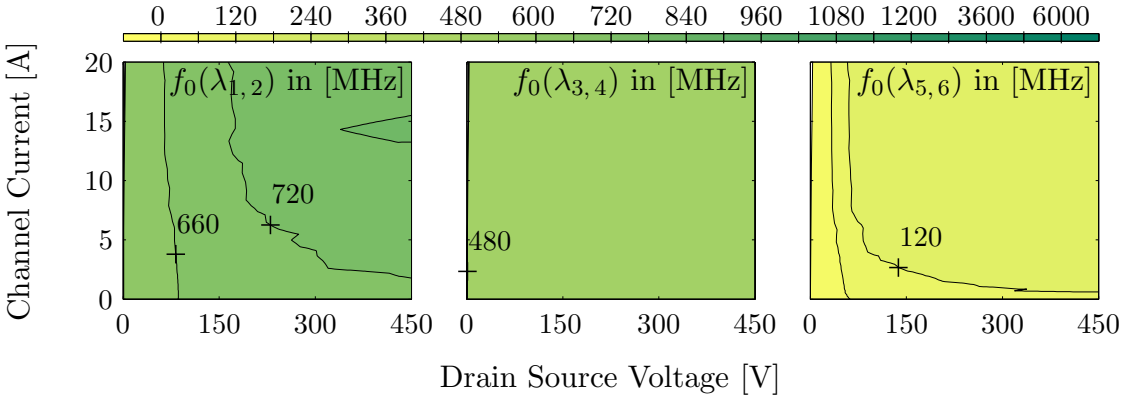


(c) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $2 \cdot L_{\mathrm{g\,cir}} = 12\,\mathrm{nH}$

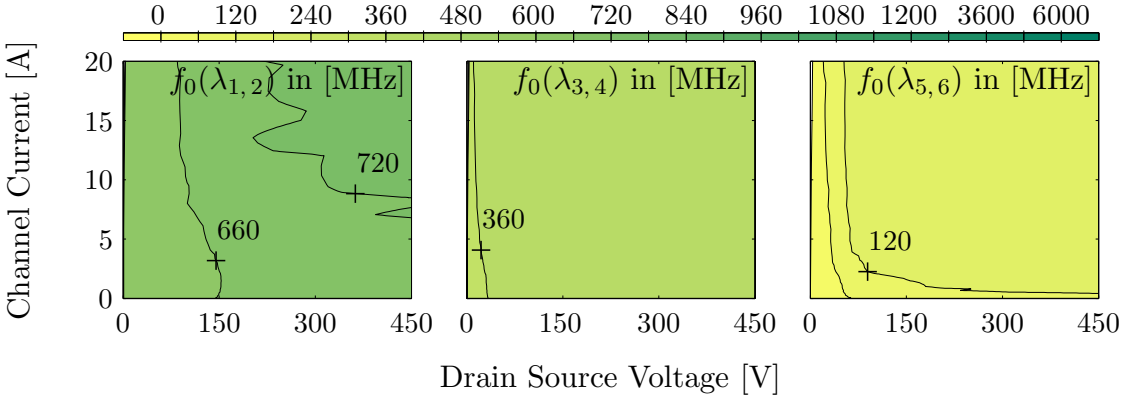
Figure C.13: Impact of the gate inductance $L_{\mathrm{g\,cir}}$ on the eigenfrequencies of the conjugate-complex eigenvalues of a buck converter topology's operating points in the MOSFET's operating range



(a) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $0.2 \cdot L_{\mathrm{s\,pac}} = 0.82\,\mathrm{nH}$

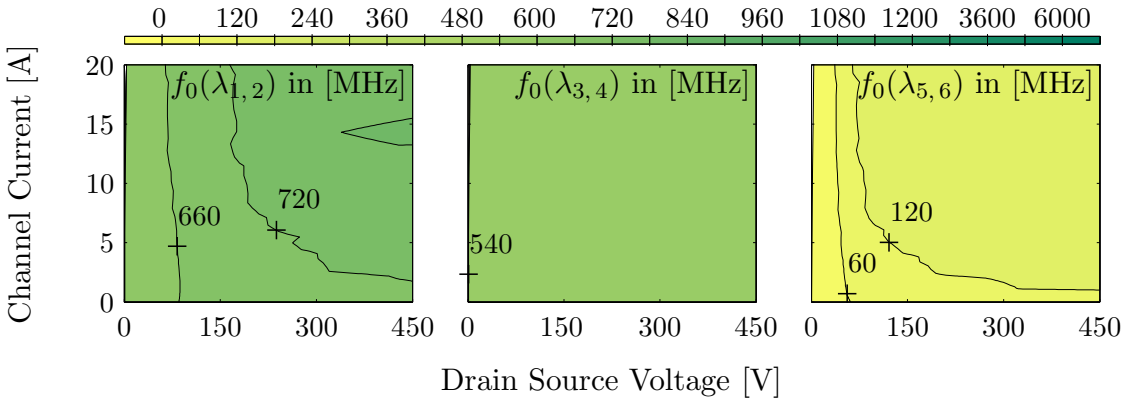


(b) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ of the initial parameterization

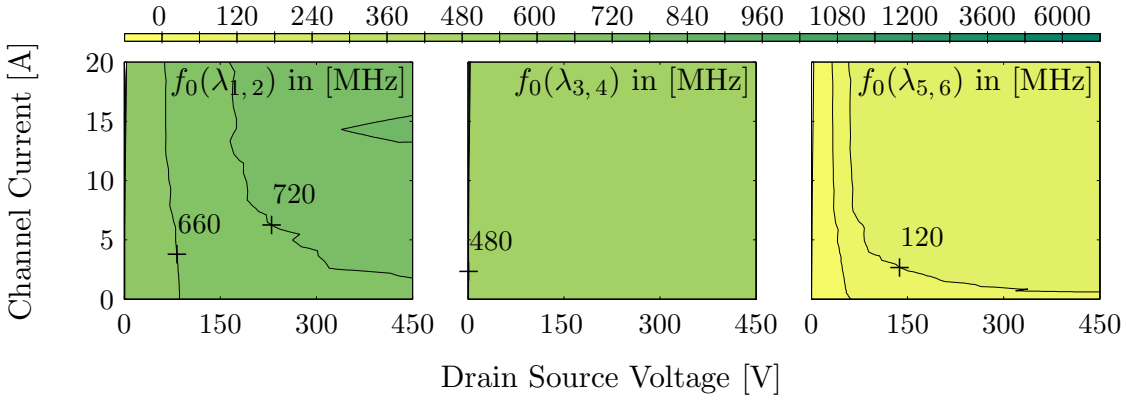


(c) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $5 \cdot L_{\mathrm{s\,pac}} = 20.5\,\mathrm{nH}$

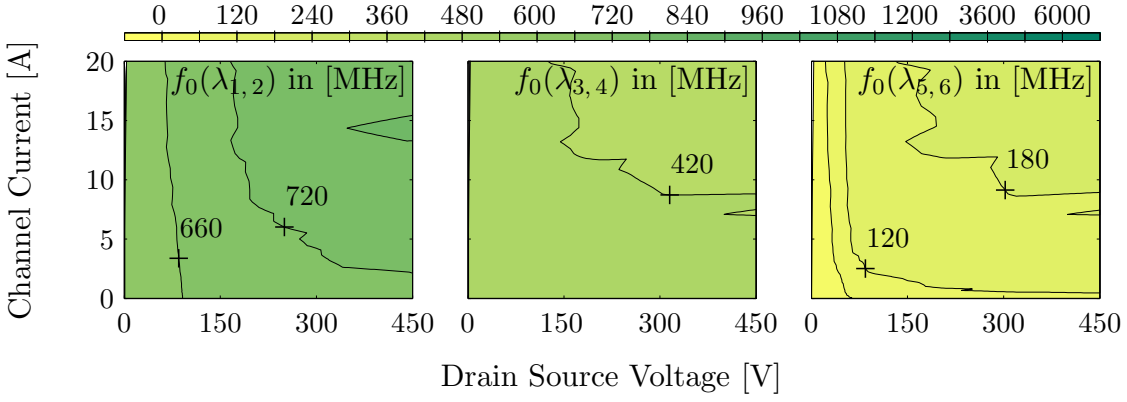
Figure C.14: Impact of the source inductance $L_{\mathrm{s\,pac}}$ on the eigenfrequencies of the conjugate-complex eigenvalues of a buck converter topology's operating points in the MOSFET's operating range



(a) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $0.2 \cdot L_{\mathrm{s\,cir}} = 0.6\,\mathrm{nH}$

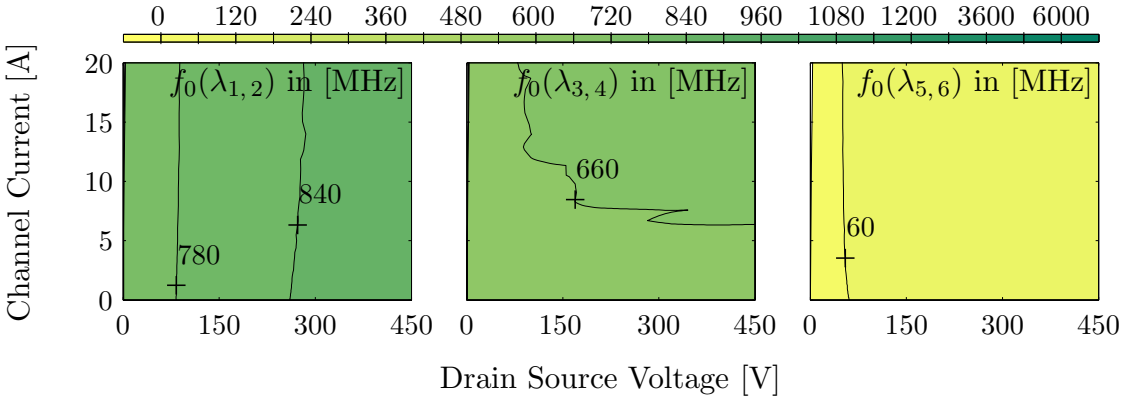


(b) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ of the initial parameterization

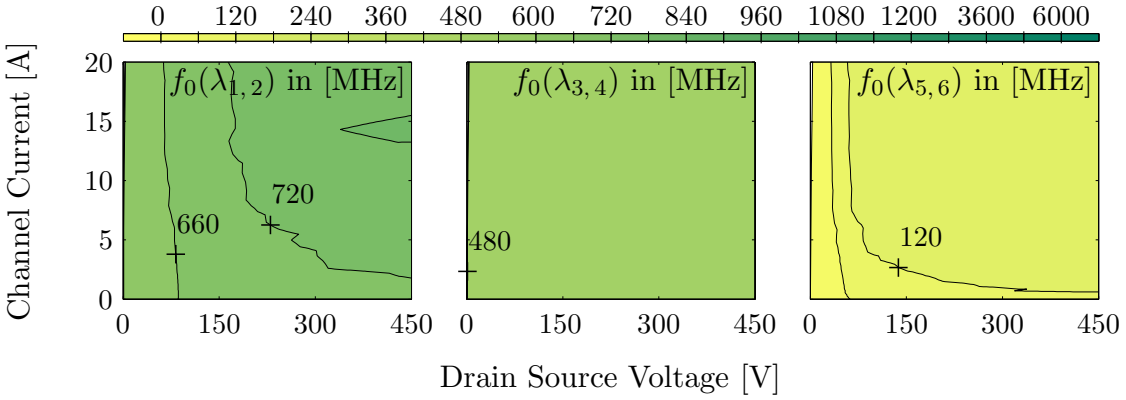


(c) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $5 \cdot L_{\mathrm{s\,cir}} = 15\,\mathrm{nH}$

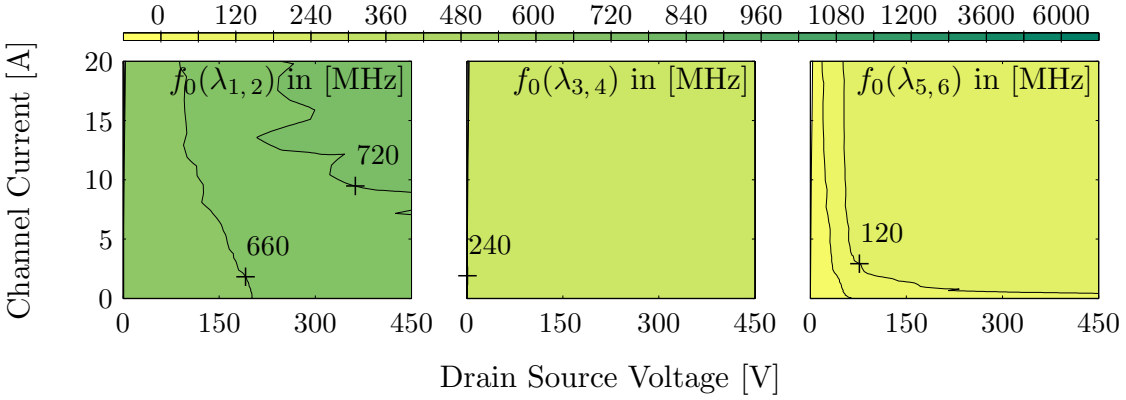
Figure C.15: Impact of the source inductance $L_{\mathrm{s\,cir}}$ on the eigenfrequencies of the conjugate-complex eigenvalues of a buck converter topology's operating points in the MOSFET's operating range



(a) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $0.2 \cdot L_{\mathrm{s\,pac}} = 0.82\,\mathrm{nH}$ and $0.2 \cdot L_{\mathrm{s\,cir}} = 0.6\,\mathrm{nH}$

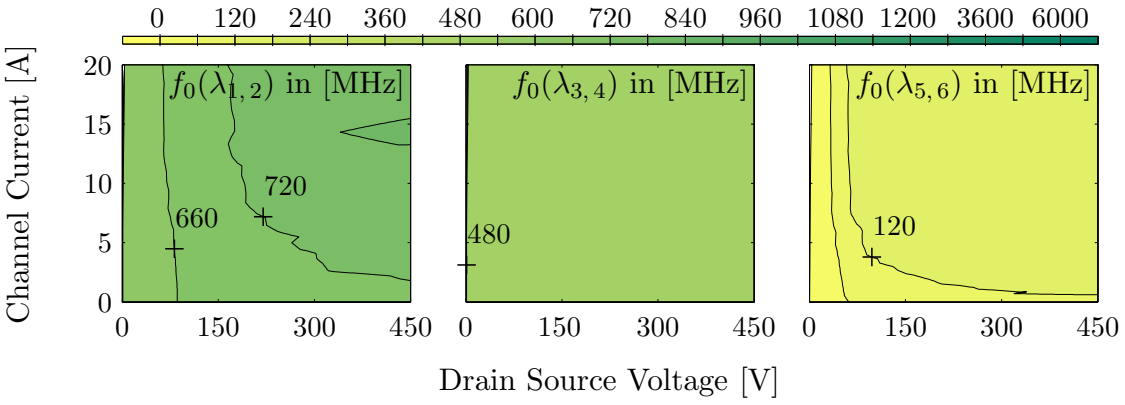


(b) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ of the initial parameterization

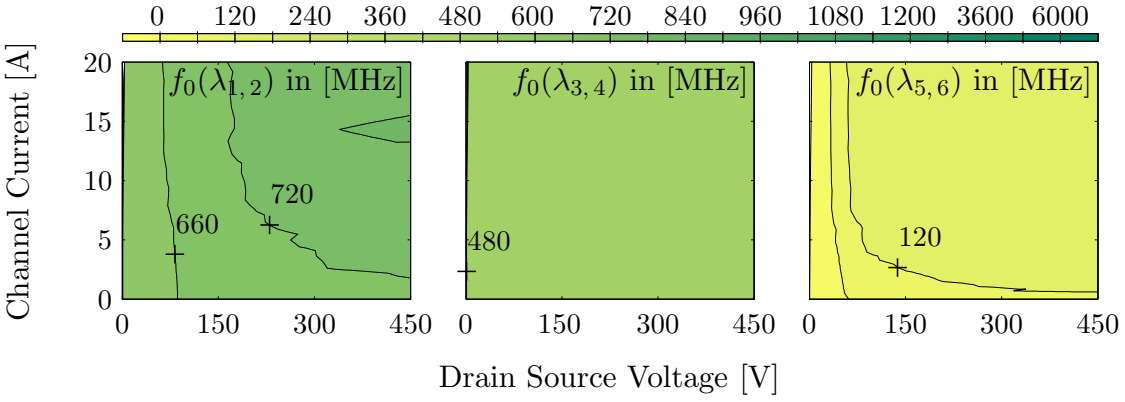


(c) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $5 \cdot L_{\mathrm{s\,pac}} = 20.5\,\mathrm{nH}$ and $5 \cdot L_{\mathrm{s\,cir}} = 15\,\mathrm{nH}$

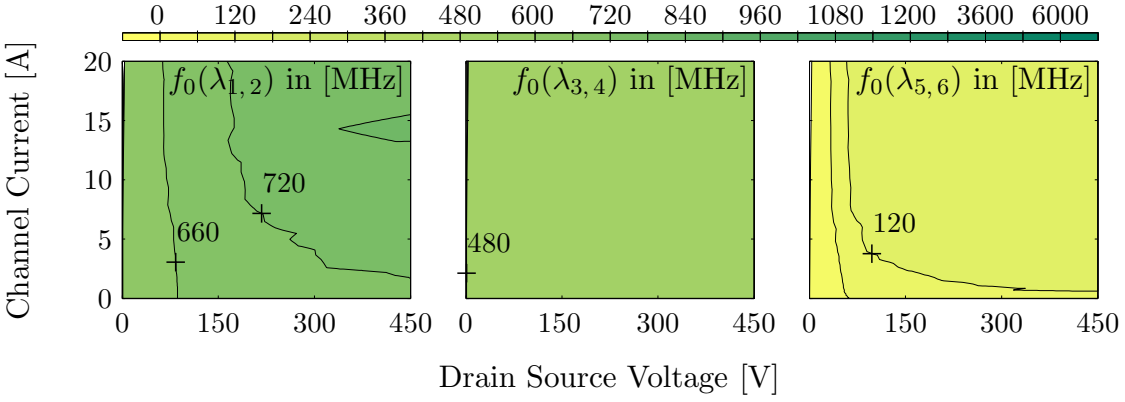
Figure C.16: Impact of the source inductances $L_{\mathrm{s\,pac}}$ and $L_{\mathrm{s\,cir}}$ on the eigenfrequencies of the conjugate-complex eigenvalues of a buck converter topology's operating points in the MOSFET's operating range



(a) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $-500 \cdot R_{\mathrm{d\,pac}} = -0.235\,\Omega$

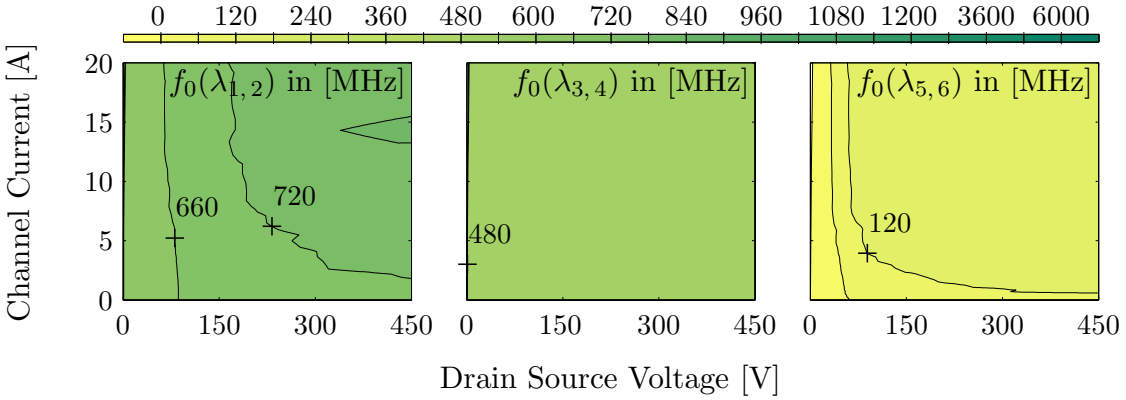


(b) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ of the initial parameterization

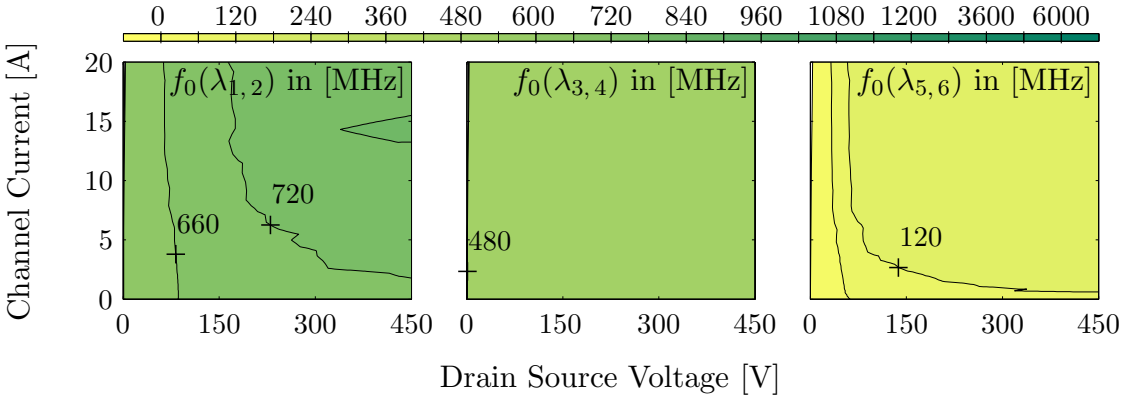


(c) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $500 \cdot R_{\mathrm{d\,pac}} = 0.235\,\Omega$

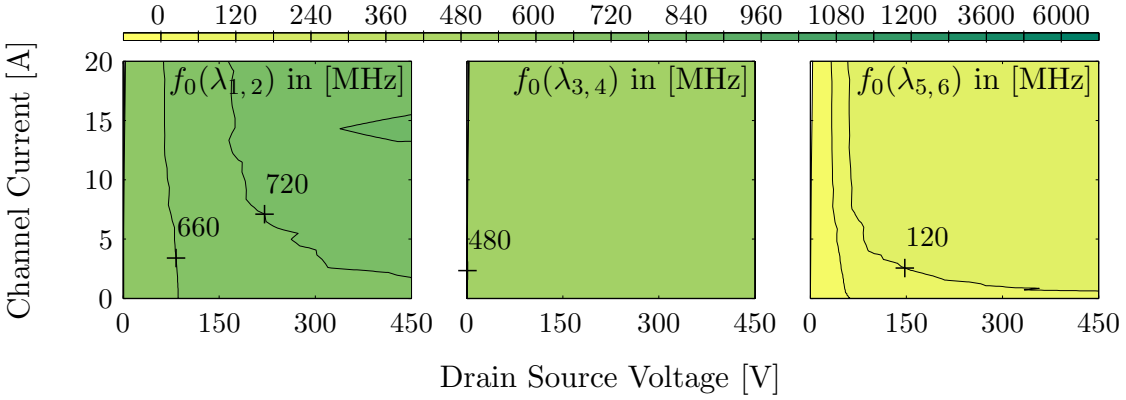
Figure C.17: Impact of the drain resistance $R_{\mathrm{d\,pac}}$ on the eigenfrequencies of the conjugate-complex eigenvalues of a buck converter topology's operating points in the MOSFET's operating range



(a) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $-500 \cdot R_{\mathrm{d\,cir}} = -0.94\,\Omega$

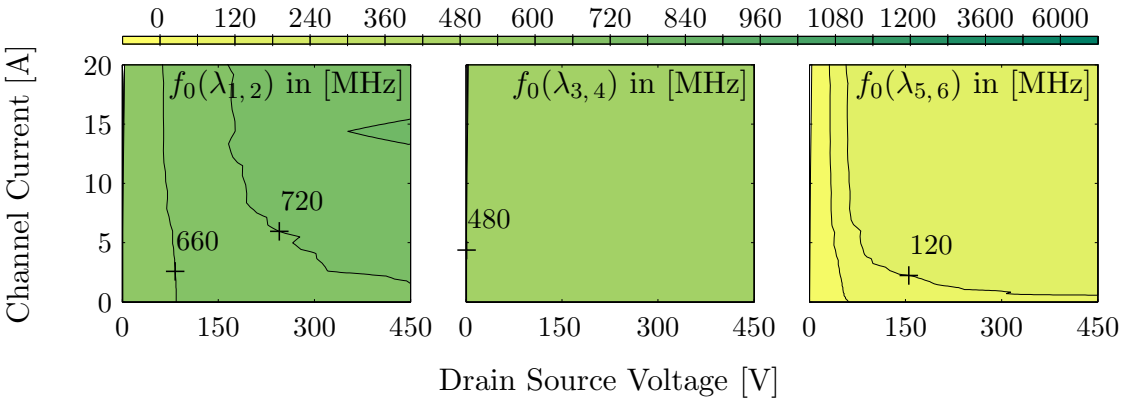


(b) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ of the initial parameterization

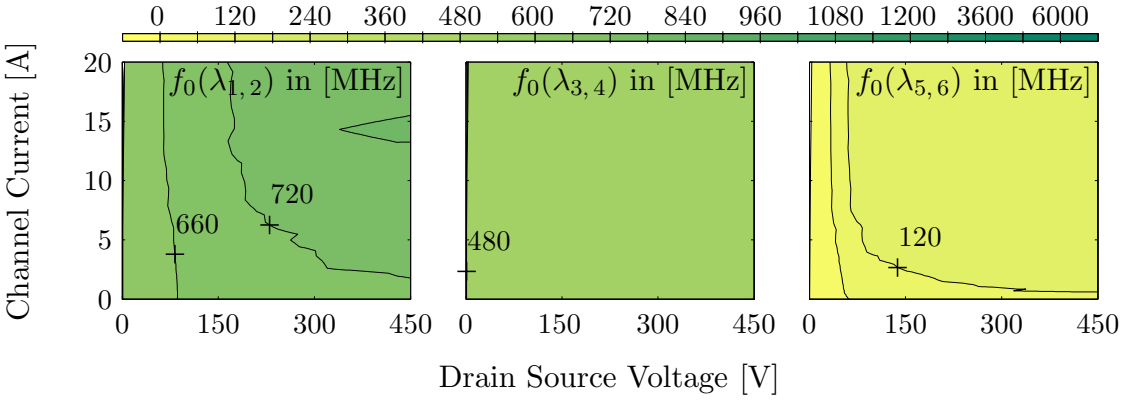


(c) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $500 \cdot R_{\mathrm{d\,cir}} = 0.94\,\Omega$

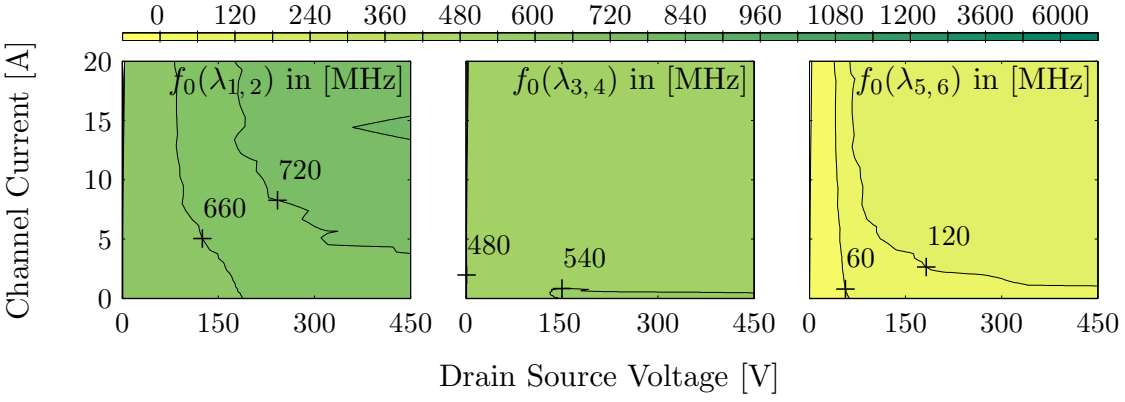
Figure C.18: Impact of the drain resistance $R_{\mathrm{d\,cir}}$ on the eigenfrequencies of the conjugate-complex eigenvalues of a buck converter topology's operating points in the MOSFET's operating range



(a) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $0.2 \cdot R_{\mathrm{g\,pac}} = 0.432\,\Omega$

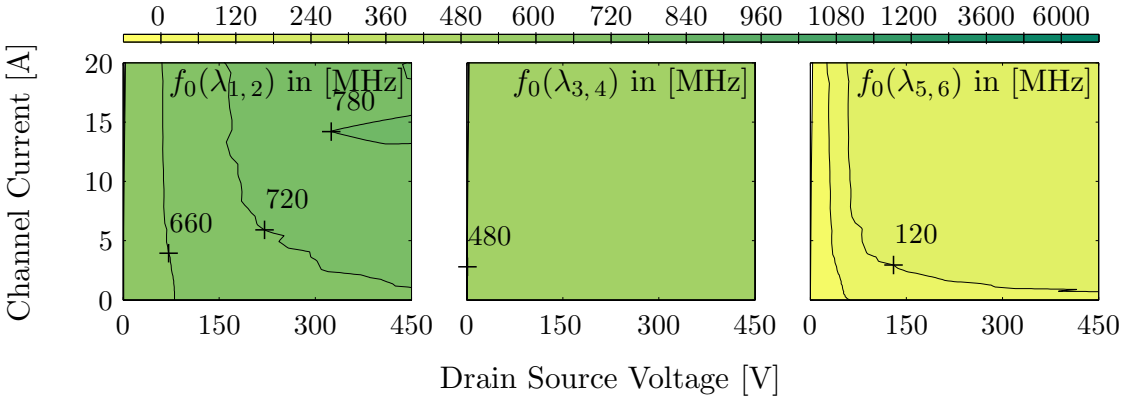


(b) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ of the initial parameterization

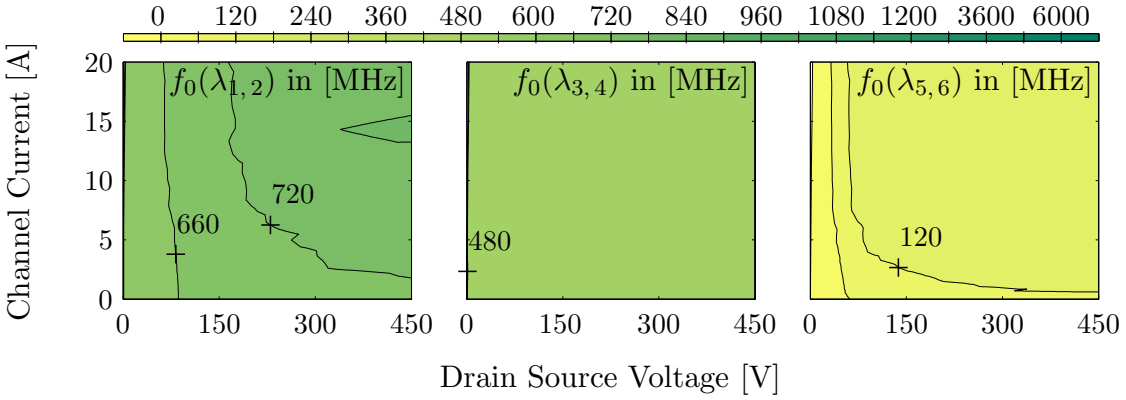


(c) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $5 \cdot R_{\mathrm{g\,pac}} = 10.8\,\Omega$

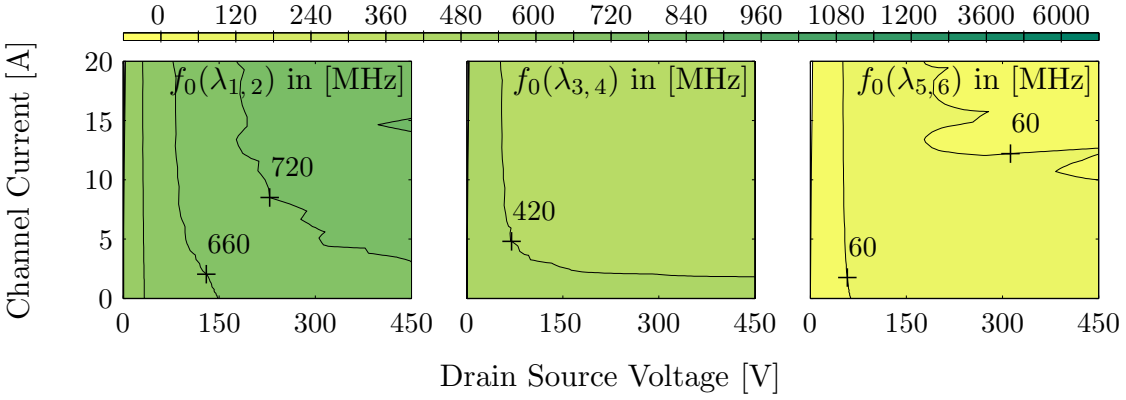
Figure C.19: Impact of the gate resistance $R_{\mathrm{g\,pac}}$ on the eigenfrequencies of the conjugate-complex eigenvalues of a buck converter topology's operating points in the MOSFET's operating range



(a) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $0.2 \cdot R_{\mathrm{g\,cir}} = 2.02\,\Omega$



(b) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ of the initial parameterization



(c) Contour plots of the eigenfrequencies of the conjugate-complex eigenvalues $\lambda_{1,2}$, $\lambda_{3,4}$ and $\lambda_{5,6}$ with $5 \cdot R_{\mathrm{g\,cir}} = 50.5\,\Omega$

Figure C.20: Impact of the gate resistance $R_{\mathrm{g\,cir}}$ on the eigenfrequencies of the conjugate-complex eigenvalues of a buck converter topology's operating points in the MOSFET's operating range

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List of Abbreviations

2D	two-dimensional
3D	three-dimensional
A	ampere
AC	altering current
BEM	boundary element method
BJT	bipolar junction transistor
BJTs	bipolar junction transistors
CG	capacitance-conductance
cp.	compare
CPU	central processing unit
DC	direct current
DIN	German Institute for Standardization
DUT	device under test
DUTs	devices under test
e.g.	exempli gratia, for example
Ed.	editor
et seq.	et sequens, and the following one or ones
etc.	et cetera, and so forth
F	farad
FEM	finite element method
FFT	fast Fourier transformation
Fig.	figure
FMM	fast multipole method
G	giga
GaAs	gallium arsenide
H	henry
Hz	hertz
i.e.	id est, that is
IC	Integrated Circuit
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronic Engineers

IGBT	insulated gate bipolar transistor
IGBTs	insulated gate bipolar transistors
J	joule
JFET	junction field-effect transistor
JFETs	junction field-effect transistors
K	kelvin
k	kilo
M	mega
m	meter and milli respectively
MOS	metal-oxide-semiconductor
MOSFET	metal-oxide-semiconductor field-effect transistor
MOSFETs	metal-oxide-semiconductor field-effect transistors
n	nano
no.	number
OP	operating point
p	pico
PCB	printed circuit board
PCBs	printed circuit boards
PFC	power factor correction
PWM	pulse width modulation
RESURF	reduced surface field
RL	resistance-inductance
RLCG	resistance-inductance-capacitance-conductance
s	second
Si	silicon
SiC	silicon carbide
SJ	super junction
SMPS	switching mode power supply
SMPSs	switching mode power supplies
SSV	state space variable
SSVs	state space variables
TPA	turbo package analyzer
V	volt
via	vertical interconnect access
vias	vertical interconnect accesses
vol.	volume
vs.	versus, against
W	watt

List of Symbols

α	real part of an eigenvalue
β	imaginary part of an eigenvalue
Δ	change of any variable
δ	skin depth
ε_0	vacuum electric permittivity $\varepsilon_0 \approx 8.854188 \cdot 10^{-12}\ {}^{As}/_{\mathrm{Vm}}$
ε	electric permittivity
ϑ	temperature
λ	eigenvalue and wavelength respectively
μ_0	vacuum magnetic permeability $\mu_0 = 4\pi \cdot 10^{-7}\ {}^{Vs}/_{\mathrm{Am}}$
μ	drift mobility, magnetic permeability and micro respectively
ϕ	work-function or barrier height and electrical potential respectively
ρ	charge density
ϱ	density
σ	specific conductance or electric conductivity
Ω	OHM
ω	angular frequency
A	area
B	FULOP constant
$\boldsymbol{A}$	system matrix
A^*	effective RICHARDSON constant
a	matrix element
C	capacitance
CC	equivalent square capacitance
CL	product of equivalent inductance and capacitance
°C	degree CELSIUS
c_0	vacuum speed of light $c_0 = 2.99792458 \cdot 10^8\ {}^{m}/_{\mathrm{s}}$
c	coefficient
c	specific heat capacity
D	damping ratio
D	duty cycle

d	stability degree
d	derivative
∂	partial-derivative
E	electric field or energy
e	error
e	base of natural logarithms
f	frequency
$\mathbf{f}(x)$	function of x
G	conductance
g	amplifier gain
$\boldsymbol{I}$	identity matrix
$\Im(x)$	imaginary part of x
I	DC current
i	current
i	imaginary unit
K	coefficient
k	counting number ($k \in \mathbb{N}$)
k	BOLTZMANN constant ($\mathrm{k} = 1.3806504 \cdot 10^{-23}\,{}^{J}/_{\mathrm{K}} = 8.617343 \cdot 10^{-5}\,{}^{eV}/_{\mathrm{K}}$)
L	inductance
LL	equivalent square inductance
l	length
$\boldsymbol{M}$	MAXWELL matrix
m	mass (in chapter **2**); multiplicity of an eigenvalue (in chapter **5**)
m	slope of a curve
N	doping concentration
$\mathbb{N}$	natural numbers
n	number, dimension or order with $n \in \mathbb{N}$
n	n-type semiconductor with $N_D = 10^{15} \ldots 10^{18}\,\mathrm{cm}^{-3}$ or (electron) density
n^+	n-type semiconductor with $N_D = 10^{19} \ldots 10^{21}\,\mathrm{cm}^{-3}$
n^-	n-type semiconductor with $N_D = 10^{12} \ldots 10^{14}\,\mathrm{cm}^{-3}$
P	electric power
p	p-type semiconductor with $N_A = 10^{15} \ldots 10^{18}\,\mathrm{cm}^{-3}$
p^+	p-type semiconductor with $N_A = 10^{19} \ldots 10^{21}\,\mathrm{cm}^{-3}$
p^-	p-type semiconductor with $N_A = 10^{12} \ldots 10^{14}\,\mathrm{cm}^{-3}$
Q	electric charge
$\mathcal{Q}$	thermal energy
q	electron charge ($q = 1.602176487 \cdot 10^{-19}\,\mathrm{C}$)
R	resistance
$\mathbb{R}$	real numbers

$\Re(x)$	real part of x
r	radius
s	LAPLACE variable
T	absolute temperature
$\mathcal{T}$	period
t	thickness or time
V	DC voltage or volume
v	voltage or velocity
w	width
x	argument or geometric dimension
$\dot{\vec{x}}$	time differential state vector
$\vec{x}$	state vector
y	geometric dimension
Z	impedance
$\mathbb{Z}$	integers
z	geometric dimension or number with $z \in \mathbb{N}$

List of Indexes

x_A	acceptor
x_{A}	anode
x_{a}	anode
x_{acc}	accumulation
x_{act}	active
x_{approx}	approximated
x_{ap}	acoustic phonon
x_{aux}	auxiliary
x_{avg}	average
x_{bi}	built-in
x_{bn}	SCHOTTKY contact with n-type semiconductor
x_{br}	breakdown
x_C	capacitance
x_{C}	case or cathode
x_{c}	cathode
x_{chip}	chip or chip-internal
x_{calc}	calculation
x_{Ch}	channel
x_{cir}	circuit
x_D	donor
x_{D}	drain
x_{d}	drain
x_{Dr}	driver
x_{DC}	direct current
x_{DClink}	DC link
x_{Dio}	diode
x_{dyn}	dynamic, i.e. transient
x_{e}	electron
x_{eff}	effective
x_{em}	electron mobility
x_{epi}	epitaxial

x_{equ}	equivalent
x_{ext}	chip-external
x_{F}	FERMI
x_{f}	fall
x_{fix}	fixed or stationary
x_G	conductance
x_{G}	gate
x_{g}	gate
x_{i}	intrinsic
x_{ii}	ionized impurities
$x_{\mathrm{i\,j}}$	row index with $\mathrm{i} \in \mathbb{N}$
x_{int}	integrated
x_{in}	input
x_{iss}	small-signal input
x_{JFET}	junction field-effect transistor
x_{J}	junction
$x_{\mathrm{i\,j}}$	column index with $\mathrm{j} \in \mathbb{N}$
x_k	index with $k \in \mathbb{N}$
x_L	inductance
x_{L}	load circuit
x_{ll}	lower limit
x_{M}	minus
x^{M}	MAXWELL
x_{MOM}	metal-oxide-metal layer sequence
x_{MOS}	metal-oxide-semiconductor layer sequence
x_{MS}	metal-semiconductor junction
x_{m}	MOSFET
x_{max}	maximum
x_{meas}	measured
x_{min}	minimum
x_n	node, harmonic or number ($n \in \mathbb{N}$)
x_{n}	n-type semiconductor, $N_D = 10^{15} \ldots 10^{18}\,\mathrm{cm}^{-3}$
$x_{\mathrm{n^+}}$	n-type semiconductor, $N_D = 10^{19} \ldots 10^{21}\,\mathrm{cm}^{-3}$
$x_{\mathrm{n^-}}$	n-type semiconductor, $N_D = 10^{12} \ldots 10^{14}\,\mathrm{cm}^{-3}$
x_{on}	turned-on
x_{op}	optical phonon
x_{oss}	small-signal output
x_{ox}	oxide
x_{P}	plus

x_{PT}	punch-through
x_P	pad
x_{pac}	package
$x_{\mathrm{pn^-}}$	$\mathrm{pn^-}$-junction
x_{pu}	pulse
x_{p}	p-type semiconductor, $N_A = 10^{15} \ldots 10^{18}\,\mathrm{cm}^{-3}$
$x_{\mathrm{p^+}}$	p-type semiconductor, $N_A = 10^{19} \ldots 10^{21}\,\mathrm{cm}^{-3}$
$x_{\mathrm{p^-}}$	p-type semiconductor, $N_A = 10^{12} \ldots 10^{14}\,\mathrm{cm}^{-3}$
x_{QS}	quasi-saturation
x_R	resistance
x_r	relative (material dependent)
x_{rss}	small-signal feedback
x_{r}	rise
x_{S}	source
x_{s}	source
x_{Si}	silicon
x_s	sampling
x_{sat}	saturation
x_{scr}	space charge region
x_{sim}	simulation
x_{ss}	small-signal
x_{sub}	substrate
x_{th}	thermal
x_{th}	threshold
x_{thv}	threshold voltage
x_{tot}	total
x_{ul}	upper limit

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