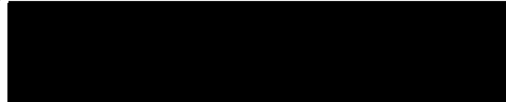
# Charge Trapping Instabilities in Amorphous Silicon/Silicon Nitride Thin Film Transistors.

A thesis presented by Anthony Robert Hepburn
(sponsoring establishment: Dundee College of Technology (Scotland)
collaborating establishment: Philips Research Laboratories (England).)
to the CNAA in partial fulfilment of the requirements
for the degree of Doctor of Philosophy, May 1988.

## DECLARATION.

I declare that while registered as a candidate for the degree for which this thesis is presented I have not been a candidate for any other award. I further declare that except where stated the work contained in this thesis is original and was performed by the author. The author is grateful to Dr. J.A Chapman, Dr. O.F Hill and Dr. I.D French for preparing the TFT specimens employed in this study.

Signed



Anthony Robert Hepburn.

## ADVANCED STUDIES.

In addition to the original research reported in this thesis, the author followed a programme of postgraduate study. This programme included attendence at the 11th and 12th International Conferences on Amorphous and Liquid Semiconductors, at both of which papers were presented. Additionally, the author attended the 1984, 1985 and 1986 Chelsea Meetings on Liquid and Amorphous Semiconductors, with a paper presented at the 1984 meeting.

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# CHARGE TRAPPING INSTABILITIES IN AMORPHOUS SILICON - SILICON NITRIDE THIN FILM TRANSISTORS

ANTHONY R. HEPBURN

Charge trapping phenomena within amorphous silicon-silicon nitride TFTs have been characterised in an extensive study. A new experimental technique has been developed and applied in conjunction with the standard measurement of threshold voltage.

The new technique reveals two electron trapping centres which exist within the α-Si:H layer, one about 0.45eV the other about 0.85eV from the conduction band edge. The amount of charge located within both states increases as the device is stressed. The annealing out of the charge trapping phenomenon is found to be thermally activated although, in some circumstances, reverse bias annealing is also found to be effective.

The results are interpreted in terms of a model in which the charge trapping instabilities are due to two separate phenomena. Charge trapping into the insulating layer is found to occur. However, a new mechanism identifed conclusively and for the first time by this study is that of single carrier creation of metastable silicon dangling bonds close to the interface. The neutralisation of charge in these states has been investigated and is found to occur through a simple thermal release process for trapped charge within the silicon layer and by a mechanism akin to xerographic depletion discharge, when charge becomes trapped in the insulating layer.

Additionally, a Meyer-Neldel relationship is found to exist between the release activation energy and attempt-to-escape pre-factor of the various localised states. Such an observation is new and no explanation is forthcoming. However, it is noted that similar experiments conducted by other groups reveal consistent data.

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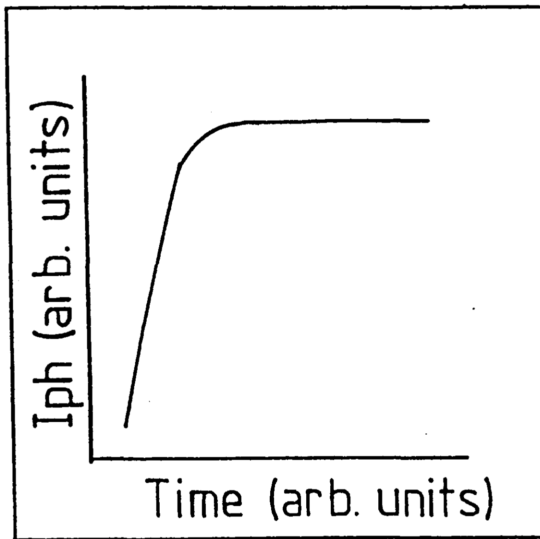
# CHAPTER 1
# INTRODUCTION.

Hydrogenated amorphous silicon (α-Si:H) is a material which presently commands a great deal of worldwide attention[1]. This interest stems from the early work of Chittick[2] and the more revealing studies by the Dundee University group[3] on α-Si:H produced by the glow discharge technique. The process produces very high quality material and also allows doping and the production of various alloys. This in turn has led to the development of a wide range of applications including solar cells, thin film transistors and memory devices[1].

Amorphous silicon thin film transistors (TFTs) are currently of great commercial interest due to applications in such areas as liquid crystal displays[4]. The best devices presently available[5] are fabricated with an hydrogenated amorphous silicon active layer and an amorphous silicon nitride gate dielectric, both deposited by the glow discharge technique. The trapping of charge in the region of the semiconductor dielectric interface is of considerable importance in determining the device stability. A TFT subjected to a high positive gate voltage for a long period exhibits a large positive shift in the threshold voltage[6]. Until the inception of this project this has been interpreted solely in terms of charge injection into the insulating layer[7].

This study originates from an M.Sc project[8] conducted by the author on the transient photoconductive response of α-Si:H TFTs. Measurements of the transient rise of the photocurrent did not reveal the normal linear relationship with time. Additional features were observed (figure 1-1) which were associated with the neutralisation of excess trapped charge. A new experimental technique was developed to investigate this phenomenon (section 4.4.1). This showed clearly that a large amount of charge remains trapped within the device for a



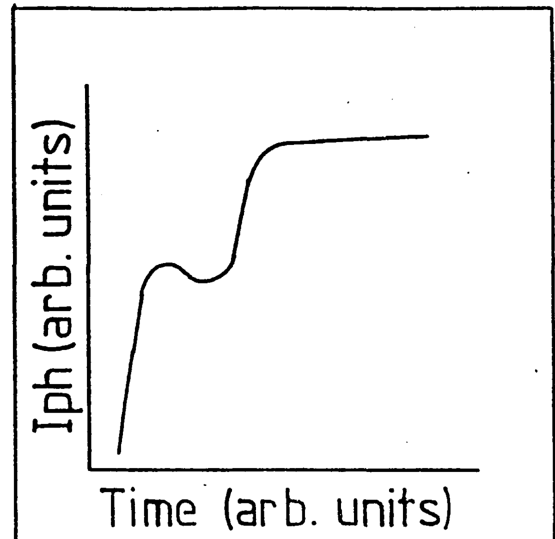




**Figure 1-1 :** Typical shape of transient rise of the photocurrent ($I_{ph}$) observed in the M.Sc study.

considerable period of time after the gate voltage has been removed. Using this technique a wide variety of information can be obtained about the spatial and energetic location of this trapped charge and the processes by which it may be neutralised.

# CHAPTER 2

# ELECTRONIC PROPERTIES OF HYDROGENATED AMORPHOUS SILICON

## 2.1 Introduction.

In this chapter, the density of states (DOS) distribution (of a generalised amorphous semiconductor) is discussed from a theoretical viewpoint and then the experimental measurements of the DOS in α-Si:H are described. Subsequently both theoretical and experimental aspects of transport in amorphous semiconductors, and in particular α-Si:H, are considered. Finally a discussion of the stability of α-Si:H is given.

## 2.2 The Distribution of Electronic States in Amorphous Semiconductors.

The electronic properties of a material are controlled by the electronic states. Therefore it is important that the character and distribution of these states be determined. In the following section, the types of electronic state expected to be found in a generalised amorphous semiconductor are described. The treatment follows that given by Mott & Davis[9].

### 2.2.1 Generalised DOS in an Amorphous Semiconductor.

Essentially there are 3 different kinds of state :-

1. Valence/Conduction band extended states
2. Valence/Conduction band localised states
3. Defect states (including impurity related centres).

#### 2.2.1.1 The Extended States

Originally, it was thought[10] that a band gap could not exist in an amorphous semiconductor, due to the lack of long range order. However, various physical properties patently show the existence of an energy gap e.g. the optical gap of glass. A model was developed which could explain the existence of bands in an amorphous semiconductor based on the tight-binding theory of crystalline semiconductors. This explains the formation of narrow bands, but the reason for the wide bands observed in amorphous semiconductors is still a matter of some speculation.

#### 2.2.1.2 The Localised Band Tail States.

There exist regions at the extremities of the bands which consist of localised electronic centres, called the band tails. Such states were first proposed to exist in the 1940's[11]. However, it was not until the late 1960's that a rigorous formulation was derived[12] for their existence. This work by Mott[12], is an extension of Anderson's theory[13] of impurity band conduction. Anderson considers the influence of a random disorder potential upon the nature of the electronic states within a narrow tight binding impurity band. The reason for localisation of the electronic states follows directly from the manner in which bands are proposed to be formed. If large potential fluctuations occur then the overlap of neighbouring electron wavefunctions is reduced. If this overlap becomes sufficiently small (i.e. $V_o$ becomes large) then the state becomes localised. The effect can be seen schematically in figure 2-1. In general, localisation of the *whole* band occurs when the ratio of the disorder potential to the bandwidth (B) reaches a critical value given by

$$V_o / B \sim 2 \qquad (2.1)$$

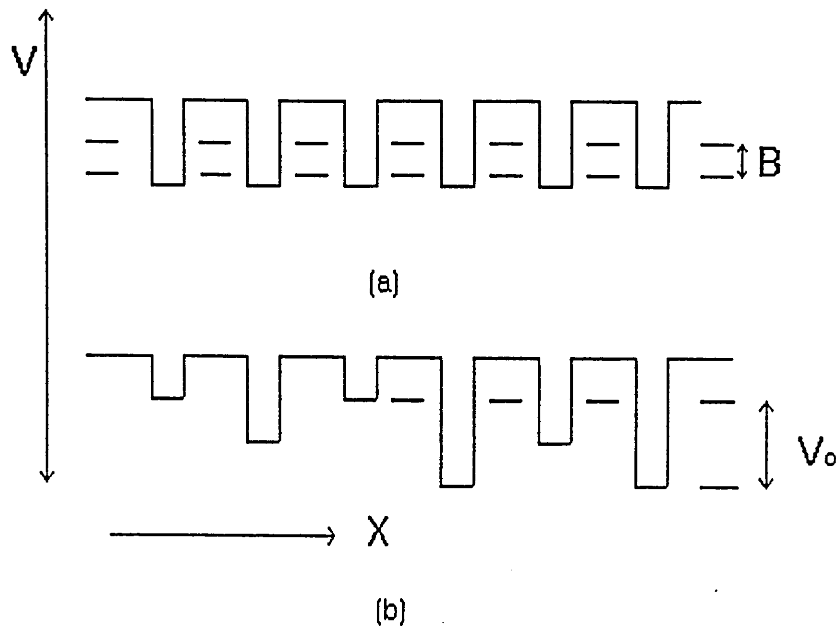



**Figure 2-1** : Tight binding model for (a) a crystalline semiconductor (b) an amorphous semiconductor

An amorphous semiconductor, by its very nature, is structurally disordered due to bond rotations, bond length variations, creation of internal surfaces and network termination (e.g. Si-H bonding in an α-Si:H lattice). Thus the local environment (beyond nearest neighbours) is not well defined. This leads to what are known as disorder potentials ($V_o$ ), which are fluctuations above or below the average lattice potential. Thus the Anderson model for impurity band conduction represents a situation similar to that which exists within an amorphous semiconductor. The extension of this work by Mott[12], considers the influence of a disorder potential on states close to the edge of a *wide* band. Since there is less overlap of the electron wavefunctions close to the band edge, a smaller disorder potential may localise these electronic states.

## 2.2.1.3 The Defect States.

Initially it was thought[12] that because of the randomness of the amorphous structure the lattice would relax to satisfy all the bonds, in accordance with the

"8-N" rule. However, defect states exist and are localised but not because of potential fluctuations; they result from broken bonds, vacancies, impurities etc.

## 2.3 Measurements of the Density of Gap States in α-Si:H.

One of the main reasons for the difference in properties of amorphous and crystalline semiconductors is the large density of localised centres in the amorphous state. Therefore, much attention has been focused on determining the density and energy distribution of these states. The DOS in α-Si:H is still a matter of some discussion, because of the wide variety of preparation and measurement techniques. A generally accepted view of the main features of the DOS in α-Si:H has, perhaps, now appeared[14] (see section 2.4).

### 2.3.1 The Field Effect.

The field effect (FE) DOS has been the subject of much controversy, perhaps mainly because it has been claimed[15] to represent a bulk DOS. However, since the actual currents to which FE analyses are applied, flow within ~ 50A of the interface, then the FE DOS is certain to be influenced by surface states[16] (if any exist). The measurements discussed herein were conducted ten years ago, on what was then regarded as high quality α-Si:H, and therefore may not be representative of today's state of the art material.

The FE DOS for undoped α-Si:H[15] is shown in figure 2-2. A broad minimum exists in the middle of the gap (typically $N(E) \sim 10^{16}\text{-}10^{17} cm^{-3}eV^{-1}$) and a small peak is found about 0.4eV from the conduction band edge, $E_c$. By studying doped α-Si:H the range of measurements is extended towards the tails of both the valence and conduction band. These studies reveal another feature about 1.2eV from $E_c$. However, the mid-gap DOS changes[17,18] when the material is doped and dopant states are introduced close to both the conduction band and

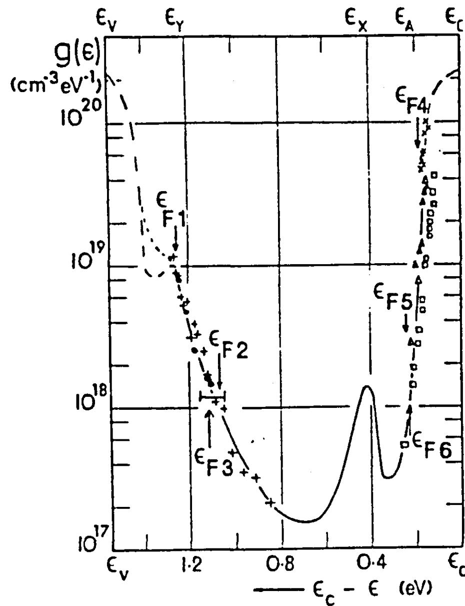



**Figure 2-2 :** The Field Effect Density of States[15].

valence band edges.

The validity of the field effect analyses has been questioned by the observation of Meyer-Neldel behaviour[16] in α-Si:H (see section 2.9.2) as the numerical methods used assume a constant conductivity prefactor. Additionally, the analysis of Schweitzer et al[19] , which includes the effect of correlated states (two electron states which have their energy level determined by occupation) raises further questions as to the validity of the FE DOS. This inclusion leads to a very different FE DOS which, in fact, is more similar to that obtained from Deep Level Transient Spectroscopy (DLTS). However, the values used for the effective correlation energies in their calculations are, in fact, considerably larger than those now proposed[20] for α-Si:H. Reviews of the field effect technique have been given by Spear[15] and Cohen[21] .

## 2.3.2 Deep Level Transient Spectroscopy.

This set of techniques is thought, by some, to give a more accurate representation of the bulk DOS than does the FE. However, DLTS can only be carried out on doped junctions and so, as mentioned above, problems relating

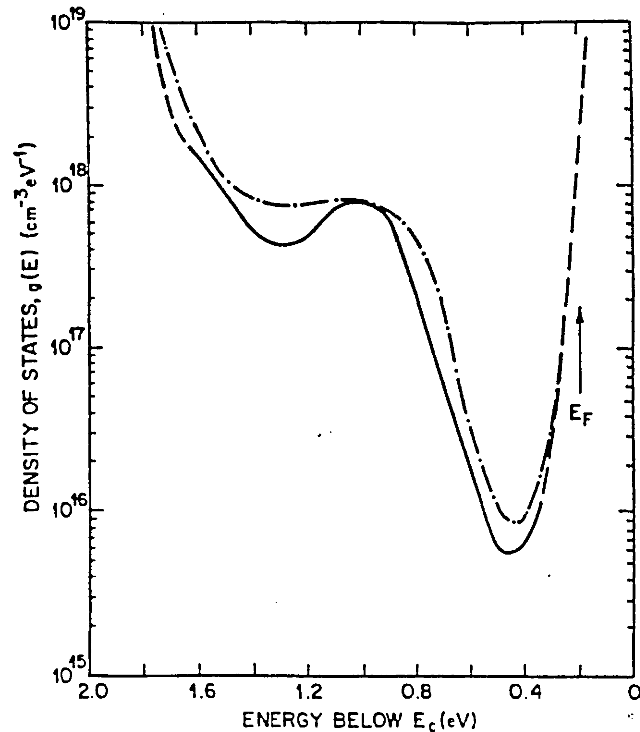



**Figure 2-3 :** Typical DLTS Density of States[21].

to inferring the DOS of *undoped* $\alpha$-Si:H, remain. A typical DLTS DOS is shown in figure 2-3. There are two features to be noted

1. A deep minimum about 0.4eV from $E_C$ (~$10^{15}$cm$^{-3}$eV$^{-1}$)
2. A peak in the middle of the gap (~$10^{18}$cm$^{-3}$eV$^{-1}$).

The analysis of DLTS has also proved to be problematical with the controversy centring around the definition of an energy scale. A review of DLTS has been given by Cohen[21].

## 2.3.3 Other Techniques.

1. Drift mobility measurements[22] suggest that the conduction band tail is nearly linear, at least from 0.08eV to 0.15eV below $E_C$. The valence band tail[14] has an approximately Gaussian profile in the range 0.2eV to 0.45eV below $E_V$.

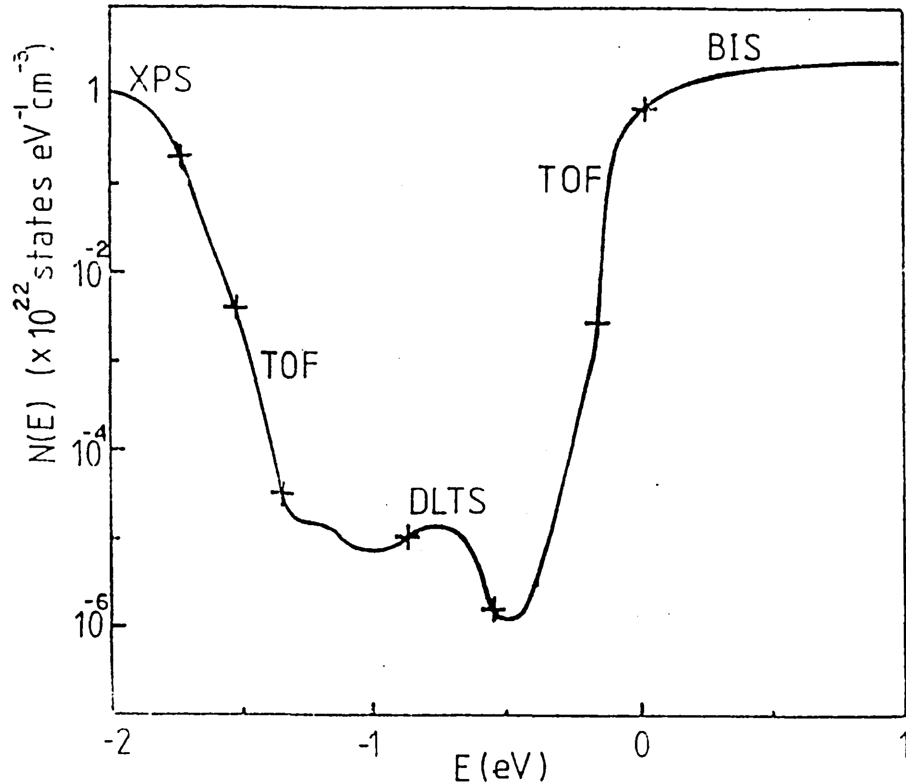



**Figure 2-4:** The distribution of states in α-Si:Has proposed by Marshall et al[14]. The techniques used to obtain the different energy regimes are also shown - Bremsstrahlung Isochromat Spectroscopy (BIS), Time of Flight (TOF), Deep Level Transient Spectroscopy (DLTS) and X-Ray Photoelectron Spectroscopy(XPS).

2. From ESR, optical absorption, luminescence, photocapacitance and photo-induced ESR, a wealth of information on the main mid-gap defects has been obtained[1]. The singly occupied dangling bond centre ($D^o$) is found to be the dominant paramagnetic centre and is situated approximately 1.1eV from $E_c$. The doubly occupied dangling bond centre ($D^-$) is placed about 0.9eV from $E_c$ (for a review of dangling bond energies see LeComber[23]). Photo-capacitance and photo-depopulation induced ESR measurements[24] suggest that the distribution of negatively charged dangling bond centres is approximately Gaussian with a standard deviation of ~ 0.1eV. The correlation energy between the dangling bond states is estimated to be[20] approximately 0.2eV.

Obviously many other techniques have been used to determine DOS profiles and some of these will be discussed later. However, the main features are qualitatively well described by those measurements detailed above.

## 2.4 The Central Features of the DOS in α-Si:H.

A consensus view[14] of the DOS in α-Si:H is perhaps beginning to appear (figure 2-4). Also shown in the figure, are the techniques used to study the different energy regimes. Obviously more work is required before this model is complete.

## 2.5 Electrical Transport Properties of Amorphous Semiconductors.

Given the disordered nature of amorphous semiconductors and that the band tail states are localised, it is possible to envisage a variety of processes by which a charged carrier might transit an amorphous semiconductor[25] (figure 2-5). In crystals, where conduction occurs through extended states, the free carrier mobility is limited by scattering events. Applying similar considerations to the amorphous state, the free electron mobility is estimated to be ~ 100 $cm^2V^{-1}s^{-1}$ (figure 2-5(a)). Much smaller mobility values may be obtained by assuming that the mean free path between scattering events is smaller than the interatomic spacing. Indeed if the free carrier transit is considered as being akin to Brownian motion, then mobility values of ~ 1 $cm^2V^{-1}s^{-1}$ (figure 2-5(b)) are obtained. If the transport is assumed to occur by direct tunneling within the localised states then an upper estimate of the mobility of ~ $10^{-2}cm^2V^{-1}s^{-1}$ (figure 2-5(c)-(d)) is obtained. Therefore, it is postulated that the mobility decreases rather sharply in the vicinity of the boundary between the localised and extended states, $E_c(E_v)$. It is for this reason that $E_c$ and $E_v$ are termed mobility edges.

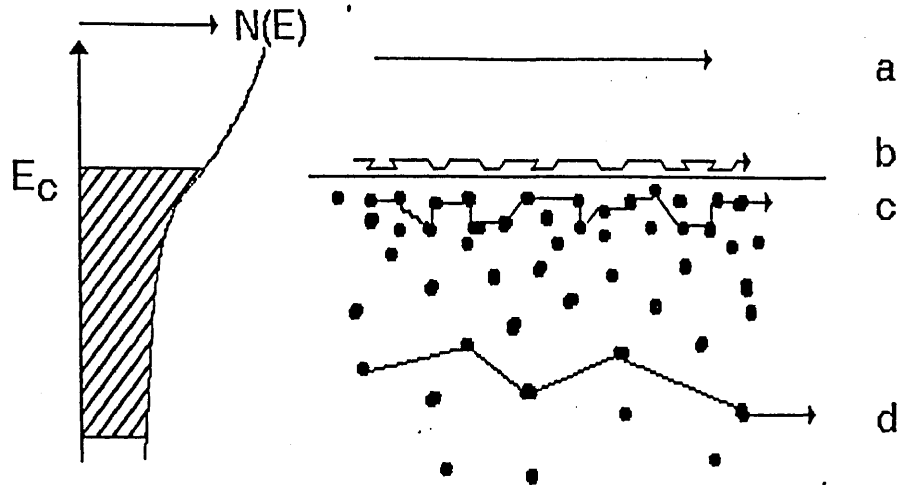



**Figure 2-5:** Electron transit through an amorphous semiconductor. Extended electronic states exist above $E_c$ while those below are localised (shaded area) (for notation see text)

A good review of the theory of conduction in amorphous semiconductors has been given by Nagels[26]. In the following electron transport is considered although similar considerations can be applied to hole conduction.

## 2.5.1 Extended State Conduction.

The conductivity of a material may be defined as

$$\sigma = -e\int N(E)\,\mu(E)\,kT\,(df(E)/dE)\,dE \qquad (2.2)$$

where N(E) is the density of states ($cm^{-3}eV^{-1}$) at an energy E, f(E) is the occupation function and $\mu(E)$ is the mobility. Since electron transport is limited to states within a few $kT$ of $E_c$, the conductivity can be written (after substituting for f(E))

$$\sigma_c = e\,N(E_c)\,kT\,\mu_o\,\exp[-(E_c-E_f)/kT] \qquad (2.3)$$

where $\mu_o$ is the electron mobility close to $E_c$. Estimates of the conductivity therefore depend on the DOS at $E_c$ and the extended state mobility (section 2.5).

## 2.5.2 Conduction in Band Tails.

When the conduction is dominated by hopping in the band tails, the mobility can be written

$$\mu_{hop} = \mu_{ho} \exp(-W/kT) \exp(-2\alpha R) \quad (2.4)$$

where $\mu_{ho} = (1/6)\, \nu_{ph}\, e\, R^2/kT$

$\nu_{ph}$ is a phonon frequency, $\alpha$ is a measure of the spatial extent of the wavefunction, R is the average hopping distance and W is the appropriately averaged hopping activation energy. The conductivity can be estimated using equation (2.2) to be

$$\sigma = \sigma_{ho} \exp(-2\alpha R) \exp[-(E_a-E_f+W)/kT] \quad (2.5)$$

where $E_a$ is the energy level at which the conduction occurs and $\sigma_{ho}$ is the conductivity prefactor. However, when the wavefunction overlap term is large the conductivity can be written

$$\sigma = \sigma_{ho} \exp[-(E_a-E_f+W)/kT] \quad (2.6)$$

### 2.5.3 Conduction in Localised States at the Fermi Level.

If the Fermi level lies in a band of localised states, the carriers can move between the states via a phonon-assisted tunneling process. The conductivity for such a process can be written

$$\sigma = (1/6)eR^2\nu_{ph}N(E_f)\exp(-2\alpha R)\exp(-W/kT) \qquad (2.7)$$

As the temperature is lowered the number and energy of the phonons decreases thus reducing the probability of the more energetic phonon assisted hops. Therefore carriers will tend to hop larger distances to find states of a similar energy. When this occurs, Mott's $T^{(-1/4)}$law is observed[9].

### 2.6 Doping of α-Si:H.

Prior to the mid 1970's, efficient doping of amorphous semiconductors had never been achieved and it was argued[12] that such a process was unlikely to occur, due to the absence of topological constraints in a random covalent network (the 8-N rule). However, once the possibility of relatively efficient doping had been successfully demonstrated[3], a new theory was required. This problem was tackled by Street[17,18] The terminology used in these sections is of form $X^a_b$ , where X represents the element, a the charge state of the individual atom and b the co-ordination number.

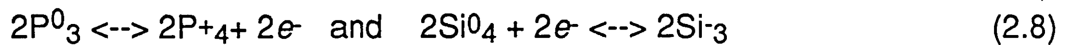
### 2.6.1 Street's Doping Model.

This discussion considers n-type phosphorus doping, although similar considerations can be applied to any dopant. In crystalline silicon, phosphorus is forced to take four-fold co-ordination by the topological constraints of the lattice - thus phosphorus bonds as $P^0_4$. The extra electron remains bound to

the parent atom unless there is sufficient thermal energy for ionisation to occur. In amorphous materials, the topological constraints are far weaker and phosphorus can bond as $P^0_3$ but not as $P^0_4$, since this is a violation of the 8-N rule. This does not explain doping. However, by extending the 8-N rule to charged defects, phosphorus may also bond as $P^+_4$, the state of the ionised donor. In singly doped α-Si:H charge neutrality is maintained via an increase in the dangling bond density of the same magnitude as the active dopant density. In compensated α-Si:H, the requirement for creation of charged dangling bonds is relaxed, since both positive and negative active dopant centres are created during deposition. The essential feature of the doping model, for α-Si:H is that phosphorus normally can only bond in the doping configuration if there is a compensating dangling bond created simultaneously (for n-type α-Si:H, a negatively charged dangling bond $D^-$ is created). Thus, the creation of dangling bonds is an integral part of the doping process and cannot be considered as a secondary phenomenon. This is a fundamentally different doping mechanism from that in crystalline silicon. In the crystalline material the dopant bonds in its neutral configuration whereas for doping to occur in the amorphous material charged defect formation must occur.*

During deposition of the doped material, the occupation of the band tail states increases significantly. A conduction band tail state is a neutral trapping centre when empty and is negatively charged when occupied. The charged state represents an unstable configuration which can be stabilised by the breaking of the weak bond responsible for the tail state. The total energy of the doubly occupied tail state and two negatively charged dangling bonds is similar, while the coulombic repulsion of the two carriers trapped in the localised band tail state produces an additional driving force for the reaction[20]. Therefore the reactions can be written

*Recently $P^0_4$ states have been found to exist in n-type a-Si:H suggesting that charged defect formation may not be a pre-requisite for doping to occur[20]



$$2P^{0}_{3} \longleftrightarrow 2P^{+}_{4} + 2e^{-} \quad \text{and} \quad 2Si^{0}_{4} + 2e^{-} \longleftrightarrow 2Si^{-}_{3} \tag{2.8}$$

However, more correctly, these should be combined as

$$2P^{0}_{3} + 2Si^{0}_{4} \longleftrightarrow 2P^{+}_{4} + 2Si^{-}_{3} \tag{2.9}$$

The law of mass action relates the total dopant concentration to the density of ACTIVE dopant centres via

$$(N_O - N_D)^2/N_D = \text{const} \tag{2.10}$$

where $N_O$ is the total phosphorus concentration and $N_D$ is the density of active phosphorus centres ($P^{+}_{4}$), and therefore, the density of negatively charged dangling bonds ($Si^{-}_{3}$).

## 2.7 The Conductivity & Mobility of α-Si:H.

The values for ($E_c$-$E_f$), as determined from the conductivity activation energy, vary from sample to sample depending on the deposition conditions and the doping levels. For good quality undoped α-Si:H the activation energy varies between 0.6 and 0.8eV over the temperature range normally covered by conductivity measurements. Additionally, mobility activation energies of 0.13eV for electrons[22] and about 0.4eV for holes[14] are obtained . Through doping, the Fermi level can be shifted to within about 0.2eV[27] of both $E_c$ and $E_v$.

The theory section (2.5) predicts different behavioural regimes of the conductivity and mobility. All of these features were experimentally observed ten years ago[27], on what was then regarded as high quality amorphous silicon. However, on today's state of the art material such features as the change in conductivity and mobility activation energies, assigned to a transition to hopping

within the tail states, and the transition to hopping through states near the Fermi level are no longer observed. It is envisaged that reductions in the tail state width and mid-gap DOS in today's high quality material, lead to these regimes not being experimentally resolved.

## 2.8 Photoconductivity in α-Si:H.

Herein the general properties of α-Si:H under illumination will be described.

### 2.8.1 Steady-State Photoconductivity.

Steady-state photoconductivity is described by a set of rate equations[28] which relate trapping, release and recombination effects. Steady-state photoconductivity, in conjuction with other techniques, identifies the main recombination centres as the various states of the silicon dangling bond, which are situated close to mid-gap. The intensity dependence of the photoconductivity has been interpreted in terms of Rose's[28] model. However, many of the experimental data are at variance with this simple interpretation and at present there is no single complete model.

### 2.8.2 Transient Photoconductivity.

These techniques study the transient rise or fall of the photoconductivity to flash illumination, either in a sandwich cell (Time of Flight Photoconductivity) or in a coplanar cell (Coplanar Photoconductivity). They allow information to be obtained about the carrier mobility, trapping and release from shallow states (and therefore capture cross-section and state densities), and also allow some information to be obtained about recombination (and possible rate limiting processes).[25,29]

## 2.9 On the Metastable Nature of Hydrogenated Amorphous Silicon.

The existence of metastable states in α-Si:H is of considerable import to this work. In this section, it is shown that α-Si:H is a metastable material. Changes in free carrier densities lead to reversible changes in the mid-gap DOS. Furthermore, the mid-gap DOS is found to depend upon previous thermal and bias conditions. The study of metastable states in α-Si:H stems from the original work of Staebler and Wronski[30], who reported fully reversible changes in the conductivity and photoconductivity as a result of prolonged illumination. Since then, further studies of the metastable nature of α-Si:H have been conducted and much progress has been made on the interpretation of this effect. Presently, there are two main models proposed for the reversible changes[31].

### (a) The two carrier model.

This model has been developed most fully by Stutzmann and collaborators[32]. Under steady-state illumination, holes become preferentially trapped in weak silicon-silicon bonding states (deep valence band tail states). Trapping of a hole leads to further weakening of the Si-Si bond, since an electron has been optically excited out of a bonding orbital. However, the majority of weak silicon-silicon bonding states are not broken by such a process. The additional energy required to break the bond is provided by a direct, non-radiative electron-hole recombination event. This results in the formation of two spatially close dangling bonds. Given the energetics of the situation, it is to be expected that the two dangling bonds will reform unless they become spatially separated by an additional atomic re-arrangement. This can be achieved by the switching of a back bonded hydrogen atom onto one of the created dangling bonds (figure 2-6). More complicated variants of the microscopic process have been put forward, but the important part of this model is that the energy for the breaking

of the weak bond is the energy released by a non-radiative electron-hole recombination event.

(b) The one carrier model.

Initially, it was thought that a one carrier process could not produce sufficient energy for bond breaking to occur. In the study by Kruhler et al[33], α-Si:H structures (both n-i-n and p-i-p) were subjected to photo-stress and bias stress. Both structures exhibited photo-degradation as expected. However, the p-i-p diode showed completely reversible effects, typical of the Staebler-Wronski effect, purely under hole injection. This was ascribed to a model in which hole trapping is responsible for breaking weak bonds and the resultant formation of dangling bonds.

A more recent study of light and current induced effects in diodes has been conducted by Yamagishi et al[39]. They studied the relationship between the mobility-lifetime product and the dangling bond density. They found that creation of dangling bonds could occur either by electron hole recombination or via free carrier trapping into weak band tail states.

A detailed model based on the above, has been developed by Muller and collaborators at the Max-Planck-Institut fur Kernphysik (see below).

**2.9.1 Thermal Equilibration and Bias Annealing of α-Si:H.**

The dangling bond density of both doped and undoped α-Si:H is found to depend on the cooling rate and bias conditions, subsequent to exposure to high temperatures. A theoretical approach to these effects has been developed[35], in which the central idea is that α-Si:H possesses an intrinsic tendency to reduce the concentrations of free carriers in the conduction and valence bands via the

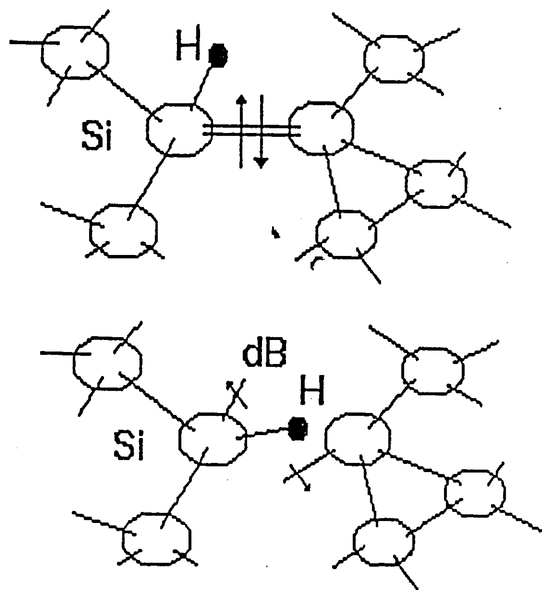



**Figure 2-6 :** Dangling bond creation and switching of back bonded Hydrogen

formation of dangling bonds. The model, which is essentially an extension of the doping mechanism proposed by Street[17,18] may be described as follows.

According to the '8-N' rule, a neutral silicon atom is incorporated into the growing film with 4-fold co-ordination. The free electron and hole densities are low at room temperature, resulting in a low tail state occupation. To a good approximation, four valence electrons are associated with each lattice site, and the four fold coordination of the silicon atoms is consistent with the 8-N rule. However, if by some means (photo-excitation, carrier injection, etc.) the free carrier density is significantly increased, then the number of silicon atoms whose co-ordination is inconsistent with the requirements of the 8-N rule is increased. It is suggested that, in reaction to this violation, atomic re-arrangements take place to satisfy the rule. The process is represented by :-

$$2Si^0_4 + 2e^- \longleftrightarrow 2Si^-_3 \qquad (2.11)$$

To avoid immediate reformation of the weak bond, it is suggested that the dangling bonds are spatially separated via the diffusion of hydrogen from a local

site (figure 2-6). In terms of the law of mass action, this equation is expressed as:-

$$\frac{[Si^0_4][e^-]}{[Si^-_3]} = K_n \qquad (2.12)$$

where $Si^0_4$ represents a neutral 4-fold co-ordinated conduction band tail state and $K_n$ is the equilibrium constant. Therefore, the higher the electron density, the greater the dangling bond concentration (and vice versa).

Annealing treatments to reduce the dangling bond density can be explained by the above model. During a reverse bias annealing process, the number of free carriers is reduced to well below the equilibrium density. At the same time, the junction is heated to a temperature sufficient to allow a new equilibrium condition to be established rapidly. During this time, the concentration of dangling bonds decreases in accordance with the law of mass action. Maintaining the reverse bias while the junction is cooled freezes in the lower number of dangling bonds.

Experimental evidence in support of such a model has recently been provided, not only from measurements of the Staebler-Wronski effect, but by determinations of thermal equilibrium processes in doped and undoped material.

Studies by Smith and co-workers[36] show that, unless the cooling rate is sufficiently slow that the system is always in equilibrium, a residual number of dangling bonds will occur. They also propose that, even at room temperature, metastable state creation occurs via intrinsic recombination. However, the rate of creation is very slow, due to the low numbers of free carriers (in the undoped material), and at room temperature is negligible.

More recently, Street and Kakalios[37,38] studied the thermal equilibration and bias annealing processes of doped α-Si:H, and the influence of such factors on the electronic transport[39]. They propose that the number of electrons in the tail states is related to the number of donor sites and dangling bonds (for n-type material) by

$$N_{BT} \sim N_D - N_{DB} \qquad (2.14)$$

also

$$N_{BT}(T) = \int N(E)\,\{1 + \exp[(E - E_f) / kT]\}^{-1} dE \qquad (2.15)$$

where $N_{BT}$ is the number of occupied band tail states, $N_D$ is the number of active dopants, $N_{DB}$ is the number of charged dangling bonds and N(E) is the density of states. At higher temperatures $N_{BT}$ increases. On cooling, two possibilities exist (subject to the constraints inherent in the above equations). If $E_f$ remains constant, then in order for $N_{BT}$ to decrease with temperature, the density of donors and dangling bonds must change. The second possibility is that as the temperature is lowered, the structure cannot relax any further (over the experimental timescale) and becomes effectively frozen in, resulting in a constant $N_{BT}$. If this occurs then the Fermi level $E_f$ has moved to a non-equilibrium position. Thus structural relaxation occurs at room temperature to return the Fermi level to the minimum energy position thus lowering $N_{BT}$. Therefore, it is this structural relaxation which causes the long time constants for the conductivity decay observed at room temperature in the doped material.

The extension of the above model to the case of reverse bias annealing[38] is straightforward. Under a reverse bias, the Fermi level moves further away from the conduction band edge and therefore away from its equilibrium position. The structure tends to re-adjust so that $E_f$ is restored to the minimum energy

configuration by changes in $N_D$ or $N_{DB}$ (but without changes in $N_{BT}$ because charge neutrality does not hold). When the temperature is lowered, the structure associated with the lower $N_{BT}$ is frozen in. Upon bias removal, charge neutrality is applicable and $N_{BT}$ increases to a non-equilibrium value thus shifting $E_f$ (equations (2.14) and (2.15)). This is an unstable configuration and so the material relaxes towards its equilibrium state.

The microscopic mechanisms involved in the above processes are not clear. However, changes in the silicon dangling bond density (given their known metastable nature) are suggested as being responsible for the structural reconfigurations. The freezing-in of the structure is tentatively associated with the reduction in mobility of hydrogen, within the amorphous silicon matrix, at lower temperatures. As a consequence, while all the above results were obtained on doped material, it is expected that an equivalent equilibration process will occur in undoped material, perhaps similar to that suggested by Smith and Wagner[36].

### 2.9.2 The Meyer-Neldel Rule.

The Meyer-Neldel rule, which relates the conductivity prefactor to the conductivity activation energy is often observed in α-Si:H. However, the reason for this behaviour is not clear. Suggestions include a statistical shift of the Fermi level[40] and the influence of band bending[41]. Recently a Meyer-Neldel type relationship has been observed[32,42] between the attempt to escape prefactor and the annealing activation energy of the Staebler-Wronski Effect. To the author's knowledge, there has never been an attempt to explain such behaviour in α-Si:H#. However, recent work on *doped* α-Si:H[39] shows that the Meyer-Neldel rule can be related to the presence a non-equilibrium density of dangling bonds, via a statistical shift model. It is suggested that the Meyer-

#Very recently, it has been proposed that the Meyer-Neldel rule may be due, in part, to the diffusion of Hydrogen through the silicon lattice[75].

Neldel rule for $\alpha$-Si:H is an artefact arising from the non-equilibrium nature of the material. Given that there is a Meyer-Neldel type relationship observed for the annealing of the Staebler-Wronski Effect (in which there is also a large excess of dangling bonds) it is possible that the metastable nature of the material contributes towards this behaviour.

## 2.10 Summary

In the above sections it is shown that many of the properties of $\alpha$-Si:H can be related to metastable changes in the mid-gap density of states. Two models are discussed in which the metastable changes can be related to the breaking of weak silicon-silicon bonds via either a recombination process or simply by carrier trapping. Additionally, thermal equilibration and bias annealing processes are discussed in terms of a model in which the transport properties of $\alpha$-Si:H are related to the non-equilibrium structure of the material.

# CHAPTER 3
# ELECTRONIC PROPERTIES OF AMORPHOUS SILICON THIN FILM TRANSISTORS AND HETEROJUNCTIONS AND OF AMORPHOUS SILICON NITRIDE.

## 3.1 Introduction.

One of the main aims of this thesis is to evaluate the evidence relating to charge trapping instabilities in amorphous silicon/silicon nitride structures. In this chapter, the various trapping effects observed in layered structures are reviewed, together with the electronic properties of $\alpha$-$Si_{1-x}N_x$:H (herein referred to as $\alpha$-SiN:H).

## 3.2 Amorphous Silicon Thin Film Transistors and Heterojunctions.

$\alpha$-Si:H TFTs were first developed to study the DOS via the Field Effect(FE) measurement technique[43]. This original work was conducted on structures with Corning 7059 glass as the gate insulator. If large voltages were applied a significant current modulation could be obtained. Therefore, it was realised that the possibility existed to build devices which would operate satisfactorily at voltages compatible with TTL circuits. Development work progressed, and TFTs with a thin film gate dielectric, constructed from $\alpha$-$SiO_x$ or $\alpha$-SiN:H, were produced. Subsequently, it has been shown[5] that the best devices are of the

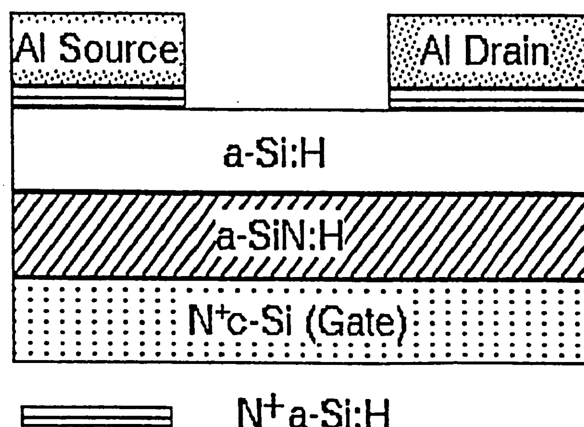



**Figure 3-1** An inverted staggered $\alpha$-Si:H thin film transistor of the configuration used in the reported Philips measurements[5]

inverted staggered configuration, (figure 3-1) with $n^+$ layers underneath the source and drain contacts, supplying the conduction electrons. Typically, a good TFT has an off current of less than $10^{-11}$A, and an on current of greater than $10^{-6}$A, at voltages compatible with TTL circuits. Very recently, more complex variants have been developed[44,45] which are capable of driving considerably larger currents.

Obviously, an important property of the TFTs is their stability. The most obvious device instability is that of the threshold voltage shift, resulting from continued application of a gate voltage[7]. Based on measurements of charge trapping effects in MNOS structures[46,47], it was suggested[7] that under application of a positive gate voltage, electrons attracted to the interface were injected into the nitride. Until this study, this was the only explanation for the long term drift of α-Si:H TFTs. The evidence relating to such a model is discussed below.

### 3.2.1 Trapping Centres at the Interface and in the Insulator.

Trapping centres in α-Si:H and the insulating layer upon which it was deposited have been studied by essentially two techniques; those of the measurement of the threshold voltage shift[5,48,49] and the determination of the electron transport mechanism through the structure[50,51,52,53]. Measurements of charge trapping phenomena on structures with different insulators or insulators prepared under different deposition conditions have revealed that the magnitude of the charge trapping effect varied (for reviews see Powell[5] and Ast[48]). The trapping phenomena have been separated in terms of two time regimes :-

- upto 0.5secs, in which the trapping was independent of the insulator
- after 0.5secs, during which trapping was dependent upon the insulator

Recent computer data by van Berkel et al[49] have provided evidence in support of such an observation.

By studying the temperature and field dependence of the slower time regime identified above, it has been possible to determine the electron transport mechanism within the insulating layer. Powell[7] conducted such studies on TFTs with insulators fabricated of α-SiN:H and proposed that the conduction was dominated by a hopping process ($E_a$~0.3eV) via a set of localised states close to the nitride Fermi level. He proposed that this slow process was the rate limiting step of the threshold voltage shift.

Direct determinations of the electron transport mechanism through structures similar to the above have also been conducted[50,51]. Charge generated within the α-Si:H was found to be tra .ferred very efficiently into the insulating layer, which it subsequently tra versed with an activation energy of 0.3eV. It was proposed that charge was injected from the silicon conduction band into lower lying defects within the insulator through which conduction occurred. The mobility of these carriers was also found to have an activation energy of ~0.3eV. Since the conductivity and mobility had the same activation energy, it was proposed the conduction occurred via a hopping process.

Information concerning the origin of the defects within the insulator may be obtained by studying charge trapping in structures with the device quality insulating and active layers separated by a degraded layer of insulating material[52,53]. The amount of charge trapped in a structure consisting of device quality layers α–Si:H and α-SiN:H separated by a poor quality layer of α-SiN:H was found to vary when the composition of the degraded layer was changed. Such an effect was ascribed to a variation in the number of nitride-related traps. The removal of trapped charge from these defects was found to have an activation energy of 0.65eV. This was interpreted as the release of

charge from nitride defects close to the interface to the α-Si:H conduction band edge.

Thus far, only the defects with long time constants ( > 1 second, herein referred to as slow states) have been considered. Fast states have also been identified using transient photoconductivity as the probe[52,54]. Such studies revealed shallow states ~ 0.25eV from $E_C$. The number of these defects was found to depend upon the order of deposition and not upon the composition of the nitride. If the nitride was deposited on top of the α-Si:H (top nitride) the defect density was found to be ~ $5 \times 10^{11} cm^{-2}$ whereas when the silicon was deposited upon the nitride the defect density was a factor of 10 less. Such an asymmetry in defect density was not unexpected, since structural studies[55] revealed a much larger nitrogen concentration within the α-Si:H for bottom nitride than top nitride. It was postulated that, as both layers were grown in the same chamber, ammonia absorbed onto the reactor chamber walls was incorporated in the α-Si:H layer subsequently grown. It was thought that the larger nitrogen contamination at the bottom nitride interface would lead to a larger trapped charge. However, since the larger trapping effect occurred at the top nitride it was postulated that the active trapping centres were not due to excess nitrogen but to ammonia molecules incorporated into the film during growth.

To summarise, two sets of states have been identified, in which charge may become trapped :-

1. Defects in the nitride, which become occupied due to charge injection from the silicon conduction band. Subsequent re-distribution of this charge via a hopping process limits the rate of threshold voltage shift. The charge in these states was

removed by a hopping process to the interface, and thence by thermal activation (0.65eV) to the silicon conduction band.

2. Defect states created during deposition, which resulted from the presence of large amounts of ammonia in the discharge plasma. These states are shallow or 'fast' and are located about 0.25eV from $E_c$.

### 3.2.2 Metastable Silicon Dangling Bonds.

Powell et al[5] carried out experimental measurements and computer calculations on TFT transfer characteristics. Agreement between computer generated transfer characteristics and experimentally obtained ones was only achieved if an excess density of mid-gap states existed within the silicon layer close to the interface. Furthermore, studies of the Staebler-Wronski effect in TFTs[56] showed that metastable state creation could lead to a positive shift in the threshold voltage.

Recently the author and co-workers[57] suggested a model in which the shift of the threshold voltage could result from the creation of metastable silicon dangling bonds under accumulation conditions (section 6.2). Schropp et al[58] have provided supporting evidence based on measurements of the on-current decay in TFTs. The structures which they studied had thermally grown, high quality "defect free" $\alpha$-$SiO_2$ as the gate insulator and therefore they could not ascribe the phenomena to tunnelling into the insulating layer.

### 3.3 Amorphous Silicon/Silicon Nitride Multilayers.

One of the main advantages of studying multilayer structures is that by varying the thicknesses of the layers, information can be obtained concerning the relative contributions of 'bulk' and interface.

### 3.3.1 General Properties of Silicon/Silicon Nitride Multilayers.

Optical absorption, photoconductivity and conductivity studies[59] have shown that, at the interfaces, a larger density of mid-gap states existed. The optical absorption studies also revealed an increase in the band gap (accompanied by an increase in the conductivity activation energy), as the silicon layer thickness decreased, suggestive of the presence of excess hydrogen or nitrogen. However, the sub-band gap absorption data indicated that no significant nitrogen contamination occurred. Furthermore, as the silicon layer thickness decreased below about 250A, the Meyer-Neldel rule for the conductivity was not observed. This was associated either with the pinning of the Fermi level in a high density of states or with nitrogen contamination (as the Meyer-Neldel rule is not observed when small amounts of nitrogen are introduced to amorphous silicon[59]). Despite the fact that a larger density of mid-gap states existed at the interface, a fatigue of the photoluminescence was also observed, under illumination. Such an observation was consistent with an increase in the mid-gap density of silicon dangling bond states.

**Persistent Photoconductivity.**

Persistent photoconductivity, the phenomenon of long term photocurrent decays subsequent to the removal of illumination, has often been observed in $\alpha$-Si:H - a related phenomenon is that of the long term on-current decay in a TFT. It has been suggested[60] that inhomogeneous regions existed at the interface in which charge might become trapped, thus polarising the film. Within this model the slow dark current decays and the persistent photoconductivity effect were associated with the depolarisation of the film. From subsequent simulation studies, it was suggested that the traps existed ~ 0.7- 0.8eV from $E_c$ and had a density ~ $10^{11}$cm$^{-2}$.

**Electroabsorption Measurements.**

Roxlo et al[61] studied charge distributions close to the interface of α-Si:H/α-SiN:H. They found an electron accumulation region through a wide layer of the α-Si:H, and a large concentration of hydrogen at the interface. Additionally the charge density found at the bottom nitride interface ($6X10^{11}cm^{-2}$ - $3X10^{12}cm^{-2}$) was greater than at the top nitride interface, in contrast with the results of the Xerox group[54].

**Photoluminescence Studies**

Recently, Wilson et al[62] studied photoluminescence of α-Si:H layers, on α-SiN and α-$SiO_2$ substrates, as a function of layer thickness. Significant changes were found to occur as the layer thickness decreased and as the number of layers inceased. Such results were interpreted in terms of a combination of excess hydrogen and excess stress at the interface, and nitrogen contamination in the α-Si:H layer.

## 3.3.2 Summary

The above experimental data provide evidence for the existence of a larger mid-gap DOS and hydrogen concentration at the α-Si:H/α-SiN:H interface than in the bulk. The observation of nitrogen contamination is more controversial, but seems probable due the reactive nature of the ammonia molecules from which the nitride layer is produced.

## 3.4 Structural, Electrical and Optical Properties of Amorphous Silicon Nitride.

Amorphous silicon nitride, produced by the glow discharge process, is rarely a stoichiometric material, and should therefore be written as $\alpha$-$Si_{1-x}N_x$:H. Many of the electronic and optical properties of $\alpha$-SiN:H have been found to vary with composition. As x increased both the optical gap and the low-field (high temperature) conductivity activation energy increased[59,63,64]. Robertson and Powell[65,66] have proposed silicon and nitrogen dangling bonds as the main defect states in the nitride. Recent measurements on heterojunctions[52,53,67] placed the silicon dangling bond, within the nitride, at approximately 0.6-1.0eV from the $\alpha$-Si:H conduction band edge and suggested that its density varied with composition and deposition conditions.

## 3.5 Summary and Model of the $\alpha$-Si:H/$\alpha$-SiN:H Interface

By assimilating the information presented above it is possible to construct a model of the silicon/silicon nitride interface. From figure 3-2 it is seen that the silicon dangling bonds within the nitride are energetically below the $\alpha$-Si:H conduction band edge. Thus, relatively efficient injection of negative charge from the $\alpha$-Si:H to the nitride can occur[50,51]. Injected electrons transit the insulating layer via hopping through silicon dangling bond defects[7,51]. The removal of charge from the nitride is thermally activated with an energy of 0.6-1.0eV[52,53,67]. Two different sets of interface state exist, one set shallow and the other deep, whose concentration depends upon the order of deposition and the composition of the nitride layer respectively[52,53,54]. Close to the interface, but within the $\alpha$-Si:H layer, a higher than bulk mid-gap density of states exists[5,59]. Additionally, it is proposed that changes in the mid-gap DOS close to the interface are induced via the excess occupation of the conduction band tail states[57,58] (see chapter 6).

In conclusion, the trapping centres and processes which occur in amorphous silicon/silicon nitride structures have been discussed. A picture has been presented in which trapping is possible either within the α-Si:H, the insulator or at the interface. In the chapter 6, the experimental results of the present study will be discussed, in terms of these competing processes.

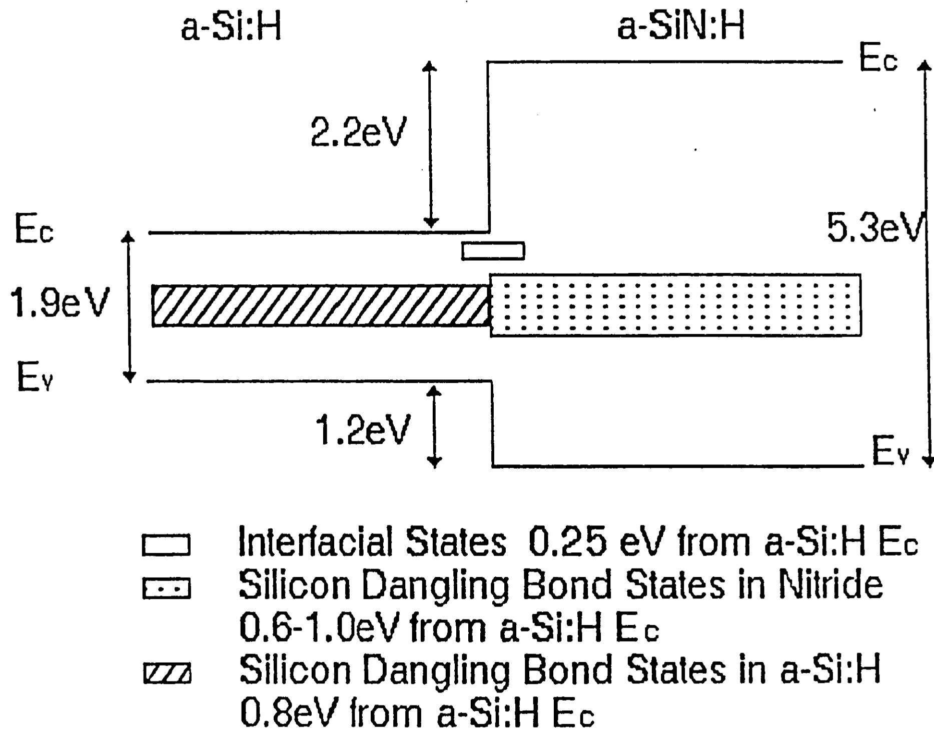



**Figure 3-2 :** Schematic model of the α-Si:H/α-SiN:H Interface

# CHAPTER 4

# EXPERIMENTAL TECHNIQUES AND SYSTEMS.

This chapter begins with a discussion of the glow discharge deposition process and its applications. The glow discharge system used to deposit the samples investigated in this study is then described. Following this, the sample structure and preparation conditions are detailed. The experimental techniques are then discussed in some detail. Finally, the experimental measurement systems are described.

## 4.1 The Glow Discharge Process.

The glow discharge process is a low power plasma processing technique, which involves coupling power (inductively or capacitively) into the reactive gas thus decomposing it. α-Si:H is produced by the decomposition of silane (which is often diluted with an inert gas such as argon) into such species as Si, Si-H etc, which then adhere to a substrate. The material quality depends on such factors as RF power and frequency, gas flow rate, chamber pressure and geometry and substrate temperature. This process has, to date, produced the best quality α-Si:H and allows relatively efficient doping. Other α-Si:H alloys produced by this technique include α-SiN:H, α-SiC:H and α-SiGe:H. Typical deposition parameters for α-Si:H, are shown in table 4-1. Spear[15] and Hirose[68] have produced excellent reviews of the glow discharge process.

| Parameter | Range |
|---|---|
| $SiH_4$ concentration | 10-100% in $H_2$ or Ar |
| Total gas flow rate | 20-200 sccm |
| Total Pressure | 0.05-2.0 Torr |
| rf Power | 1-100 W |
| Substrate Temperature | 200 - 300$^{o}$C |
| Substrate Bias | Mostly zero |

**Table 4-1:** Typical deposition parameters for capacitively coupled glow discharge systems[68].

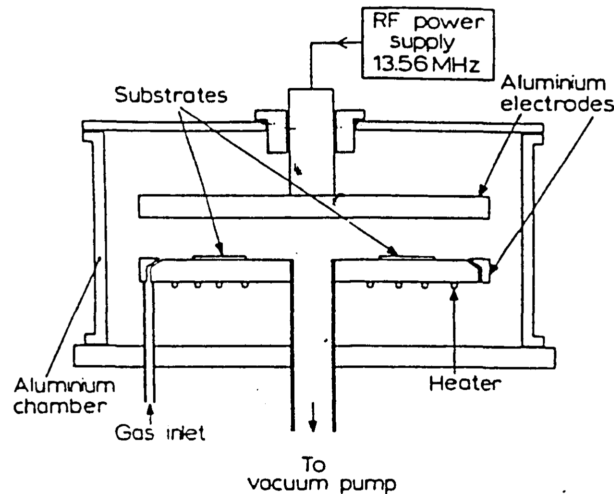



**Figure 4-1 :** Schematic layout of the capacitive reaction chamber at Philips Research Laboratories[69]

## 4.2 The PlasmaTherm PK12 Deposition System at Philips Research Laboratories

The lay-out of the reaction chamber is shown in figure 4.1. The gases flow from the perimeter of the heated lower electrode, which supports the substrates. Spent gases are pumped down through the centre of this chamber. Radio Frequency power at 13.56MHz is supplied (and is coupled capacitively into the plasma) from a 500W generator fitted with automatic power and matching facilities. An automatic valve and rotary blower in the vacuum line provide a wide range of working pressures. The gas flow rates are controlled by mass flow controllers. A detailed description of the structural and electronic properties of the "as produced" material, has been given by Easton et al[69].

## 4.3 Sample Preparation.

The TFTs investigated in this study are of the inverted staggered configuration (figure 4-2). An n+ crystalline-silicon substrate is used for the gate electrode, a thin (~0.5μm) layer of near-stoichiometric α-SiN:H is deposited as the insulator

| Sample | Flow Rates SiH4 (sccm) | NH3 | NH3/SiH4 ratio(R) | Growth Rate (A/min) | Pressure (Torr) | Power (W) | $T_D$ ($^oC$) |
|---|---|---|---|---|---|---|---|
| α-Si:H | 36 | - | | 304 | 0.8 | 20 | 300 |
| P2301 | 20 | 200 | 6.0 | 180 | 0.6 | 20 | 300 |
| P4482 | 20 | 200 | 6.0 | 180 | 0.6 | 20 | 300 |
| P526 | 16 | 200 | 7.5 | 230 | 0.6 | 20 | 300 |
| P527 | 13.4 | 200 | 9.0 | 200 | 0.6 | 20 | 300 |
| P530 | 8 | 200 | 15 | 220 | 0.6 | 20 | 300 |

**Table 4-2:** Deposition parameters for the thin film transistors used in this study. The first line gives the parameters for the α-Si:H and the others the deposition parameters for the nitride layers.

while the active layer (0.5μm) is pure α-Si:H. The complete structure is grown in the one chamber. The deposition parameters are shown in table 4-2. Conventional photolithography is used to define the source and drain contacts of evaporated aluminium. The channel length of the transistors is 50μm, and the channel width to length ratio is ~ 1700.

## 4.4 Experimental Techniques

Charge trapping effects are known to be responsible for the threshold voltage instabilities observed in α-Si:H TFTs. Therefore, it is important that the energetic and spatial location of the excess charge be determined. Additionally, it is desirable to identify any factors which influence the magnitude of the excess trapped charge.

Prior to the initiation of this study, no direct probe had been developed to study excess trapped charge in α-Si:H TFTs. The technique described below acts as a probe of any charge which is trapped in slow states and renders information about its magnitude and spatial location. Additionally information can be obtained concerning the activation energies of the processes which contribute towards the dark discharge of the excess charge (chapter 6.3).

The novel "discharge technique" was developed as a consequence of work carried out by the author et al, on the transient photoconductive response of α-Si:H TFTs[8]. While the techniques used at both Philips Research Labs. and at Dundee College of Technology are basically the same and return similar information, there are a few procedural differences as indicated.

As shown in figure 4-2, the TFT is operated as a capacitor with the source and drain electrodes linked together. A positive voltage is applied to the gate of the TFT, for a time $t_g$, trapping charge close to the silicon/silicon nitride interface. During the subsequent time period, $t_d$, a dark discharge occurs during which some of the excess charge is neutralised via internal processes. This

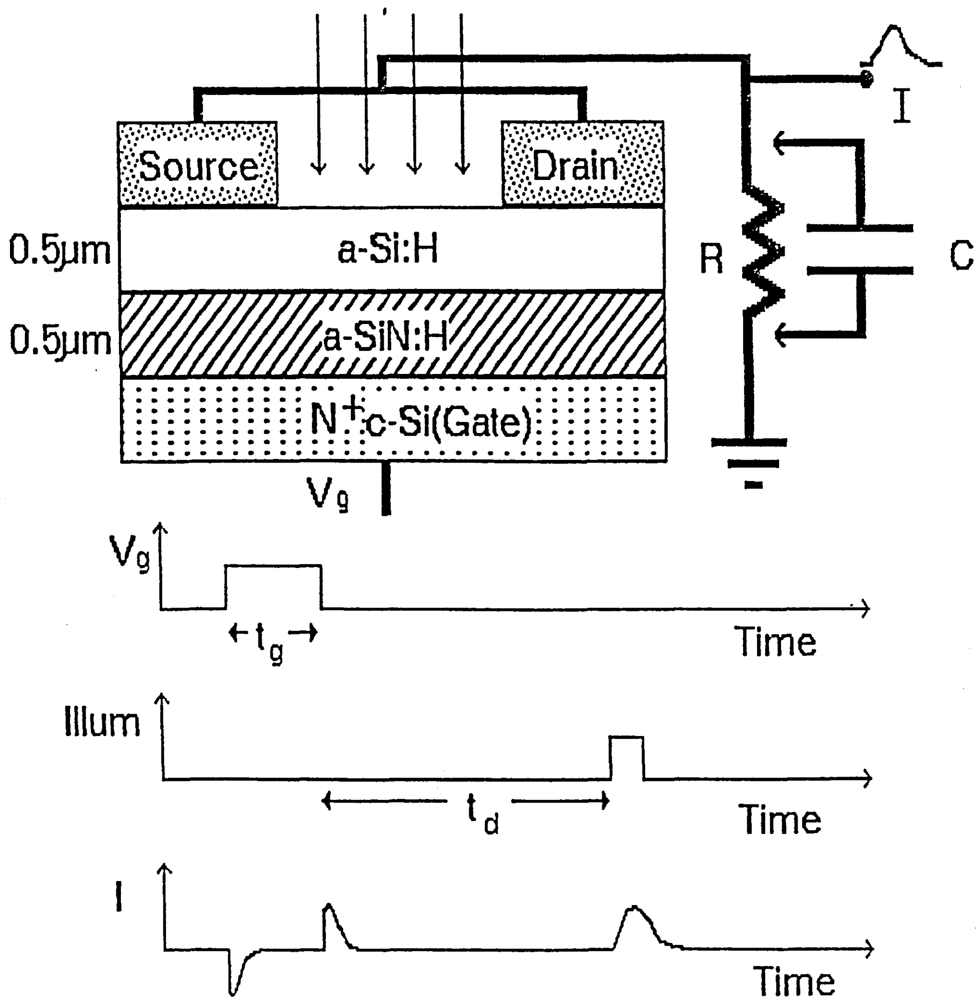



**Figure 4-2 :** Experimental procedure.

neutralisation process (which necessarily involves charge movement) can be monitored directly, as in the experiments conducted at Philips. Alternatively, at the end of the delay period, the remaining excess trapped charge can be determined via integration of a photo-discharge transient, generated as a consequence of illumination. This technique allows the experimenter to vary the magnitude and length of the field pulse, the delay time, the intensity and wavelength of the illumination and the temperature at which the measurement is conducted.

### 4.4.1 Detailed Description of the Experimental Procedure.

A positive voltage (typically 10-30V) is applied to the gate of the TFT, for a time period $t_g$ (typically 10-20 seconds - however, in some circumstances the gate voltage was applied for periods upto a week). Under these conditions, essentially the whole of the α-Si:H active layer is under accumulation and the source/drain electrodes are injecting. Electrons attracted towards the interface may become trapped in :-

- localised states in the α-Si:H
- trapping centres in the nitride (after a tunneling process)

After the gate field application time, $t_g$, the gate voltage is removed. Due to the residual excess negative charge trapped at the interface, the device now moves into depletion. During a subsequent delay time, $t_d$ (20ms - 10000s), this excess charge is partially or totally neutralised (in the dark) by internal processes, such as (section 6.3) :-

- Tunneling of electrons from the nitride to deep states at the interface, followed by thermal release from these states to the silicon conduction band.

- A xerographic dark discharge mechanism
- Thermal release of trapped electrons from within the α-Si:H or at the interface, to the silicon conduction band

At Dundee, subsequent to $t_d$, the sample is illuminated from a LED, with a pulse of light of sufficient total flux to completely photo-discharge the excess charge. The illumination occurs through the free surface of the α-Si:H. A xerographic photo-discharge process is suggested for the neutralisation mechanism under illumination (see section 5-2). The illumination of the sample causes generation of electrons and holes, which separate under the field induced by the residual excess trapped charge. This separation of charge results in a photo-discharge current transient, which is detected across a sampling resistor. Thus, even though the illumination does not directly release the trapped carriers, the magnitude of charge detected by the sampling resistor establishes the amount of charge remaining trapped in slow centres.

For delay times less than 2s integrated pulse measurements were not performed (because of time constant limitations). In these circumstances, the pulse height is measured and converted into a maximum current, while the temporal width at half height, t, is also noted. The total charge is then estimated via

$$Q = I.t$$

This obviously is not as accurate as the integrated charge measurements, but in practice the error involved proved not to be significant.

The amount of excess charge residing in the sample is determined as a function of time $t_d$. Plotting excess charge versus $t_d$ generates what are termed "discharge curves". Measurements of these curves as a function of

temperature allow activation energies and attempt-to-escape pre-factors of the dark discharge processes to be determined. The activation energy is determined from a plot of the natural log of the discharge time constant against inverse temperature, and the attempt to escape pre-factor from the intercept with the time axis. As discussed in section 5-3, the discharge curves are not of a singly exponential nature. Thus a fitting procedure must be used to determine a release time constant from a distributed set of states. In this case release from a gaussian distribution of states is found to provide a good fit to the experimental data. Release curves are generated for gaussian distributions of states (of varying standard deviations) with a central release time constant set to be 1000 arbitrary units. The experimental data are then fitted to these computer generated curves, giving a measure of the width of the gaussian distribution. The known central release time constant is then converted into real time by comparison of the two time scales ie 10 seconds may be found to equal 250 arbitrary units so the central release time (1000 arbitrary units) corresponds to 40 seconds.

The measurement technique used at Philips is different, in that the current induced by charge redistribution within the specimen (subsequent to the removal of $V_g$) is continuously monitored by an electrometer <u>during</u> the time $t_d$. Thus a measurement of the amount of charge which has been dark discharged, rather than the amount remaining is obtained. However, this does not allow a direct comparison with the experimental results obtained at Dundee. This is achieved by using the illumination technique at the end of the measurement time($t_d$), to determine the residual charge. By combining the two measurements composite discharge curves may be generated.

### 4.4.2 Variations on the basic Measurement Technique.

#### 4.4.2.1 Device Stressing.

In this measurement, the gate voltage is applied for an extended time. Subsequently, after a fixed delay time ($t_d$=2 secs), the amount of excess charge residing in the sample is determined. This allows the build-up of charge within the sample to be monitored as a function of the stressing time. The time of field application constitutes a cumulative variable, in the sense that the total stressing time is treated as being of import, rather than the length of the individual stressing pulse. At Philips Research Labs. the devices are stressed with a source-drain voltage applied as well as a gate voltage. The amount of charge trapped in the device may also be measured independently by determining the threshold voltage shift from measurements of the transfer characteristic (section 4.4.3), in addition to the direct probe described above (section 4.4.1). This allows a direct assessment of the relationship between the two techniques and a comparison of their sensitiviy to the magnitude of the total trapped charge. Additionally, the activation energies of the dark discharge processes after various amounts of stress are investigated using the following procedure. The device is stressed for a given time period and the threshold voltage determined from the transfer characteristics. The activation energies of the dark discharge processes are then measured using the procedure described in section 4.4.1. The transfer characteristic is then measured again to check that the threshold voltage has remained constant during the discharge measurement. The device is then further stressed and the measurement sequence repeated.

#### 4.4.2.2 Device Annealing.

Typically the devices are stressed for ~ 24 hours before this high temperature (typically 350K-400K) measurement is initiated. The basic procedure is shown

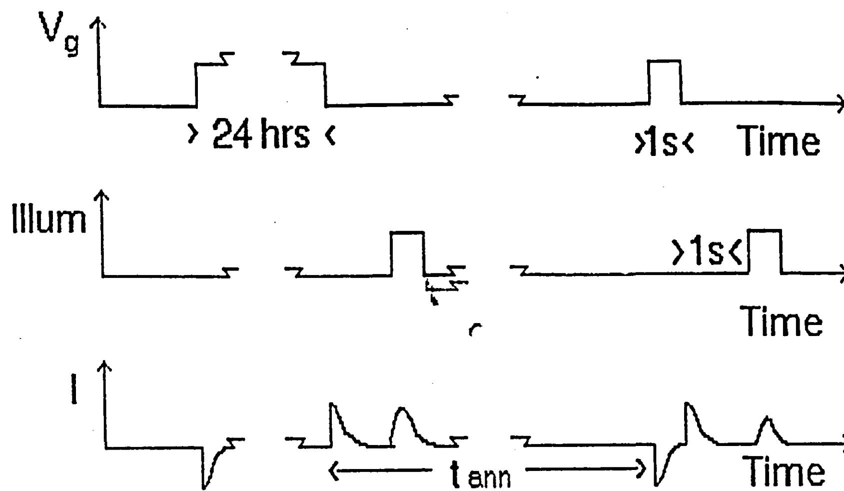



**Figure 4-3 :** Annealing Procedure

in figure 4-3. After stressing, the device is discharged completely by a pulse of illumination. After a period (the annealing time $t_{ann}$), a further short (1 sec) application of gate voltage occurs. Following this, the amount of charge remaining in the sample is determined by the flash illumination technique described in section 4.4.1. The flash is applied after a short delay time ($t_d$ of 1 sec). This process yields trapped charge densities of considerably greater magnitude than when a freshly annealed sample is subjected to a single charge-discharge cycle of $t_g$=$t_d$=1 second. The annealing out of this "pulse-enhancement" phenomenon is explored by varying the annealing time. Such a procedure allows "annealing curves" to be generated from which an annealing time constant may be determined (the time at which the charge detected by the above procedure ($t_d$=$t_g$=1sec) has fallen to 1/*e* of its initial value). By varying the temperature, the annealing activation energy and associated attempt to escape pre-factor may be determined from a plot of annealing time constant versus inverse temperature. However at these high temperatures, even after a short delay time $t_d$, much of the charge within the sample has been thermally released. Therefore, an extrapolation procedure has to be used to compensate for this effect. This procedure calculates the fraction of charge removed from the trapping states during the delay time and therefore allows the amount of charge trapped in the sample at $t_d$=0 seconds to be determined. The fit is very

sensitive at high temperatures (to small changes in central energy depth and distribution of the trapping centres shifting the trapped charge scale quite dramatically) but does not influence the shape of the annealing curves. Therefore, since it does not affect the measurement of the time constant it does not influence the calculation of the annealing activation energy.

### 4.4.3 Transfer Characteristics.

The computer system described in section 4.5.2 is used to conduct these measurements. The threshold voltage $V_t$ is obtained from a linear plot of source-drain current against gate voltage. For all measurements, the source-drain voltage is fixed at $V_{sd}$= 0.25V and the temperature at room temperature.

## 4.5 Measurement Systems.

### 4.5.1 Dundee College of Technology.

The experimental set-up is shown schematically in figures 4-4 and 4-5. The

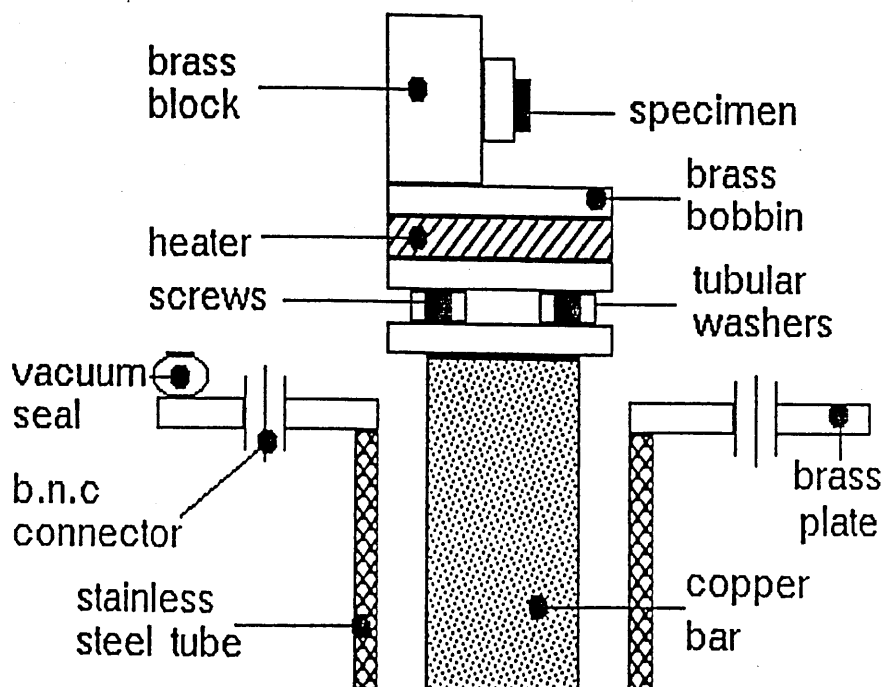



**Figure 4-4 :** Sample Holder

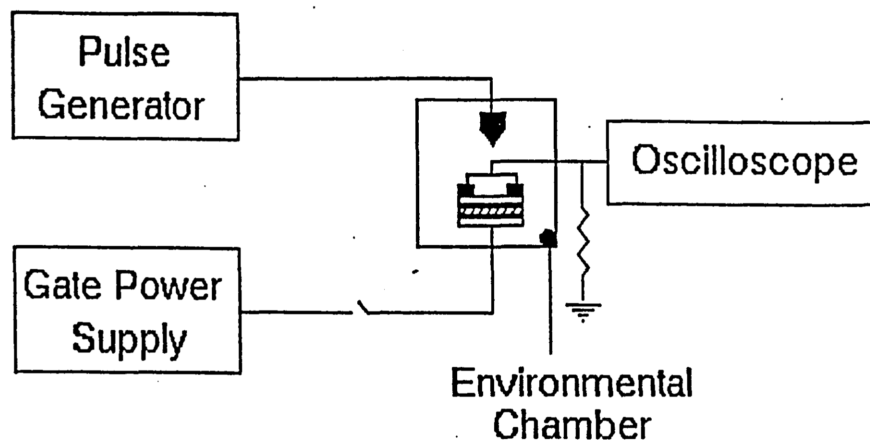



**Figure 4-5 :** Measurement system used at Dundee College of Technology

sample is mounted upon a brass block (to which appropriate electrical connections are made), connected to a cold finger and heater and placed in a vacuum chamber (figure 4-5). Illumination of the sample occurs via a light emitting diode (Stanley type ESPY5501) connected to a light pipe which is inserted into the chamber via a vacuum tight connector. The voltage pulses to the LED are produced by a Lyons PG2 pulse generator (typical pulse widths ~ 150ms). This system provides photon fluxes of ~ $10^{16}cm^{-2}s^{-1}$. The LEDs are calibrated by placing a thermopile at the end of the light pipe such that it acts as the equivalent of the optical plane of the sample. The temperature is sensed using a platinum resistance thermometer, placed inside the brass block (sample holder), and connected to an Oxford Instruments Temperature Controller. The temperature was varied between 150K and 550K. To reduce thermal leakage, the electrical connections to the TFT sample are made with silver DAG suspension on thin (60µm) aluminium wires. The gate connection of the TFT is linked to a Fluke 415B HT power supply (when required, drain voltages are supplied by a Farnell stabilised power supply). The discharge current transients obtained under illumination, are recorded on a Telequipment DM63 storage oscilloscope.

### 4.5.2 Philips Research Laboratories.

The experimental set-up is shown schematically in figure 4-6. There are a few differences between this system and the one described in section 4.5.1. The system, including power supplies, temperature control equipment and LEDs, is wholly computerised. The sample is mounted on a heated substrate within a light tight box. Electrical contacts to the sample are made using micro-probes. Additionally the system is not evacuated and studies below room temperature are precluded. Measurements of the transfer characteristics or the discharge process were conducted by connecting the appropriate switches - S2 and S3 for the discharge measurement and S1 and S4 for the transfer characteristics.

The system controller, a Zilog Z-80 microcomputer, commands power supplies, electrometers and picoammeters through multiple ADC/DAC input/output ports. Currents (for the transfer characteristics) are measured via a Keithley 612 picoammeter while charge is measured via a Keithley 616 electrometer working in the charge collection mode. The LED is driven directly from the computer. The controlling software was written jointly by the author and D.H Nicholls.

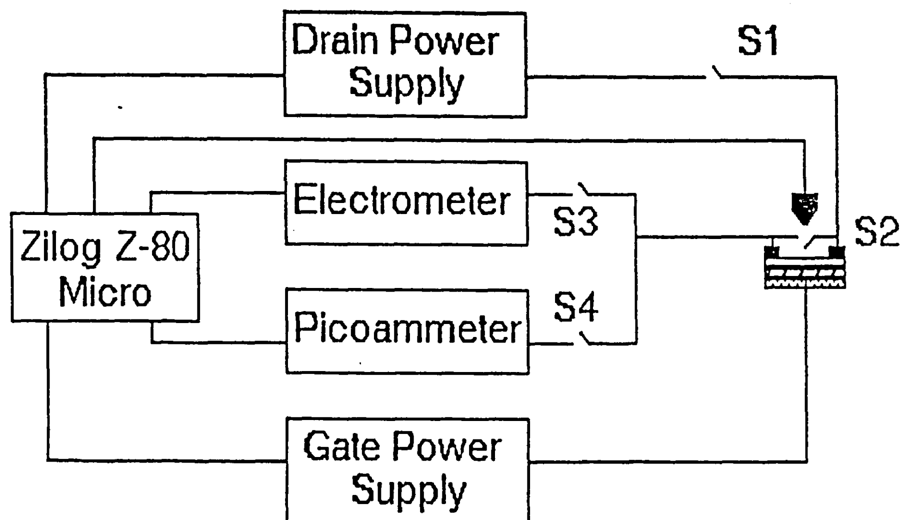



**Figure 4-6 :** Experimental measurement system used at Philips Research Laboratories

# CHAPTER 5
# EXPERIMENTAL RESULTS.

## 5.1 Introduction

In this chapter, the various experimental results are reported. This includes the measurements conducted to characterise the experimental method and to clarify the processes occurring under the experimental conditions. For measurements on samples labelled MSC, P4482, P526 and P527 a gate voltage of 10V was applied, while for samples P2301 and P530 30V was applied. Sample P530 was studied with the modified experimental technique described in the latter stages of section 4.4.1. Some samples were investigated twice - before and after resting for 2 years on the laboratory bench.

## 5.2 Characterisation of the Experimental Technique.

The characterisation procedure involved investigating the influence of various experimental parameters upon the magnitude of the charge detected by the discharge technique. It was necessary to determine if all the charge was being neutralised by the light pulse and also to determine how charge was being neutralised under illumination. Additionally, it was important to determine whether the application of different gate voltages led to the probing of charge trapped in different locations, either spatially or energetically. It is virtually certain that if these characteriation studies were to be repeated on the higher quality samples now available different effects would be observed. Specifically, the effect of applied gate voltage on the discharge transient would be more significant (section 6.5)

a) Illumination Intensity. By varying the illumination intensity, it is possible to identify the total flux required to produce a complete discharge of the device.

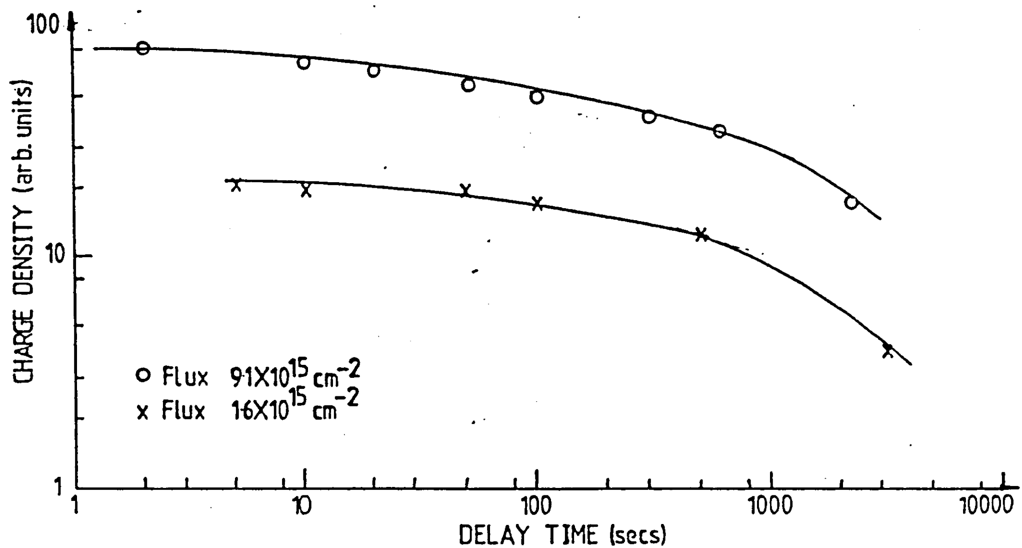



**Figure 5-1** Effect of illumination intensity upon the discharge transient

This is an important procedure, since an underestimation of the required flux would result in the excess trapped charge being underestimated (see below). The influence of illumination intensity on the discharge transient is shown in figure 5-1. It is seen that the discharge time constant remains essentially unchanged (for a given temperature) while the total charge detected varies over a wide range. By inspection it is found that a complete discharge is obtained for illumination pulses of flux ~ $10^{16}cm^{-2}s^{-1}$ and duration ~ 150ms.

b) Illumination Wavelength. By varying the illumination wavelength it is possible to elucidate the photo-discharge mechanism. As mentioned in section 4.4.1,

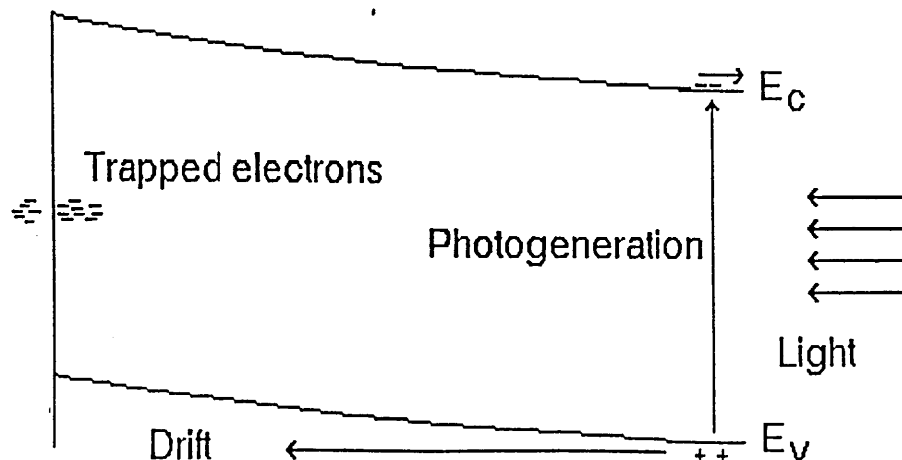



**Figure 5-2 :** Physical processes occurring during the photodischarge

illumination occurs via the free surface, rather than through the silicon/silicon nitride interface. Provided that the photon energy exceeds the optical gap, variation of the wavelength (and thus the absorption depth) has little effect on the magnitude of the charge detected. However, at sub-band-gap energies, the magnitude of the trapped charge detected by this technique approaches zero. Thus, internal photoemission can be ruled out as the process responsible for the discharge under illumination. Rather, it is thought that a process akin to xerographic photo-discharge is occurring (figure 5-2). During application of the positive gate voltage, electrons become trapped in states close to the interface. Subsequent illumination causes generation of excess carriers within the α-Si:H layer, and the re-distribution of these to neutralise the residual trapped charge gives rise to the observed discharge current transient.

c) Variation of Gate Voltage. It can be seen that the time constant of the dark discharge curves is unaffected (at any given temperature) by changes in gate voltage (figure 5-3). When these results were obtained, it was thought that the technique identified only one dark discharge process. However, measurements on subsequent samples of varying qualities revealed that more than one process was occurring - see below.

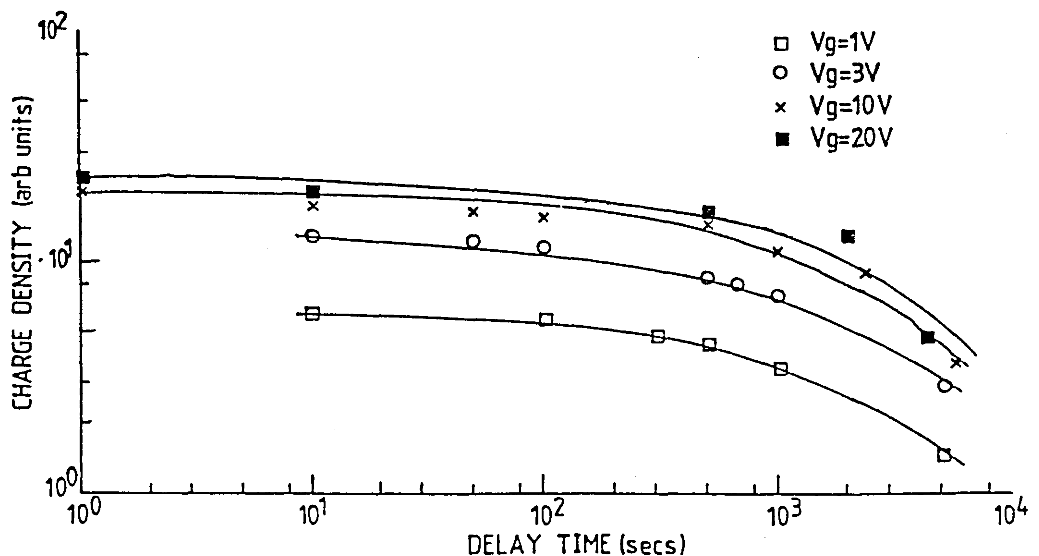



**Figure 5-3 :** Influence of applied gate voltage on the dark discharge transient.

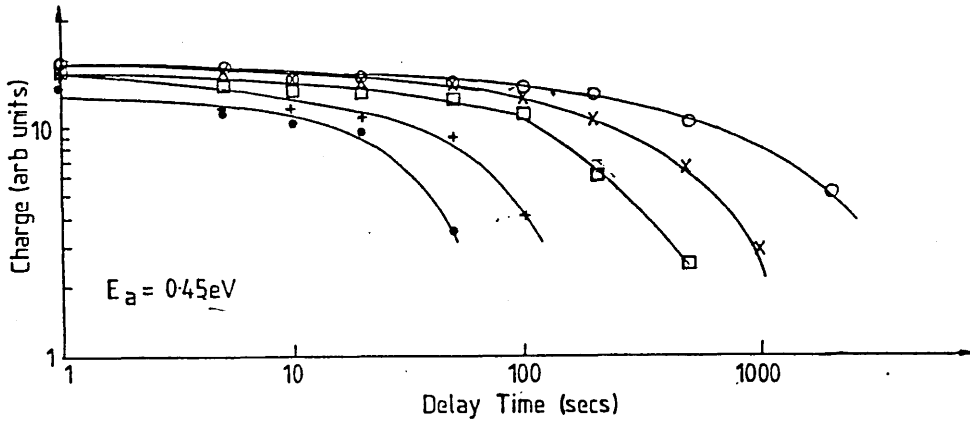
| Sample Number | Centre Activation Energy(eV) | Standard Deviation of Distribution(eV) | Attempt-to-Escape Pre-factor(Hz) |
|---|---|---|---|
| P3342 (a) | 0.8+/-0.1 | - | $10^{12}$ |
| (b) | 0.45+/-0.05 | 0.1+/-0.02 | $10^{6}$ |
| P4482 (a) | 0.85+/-0.05 | 0.08+/-0.02 | $10^{12}$ |
| (b) | 0.45+/-0.05 | 0.1+/-0.02 | $10^{6}$ |
| P526 | 0.45+/-0/05 | 0.1+/-0.02 | $10^{6}$ |
| P527 | 0.45+/-0.05 | 0.1+/-0.02 | $10^{6}$ |
| P2301 | 0.8+/-0.1 | - | $10^{12}$ |
| P530 (1) | 0.45+/-0.05 | 0.1+/-0.02 | $10^{5}$-$10^{7}$ |
| (2) | 0.75+/-0.05 | 0.1+/-0.02 | $10^{9}$-$10^{11}$ |

**Table 5-1 :** Sample by sample experimental results. Results denoted (a) and (b) represent respectively activation energies before and after resting on the laboratory bench for ~ 2 years. (1) and (2) refer to the short and long time components of the dark discharge in figure 5-4(c)

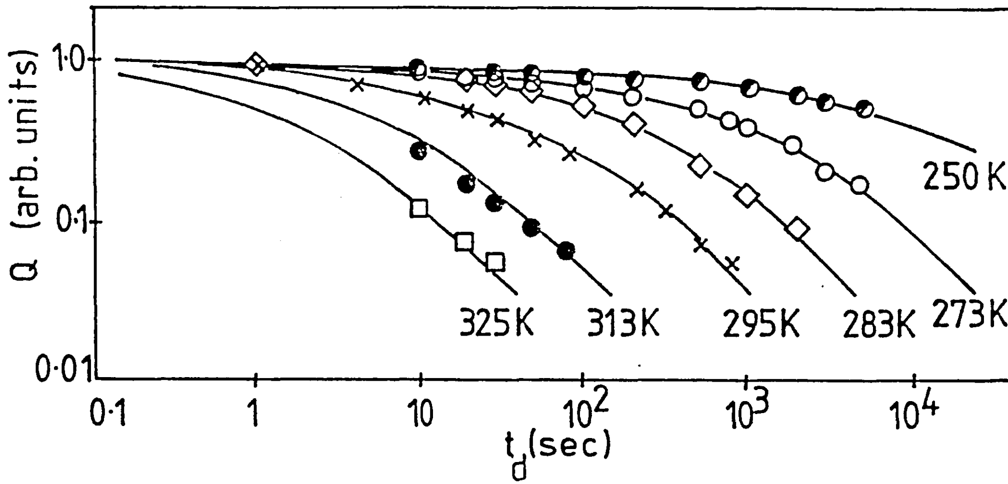
## 5.3 Discharge Measurements.

This section reports on the dark discharge characteristics of the different samples. By analysing the discharge curves it is possible to identify the energetic depth and distribution of the centre(s) involved in the dark discharge mechanism(s) and the associated attempt to escape pre-factor(s). The discharge curves, in all cases exhibit non-exponential features, and thus require the use of a fitting procedure to determine the time constant (section 4.4.1). Typical discharge curves obtained in this study are shown in figure 5-4. The fit of the experimental data to computer generated release curves, is shown in figure 5-5 for the discharge curves in figure 5-4(b). Figure 5-4(a) and (b) show curves due to a single dark discharge process :- (a) characteristic of a process with an activation energy of 0.45+/-0.05eV, attempt-to-escape pre-factor of $10^{5}$-$10^{6}$Hz, which occurs via a set of centres of standard deviation 0.08+/-0.02eV; (b) represents a process which occurs through a set of centres 0.8eV+/-0.1eV from the conduction band edge with a standard deviation of 0.08 +/- 0.02eV and an associated attempt-to-escape pre-factor of $10^{9}$-$10^{13}$Hz; (c) these curves (measured on sample P530) reveal the two components described above, and

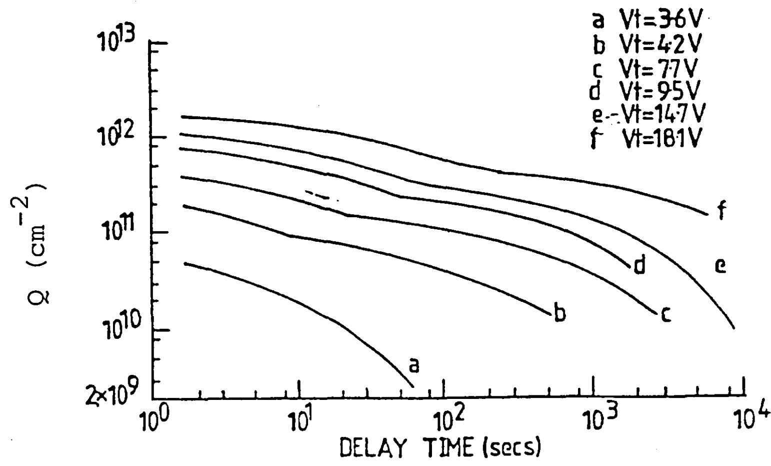
**Figure 5-4 :** Typical discharge curves observed in this study.




(a)




(b)




(c)

the two components described above, and shows that they can and do occur together - the first component has an activation energy of ~ 0.4eV while the second has an activation energy of ~ 0.75eV.

It should be noted that when a single low activation energy is observed the magnitude of the excess trapped charge is also low, while the larger activation energy is associated with a significantly larger trapped charge magnitude. Additionally, it is found that a relationship exists between the characteristic time of the first component and the magnitude of the total trapped charge - section 6.4.

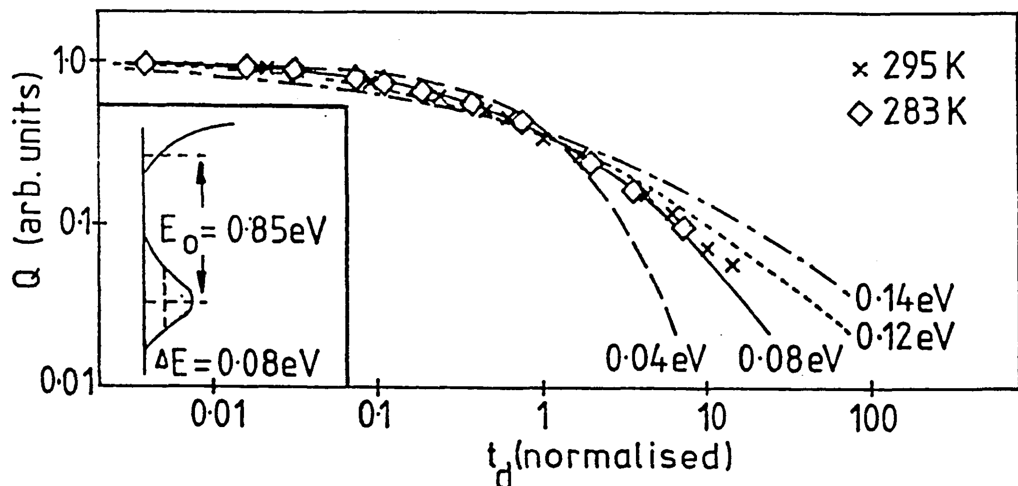



**Figure 5-5** Fit of the experimental data to computer generated curves for thermal release from a Gaussian distribution of states

## 5.3.1 Summary of the Discharge Results.

The dark discharge behaviour of a TFT is characterised by the following :-

1. The dark discharge involves two thermally activated components.
2. One component has an activation energy of 0.8+/-0.1eV and attempt to escape pre-factor of $10^{9}$-$10^{13}$Hz, the other an activation energy of 0.45+/-0.05eV and attempt to escape pre-factor $10^{5}$-$10^{6}$Hz.
3. Low values for the magnitude of the total trapped charge are associated with a dark discharge process occurring through a set of states centred

0.45eV from $E_c$. Larger magnitudes of trapped charge are associated with a dark neutralisation process with a larger central activation energy (~0.8eV) or with both processes occurring simultaneously.

4. Where both components are observed, the time constant of the first component is found to vary with the magnitude of the trapped charge density.

## 5.4 The Influence of Bias Stress upon the Dark Discharge of a TFT.

This section describes how bias stress affects both the magnitude of the charge detected by the discharge technique and the characteristics of the discharge curves (ie activation energy and attempt-to-escape pre-factor). Measurements of the threshold voltage shift provide an independent assessment of the influence of bias stress upon the magnitude of the excess trapped charge. By conducting the two measurements in parallel it is possible to compare the magnitude of the charge detected by the two techniques.

The total charge detected and the threshold voltage increase simultaneously as

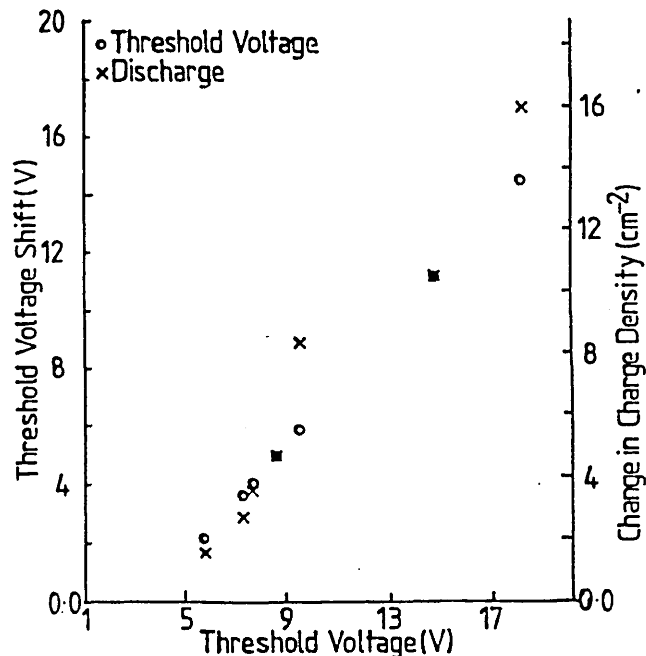



**Figure 5.6 :** Comparison of detected charge density and shift in threshold voltage as a function of bias stress

effects are shown in figure 5.6. As can be seen there is a direct relation between the threshold voltage shift and the change in trapped charge density. The two quantities are related via the experimentally determined device capacitance. Therefore, it is established that the discharge technique provides a sensitive and valid measure of the charge responsible for the observed threshold voltage shift.

In figure 5-4(c) it is seen that the nature of the discharge changes as the device is stressed. Prior to measurements on P530 only one component had been observed during the dark discharge (at any one time). However, these results show that the discharge is characterised by two thermally activated components occurring simultaneously. The activation energies of the different components were measured as a function of threshold voltage (stress). However, despite a wide variation in threshold voltage (4.5V $< V_t <$ 18.1V), the activation energies of the two components of the discharge remain approximately constant.

## 5.5 Annealing Measurements.

These measurements were conducted at Dundee using the procedure described in section 4.5.2. They reveal that the annealing process is also thermally activated. Typical annealing results are shown in figure 5-7. The curves are again not representative of a single exponential, but are characteristic of the annealing process occurring via a distribution of centres. The sample by sample results are shown in table 5-2. From this table it is possible to infer that there are two annealing activation energies one ~ 1.5eV with an attempt to escape pre-factor of ~ $10^{15}$Hz and the other ~ 0.85eV and attempt to escape pre-factor ~ $10^{12}$Hz. It is interesting to note that the larger annealing activation

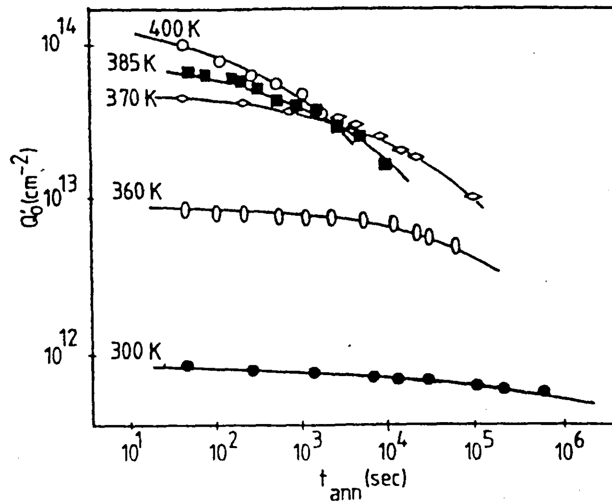



**Figure 5-7 :** Typical annealing curves

| Sample Number | Activation Energy (eV) | Attempt-to-escape Pre-factor (Hz) |
|---|---|---|
| P4482 | 1.5+/-0.1 | $10^{15}$ |
| P3342 | 1.6+/-0.1 | $10^{16}$ |
| P526 | 0.85+/-0.1 | $10^{12}$ |

**Table 5-2 :** Sample by sample annealing results

energy was observed on samples with a dark discharge activation energy centred ~ 0.8eV from $E_C$, while the lower annealing activation energy was found for the sample with a dark discharge activation energy of 0.45eV.

Comment : In the process of conducting the measurements on stressing at Philips Research labs. it was noticed that the threshold voltage shifts could be completely removed through reverse bias annealing. This was an unexpected observation, since the measurements at Dundee had suggested that the annealing process (and thus the removal of the threshold voltage shift) was a thermally activated process - see section 6.5.

# CHAPTER 6

# DISCUSSION OF THE EXPERIMENTAL RESULTS.

## 6.1 Introduction

From chapter 5 it is clear that two distinct processes occurring under dark conditions contribute towards the neutralisation of excess trapped charge within a TFT. By identifying the neutralisation processes occurring during the dark discharge, it is possible to obtain information concerning the spatial and energetic location of this excess charge and thereby the TFT instability mechanisms. This chapter begins with a presentation of a consistent model for charge trapping instabilities within a TFT. Subsequently, the dark neutralisation processes occurring under the experimental conditions are discussed within the model framework and the various experimental results reconciled.

## 6.2 Model of Charge Trapping Instabilities in α-Si:H/SiN:H TFTs.

It is proposed that there are two processes responsible for the threshold voltage shift in a TFT :-

- creation of metastable silicon dangling bonds
- charge injection into the insulating layer

### (a) Creation of Metastable Silicon Dangling Bonds.

Street[17,18] proposed that free carrier trapping could induce metastable silicon dangling bonds **during film growth**. Herein, it is proposed that in **any** situation in which the band tail state occupation is significantly increased (ie during film growth, by illumination, electron/hole injection,accumulation) metastable state creation will occur. When the occupation of the conduction band tail is increased

via formation of an electron accumulation layer, a silicon atom just below $E_f$ will have five electrons and thus will constitute an unstable configuration. This situation can be resolved via the formation of dangling bond defects:

$$2Si^0_4 + 2e^- \longrightarrow 2Si^-_3 \qquad (6.1)$$

The energetics of the above reaction have been calculated recently by Stutzmann[20]. He has shown that the energy of a doubly occupied conduction band tail state is equivalent to that of two negatively charged dangling bond states. An additional driving force for the reaction comes from the coulombic repulsion energy of the two electrons localised on the same defect. However, it is difficult to envisage why a large activation energy should be required to reform the broken Si-Si bond upon elimination of the excess electrons, in this case when the device is discharged. The total bond breaking reaction is likely to be more complex than the above, possibly including hydrogen bond switching (section 2.9.1, figure 2-6) and the presence of impurity atoms. Indeed, it has been shown that the hydrogen diffusion energy is ~ 1.5eV[71] similar to that measured for the annealing of the Staebler-Wronski effect[42] (and herein for the annealing activation energy).

**(b) Charge Injection into the Insulating layer.**

It is proposed that charge is injected into silicon dangling bonds within the nitride layer directly from the amorphous silicon conduction band. Given the high injection efficiency[50] observed in amorphous silicon structures, the re-distribution of charge within the nitride limits the rate of threshold voltage shift[7]. Assuming that conduction (in the nitride) occurs by hopping close to the Fermi level[7,51], the nitride mid-gap defect density (and therefore material quality) will influence the rate of stressing. Additionally, the applied voltage may influence

the rate of stressing, if the field is great enough to induce field-enhanced conduction or (at larger voltages) Poole-Frenkel conduction.

## 6.3 Electron Trapping Centres and Dark Discharge Mechanisms.

When a positive voltage is applied to the gate of a TFT, electrons attracted to the interface may become trapped in :-

1. Silicon dangling bonds within the nitride through charge injection
2. Silicon dangling bonds within the $\alpha$-Si:H

The discharge experiment measures the total charge trapped within a TFT at any given time. This allows the dark neutralisation of the excess trapped charge to be monitored. This neutralisation may occur via :-

1. Tunneling from states in the nitride to the interface, followed by thermal release to the $\alpha$-Si:H conduction band edge
2. Creation of a space charge layer of the opposite polarity (Xerographic Depletion Discharge).
3. Thermal release of electrons trapped in localised states close to or at the interface.

Wherever the charge is trapped, it can be neutralised either by the mechanism of electron release from slow states (before or after a tunnelling event) or via the accumulation of positive space charge within the $\alpha$-Si:H as the device is swept into depletion. These processes have characteristics as described below.

### (a) Tunnelling From States within the Nitride.

It has been suggested[52,53,67] that results previously reported from this study[57] (in particular, the 0.85eV activation energy of the dark discharge behaviour) are representative of charge emission from the nitride - process shown schematically in figure 6-1. Trapping into the nitride is a very slow process in device quality material and, therefore, the consequent shift in $V_t$ would occur over an extended stressing period. Significantly, threshold voltage measurements performed immediately before and after a discharge measurement return the same value for $V_t$, despite the fact that the charge responsible for the threshold voltage is completely neutralised during the discharge measurement. Therefore, since no extended stressing occurs between the discharge measurement and the determination of $V_t$, ***charge is not emitted from the nitride during the discharge process.***

Additionally, reproducible discharge curves are obtained without any stressing between measurements - a feature which would not be observed if the discharge curves were representative of charge emission from the nitride. If the discharge curves did represent charge removal from the nitride, then consecutive measurements of complete dark discharge curves would detect significantly different magnitudes of trapped charge. Therefore, it is concluded that the charge movement detected during the dark discharge is limited to processes occurring with the α-Si:H active layer. However, charge trapping into

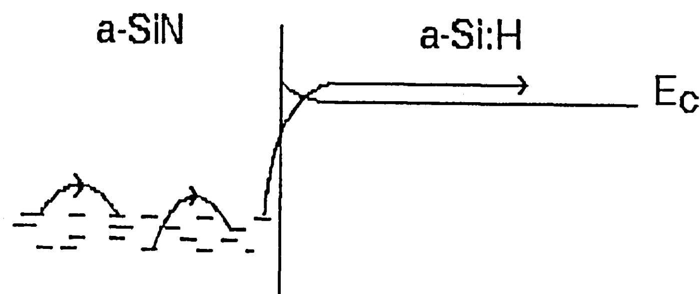



**Figure 6.1 :** A process by which charge emission may occur from the nitride

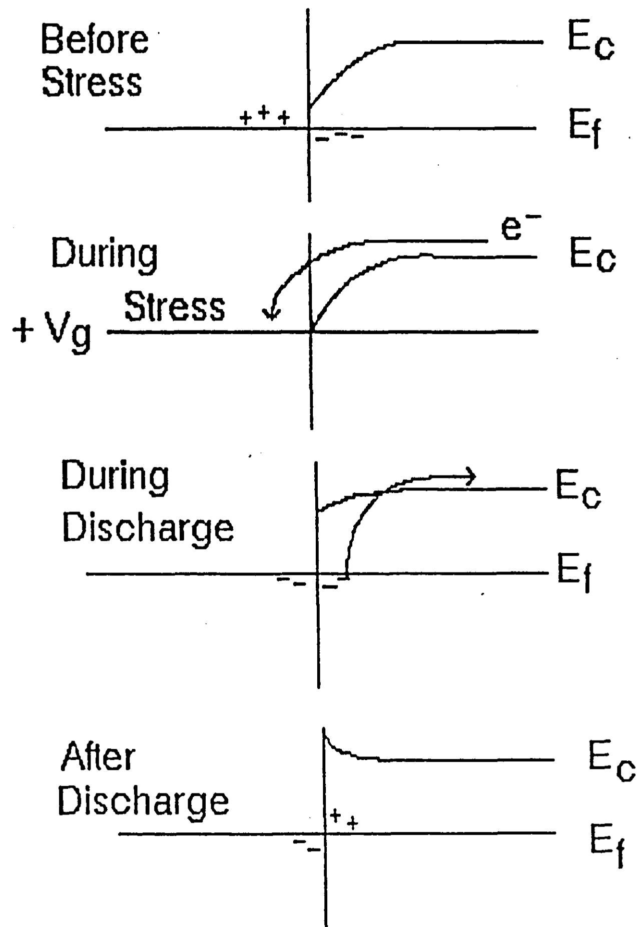



**Figure 6.2 :** Figures showing the band bending profiles and how they relate to the xerographic depletion discharge mechanism.

the nitride layer can still occur, in which case neutralisation of the trapped charge is via the establishment of a space charge layer in the α-Si:H as discussed below.

<u>(b) Characteristics of a Xerographic Depletion Discharge Model</u>

The discharge experiment detects charge movement within the α-Si:H layer resulting from the removal of the applied field. If the effect of the applied field is simply to change the occupancy of states within the α-Si:H layer, then the dark discharge measurement monitors the thermalisation of the electron quasi-fermi level to its equilibrium position. This thermalisation process may be dominated by a given set of states if significant structure exists (see (c) below). However, if charge becomes trapped in slow states within the nitride, then the removal of

the applied field effectively results in the application of a smaller field of the opposite polarity. This results in the reduction or inversion of the space charge layer which naturally occurs at the α-Si:H/SiN:H interface[54,61,62,66](figure 6-2). The characteristics of such a process may be described by a model based on the xerographic depletion discharge process.

Xerographic depletion discharge[70] is a process by which space charge accumulates via carrier emission from deep centres. For such a process a characteristic neutralisation time can be defined; the value being dependent upon the *magnitude* of the charge in the surface or interfacial layer, and upon the energetic depth of the centres from which charge generation is occurring.

The depletion discharge model describes a dark discharge in which only one sign of thermally generated carrier is mobile on the time scale of the experiment. As thermal generation and sweepout of the mobile carrier proceeds, the bulk develops deeply trapped space charge of the opposite sign. A characteristic time for the generation of bulk space charge can be defined as follows. Let $\rho(t)$ be the bulk charge density, R is the release co-efficient, $N_0$ the density of centres from which the charge is generated and n the number of free carriers, then

$$\rho(t) = en = eN_0[1-\exp(-Rt)] \qquad (6.2)$$

where

$$R = \nu\exp(-E/kT) \qquad (6.3)$$

then if $\rho(t) < eN_0$ and $Rt < 1$

$$\rho(t) \sim e\,N_0Rt \qquad (6.4)$$

then, by substitution of equation 6.3 into equation 6.4

$$\rho(t) = eN_o t\nu\exp(-E/kT) \qquad (6.5)$$

The time at which this reaches any given fraction (say 1/2) of the trapped charge at the interface $Q_o$, then may be calculated from

$$Q_o/2AL = t_{1/2} eN_o\nu\exp(-E/kT) \qquad (6.6)$$

Thus

$$t_{1/2} = Q_o\exp(E/kT)/2N_oALe\nu \qquad (6.7)$$

Thus the time for neutralisation of any given fraction of the surface charge, via a process involving generation from bulk centres, depends upon the magnitude of this surface charge as well as the energetic depth of the centres through which charge generation is occurring. Therefore, if charge trapping into the nitride does occur, it would be expected that the characteristic time would depend upon both the energetic depth of the centres through which the depletion discharge is occurring and on the magnitude of the charge in the nitride. Additionally, it would be expected that the gradient of a graph of $Q_o$ vs $t_{1/2}$ would have a value similar to that given by the experimentally determined attempt-to-escape pre-factor and energy depth and a reasonable value for the density of states at this level.

### (c) Characteristics of a Thermal Release Process

Thermal release from a distribution of states (such as silicon dangling bonds) may be characterised by a function of form

$$Q(t) = Q_0 \int \frac{N(E)}{N_t} \exp\left[\frac{-t}{\tau(E,T)}\right] dE \qquad (6.8)$$

where Q(t) is the charge remaining as a function of time, $Q_o$ is the total charge trapped in these centres by the gate voltage, $\tau(E,T) = \nu^{-1}\exp(E/kT)$ and $N_t = \int N(E)dE$. If the DOS is highly structured then the decay of the charge will have corresponding features. On the other hand a featureless DOS will render a featureless decay curve.

If the charge trapping instabilities are due to creation of metastable silicon dangling bonds within the α-Si:H layer, then it would be expected that the discharge curves would be dominated by release from these states. Such release curves would return information on the depth, profile and distribution of the dominant centres. Johnson and Beigelsen[24] have performed a study in which capacitance and ESR measurements are carried out during the photodepopulation of deep states. The measurements allow an identification of silicon dangling bond states located 0.8-0.9eV below the conduction band mobility edge, and broadened into a Gaussian distribution with standard deviation ~ 0.12eV. Therefore, if metastable state creation is occurring, it would be expected that the release curves would return similar values.

Further evidence in support of the above model comes from studies with a "defect-free" $SiO_2$ insulator. Similar charge trapping instabilities are observed and must be related to processes occurring within the active layer.

## 6.4 Interpretation of the Experimental Results.

In the above sections a model has been presented in which charge can become trapped in created metastable silicon dangling bonds or may be injected into the nitride. For both processes the characteristics of a neutralisation process have been detailed - for charge trapping into the nitride a xerographic depletion

discharge is expected, whereas for metastable state creation, charge is neutralised via a thermal release process. Below the experimental results are compared to the proposed model.

The neutralisation of the excess charge is characterised by processes occurring through distributions of states centred either 0.45eV($E_x$) or 0.85eV($E_{db}$) from $E_c$. Measurements on sample P4482 show a significant change in the magnitude of the total trapped charge $Q_0$ as the applied voltage is varied (section 5.2, figure 5-3). Despite this variation, the time constant of the dark discharge remains essentially unchanged. Since this is not as expected from equation 6.7, it is concluded that a xerographic depletion discharge type process does not occur. Bearing this in mind, it is unlikely that significant quantities of charge are injected into the nitride. The discharge curves for this sample could be modelled using a simple thermal release process from a distributed set of states centred ~ 0.85eV from the conduction band edge with a gaussian profile and standard deviation of ~ 0.08eV. Additionally, continued stressing of the device leads to an increase in trapped charge at this level. This may be annealed with an activation energy of ~ 1.5eV. If stressing induces the formation of excess dangling bonds, it would be expected that the annealing process would have an

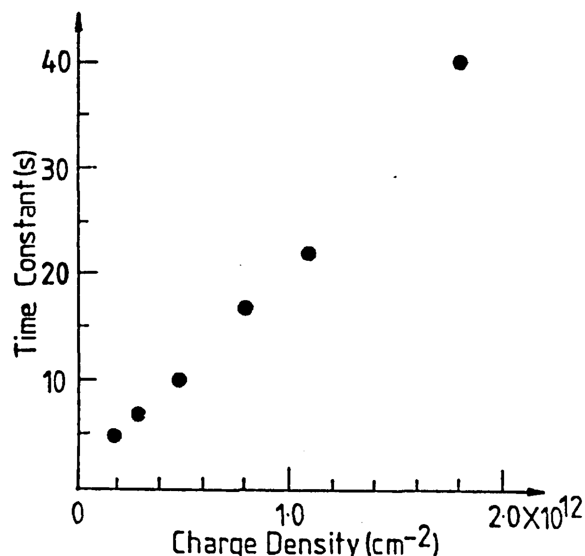



**Figure 6-3 :** Variation of characteristic time (of the short time component) with initial trapped charge density (sample P530)

activation energy similar to those observed for the Staebler Wronski effect. Since these energies are similar to what would be expected for silicon dangling bonds, it is concluded that the charge trapping instabilities in this sample are due to metastable changes in the number of silicon dangling bonds.

However, similar measurements on sample P530 reveal a significant difference in behaviour. The discharge is more complicated and includes two components figure 5-4(c). As the magnitude of the trapped charge increases the characteristic time of the shorter time component is found to increase. This is shown in figure 6-3, from which it can be seen quite clearly that a linear relationship exists between the characteristic time and the magnitude of the total trapped charge, $Q_o$. Additionally, the maximum charge detected corresponds to a volume density of states of ~ $10^{18}cm^{-3}eV^{-1}$ (similar to that detected in field effect studies[15] close to this energy level). Finally, comparing the gradient of an experimentally obtained graph of $Q_o$ vs $t_{1/2}$ (figure 6-3) with a value calculated using model parameters (E~0.45eV, T~300K, $N_o$~$10^{17}cm^{-3}$, v~$10^6$Hz, with a sample volume of 3 X $10^{-6}cm^{-3}$) renders a gradient different by less than a factor of 2. By fine tuning the parameters (ie changing $N_o$ by a factor of 2 or 3) an exact fit may be obtained. Such observations are consistent with the postulate that a xerographic depletion discharge is occuring and, by inference, that charge is trapped within the nitride layer.

The time constant of the slower component of sample P530 does not show a dependence on $Q_o$. As the magnitude of the total trapped charge increases, the time constant of the dark discharge is found to remain essentially unchanged. This component has the characteristics of a thermal release process from a distributed set of states deep within the energy gap, very similar to that of sample P4482. Since this component is also found to increase in magnitude with device stressing, it is concluded that metastable state creation is also occurring, but at a slower rate than the injection into the nitride.

The reverse bias and thermal annealing of the second component may also be explained within this framework. Using the model of the silicon/silicon nitride interface presented at the end of chapter 3, it is seen that the deep traps in the amorphous silicon and the silicon nitride are at approximately the same energy. Therefore a reverse bias would remove electrons from the nitride via a hopping process to localised silicon dangling bond states within the active layer but close to the interface. The annealing activation energy would then represent release of electrons from silicon dangling bond states close to the interface to the α-Si:H conduction band. Such a process would be expected to have an activation energy ~ 0.8eV but would also be influenced by the application of an applied voltage. In practice, reverse bias annealing was found to be successful in those cases where the dark discharge was dominated by release processes through $E_X$. Additionally, thermal annealing with an activation energy of 0.8eV was found on a sample whose dark discharge characteristics were consistent with insulator trapping.

Unfortunately, measurements of time constants and activation energies as a function of stress were not conducted on other samples. The dark discharge of samples P526 and P527 is characterised by an activation energy of ~ 0.45eV.

## 6.5 The Influence of Experimental and Materials Parameters.

Within the framework described in some detail in the previous sections, it is possible to identify some experimental and materials parameters which influence the relative contributions of the two instability mechanisms to the dark discharge behaviour and the threshold voltage shift.

When the dark discharge is solely controlled by release through states centred at $E_X$, the magnitude of the total trapped charge, $Q_o$, is low. This suggests that the threshold voltage is low and that the Fermi level at the interface lies close to

the conduction band edge, possibly within a distribution of states centred at $E_x$. Changes in occupancy of these states induced by an applied voltage would result in the dark discharge being dominated by release from states at $E_x$ as the electron Fermi level thermalises to its equilibrium position (assuming no larger features in the DOS distribution). The origin of these states is presently unclear. Field effect measurements, with a wide variety of different gate insulators have been interpreted as having a maximum close to $E_x$. This suggests that the states at $E_x$ are not impurity related but are in fact bulk silicon defects. However, there is very little evidence from other measurements for a bulk density of states feature close to $E_x$. Further work is required to identify the origin of the centre 0.45eV from $E_c$.

If the device has a large intrinsic density of dangling bonds within the $\alpha$-Si:H layer, then the Fermi level will lie in the middle of the gap and the discharge behaviour will be dominated by release processes from states at $E_{db}$. It is not necessary to assume that states shallower than $E_{db}$ do not exist, only that they are smaller in number.

Sample P530 reveals both components. A possible solution has recently been suggested in a paper by the Philips group[72]. They studied the influence of the magnitude of the applied gate voltage upon the rate of device stressing and found that the latter remains essentially constant until the applied voltage reaches ~ 30V whence the stressing rate increases significantly (for a sample of similar quality to P530). They suggest that above 30V the stressing process is dominated by charge injection into the nitride, whereas below 30V metastable state creation dominates. By relating these data to those for curve f in figure 5-4(c), it would be expected that charge trapping into the insulating layer would be responsible for ~ 75% of the observed threshold voltage shift. The ratio of the two components in the discharge is of approximately this value. Therefore, it is proposed that the dual nature of the discharge of sample P530 results directly

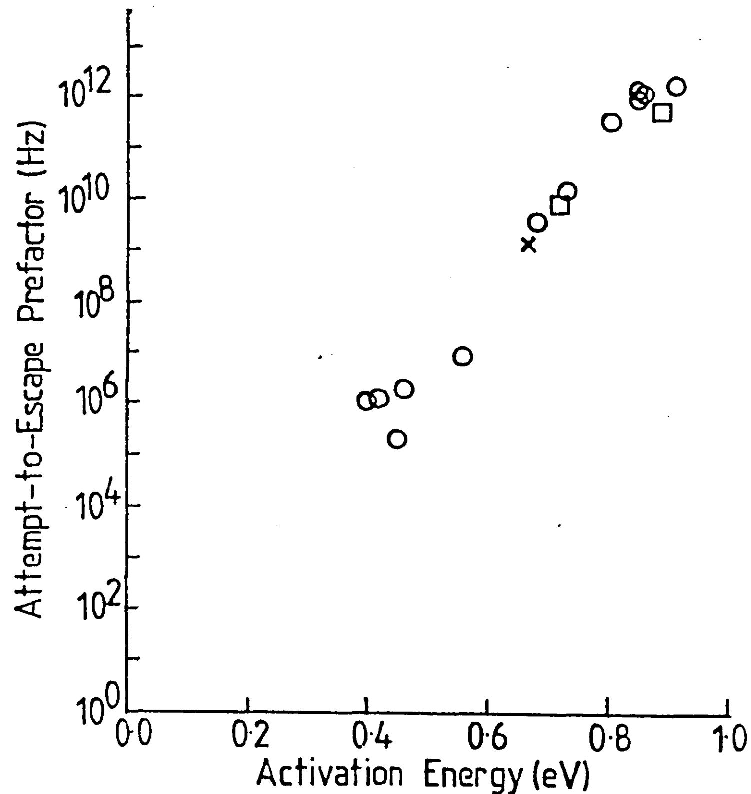



**Figure 6-4 :** Meyer-Neldel behaviour, including data from other experiments

from the stressing conditions. As was mentioned earlier, sample P530 was the only device stressed at larger gate voltages. Therefore, such dual behaviour would not necessarily be witnessed on other devices.

## 6.6 Meyer-Neldel behaviour.

A Meyer-Neldel type behaviour occurs between the attempt-to-escape pre-factor and the discharge activation energy. A plot of the experimental results is shown in figure 6-4 (o). Also plotted are the data of Street et al[52,53](x) for their measurements on the slow component of the discharge of silicon/silicon nitride structures and xerographic data of Imagawa et al[73](open square). It can be seen that all of these data exhibit a consistent pattern. At present the reason for this is not clear.

## 6.7 Summary.

In the above sections, the possible electron trapping centres and neutralising processes have been described in some detail. The study has revealed that the charge trapping effects observed under positive bias stress result from electron trapping into :-

- silicon dangling bond states within the nitride
- metastable silicon dangling bond states within the active layer

Such trapped charge is neutralised by two distinct processes :-

- xerographic depletion discharge through states centred at $E_x$ within the $\alpha$-Si:H
- thermal release from the occupied trapping centres ( either at $E_x$ or at $E_{db}$)

The relative contributions of the two instability mechanisms to the observed threshold voltage shift depend upon both the deposition conditions and the conditions under which the device is stressed. It is suggested that at larger gate voltages a greater fraction of charge is injected into the insulating layer and that under these conditions the threshold voltage shift is dominated by such a process. At lower applied voltages a smaller fraction of charge is injected and the charge trapping instability is dominated by metastable state creation within the $\alpha$-Si:H layer.

# CHAPTER 7
# CONCLUSIONS AND FUTURE DIRECTIONS.

The charge trapping phenomena within amorphous silicon-silicon nitride thin film transistors have been characterised experimentally within an extensive study. A new experimental technique has been developed and extended to allow a wide range of important parameters to be determined. A new TFT instability mechanism, that of single carrier creation of metastable silicon dangling bonds has been identified and the parallel process of charge trapping into the insulating layer has also been observed. The metastable silicon dangling bonds are situated approximately 0.8eV from $E_C$ and have an approximately Gaussian distribution of standard deviation 0.08eV. A shallower set of states within the a-Si:H approximately 0.45eV from $E_C$ has also been identified. However, the origin of these states is not clear. Additionally a Meyer-Neldel relation is found to exist between the release activation energy and the attempt to escape pre-factor - a relation for which no explanation is presently forthcoming.

The consequences of this newly reported TFT instability mechanism are in fact widespread and appear to form a fundamental material limitation. A wide variety of different measurement techniques are now confirming that single carrier trapping does induce metastable state creation not only in TFTs but also in the bulk material. Measurements of the transfer characteristics on ambi-polar TFTs[72] have shown that extended bias stressing increases the amount of charge required to sweep the device from electron accumulation to hole accumulation. Such an observation requires that an increase in the number of trapping centres in communication with the conduction band occurs. Based on results already reported from this study it is suggested[72] that this could result from an increase in the silicon dangling bond density. Capacitance-Voltage measurements[74] on α-Si:H/α-SiN:H structures show that the number of

interfacial states also increases as the capacitor structure is subjected to a continued bias. Again it is proposed that this is due to single carrier creation of silicon dangling bond states. More detailed studies of the doping mechanism[20] have shown that neutral four-fold co-ordinated phosphorus atoms exist in phosphorus doped α-Si:H. Within the confines of the original doping model this was not expected. If silicon dangling bond states are created as a secondary consequence of doping rather than as an integral part of the doping mechanism, it is possible to reconcile this experimental observation. Under these circumstances silicon dangling bonds are again created via the trapping of free carriers in weak band tail states.

A further investigation of α-Si:H TFTs is now underway at Swansea. By studying the conductivity through the interface between the semiconductor and insulator, it should be possible to identify an interface or dielectric which minimises injection processes. However, the creation of metastable states provides a more fundamental limitation, since the material is directly degraded by the presence of the charge carriers. It is hoped to study devices consisting of hydrogenated amorphous silicon layers of different qualities alloyed with impurities to improve the rigidity of the amorphous structure. Any changes which occur in the interfacial state density will be probed using the discharge technique described herein and also with capacitance-voltage techniques. These would monitor the quality and stability of the device. It is also hoped to perform charge sweep-out measurements to identify any shallow states which may exist at the interface.

**Publications.**

The papers detailed below have been presented, published or are in preparation :-

1. "Transient Photoresponse of Amorphous Silicon Thin Film Transistors", Authors A. R. Hepburn, J.M.Marshall, C. Main and M.J. Powell, paper presented at the 1984 Chelsea Meeting on Amorphous and Liquid Semiconductors.
2. "Evidence for Metastable Defects in Amorphous Silicon Thin Film Transistors", Authors A.R. Hepburn, J.M. Marshall, C.Main, M.J.Powell and C. van Berkel; Proceedings of the 11th International Conference on Amorphous and Liquid Semiconductors,Eds. F.Evangelisti and J.Stuke, Journal of Non-Crystalline Solids, Volume 77-78, page 1409, 1985.
3. "Metastable Defects in Amorphous Silicon Thin Film Transistors", Authors A.R. Hepburn, J.M. Marshall, C. Main, M.J. Powell and C. van Berkel, Physics Review Letters, Volume 56, page 2215, 1986.
4. "Charge Trapping Effects in Amorphous Silicon/Silicon Nitride Thin Film Transistors", Authors A.R. Hepburn, J.M. Marshall, C.Main, C. van Berkel and M.J. Powell, Proceedings of the 12th International Conference on Amorphous and Liquid Semiconductors, Eds. M. Matyas, J. Kocka and B. Velicky, Volume 97-98, p903, 1987.
5. "The Origins and Nature of Charge Trapping Phenomena in Amorphous Silicon Silicon Nitride Thin Film Transistors", Authors A.R. Hepburn, J.M. Marshall, C. Main, C. van Berkel and M.J. Powell Manuscript in preparation.

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