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Programmable CubeSat Interface Board to Reduce Costs and Delivery Time

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ABSTRACT

A standardized interface for different CubeSat missions is one of the keys to reduce costs and delivery time. A backplane interface approach, proposed by the University of Wuerzburg in Germany as UWE-3, was implemented in three CubeSat projects at the Kyushu Institute of Technology (Kyutech) in Japan to shorten the development and assembly times. The backplane approach also helped to reduce the risk of workmanship errors associated with the harness. The proposed standard interface board, however, needed changes in every CubeSat project to comply with the mission requirements. To obtain more flexibility especially for data connections, this work introduces a novel idea of a software-configurable bus interface with the backplane board. A Complex Programmable Logic Device (CPLD) was used instead of the hardware routing so that we can reconfigure the bus interface by reprogramming the CPLD. The concept was validated by a functional test with a breadboard module. A radiation test verified that the selected CPLD has enough strength to survive total ionization dozes of more than 2 years in low Earth orbit. A new backplane board with CPLD have been integrated with Engineering Model and Flight Model of the fourth CubeSat project at Kyutech, BIRDS-3 project, and system level verification was conducted. The flight model is now ready for delivery to JAXA in February 2019 for a planned launch to International Space Station in April 2019. The initial on-orbit data will be obtained by the time of the conference in August 2019 and will be presented to the audience.

INTRODUCTION

Reducing costs and delivery times of the CubeSat projects are essential, especially in the university CubeSat projects where the students are playing important roles of the project. To learn entire processes of the space system engineering, students need to experience all the systems engineering process, such as designing, building, testing and operating, with hands-on training in limited time with limited resources. However, this is very challenging because of the general time period of the program in graduate schools, for example for the Master Course, is 2 years. Which means that the entire processes of the CubeSat project need to be completed in less than 2 years to educate students effectively.

On the other hand, reducing the development and assembly times of CubeSat projects are indirectly help to have higher reliability in space after the launch. Because short development time gives more opportunity to test the satellite on the ground. Due to they are often launched as the secondary payload, many pico/nano satellite projects didn't have a right to change the launch schedule. Once the development, integration, and assembly took a lot of time, they could not spend much time to find out the potential failure after launch by testing. This is one of the reasons that many CubeSats have failed to achieve their full mission objectives [1], [2].

To improve CubeSats mission success, builders should not ignore several things which recommended by [2], for instance, try to make less changes as much as possible during the development, increase testing time, conduct risk-based mission assurance, simple and robust design is good, team members' experience is important, have the spare parts and components, perform necessary tests and verify the purchased component or subsystem.

Backplane approach

Last few years, we worked on standardized backplane interface board which introduced by the University of Wuerzburg to reduce costs and delivery times of the CubeSats at Kyushu Institute of Technology (Kyutech). The reason we working on the backplane interface

board is that the backplane board implements all the harnesses on the PCB. Which prevents workmanship errors due to harness. And the board makes assembly and disassembly faster because of easy plug-in-play architecture.

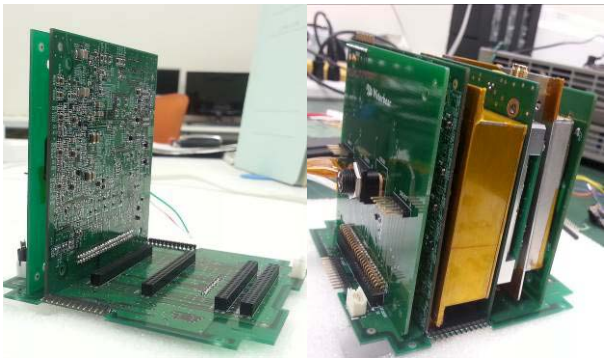

Figure 1. An example of the backplane board for 1U CubeSats with subsystems

So far, four CubeSat projects [3]–[6] (three CubeSat constellations and one 2U CubeSat) with a total of 12 CubeSats that has been designed, developed and tested at Kyutech have launched into space. All those 12 CubeSats were equipped with backplane interface boards. However, every CubeSat projects have different interface board due to their interface definitions. Mission, design and launcher requirements were the major driver of those interface changes. Even in one project, the interface has changed several times during development. Very tiny changes can create big problems. Every change during the project needs to be done in a very careful way. Thus the hardware changes are the enemy of the time reduction and it neglects the advantages of the backplane.

Therefore, we introduced a new approach to address this issue by creating a software-configurable backplane interface board that we named SoftCIB [7]. This programmable interface board allows user (CubeSat builder) to change the interface in a very short time at any phase of the CubeSat project. The main idea behind this programmable interface board is that the board should make the interface changes are possible even after CubeSats fully assembled.

OPERATIONAL CONCEPT

The key component of the SoftCIB is the single chip, so-called Complex Programmable Logic Device (CPLD), which mounted on the backplane PCB. This reprogrammable device will handle the interface connections as programmed. Figure 2 shows the operational concept of SoftCIB. The backplane accepts subsystem boards via 50-pin connectors. There are PCB routing from pins of 50-pin connectors to pins of the CPLD on the backplane as illustrated by purple color in Figure 2. However, interface connections between subsystems will be defined by software (blue color on Fig.2). Thus, any changes required on the interface connection can be done by reprogramming the CPLD. In other words, changing the interface connection doesn't change any hardware on the interface board. If it was hard-wired backplane board, the whole board needs to be manufactured again, in the same case as above. Which normally takes time, cost and verifications may need for the new board.

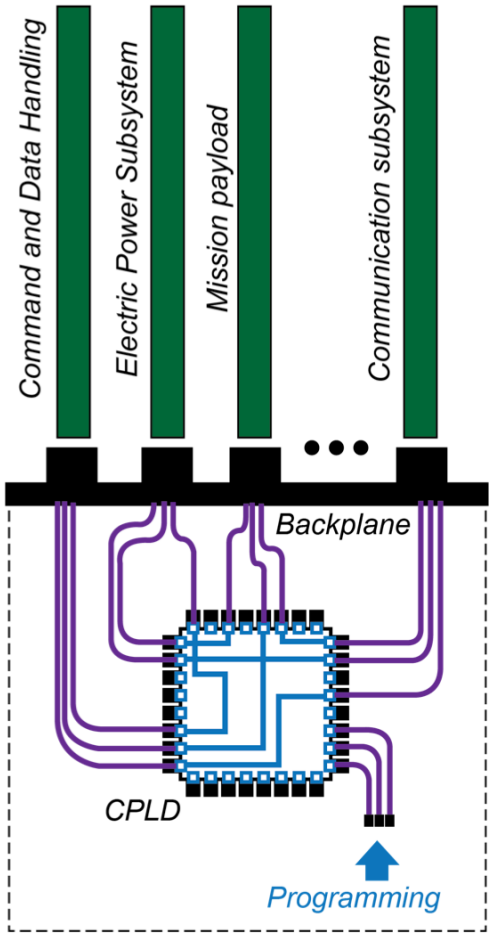

Figure 2. Operational concept of SoftCIB

Furthermore, this board can be used for different CubeSat projects which have different interface requirements with different payloads and subsystems. Instead of designing and manufacturing new board, the CubeSat builder can use SoftCIB to save time and cost.

DESIGN AND SPECIFICATIONS

Based on the trade-off study among different CPLDs, an ispMACH®4000ZE (4256ZE-7TN144I) device of the Lattice Semiconductor Corporation had chosen to implement on the SoftCIB considering power

consumption, price, temperature range, a number of pins, physical size, and development environment. Similar devices with CPLD, for example, FPGA, actually can implement the function that SoftCIB needed. However, the power consumption was critical factors since the CubeSats have a very limited power budget. The physical shape of the SoftCIB is similar to the BIRDS-1 and BIRDS-2 backplane. There are 6 units of 50-pin connectors which are purposed to host Onboard Computer Subsystems (OBC), Electric Power Subsystems (EPS), Front Access board(FAB), communications board (COM), Mission payload board (MSN) and Rear access board (RAB). The power lines such as 3.3V, 5V, and unregulated voltages are directly routed on the PCB. The analog signals and power lines are not going through the CPLD. Also, a few signal lines for critical communications were kept hard-wired on the PCB as the primary connection between OBC and COM. This means that not all signal lines on the backplane board can be programmed. Since SoftCIB is not space-proven yet, we decided to avoid SoftCIB to make critical communications. Photography of the SoftCIB is shown in the Fig.3. The specifications of the board are represented in Table 1. SoftCIB functions are tested with many different subsystem boards of the TableSat versions for BIRDS-1, and 2 projects. The main function, which is software interface connections (or software routing), worked properly and did not fail during the tests.

Table 1: The specifications of the SoftCIB

Specifications	Performance or information
Number of subsystems that can be installed on the backplane	6 subsystems
Number of Deployment switch connectors	4 deployment switches
Number of Solar Panel connectors	4 solar panel connectors
Number of software configurable connections	46
Total Power Consumptions	~ 40mA
Maximum tested speed for SPI communications through CPLD	4 Mbps
Maximum tested UART baud rate communications through the CPLD	115200 bps
Signal delay from input to output	9ns
Dimensions	97 × 99 × 1.2 (mm)
The programming method of CPLD	JTAG
Compatible Voltages from EPS	3.3V to 5V

The software of the SoftCIB

A software algorithm for the CPLD is very simple and shall be written in VHDL. Before programming the CPLD all interface connections are must be defined in the Interface Control Document (ICD). The program just needs to make connections that defined on the ICD. Each pin of the CPLD is already connected to particular pins of the connector. So, the user needs to guide the corresponding input and output. Then the signal on the input should directly go to the output. There are no other blocks or software circuits need to be defined in between inputs and outputs.

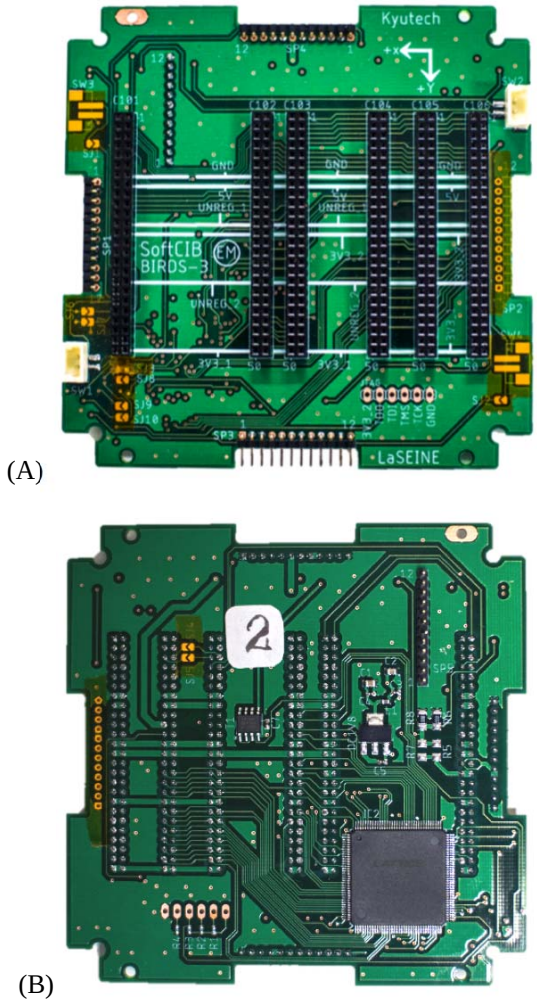

Figure 3. Software configurable backplane interface board; (A) – front view (B) – back view

VERIFICATIONS AND IMPLEMENTATIONS

There are many things to consider since the interface is a critical part of the satellite. Especially when there is an active semiconductor device and that handles the interface connections. Firstly, we conduct the Total Ionizing Dose (TID) test for the radiation. Three samples of the selected CPLD have been tested under the radiation up to 30 krad. This is a higher level of radiation dose than the unit qualification test level

defined in the ISO standards (ISO-19683:2017). And CPLD survived in that conditions. Which means that the CPLD can withstand at least two years in LEO. Next test for radiation was Single Event Effect test using heavy ions from the Californium-252. The test method described in this [8] research. The Single Event Latch-up (SEL) effects are detected by monitoring the current. And the current jump due to SEL was small, and it can be removed by power reset.

Table 2: Summary of the test results

Tests	Conditions	Results
Total Ionizing Dose radiation test	Up to 30 Krad	Passed, no failure
Single Event Effect Radiation Test	Heavy ion test with Californium-252, four samples, a total of 7 hours of exposure	No SEU detected, SEL detected by current consumption, Current increase due to SEL was 14 – 30mA. Effect of SEL is removed after power reset
Hot/Cold start test	-35^{o}C for a cold start, 65^{o}C for hot start	Passed, no failure
Thermal Vacuum Test	Four cycles, Coldest at -42°C, hottest at 67°C The pressure was below 1×10^{-3} Pa	Passed, no failure
Vibrations Test	6.8 Grms for random vibration, 22.6 G for quasi-static acceleration	P Passed, no failure

Another important test for an active electronic device of the SoftCIB was hot and cold start test. Because satellite shall be turned on after injected into space whatever the conditions. We conducted the Hot/Cold start test for SoftCIB in the thermal static chamber. SoftCIB started normally in both conditions at lowest -35^{o}C and highest 65^{o}C. All the tests above mentioned was at the subsystem or component levels. However, we conducted the system level testing after integrated as CubeSat. The summary of the test results shown in Table 2. Basically, the SoftCIB passed all the tests.

The BIRDS-3 project was the first user and a real implementation of the SoftCIB for CubeSat project. The BIRDS-3 have three CubeSats which have identical design except for backplanes. The flight models of the BIRDS-3 CubeSat are shown in Figure 4. Two of the satellites have hard-wired PCB backplane and one has the SoftCIB. System level tests after integration with the engineering model and the flight model of the BIRDS-3 have been conducted. All the test results of the SoftCIB test were compared with hard-wired backplanes. During the BIRDS-3 development, two versions of hard-wired backplanes were manufactured, including the test-bed versions for TableSat. And only one version of the SoftCIB backplane was used.

Figure 4. Flight models of the BIRDS-3 CubeSats

BIRDS-3 CubeSats are delivered to ISS by Cygnus NG-11 mission with Cygnus spacecraft in April 2019. The time after this paper has submitted, the CubeSats are going to be deployed from ISS.

CONCLUSIONS

We have presented the summary of the work which is programmable interface board for 1U CubeSat. The board is designed and developed at Kyushu Institute of Technology to reduce the cost and delivery time of the CubeSat project. The key idea is to use CPLD as a router of the interface connection between subsystem boards. The biggest merits this idea is that the CubeSat builders can change the interface connection at the phase of the project, even after the assembly has completed, without changing hardware, only reprogramming the CPLD. With a very low power consumption, 4256ZE-7TN144I device has been selected, tested and implemented for the SoftCIB. The various test has conducted at component, subsystem and system levels, and results are presented. The SoftCIB is implemented to real CubeSat project which is third of the BIRDS project series. And waiting for deployment in June 2019.

ACKNOWLEDGMENTS

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