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SpaceCube v3.0 NASA Next-Generation High-Performance Processor for Science Applications

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ABSTRACT

Electronics for space systems must address several considerable challenges including achieving operational resiliency within the hazardous space environment and also meeting application performance needs while simultaneously managing size, weight, and power requirements. To drive the future revolution in space processing, onboard systems need to be more flexible, affordable, and robust. In order to provide a robust solution to a variety of missions and instruments, the Science Data Processing Branch at NASA Goddard Space Flight Center (GSFC) has pioneered a hybrid-processing approach that combines radiation-hardened and commercial components while emphasizing a novel architecture harmonizing the best capabilities of CPUs, DSPs, and FPGAs. This hybrid approach is realized through the SpaceCube family of processor cards that have extensive flight heritage on a variety of mission classes. The latest addition to the SpaceCube family, SpaceCube v3.0, will function as the next evolutionary step for upcoming missions, allow for prototyping of designs and software, and provide a flexible, mature architecture that is also ready to adopt the radiation-hardened High-Performance Spaceflight Computing (HPSC) chiplet when it is released. The research showcased in this paper describes the design methodology, analysis, and capabilities of the SpaceCube v3.0 SpaceVPX Lite (VITA 78.1) 3U-220mm form-factor processor card.

I. INTRODUCTION

Accessibility to space resources, such as Earth-observation imagery, has been rapidly increasing due to contributions from the small satellite community [1]. Today, NASA is challenged with achieving a "balanced program" that manages the requirements and funding between varying trade-spaces such as; large vs. small missions, extended operations vs. new missions, and heritage vs. new technology [2]. However, even with these difficult programmatic decisions, NASA's 2015 technology roadmap [3] highlights cross-cutting technologies that can be improved to provide benefits across all topics and areas. One of these cross-cutting technologies is *avionics* which are the crucial electronics for spaceflight. For next-generation science and defense missions, spacecraft avionics and science data processing systems must provide advanced processing capability to support a variety of computationally intensive tasks including rapidly processing high-volume data from sensors (e.g. lidars, hyperspectral imagers), computing solutions for autonomously acting single or constellation spacecraft, and enabling complex algorithms for real-time/near-real-time data product generation and compression.

Significant needs for science are provided most recently in the 2018 decadal survey for Earth Observation [4] by the Space Studies Board of the National Academies. This survey emphasizes supporting new sensors to achieve higher resolutions, shorter temporal spacing, and improved accuracy.

"A critical element for all of these is the infrastructure for downloading and processing ever-increasing data streams. [4]*"*

Next-generation defense needs for on-board computation are most recently exemplified in the complex program goals of the Blackjack "Pit Boss" edge-processing node [5]. The "Pit Boss" emphasizes difficult artificial intelligence algorithms to enable a proliferated satellite constellation to autonomously task, collect, process, exploit, and disseminate multi-sensor data to varying global locations.

Jointly, for both science and defense, NASA and AFRL have recognized improving spaceflight computing capability as a natural "technology multiplier" for space missions. Through an agency level partnership, AFRL and NASA have performed extensive studies into computer architectures to address a range of flight computing requirements for future missions [6].

As previously highlighted, next-generation missions will require SmallSats to provide more capable processing solutions while also satisfying restrictive cost and reliability requirements. These considerations are

thoroughly described in [7], but in summary, space systems must address challenges including operational resiliency within the hazardous space environment, and meeting application performance needs, while simultaneously meeting size, weight, and power (SWaP) requirements. Therefore, to drive the future revolution in space processing, onboard systems need to be more flexible, affordable, and robust.

To address platform limitations, the SpaceCube family of processor cards were developed to provide a suitable system balance between power, size, reliability, cost, and data processing capability for spacecraft avionics and instrument processing. The SpaceCube v2.0 [8] processor system represented a significant improvement over heritage radiation-hardened (rad-hard) flight processor systems; however, the processing requirements of emerging science missions are exceeding even its capabilities. Increases in sensor capabilities coupled with data downlink constraints will continually drive these missions to require higher processing capabilities for generating data products on-board. This desire for even more on-board processing capacity has led to the development of the SpaceCube v3.0 which represents impressive performance gains of 10-100x or more over other flight single-board computers. The SpaceCube v3.0 processor card and box-level architecture are a flexible, modular, and compatible solution for varying sized spacecraft.

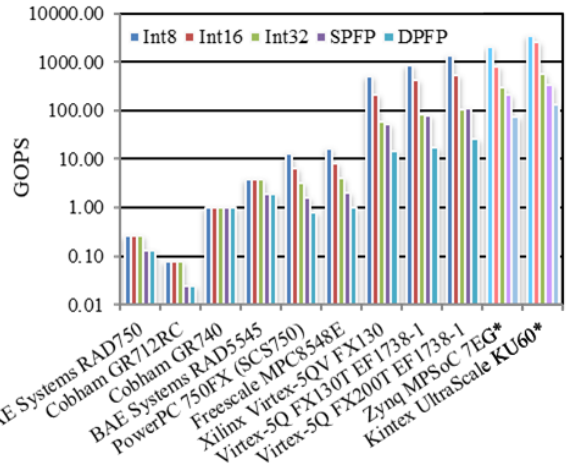
In this paper, we describe the design methodology and main features of the SpaceCube v3.0 (SCv3.0) processor card. The organization of the remainder of the paper is as follows. In Section II, we give a background of enabling programs and key concepts relating to the SCv3.0 development. Section III describes the overall SpaceCube family design approach. In Section IV, we present the hardware architecture design of the processor card. Section V describes the mechanical design. In Section VI, we describe the thermal solution. Finally, Section VII provides concluding remarks and future plans.

II. BACKGROUND

This section provides a brief description of available computing capabilities. Additionally, a brief description of SpaceCube heritage is provided along with an overview of the upcoming HPSC processor chiplet [9] that is complementary with the SpaceCube design development.

Space Computing Capabilities

Traditional rad-hard processors are typically several generations behind commercial devices in terms of processing capability. A study of space-grade processors [10] provides metrics to compare different types of devices, and highlights the disparity in performance between several state-of-the-art rad-hard processors and the Virtex-5 featured in the SpaceCube v2.0. Figure 1 extends these results and notionally includes the performance of the newer devices in the SpaceCube v3.0 for comparison. Figure 1 shows Giga-Operations per Second (GOPS) of these devices in log scale, where the Xilinx devices featured in the SpaceCube family of cards dramatically outperform the state-of-the-art rad-hard processors.



*UltraScale and MPSoC are estimates based off of existing data in [10], new metrics are in progress but not currently available

Figure 1. Log Scale Comparison of Giga-Operation Per Second of Space Devices

High-Performance Spaceflight Computing (HPSC)

The need for a new rad-hard spaceflight computing system with significantly more computational performance and power efficiency than the BAE RAD750 resulted in a joint partnership between AFRL and NASA from as early as April 2013. Together, this partnership issued a Broad Agency Announcement (BAA) entitled the Next Generation Space Processor (NGSP) Analysis Program, which would solicit contractors and vendors to propose architecture designs for a rad-hard general-purpose multi-core flight computer for the High-Performance Spaceflight Computing (HPSC) project [6]. Since formulation, the HPSC project contract was awarded to Boeing to provide these rad-hard multi-core computing processors or chiplets by April of 2021 [9]. The latest addition to the SpaceCube family, SpaceCube v3.0, will function as the next evolutionary step for upcoming missions, allow for prototyping of designs and software, and provide a flexible and mature architecture that is ready to adopt HPSC when it is released. The effort is complementary because the MPSoC (Multi-processor System-on-Chip) included in the SCv3.0 processor card features a quad-core ARM Cortex-A53 which will provide similar

computing capability and architecture to HPSC, but for missions that need more performance in the near-term or require a lower cost profile.

SpaceCube Heritage

SpaceCube is a family of Field Programmable Gate Array (FPGA) based on-board science data processing systems developed at the NASA Goddard Space Flight Center (GSFC). The goal of the SpaceCube program is to provide substantial improvements in on-board computing capability while lowering relative power consumption and cost.

The concept for the SpaceCube processing system was started in 2006, initially with Internal Research and Development (IRAD) program funding. Through a number of prototype demonstrations and proposal efforts, the SpaceCube program was funded by the Earth Science Technology Office (ESTO) to develop processor solutions for a variety of applications. To date, versions of SpaceCube have flown on a number of successful missions including HST-SM4, SMART, MISSE-7/8, STP-H4/H5, RRM3, and most recently with STP-H6/CIB and NavCube (STP-H6/XCOM). The version of the SpaceCube that was initially developed from 2006 to 2009 is known as SpaceCube v1.0 [11]. Since then, there have been many more iterations of SpaceCube designs developed and deployed. The SpaceCube v2.0 [8] was commercialized and can be purchased as a space-off-the-shelf solution called the GEN6000 from Genesis Engineering Solutions, Inc. The SpaceCube v2.0 was also adapted for other applications and missions described in [12]. Lastly, a CubeSat form-factor version of the SpaceCube v2.0 was developed, named SpaceCube v2.0 Mini, which was flown on STP-H5 and is described in detail in [13].

III. SPACECUBE APPROACH

In order to provide a robust solution to a variety of missions and instruments, the Science Data Processing Branch at NASA GSFC has pioneered a hybrid-processing approach that combines radiation-hardened and commercial components while emphasizing a novel architecture harmonizing the best capabilities of CPUs, DSPs, and FPGAs. This hybrid approach is realized through the SpaceCube family of data processors, which have extensive flight heritage as previously noted. In addition to the hybrid architecture design, the SpaceCube approach encompasses several design principles for both reliability and configurability at both card- and box-design levels.

Reliable Monitors

The SpaceCube design emphasizes the best capabilities of Xilinx devices; however, since these devices are more susceptible to radiation effects, the SpaceCube incorporates a more radiation resilient device as a monitor. The SpaceCube v1.0 and SpaceCube v2.0 featured the Cobham Aeroflex UT6325 radiation-hardened FPGA, while the SpaceCube v3.0 uses the Microsemi RTAX FPGA. These reliable supervisors serve as the health monitor of the Xilinx configuration and can trigger a rollback or reconfiguration from memory. To mitigate configuration Single-Event Upsets (SEUs), the monitor or the Xilinx FPGAs themselves can perform configuration monitoring and scrubbing. The scrubbing occurs at a programmable rate (blind scrubbing) or when an error has been detected (readback) depending on the configuration of the monitor. This architecture allows for a reliable means of externally controlling the Xilinx configuration data.

Quality Parts Selection

As noted in NASA's Small Satellite Reliability Initiative [14], incorporating commercial components into flight avionics systems can be challenging for designers because while use of commercial and automotive grade parts reduce costs, many off-the-shelf commercial components may not have any screening or radiation testing heritage. Due to the proliferation of new board designers and vendors that need to meet an increased demand in the SmallSat space ecosystem, many commercially available designs are developed without radiation or parts reliability considerations, which upon further analysis may not be appropriate for the risk posture assumed by high-value science missions. The SpaceCube approach begins with selection of NASA-qualified flight parts where feasible. However, when newer parts or components are desirable to push cutting-edge development, they are included, but screened and selected through a rigorous internal NASA GSFC parts control board, and have risk mitigation identified and designed into the system. The experts in the parts control board assist the SpaceCube development team in pursuing parts qualification processes and perform selective radiation testing where required for mission needs.

Modularity

The original SpaceCube v1.0 design was based on a custom stacking connector architecture. While there were some advantages, the custom stacking connector approach used in SpaceCube v1.0 introduced more signal discontinuities, affecting signal integrity, and also supported fewer point-to-point connections between cards because all pins routing between cards must be contained within a single connector's pin count. The SpaceCube v2.0 design converged on supporting industry standard backplane-style interfaces to provide more compatibility with other systems and commercial

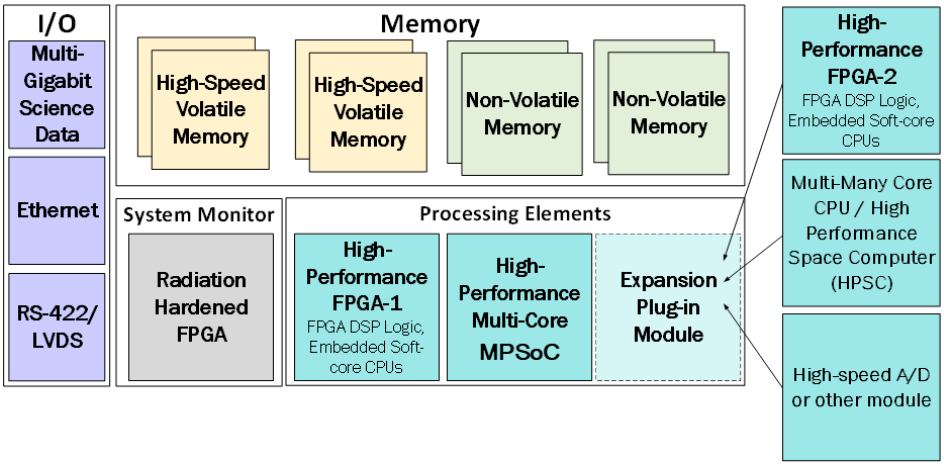


Figure 2: High-Level Block Diagram of SpaceCube v3.0 Processor Card

designs. The backplane design can be easily expanded to include additional cards, and unlike the original SpaceCube v1.0 stacking architecture, cards can be easily swapped in and out of the system.

Xilinx Devices and Intelligent System Design

The keystone foundation of SpaceCube designs are the reconfigurable Xilinx FPGAs. The philosophy of the SpaceCube approach is to use the latest radiation-tolerant (i.e. susceptible to radiation induced upsets but not radiation induced destructive failures) processing element for the advantages they provide in performance, SWaP, and affordability. Then, to address reliability and radiation concerns, accept that upsets will occur on these devices and mitigate the consequences with system design strategies. The resulting platform is inherently reconfigurable, and provides application designers with a flexible system that enables rapid development and can be reused for multiple missions. The reconfigurable capability allows for the SpaceCube to change its functionality and support different roles at varying stages of a mission

Custom Mission-Specific IO Card Support

The SpaceCube box-level processing system typically supports a base configuration that consists of a power card, processor card, and backplane with additional card slots. To avoid expensive one-off avionics systems, the SpaceCube approach reuses the base system hardware architecture, and incorporates a mission-unique IO interface card. The SpaceCube is reconfigurable, therefore, the hardware design adapts to new system requirements by reconfiguring the underlying programmable elements on the processor card to interface with the application-unique IO cards. Examples of this approach for the SpaceCube v2.0 system are described in [12].

IV. HARDWARE ARCHITECTURE

The SCv3.0 design uniquely introduces the combination of a high capacity FPGA, a high performance SoC (System-on-Chip), and reliable FPGA supervisor. This section describes the architecture and key features of the SCv3.0 processor card.

High-Level Design

The SpaceCube v3.0 is a SpaceVPX Lite (VITA 78.1) [15] 3U-220mm form-factor card featuring two core technologies, combining a Xilinx Kintex UltraScale (20 nm FPGA) with a Xilinx Zynq MPSoC (quad-core 64-bit ARM Cortex-A53, dual-core Cortex-R5, 16 nm FinFET+ FPGA) to provide powerful fixed-logic processors with vast amounts of reconfigurable-logic FPGA resources. The Kintex UltraScale FPGA and Zynq MPSoC are in-flight reconfigurable which allows for extreme adaptability to meet dynamic mission objectives, while the rad-hard supervisor provides reliable operation and monitoring. A high-level block diagram of primary components is pictured in Figure 2.

The architecture of the SCv3.0 is versatile for porting and mapping algorithms to the design because they can benefit from both the extensive reconfigurable fabric of the Kintex UltraScale FPGA and the high-performance ARM processors in the Zynq MPSoC. As described in [16], hybrid architectures are advantageous for algorithm acceleration because sequential or control flow portions of an algorithm can be implemented quickly and efficiently on the quad-core processors, while other dataflow-oriented algorithms that are highly parallel or are comprised of computation-heavy iterative operations can be accelerated in the FPGA fabric of both the Kintex UltraScale and the Zynq MPSoC. The Zynq MPSoC multi-core processor (ARM Cortex-A53) alone provides an immense speedup over the embedded processors in the SpaceCube v2.0 (IBM PowerPC440). CoreMark is a

performance benchmark developed by the Embedded Microprocessor Benchmark Consortium, designed to replace the antiquated Dhrystone benchmark. Table 1 displays the CoreMark scores of the processor architectures used by SpaceCube processors, and further highlights the significant computational margin increase from SpaceCube v2.0 to SpaceCube v3.0. Additionally, the Kintex UltraScale FPGA device is a significant upgrade in both performance and FPGA resources over the Virtex-5 FPGA. Table 2 shows a comparison of the FPGA logic resources available throughout the generations of SpaceCube processors.

The SCv3.0 processor card features an expansion card option / plug-in module connector that allows tightly-coupled, mission-unique cards to be developed and interfaced directly to the processor card. This feature allows mission developers to expand the system as needed without an obligation to provide or develop a separate I/O card should the mission be unable to support that configuration for the avionics box. This expansion card interface takes advantage of the VITA 57.4 FPGA Mezzanine Card Plus (FMC+) [17] industry standard which provides flexibility for testing and developing with available commercial cards already compliant with the standard. This FMC+ maintains backward compatibility with the standard FMC, however, it also breaks out a large number of Multi-Gigabit Transceiver (MGT) interfaces which, using the JESD204B standard, can interface with multi-giga-sample ADC/DACs. These ADCs/DACs are essential to implementing lidar, radar, communication, and other applications. The SpaceCube v3.0 expansion card, however, is not limited to FMC+ dimensions and can accept larger cards if needed. Incorporating the mission-unique expansion card allows the SCv3.0 processor card to fullfill a number of roles as a powerful instrument processor, since ADC converters, DAC converters, Gigabit Ethernet, 1553, additional co-processors, etc… can be interfaced directly to the card.

For memory storage resources, each of the three FPGAs has an attached flash memory for non-volatile storage. The NAND flash memory attached to the radiation-hardened monitor (RHM) stores configuration files, enabling the radiation-hardened monitor to configure and scrub the Kintex UltraScale FPGA. Each NAND flash memory attached to the Kintex UltraScale FPGA and MPSoC stores software applications, FPGA configuration files, and other application data. However, the Kintex UltraScale NAND flash memory is designed to optimize write throughput, due to the expectation of users to integrate sensors and high-throughput instruments to this device.

Table 1: CoreMark Results for SpaceCube Devices

Processor	Configuration	CoreMark
MicroBlaze (Softcore FPGA Fabric)	Xilinx v8.20b Virtex-5, 5-Stage Pipeline 16K/16K Cache 125MHz	238[1]
IBM PowerPC 405 (SpaceCube v1.0 Virtex-4)	300 MHz	664.79[1]
IBM PowerPC 440 (SpaceCube v2.0 Virtex-5)	400 MHz, Bus 100 MHz	1155.62
	125 MHz, Bus 125 MHz	361.13
ARM Cortex-R5 (SpaceCube v3.0 Zynq MPSoC)	500 MHz	1286.03
ARM Cortex-A53 (SpaceCube v3.0 Zynq MPSoC)	1.2 GHz, -O3	16449.62[1]
	1.2 GHz, -O2	15866.62

Both the Kintex UltraScale FPGA and Zynq MPSoC have attached DDR3 (x72-bit wide, 533 MHz) SDRAM volatile memory that provide significant bandwidth for high-performance processing. Two DDR3s are attached to the Kintex UltraScale and one DDR3 is attached to the ARM processing system side of the Zynq MPSoC. The selected memories have an extra byte to support EDAC (Error Detection and Correction) for improved radiation mitigation for space operation. These memories can be used for operating system storage, but also enable real-time application data processing, by buffering images, instrument data, and intermediate products.

Table 2: SpaceCube v3.0 FPGA Resources

Resources	SpaceCube v1.0	SpaceCube v2.0		SpaceCube v3.0
		(FX130 Ver.)	(FX200 Ver.)	
LUTS (K)	101	164	246	562
FF (K)	101	164	246	1124
RAM (Mb)	0.79	21	33	49 + 27 UltraRAM
DSPs	256	640	768	4488

The Xilinx FPGAs are low-cost, radiation-tolerant components; however, the remaining system is designed with NASA-qualified flight parts. As previously described in Section III, to monitor Xilinx devices, the architecture includes a radiation-hardened Microsemi RTAX FPGA to mitigate radiation effects across the system. This radiation-hardened monitor provides

[1] https://www.eembc.org/coremark/scores.php

radiation mitigation and system monitoring through several means. The monitor can configure the Kintex UltraScale FPGA from up to 64 unique configuration files and scrub the configuration memory to correct any upsets. These configuration files can also be updated via ground commands to the monitor. It also uses error detection and redundant copies to mitigate radiation upsets to the Xilinx configuration files stored in the external non-volatile memories. In addition, it monitors the health of the Zynq MPSoC processors, the Kintex UltraScale FPGA, and any co-processors on the expansion card using watchdog timers.

The system has been deliberately designed so that the radiation-hardened monitor powers on first, and then controls the power sequencing of the numerous Xilinx FPGA voltage rails. In addition, the RHM monitors each voltage rail on the board and the current on critical power rails to aid in fault detection. This allows the Xilinx FPGAs to be power-cycled locally to clear any radiation-induced upsets. Due to this functionality, the radiation-hardened monitor can respond to ground commands even while the Xilinx FPGAs are unpowered, and does not require the entire card to be power-cycled. The radiation-hardened monitor also hosts a SpaceWire (SPW) router which connects externally through the backplane and front-panel connectors, and connects to the Kintex UltraScale and the Zynq MPSoC. This feature allows the spacecraft to communicate directly with the radiation-hardened monitor and both Xilinx FPGAs through the same interface.

The SpaceCube v3.0 advances the state-of-the-art of MGT quantity, routing, and performance for spaceflight. Both the Kintex UltraScale FPGA and Zynq MPSoC feature dozens of Multi-Gigabit Transceiver interconnects that route between the Zynq MPSoC and Kintex UltraScale FPGA, to the backplane connectors, and to the expansion card connector. These transceivers allow high volumes of data to be exchanged in short periods of time while minimizing the Printed Circuit Board (PCB) area for routing resources. Due to radiation-effects mitigations needed for the Zynq MPSoC, the expected system architecture deployment for the SCv3.0 processor card is to integrate high-speed sensor or instrument interfaces to the Kintex UltraScale, which will perform significant preprocessing before transferring the data to the Zynq over this high-bandwidth (8x MGT lanes) interface for higher order processing or additional pipelined algorithm stages. In addition, the SCv3.0 processor card includes an innovative technique that allows selectable routing of the MGT differential pairs to varying destinations.

The VPX backplane connector is a high-density connector that provides 3.3V, 5V, +/-12V power rails from the backplane card. The backplane connector I/O includes Multi-Gigabit Transceiver interfaces, LVDS, and GPIO. The VPX connector allows significantly faster signal rates than typical flight connectors. Finally, the SpaceCube v3.0 processor card also features a 37-pin Nano connector, a 21-pin Nano connector, and an 85-pin Nano connector that provide debug and flight interconnects. A high-level view of the main interconnects is displayed in Figure 3.

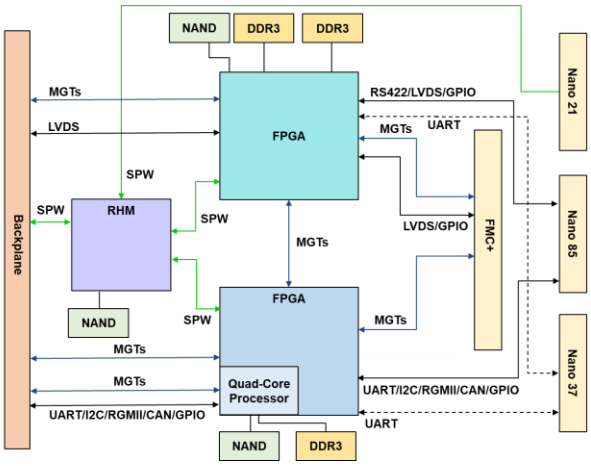


Figure 3: High-Level SpaceCube v3.0 Interconnects

HPSC Integration

As described in Section II, the HPSC rad-hard-by-design manycore processor, being co-developed by GSFC, AFRL, and JPL is targeted for a variant of the SpaceCube v3.0 processor card, replacing the Zynq MPSoC in the design. For more immediate integration of the HPSC with SpaceCube v3.0, a planned FMC+ Card in the expansion slot, as displayed in Figure 2, will be in development when the chiplets are available.

Device Selection

As described previously, the SCv3.0 processor card features two complex Xilinx devices, the Kintex UltraScale and the Zynq MPSoC. Following the results of the SpaceCubeX project [18], the SpaceCube team performed a thorough design trade before finalizing the selection of these devices. The Kintex UltraScale was selected primarily because of Xilinx's commitment to make the design its first 20 nm FPGA product for space applications with the XQRKU60 device. This decision was cemented with the compelling results provided in [19] and [20] for several radiation tests of the device. For the second device, the Zynq MPSoC was originally selected due to the initial support suggested by Xilinx for the ZU19EG as a Space Grade Device in [21], however, radiation testing such as [22], [23] and other reports showed single-event latchup for the device. Further details cannot be disclosed; however, mitigation

schemes have been suggested, a number of which have been incorporated into the design, to allow the MPSoC to be capable for space operation in certain use cases. Additionally, from a NASA strategic perspective, lessons for creating designs around the ARM Cortex-A53 would benefit the future HPSC.

V. MECHANICAL DESIGN

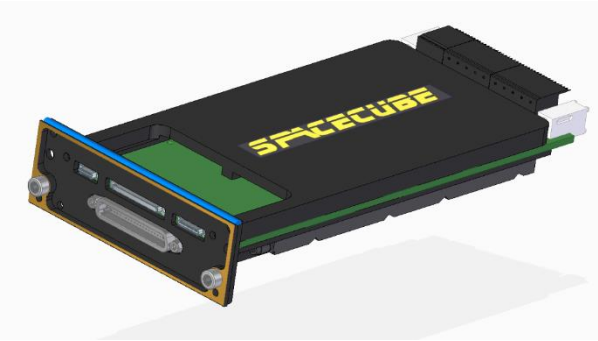


Figure 4: 3D Model of SpaceCube v3.0 Mechanical Design

The mechanical design is a key aspect of the system design that enables a high-performance processing system to operate in a space environment. The SpaceCube system uses advanced devices and imposes grid array densities that present a variety of challenges in the process of obtaining a suitable mechanical and packaging design for spaceflight applications. The card module (Figure 4) installs into a plug-in style chassis that accommodates 220mm long cards conforming to most guidelines in the space VPX standard. The card module is equipped with rugged, captive hardware mounted to the front panel. The captive hardware provides the dual function of insertion and extraction into and out of the chassis assembly. The design accommodates the use of several card retainers: those mounting directly to the module (card-loks or wedge-locks) and those mounting directly to the chassis, such as wedge-tainers). The pitch of the card is configurable based on the application need for a mezzanine card on the secondary side of the module and based on the power dissipation of the electronics. The baseline design without the mezzanine conforms to the 1.2 inch pitch option for a primary side retainer per the SpaceVPX Lite standard. The higher dissipating option that includes a mezzanine card has a 1.5 inch pitch.

The mechanical frame and front panel construction allows the SpaceCube v3.0 to conform to industry-leading MIL-STD specifications and NASA guidelines including GSFC-STD-7000 for sine vibration, random vibration, quasi-static, shock, thermal vacuum, and thermal cycling. The analysis successfully verifies the module is able to survive a 14.1 GRMS 3-sigma and 50g static input load. The frame uses a fastened construction made of durable CNC machined 6061-T6 aluminum. All fasteners are stainless steel and all threaded holes have self-locking, stainless steel inserts to withstand severe vibration, shock, and multiple insertion/extraction cycles. The design accommodates multiple thermal design solutions to dissipate the heat.

VI. THERMAL DESIGN

This conduction-cooled, electronics packaging assembly design offers a reliable and lightweight processor system to meet stringent weight requirements and perform in the harsh, rugged and confined environments encountered in space, military, and airborne applications. Several thermal, structural, and thermo-mechanical analyses trade studies were conducted to achieve an optimal balance of designing for processing performance, PWB layout IPC-6012DS Class 3/A requirements, assembly of components on the dense PWB, and environmental performance goals. The main driver was the thermal design implementation. The multi-functional stiffener frame is the mechanism which addresses thermal and structural design concerns. Along with other thermal design features, it acts as an effective passive thermal design solution and the primary thermal path from PWB to card retainers. For representative use-cases, the SCv3.0 processor card shows a power dissipation range from 22.6 to 45.8 W. Analysis designed to a 50W worst case scenario has shown that use of the thermal design solution enables all assembled components to meet de-rated junction temperatures. The analysis was performed assuming the card module is installed in a standard aluminum electronics chassis with only the base controlled at 55C, see Figure 5.

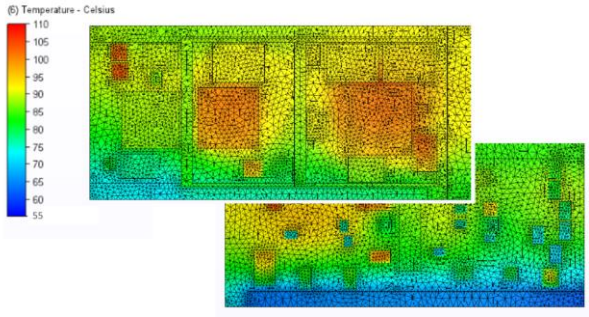


Figure 5: Thermal Analysis of SpaceCube v3.0 Processor Card

VII. SUMMARY AND CONCLUSIONS

The SpaceCube v3.0 processor card is an evolutionary advancement of spaceflight computing capability. This novel design integrates two complex, high-performance Xilinx devices with a radiation-hardened monitor to provide exceptional performance and reliability, in a

commercial form factor. This design, following the SpaceCube design approach, leverages years of development experience from the highly successful SpaceCube v2.0. Therefore, this new processor card will provide a processing solution for next-generation needs in both science and defense missions. Finally, lessons learned and design implementation experience can be used to incorporate the HPSC chiplet in future iterations of the design or as an independent expansion card.

Future Plans

The prototype SpaceCube v3.0 processor card will be available in October 2019. Additionally, this design has been leveraged to construct the SpaceCube v3.0 Mini processor card, which transfers a subset of the SCv3.0 capability onto a 1U CubeSat form-factor card.

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