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NEW PROCESSING METHODS FOR LARGE AREA ELECTRONICS

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ACADEMIC DISSERTATION

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ABSTRACT

In Large Area Electronics (LAE) there are multiple processing methods to take advantage of. Components can be produced for example by directly printing patterned layers on top of each other. Most common printing methods are gravure, flexographic, silk screen and inkjet. Electronics done only by such processes suffer from the limitations stated by the printable materials and the process equipment.

This thesis shows some critical LAE processing challenges, and introduces new ways to overcome them. The goal is to use roll-to-roll compatible methods. Some traditional processing techniques are used in a new way. Commercial and prototype materials are used in the testing. The work includes experimental results of printed thin films made with *polymer* or *carbon nanotube* semiconductors and either *low-* or *high permittivity* dielectrics.

After material selection, the transistor electrode quality and pattern resolution (dimensions) govern the electrical performance. Electrical results of low-voltage (5V) thin film transistors and circuits are reported. This work includes the experimental results of roll-to-roll (R2R) compatible thin metal film patterning methods like etching with a new *printable gel etchant*, and high resolution *laser ablation*. Furthermore, a new lamination concept is introduced. Laminating together two separate substrates allows new possible material combinations and new electrode options for both sides of the device.

Finally, these methods are combined in a demonstration device: a tactile sensor matrix is built using air-gap transistors. The transistors are constructed using R2R printed active layers including gel etched electrodes on one foil, and inkjet printed spacers and electrodes on another foil. When foils are laminated together, air-gap transistors are formed, and the flexible structure make the transistors sensitive to tactile input. The shape and sensitivity of such sensor structure is easy to modify for different applications.

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The publications were done with colleagues at VTT and Konkuk University, and my warmest thanks go to all who participated in the hard work.

CONTENTS

LIST OF ORIGINAL PUBLICATIONS

This thesis is based on the following original publications which are referred to in the text with Roman numerals **I–V**. The publications are reproduced with kind permission from the publishers.

I **T. Hassinen**, H.G. Sandberg, *"Gravure printed low voltage polymer transistors and inverters"*, Thin Solid Films, vol. 548, pp. 585–589, 2013.

II **T. Hassinen**, B. Ahn, S-L. Ko, *"Printed Polymer and Carbon Nanotube Thin Film Transistors with High-k Barium Titanate Insulator"*, Japanese Journal of Applied Physics, vol. 53, no. 05HB14.1-4, 2014.

III M. Vilkman, **T. Hassinen**, M. Keränen, R. Pretot, P. van def Schaaf, T. Ruotsalainen, H.G. Sandberg, *" Fully roll-to-roll processed organic top gate transistors using a printable etchant for bottom electrode patterning"*, Organic Electronics, vol. 20, pp. 8-14, 2015.

IV **T. Hassinen**, T. Ruotsalainen, P. Laakso, R. Penttilä, H.G. Sandberg, *"Roll-to-roll compatible organic thin film transistor manufacturing technique by printing, lamination, and laser ablation"*, Thin Solid Films, vol. 571, pp. 212–217, 2014.

V **T. Hassinen**, K. Eiroma, T. Mäkelä, V. Ermolov, *"Printed pressure sensor matrix with organic field-effect transistors"*, Sensors and Actuators A: Physical, vol. 236, pp. 343-348, 2015.

AUTHOR'S CONTRIBUTIONS

I The author planned the experiments and decided the printable active material combinations, oversaw the printing processing, and did the final layer processing. He measured and analysed the results, and wrote the paper.

II The author took part in material selection, planning and processing of the samples. He measured the electrical characteristics and analysed the results. He wrote the paper with the help of the co-authors.

III The author took part in semiconductor and dielectric material screening and testing for the final *thin film transistor* (TFT) printing process. With the help of the co-authors he planned the TFT active layer printing processes. He measured the electrical characteristics and analysed the results. He wrote the transistor characterization and analysis part of the paper.

IV The author took part in planning, measuring, and analysing the laser ablation work. He took part in the transistor testing. The author designed, processed, measured and analysed the final laminated TFT structure. He wrote the paper with the help of the co-authors.

V The author took part in designing the structure and the process. He constructed the final laminated air-gap transistors using the foils that had been separately processed by the co-workers. The author measured and analysed the devices and wrote the paper with the help of the co-authors.

Other related publications by the author

T. Hassinen, A. Alastalo, K. Eiroma, T.-M. Tenhunen, V. Kunnari, T. Kaljunen, U. Forsström, and T. Tammelin, “All-Printed Transistors on Nano Cellulose Substrate”, MRS Advances, vol. 1, no. 10, pp. 645–650, 2015.

S. Jussila, M. Puustinen, **T. Hassinen**, J. Olkkonen, H. G. Sandberg, and K. Solehmainen, “Self-aligned patterning method of poly (aniline) for organic field-effect transistor gate electrode”, Organic Electronics, vol. 13, pp. 1308-1314, 2012.

J. Kim, **T. Hassinen**, W. H. Lee, and S. Ko, “Fully solution-processed organic thin-film transistors by consecutive roll-to-roll gravure printing”, Organic Electronics, vol. 42, pp. 361–366, 2017.

J. Kim, J. Kim, B. Ahn, **T. Hassinen**, Y. Jung, and S. Ko, “Optimization and improvement of TIPS-pentacene transistors (OTFT) with UV-ozone and chemical treatments using an all-step solution process”, Current Applied Physics, vol. 15, pp. 1238-1244, 2015.

G. C. Schmidt, D. Höft, K. Haase, M. Bellmann, B. Kheradmand-Boroujeni, **T. Hassinen**, H. Sandberg, F. Ellinger, and A. C. Hübler, “Fully printed flexible audio system on the basis of low-voltage polymeric organic field effect transistors with three layer dielectric”, Journal of Polymer Science Part B: Polymer Physics, vol. 53, no. 20, pp. 1409–1415, 2015.

K. E. Lilja, T. G. Bäcklund, D. Lupo, **T. Hassinen**, and T. Joutsenoja, “Gravure printed organic rectifying diodes operating at high frequencies”, Organic Electronics, vol. 10, no. 5, pp. 1011–1014, 2009.

J. Seong, J. Park, J. Lee, B. Ahn, J. H. Yeom, J. Kim, **T. Hassinen**, S. Rhee, S. Ko, D. Lee, and others, “Practical Design Guidelines for the Development of High-Precision Roll-to-Roll Slot-Die Coating Equipment and the Process”, IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 6, no. 11, pp. 1677–1686, 2016.

ABBREVIATIONS

FET	field-effect transistor
μ	mobility ($cm^2/(Vs)$)
ε_o	permittivity of vacuum
ε_r, k	relative permittivity of a material, a.k.a dielectric constant
d_{air},d_{ox}	thickness of air gap layer or oxide layer
E	*Young's modulus*
γ	*Poisson's ratio*
f_T	transfer frequency
low-k	material with low relative permittivity
high-k	material with high relative permittivity
AFM	atomic force microscope
C, C_A	capacitance (F), capacitance per unit area (F/cm^2)
C_{ins}	insulator capacitance per unit area (F/cm^2)
CNT	carbon nanotube
g	acceleration of gravity
G	gate (transistor electrode)
h	thickness
W	channel width (μm)
L	channel length (μm)
LAE	large area electronics
N_T	interface trap density (cm^{-2})
d	thickness (nm)
I_{DS}	drain to source current (amperes)
IoT	internet of things
ITO	indium tin oxide
k	Boltzmann constant $1.3806504 \cdot 10^{-23}$ JK^{-1}
OFET	organic field-effect transistor
OTFT	organic thin film transistor
P	pressure
PECVD	plasma enhanced chemical vapor deposition
PEN	poly(ethlylene naphthalate)

PET	poly(ethylene terephthalate)
PMMA	poly(methylmethacrylate)
PS	polystyrene
r	radius
R	resistance (Ω)
R2R	roll-to-roll (e.g. printing)
S2S	sheet-to-sheet
S	(inverse) subthreshold slope (V/dec)
S-D	source – drain (transistor electrodes)
SEM	scanning electron microscope
EDS	energy dispersive x-ray spectroscopy
T	temperature in absolute scale (Kelvin)
TFT	thin film transistor
UV	ultraviolet (laser light wavelength)
UV-Vis-NIR	ultraviolet-visible-near infrared (spectroscopy)
V	voltage (volts)
V_{DS}	drain to source voltage (volts)
V_{GS}	gate to source voltage (volts)
V_{TH}	threshold voltage (volts)

1 INTRODUCTION

1.1 BACKGROUND AND MOTIVATION

The electronics industry is looking for new areas to expand into, and one possible direction is the concept “internet of things”, IoT. At the lowest level it consists of sensors and readout electronics. In some applications, the traditional silicon based electronics is not suitable because of the processing cost, processing area limitations, or processing temperatures needed. The rigidity of silicon makes it unsuitable for flexible applications. In cases where high performance is not needed, new Large-Area Electronics (LAE) processes can be suitable. In LAE, traditional mass-production methods like printing, sputtering, and wet etching have been exploited for deposition and pattering of new electronic materials [1-4].

In traditional “large” area electronics applications like TFT backplanes for displays, a comparably high resolution patterning and high performance is needed. In that case the semiconductor is typically deposited using evaporation or plasma enhanced chemical vapour deposition (PECVD) (organic small molecules like pentacene or amorphous silicon) [5]. Patterning is done by lithographic processes. For large-area applications with less strict needs for resolution and performance, a cheaper processing method is available: deposition from solution phase. Certain organic or inorganic semiconductors, dielectrics, and metal nanoparticles can be formulated into printable inks. The ink can be deposited as suitable patterns with a printing method like gravure, flexographic, or inkjet printing. The patterned layers can be deposited successively on top of each other [6-8]. This kind of additive processing is fast and cheap, but lacks in performance. The printing process is limited by the deposition technique, so the printing pattern dimensions and the ink’s fluidic behaviour limit the line width to 5-100 μm [9-11]. The latest development with *reverse offset* makes it possible to print micron size patterns, but the printable area is small and the cost is relatively high [12, 13].

Printed conductors (electrodes and wiring) are often made with conductive polymer inks [7, 14–16], carbon based inks, or metal inks. The polymeric conductors have many orders of magnitude lower conductivity than metals and they can be sensitive to changes in humidity and even gases [17, 18]. Carbon nanotube (CNT) and graphene inks are extensively investigated for use in future electronics, but their processability in solution phase and in large amounts must be improved [19]. Organometallic compounds make smooth films, but are relatively expensive and are usually used only in inkjet printing due to their low viscosity [20]. Printed metal nanoparticle inks often produce a rough surface that sometimes feature peak defects, which create short circuits in stacked structures [20, 21]. This increases the required dielectric thickness between the conducting layers. Sintering of metal inks is typically

done at 100-200 °C. Their conductivity increases with increasing temperature [22]. For some substrates and active materials this temperature range is unsuitable. The conductivity of sintered metal ink is always lower than that of bulk metal of similar dimensions [23].

When printing methods provide inadequate electrode quality, some processing methods commonly used in traditional electronics industry can be applied. Pre-patterning of the substrate with a sputtered or evaporated metal film is one option to get high conductivity and a smooth, thin film. Traditional lithography is often employed, but it is only available as a batch process, or in very slow continuous processes [24, 25]. In high throughput roll-to-roll (R2R) compatible processes etching mask printing [26], lift-off mask printing [27], [28] and direct etchant printing [29] have been used. Laser patterning can produce fine details [30–33]. The patterning topics in this thesis are mass production compatible direct etch printing and laser ablation.

Many organic and inorganic solution based semiconducting and dielectric materials can be used to build an active device like a *field effect transistor* [34]. Finding a good combination of materials is important [35]. The material supplier can often provide a set of materials that work together in a certain stack structure. The dielectric layers must be thin, continuous, smooth, and have good electrical insulating behaviour.

For some semi-crystalline materials it may be hard to optimize the semiconductor printing approach. Film formation is sensitive to many parameters: solvent, drying temperature (how much time the film has to form), printing pressure, -speed, –pattern, and underlying surface properties. The molecular ordering that affect the electrical performance can be sensitive to shear forces present during printing and lamination (see chapter 4.2) [36-39]. In this thesis printing topics are covered mainly in **I-III**, whereas lamination topics are covered in **IV** and **V**.

Lamination is traditionally used to attach a foil that protects the thin active layer. Active layers can also be laminated [30, 40]. This technique allows the use of materials with non-compatible solvents [41]. It allows the use of pre-patterned (e.g. metal) electrodes on both sides of the structure [42, 43]. The active layers are automatically shielded by the two substrates. Lamination enhances the lifetime of organic transistors [44]. In one work the printed circuits were stacked in a 3D structure, with through vias connecting the circuit [45]. Lamination can be used to study interface physics [4, 40]. The surface microstructure is formed differently when laminating dry films together compared to film formation from solvent [46]. This possible enhancement in device properties is studied in this thesis by comparing laminated devices with gravure printed and spin coated devices.

One case where lamination must be used is the air-gap transistor. Air voids form the gate dielectric part in the transistor [47] (see 2.3). In this thesis a sensing application that uses laminated air-gap transistors is presented.

1.2 SCOPE AND CONTENTS OF THE THESIS

Many processing methods are available for LAE. The choice of method depends on the application, substrate, cost, and available equipment. This thesis introduces new options and ways to combine traditional processing methods. The focus is on producing thin high quality layers with adequate patterning resolution. To reach high *large area electronics* performance using relatively cheap, high throughput mass production or roll-to-roll methods, this thesis addresses the following questions:

- Can low-voltage OTFT operation be reached with
    - printed thin films? (**I**)
    - printed high-k dielectric? (**II**)
- Can high quality thin metal electrodes be patterned by
    - etchant printing? (**III**)
    - laser ablation? (**IV**)
- Can active layer lamination be used in transistor processing?
    - (**IV, V**)
- Can an example application be demonstrated using R2R processes and lamination?
    - air-gap transistors as tactile sensor matrix (**V**, using methods from **III** and **IV**)

The roman numerals of the included publications where these questions were studied are given in parenthesis. The work is divided into a material testing phase and a process development phase, see Figure 1. Most of the work was done at laboratory scale, but some roll-to-roll pilot printing demonstrations were also done. The tactile sensor application proof-of-concept was done at laboratory scale, using R2R processed transistor layers.

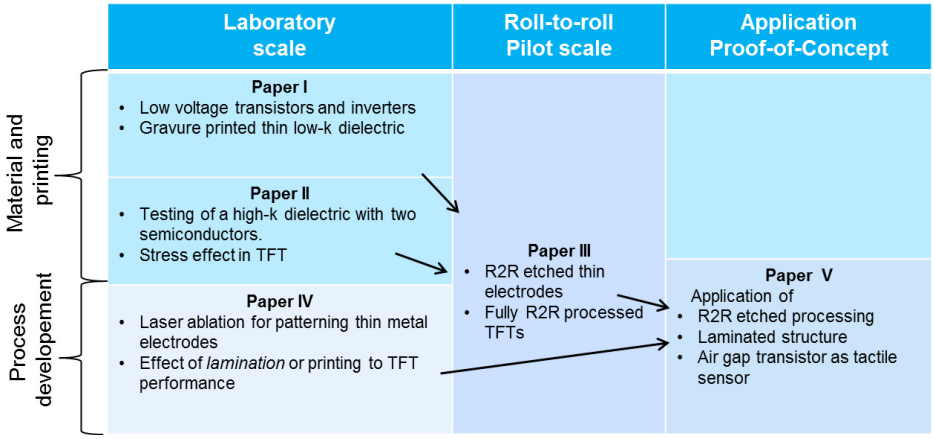


Figure 1. Overview showing how the research work was divided into laboratory scale testing, pilot scale R2R testing, and an application proof-of-concept testing.

2 THEORY

To understand the challenges in thin film electronics production that employ large area processes, a crucial and demanding component was chosen to test the capability of the processes: the *thin film transistor* (TFT). The transistor structure and operation is briefly explained to elucidate the effect of transistor dimensions, layer quality, and material selection on transistor performance.

2.1 THIN FILM TRANSISTOR STRUCTURE

The TFT structure is shown in Figure 2 and Figure 3. The distance between the source and drain electrode is called channel *length L*. The channel *width W* is the effective length of the parallel source-drain electrodes. There is an insulating (dielectric) layer with a *thickness d* between the gate and the semiconductor. The TFT can be processed with the gate on the bottom or on the top by having the material stack inverted (Figure 2). The configuration is usually chosen by necessity, since the materials work better when deposited on each other in certain order [48].

The bottom-gate configuration is suitable for transistors that use inorganic oxide or small molecule semiconductors. The electrodes are often in the same plane with the electrical channel (in a co-planar configuration). This allows a direct contact into the channel region. High performance crystalline or semi-crystalline small molecule semiconductor TFTs can be constructed in this way, but the performance of such transistors is sensitive to processing variations [49]. A drawback of this configuration is that the semiconductor is exposed to the environment, and an additional barrier layer is always needed.

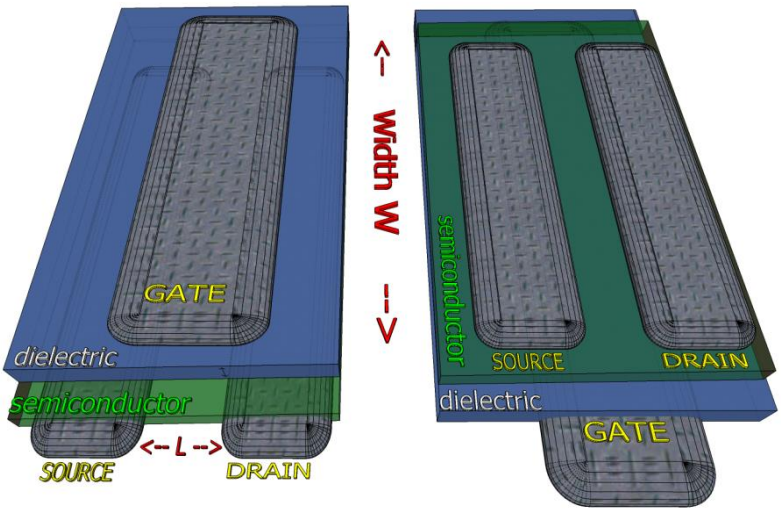


Figure 2. Concept pictures of top-gate and bottom gate *staggered contact* thin film transistors. The blue layer is the gate insulating layer (dielectric) whereas the green layer is the semiconductor layer. Conductive *source*, *drain*, and *gate* electrodes as well as the *channel length* **L** and *width* **W** are indicated.

The top-gate configuration is often preferred if the materials can be deposited in that order [50-53]. This is especially true for solution based amorphous or semi-crystalline polymer semiconductors. In top-gate configuration the sensitive semiconductor layer is protected by the dielectric layer. There is freedom to pattern the bottom source and drain electrodes with high precision. There are many options for top gate deposition, as it does not need as high resolution as the source-drain electrodes. Still, the positioning of the top gate relative to the transistor channel needs high precision.

The active channel forms in the semiconductor next to the dielectric interface. Figure 2 shows a *staggered* contact configuration where the semiconductor is placed *between* the source and drain electrodes *and* the dielectric. The injected charge has to travel through the semiconductor into the active channel, and this causes some bulk resistance. But the overlapping area between the channel and the S-D electrodes is large, compared to the small contact area with the electrodes and the channel in a co-planar case [40, 54, 55]. Larger area allows promoted charge injection from the metal to the semiconductor and the overall positive effect on current is larger than the small negative effect caused by extra bulk resistance and increased effective channel length [56-58].

Figure 3. shows also the overlapping area between the top and bottom electrodes. This area causes unwanted parasitic capacitance. Resolution and accuracy limitations in the large-area electronics processing can make this capacitance exceed the channel capacitance, which slows down the dynamic operation of the transistor [8, 58].

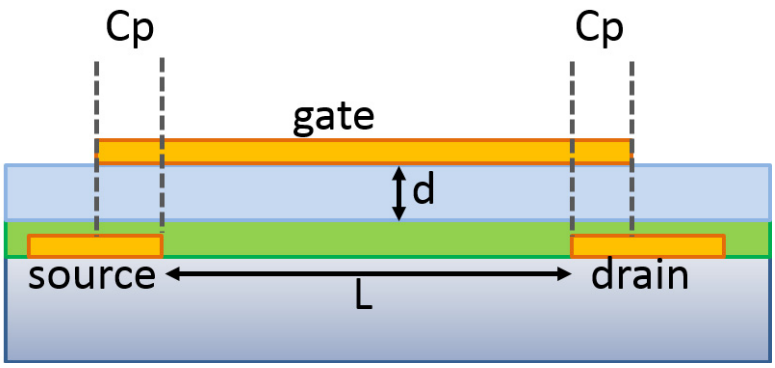


Figure 3. Side view shows the thin film transistor critical dimensions *channel length* **L** and *dielectric thickness* **d**. Overlapping areas cause *parasitic capacitance* **Cp**.

2.2 EFFECT OF DIMENSIONS ON TRANSISTOR PERFORMANCE

According to the field-effect transistor theory [59], the current flows between the biased source and drain electrodes and the current level is controlled by the gate to source voltage. Equation 1 shows the first order approximation of the *saturated drain to source* current I_{DS} when the *drain to source voltage* V_{DS} exceeds the *gate to source* voltage V_{GS} with the *threshold voltage* V_T subtracted V_{GS}-V_T. See Chapter 2.4 for an explanation of V_T.

$$I_{DS} \approx \frac{\varepsilon_r \varepsilon_0}{d} \mu \frac{W}{2L} (V_{GS} - V_T)^2 \qquad (1)$$

ε_r is the relative permittivity of the gate dielectric layer and ε_0 is the permittivity of vacuum. The charge carrier mobility μ is an inherent semiconductor material characteristic. Equation 2 shows the transistor current in the *linear* regime, where V_{DS} is small compared to V_{GS}-V_T.

$$I_{DS} \approx \frac{\varepsilon_r \varepsilon_0}{d} \mu \frac{W}{L} (V_{GS} - V_T) V_{DS} \qquad (2)$$

In printed electronics, the semiconducting materials have low mobility, which means low current levels. Equations 1 and 2 show that since the chosen materials have certain mobility μ and permittivity ε_r, and since the operating voltage should be reasonable, the only way to increase the current level is to modify the dimensions W, L, and d. Increasing the transistor channel width or decreasing the dielectric thickness increases the current. Decreasing the channel length (gap for the charge carriers to travel) increases the current but more importantly makes the transistor operation faster. When the transistor gate bias voltage is switched On and Off, the transistor channel is filled and depleted by moving charge carriers. The charge carriers are moved between

the source and drain by the electric potential difference V_{DS}. For shorter channels, the distance to move is shorter and the electric field that drives the movement is stronger. The transistor operating speed in the linear region can be expressed as the transfer frequency f_T in Equation 3.[60]

$$f_T = \frac{1}{2\pi}\mu\frac{V_{DS}}{L^2} \quad (3)$$

The switching time of the transistor has inverse square dependency on channel length L. As L can be large in printed structures, the switching speed can be small. Consequently, the channel should be as short as possible. The channel width, dielectric thickness, and permittivity have no effect on the operating speed in the ideal case.

2.3 ROLE OF DIELECTRIC

As discussed in Chapter 2.2 the dielectric thickness should be as small as possible. Naturally the materials have to possess good electrical properties but also be printable as even and smooth films. The leakage current increases exponentially as the dielectric gets thinner [61, 62]. The probability of defects like pinholes or dirt in the film grows. Defects can cause large leakage current or short circuits through the layer. The printed dielectric layer quality is limited by the material, processing method and environment.

To have low operating voltages and high current levels (Equations 1, 2) with reasonable transistor dimensions, one way is to choose a dielectric material with high permittivity [63]. This was tested in **II**. There is a risk that a high-permittivity material causes non-ideal dynamic behaviour. In some applications this is not a problem, but the most ideal and fast transistor operation is achieved with low permittivity materials [64].

A thick dielectric layer (whatever the permittivity) has many trapped charges which causes non-ideal transistor behaviour (see 2.5) [48, 65] (**I**). Sometimes the threshold voltage shift is desirable, and an intentional charge is introduced into the layer by a suitable material layer [66–68](**IV**). In special cases, like in air-gap transistor (**V**), the dielectric-air interface is easily charged, and can affect the device operation [69].

In case of multiple dielectric layers, the capacitances are added in series. In the air gap transistor presented in **V**, there is a thin protective dielectric layer with thickness d_{ox} on top of the semiconductor, and an air layer with thickness d_{air} that changes when pressure is applied to the structure (Figure 4). In the relaxed state, there is no bending of the structure, and the capacitance per unit area in Equation 2 is

$$C_A \approx \varepsilon_0 \frac{\varepsilon_r}{d_{air}\varepsilon_r + d_{ox}}, \quad (4)$$

where ε_r is the relative permittivity of the thin dielectric layer material and the permittivity of air is ε_0. When the foil is pressed, the distance d_{air} is changed due to the bending of the top substrate foil [70].

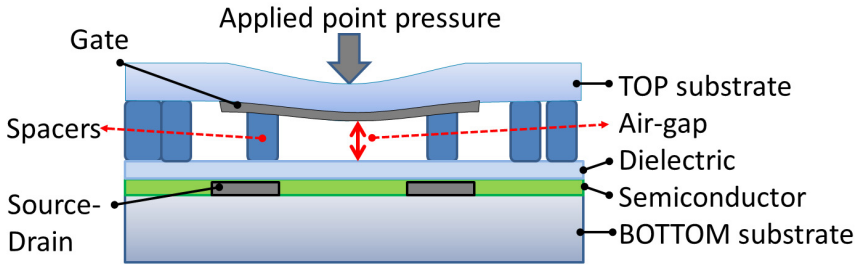


Figure 4. Schematic illustration of the device structure and operation principle. The applied pressure changes the gate distance from the channel. The displacement is seen in the source-drain current of the air-gap transistor.

One example of mechanical deflection d_{air} in the centre of a circular foil is

$$d_{air} \approx \frac{3(1-\gamma^2)P \times r^4}{16Eh^3}, \quad (5)$$

where P is the applied pressure, r and h are the radius and thickness of the foil membrane, and E and γ are the *Young's modulus* (for elasticity) and *Poisson's ratio* (for transverse axial expansion) of the foil material [71]. When pressure is applied, the air-gap decreases and the capacitive term increases, thus increasing the transistor's drain current in the *On*-biased set-up. In reality, Equation 5 gives only the deflection at the centre of the foil, so the true capacitive term should be calculated by integrating over the bent foil and the total active area. The effect of the applied pressure in transistor operation depends on the spacer structures around the foil, the bending characteristics of the foil, and the shape of the manipulator that applies the pressure.

2.4 TRANSISTOR CHARACTERIZATION AND EFFECT OF CHARGE TRAPPING

Transistor characteristics typically reported in the literature (including this thesis) are mobility, threshold voltage, *(current) On/Off*-ratio, and (inverse) subthreshold slope. A transistor test measurement is done by changing the gate voltage and by measuring the drain current for a fixed bias voltage on the drain and source electrodes. The *On/Off*-ratio is the drain current ratio between *On*- and *Off*-biased transistors. The V_{DS} is fixed at the operating

voltage, and V_{GS} is changed from maximum to minimum (or zero voltage). Thus the *On/Off*-ratio depends on the reported voltage range, and that relation actually gives us the "transconductance average" over the full control voltage range. Transistor transconductance g_m is defined as the change of drain current divided by small change in gate-source voltage in the normal operating voltage range (not near either fully *On* or fully *Off* voltages). For a transistor operating in active control voltage region with small voltage changes, the resulting transconductance values are higher than the "average" value given above. A high *On/Off*-ratio indicates high transconductance and is achieved typically only with small *Off*-current levels. These properties are needed in display backplane applications where low leakage is necessary to keep the pixel capacitors charged. The *saturation mobility* can be calculated using the slope of square root of the (absolute) drain current shown for example in Figure 15 in 4.2. The line used in the slope calculation intersects the x-axis at the *threshold voltage* V_T. The ideality of the transistor operation is evident in the figure: the square root slope should be linear if it follows the theory (Equation 1). In practice there is *contact resistance* [72], *charge carrier trapping* [73], and *field dependent mobility* [74] that cause deviation from ideal operation.

The choice to use saturation or linear mobility when reporting the effective mobility is up to the author, and often the larger value is reported. In [75] the linear mobility is preferred, claiming that the saturation mobility is less reliable for various reasons. For example the proportional effect of the contact resistance increases with increasing current levels. On the other hand with materials that have large contact resistance or contact barrier, the linear region can be distorted (showing as diode-like curves in the output plot). In that case the linear mobility measurement does not give useful information, but in the saturation region the *saturation mobility* value can still be measured. Any contact effects are embedded in the calculated values, and these effects decrease the effective mobility. In this thesis only saturation mobility is reported.

The thin film transistors made with materials that are compatible with LAE processes are inherently limited by charge carrier trapping [75, 76]. The semiconductor or the semiconductor-dielectric interface has trapping sites that can immobilize charge carriers with favourable energy. The origin of the traps can be grain boundaries, morphological or physical distortions, and impurities. The traps can be considered to be locations with low energy, where the charge can be immobilised and then released if enough energy is given by the external electric field. The traps distributed in the material have a continuation of different energy levels (energy band). Low energy (shallow) traps are easier and faster to fill and empty whereas high energy (deep) traps can hold the charge for a long time (even days). Charged deep traps (or fixed charges) cause a steady electric field that shows as *threshold voltage* in the transistor's electrical behaviour.

The trapping phenomenon can be tested by making fast and slow measurements. Some of the shallow (fast) traps are filled and emptied during the measurement sweep, and that makes a deviation from ideal, trap-free behaviour. The temporarily immobilised charges make a changing electric field, and that shows as hysteresis in the measurement sweep that goes in the forward and reverse direction. The trapping effect is most severe at the voltages below the threshold voltage when the transistor is just barely turning on. The *Turn On* voltage is the voltage where the "exponential" rise starts, and it is always smaller than the threshold voltage (in case there is no fixed charge). The *(inverse) subthreshold slope* S value shows how steep the logarithmic current rise I_{DS} is when the transistor is turning On (Equation 6). The value is reported as how much V_{GS} has to be changed in order to raise the drain current by one decade

$$S = \left(\frac{d\,(\log_{10} I_{DS})}{dV_{GS}}\right)^{-1} \qquad (6)$$

The number of traps can be estimated from the subthreshold behaviour [68, 77, 78]. Theoretical analysis by Stallinga [75] shows that the traditional equation for the exponential rise in the current at subthreshold voltage is valid only for traditional MOSFETs operating in *inversion*. This is however never the case with printed electronics. Still, the inverse subthreshold slope value is reported widely in the literature for printed or organic thin film transistors. The value permits comparing transistors and processes, even if it does not have the original physical meaning. In **I** the *relative estimate* (for comparison purposes) for upper limit of *interface trap density* N_T was calculated using Equation 7,

$$N_T = \left[\frac{qS\cdot\log(e)}{kT} - 1\right]\frac{C_{ins}}{q}, \qquad (7)$$

where C_{ins} is the *dielectric capacitance* per unit area, T is the *temperature*, k the *Bolzmann's constant* and q the *electronic charge* ($\log(e)$ is the conversion factor from *10 – based* to *natural logarithm*).

With slow measurements deep level trapping can take place. Bias stressing is a way to measure how much the trapping affects the transistor behaviour (**III**). The transistor gate is biased to a negative or positive high voltage for a long time (minutes, hours), and then the transistor curves are measured normally [79]. The amount of change in threshold voltage is reported.

2.5 CONTACT RESISTANCE

The contact resistance and the contact barrier between the electrode material and the semiconductor decrease the transistor's channel current and switching speed. Often the term contact resistance includes the effect of the contact barrier, especially if the effect is so small that the contact appears ohmic. The contact barrier comes in theory from the work function difference

of the materials, but in practice it is strongly related to the molecular contact of the actual interface [8]. For p-type organic semiconductors the *highest occupied molecular orbit* (HOMO) level aligns closely with the work function of gold. Gold is an inert, noble metal that is easy to process, so it is often used in test and reference structures. For real applications gold is often too expensive, so silver has been used widely, also as printable nanoparticle inks or organometallic compound inks. With silver the contact resistance can dominate the transistor's drain to source resistance. With proper selection of materials, treatment and processing the contact resistance and barrier can be decreased [8, 80, 81].

3 METHODS

This chapter introduces the processing equipment and methods, materials, and characterization equipment.

3.1 MATERIALS

The plastic substrate material that was mainly used was poly(ethylterephtalate) (PET) *Melinex ST504* from *Dupont Teijin Films*. In addition to PET plastic, polyethylene naphthalate (PEN), polyimide, and glass were tested as substrates to be used in laser ablation. In the first lamination tests *indium tin oxide* (ITO) coated PEN and silicon substrates with thermal oxide and lithographically patterned gold electrodes were used (**IV**).

Materials purchased from Sigma Aldrich were the etchant *ferric nitrate* ($Fe(NO_3)_3$), dielectrics *poly(methyl methacrylate)* (PMMA), *poly(methyl silsesquioxane)* (PMSSQ), *poly(4-vinylphenol)* (PVPh) and *poly(melamine-co-formaldehyde)* (PMF), a cross-linker for PVPh.

For the etching ink the antifoaming agent FoamStar SI2213 and triblock copolymer *poly(ethylene oxide)–poly(propylene oxide)–poly(ethylene oxide)* (PEO–PPO–PEO) were purchased from BASF. Comparison of etching was done with a commercial silver etching screen printable ink HiperEtch 09S Type 40 from Merck. The single wall carbon nanotube (SWCNT) semiconductor ink PR-010, the high permittivity dielectric PD-100 (blend of $BaTiO_3$ and PMMA), and the silver ink PG-07 for inkjet printing was purchased from PARU. The silver paste (IPC114) for the gate electrode screen printing was received from Inkron.

The Lisicon family products purchased from Merck were the semiconductors S1036 (**II**), SP300 (**I**), and the dielectric D320. The S1036 was polytriarylamine (PTAA), but the composition of the others is not public. The polymeric semiconductor ink (product GRAPE114) used in **III** and **V** was received from BASF. In **IV** earlier prototype versions of the same semiconductor was used.

The inkjet printed gate electrodes for the air-gap transistors (**V**) were created with DGP 40-LT-15C silver nanoparticle ink from Advanced Nano Products. Inkjet printed spacer structures for the same device were printed with a Norland Optical Adhesive NOA 89 from Norland Products Inc.

3.2 DEVICE PREPARATION

In small scale testing of new materials and material combinations, traditional laboratory processing methods like spin coating and metal evaporation through a shadow mask were used (**IV**). Pre-patterned substrates with lithographically processed thin metal electrodes were used when applicable (**I**). In **III** the thin 35 nm silver layer was deposited on the PET roll with a roll evaporation system. Rolls with already deposited thin metal films are commercially available.

3.2.1 ETCHING

Thin metal layer patterning can be done by direct etching, with a screen printed etchant. The process has only one printing and washing step. In **III** the printing of a special etching ink is presented. The etchant is added into a thermoreversible triblock copolymer, which forms a gel at elevated temperatures and at high concentrations. By carefully choosing the ink properties so that before printing it is just above the gelation point, it can be printed with high density screen mesh with comparably high resolution. Just after the printing the ink turns into a gel when it is heated briefly for 10 seconds under a 1 kW infrared lamp. Too much heating would dry the gel, and the etching would not take place. The substrate can be heated before printing, so that the gelation takes place immediately. There were four different screen printing mesh types tried, the details and results are given in section 4.1.1. Comparison with a commercial etchant is shown.

3.2.2 LASER ABLATION

Laser ablation of the thin metal layer on plastic substrates was studied with three different lasers. Picosecond pulse lasers from Lumera using 355 nm ultraviolet wavelength and 1064 nm infrared wavelength were tested. A femtosecond pulse laser from Quantronix with 800 nm wavelength was also tested. Initial shapes were patterned by evaporating 40 nm gold through a shadow mask. These initial electrodes were then cut into two (source and drain) electrodes by laser ablation (Figure 10). The laser spot size with the chosen optics was 15 μm in diameter, but it can be made smaller.

The UV laser wavelength was not absorbed by glass or PET substrate, and that was why UV laser was chosen for the final demonstration where PET was used. The patterning process with laser ablation causes the removed material to shoot upwards, making protruding edges [31] (Figure 11) and even spread some ablation residue into the surrounding area. The laser power and pulse repetition rate had to be carefully optimised, to ensure that the substrate is not damaged and that the quality of the edge is proper for thin film applications. Horizontal waviness of the pattern edge is not critical in low frequency systems, but vertical protruding edges can cause short circuits in stacked thin

film structures. The processing in vacuum [82] or with an extra resist layer on top of the metal did not improve the edge quality. The resist on top of the metal could be used to remove possible ablation residue. In our optimised process the ablation residue was negligible, so the extra resist layer was not used in the final process.

3.2.3 PRINTING

The laboratory scale printing tests were done using a *Schläfli Labratester* for semiconductor and dielectric gravure printing. Gravure plates were engraved with test patterns with different transfer volumes and cell dimensions. The transfer volumes were 3.2 - 17.5 ml/m^2. The printing speed was 4-8 m/min. The printed layers were dried in oven at 100°C for 2-20 min.

An EKRA E2 was used for flat-bed screen printing. Different screen types and resolutions (200-400 wires/inch) were tested, as was different temperatures and printing speeds. In **III** all the R2R printing and drying processes including gravure printing, screen printing, and the etchant washing step were done using the PrintoCent pilot printing line "ROKO" in Oulu (Figure 5). Only one printing unit was used at a time. After printing and drying, the rolls were rewound before the next printing step. The cylinder for semiconductor printing had 3.2-4.4 ml/m^2 and dielectric printing 50 ml/m^2 transfer volumes. The printing speed was 10 m/min and 8 m/min, respectively.

Figure 5. Photograph shows fully R2R processed transistors in the pilot printing line. Screen printed top gate electrodes show as white bars. Plastic substrate was 300 mm wide.

The top and bottom electrodes in **II** were inkjet printed with a Fujifilm Dimatix DMP2800 inkjet printer using a standard Dimatix cartridge with 10 pL nozzle size. The inkjet printing part of the air-gap transistor (**V**) was done with a PixDRO LP50 printer. The industrial multinozzle print head used for silver nanoparticle ink was SX30 with 10 pl nozzle size from Fujifilm Dimatix. To ensure optimal printing quality, the PEN foil was treated with O_2 plasma for 2 minutes at 300 mW/cm² before printing. The sintering of the printed pattern was done in oven at 150°C for 1 hour. The printing head for the *spacer* printing was KM512LHX with 42 pL nominal drop volume from Konica Minolta. The PEN substrate was treated by dip coating in 20 wt% diluted fluorosilane polymer Novec EGC-1720 from 3M in hydrofluoroether solvent. This ensured good wetting properties in order to get high aspect ratio *spacers*.

3.2.4 LAMINATION

Lamination tests in **IV** were performed with different substrates, materials, and configurations. First tests were done using rigid silicon substrates with lithographically defined source-drain electrodes. It was laminated on a flexible PET substrate which had an ITO gate electrode, and printed dielectric and semiconductor layers. The next step was to replace the silicon wafer with PET plastic substrate which had lithographically patterned gold electrodes (Figure 6a). Demonstration transistors, inverters, and ring oscillators were constructed with these flexible substrates. After successful demonstration, the fragile ITO coated substrate was replaced with another PET substrate, which had gold electrodes patterned by laser ablation (Figure 6b).

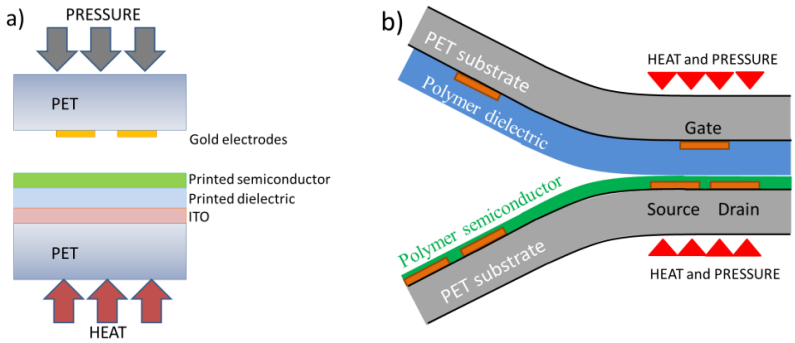


Figure 6. (a) Laminated TFT test circuits were done with ITO coated substrates. (b) Laminated structure with the ITO layer replaced by (laser) patterned metal

The lamination process is shown in Figure 6 and Figure 7. By introducing heat and pressure, the sheets make the contact between the polymer layers. In all lamination processes, two substrates with different processed layers were attached together on a hot plate by applying pressure (10–40 kN/m²) and heat

(140-160 °C) for 15–20 minutes. Reference samples without the lamination step were made by spin coating organic layers on Si/SiO_2 substrate, or by printing the dielectric and semiconductor on ITO-coated PET substrate and evaporating top source and drain electrodes. All tests were done manually with small sheets. The roll-to-roll process was not tested due to lack of compatible machinery with proper aligning accuracy between the features on top and bottom substrates.

The electrodes were visible through the polymer layers and the substrates, and could be aligned on top of each other. After lamination, glue was added on the substrate edges to fix the structure and make it more robust to handle.

A similar approach was used with the tactile sensor lamination in **V**. The only difference was that the top substrate had only the printed gate electrodes and spacer structures (see 3.2.3). The bottom substrate had the source-drain electrodes and printed semiconductor and dielectric layers (TFT structure in **III** without the gate). When these substrates were laminated together, the spacer structures attached the two substrates together. The spacers kept the substrate foils separated in designed areas, leaving air voids and thus forming air gap transistors.

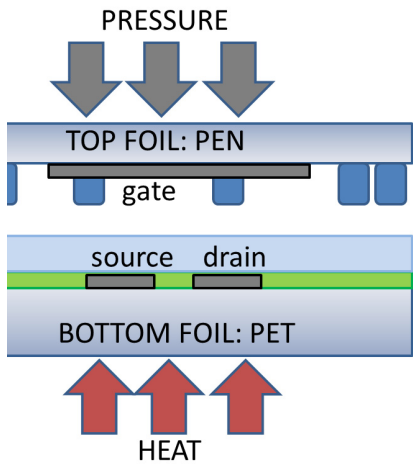


Figure 7. Air-gap transistor lamination concept.

3.3 CHARACTERIZATION

The printed layers were characterized using optical microscopy. Layer thicknesses were measured with a *Dektak 150* profilometer. The edge quality of the patterned metal electrodes was characterized with scanning electron microscopes (SEM) *Leo 1420* in **I** and *Zeiss Merlin* in **II**. *NT-MDT Scanning Probe Microscope* in contact AFM (atomic force microscopy) mode was used in **I**. The printing plates were characterized with *Nanofocus µSurf* optical profilometer. Capacitance (for dielectric constant calculation) was measured with *Novocontrol Alpha-A High Performance Frequency Analyzer*.

The organic field-effect transistors were characterized according to the *IEEE standard 1620-2004*. The current-voltage measurements were done *with a Keithley 4200 Semiconductor Characterization System*, whereas the capacitance measurements were done with a *HP 4192A LF Impedance Analyser*.

The field effect transistor's source-drain electrode contact resistance was calculated using the *transmission line method* (TLM) [23] in **I** and **III**. Transistors with different semiconductor channel length L were measured. From the results the contact resistance at a certain gate voltage can be interpolated (Figure 12).

The applied force on the pressure sensor structure in **V** was measured with a laboratory scale, using differential reading from unstressed starting value divided by *acceleration of gravity g* (*F=mg*). The force was divided by the estimated area of the manipulator probe head, giving the applied touch pressure in (kilo)Pascals kPa. The current through the sensor transistor was measured continuously during the pressure application, and the change in current as a function of change in pressure gives the sensitivity of the sensor.

4 RESULTS AND DISCUSSION

The results are shown in the order of transistor processing. First the electrode layers, then the semiconductor and dielectric layers, and finally the lamination methods are presented. The effect on the electrical performance is explained and the main transistor and circuit results are shown in the relevant chapters. The main results are shown and different methods are compared and discussed.

4.1 ELECTRODES

The R2R compatible *direct etching* and *laser ablation* methods for thin metal film patterning were studied in **III** and **IV**. The goal was to achieve thin, smooth, and highly conductive electrodes with high patterning resolution.

4.1.1 R2R ETCHING

After trials, a working composition for the etching ink was found: 46 wt% of etchant, 22 wt% of triblock copolymer, and 0.3 wt% of antifoam agent, all in water solution. The etching works properly within the short available time in the continuous R2R process, removing the thin metal layers completely. The etching speed was not studied, but the metal was etched so fast that there is room to increase the metal thickness. The printing resolution is limited by the screen printing mesh. Patterns with 50-55 μm line and gap widths were demonstrated with a sheet screen printer. In rotary screen printing the screen mesh has to be strong and thick, which limits the achievable resolution to ~100 μm. Figure 8 shows how the mesh affects the edge quality. Lower resolution shows as jagged edges in the case of rotary screen printing.

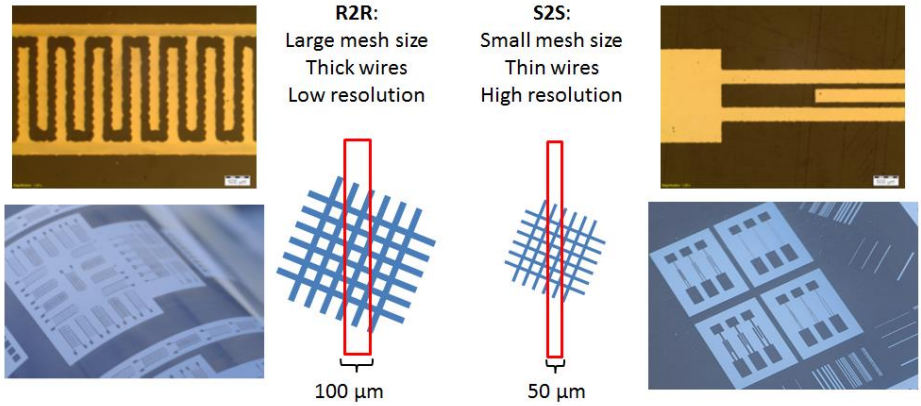


Figure 8. Images of screen printing results with different screen mesh sizes. Rotary screen printed results are on the left, and sheet screen printed on the right.

Studying the microstructure of the edge with *scanning electron microscope* including *energy dispersive x-ray spectroscopy* (SEM/EDS) showed that the etchant affected the first few microns of the edge area of the remaining metal (Figure 9). The thin metal was agglomerated into connected nanoparticles, which could grow into large crystals. These crystals could cause problems in thin film applications.

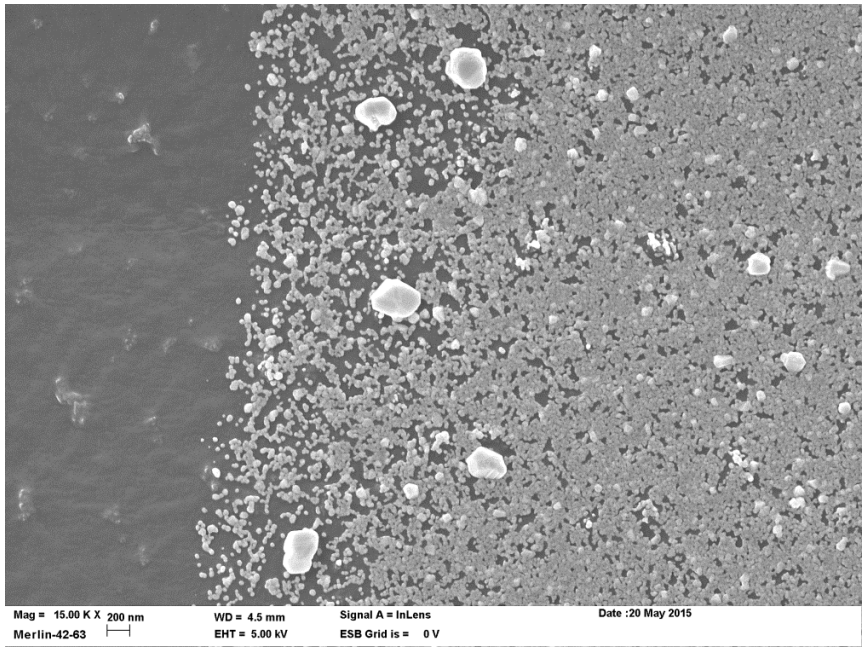


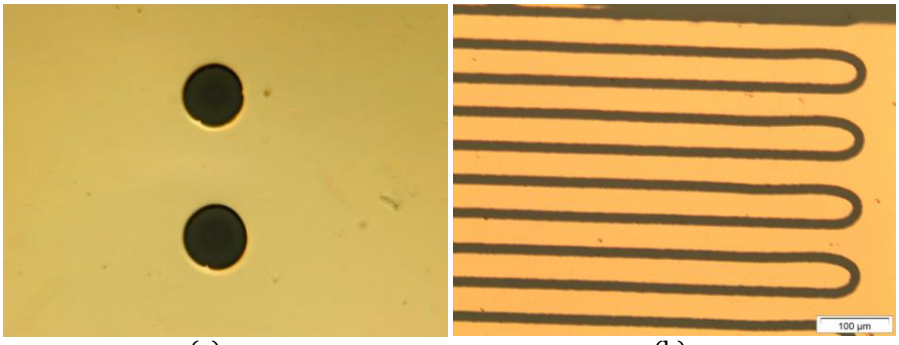
Figure 9. SEM image of the edge of the etched metal. Some of the silver has agglomerated into large silver crystals.

Traditional etching ink from Merck was tested for comparison. The details are not shown in the paper, but the main results are given here. The traditional ink needed comparably higher temperature and longer heating time (4 successive heating units compared to 1 in the R2R system) and the etching residual material was difficult to wash away (manual scrubbing with wet cleanroom cloth). The printed etching paste line width was larger than the pattern opening in the mesh due to ink spreading. Consequently the rotary screen printing of the traditional ink over-etched the metal by 40 µm, when the gel-etch over-etched only by 13 µm. In sheet screen printing the over-etching with the gel-etchant was only 2-3 microns.

The R2R etched silver electrodes were used in fully R2R manufactured transistors, and in air gap transistors. The electrical results are compared in Chapter 4.5.

4.1.2 LASER ABLATION

The etched line and gap widths are too large for most electronic applications. In **IV** a thin gold film (40 nm) was patterned by scanned laser ablation. Other metals could be patterned in the same way. Figure 10a shows a circular ablated area where metal is removed, done with a single picosecond UV laser pulse with 15 mW energy. Figure 10b shows the transistor channel that is formed by multiple similar pulses scanned across the thin metal layer at 50 kHz pulse rate and at 200 mm/s scanning speed. These structures were used in the laminated transistors as the source and drain electrodes (electrical results in Figure 15 in Chapter 4.2).



(a) (b)

Figure 10. Microscope images of laser ablated patterns in thin gold film. (a) Single ablated spot is 15 µm in diameter with the chosen optics. (b) Ablated serpentine pattern forms the source-drain electrodes for TFT. The gap is 16 µm wide.

The patterned edge was mostly flat, but there were loose metal film edges seen in the profilometer, SEM, and AFM measurements (Figure 11). The tallest measured edge defects were less than 200 nm high. They prevent the use of very thin layers in stacked devices.

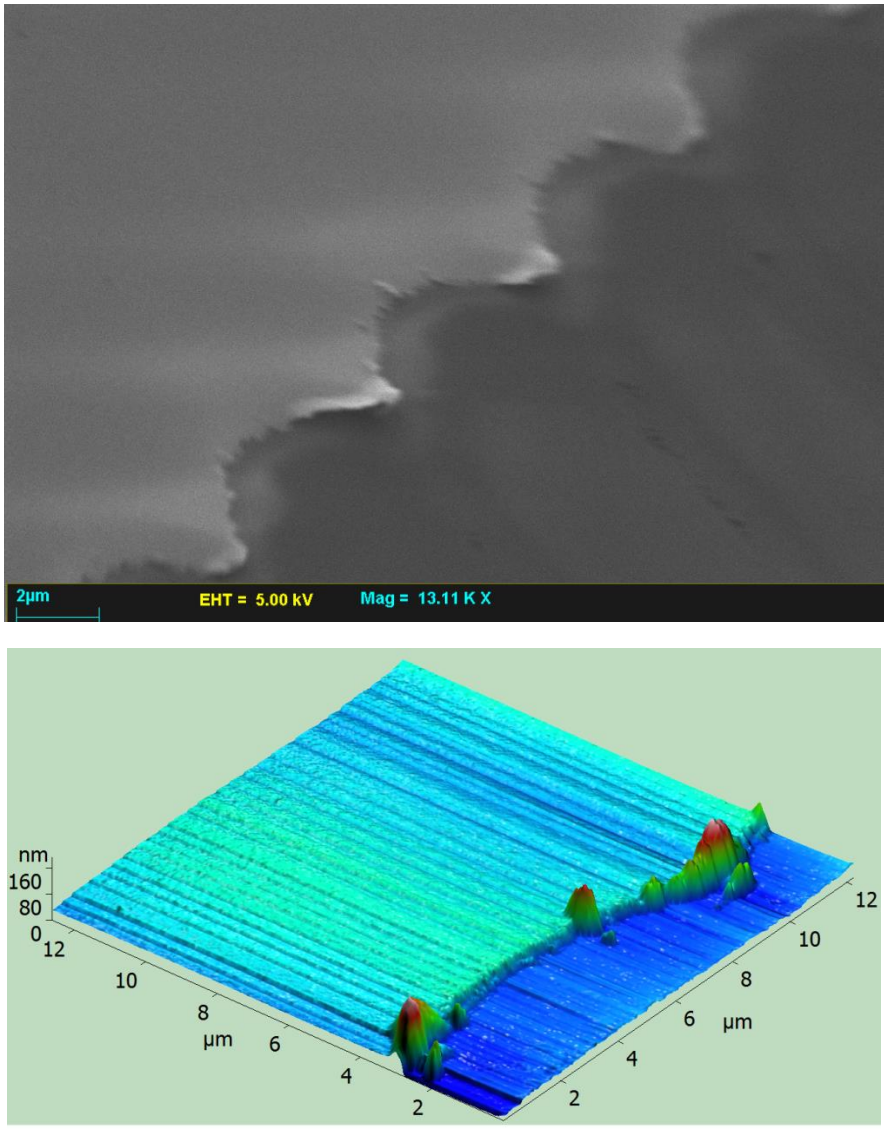
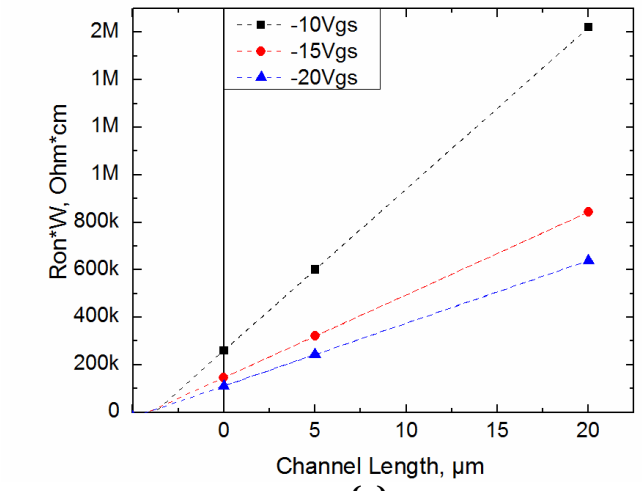


Figure 11. Scanned images with SEM (top) and AFM (bottom) show edge defects.

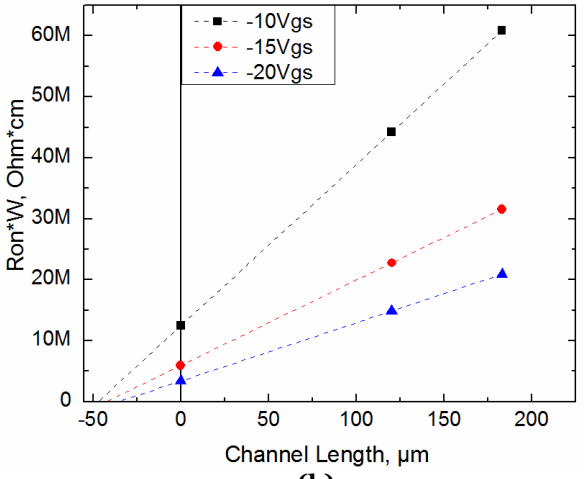
The scanning speed of the laser is suitable for roll-to-roll processing, if only the patterns needing high definition are patterned (for example transistor channels). Larger patterns could be patterned for example by a printed etching method or by printing metal inks.

4.1.3 CONTACT RESISTANCE OF GOLD AND SILVER ELECTRODES

The contact resistance between the lithographically etched gold and the semiconductor in **I** was interpolated from measurements plotted in Figure 12a. The contact resistance was 100 kΩ·cm with -20 V gate bias. In **III** with the R2R etched silver electrodes in contact with the semiconductor, the contact resistance was measured to be 3 MΩ·cm with -20 V bias (Figure 12b). In our other printed transistor work silver also exhibited more than 20 times larger contact resistance than gold. However, in later work [20, 83] a chemical treatment (using Merck Lisicon M001) on the metal electrode contacts was studied on *etched, inkjet,* and *gravure* printed nanoparticle silver electrodes, and similar enhancement and results were achieved as presented by Grau *et.al.* [9]. Chemical treated silver electrodes can have only 3-5 times larger contact resistance than gold. Silver is cheaper than gold in large area electronics, and there are many silver inks commercially available.



(a)



(b)

Figure 12. Contact resistance interpolation plots using the TLM method. (a) TFT with gold electrodes from **I**. (b) TFT with silver electrodes from **III**. Different semiconductors were used, and there was no contact enhancing treatment.

4.2 SEMICONDUCTOR LAYER AND ITS EFFECT ON TFT PERFORMANCE

Semiconductor inks have often a low solid content to solvent ratio, ca. 1%. For some semiconductors, the poor solubility of the solids restricts the ink thickness and choice of solvent. Printing a patterned layer with a certain thickness is therefore challenging. In this work the polymeric semiconductors SP300 and PTAA in **I** and **II** were used as received. In **III**, **IV,** and **V** the semi-crystalline semiconductor was dissolved in solvents and an optimal ink for printability and electrical characteristics was found.

In **I** thin semiconductor films were gravure printed on top of a plastic substrate that featured patterned metal source and drain electrodes. The wetting difference between the substrate and electrodes caused uneven film thickness in the open areas around the metal electrodes. The interdigitated electrode structure was sufficiently dense (10-25 μm line width) that the ink did cover its electrodes and channel areas between the electrodes evenly. Consistent transistor behaviour showed that the film formed evenly in the active region. In **I** an amorphous polymer was used, and there seemed to be no difference between printing along or orthogonally to the transistor channel. The semiconductor film was printed using 10 - 80 nm thicknesses and the best electrical results (*mobility* and *On/Off ratio*) were achieved with the thickest 70-80 nm layers. In printed polymer transistors the optimal printed layer thickness is typically 50-100 nm [84, 85, 57]. Electrical results are shown in 4.3.

In **II** a polymeric semiconductor or carbon nanotube ink was used. Printed or drop casted carbon nanotube semiconductor ink provided uneven layers and poor electrical characteristics. Additional ink treatments (e.g. sonication at low temperature) suggested by the manufacturer did not help. The reference material, a polymeric semiconductor PTAA, was drop casted and worked as expected (Figure 19).

Semiconductor materials in **I** and **II** could be printed and processed in normal laboratory environment in air. In **III, IV,** and **V** a semi-crystalline semiconductor was used. It was sensitive to air and the deposited films had to be covered with the next layer as soon as possible (within minutes) to render the structure insensitive to air. In **IV** the materials were mainly spin coated. The films were smooth and even. The electrical behaviour improved when a laminated structure was used when compared to spin coated references (Figure 13).

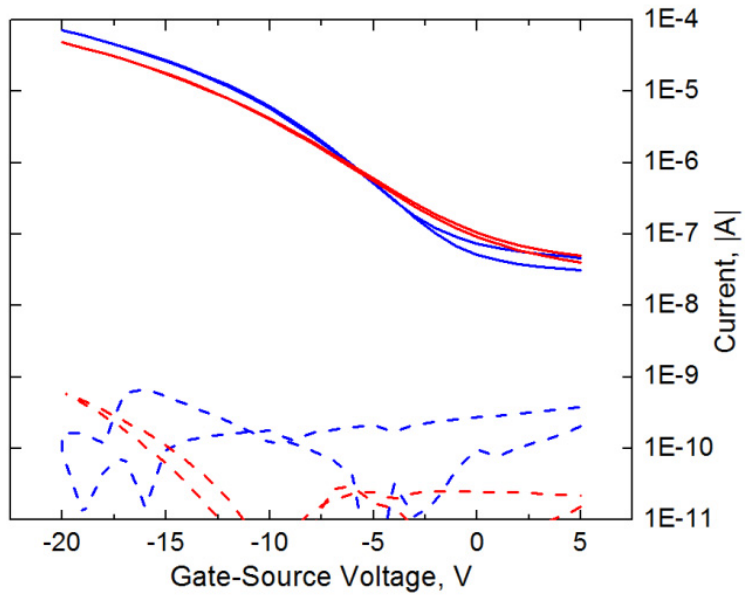


Figure 13. Comparison of the transfer characteristics of spin coated (red) and printed (blue) transistors. The absolute drain current is shown as a solid line whereas the gate leakage current is shown as a dashed line. V_{DS} was -20 volts in both.

The semiconductor in **III** was gravure printed, and also in this case there was an enhancement in performance compared to the spin coated device (transistor results are shown in Chapter 4.5). The reason for the improvement could be shear forces involved in the lamination and in the printing. The favourable pressure and temperature in the lamination (**IV**) might enhance molecular packing and film formation, and the shear forces that occur during printing might provide favourable conditions for crystalline film formation (Figure 14) [39, 86].

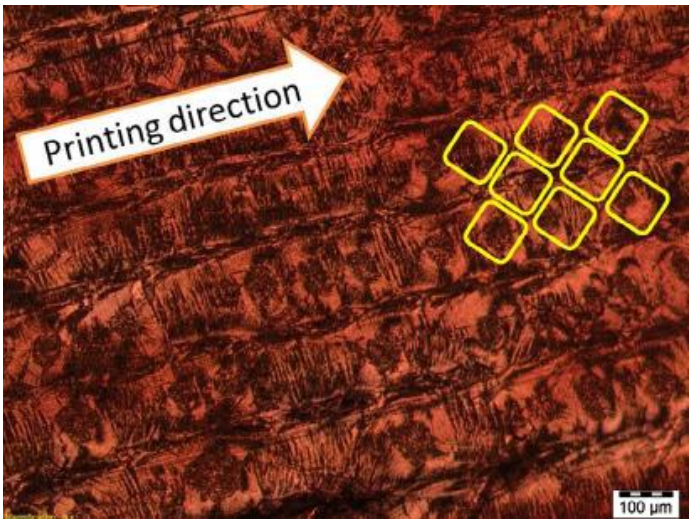


Figure 14. Semi-crystalline film formation is affected by the printing cylinder cell pattern. Yellow shapes mark the engraved gravure cell shape, size and spacing (100 µm wide cells with 100 lines/cm line spacing).

The laminated and printed transistors had long lifetime in air (Figure 15). Figure 16 shows the field effect mobility of a laminated transistor that was measured occasionally over a period of 6 years. There is little degradation in mobility (only 5% projected decay in 10 years), but there is sensitivity to humidity that is common in polymer semiconductors [83].

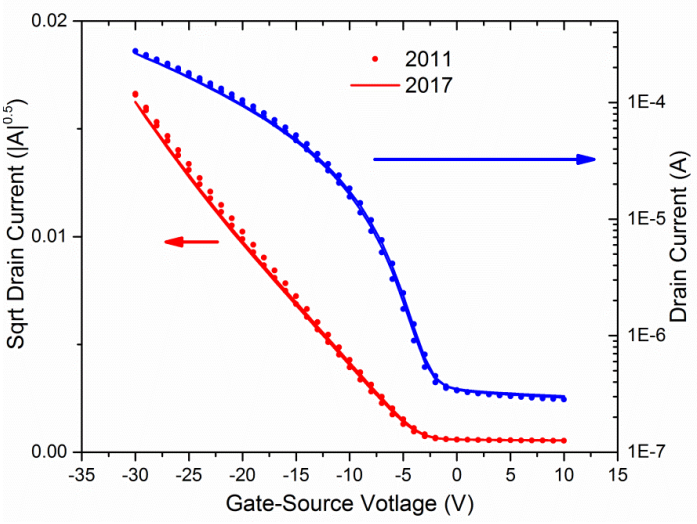


Figure 15. Transistor transfer characteristics show little change after storage in air. Dots represent values measured 3 months after production whereas solid lines represent values measured 6 years after production.

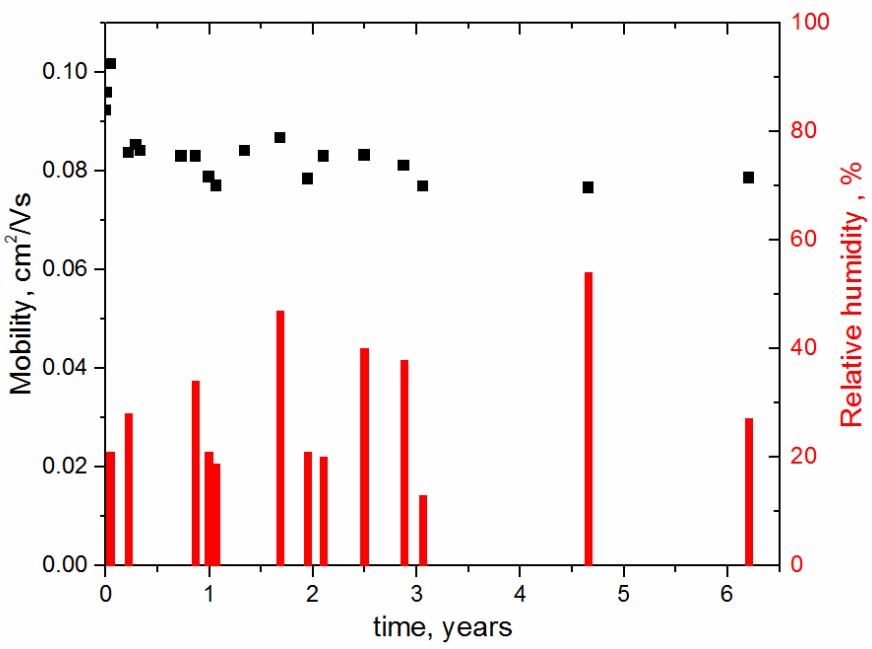


Figure 16. Transistor field effect mobility (dots) over a period of 6 years, and relative humidity values (bars). There is a dip in the values measured during the dry winter months.

4.3 DIELECTRIC LAYER AND ITS EFFECT ON TFT PERFORMANCE

Overall, the printability of the dielectric materials was good in all presented cases. The edges of the printed patterns were precise, and followed the mechanical limits of the gravure printing patterns. The b*arium titanate* dielectric blend presented in **II** had microscopic particles inside the printed film (Figure 19), otherwise the dielectric films were visibly smooth and pin hole free.

In **I** the thickness of the dielectric was taken to the lower limit. The fully processed transistors of different dielectric thicknesses were measured and the results compared. The role of trapped charges in the bulk dielectric was evident, as the threshold voltage and subthreshold slope decreased when the dielectric was thinner (see Figure 17 and Table 1).

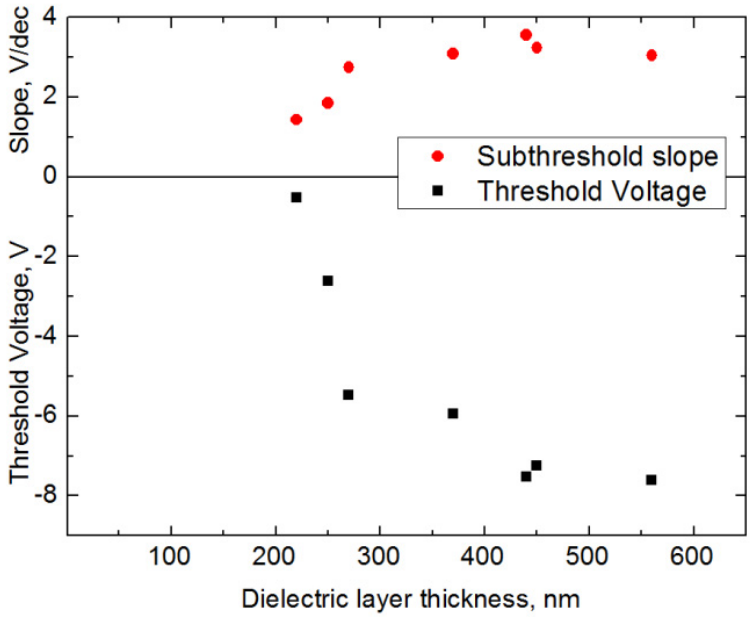


Figure 17. Printed transistor subthreshold slope (red) and threshold voltage (black) plotted versus the thickness of the printed dielectric.

Table 1. Transistor characteristics of a printed sample series with different dielectric thickness. The semiconductor thickness measurement was difficult, so only rough estimates based on the measurements are presented.

Dielectric thickness, nm	**560**	**440**	**450**	**370**	**270**	**250**	**220**
Semiconductor thickness, nm	**~10**	**~25**	**~30**	**~40**	**~50**	**~70**	**~80**
Mobility, cm²/(Vs)	**0.01**	**0.02**	**0.02**	**0.03**	**0.02**	**0.04**	**0.03**
Threshold voltage, V	**-7.6**	**-7.5**	**-7.2**	**-5.9**	**-5.5**	**-2.6**	**-0.5**
On/Off ratio	**4 000**	**1 400**	**2 200**	**6 800**	**4 000**	**7 500**	**6 500**
Subthreshold slope, V/dec	**3**	**3.6**	**3.2**	**3.1**	**2.7**	**1.8**	**1.4**

Transistors with 250 nm dielectric thickness were used in low voltage operation tests. Figure 18 shows that an inverter constructed from two transistors has gain even at -5 V supply voltage.

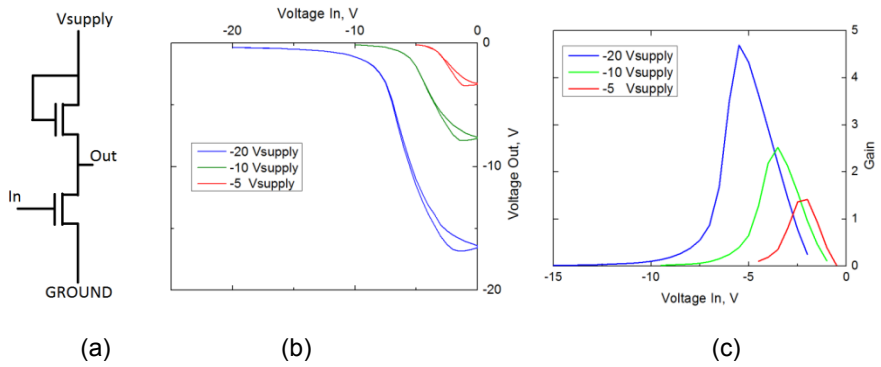


Figure 18. The thin dielectric transistors in a) diode connected inverter circuit worked at low voltages, shown by b) output swing and c) corresponding voltage gain values at V_{SUPPLY}= -20 V, V_{SUPPLY}= -10 V and V_{SUPPLY}= -5 V.

The choice of dielectric was important. When the low permittivity (k=2.2) dielectric D320 was replaced with PMMA that has a typical polymer permittivity (k=3.3-3.7), the results were poor. The dielectric characteristics concerning the transistor operation were good (low threshold voltage, subthreshold slope, and leakage current), but the mobility was low. Furthermore in **II** a high permittivity dielectric was used, and the same kind of low mobility was seen. The semiconductors SP300 and PTAA in these tests were prone to field effect mobility degradation when a high permittivity dielectric was used (see explanation in Chapter 2.3). Semiconductors in **III-V** did not suffer from this phenomenon with PMMA printed on top. In those papers the PMMA worked well as gravure printed dielectric layers, when the thickness exceeded 600 nm. Thinner films as with D320 in **I** could not be printed reliably.

A high-permittivity dielectric blend was characterized in **II**. The measured permittivity k was 11, as promised by the supplier. When an electric field exceeding 0.3 MV/cm was applied across the dielectric, a hysteretic behaviour was experienced. This could come from the ferroelectric characteristic of barium titanate in the blend [87]. In the transistor testing, the fields were kept below 0.1 MV/cm. Aside from the mentioned mobility degradation, the transistors made with the blend and the PTAA semiconductor showed similar characteristics as with low permittivity dielectrics, when scaled with the permittivity (Figure 19b). They also showed similar gate bias stress behaviour as other organic transistors made from different materials [83]. Consequently, at low field strengths the dielectric blend material can be used in organic transistors if high gate capacitance is needed.

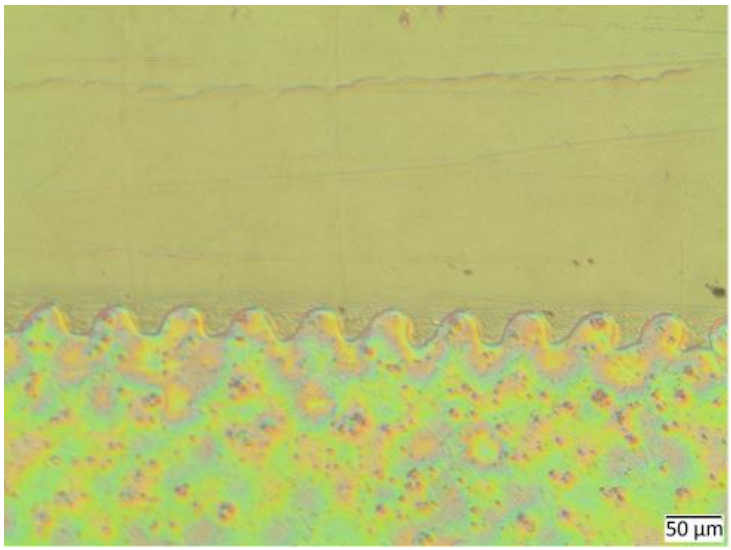
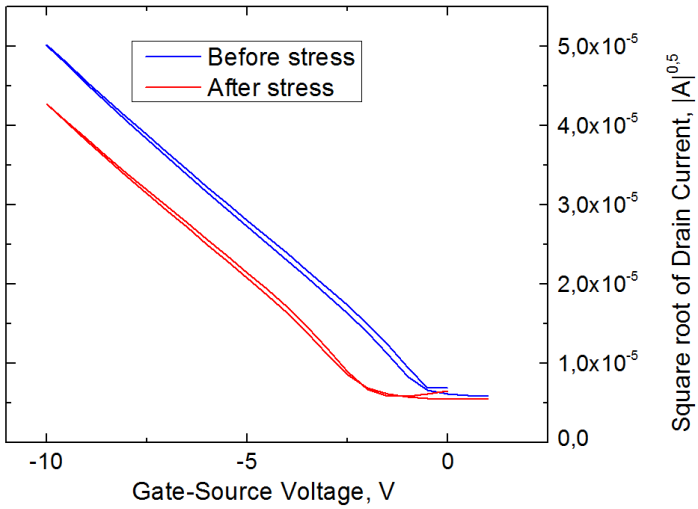


Figure 19. (a) Optical microscope image shows that the gravure printed PD100 dielectric layer has microscopic particles in it. The printed pattern edge follows the jagged pattern edge of the printing cylinder. Printed CNT semiconductor layer shows as dark haze in the top part of the image. The printed film was too thin for transistor use.



(b) Transistor made with PD100 dielectric and PTAA semiconductor shows typical stress behaviour: the threshold voltage shifts slowly towards the negative direction for negative gate bias voltage. Total stressing time was 1500 seconds.

The ring oscillator presented in **IV** was constructed with *diode connected* load transistors. The sizes and threshold voltages of the drive and load transistors are designed so that the inverter operation is possible. The drive transistors in

the circuit had -10 V threshold voltages. It was achieved by choosing PVP:PMF as dielectric. Getting a positive threshold voltage for the diode connected load transistor was not straightforward. A double layer had to be constructed. A positive threshold voltage of 20 V was achieved by adding a thin pMSSQ layer on top of the PMMA layer. Unfortunately the electrical properties of the layer were unstable. The favourable threshold voltages were present only for a limited time, during which the ring oscillator operation was tested. The inverter gain was 9.5 at maximum, and the ring oscillation frequency was 31 Hz at -45 V supply voltage.

4.4 LAMINATION

Laminated transistors are presented in **IV** and **V**. In both cases, the adhesion of the laminated surfaces was imperfect. They were easily delaminated if the structure was bent. This is understandable, when considering the thin layers used in **IV** and the small contact area of the spacers used in **V**. The adhesion could be enhanced by using extra glue with similar thickness outside the active transistor areas. Also thinner substrates make differential forces smaller when structures are bent. In **V** extra spacer frames were printed around active regions to enhance the adhesion between the layers (Figure 20 in 4.5). The lamination temperature and pressure was critical, as spacers had to be melted somewhat for the bonding to occur, but not so much that the spacer height is overly reduced.

For both laminated transistors in **IV** and **V**, a different gluing material outside the active region would be beneficial. The glue would help fixing the substrates together, and the active areas would not have to contribute so much to the overall rigidity of the structure. Therefore bonding of the laminated active layer could be done at an optimal temperature. One must keep in mind that lamination works only with suitable material combinations, and with materials that withstand the heat or pressure during lamination.

The effect of lamination on transistor performance is presented in chapter 4.2 and air-gap transistor results are presented in chapter 4.5.

4.5 AIR-GAP TRANSISTOR AS TACTILE SENSOR

Figure 20a shows a laminated air-gap transistor matrix. The zoom-in Figure 20 (bottom) shows the R2R (**III**) etched electrodes with transparent printed active layers on the bottom foil, and spacer and gate foil laminated on top. The flexible top substrate allows the use of air-gap transistors as tactile pressure sensors. The spacers (black dots in Figure 20 bottom) were distributed evenly across the active transistor area. The idea was to make a general process without an accurate alignment step. Spacers could be positioned with high

accuracy around the channel areas, making the air-gap across the transistor channel sensitive to tactile input.

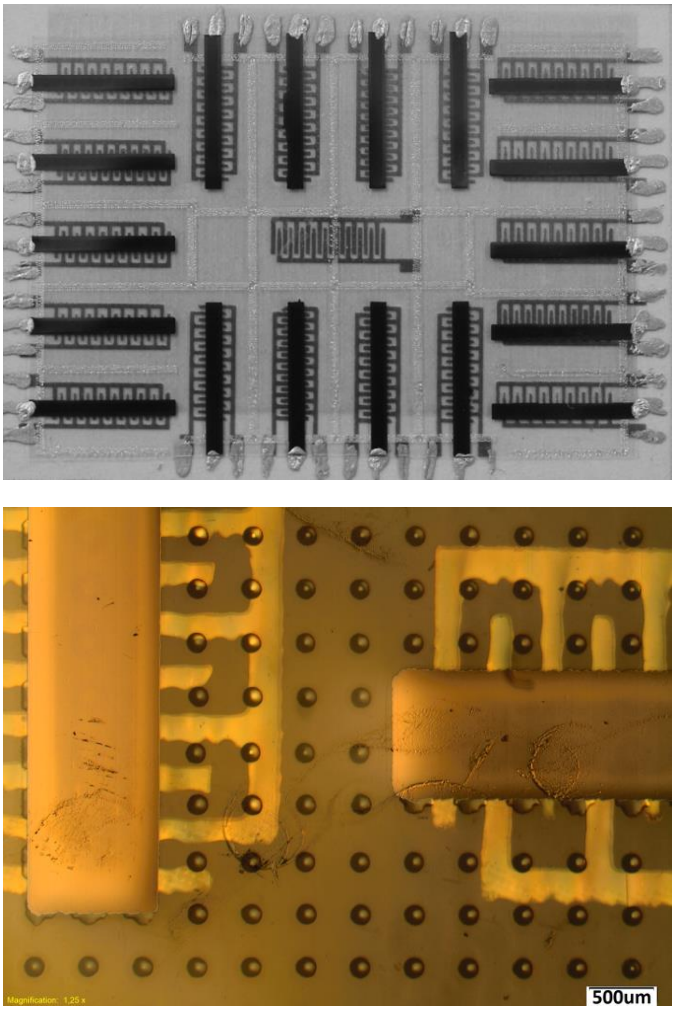


Figure 20. (top) Final demonstration matrix with laminated top and bottom foils. (bottom) Microscope image shows finger electrodes on the bottom, spacer dots in the middle, and the gate on the top through the transparent top foil. Printed polymer films are transparent.

The electrical results of a fully R2R processed transistor (**III**) *without the air-gap* are presented in Figure 21 for comparison. Results of an air-gap transistor are shown in Figure 22. As expected, the large air gap makes the gate field effect small, which causes small currents compared to similar reference

transistor without the air-gap. The transistor drain current changes, when a strong pressure (>4 kPa) was applied on the top (gate) substrate.

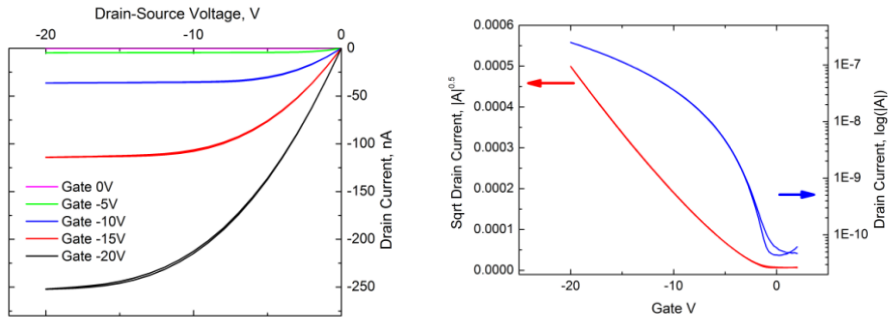


Figure 21. Measured current-voltage characteristics of a R2R processed transistor (reference transistor, no air-gap). Forward and reverse sweeps in both (a) output and (b) transfer plots show little hysteresis. In (b) the transfer characteristics were measured at $-20V_D$. The plot of the square root of the absolute drain current is shown in red.

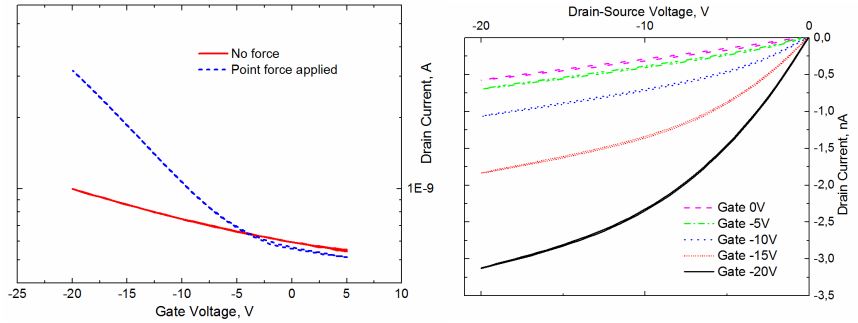


Figure 22. Pressure sensitive (air-gap) transistor characteristic plots. a) Transfer curve ($I_{Drain\text{-}Source}$ vs. V_{Gate}) for two applied forces (no force, strong >4 kPa force). b) Output curve of the same transistor with similar applied strong point force.

Figure 23 shows the transistor current levels over time when different point pressure values were applied in steps. The response was repeatable.

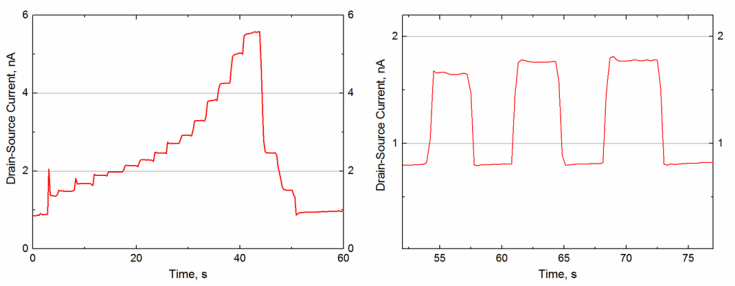


Figure 23. Examples of two pressure sensitive laminated OTFTs with different point pressures applied to the top layer. In (a) the pressure was applied in increasing and decreasing steps, and the resulting change in transistor current is shown. In (b) also repetitive pressure application and release indicates repeatability in transistor response.

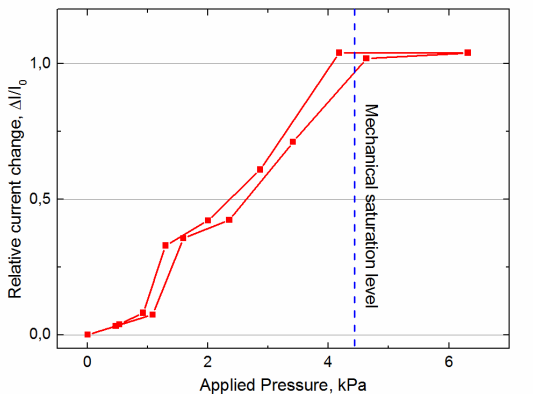


Figure 24. Change in relative TFT current level as a function of applied pressure (from unstressed level up and back). Connecting lines show the successive measurement points of the measurement cycle. There is hysteresis in the sensor behaviour when forward and reverse measurement sweeps are compared.

Figure 24 shows the relative current change from a starting unstressed value for a range of applied pressure. The measurement range of the cell was from 0.4 kPa to 4.4 kPa. The sensitivity of the cell was 0.4 ± 0.1 kPa^{-1}. The working range and sensitivity can be tuned by adjusting the spacer spacing or height, foil thickness, and elastic properties of the spacer or the foil materials. There is a small amount of hysteresis in the sensor behaviour when forward and reverse measurement sweeps are compared. This could come from both

mechanical slowness of the bending substrate and electrical hysteresis in the air gap transistor. The interface between the dielectric and air is easily charged, which is detrimental in a tactile sensor application. On the other hand this could be exploited in (gas) sensing applications by using a selective material in the air-dielectric surface [47, 69, 88].

5 SUMMARY

This thesis shows some critical LAE processing challenges, and introduces new ways to overcome them. Some traditional processing techniques are used in a new way. Commercial and prototype materials are used in the testing. Characteristics of the printed electronic device, mainly the thin film transistor, are reported. The focus and goal was on using roll-to-roll (R2R) processes, and processes that are compatible with large area mass production.

I shows that modern polymer semiconductor and dielectric materials are suitable for gravure printing in thin films. The demonstration transistor inverters operating below 5 volts were realized. In **I**, two transistor dielectrics with low permittivity were compared. In **II**, also a high-permittivity transistor dielectric was tested and characterized with a polymer or carbon nanotube semiconductor.

In **III**, thin film transistors were printed and processed using *roll-to-roll* processes. Thin metal film was deposited on the substrate by R2R evaporation and patterned using a special *screen printed etchant*. The etched electrode quality was suitable for transistor applications. Other layers were gravure and screen printed.

In **IV**, the transistors were made using different kinds of lamination processes. Laminating together two separate substrates allows new material combinations and new electrode options for both sides of the device. Laminated transistor had very good lifetime. Still, the lamination process works only with certain materials and the adhesion has to be improved. Use of laser ablation was studied as a high definition patterning method. Electrode structures with proper edge quality were realized and used in the laminated transistor demonstration.

As an application example a pressure sensitive air-gap transistor matrix was realized in **V**. The device included the R2R processed transistor structures from **III**, inkjet printed spacer and top electrode structures, and the lamination method from **IV**. The sensor structure is easy to modify, so arbitrary sensing shapes with different sensing range can be processed. In this demonstration simple structures were realized and tested as tactile sensors. Other possible applications for the lamination method could be e.g. electronic labels and signs with a display element and a backplane lamination step (could simplify the process), smart cards, and sensor applications [47].

6 CONCLUSIONS

Three general observations about the present situation and outlook for the high throughput low-cost LAE electronics are:

1) **Commercially available polymer materials are good for real applications**

The best materials are commonly sold exclusively to large customers only, and only older versions are available for small customers or research groups. The investigated commercial active polymer materials were state of the art when the work started (2011). At that time a common problem with polymer semiconductors was air-stability. Printing of the materials was tested and the demonstration transistors worked in thin films in low voltage circuits. The lifetime of even old versions of the material was good. With current materials (2018) the mobility and lifetime has improved. Optimized semiconductor-dielectric combinations can be purchased and used as received.

2) **Processing possibilities are plentiful**

The LAE application developer can choose from many different processing possibilities depending on performance, substrate, or area needed. Traditional processes can be combined with new large area electronics methods to reach better results. Roll-to-roll or sheet-to-sheet processes are available, and options should be carefully considered. Parts of the process can be made with different levels of technology. Some parts can be purchased directly, like substrate rolls with a thin metal layer on top. Some parts of the process might be done in different locations as a service, for example laser patterning of the fine details into the metal electrodes. *Direct etching, laser ablation, and lamination techniques reported in this thesis add to the many mass production possibilities* already available in the field and may provide a crucial advantage for device performance and manufacturing efficiency for certain material combinations.

3) **Overall processing quality is the bottleneck**

Typically the bottleneck is in the processing technology. For example printing machines designed for graphic printing cannot provide the repeatability needed for real electronics production. To reach proper operational level, the processing equipment should be designed for the job. Processing should take place be in a regulated clean room standard environment. The substrate quality has to be high. A single defect or particle can ruin a circuit. In an optimal situation the process steps should be monitored in-line to get the repeatability needed for production. These challenges can be tackled if the

total process is planned ahead without compromising the quality in any processing step.

REFERENCES

[1] A. C. Arias, J. D. MacKenzie, I. McCulloch, J. Rivnay, and A. Salleo, "Materials and applications for large area electronics: solution-based approaches", *Chemical reviews*, vol. 110, no. 1, pp. 3–24, 2010.

[2] C.-Y. Lo, J. Hiitola-Keinänen, O.-H. Huttunen, J. Petäjä, J. Hast, A. Maaninen, H. Kopola, H. Fujita, and H. Toshiyoshi, "Novel roll-to-roll lift-off patterned active-matrix display on flexible polymer substrate", *Microelectronic Engineering*, vol. 86, no. 4, pp. 979–983, 2009.

[3] N. Choi, "Metal Oxide Thin Film Transistors on Paper Substrate: Fabrication, Characterization, and Printing Process", *Theses and dissertations. Paper 1245, Leigh University*, 2012.

[4] E. Menard, M. A. Meitl, Y. Sun, J.-U. Park, D. J.-L. Shir, Y.-S. Nam, S. Jeon, J. A. Rogers, and others, "Micro-and nanopatterning techniques for organic electronic and optoelectronic systems", *Chemical Reviews-Columbus*, vol. 107, no. 4, pp. 1117–1160, 2007.

[5] A. Nathan, A. Kumar, K. Sakariya, P. Servati, K. S. Karim, D. Striakhilev, and A. Sazonov, "Amorphous silicon back-plane electronics for OLED displays", *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 10, no. 1, pp. 58–69, 2004.

[6] J. Noh, M. Jung, K. Jung, S. Lim, G. Lee, V. Subramanian, A. D. Leonard, J. Tour, and G. Cho, "Modeling of printed single walled carbon nanotube thin film transistors for attaining optimized clock signals", *Journal of Applied Physics*, vol. 108, no. 10, pp. 102811–102811, 2010.

[7] G. C. Schmidt, D. Höft, K. Haase, M. Bellmann, B. Kheradmand-Boroujeni, T. Hassinen, H. Sandberg, F. Ellinger, and A. C. Hübler, "Fully printed flexible audio system on the basis of low-voltage polymeric organic field effect transistors with three layer dielectric", *Journal of Polymer Science Part B: Polymer Physics*, vol. 53, no. 20, pp. 1409–1415, 2015.

[8] J. Chang, X. Zhang, T. Ge, and J. Zhou, "Fully printed electronics on flexible substrates: High gain amplifiers and DAC", *Organic Electronics*, vol. 15, no. 3, pp. 701–710, 2014.

[9] G. Grau and V. Subramanian, "Fully High-Speed Gravure Printed, Low-Variability, High-Performance Organic Polymer Transistors with Sub-5 V Operation", *Advanced Electronic Materials*, vol. 2, no. 4, p. 1500328, 2016.

[10] A. Huebler, F. Doetz, H. Kempa, H. Katz, M. Bartzsch, N. Brandt, I. Hennig, U. Fuegmann, S. Vaidyanathan, J. Granstrom, and others, "Ring oscillator fabricated completely by means of mass-printing technologies", *Organic Electronics*, vol. 8, no. 5, pp. 480–486, 2007.

[11] H. K. Kang, "Gravure-printed Highly-scaled Organic Thin-film Transistors for Low-cost and Large-area Electronics", *Thesis at University of California, Berkeley*, 2013.

[12] Y.-M. Choi, K.-Y. Kim, E. Lee, J. Jo, and T.-M. Lee, "Fabrication of a single-layer metal-mesh touchscreen sensor using reverse-offset printing", *Journal of Information Display*, vol. 16, no. 1, pp. 37–41, 2015.

[13] Y.-M. Choi, E. Lee, and T.-M. Lee, "Mechanism of reverse-offset printing", *Journal of Micromechanics and Microengineering*, vol. 25, no. 7, p. 075019, 2015.

[14] T. Cui, Y. Liu, B. Chen, M. Zhu, and K. Varahramyan, "Printed polymeric passive RC filters and degradation characteristics", *Solid-state electronics*, vol. 49, no. 5, pp. 853–859, 2005.

[15] S. Jussila, M. Puustinen, T. Hassinen, J. Olkkonen, H. G. Sandberg, and K. Solehmainen, "Self-aligned patterning method of poly (aniline) for organic field-effect transistor gate electrode", *Organic Electronics*, vol. 13, pp. 1308–1314, 2012.

[16] T. Mäkelä, T. Haatainen, P. Majander, and J. Ahopelto, "Continuous roll to roll nanoimprinting of inherently conducting polyaniline", *Microelectronic engineering*, vol. 84, no. 5, pp. 877–879, 2007.

[17] H. Bai and G. Shi, "Gas sensors based on conducting polymers", *Sensors*, vol. 7, no. 3, pp. 267–307, 2007.

[18] N. Li, X. Li, W. Geng, T. Zhang, Y. Zuo, and S. Qiu, "Synthesis and humidity sensitivity of conducting polyaniline in SBA-15", *Journal of applied polymer science*, vol. 93, no. 4, pp. 1597–1601, 2004.

[19] M. Jung, J. Kim, J. Noh, N. Lim, C. Lim, G. Lee, J. Kim, H. Kang, K. Jung, A. D. Leonard, and others, "All-printed and roll-to-roll-printable 13.56-MHz-operated 1-bit RF tag on plastic foils", *IEEE Transactions on Electron Devices*, vol. 57, no. 3, pp. 571–580, 2010.

[20] J. Kim, T. Hassinen, W. H. Lee, and S. Ko, "Fully solution-processed organic thin-film transistors by consecutive roll-to-roll gravure printing", *Organic Electronics*, vol. 42, pp. 361–366, 2017.

[21] J. Kim, J. Kim, B. Ahn, T. Hassinen, Y. Jung, and S. Ko, “Optimization and improvement of TIPS-pentacene transistors (OTFT) with UV-ozone and chemical treatments using an all-step solution process”, *Current Applied Physics*, vol. 15, pp. 1238–1244, 2015.

[22] J. Perelaer, A. W. De Laat, C. E. Hendriks, and U. S. Schubert, “Inkjet-printed silver tracks: low temperature curing and thermal stability investigation”, *Journal of Materials Chemistry*, vol. 18, no. 27, pp. 3209–3215, 2008.

[23] M. L. Allen, M. Aronniemi, T. Mattila, A. Alastalo, K. Ojanperä, M. Suhonen, and H. Seppä, “Electrical sintering of nanoparticle structures”, *Nanotechnology*, vol. 19, no. 17, pp. 175201–175205, 2008.

[24] M. K. Kwak, J. G. Ok, J. Y. Lee, and L. J. Guo, “Continuous phase-shift lithography with a roll-type mask and application to transparent conductor fabrication”, *Nanotechnology*, vol. 23, no. 34, p. 344008, 2012.

[25] S. H. Ahn and L. J. Guo, “High-speed roll-to-roll nanoimprint lithography on flexible plastic substrates”, *Advanced materials*, vol. 20, no. 11, pp. 2044–2049, 2008.

[26] J. A. Rogers, Z. Bao, A. Makhija, P. Braun, and others, “Printing process suitable for reel-to-reel production of high-performance organic transistors and circuits”, *Advanced materials*, vol. 11, no. 9, pp. 741–745, 1999.

[27] C.-Y. Lo, O.-H. Huttunen, J. Hiitola-Keinanen, J. Petaja, H. Fujita, and H. Toshiyoshi, “MEMS-controlled paper-like transmissive flexible display”, *Microelectromechanical Systems, Journal of*, vol. 19, no. 2, pp. 410–418, 2010.

[28] M. Vilkman, T. Ruotsalainen, K. Solehmainen, E. Jansson, and J. Hiitola-Keinänen, “Self-Aligned Metal Electrodes in Fully Roll-to-Roll Processed Organic Transistors”, *Electronics*, vol. 5, no. 1, p. 2, 2016.

[29] P. Apilo, J. Hiltunen, M. Välimäki, S. Heinilehto, R. Sliz, and J. Hast, “Roll-to-roll gravure printing of organic photovoltaic modules—insulation of processing defects by an interfacial layer”, *Progress in Photovoltaics: Research and Applications*, vol. 23, no. 7, pp. 918–928, 2015.

[30] T. Blaudeck, P. A. Ersman, M. Sandberg, S. Heinz, A. Laiho, J. Liu, I. Engquist, M. Berggren, and R. R. Baumann, “Simplified Large-Area Manufacturing of Organic Electrochemical Transistors Combining Printing and a Self-Aligning Laser Ablation Step”, *Advanced Functional Materials*, vol. 22, no. 14, pp. 2939–2948, 2012.

[31] D. Kim, S. Jeong, J. Moon, S. Han, and J. Chung, “Organic thin film transistors with ink-jet printed metal nanoparticle electrodes of a reduced channel length by laser ablation”, *Applied Physics Letters*, vol. 91, no. 7, pp. 071114–071114, 2007.

[32] S. H. Ko, H. Pan, C. P. Grigoropoulos, J. M. Fréchet, C. K. Luscombe, and D. Poulikakos, "Lithography-free high-resolution organic transistor arrays on polymer substrate by low energy selective laser ablation of inkjet-printed nanoparticle film", *Applied Physics A*, vol. 92, no. 3, pp. 579–587, 2008.

[33] M. Knowles, G. Rutterford, D. Karnakis, and A. Ferguson, "Micro-machining of metals, ceramics and polymers using nanosecond lasers", *The International Journal of Advanced Manufacturing Technology*, vol. 33, no. 1–2, pp. 95–102, 2007.

[34] H. Sirringhaus, "25th Anniversary Article: Organic Field-Effect Transistors: The Path Beyond Amorphous Silicon", *Advanced materials*, vol. 26, no. 9, pp. 1319–1335, 2014.

[35] V. Subramanian, J. Cen, A. de la Fuente Vornbrock, G. Grau, H. Kang, R. Kitsomboonloha, D. Soltman, and H.-Y. Tseng, "High-Speed Printing of Transistors: From Inks to Devices", *Proceedings of the IEEE*, vol. 103, no. 4, pp. 567–582, 2015.

[36] J. H. Oh, W.-Y. Lee, T. Noe, W.-C. Chen, M. Könemann, and Z. Bao, "Solution-shear-processed quaterrylene diimide thin-film transistors prepared by pressure-assisted thermal cleavage of swallow tails", *Journal of the American Chemical Society*, vol. 133, no. 12, pp. 4204–4207, 2011.

[37] W.-Y. Lee, J. H. Oh, S.-L. Suraru, W.-C. Chen, F. Würthner, and Z. Bao, "High-Mobility Air-Stable Solution-Shear-Processed n-Channel Organic Transistors Based on Core-Chlorinated Naphthalene Diimides", *Advanced Functional Materials*, vol. 21, no. 21, pp. 4173–4181, 2011.

[38] G. Giri, E. Verploegen, S. C. Mannsfeld, S. Atahan-Evrenk, S. Y. Lee, H. A. Becerril, A. Aspuru-Guzik, M. F. Toney, and Z. Bao, "Tuning charge transport in solution-sheared organic semiconductors using lattice strain", *Nature*, vol. 480, no. 7378, pp. 504–508, 2011.

[39] X. Zhang, L. J. Richter, D. M. DeLongchamp, R. J. Kline, M. R. Hammond, I. McCulloch, M. Heeney, R. S. Ashraf, J. N. Smith, T. D. Anthopoulos, and others, "Molecular packing of high-mobility diketo pyrrolo-pyrrole polymer semiconductors with branched alkyl side chains", *Journal of the American Chemical Society*, vol. 133, no. 38, pp. 15073–15084, 2011.

[40] M. Ling, Z. Bao, and D. Li, "Transistor performance of top rough surface of pentacene measured by laminated double insulated-gate supported on a poly (dimethylsiloxanes) base structure", *Applied physics letters*, vol. 88, no. 3, pp. 033502–033502, 2006.

[41] F. Li, A. Nathan, Y. Wu, and B. S. Ong, *Organic Thin Film Transistor Integration*. Wiley-VCH, 2011.

[42] Y.-L. Loo, T. Someya, K. W. Baldwin, Z. Bao, P. Ho, A. Dodabalapur, H. E. Katz, and J. A. Rogers, “Soft, conformable electrical contacts for organic semiconductors: High-resolution plastic circuits by lamination”, *Proceedings of the National Academy of Sciences*, vol. 99, no. 16, pp. 10252–10256, 2002.

[43] J. Zaumseil, K. W. Baldwin, and J. A. Rogers, “Contact resistance in organic transistors that use source and drain electrodes formed by soft contact lamination”, *Journal of Applied Physics*, vol. 93, no. 10, pp. 6117–6124, 2003.

[44] J. H. Lee, G. H. Kim, S. H. Kim, S. C. Lim, Y. S. Yang, J. H. Youk, J. Jang, and T. Zyung, “Longevity enhancement of organic thin-film transistors by using a facile laminating passivation method”, *Synthetic metals*, vol. 143, no. 1, pp. 21–23, 2004.

[45] A. Hübler, G. Schmidt, H. Kempa, K. Reuter, M. Hambsch, and M. Bellmann, “Three-dimensional integrated circuit using printed electronics”, *Organic Electronics*, vol. 12, no. 3, pp. 419–423, 2011.

[46] A. Tunnell, D. Hines, E. Gomar-Nadal, and E. Williams, “Printing-induced improvements of organic thin-film transistors”, *Organic Electronics*, vol. 9, no. 4, pp. 507–514, 2008.

[47] S.-H. Shin, S. Ji, S. Choi, K.-H. Pyo, B. W. An, J. Park, J. Kim, J.-Y. Kim, K.-S. Lee, S.-Y. Kwon, and others, “Integrated arrays of air-dielectric graphene transistors as transparent active-matrix pressure sensors for wide pressure ranges”, *Nature Communications*, vol. 8, p. 8, 2017.

[48] G. Nisato, D. Lupo, and S. Ganz, *Organic and Printed Electronics: Fundamentals and Applications*. CRC Press, 2016.

[49] K. Fukuda, Y. Takeda, M. Mizukami, D. Kumaki, and S. Tokito, “Fully solution-processed flexible organic thin film transistor arrays with high mobility and exceptional uniformity”, *Scientific reports*, vol. 4, 2014.

[50] Y.-Y. Noh and H. Sirringhaus, “Ultra-thin polymer gate dielectrics for top-gate polymer field-effect transistors”, *Organic Electronics*, vol. 10, no. 1, pp. 174–180, 2009.

[51] R. Hamilton, J. Smith, S. Ogier, M. Heeney, J. E. Anthony, I. McCulloch, J. Veres, D. D. Bradley, and T. D. Anthopoulos, “High-performance polymer-small molecule blend organic transistors”, *Advanced Materials*, vol. 21, no. 10–11, pp. 1166–1171, 2009.

[52] J. Veres, S. D. Ogier, S. W. Leeming, D. C. Cupertino, and S. Mohialdin Khaffaf, “Low-k Insulators as the Choice of Dielectrics in Organic Field-Effect Transistors”, *Advanced Functional Materials*, vol. 13, no. 3, pp. 199–204, 2003.

[53] M. M. Ling and Z. Bao, “Thin film deposition, patterning, and printing in organic thin film transistors”, *Chemistry of materials*, vol. 16, no. 23, pp. 4824–4840, 2004.

[54] D. Hong, G. Yerubandi, H. Chiang, M. Spiegelberg, and J. Wager, “Electrical modeling of thin-film transistors”, *Critical Reviews in Solid State and Materials Sciences*, vol. 33, no. 2, pp. 101–132, 2008.

[55] V. Vinciguerra, M. L. Rosa, D. Nicolosi, G. Sicurella, and L. Occhipinti, “Modeling the gate bias dependence of contact resistance in staggered polycrystalline organic thin film transistors”, *Organic electronics*, vol. 10, no. 6, pp. 1074–1081, 2009.

[56] J. Verilhac, M. Benwadih, S. Altazin, S. Jacob, R. Gwoziecki, R. Coppard, and C. Serbutoviez, “Effects of amorphous semiconductor thickness on top gate staggered organic field-effect transistors”, *Applied Physics Letters*, vol. 94, no. 14, p. 102, 2009.

[57] D. Boudinet, M. Benwadih, S. Altazin, R. Gwoziecki, J. Verilhac, R. Coppard, G. Le Blevennec, I. Chartier, and G. Horowitz, “Influence of the semi-conductor layer thickness on electrical performance of staggered n-and p-channel organic thin-film transistors”, *Organic Electronics*, vol. 11, no. 2, pp. 291–298, 2010.

[58] T. Zaki, S. Scheinert, I. Horselmann, R. Rodel, F. Letzkus, H. Richter, U. Zschieschang, H. Klauk, and J. N. Burghartz, “Accurate capacitance modeling and characterization of organic thin-film transistors”, *IEEE Transactions on Electron Devices*, vol. 61, no. 1, pp. 98–104, 2014.

[59] S. M. Sze, *Semiconductor devices, physics and technology*. Wiley, 1985.

[60] A. Hoppe, D. Knipp, B. Gburek, A. Benor, M. Marinkovic, and V. Wagner, “Scaling limits of organic thin film transistors”, *Organic Electronics*, vol. 11, no. 4, pp. 626–631, 2010.

[61] R. P. Ortiz, A. Facchetti, and T. J. Marks, “High-k organic, inorganic, and hybrid dielectrics for low-voltage organic field-effect transistors”, *Chemical reviews*, vol. 110, no. 1, p. 205, 2010.

[62] J. Fisher and I. Giaever, “Tunneling through thin insulating layers”, *Journal of Applied Physics*, vol. 32, no. 2, pp. 172–177, 1961.

[63] P. Kim, X.-H. Zhang, B. Domercq, S. Jones, P. Hotchkiss, S. Marder, B. Kippelen, and J. Perry, “Solution-processible high-permittivity nanocomposite gate insulators for organic field-effect transistors”, *Applied Physics Letters*, vol. 93, p. 013302, 2008.

[64] J. Veres, S. Ogier, G. Lloyd, and D. De Leeuw, “Gate insulators in organic field-effect transistors”, *Chemistry of Materials*, vol. 16, no. 23, pp. 4543–4555, 2004.

[65] N. Gupta, “Threshold voltage modelling and gate oxide thickness effect on polycrystalline silicon thin-film transistors”, *Physica Scripta*, vol. 76, no. 6, p. 628, 2007.

[66] A. Wang, I. Kymissis, V. Bulovic, and A. I. Akinwande, “Engineering density of semiconductor-dielectric interface states to modulate threshold voltage in OFETs”, *IEEE Transactions on Electron Devices*, vol. 53, no. 1, pp. 9–13, 2006.

[67] C. Huang, J. E. West, and H. E. Katz, “Organic Field-Effect Transistors and Unipolar Logic Gates on Charged Electrets from Spin-On Organosilsesquioxane Resins”, *Advanced Functional Materials*, vol. 17, no. 1, pp. 142–153, 2007.

[68] K. Pernstich, S. Haas, D. Oberhoff, C. Goldmann, D. Gundlach, B. Batlogg, A. Rashid, and G. Schitter, “Threshold voltage shift in organic field effect transistors by dipole monolayers on the gate insulator”, *Journal of Applied Physics*, vol. 96, no. 11, pp. 6431–6438, 2004.

[69] Y. Chen and V. Podzorov, “Bias stress effect in ‘air-gap’ organic field-effect transistors”, *Advanced Materials*, vol. 24, no. 20, pp. 2679–84, 2012.

[70] W. Olthuis, “Chemical and physical FET-based sensors or variations on an equation”, *Sensors and Actuators B: Chemical*, vol. 105, no. 1, pp. 96–103, 2005.

[71] W. K. Schomburg, *Introduction to microsystem design*. Springer, 2015.

[72] A. Mukherjee, A. Thakur, W. Takashima, and K. Kaneto, “Minimization of contact resistance between metal and polymer by surface doping”, *Journal of Physics D: Applied Physics*, vol. 40, no. 6, p. 1789, 2007.

[73] H. Sirringhaus, “Reliability of Organic Field-Effect Transistors”, *Advanced Materials*, vol. 21, no. 38–39, pp. 3859–3873, 2009.

[74] D. Gupta, N. Jeon, and S. Yoo, “Modeling the electrical characteristics of TIPS-pentacene thin-film transistors: Effect of contact barrier, field-dependent mobility, and traps”, *Organic electronics*, vol. 9, no. 6, pp. 1026–1031, 2008.

[75] P. Stallinga, *Electrical Characterization of Organic Electronic Materials and Devices,* John Wiley & Sons, 2009.

[76] O. Marinov, M. Deen, B. Iniguez, and B. Ong, "Charge localization in polymeric metal-oxide-semiconductor capacitors", *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, vol. 24, no. 3, pp. 649–653, 2006.

[77] M. McDowell, I. Hill, J. McDermott, S. Bernasek, and J. Schwartz, "Improved organic thin-film transistor performance using novel self-assembled monolayers", *Applied physics letters*, vol. 88, no. 7, pp. 073505–073505, 2006.

[78] L. Teng and W. A. Anderson, "Thin-film transistors on plastic and glass substrates using silicon deposited by microwave plasma ECR-CVD", *IEEE Electron Device Letters*, vol. 24, no. 6, pp. 399–401, 2003.

[79] S. Zilker, C. Detcheverry, E. Cantatore, and D. De Leeuw, "Bias stress in organic thin-film transistors and logic gates", *Applied Physics Letters*, vol. 79, no. 8, pp. 1124–1126, 2001.

[80] B. Stadlober, U. Haas, H. Gold, A. Haase, G. Jakopic, G. Leising, N. Koch, S. Rentenberger, and E. Zojer, "Orders-of-Magnitude Reduction of the Contact Resistance in Short-Channel Hot Embossed Organic Thin Film Transistors by Oxidative Treatment of Au-Electrodes", *Advanced Functional Materials*, vol. 17, no. 15, pp. 2687–2692, 2007.

[81] J.-P. Hong, A.-Y. Park, S. Lee, J. Kang, N. Shin, and D. Y. Yoon, "Tuning of Ag work functions by self-assembled monolayers of aromatic thiols for an efficient hole injection for solution processed triisopropylsilylethynyl pentacene organic thin film transistors", *Applied Physics Letters*, vol. 92, no. 14, p. 143311, 2008.

[82] C. Momma, B. N. Chichkov, S. Nolte, F. von Alvensleben, A. Tünnermann, H. Welling, and B. Wellegehausen, "Short-pulse laser ablation of solid targets", *Optics communications*, vol. 129, no. 1, pp. 134–142, 1996.

[83] T. Hassinen, A. Alastalo, K. Eiroma, T.-M. Tenhunen, V. Kunnari, T. Kaljunen, U. Forsström, and T. Tammelin, "All-Printed Transistors on Nano Cellulose Substrate", *MRS Advances*, vol. 1, pp. 645–650, 2015.

[84] S. Hoshino, T. Kamata, and K. Yase, "Effect of active layer thickness on device properties of organic thin-film transistors based on Cu (II) phthalocyanine", *Journal of applied physics*, vol. 92, no. 10, pp. 6028–6032, 2002.

[85] H. Jia, S. Gowrisanker, G. K. Pant, R. M. Wallace, and B. E. Gnade, "Effect of poly (3-hexylthiophene) film thickness on organic thin film transistor properties", *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, vol. 24, no. 4, pp. 1228–1232, 2006.

[86] T. Kushida, T. Nagase, and H. Naito, “Angular distribution of field-effect mobility in oriented poly [5, 5′-bis (3-dodecyl-2-thienyl)-2, 2′-bithiophene] fabricated by roll-transfer printing”, *Applied Physics Letters*, vol. 104, no. 9, p. 093304, 2014.

[87] P. Schwinkendorf, M. Lorenz, H. Hochmuth, Z. Zhang, and M. Grundmann, “Interface charging effects in ferroelectric ZnO-BaTiO3 field-effect transistor heterostructures”, *Physica Status Solidi A*, vol. 211, no. 1, pp. 166–172, 2014.

[88] H. Mahfoz-Kotb, A.-C. Salaun, T. Mohammed-Brahim, and O. Bonnaud, “Air-gap polycrystalline silicon thin-film transistors for fully integrated sensors”, *Electron Device Letters, IEEE*, vol. 24, no. 3, pp. 165–167, 2003.