PROCEEDINGS OF SCIENCE

Laboratory and Beam Test Results of TOFFEE ASIC and Ultra Fast Silicon Detectors

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In this report we present measurements performed on the full custom ASIC TOFFEE, designed to pre-amplify and discriminate signals of Ultra Fast Silicon Detectors. The ASIC has been characterized in laboratory with custom test boards, and with infrared laser light hitting the sensor emulating a minimum ionizing particle signal. Laser measurements show that a jitter term better than 50 (40) ps is achievable with a 10 (12) fC input charge.

We also present some preliminary results on the TOFFEE performances, as obtained during recent beam tests with a 180 GeV/c pion beam, on the SPS-H8 beam line at CERN.

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1. Introduction

In many physics research fields, there is a common trend towards high resolution time measurements, aiming to distinguish events within a few tens of picoseconds. For such precise time information, detectors, required to generate large and uniform signals, have to be coupled to fast and low noise read-out electronics.

The original motivation for the design of this ASIC was the development of a low-noise/high slew-rate read-out chip to be coupled to multi-channel Ultra Fast Silicon Detectors (UFSD [5]), for testing purposes and for a possible application to the CT-PPS timing stations[2]. The CT-PPS timing detector has to measure the time of passage of protons, scattered at low angle from the CMS interaction point, with a resolution of 20 ps (around 40-50 ps per plane).

The specifications of the TOFFEE chip (which stands for Time Of Flight Front-End Electronics) are tailored to match the characteristics of the signal of UFSD sensors. These sensors feature internal charge multiplication (UFSD gain), electrode segmentation and provide a signal between 8 and 10 fC for a minimum ionizing particle. The moderate charge multiplication produces a fast and steep signal while keeping the avalanche noise low. Their intrinsic time resolution depends on the multiplication gain (i.e. on the bias voltage) and on the thickness of the active area.

All the measurements here reported have been obtained with a TOFFEE chip wire-bonded to a multi-channel UFSD sensor produced by CNM[1], specifically designed for the CT-PPS application (see figure 2-right plot): it consists of a 16×2 pad matrix, with 16 narrow pads (3×0.5 mm^2- 3 pF capacitance) and 16 wide pads (3×1 mm^2- 6 pF capacitance), built on a 50-microns wafer.

2. The TOFFEE ASIC

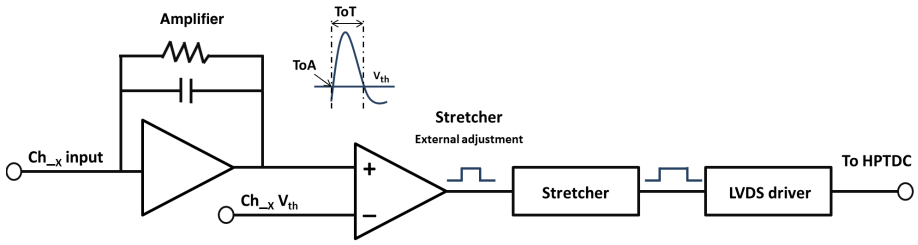

Figure 1: The channel architecture of the TOFFEE ASIC

The TOFFEE ASIC[3], a fully custom-made analog ASIC, is a 8-channel amplifier comparator chip which has been designed with an input stage optimized for the shape and charge of the UFSD signal. The ASIC has been developed in UMC 110 nm CMOS technology. It features LVDS outputs matching the High Precision TDC system requirements[4]. Fig. 1 represents the logical architecture of one channel. The chip provides a step-like output signal where the leading edge is the *Time of Arrival* ToA of the signal and its duration the *Time over Thresholds* ToT.

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The design specifications are: wide input dynamic range, 3 - 60 fC; analog pre-amplifier gain G_T= 7 mV/fC at 23°C, with a slight temperature dependence; signal rise time of 3 ns; slew rate of 25 mV/ns; noise RMS of 0.8 mV.

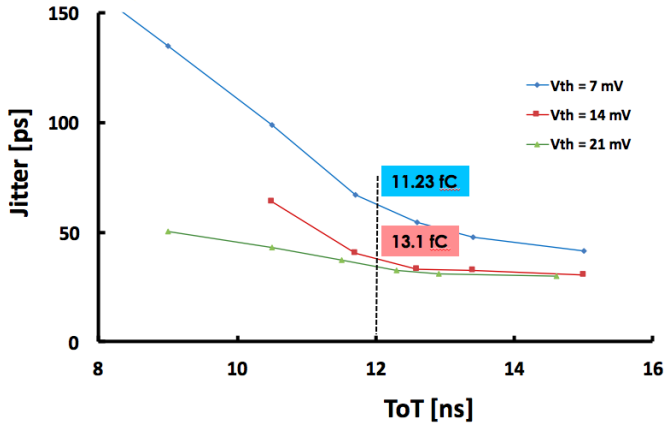
The time resolution of the TOFFEE chip is determined by two contributions: the electronic noise of the front end and the *time walk* related to different amplitude signals crossing the discriminator threshold. The time walk term is mitigated by the ToT correction, which consists in using the correlation between the time of arrival of a signal and its time over threshold, in first approximation linear, to correct the time of arrival (small signals have a smaller slew rate and cross the discriminator threshold later than big signals).

2.1 TOFFEE characterization in Laboratory

Several tests have been done to characterize the chip, with an external input charge injector directly connected to the TOFFEE chip or with an infrared laser setup illuminating the sensor, able to mimic the signal released in the device by a minimum ionizing particle (MIP). The charge produced by the laser has been calibrated by means of a pin diode without charge multiplication.

The pre-amplifier output signal shape has been reconstructed, in the laboratory, by recording the ToA and ToT values during a fine-grained discriminator threshold scan. This method allows measuring the rise time (3.5 ns), slew rate (25 mV/ns) and electronic noise (0.8 mV), all found to be in very good agreement with the design and post-layout simulation of the ASIC.

The measurement of the jitter, $\sigma_{Jitter} \simeq Noise/(dV/dt)$, as a function of the ToT measured by the TOFFEE, has been achieved varying the laser intensity, such to explore the response in a large range of ToT. The measurements have been repeated for different values of discriminator threshold Vth. Fig. 2 (left plot) shows the results for three different thresholds, 7 mV, 14 mV and 21 mV above the baseline. These results are in very good agreement with the initial characterization of the chip, and with the simulations[3].



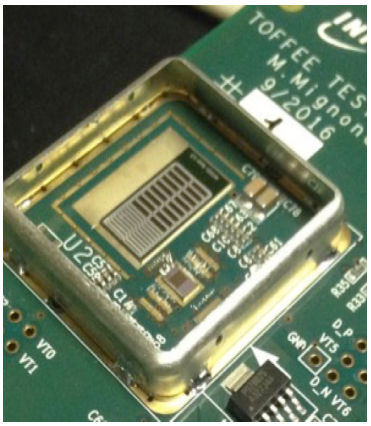


Figure 2: TOFFEE jitter, measured in bins of ToT, for three different discriminator thresholds (Laser on CNM 50 micron-thick UFSD biased at 200 V) (on the left). Custom carrier board with UFSD CT-PPS sensor wire-bonded to a TOFFEE ASIC (on the right)

3. Beam Test measurements

The TOFFEE ASIC, connected to the UFSD CT-PPS sensor, has been recently tested with minimum ionizing particles, in the H8-SPS/CERN beam line with 180 GeV/c pions. The experimental setup consisted of a small telescope with one TOFFEE board and one *reference* board, consisting of a CNM UFSD sensor, 1×1 mm^2 pad, read out by the *UCSC pre-amplifier* board (for a detailed description please see [5]). The sensor on the UCSC board was biased at 220 V: this system provides a reliable and well known reference signal, as it has been used in previous beam tests, with a time resolution $\sim$35 ps. Both boards were read out by a 4 GHz scope (LeCroy HDO9404). Given the slightly different geometry of the two sensors, three TOFFEE channels were partially overlapping with the UCSC board sensor.

In order to study in details the TOFFEE performances, data have been taken in different configurations, scanning over the bias voltage V_{bias} in the 100-230 V range, and the discriminator threshold Vth, between 7 and 25 mV above the baseline. The analysis of the TOFFEE time resolution achieved during the beam test is in progress. The ToA-ToT relationship presents, in certain conditions, some unforeseen features which are under investigation. A beam test campaign using single pad and multi-pad UFSD sensors from other vendors (HPK, FBK) will be performed shortly to complement the studies.

3.1 Experimental determination of the pre-amplifier gain

One of the measurements done at the beam test is the determination of the TOFFEE pre-amplifier analog gain G_T (mV/fC).

The internal gain of a given UFSD wafer varies with the bias voltage, with a dependence that can be determined by dividing IV curves for gain(UFSD)/no-gain(pin diodes) identical devices. The uniformity of the gain charecteristics on a wafer is better than 30%, therefore the *gain(V_{bias})* curve for the sensor used at the beam test is very well known. The most probable value (MPV) of the charge deposited by a MIP in 50 microns of silicon is $\sim$0.46 fC. At every bias voltage, *Qin* = 0.46 fC $\cdot$ *gain(V_{bias})* represents the TOFFEE MPV input charge. Data collected during the test beam cover the 2.5 - 12 fC range in input charge (G = 5-25).

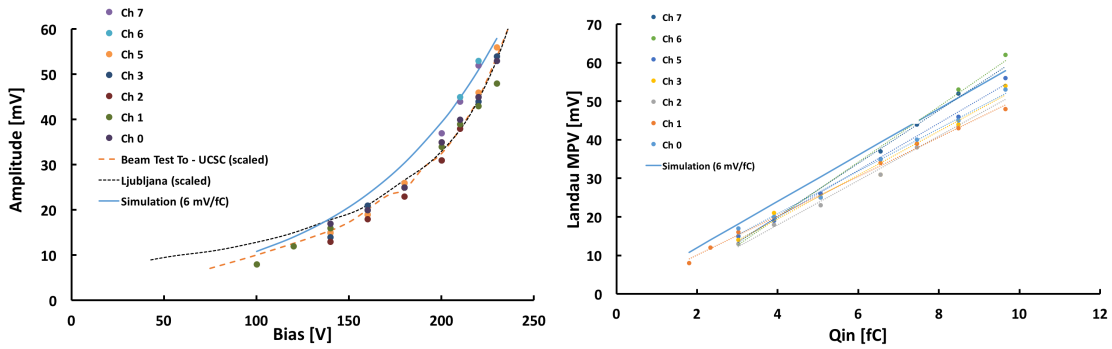


Figure 3: Amplitude versus bias voltage for MIP, measured in the 7 active channels with the *Vth-70%* method, compared with previous measurements (scaled) (on the left); MPV amplitude of the pre-amplifier signal versus MPV *Qin*, for the 7 active channels (on the right)

One can measure the MPV of the amplitude of the signal produced by the TOFFEE pre-amplifier stage exploiting the properties of the Landau distribution. The Landau cumulative distribution function at the MPV is 30%. By counting the number of events in a Δt as a function of Vth, one can find the value *Vth-70%* which keeps 70% of the events observed with the baseline threshold; *Vth-70%* is the Landau MPV. Fig. 3 (left plot) shows the MPV amplitude as a function of the bias voltage, for every channel. The plot also shows a comparison with the analogous curves obtained during a beam test in 2016 (TO-UCSC) or in laboratory by the Ljubljana group, with the same sensor type and different read-out electronics. The good agreement demonstrates that the pre-amplifier performs correctly. Finally, one can correlate *Qin* and amplitude values via their dependence on V_{bias}, obtaining the charge versus amplitude plot shown in fig. 3 (right plot). This plot suggests that G_T= 6 mV/fC, which is in pleasing agreement with the post layout simulation of the TOFFEE chip.

4. Conclusions

The laboratory characterization of TOFFEE coupled to the UFSD CT-PPS sensor (3.0× 0.5 mm^2 pads) demonstrates the correct behavior of the ASIC, with noise level, slew rate and rise time in good agreement with the design specs. For a discriminator threshold of 14 mV, the electronic jitter is better than 50 (40) ps for input charges above 10 (12) fC. The pre-amplifier gain has been measured at the beam test to be ∼6 mV/fC, in good agreement with the ASIC simulations. Extensive studies of the performances achieved during the beam tests in SPS-H8 are ongoing. A new beam test, with a telescope made of two TOFFEE boards connected to Hamamatsu UFSD single pads, is in preparation for mid October 2017.

Acknowledgments

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References

[1] N. Cartiglia et al, *Design Optimization of Ultra-Fast Silicon Detectors*, Nucl.Instrum.Meth. **A 796, (2015)**, 141-148

[2] R. Arcidiacono et al, *A new timing detector for the CT-PPS project*, NIM**A 845** (2017) 16-19

[3] F. Cenna et al., *TOFFEE: a full custom amplifier-comparator chip for timing applications with silicon detectors*, JINST **12** (2017) C03031

[4] J. Christiansen, *http://cds.cern.ch/record/1067476*, 2004

[5] N.Cartiglia et al, *Beam test results of a 16 ps timing system based on ultra-fast silicon detectors*, Nucl.Instrum.Meth. **A 850** (2017) 83-88.