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Safe-Operating-Area of Snubberless Series Connected Silicon and SiC power devices

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***Abstract*— As power devices are series connected for voltage sharing, loss of gate drive synchronization and/or variation in device switching time constant can cause voltage imbalance. Capacitors (in snubbers) are usually added to maintain series voltage balance, however, in snubberless designs, where active gate drivers are used for voltage balancing during transients, it is necessary to evaluate the limits of the power device under transient unsynchronized switching. In series devices, desynchronization of the gate drivers in series connected devices will cause the faster switching device into avalanche during turn-OFF. Power device failure from BJT latch-up in MOSFETs and thyristor latch-up in IGBTs can result in potentially destructive consequences for the entire converter. Failure of the power device under avalanche is exacerbated by the (i) device commutation rate (ii) device junction temperature (iii) magnitude of gate drive switching mismatch and (iv) ratio of the DC bus voltage to intrinsic breakdown voltage of the device. This paper uses experimental measurements and finite element models to investigate the limits of power device failure under transient unsynchronized switching of series connected SiC trench MOSFET and silicon IGBT devices.**

Keywords—series connection, unsynchronized switching, BJT latch-up, Si IGBT, SiC MOSFET

I. INTRODUCTION

In high voltage applications such as grid connected power converters and DC-circuit breakers [1], high voltage blocking capability of the switching power electronic devices are needed. For such applications, series connection of the IGBTs and more recently with emerging of wide bandgap semiconductors, SiC MOSFETs may be required [2, 3]. The design limitation with the series connection of power devices is the potential loss of gate synchronization leading to severe voltage imbalance. This can result from variation in the electrothermal parameters of the series devices as well as mismatch in the gate drive system. The result of uncontrolled voltage imbalance is destructive failure from avalanche induced latch-up [4-7].

Snubber capacitors are typically used for maintaining the voltage balance between series connected devices; however, they reduce the switching speed and increase the switching losses and cost of the system. Active gate drivers can potentially dispense with the snubbers by maintaining voltage balance by using a control loop to sense the output voltage and adjust the gate drive current [8]. In the case of failure of the control loop to maintain voltage balance, the power devices used in active gate drive systems should withstand unforeseen malfunctions. Hence, it is necessary to understand the limits of device ruggedness under dynamic avalanche resulting from loss of voltage balance in series devices.

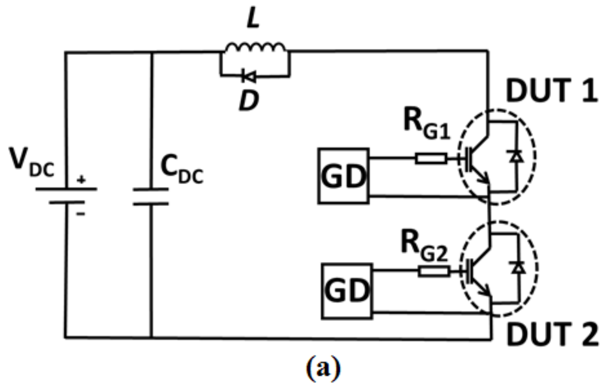
In this paper, using experimental measurements and finite element models, a systematic investigation is performed into the limits of the safe-operating-area (SOA) of series connected power devices under dynamic voltage imbalance. SiC trench MOSFETs and silicon field stop IGBTs have been selected for the study. The experiments compare the ruggedness of the two technologies and proposes a method to define the safe-operating-area (SOA) of series connected power devices.

II. EXPERIMENTAL SETUP

A circuit has been developed to test dynamic avalanche of power devices under series connection. The circuit schematic and picture is shown in Figure 1 (a) and (b) respectively. The devices under investigation were 600 V/20A Infineon Field Stop IGBTs with datasheet reference IKW20N60H3 and 650 V/39A ROHM SiC trench power MOSFET with datasheet reference SCT3060AL. A 1200V/16A SiC Schottky diode with datasheet reference IDH16G120C5 was used as the clamping diode.

The DC link voltage of the power devices was originally set so that each device would block half its rated voltage. To determine the SOA of the power devices under dynamic conditions, a mismatch is introduced into the gate driver signals, thereby causing the devices to switch at different instances. The magnitude of this gate mismatch delay is varied together with the device current/voltage commutation rate which is controlled by the gate resistance. Hence, for a given gate resistance, the gate mismatch delay between the gates of the series connected devices is varied until the device exceeds the SOA thereby going into avalanche and potentially destructive latch-up. For gate mismatch delay between 2 series connected devices, the faster switching device may go into avalanche during turn-OFF. The SOA under these conditions will depend on (i) the magnitude of

gate mismatch delay (ii) the magnitude of the inductive voltage overshoot during turn-OFF and (iii) the ratio of the measured peak voltage to the rated voltage.



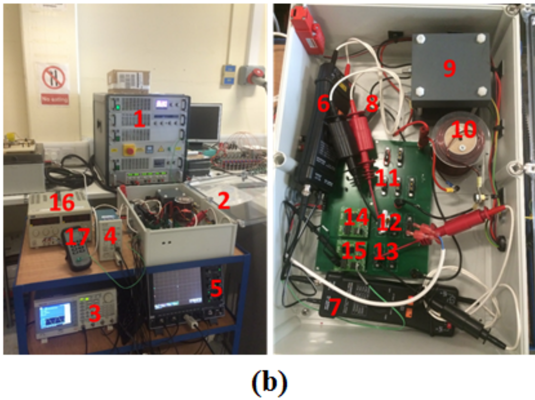


Fig. 1. (a) Circuit schematic and (b) test rig setup: [1] DC Power Supply. [2] Test Chamber. [3] Function Generator. [4] Current probe Amplifier. [5] Oscilloscope. [6] and [7] Voltage probes. [8] Current Probe. [9] DC capacitor. [10] Inductor. [11] Clamped diode [12] and [13] DUTs. [14] and [15] Gate Drives.

III. RESULTS AND DISCUSSION

Fig. 2 (a), (b) and (c) show the turn-OFF voltage and current waveforms of series connected IGBTs. Fig. 2 (a) shows the case where the gate drivers are perfectly synchronized. It can be seen from Fig. 2(a) that the devices share the total voltage equally. Fig. 2(b) shows the turn-OFF transient waveforms of the series connected IGBTs with 233 ns gate delay. It can be seen from Fig. 2(b) that the faster switching IGBT blocks the DC link voltage entirely. Fig.2(c) shows the measurements for a case where there is a 240ns delay between the gate drivers. It can be seen from Fig. 2(c) that the fast switching device, DUT1, goes into destructive failure since the maximum blocking voltage has been exceeded. At approximately 600ns, DUT1 (the faster IGBT) fails through thyristor latch-up and thus results in a short circuit. At that instant, the current, which was initially commutating into the free-wheeling diode, starts to rise through the IGBT as can be seen between 600 ns and 900 ns in Fig. 2(c).

The mechanism of thyristor latch-up is shown in Fig 3(a) and Fig. 3(b) where the equivalent circuit of the IGBT is shown during normal conduction mode and during avalanche conduction mode. The equivalent circuit comprises of the MOS channel gate and the cross-coupled NPN and PNP BJTs that constitute the parasitic thyristor inherent in every IGBT. The drift resistance of the voltage blocking epitaxial layer is also shown together with the parasitic resistance of the p-body.

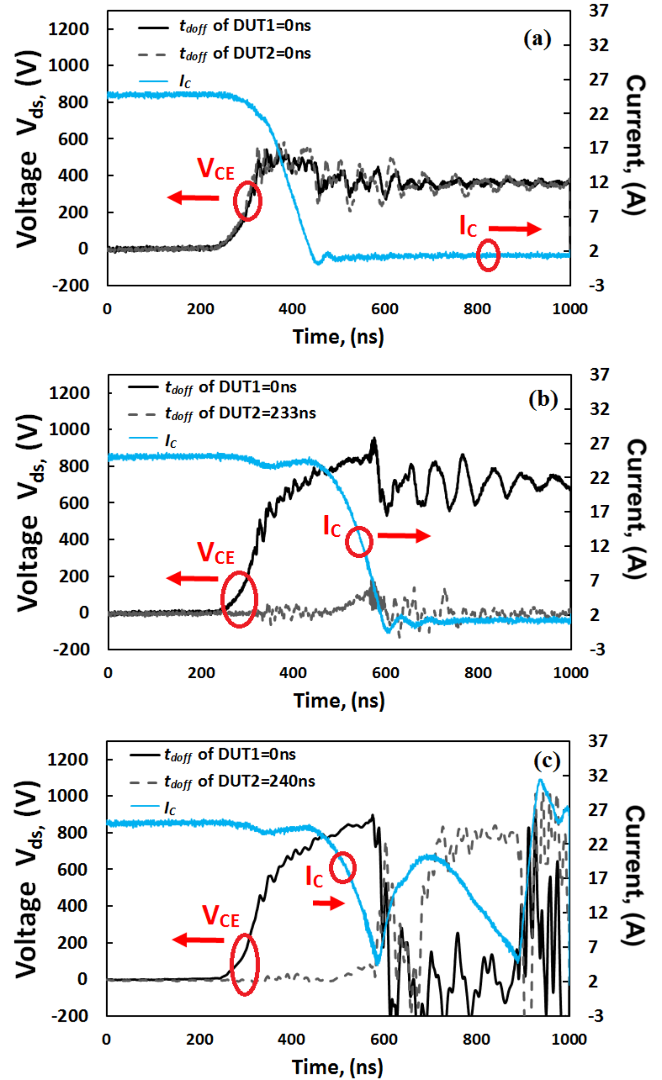


Fig. 2. Current and Voltage waveforms of series connected silicon IGBTs during turn-OFF with (a) perfectly synchronized gates (b) 233ns gate delay pre-failure condition and (c) 240 ns gate delay leading to avalanche breakdown.

During normal conduction mode, the electron current flows from the emitter into the channel which is inverted by the positive gate voltage. A corresponding hole current is injected from the positively biased collector PN junction at the collector end of the IGBT. The electron and hole currents recombine in the voltage blocking drift region through a process known as conductivity modulation. However, as the IGBT is turned OFF and the electron current disappears, the hole current flows into the base of the NPN BJT. If the voltage drop across the p-body resistance is sufficient to forward bias the emitter-body PN junction and the sum of the combined common-base gains of the BJTs is greater than 1, then thyristor latch can occur since the NPN and PNP BJTs are cross-coupled. In the case of series connected IGBTs, the thyristor latch-up can occur if (i) during the switching transient if uncompensated holes trigger the NPN BJT and (ii) if the critical field across the voltage blocking junction is

exceeded thereby causing uncontrolled electron-hole pair generation leading avalanche via impact ionization.

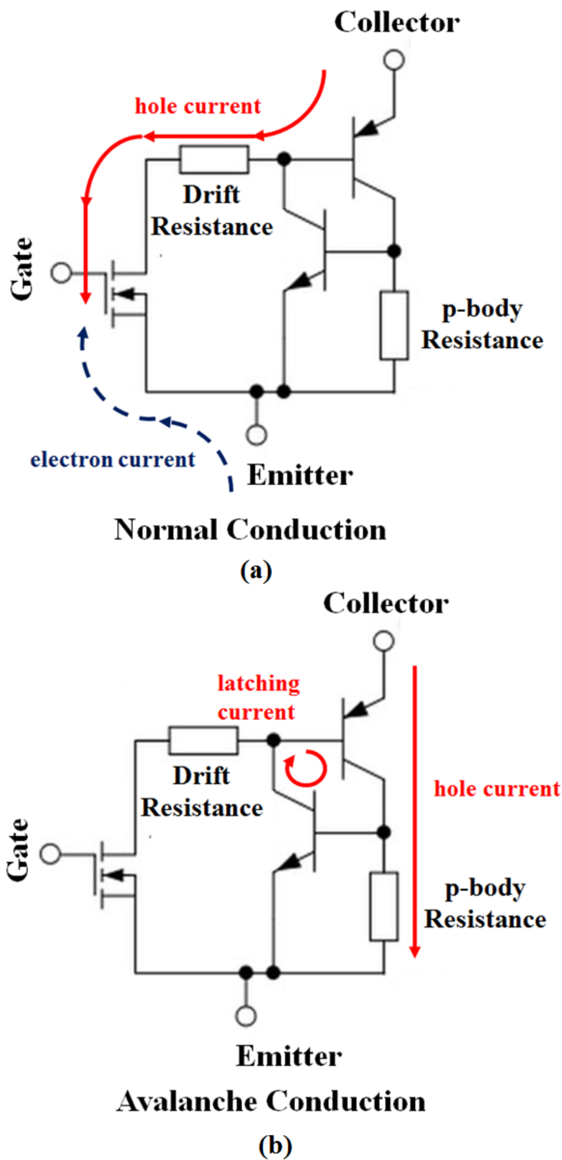


Fig. 3. Equivalent circuit of the IGBT showing the parasitic NPN BJT as well as the drift and p-body resistances. (a) under normal conduction mode and (b) under avalanche conduction mode.

The measurements of the series connected IGBTs have been repeated over a wide range of switching rates by using different gate resistances. It was observed that increasing the switching rate reduces the magnitude of the gate delay required for thyristor latching and destructive failure. This is because the peak inductive voltage overshoot during turn-OFF increases with the switching rate, hence, the potential for latching and destructive failure increases concomitantly.

The measurements of the turn-OFF transient for series connected IGBTs that were done for several switching rates is shown in Figure 4(a) for a DC link voltage of 650V and (b) for a DC link voltage of 700V. Fig. 4 shows the ratio of the peak measured voltage to the breakdown voltage of the device as a function of switching rate and the maximum gate mismatch delay before failure under latch-up. In both Fig. 4(a) and 4(b), the shaded regions on the plots indicate measurement points where destructive failure through thyristor latching occurred. Hence, the SOA of the series pair is clearly identified in both plots. The general trends show that the SOA reduces as the DC link voltage is increased and that there is a trade-off between the need to increase the switching rate (to reduce switching losses) and the maximum allowable delay in gate signaling between the series pair. The SOA reduces with increasing DC link voltage and increasing switching rate. The SOA plots can be very useful for converter design engineers that need to know the limits of the gate signaling delay in active gate drive systems.

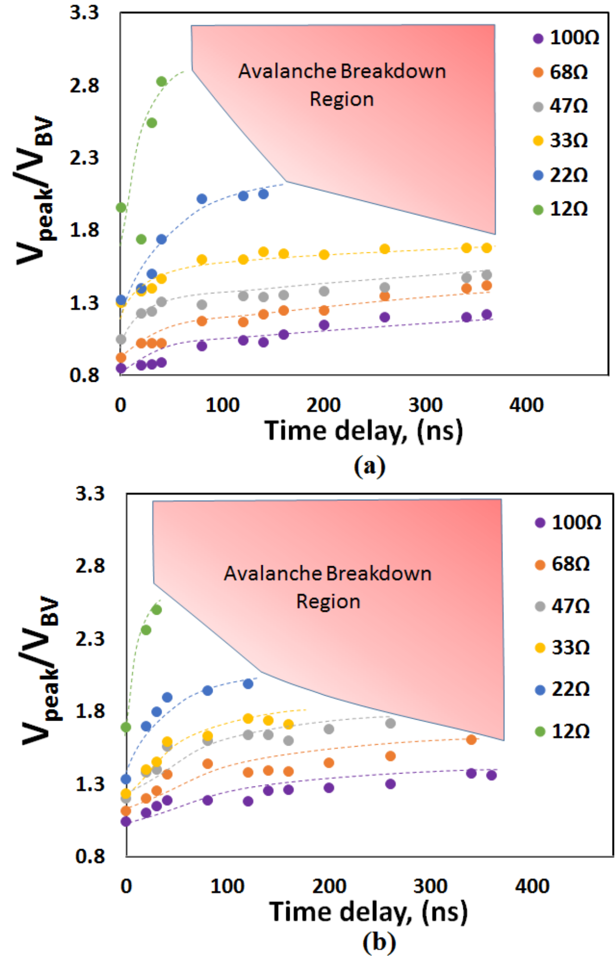


Fig. 4. Ratio peak measured voltage to rated breakdown voltage as a function of the gate signaling delay. (a) 700V (b) 650V.

Similar measurements have been done on SiC MOSFETs. The gate signaling delay was varied over a wide range for series connected 650V SiC trench MOSFETs at 700V DC link voltage. The turn-OFF transient voltage and current waveforms for the series devices are shown in Figure 5(a) for perfectly timed gate signals and 5(b) for a maximum delay of 240 ns. Unlike the silicon IGBTs, the SiC devices did not undergo avalanche failure. SiC MOSFETs are known to be more avalanche capable as various investigations have shown that the devices can dissipate larger amounts of avalanche energy without latch-up. Although the switching rates are higher (hence the turn-OFF voltage waveforms are prone to have higher inductive voltage overshoots) the larger headroom in the blocking voltage is critical in ensuring the SiC MOSFETs do not undergo avalanche during desynchronized turn-OFF of series connected devices. It also

important to note that temperature imbalance between the series devices can become critical since the switching rates in SiC are known to be temperature sensitive [9, 10].

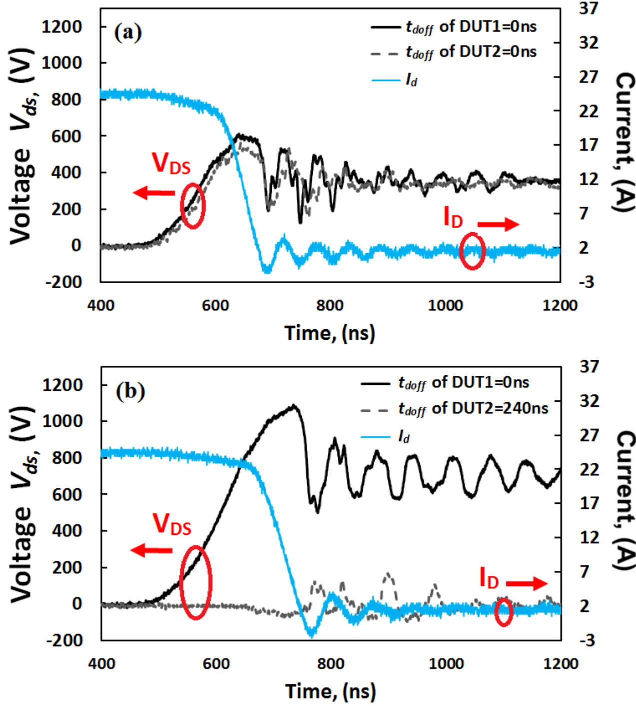


Fig. 5. Current and Voltage waveforms of series connected SiC trench MOSFETs during turn-OFF with (a) perfectly synchronized gates and (b) 240 ns gate delay leading to avalanche breakdown.

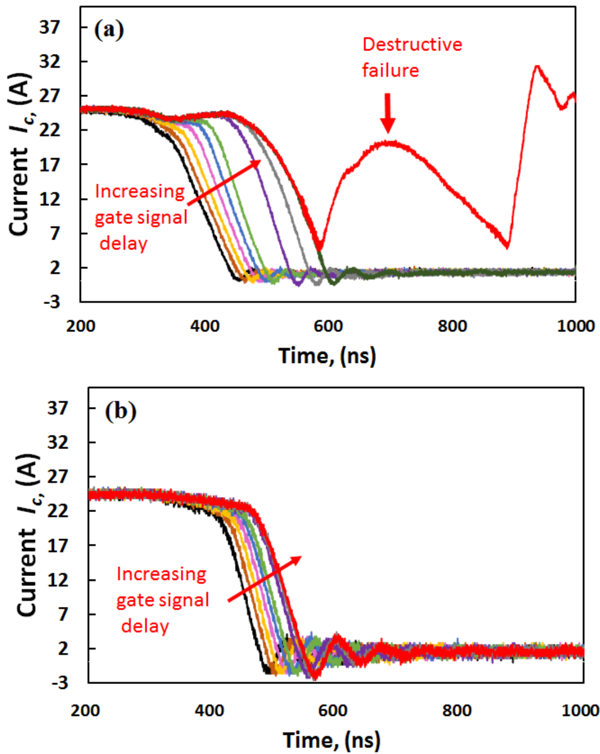


Fig. 6. The turn-OFF current waveforms through the series connected devices for different gate signaling delay for the (a) silicon IGBT and (b) SiC MOSFET.

Fig. 6 shows the turn-OFF current waveforms with different magnitudes of gate mismatch delay for the series Silicon IGBT in 6(a) and the series SiC trench MOSFET in 6(b). The rightward shift of the current waveform is due to increasing gate mismatch delay. It can be seen that the turn-OFF current waveform shifts rightwards in time and for the silicon IGBT, the current rises uncontrollably during turn-OFF for the longest gate signaling delay (240 ns). The sudden rise of current at 600 ns is due to the IGBT latch-up.

IV. Finite Element Modelling

Finite element simulations using SILVACO TCAD have been performed to validate the failure hypothesis of IGBT during transient switching under clamped inductive load. The circuit shown in Fig. 1(a) has been simulated in ATLAS from SILVACO using the mixed mode circuit application to solve the switching transients with the finite element model. Finite element simulations have been performed on Si IGBTs and SiC MOSFETs under clamped inductive load to gain a deeper insight into the physics of device failure with two series connected devices.

A. Series connected Si IGBTs

The silicon IGBT is simulated with a drift layer doping of 1×10^{14} cm^{-3}, a p-body doping of 7×10^{16} cm^{-3}, buffer layer doping of 1×10^{18} cm^{-3} and a voltage blocking drift layer thickness of 83 µm. Fig. 7 shows the cross-section view of Si IGBT which was modelled in SILVACO and the vertical cut-line through the channel under the gate to the p-body down to the collector of the device. Fig. 8 shows the simulated voltage transients for the series connected IGBTs switched at different gate delays (0ns, 300ns).

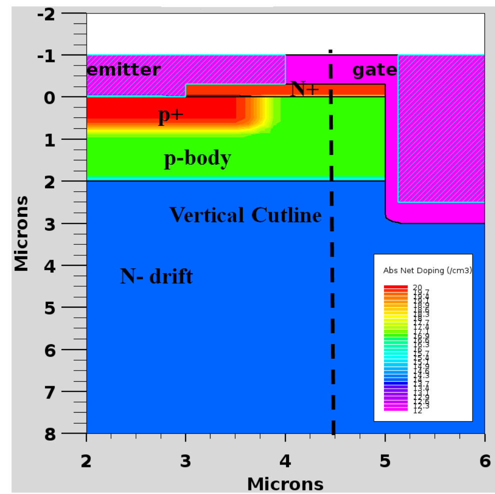


Fig. 7. Si Trench IGBT model rated at 900V

Fig. 8 shows the simulated voltage and current transient of the series connected silicon IGBTs extracted from the mixed-mode circuit in SILVACO. It can be seen from Fig. 8 that that the simulated collector voltage divergence rates between the series devices replicate the experimental measurements shown in Fig. 2(b). Seven points in the transient waveform have been identified as can be seen below. The internal electric field along the cross-section of the device (shown along the cut-line in Fig. 7) is extracted at these time intervals to show the internal fields during turn-

OFF. At point t5 in Fig. 8, the maximum blocking voltage of the IGBT is reached. In experimental IGBTs (where thousands of internal cells conduct current in parallel) where several IGBT cells are paralleled in the main device, failure would occur before this point due to current non-uniformity [11]. However, since a single IGBT cell is being simulated, thyristor latch-up is not properly emulated.

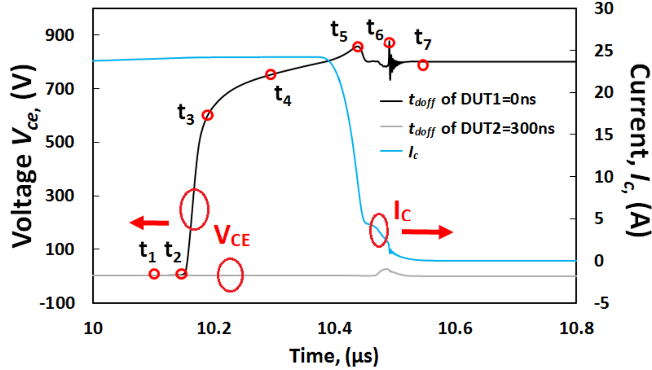


Fig. 8. The simulated current and voltage waveforms of series connected Si IGBTs during turn-OFF with 300 ns gate delay leading to avalanche breakdown.

Fig. 9(a) and 9(b) show the simulated internal electric field across the fast and slow IGBT at different stages of the turn-OFF transient, as it blocks voltage across the reverse biased PN junction.

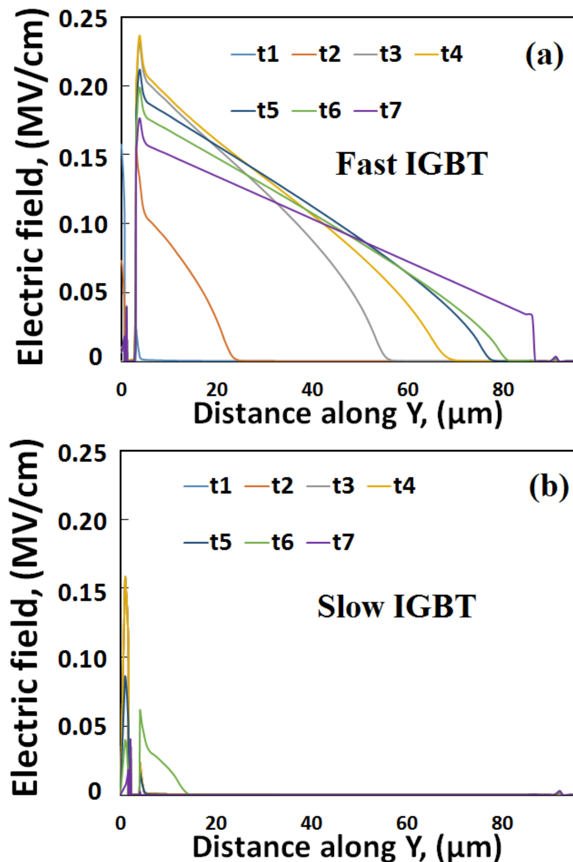


Fig. 9. Internal Electric field simulation (a) fast IGBT (b) slow IGBT

The fast switching IGBT, as shown in Fig. 9(a) has an internal electric field that spreads across the device and depletes holes from the drift region. In the slow switching IGBT shown in Fig. 9(b), the internal electric field is at a minimim, hence, there is no depletion of holes from the drift region.

The hole concentration profile at different time steps shows the process of formation of depletion region during the switching transient in Figure 10(a) and (b). It can be seen that the faster device is depleted quicker, the depletion region forms completely in this device whereas in the slower device there are some charge still remaining in this region. Hence, the faster device has higher blocking voltage.

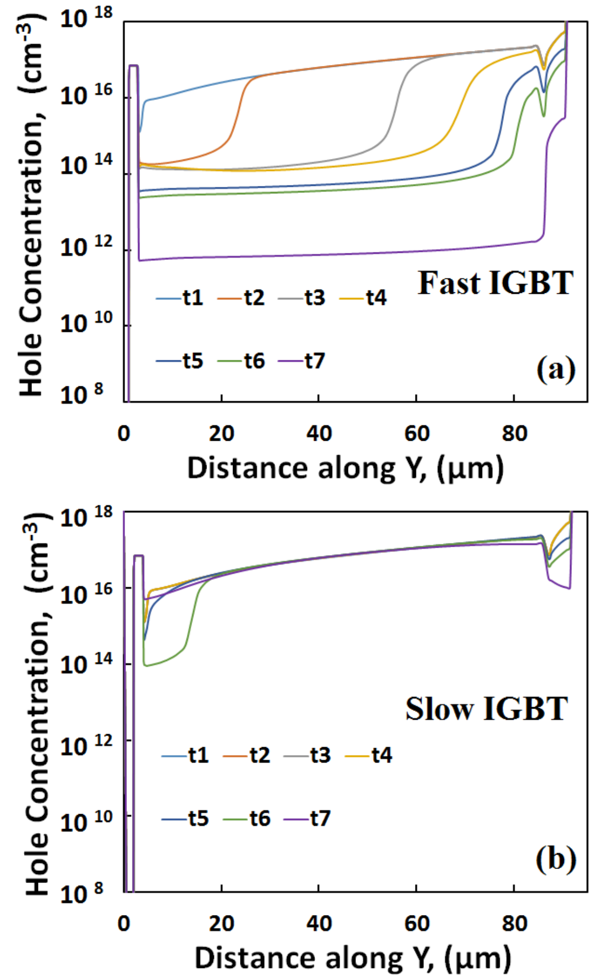


Fig. 10. Hole concentration simulation (a) fast IGBT (b) slow IGBT

B. Series connected SiC MOSFETs

The SiC device in the simulation was optimized to a breakdown voltage of 1200 V using a ~9 μm depletion layer with a doping of 2×10^{16} cm^{-3}. A gate oxide thickness of 80 nm, a source doping of 1×10^{18} cm^{-3} and p-body doping of 1×10^{17} cm^{-3} was used in the simulation. The simulated voltage and current turn-OFF transients as shown in Fig. 12 where significant ringing in the output characteristics can be observed. This is due to resonance between the parasitic capacitance in the SiC MOSFET and the parasitic inductance added to emulate the package inductance.

Ringing in SiC MOSFETs is a well characterized switching hazard [12].

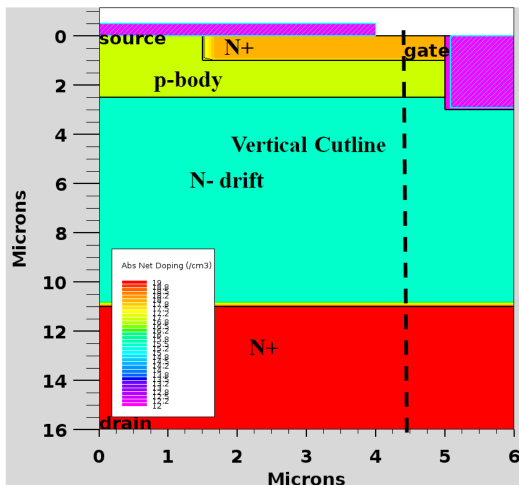


Fig. 11. SiC Trench MOSFET model rated at 1200V

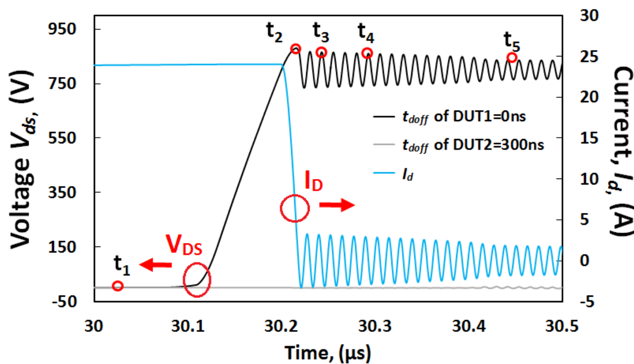


Fig. 12. The simulated current and voltage waveforms of series connected SiC MOSFETs during turn-OFF with 300 ns gate delay leading to avalanche breakdown.

Fig. 13 shows the simulated internal electric fields of the series connected SiC trench MOSFETs. The internal electric fields were extracted along the vertical cross-section of the SiC MOSFET at the time intervals t1 to t5 shown in Fig 12. Like the Si IGBTs, the fast switching device has a higher internal electric field compared to the slower switching device. It can also be observed that the electric fields in the SiC MOSFETs are much higher (approximately 10 times higher) that those in the Si IGBTs. This is due to the significantly thinner drift region in the SiC MOSFET that is enabled by the higher critical fields. This is an intrinsic property of SiC as a material. SiC MOSFETs have parasitic BJTs and not thyristors, hence, latch-up involves the triggering of the internal NPN BJT. If during turn-OFF, the voltage limits of the device are exceeded, avalanche mode conduction will occur which may trigger NPN BJT latch-up.

V. Conclusion

Series connected devices are used for blocking higher voltages. Snubbers are typically used for static and dynamic voltage balancing however active gate drive systems do not use snubbers, hence, it is important to develop a technique for determining the SOA for series connected devices. Gate timing mismatch (loss of gate synchronization) can cause destructive failure from avalanche conduction. Experimental measurements and simulations have been used to investigate the SOA of series connected silicon field-stop IGBTs and SiC trench MOSFETs. The SOA is reduced by increased switching rates and DC link voltages. For a given switching rate, the maximum gate mismatch between the series devices to trigger avalanche induced failure reduces with increasing DC link voltage. Likewise, for a given DC link voltage, the maximum gate mismatch delay for triggering avalanche mode failure reduces with increasing switching rate. Hence, as far as maximizing the SOA is concerned, there is a trade-off between the DC link voltage and the switching rate.

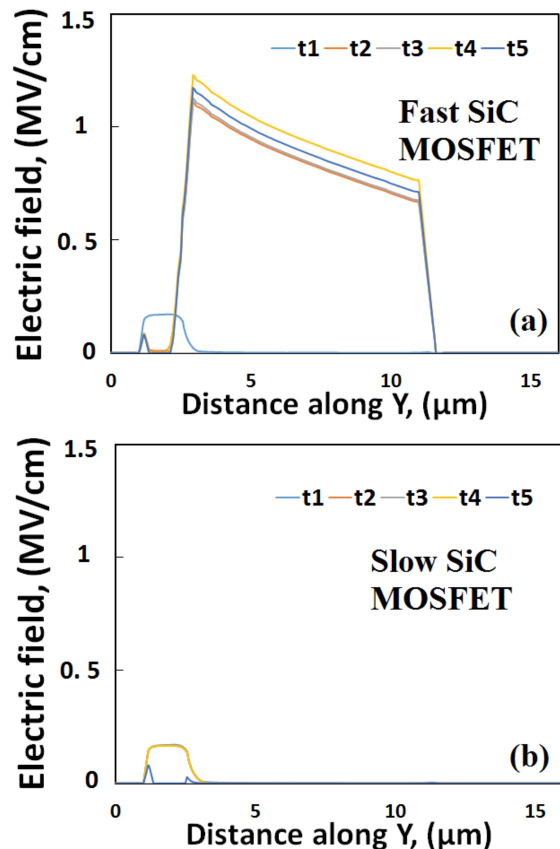


Fig. 13. Internal Electric Field (a) fast SiC MOSFET (b) slow SiC MOSFET

Acknowledgment

The research here was supported by the Engineering and Physical Science Research Council (EPSRC) through the following projects (EP/R004366/1) and (EP/L021579/1).

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