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Recoverable electrical breakdown strength and dielectric constant in ultra-low *k* nanolattice capacitors

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ABSTRACT: The dielectric reliability of low *k* materials during mechanical deformation attracts tremendous attention owing to the increasing demand for thin electronics to meet the ever-shrinking form factor of consumer products. However, the strong coupling between dielectric/electric and mechanical properties limits the use of low-*k* dielectrics in industrial applications. We report the leakage current and dielectric properties of a nanolattice capacitor during compressive stress cycling.

Measuring electrical breakdowns during the stress cycling, combined with a theoretical model and *in-situ* mechanical experiments, provide insights to key breakdown mechanisms. Electrical breakdown occurs at nearly 50% strain featuring a switch-like binary character, correlated with a transition from beam bending and buckling to collapse. Breakdown strength appears to recover after each cycle, concomitant with nanolattice's shape recovery. The compressive displacement at breakdown decreases with cycling due to permanently buckled beams, transforming conduction mechanism from Schottky to Poole-Frankel emission. Remarkably, our capacitor with 99% porosity, k ~ 1.09 is operative up to 200 V whereas devices with 17% porous alumina films breakdown upon biasing based on a percolation model. Similarly with electrical breakdown, the dielectric constant of the capacitor is recoverable with five strain cycles, and stable under 25% compression. These outstanding capabilities of the nanolattice are essential for revolutionizing future flexible electronics.

KEYWORDS: *Nanolattice capacitor, Electrical breakdown, Dielectric constant, Buckling, Poole-Frenkel emission*

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Developing and integrating reliable low-*k* materials is a key challenge for next generation interconnect[1,2] and wireless communication[3–6] technologies. Lowering the dielectric constant *k* which has commonly been enabled by introducing pores into the dielectric material[7,8] decreases the resistance-capacitance (RC) delay, reduces power consumption, reduces cross-talk between nearby interconnects in integrated circuits (ICs)[9–11], and increases the bandwidths in antennas by preventing surface wave propagation[12]. Lowering the *k* through increasing porosity often degrades intrinsic electrical reliability[13], and leads to a higher leakage current and lower dielectric breakdown voltages along with other physical properties including mechanical integrity, thermal stability, and dielectric loss.[7,8] Despite extensive research efforts, no material has successfully broken the negative link between the physical and dielectric properties of the materials.[7,8]

The electrical and dielectric reliabilities of low-*k* materials under stress require characterization due to the increasing popularity of thin and flexible electronic devices in a wide-variety of technological areas, such as batteries[14–18], transistors[19–21], electrodes[22,23], displays[24], biosensors[25–29] and biomedical instruments[30–32]. These devices are required to undergo large mechanical deformation in use that includes bending, stretching, twisting, and folding while maintaining reliable high performance of the devices. These reliabilities are of great concern in manufacturing of the ICs, particularly the cool-down procedure in the back-end-of-line (BEOL) processes that induce thermal expansion.[33] Porous low-*k* films have shown a large degradation in both reliabilities under mechanical stress, and after unloading the stress, both leakage current and dielectric constant were not recovered.[34]

A vertical-type three-dimensional (3D) nano-architected hollow-beam alumina capacitor demonstrated a substantial improvement of physical properties, and achieved the lowest reported *k* of 1.06 – 1.10 at 1 MHz in the 1% density regime.[35] This architected

capacitor emerges as a potential solution for current low-*k* materials because it provided stable *k* values over the voltage range of -20 to 20 V and a frequency range of 100 kHz to 10 MHz, with excellent mechanical properties such as a Young's modulus of 30 MPa, a yield strength of 1.07 MPa, a nearly full shape recoverability after >50% compressions, and outstanding thermal stability with a thermal coefficient of dielectric constant (TCK) of 2.43×10^{-5} K^{-1} up to 800 °C.[35]

In this work, we fully and for the first time investigated the electrical and dielectric properties of these nanolattice capacitors under electrical and mechanical stress. We probed the leakage current of a 8 μm-tall hollow-tube alumina nanolattice capacitor with octet architecture, comprised of a 8 μm-wide layer of unit cells subjected to cyclical loading to strains of 0 – nearly 50%. Quantifying the conditions that resulted in electrical breakdown combined with a phenomenological model provides insights into the uniquely reliable response of such nano-architected materials under mechanical strain, including the high strength, binary nature, recoverability and degradation of the electrical breakdown, and recoverability of dielectric properties.

We fabricated vertical-type nanolattice capacitors to probe the electrical properties of nano-architected materials under stress. Figure 1a shows a schematic depicting the nanolattice capacitor with a single 8 μm octet geometry unit cell layer with a monolithic top plate, fabricated by two-photon lithography[36] as detailed in Methods. The planar top area and height of the nanolattice are 350×350 μm^2 and 8 μm, respectively, as exhibited in Figures 1b,c. A bright-field (BF) transmission electron microscopy (TEM) image and the corresponding selective area diffraction (SAD) pattern of an alumina tube of the nanolattice indicate that the nanolattice is mostly comprised of an amorphous matrix with nano-grains in the size range of 2 ~ 10 nm.

To understand the effect of nanolattice strain on the electrical properties, we measured

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the electric breakdown field (E_{BD}) and current density (J_{BD}) of a nanolattice capacitor while applying a compressive strain along the top of the capacitor using a specially-designed tungsten probe tip. The cross-sectional area of the 550 μm-diameter tip is approximately 2 times larger than the top area of the capacitor, whose surface roughness is +/-20 nm as measured by Atomic force micrscopy (AFM) (Figure S1), which enabled conformal contact and homogeneous displacement. During the experiments, the strain was gradually increased as the underlying substrate moved upwards with a step size of 500 nm while the tip maintained its position of full top contact. After reaching a displacement of 3500 nm, the sample was unloaded to remove all strain over the same increments until the sample reached its initial height (Figures 2a,b). The breakdown field was measured as the current density abruptly jumps, and can be classified as either a partial breakdown, marked by the first sudden increase in current of at least one order of magnitude, or a full breakdown, which indicates the onset of a metallic conducting state. We observed only partial breakdown events for all displacements below 2500 nm, with slight and gradual increases in J_{EBs} (up to 7×10^{-5} A/cm^2) for the electric field values beyond E_{BDs} and overall J as the displacement increases. Displacements greater than 2500 nm resulted in decreases in E_{BD} and drastic increases in J_{BD} up to 7 A/cm^2, (the compliance current for this experiment), which indicate full breakdowns (Figure 2c). It is evident that both trends are recovered upon unloading, which demonstrates that the capacitor regains the ability to maintain a voltage across its electrodes.

To understand the evolution of the electrical response to mechanical deformation, we mechanically cycled the capacitors nine times. Figure 3b shows the E vs. J plots of the unloaded capacitor after their return to initial height from each cycle. No breakdown events were observed before or after the first cycle due to the maximum voltage limit of the experiment. Partial breakdowns occurred in the 2nd and 3rd cycles while full breakdowns were observed in the 4th cycle and beyond. Figure 3c depicts a 3D representation of the full

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E_{BD} with displacement and cycle number. Data points do not exist for experiments where electrical breakdowns were not observed during voltage sweeps. Points that equal zero designate short circuits that led to full breakdowns. Images in Figure 3d show that non-recoverable deformation and cracks formed beyond the 4th cycle where instantaneous breakdowns occurred.

It has been shown that DC conduction of Al_2O_3 at high electric fields can be described by the space charge limited conduction (SCLC) model[37,38] where electrons or holes are injected into the material via the electrodes and alter the local space charge distributions. Such conditions can create a conducting path within the material such that the local internal electric field exceeds the breakdown voltage of the material, and this conducting path can lead to global electrical breakdown of the material, characterized by a drastic increase in measured current. We developed a simplified phenomenological model with corresponding qualitative finite element analysis (FEA) maps to estimate the local electric field within the nanolattice capacitor. We modeled a stationary 2D slice of the hollow ceramic nanolattices with the voltage difference between the terminal and ground as 100 V, equal to the condition of Figures 2c,d. The terminal and ground were designated as the top and bottom boundaries, respectively, and were assigned the default material parameters for gold. The 10 nm shell members were designated as alumina with an $\varepsilon_r = 8$.[39] All remaining components are designated as air ($\varepsilon_r = 1$). The model involves solving both Gauss' law and the electrical potential equations as follows:

$$\nabla \cdot D = \rho_V \quad (1)$$

$$E = -\nabla V \quad (2)$$

where D is the electric flux density, ρ_V is the volumetric charge density, E is the electric field, and V is the voltage.

We modeled five geometric cases to match the mechanical deformation morphology that evolves during cyclic testing of the capacitor (Figure 4) (see Details in Methods). Each case has a corresponding SEM image in panel I and an FEA image that shows the norm of the electric field in panel II. The areas marked by the red and blue rectangles on each image in panel II are magnified in panels III and IV, respectively. The initial undeformed case is illustrated in Figures 4a-c. The local electric field within the undeformed beam is uniform and designated as 100%. We explored three intermediate deformation mechanisms: Beam bending, partial beam buckling and full beam buckling. The model for this regime uses 1000 nm of displacement, which qualitatively represent the cases of displacement between 0 and 3500 nm in the experiments. The first mechanism is beam bending, (Figures 4d-g) where both walls of the hollow tube bend and remain roughly parallel. This model estimates the local electric field to be higher than the breakdown field above the point of bending in the shell and lower below this point. The lower half of the unit cell has a field that is 110% of the original, which is caused by reducing the plate separation at the same voltage. This does not lead to a continuous pathway of higher electric field, and thus is not likely a contributor to decreasing the required breakdown field. The second deformation case is partial beam buckling, (Figures 4h-k) which gives rise to the similar effect as beam bending; the local electric field is 107% of the original field above the initiation of buckling and 96% of the initial field below. The lower half of the unit cell also has a field that is 110% of the original. Like in the first case, there is no continuous pathway of increased electric field, which would result in greater breakdown susceptibility. The final intermediate deformation case is full beam buckling (Figures 4l-o), which can occur after repeated compression cycles where the hollow tube fails to recover its original shape. In this scenario, the higher electric field in the top shell above the wrinkling vertex comes into contact with the relatively unchanged electric field of the bottom shell below the vertex. Similar to the previous scenarios, the lower half of

the unit cell has a field that is 110% of the original. This scenario creates a potential continuous pathway of increased electric field, which can result in a lower effective breakdown strength. The fifth and final scenario describes the geometry at the maximum displacement of the experiment (Figures 4p-r). At this displacement, the top half of the unit cell is completely compressed, resulting in the conductive tip contacting the plane of nodes that are positioned at roughly half the height of the structure. This effectively removes the entire pathway along the top half of the structure and creates a direct pathway between the tip, the shell below the node, and the substrate. Additionally, the applied field reaches its maximum value, almost twice what was found in the undeformed case, due to the decreased plate separation.

This simple model lends insights into the three main experimental observations: (1) the binary character, (2) recoverability, and (3) degradation of the electrical breakdown. The binary nature (observation (1)) of the full-breakdown response within a cycle could be explained by the transition from beam bending and buckling to lattice collapse, which disrupts the continuous current pathway with an increased local electric field. Once the tip is in contact with the node halfway down the structure, a large increase in field as shown in the model leads to a full electrical breakdown. This suggests that within the first cycle, the capacitor behaves as a switch – it either breaks down according to the structural and material breakdown strength or behaves as a short circuit once the tip reaches the node. No full breakdowns are observed before this displacement in the cycle, since there is no large increase in the internal electric field in a continuous conduction pathway through the structure. For the partial breakdowns that occur at displacements below 3000 nm in the first cycle (Figures 2c,d), only some of the beams in the top-half of the unit cell experience full beam buckling, which forms a limited number of continuous pathways, and the number of the beams increases with the displacement, as reflected by the increase in leakage currents at

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intermediate plateaus of electrical breakdown, partial electrical breakdowns (Figures 2c,d).

The recoverability of electrical breakdown (observation (2)) is correlated with the material regaining most of its breakdown strength after each cycle (Figure 3b). Hollow alumina nanolattices have been ubiquitously shown to recover structural shape, and the capacitor may be able to reverse its collapsed state upon recovery and break the continuous pathways that caused breakdown. We note that despite the lattice recoverability, the overall current level increases with increasing the number of cycles, representing some damage might be accumulating in the junctions of the nanolattice. The displacement at which electrical breakdown occurs (observation (3)) decreases with cycling. This observation could be explained by the accumulation of fully buckled beams which cause continuous pathways of increased local electric fields. As each cycle introduces an increasing number of beams which are fully buckled and no longer recover, the number of pathways for breakdown increases and the electrical performance subsequently degrades.

Further expanding the correlation between the electrical breakdown behavior and mechanical degradation properties of the capacitor, Figure 3e shows the normalized energy dissipation, defined as the line integral along the stress-strain curve for a given cycle, normalized recovered height, and full E_{BD} at zero displacement as a function of cycle number. Normalized recovered height characterizes the structure's shape recovery after stress is applied and energy dissipation is linked to the material's ability to relax stress. Both characteristics scales with structural deterioration as they both depend on defects accumulated during cycling. Figure 3e shows energy dissipation and height recovery decrease by 61.6 % and 18.8%, respectively, between the 1st and 2nd cycles during which no full electrical breakdown occurs. This steep mechanical signature is likely due to initial nodal fractures followed by subsequent hinge-like deformation (Figure S2). Subsequent cycles display marginal lowering of recoverability (approximately 10% and 20% for the normalized

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4 recovered height and energy dissipation, respectively for the entire periods of 2nd to 10th
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6 cycles.), indicating that the primary permanent deformation occurs during the initial
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8 compression. Full electrical breakdown first occurred in the 4th cycle and subsequently the
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10 capacitor becomes completely short-circuited beyond the 7th cycle. Such discrepancy
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12 between mechanical and electrical breakdown behavior can be explained as follow. With
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14 increasing cycling, more beams in the top-half of the unit cell form direct current pathways
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16 close to the nodes, which ultimately replicates the case at which the conducting tip is in
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18 contact with nodes, leading to an immediate breakdown at a low E_{BD}. Beam buckling helps to
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20 prevent further fracture of nodes and tubes by relaxing the stress as exhibited in Figure 3d.[36]
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22 A sufficient number of nodal connections remain intact to enable the structure to recover its
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24 height and to preserve the amount of energy dissipation. To confirm this hypothesis, we
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26 measured the decrease in the height of the capacitor after 7 mechanical cycles with biasing up
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28 to 100 V. The cross-sectional SEM image (Figure S3) indicates the height decreases by about
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30 25 % which is similar to the value when only 7 mechanical cycles are engaged as shown in
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32 Figure 3e. Therefore, electrical breakdown is facilitated by deterioration of beam structure
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34 through buckling while the mechanical degradation is linked to failure at the nodal regions.
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36 Examining and quantifying the effect of compressive stress on the dielectric properties
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38 of nano-architected capacitors, that have been demonstrated to possess mechanical, thermal,
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40 and dielectric stability, is of critical importance.[35] We measured the capacitance of an 8 μm
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42 single unit cell layer nanolattice in this work using a Keithley 4200-SCS impedance analyzer,
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44 with 5 stress cycles (see details in Methods). Figures 5a-d show capacitance density vs.
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46 frequency plots of the fabricated sample before stress cycling, under loading of 2000
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48 nm at the 1st cycle, under unloading of 2000 nm at 5th cycle and after the 5th stress
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cycle. The data conveys that all cases exhibit similar values with nearly constant capacitance densities over the frequency range of 100 KHz to 10 MHz at an applied bias of $\pm$ 200 V. The capacitance densities of the four cases are 1.210 $\pm$ 0.006, 1.223 $\pm$ 0.006, 1.237 $\pm$ 0.010 and 1.220 $\pm$ 0.006 pF/(mm)^2, respectively, which equate to dielectric constants of 1.094 $\pm$ 0.005, 1.106 $\pm$ 0.005, 1.118 $\pm$ 0.010 and 1.103 $\pm$ 0.005, respectively (see details for calculating *k* in Supporting Information). These results indicate that dielectric constant is stable under loading of up to 2000 nm and fully recoverable up to 5 cycles beyond which the measurements of capacitance fail due to high levels of leakage current (Figures 2c,d, Figures S5a,b and Figure 3b).

Figures 5e-h show capacitance densities of the four cases as a function of bias swept from - 200 V to + 200 V at frequencies of 100 KHz, 1 MHz and 10 MHz. These plots show that the capacitance densities were stable, and the dielectric losses are below 0.061 throughout the range of frequencies and voltages used (Figures S4a-h). The C-V plots shown in Figures 5e-h were normalized by the relative capacitance as a function of applied voltage at varied frequencies to extract the voltage coefficients of capacitance (VCCs), $(C-C_o)/C_o$, where C_o is the capacitance density at zero

bias (Figures S4i-l). These measurements revealed that the VCCs were virtually non-existent, which implies that the nanolattice is stable over this voltage range. Measurements of nanolattice capacitance over 3 experiments produced approximately identical data, as conveyed in the plots in Figure 5 and S4.

To examine the dependence of compressive strain on full electrical breakdown, we doubled the applied voltage up to 200 V (the maximum bias of our system), with another nanolattice capacitor and observed that the full E_{BD} decreases with increasing strain as shown in Figure S5c (see all the data of Figures 2c,d and Figures S5a,b). By combining the known models of porosity (based on percolation model)[13] and thickness dependence[38] (see Supporting Information for deriving the integrated equation) with the previous experimental results of porous alumina films[38] (Figure S5d), we estimated the porosity value (of the alumina film normalized in the same thickness with our capacitor, 8 μm) of 16.71% at which the full E_{BD} becomes zero and above which the device with this porous material should instantly breakdown when electric field is applied. Also, the alumina film with a 16.71% porosity has a k value of 6.83 as calculated by the model in Ref. 35 (see Supporting Information). However, it is remarkable that our nanolattice capacitor with a ~ 99% porosity (when uncompressed) does not breakdown up to 0.25 MV/cm (Figures S5a,b), representing an exceptionally strong breakdown strength while maintaining an extremely small k of ~ 1.10 which is electrically stable and mechanically recoverable (Figure 5 and Figure S4).

In determining the conduction mechanisms of the capacitor before full breakdown occurs, we first focus on the data at zero displacement before and after compression cycles. Figure 3b shows two distinct regions of E before full electrical breakdown. In the low electric

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field range (0 – 0.036 MV/cm), the current density linearly increases with electric field, indicating Ohmic conductions (OCs) (Figure 6a, see the definition of Ohmic conduction mechanism in Supporting Information), and mechanical cycling leads to higher conductivity. This increase in conductivity might be caused by a greater number of electronic defect states with mechanical cycles, forming shallower traps (efficient sites for electrons to hop; see the schematic in Figure 6h) that generate a current even at room temperature.[40] Beyond the Ohmic regime, the Schottky emission (SE) dominates the conduction mechanisms for the leakage current before the 1st cycle (Figure 6b), and the Poole-Frankel emission (P-FE) controls the mechanism after the 1st cycle (Figure 6c). These mechanisms are confirmed by linear correlations between $ln(J/T^2)$ and $E^{1/2}$ for SE and $ln(J/E)$ and $E^{1/2}$ for P-FE. The effective dielectric constant, k of ~ 1.07±0.05 calculated by this method is consistent with the measured value shown above, for the SE mechanism before loading and the P-FE mechanism after loading. (see the definitions of the SE and P-FE mechanisms in Supporting Information) Since SE defines a mechanism for “electrode-limited conduction” and P-FE describes “bulk-limited conduction” as shown in Figures 6i,j,[33,41] the transition from SE to P-FE indicates the creation of trap (defect) states in the capacitor during the cycle. The number of states accumulates with the cycle, leading to an increase in the y-intercept values of the plots after each cycle (Figure 6c). The identical trends are observed in the leakage current during loading. As exhibited in Figures 6d-g, the conduction initially shows Ohmic behavior (Figures 6d,e) followed by characteristics of the P-FE mechanism (Figures 6f,g) with the level of the current density gradually increasing as the displacement becomes larger. Similarly, this behavior is due to the increased conductivity that is attributed to the defect sites [40] and/or the strain under compression.

The investigation presented here provides critical insights into the unique electrical

breakdown behaviors, conduction mechanisms, and dielectric properties of hollow alumina nanolattices under cyclic compressions to nealy 50 % strain. We discovered that this material maintains a stable dielectric breakdown strength, and recovers a substantial portion of its breakdown strength for a given displacement within a few cycles. Similar trends also observed in dielectric properties. These features could provide a pathway to increase resilience of devices that have to function in extreme environments. For example, such reversibility in both electrical and dielectric properties may offer opportunities to rescue data in memory after an electrical and/or mechanical failure without using complicated and expensive restoration processes and facilities. Finally, the simple model used in our work suggests that it may be possible to utilize the breakdown voltage as a diagnostic tool to characterize the mechanical integrity of architected dielectric materials.

Methods

Sample fabrication**:** Low-density octet geometry nanolattices comprised of 8 μm unit cell and a monolithic top plate were designed in computer-aided design (CAD) software. Utilizing this code, IP-DIP 780 polymer nanolattice scaffolds were created using two-photon photolithography (TPL) direct laser writing (DLW) in the Photonic Professional TPL-DLW System (Nanoscribe GmbH) on Si wafers coated with titanium (12 nm) and gold (80 nm). These polymer nanolattices were then coated with a 10-nm-thick atomic layer deposition (ALD) alumina film in a Cambridge Nanotech S200 ALD System using H_2O and trimethylaluminum (TMA) precursors. The interior polymer nanolattice scaffold was then removed by using a focused ion beam (FIB) system (FEI Versa 3D) to remove portions of the outer alumina coating and placing the sample in a Diener Zepto oxygen plasma system for several hours. The top electrode was formed by depositing titanium (12 nm) followed by gold

(80 nm) on top of the structure. This results in a vertical capacitor with an interior dielectric material composed of a hollow 3D ceramic nanolattice. The maximum 2D size for each nanolattice was typically 350 μm × 350 μm.

Electrical measurements**:** The measurements for dielectric and electrical properties of 3D-ceramic nanolattice were carried out with a semiconductor characterization system (Keithly 4200-SCS connected to a 4210-CVU multi frequency capacitance-voltage unit). For dielectric properties, a voltage range of -200 to 200 V and a frequency range of 100 kHz to 10 MHz were applied while for electrical properties, a range of voltage up to 200 V was engaged. To avoid applying stress to the nanolattice from contact and from thermal expansion of the material during the impedance measurements, we used flexible thin tungsten hair pins (diameter = 0.4 μm) and a specially designed stage which controls its height with a step of 100 nm, allowing us to monitor the measurement using a high resolution optical microscope (OM). The resolution of the OM is 300 nm. To effectively measure the electrical reliability under stress, we used a rigid tungsten tip that can measure electricity with simultaneously giving compressive stress to the nanolattice. We performed a voltage sweep at 0.16 V/s while measuring the current at each displacement. To confirm the tip does not significantly press the nanolattice at the condition of no displacement, we compared the currents measured by the rigid and the flexible tips in the range of voltage from 0 to 200 V, and found that the two currents are similar in a range of deviations of ± 5% and both cases show Ohmic conduction.

Mechanical Measurement**:** Energy absorption and recovery height measurements were performed by cyclically compressing nanolattice capacitor structures quasistatically using a flat punch tip in an in-situ InSEM Nanomechanical Module (Nanomechanics, Inc.) attached to a Quanta SEM (ThermoFisher Scientific) to 3500nm of maximum displacement for 10 cycles.

Modeling for electrical reliability**:** COMSOL multiphysics 5.3 (COMSOL Inc.) using

the electrostatics package was utilized following the configuration described in the text.

ASSOCIATED CONTENT

Supporting Information

Supporting Information is available from free of charge on the ACS Publications website.

A thorough description of the dielectric constant, VCCs, and an analytical model to calculate dielectric constant using relative density, conduction mechanisms, a model integrating the dependence of porosity and thickness on breakdown strength as well as additional figures.

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Author Contributions

M.-W.K. and M.L.L. have contributed equally to this work.

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Main Figures

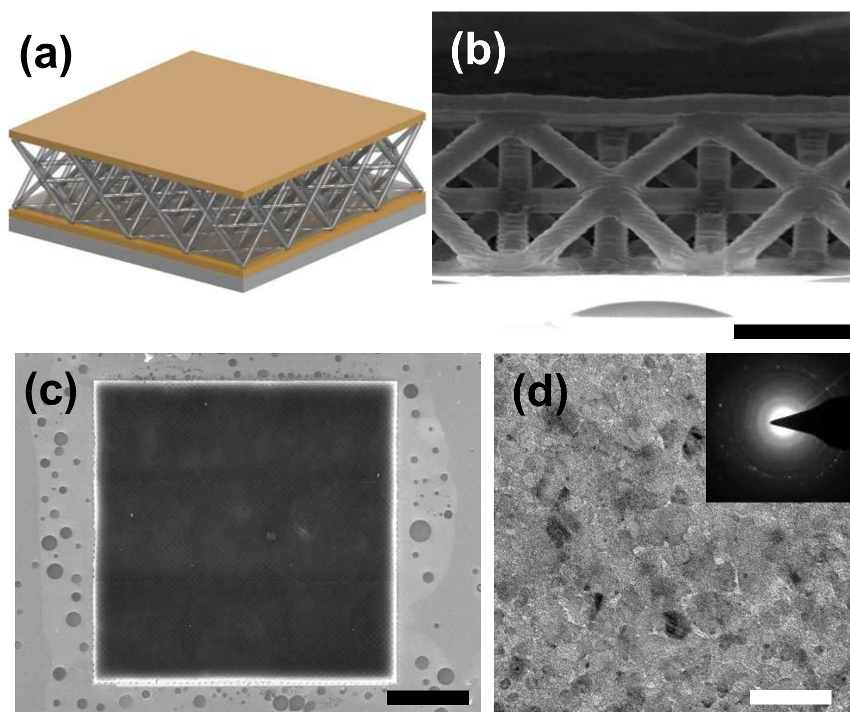

Figure 1. Architected alumina nanolattice capacitor (a) Schematic of the octahedron nanolattice capacitor with top and bottom electrode layers. (b, c) Side-and top-view SEM images of a fabricated nanolattice capacitor (a 8 μm single unit cell layer, 8 μm sample height and 350 × 350 μm^2 planar top), respectively. The scale bars of Figures 1(b,c) are 5 and 100 μm, respectively. (d) TEM bright field image of an alumina tube. The corresponding SAD pattern is shown in the inset of the image. The scale bar is 50 nm.

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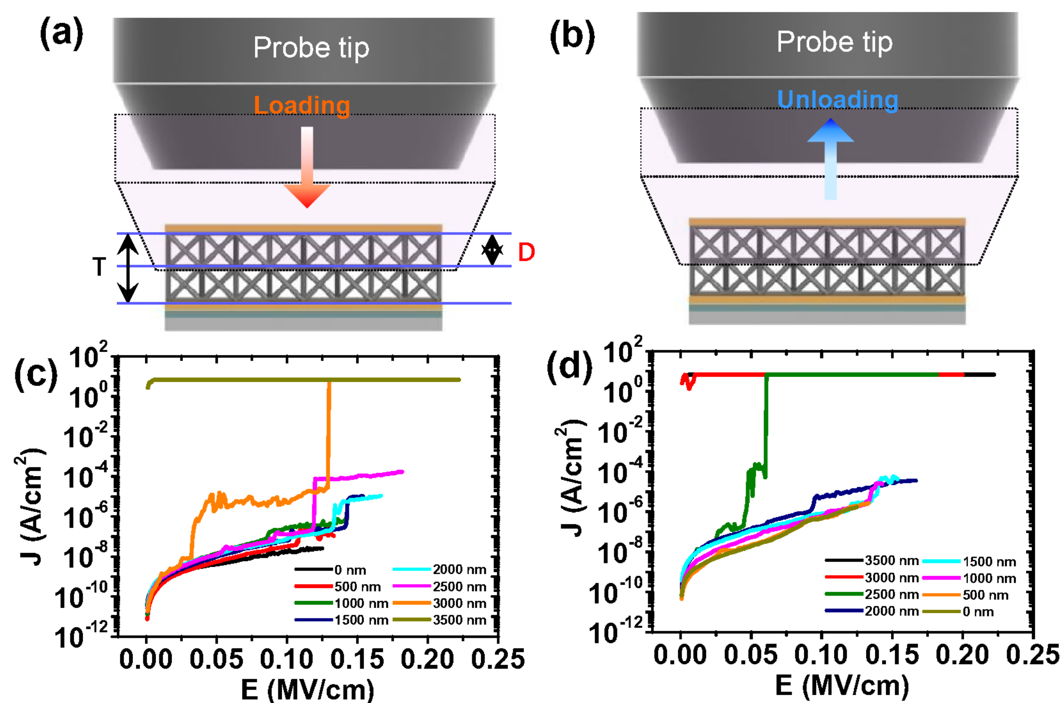

Figure 2. Electrical reliability tests for the 1st stress cycle. (a, b) Schematics of the electrical reliability tests of the nanolattice capacitor under loading (compressive stress) and unloading (removing the stress), respectively. Note that the T is the initial height of sample and D is the displacement of tungsten probe. (c, d) Representative current density (J) vs electric field (E) plots of the nanolattice capacitor under various displacements during loading (c) and unloading (d) the stress, respectively.

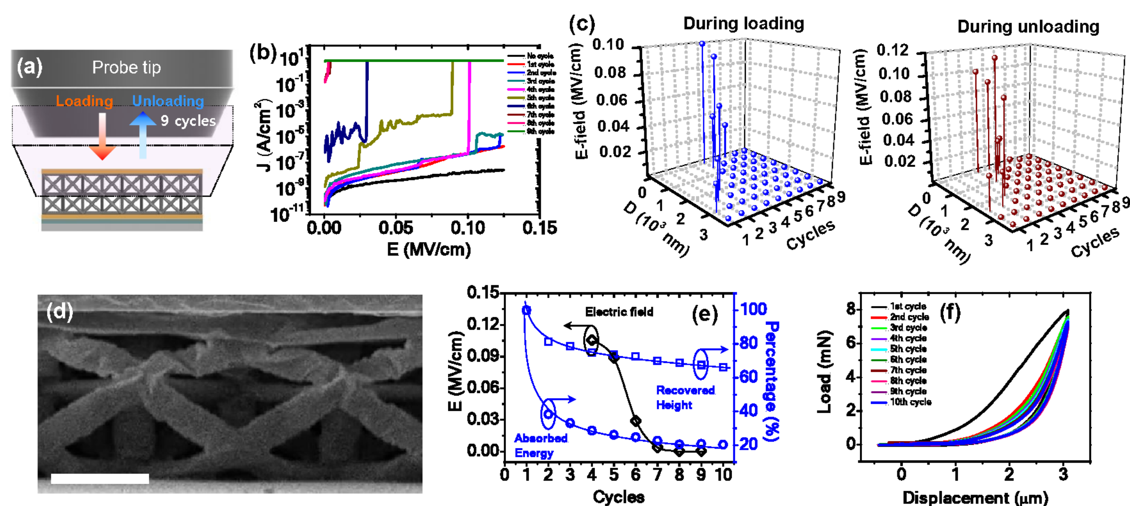

Figure 3. Electrical reliability tests of the nanolattice capacitor for repeated stress cycles and their analyses. (a) A schematic of the electrical reliability tests for 9 cycles. (b) The J vs. E plots at the initial height (with no displacement) after each of the cycles. (c) The profiles of full-breakdown fields during loading and unloading processes as a function of the displacement (D) and cycle. (d) The cross-sectional SEM image of the nanolattice capacitor after 9 compression-cycles. The scale bar is 4 μm. (e) The normalized absorption energy, recovered height and full-breakdown fields as a function of the cycles. (f) Load-displacement plots of the capacitor showing the recoverability of their shape with an initial large drop in energy absorption, followed by a plateau, up to 3500 nm of displacement during the repeated cycles for 10 times.

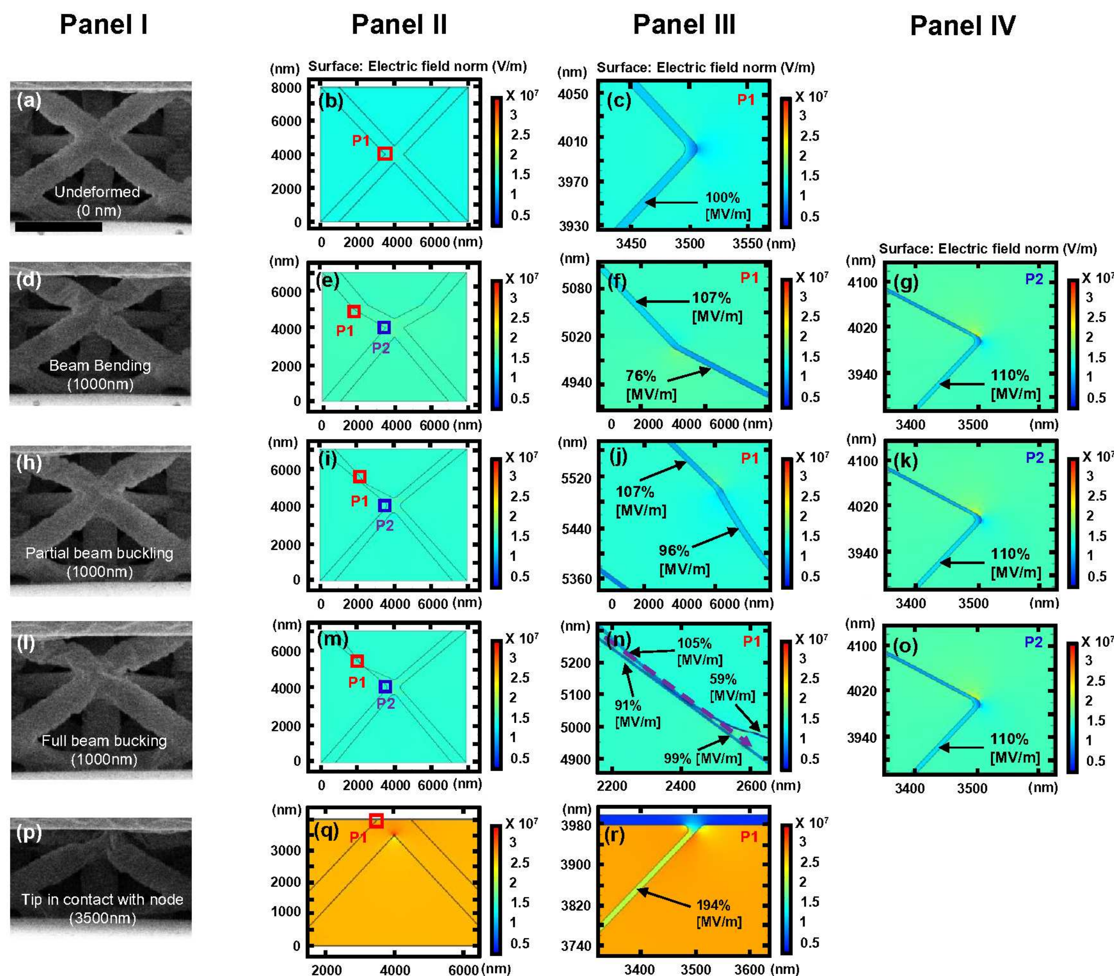

Figure 4. FEA simulation results of the five representative geometric cases of the nanolattice capacitor in different regimes of compressive stress with matching images from *in-situ* mechanical experiments. (a-c) Undeformed case at no displacement. (d-n) Three intermediate deformation cases occurring at 1000 nm of displacement as a representation for the cases of displacements between 0 to 3500 nm: (d-g) Beam bending, (h-k) Partial beam buckling and (l-o) Full beam buckling cases. (p-r) Full displacement case at 3500 nm of displacement where the tip comes into contact with the halfway plane of nodes. The panel I and II show the cross-sectional SEM image corresponding to the each case and the FEA image for the norm of the electric field. The panel III and IV show the magnified images that are marked by the red and blue rectangles, respectively, in panel II. The scale bar in Figure 4(a) is 4 µm.

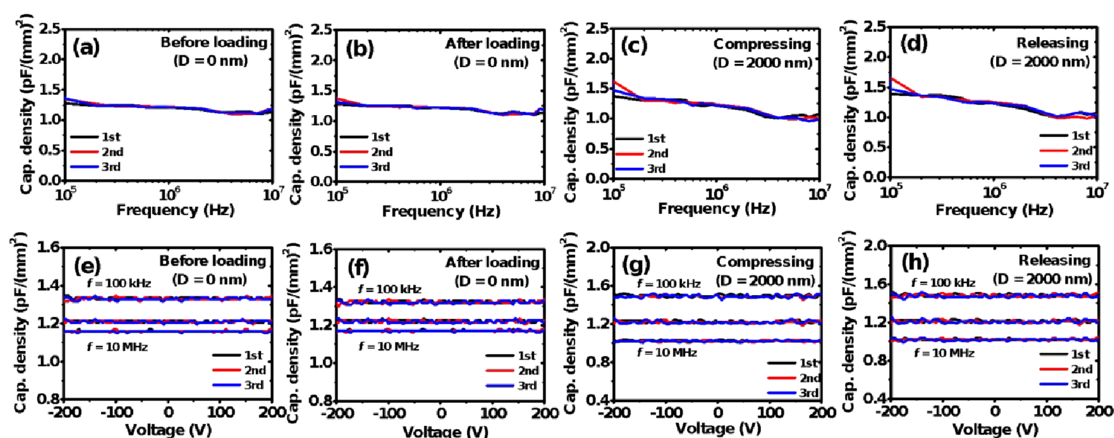

Figure 5. Dielectric properties of the nanolattice capacitor measured before cycling, during loading of 2000 nm at the 1st strain cycle, during unloading of 2000 nm at the 5th stain cycle, and after the 5th strain cycle (no strain): (a-d) Capacitance density vs. frequency plots. (e-h) Capacitance density vs. voltage plots at frequencies of 100 KHz, 1 MHz and 10 MHz.

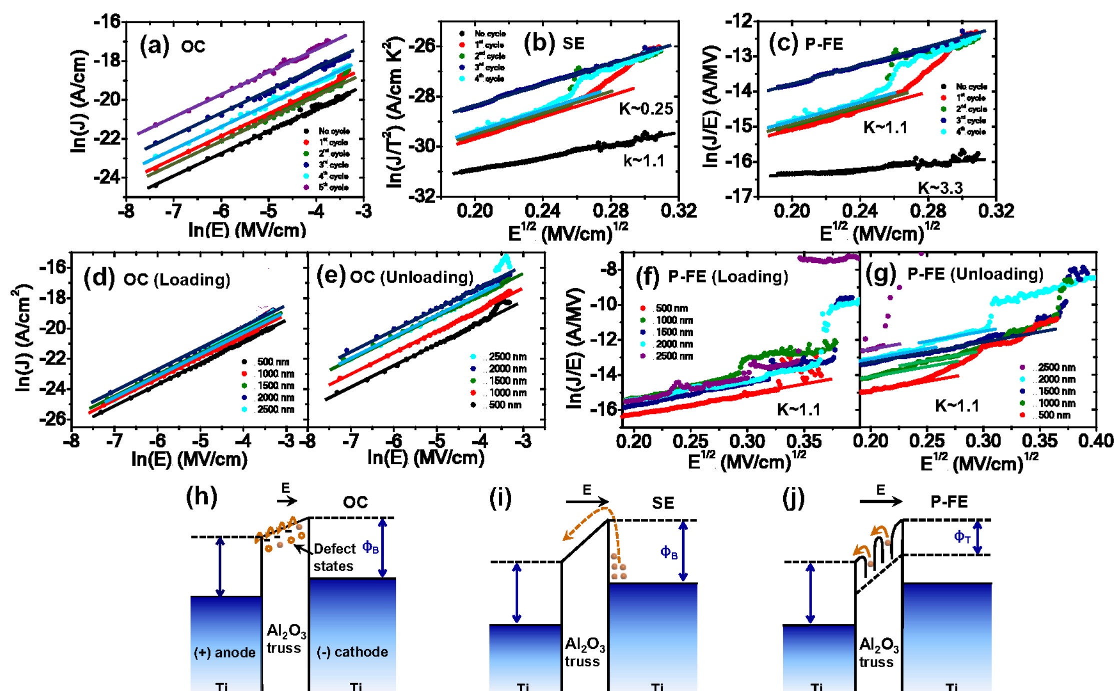

Figure 6. Conduction mechanisms of the nanolattice capacitor prior to full breakdowns: Leakage data obtained before stress cycling and after the cycles shown in Figures 6(a-c) and those acquired during the cycles with varied displacements shown in Figures 6(d-g). (a) Plots of the leakage current varying linearly with electric fields at 0 – 0.036 MV/cm (Ohmic conduction (OC)). (b, c) Plots of $ln(J/T^2)$ and $E^{1/2}$ and $ln(J/E)$ and $E^{1/2}$ beyond the Ohmic conduction regime. The former is for SE and the latter is for P-FE. (d, e) Plots of the leakage current varying linearly with electric fields at 0 – 0.036 MV/cm (Ohmic conduction (OC)). (f, g) Plots of $ln(J/E)$ and $E^{1/2}$ beyond the Ohmic conduction regime. (h-j) Schematic illustrations of electrical conduction mechanisms of OC, SE, and P-FE, respectively.

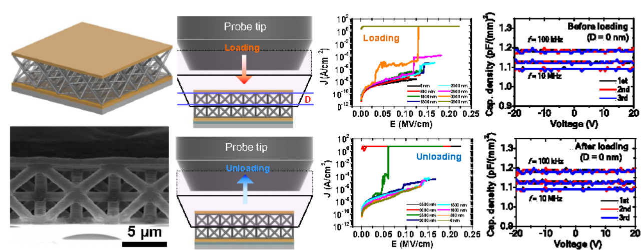

Table of Contents