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High Temperature Silicon Carbide Mixed-signal Circuits for Integrated Control and Data Acquisition

A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor Philosophy in Electrical Engineering

by

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Bangladesh University of Engineering and Technology
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This dissertation is approved for recommendation to the Graduate Council.

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Abstract

Wide bandgap semiconductor materials such as gallium nitride (GaN) and silicon carbide have grown in popularity as a substrate for power devices for high temperature and high voltage applications over the last two decades. Recent research has been focused on the design of integrated circuits for protection and control in these wide bandgap materials. The ICs developed in SiC and GaN can not only complement the power devices in high voltage and high frequency applications, but can also be used for standalone high temperature control and data acquisition circuitry.

This dissertation work aims to explore the possibilities in high temperature and wide bandgap circuit design by developing a host of mixed-signal circuits that can be used for control and data acquisition. These include a family of current-mode signal processing circuits, general purpose amplifiers and comparators, and 8-bit data converters. The signal processing circuits along with amplifiers and comparators are then used to develop an integrated mixed-signal controller for a DC-DC flyback converter in a microinverter application. The 8-bit SAR ADC and the 8-bit R-2R ladder DAC open up the possibility of a remote data acquisition and control system in high temperature environments. The circuits and systems presented here offer a gateway to great opportunities in high temperature and power electronics ICs in SiC.

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Dedication

I would like to dedicate this work to my family – my mother, father, brother, sister-in-law, and my lovely nephew and niece, Naveed and Nayara. They are my biggest inspiration and they make want to be a better person in my life by showing courage, love and compassion in their own.

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CHAPTER 1 INTRODUCTION

1.1 Background

Fast switching, high temperature and high voltage electronics for power converter and system applications have become one of the most promising fields of research in analog and mixed-signal integrated circuits design. As power electronics and power conversion circuits have moved towards power devices that can withstand higher temperatures and faster switching frequencies, the need for control and protection circuits that can withstand similar environmental conditions has grown. This has led to the development of integrated circuits in other semiconductor materials, such as silicon on insulator (SOI), gallium nitride (GaN), gallium arsenide (GaAs), silicon carbide (SiC) and various others [1]. Each of these materials comes with a unique combination of advantages and disadvantages, leading to the different materials carving out their own individual niches of applications in the IC industry. Among these, GaN and SiC have shown excellent promise as rugged and high temperature IC material [2], [3]. And having a material that can be used for high temperature integrated circuits has opened the prospect of data sensing and acquisition as a real possibility in high temperature and extreme environment applications. A SiC data acquisition system will lead to better control and operation of high temperature systems used in applications such as deep earth drilling, heavy transport, aviation and aerospace.

1.2 Alternatives to Silicon

From the very start of the semiconductor revolution silicon has been the ‘go to’ material for all major commercial and industrial designs. Over the years the fabrication and validation process for silicon ICs has been perfected to a point where highly complex Si ICs can be very stable and dependable while fitting onto the tip of a humauman finger. As device features become

ever so smaller, Si digital and analog ICs have become faster and more compact. However, the operation of Si ICs is limited in terms of temperature because of the intrinsic properties of silicon, namely its bandgap energy, thermal conductivity and electric field breakdown voltage. Because of these properties, silicon has been limited to ambient temperature applications of up to 150 °C. This limitation has led to the aforementioned migration to other materials like SOI, SiC and GaN [4].

The first of these alternatives and the one most similar to silicon is SOI. The separation from the bulk with an isolation layer of oxide decreases the surface area of the source and drain junctions, thus lowering the leakage associated with these junctions. This allows SOI circuits to be more immune to high temperature environments. The silicon FETs also allow SOI circuits to behave more like Si circuits. This operational resemblance with Si and the added ruggedness due to device structure has allowed SOI circuits to operate at temperatures as high as 225 °C without any special cooling system. These circuits range from power FET gate drivers [5]-[7] to extreme environment applications [8].

1.3 The Future of Silicon Carbide ICs

Recent research has explored the possibility of using wide bandgap semiconductor materials such as silicon carbide (SiC) and gallium nitride (GaN) to replace traditional Si and SOI integrated circuits in extreme environment applications. Given that these wide bandgap semiconductors are already the preferred power devices for high temperature, high voltage, fast switching, and high efficiency power conversion systems, a transition to wide bandgap ICs has long been suggested [2], [4]. The use of wide bandgap materials could facilitate the packaging of control and protection circuits with power devices in one single package which would significantly reduce parasitics in the module and allow much higher switching frequencies and better efficiencies.

All these benefits make both GaN and SiC attractive IC processes for the near future. GaN ICs have shown great promise for high frequency switching applications such as radio frequency communication [9], [10] and power conversion [11]. SiC ICs have mostly concentrated on high temperature applications, with some circuits having been reported above 500 °C and up to 600 °C [12].

1.4 SiC Circuits for DC-DC Converter and Data Acquisition

This work is a part of two projects – the first is a project under grant #IIP1237816 by the National Science Foundation Building Innovation Capacity (NSF-BIC) aimed at exploring the design of analog and mixed-signal circuits in SiC at high temperature. The other project is under the NSF EPSCoR initiative with VICTER (Vertically-Integrated Center for Transformative Energy Research), under grant #EPS-1003970, which aims to provide a controller and gate driver solution for a solar microinverter. A family of mixed-signal SiC circuits including amplifiers, comparators and current-mode signal processing circuits have been developed to implement a sliding mode controller for the DC-DC flyback converter.

The solar microinverter is specified to supply a single-phase output. The DC-DC flyback converter will be operated with a sliding mode control scheme, with an input of 25 ~ 35 V from the 60 cell PV panel, at a nominal output voltage of 200 V and current of 0.5 ~ 1.0 A. The flyback converter uses a 1:6 pulse transformer and the nominal switching frequency is 50 kHz.

The signal conditioning and control circuits developed to implement the controller are generic enough that they can be adapted to be used in other control schemes. A pair of data converters – an 8-bit R-2R ladder DAC and an 8-bit successive approximation register (SAR) ADC – were also developed as part of the design. These data converters can not only provide a mixed-

signal interface with a SiC digital controller, but also can form the basis of a remote data acquisition system in high temperature and extreme environment applications. These circuits have been designed in the CMOS 1.2 μm HiTSiC process developed by Raytheon Systems Limited.

1.5 Dissertation Structure

The dissertation is divided into the following chapters.

- Chapter 1: Introduction – Motivation and background of the work are presented here.
- Chapter 2: Silicon Carbide and SiC ICs – A description of the SiC IC process is presented in this chapter. The Raytheon HiTSiC CMOS process and its devices are discussed, as well as circuits already designed in this process and other SiC processes.
- Chapter 3: Circuit and Systems Overview – A brief overview of the basic analog building block circuits for the controller is presented here. Typical topologies and parameters of the analog-to-digital and digital-to-analog converters are explained. The DC-DC flyback converter and the basics of the sliding mode control are also described.
- Chapter 4: Design and Simulation – This chapter describes the complete design process – determining the specification of the circuits from system requirements, developing design equations and using them to build schematics, and simulation and layout of the circuits.
- Chapter 5: SiC IC Test Results – This chapter lists the test results from the analog building block circuits, the data converters and the all-analog DC-DC controller.
- Chapter 6: Conclusions and Future Work – A summary of the design and test results is presented in this chapter. Contributions to the state of the art as well as methods and goals for future development of high temperature SiC ICs are also discussed.

CHAPTER 2 SILICON CARBIDE AND SIC ICS

2.1 Silicon Carbide and Its Properties

Silicon carbide is a compound of silicon (Si) and carbon (C). Over the last two decades SiC and other wide bandgap devices have started to replace silicon in power electronics applications as the power device of choice. The inherent properties of SiC, GaN and other wide bandgap devices make them better candidates for high power and high temperature applications than the traditional silicon power devices [12], [13].

2.1.1 Properties of SiC

Silicon carbide has many polymorphs – the three most common are 3C-SiC (also known as β-SiC), 4H-SiC, and 6H-SiC. Some of their key properties are listed in Table 2.1 [13].

Table 2.1. Properties of Wide Bandgap Semiconductors along with Silicon

Material	Bandgap Energy E_g (eV)	Intrinsic Carrier Concentration n_i (cm^{-3})	Di-electric Constant ε_r	Electron Mobility μ_n ($cm^2/V.s$)	Critical Electric Field E_c (MV/cm)	Thermal Conductivity λ (W/cm.K)
Si	1.1	1.5×10^{10}	11.8	1350	0.3	1.5
Ge	0.66	2.4×10^{13}	16	3900	0.1	0.6
GaAs	1.4	1.8×10^{6}	12.8	8500	0.4	0.5
GaN	3.39	1.9×10^{-10}	9	900	3.3	1.3
3C-SiC	2.2	6.9	9.6	900	0.2	4.5
4H-SiC	3.26	8.2×10^{-9}	10	720^a 650^c	2	4.5
6H-SiC	3	2.3×10^{-6}	9.7	370^a 50^c	2.4	4.5

Note: a – mobility along a-axis, c – mobility along c axis.

Some of the properties of the 4H-SiC and 6H-SiC that stand out from the table are –

- A three times higher bandgap energy than silicon – a higher bandgap leads to a lesser generation of carriers in the depletion region, which in turn reduces the leakage current.
- An almost ten times higher critical electric field than silicon – a higher critical electric field translates to a higher breakdown voltage. This means SiC devices can withstand considerably higher voltage across it than their silicon counterparts.
- A three times higher thermal conductivity than silicon – a higher thermal conductivity means the semiconductor can dissipate heat more easily. Hence, while silicon power devices can operate up to 150 °C, SiC devices have the potential to go much higher than that.
- The higher critical electric field and thermal conductivity lead to another advantage – low device resistance and the possibility of faster switching. A SiC device can be a tenth of the size of a silicon device with the same voltage rating – with the thinner device providing the opportunity for higher operating frequencies. With many power generation applications based on switching converters and inverters, SiC and GaN provide much better solutions than traditional silicon [15].

These distinct advantages over silicon in high voltage and high temperature power applications have led to a significant amount of use of silicon carbide in a variety of power generation systems. An all-SiC 800 kHz, 1 kW, 800 V output boost DC-DC converter has been reported operating at 320 °C [16]. The module used in this application integrates a SiC MOSFET and SiC Schottky diode. SiC power device (JFET, MOSFET and BJT) performance in matrix converters have been compared with Si IGBT and have been found to offer much lower switching losses [17]. SiC JFETs, Schottky diodes, BJTs and MOSFETs have been evaluated and found to

outperform traditional silicon power devices at high voltage and high temperature for a variety of other applications [18]–[20].

2.1.2 Bandgap Energy and Electron Mobility

Two key performance criteria for any semiconductor device are the bandgap energy and the electron mobility. A comparison of these two in the cases of silicon and silicon carbide is described in this section.

The bandgap energy is defined as the gap between the top of the valence band and the bottom of the conduction band. As seen in Table 2.1, SiC has a much higher bandgap energy than silicon (almost thrice). The intrinsic carrier concentration of Si and 4H-SiC over temperature are shown in Fig. 2.1.

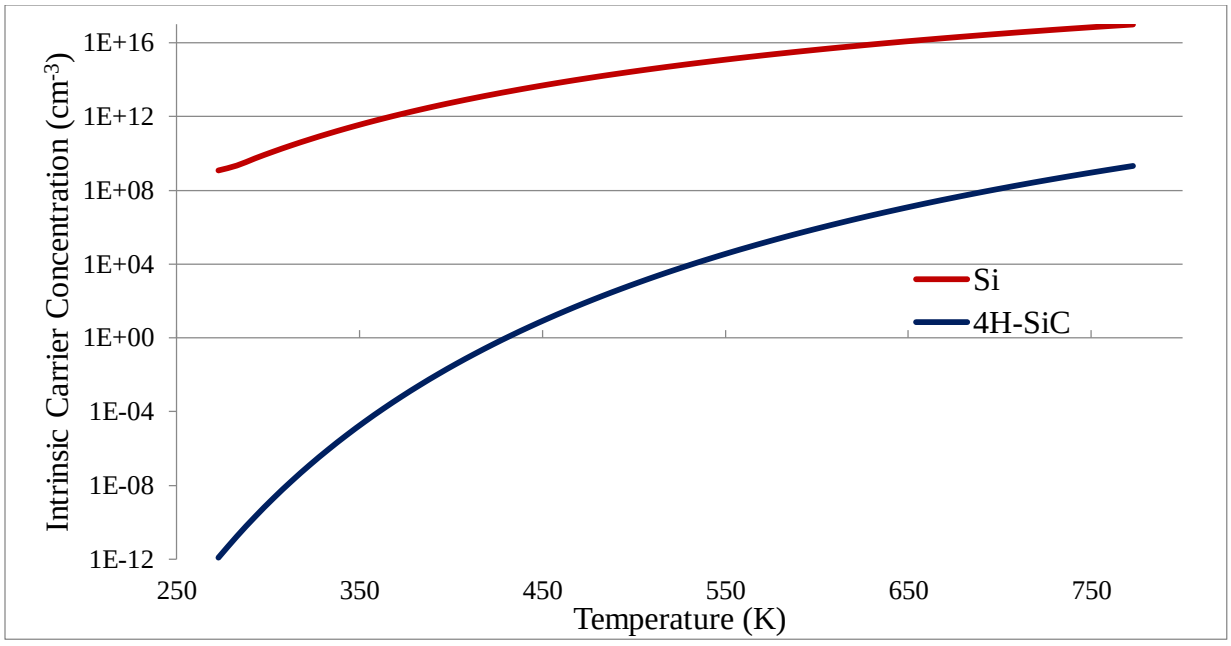


Fig. 2.1 Intrinsic carrier concentration over temperature for Si and 4H-SiC.

The silicon intrinsic carrier concentration reaches upwards of 10^{16} cm^{-3} at temperatures over 400 °C, which makes it pretty much unusable as a semiconductor at high temperatures. The

intrinsic carrier concentration of SiC, on the other hand, is very small at lower temperatures and rises to around 10^{10} cm^{-3} at 500 °C, making it an ideal candidate for a semiconductor at high temperatures.

The other key property of a semiconductor material is its electron mobility which dictates how much current a particular device can carry. Thus, the electron mobility is an indication of how fast circuits can perform. The electron mobility of silicon and silicon carbide are plotted over *n*-type doping concentration, N_D, in Fig. 2.2.

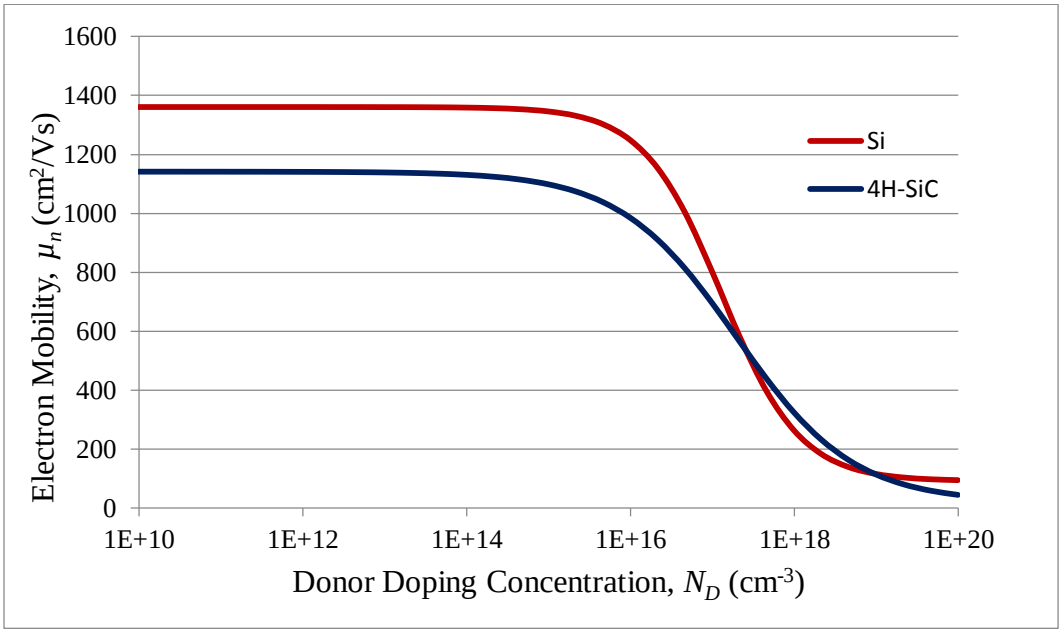


Fig. 2.2 Electron mobility over doping concentration for Si and SiC.

This is an ideal plot of the electron mobility which considers similar conditions in the silicon and silicon carbide structure. In reality, SiC suffers from material defects and artifacts that drastically reduce the mobility of the carrier charges. These defects will be discussed in the next section. Fig. 2.3 shows the effect of temperature on electron mobility for Si and SiC.

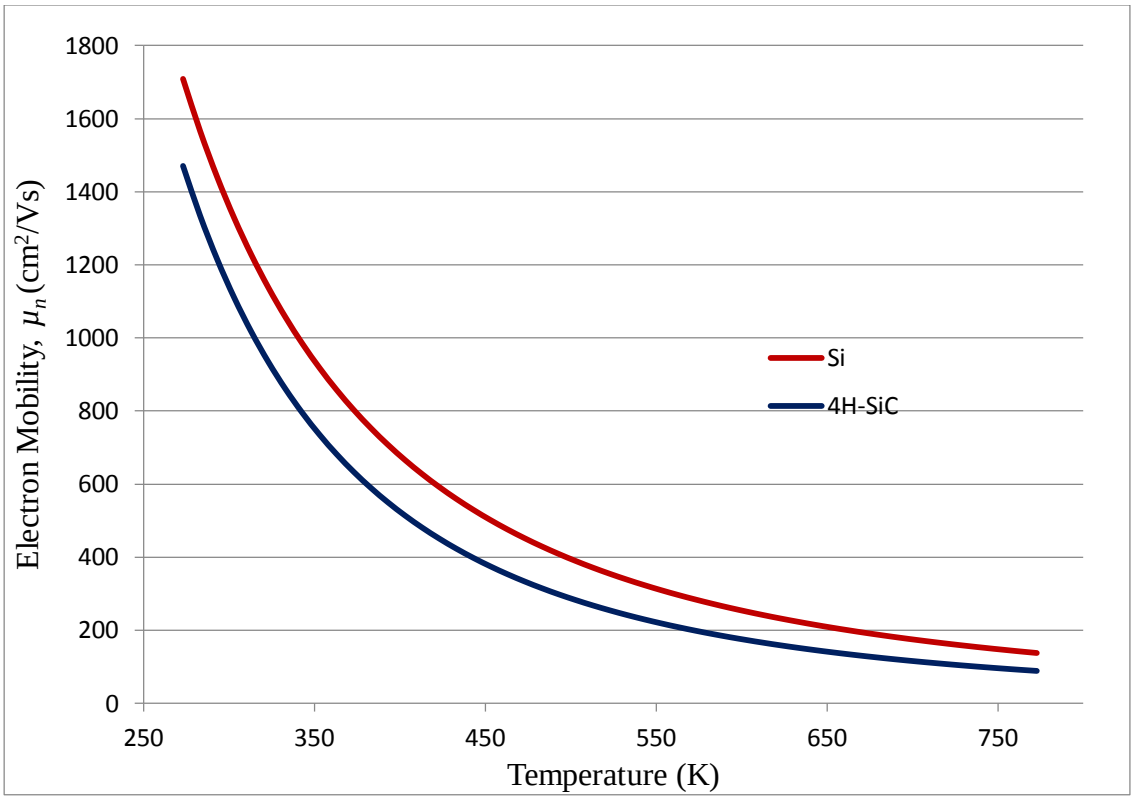


Fig. 2.3 Electron mobility over doping temperature for Si and SiC.

The behavior shown here again is for an ideal case, the presence of interface traps, discussed in the next section cause a deviation from the ideal curve in the case of SiC. To summarize briefly – SiC has a lower electron mobility than Si as well as a significantly lower intrinsic carrier concentration. This makes SiC much slower at room temperature but opens up the possibility of operation at high temperatures due to low leakage currents.

2.2 SiC Fabrication and Devices

The biggest disadvantages SiC devices have at this moment are the fabrication cost and defects in the chip. While silicon manufacturing is a very mature and well defined process, silicon carbide fabrication is still trying to achieve low cost and high reliability. Silicon carbide manufacturing provides a lot more challenges than silicon.

2.2.1 Device Breakdown

Micropipes and dislocation errors are more common in silicon carbide than in silicon. Micropipes can lead to junction breakdown at much lower than the nominal critical voltage [21]. The breakdown voltage was found to be much lower at defective sites where the impact ionization coefficients were higher than normal [22]. Impact ionization is a process where a carrier with enough kinetic energy can knock another carrier into the conduction band from the valence band. This phenomenon is used in avalanche diodes. The impact ionization coefficient, α, is a measure of how fast this 'avalanche' of carrier production will be and is given by Chynoweth's law [22], [23],

$$\alpha = ae^{-b/E} \tag{2.1}$$

where E is the electric field applied and a and b are semiconductor parameters. Generally, impact ionization coefficients in SiC become significant at electrical fields of an order of magnitude higher than that of silicon [25]. Defects not only lessen the nominal breakdown voltage but also produce a negative temperature dependence of the breakdown voltage [22].

2.2.2 Oxide and Interface Traps

Silicon carbide devices also suffer from oxide and interface traps created in the semiconductor material during the fabrication process. Traps are impurities or dislocation in the material that can trap an electron or hole until a pair is completed. Oxide traps refer to the traps in the gate oxide – these traps have been found to cause a positive shift in the threshold voltage with a positive gate bias stress, and a negative shift in the threshold voltage with negative gate bias stress [25], [26]. The oxide traps can be reduced in 4H-SiC by doing post oxidation annealing in NO [28].

While oxide traps cause shifts in the device behavior over a longer period of time, the effect of the interface traps are more immediate [29]. Interface traps are carrier traps at the interface of the SiO_2 and SiC material. The presence of a high number of shallow interface traps have been found to be a major cause for the low channel mobility observed in SiC MOSFETs [30]. The threshold voltage is shifted positive by negatively-charged interface states, which means a higher voltage is required to induce the same inversion layer concentration than in a case without traps [31].

2.2.3 SiC Power Devices

Significant improvements have been achieved in developing stable and cost effective methods for SiC device manufacturing over the past two decades. These include establishing standard fabrication and semiconductor growth techniques [32] and optimization of SiC fabrication for special purposes [33]. With the development of reliable fabrication processes, a considerable amount of power devices are now available in the market. These include state of the art Schottky diodes, JFETs, MOSFETs, and BJTs. Some examples of these devices are listed here.

- 1200 V SiC JFET (CoolSiC) from Infineon offers R_{dson} of 70 mΩ, maximum current of 35 A, rated for up to 238 W [34],
- 1200 V SiC MOSFET (Z-FET) from Cree offers R_{dson} of 25 mΩ, maximum current of 60 A [35],
- 1200 V SiC Schottky diodes from Cree and Infineon (thinQ!) [33], [34],
- 1200 V SiC BJT from Fairchild Semiconductor offers R_{dson} of 2.2 mΩ [36].

The availability of these high voltage power devices has caused a significant shift in power electronics system design in recent years. These devices are replacing large silicon devices, using

far less space, reducing cooling requirements and lessening passive component sizes by switching at higher frequencies. The result is a smaller, faster, more efficient and cost effective system [37]. These devices are now being integrated into modules for high temperature and high voltage, ranging from a 300 ℃, 4 kW, 3-phase SiC motor drive module [38], to a 50 kW three-phase SiC power module [39], to a 4 kV silicon carbide solid-state fault current limiter [40]. With further advances on the horizon, SiC is now perfectly poised to completely take over the high power and high temperature power electronics sector.

2.3 SiC Integrated Circuits

As SiC power devices grow in popularity, research has been directed towards SiC integrated circuits. All the challenges faced in the SiC power device fabrication are present in some form or another in SiC ICs as well. The first SiC integrated circuits were mostly reported in the 1990s – an integrated inverter and ring oscillator operating at 625 kHz working from 30 °C to 300 ℃ have been reported [41]. A family of monolithic NMOS digital integrated circuits including NAND, NOR, XNOR gates, D-latches, RS flip-flops, binary counter and half-adders in 6H-SiC have also been reported [42]. In terms of analog and mixed-signal circuits there have been reports on a 6H-SiC JFET-based op amp operating at 600 ℃ [43] and 6H-SiC CMOS op amp at 500 °C [44]. The first integrated gate driver in 6H-SiC was reported in [45] with some of the circuits being tested at over 300 ℃.

The recent SiC circuits have mostly been in 4H-SiC. This may very well be because the power device fabrication has shifted to 4H-SiC as well. The first 4H-SiC integrated circuits were also mainly basic logic gates and single or two-stage differential amplifiers. Some of the circuits reported include a SiC MESFET-based differential amplifier with 63 dB gain and a unity gain bandwidth of 250 kHz operating at 25 ℃ – 365 °C [46], and SiC BJT-based TTL and STTL

inverters at 300 °C [47]. There have also been reports of all NMOS SiC op amps and digital circuits including counters, shift registers, multiplexers and buffers [48]. Along with SiC MOSFETs, integrated circuits in JFETs have also been reported in the form of a sense circuit built from a SiC JFET at 600 °C [49].

As confidence has grown in the SiC IC process, more complex and integrated circuits have been reported in SiC. Most of the recent work has been directed toward creating a fully integrated gate driver to be packaged with the SiC power device in a module [50]. This gate driver was developed to work within integrated power systems for high voltage and high temperature. Along with the gate driver module, an under voltage lock-out circuit in an all-NMOS 2 µm SiC was reported [51]. A linear voltage regulator with 3 A output current operating at 300 °C in the process has also been developed as the first foray into on-chip power management [52].

While a significant amount of advancement has been made in the last few years, the lack of a stable *p*-channel MOSFET, single metal routing layer and absence of reliable on-chip capacitors and resistors have meant that SiC ICs so far have been limited to buffer, protection and simple control circuits.

2.4 Raytheon HiTSiC Process

The circuits and systems presented here have all been designed in the 1.2 µm CMOS SiC process developed by Raytheon Systems Limited, called HiTSiC (High Temperature Silicon Carbide). The key features of the process are given below [53]:

- Operating temperatures greater than 300 °C (the target was set to 400 °C),
- 40 nm electrical oxide thickness,
- Supply voltage of 15 V (a maximum of 20 V),

- Two layers of polysilicon – one of the layers being high sheet resistance poly.

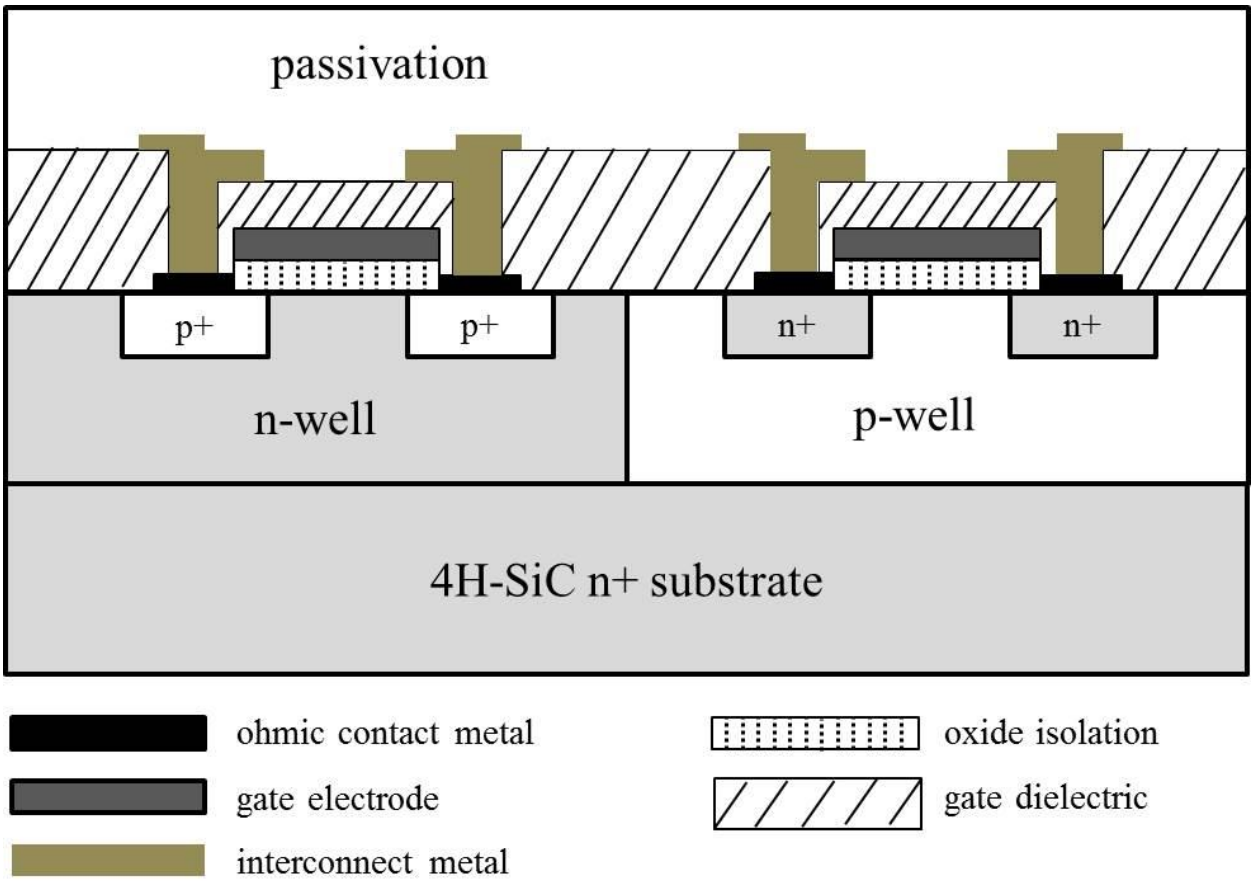


Fig. 2.4 Cross section of the Raytheon 1.2 µm HiTSiC CMOS process.

The chip is built on an *n*+ type substrate. The PFETs are built on the *p*-well with ion implantation. The bodies of all the PFETs are connected to the substrate which also has to be the highest voltage in the chip. A *p*-well is created on top of the *n*-substrate through epitaxial growth after which the *n*+ diffusion is created through ion implantation. The NFETs, thus created, can have separate body connections which allow designers to use body-source connected MOSFETs. This avoids the increase in threshold voltage for FETs which have a body-source bias voltage present during operation.

The NFET and PFET in the HiTSiC process will be described in detail in the following section. Some other components available in the process make this an attractive process for system integration in SiC. These are on-chip capacitors, diodes and resistors. A brief description of these components is given here.

The floating capacitor available in the process has thin dielectric layers and an area capacitance of 0.7 fF/μm^2. The breakdown voltage of the capacitor is 40 V at room temperature, and the leakage current is less than 1 pA for a 7 pF capacitor at 350 °C [53]. The second layer of polysilicon provides for a high sheet resistor which is independent of voltage coefficients. The resistance of the poly resistor has a negative temperature coefficient [53]. The presence of an on-chip resistor and an on-chip capacitor allows for the use of the compensation, resistor ratio voltage dividers and switched-capacitor circuits.

There are also two on-chip diodes – the *n*+ diffusion to *p*-well diode and the *p*+ diffusion to *n*-sub diode. Both the diodes can be employed in a reverse biased condition, thus providing the opportunity for ESD protection in the chip pads. The *n*+ diffusion to *p*-well diode can also be used in regular forward bias mode.

2.5 HiTSiC MOSFETs and Models

The availability of the PFET in the HiTSiC process makes it a very attractive process for integrated circuits for both analog and digital systems. However, the PFETs have been found to be less stable than the NFETs in this process. The PFET threshold voltage is also considerably higher and more variable (6~7 V compared to 2.5~3 V in NFETs) across wafers while the hole mobility ranges from $1/3^{rd}$ to $1/10^{th}$ of the electron mobility in this process. The variability in threshold voltage and carrier mobility, the presence of interface traps, and the significant effect of the body

source voltage bias makes the task of developing representative device models a very challenging task.

2.5.1 BSIM3 FET Models

The first models developed for the FETs were BSIM3 HSpice models. BSIM3 is a model specifically developed for silicon, hence, incorporating all the artifacts of SiC was not possible in a model scalable by either geometry of temperature. Models were thus produced in bins

- Device lengths of 1.2 µm, 1.5 µm, 2 µm, 5 µm and 10 µm (10 µm model was developed only for PFET)
- Operating temperatures of 25 °C, 100 °C, 200 °C and 275 °C.
- Mobility spread of fast, slow and nominal devices.

Along with these considerations designers were encouraged to design with recommended device widths of 4 µm, 8 µm and 20 µm. The devices used for modeling were selected from the process control monitor (PCM) test structures provided by Raytheon Systems Limited. The PCM devices were characterized on the Semiprobe probe station and Cascade probe station with the Keithley meter in the Mixed-Signal Computer-Aided Design (MSCAD) Laboratory at the University of Arkansas. The three most significant short-comings of the BSIM3 models were

- BSIM3 does not allow inputs for SiC parameters like carrier concentration, surface potential at strong inversion etc. Hence, C-V behavior could not be properly modeled.
- BSIM3 models could not capture the phenomenon of interface trapped charge induced Coulomb scattering in weak and moderate inversion region.
- BSIM3 models cannot represent the soft transition from subthreshold to strong inversion region observed in SiC MOSFETs.

These shortcomings of the BSIM3 model led to the development of BSIM4 models for run 2 based on the device characterization data from run 1.

2.5.2 BSIM4 Models

The development of BSIM4 models allowed the incorporation of the main artifacts that could not be modeled in BSIM3. A temperature scalable FET model was still not possible with BSIM4, but the variations were much better modeled. The models were binned in similar fashion, with the only difference being a 300 °C model instead of a 275 °C one and the use of 1.2 µm, 2 µm, 5 µm, 10 µm and 20 µm device length bins. Aging models at 200 °C and 300 °C were also developed.

Some salient points of the device models and their usage were

- The source-body bias effect of the PFETs was modeled more precisely sacrificing subthreshold region behavior. NFETs can be body-source tied, so the source-body bias effect was not modeled as accurately.
- Devices of 1.2 µm length were designated for digital circuits, while 2 µm length devices were to be used for analog circuitry.
- The models are best fitted for devices of specific drive strength per FET finger of 20 µm X 2 µm (5 µA to 15 µA for NFETs and 0.5 µA to 1.5 µA for PFETs).

In summary, the BSIM4 models available for circuit design had good I_d-V_d, I_d-V_g, g_m-V_g, r_o-V_d characteristic predictability. The C-V characteristics were significantly improved from BSIM3. Also, the parasitic body diodes and the diffusion resistance were modeled thoroughly.

2.6 Analog and Digital Circuits in the HiTSiC process

Several analog and digital circuits have been designed and tested in this process by Raytheon. These include NAND, NOR, XOR, AND, OR, INV and DTYPE logic elements as well as an op amp that can drive external loads [54]. The analog circuits were developed with a view to future implementation of auto-zeroing techniques and switched-capacitor circuits.

A large amount of circuits have been tested and reported on from the run 1 design. These include the first SiC phase-locked loop (PLL) operating at 1 MHz and 300 °C [55], some of the first current and voltage references in SiC operating at 300 °C [56], as well as a large family of Boolean and asynchronous logic gates and circuits [56], [57]. Digital circuits with reliability and wafer variability data have also been reported in this process [59].

2.7 Summary

This chapter has provided a background on SiC and its fabrication, as well as the challenges and progresses in the development of power devices and integrated circuits in SiC. The Raytheon HiTSiC process has also been described along with a brief summary of the models available to the designers and a list of circuits already tested and reported in the process. Chapter 3 discusses the background and popular topologies of the circuits developed for mixed-signal control and data acquisition.

CHAPTER 3 CIRCUITS AND SYSTEMS OVERVIEW

This chapter provides an overview of the different circuits that were designed to meet the requirements of the data acquisition and the DC-DC converter system. The circuits and systems described in this chapter are divided into four major categories

- Current-based signal conditioning and processing circuits
- Amplifiers and comparators
- Data converters
- DC-DC flyback converter system

3.1 Signal Conditioning and Processing Circuits

Signal processing and conditioning is the basis of any control system – be it analog or digital. Signal processing and conditioning circuits include, but are not limited to, voltage to current converters, offset-nulling circuits, voltage amplifying circuits, low-noise amplifiers, and filters. Bulk silicon fabrication is now at a stage where complicated and elaborate integrated control systems are being built on tiny chips. These range from video and audio micro-controllers and processors, power converter controllers, and data acquisition and temperature controls, etc. With feature sizes of 14 nm and lower, miniscule chips are being fabricated with billions of transistors in them. In addition to that, the availability of 6-8 metal layers for interconnection makes it possible to build very complex controllers for all sorts of applications.

3.1.1 Analog Signal Processing

Almost all available signal processing and controlling circuits available at present are digital circuits. Digital controllers have the following advantages:

- Digital controllers are more resilient to noise than analog processing,
- The CMOS FETs for digital signal processing can be of minimum feature sizes, thus minimizing the area required,
- Digital circuits are less reliant on bias voltages and currents,
- Digital circuits only have outputs of 1 and 0, unlike analog circuits that have a range of outputs.

Despite these advantages, analog signal processors are in some cases preferable to digital controllers. Some of these reasons include:

- Digital controllers must use data converters to interact with the outside environment, which requires more circuitry and control,
- Digital controllers are synchronous in nature – that means its operation speed is limited by the available clock,
- Digital circuits can sometimes give an erroneous 1 or 0 because of power supply noise. This requires the addition of error correction and data sampling/average circuits,
- Digital signal levels are discrete – limited by the amount of bits. For example, an 8-bit code can only achieve a resolution of $1/256^{th}$ of the full range. Analog circuits, theoretically have infinite resolution.

Over the past few decades though, the IC industry has worked hard to remedy these drawbacks of the digital circuits by increasing data stream bits, clock speeds, and improving error detection and correction algorithms with the introduction of digital filters. There are still some applications where there is opportunity for analog signal processing. Recent research has focused on signal processing in neural networks – the characteristics of sub-micron MOS devices have

been shown to be of use in implementing efficient pattern discriminators [60]. A Matlab-based analysis and CMOS implementation of a Kohonen neural network (KNN) is presented in [61]. The analog signal processing is based on a current-mode approach and uses voltage to current converters, current comparators, current squaring and subtraction circuits to implement a Euclidean distance calculation circuit (EDC) based on [62]. The application of analog VLSI circuits in synaptic matrices is also discussed in [63].

Analog signal processing is more favorable in systems where high precision is not required [64]. A simple model of the MOS transistor along with some basic circuits, including current mirrors, differential pairs and the translinear loops are discussed in [64] to demonstrate the possibility of analog signal processing in different applications. The MOS translinear (MTL) principle is used to develop a configurable analog block (CAB) that can perform various nonlinear functions such as squaring, inversion, rectification, square-root and geometric mean [65]. A programmable and configurable analog signal processing array is developed and its size, power and computational tradeoffs are compared with its digital counterpart [66]. The application of programmable analog processing blocks in low power portable devices for imaging, audio and speech processing is explored in [67]. The results show power efficiency improvement by a factor of 1000 to 10,000 with programmable analog arrays when compared to custom digital circuitry. The analog processing blocks have also been used to form the control block of a CMOS dB-linear variable gain amplifier with 60 dB gain and 2.5 MHz 3-dB bandwidth intended to be applied in direct conversion receivers [68].

Analog integrated circuit design in general has shifted towards a current-mode approach in terms of bias conditions and operating points [68] [69]. The analog signal processing circuits employ the current-mode approach as well. Most circuits and systems employ an initial voltage to

current converter if the incoming signals are voltages and the subsequent processing is done with currents [59]–[61], [64]. It is possible to perform mathematical operations such as summation, subtraction, multiplication, division, squaring and inversion in the voltage domain through the use of op amps, but current-mode processing takes a lot less area and is much more power efficient. Also, unlike the voltage-mode approach its performance is not limited by the specifications of the op amp. It is also critically dependent on the values of the process passives, and without statistical models for the resistors and capacitors depending on their values for proper functionality can be very risky for system operation.

The motivation behind developing an analog signal controller in SiC is not borne out of a need to create portable or low-power devices. Rather, it is necessitated by the lack of routing options in SiC materials today which make complex digital circuitry too large to be fabricated in an IC. At present SiC fabrication processes offer only one layer of metal with a low-resistive polysilicon used as a second routing layer. Designing digital circuits as complex as a simple 8-bit by 8-bit multiplier results in huge routing paths. This means the majority of the IC space is consumed for routing and the parasitic resistance and capacitance due to routing paths are extremely high. While analog signal processing circuits are not as linear as the digital signal processors, they provide more resolution than presently available digital circuits in SiC. The following section discusses some of the basic current-mode signal processing circuits.

3.1.2 Building Block Analog Circuits

A family of building block analog circuits are developed and described in [71]. The circuits designed in this work are based on that report. These circuits include linear voltage to current (V-to-I) converter, squaring, multiplying, inverting, and dividing circuits. The circuits developed in

[71] are based on the square-law characteristics of the MOSFETs in the saturation region of operation. The drain current equation for an NFET operating in the saturation region is given by

$$\boldsymbol{I_{ds} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)\left(V_{gs} - V_{tn}\right)^2} \quad (3.1)$$

where I_{ds} is the drain current, μ_n is the electron mobility, C_{ox} is the gate oxide capacitance, V_{gs} is the gate to source voltage, V_{tn} is the threshold voltage, and W/L is the aspect ratio of the NFET.

Similarly, the drain current equation for a PFET is given as

$$\boldsymbol{I_{sd} = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)\left(V_{sg} - |V_{tp}|\right)^2} \quad (3.2)$$

where I_{sd} is the source to drain current, μ_p is the hole mobility, C_{ox} is the gate oxide capacitance, V_{sg} is the source to gate voltage, V_{tp} is the PFET threshold voltage, W/L denotes the width to length ration of the PFET.

3.1.2.1 Two-transistor Biasing Circuit

The basis of the circuits described in this section is the basic two-transistor configuration that converts a differential input voltage to differential currents as shown in Fig. 3.1.

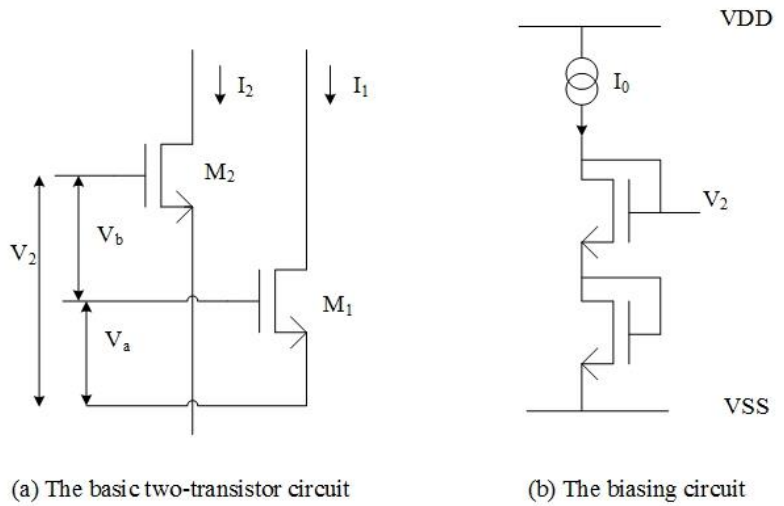


Fig. 3.1 Basic Circuits – (a) the basic two-transistor circuit and (b) the biasing circuit.

It is assumed that M_2 and M_1 have the same *W/L* ratio. Hence, the term $½\mu_n C_{ox}(W/L)$ would be the same for both FETs. If that term is designated as K_n, then the current equations for the two FETs can be rewritten as,

$$\boldsymbol{I_1 = K_n(V_a - V_{tn})^2} \tag{3.3}$$

$$\boldsymbol{I_2 = K_n(V_b - V_{tn})^2} \tag{3.4}$$

From there the following can be deduced (shown in Appendix A),

$$\boldsymbol{I_1 - I_2 = K_n\,(V_2 - V_{tn})(V_a - V_b)} \tag{3.5}$$

$$\boldsymbol{I_1 + I_2 = \frac{1}{2}K_n(V_2 - V_{tn})^2 + \frac{(I_1 - I_2)^2}{2K_n\,(V_2 - V_{tn})^2}} \tag{3.6}$$

3.1.2.2 Linear Voltage to Current Converter and Current Squaring Circuit

This relationship forms the basis of the linear analog current processing circuits. V_2 in this relationship is generated by two diode-connected MOSFET devices that are supplied by a fixed current, as shown in Fig. 3.1. The circuits in Fig. 3.2 show the linear V-to-I converter (a) and the current squaring circuit (b).

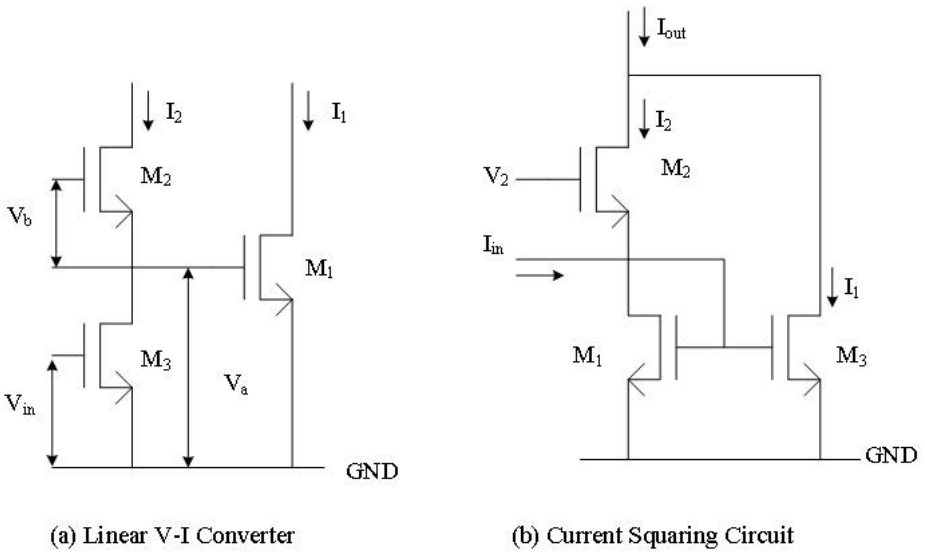


Fig. 3.2 Current converters – (a) Linear V-I (b) Current squaring circuit.

The relationship of the linear V-to-I converter (LVIC) can be derived from Eq. (3.5). If V_a is replaced by V_{in} and V_b can be written as $V_b = V_2 - V_{in}$, Eq (3.5) can be rewritten as,

$$\boldsymbol{I_1 - I_2 = (V_2 - V_{tn})(V_2 - 2V_{in})} \quad \textbf{Or,}$$

$$\boldsymbol{I_2 - I_1 = (2V_{in} - V_2)(V_2 - V_{tn})} \tag{3.7}$$

So the output current is a differential of the two branch currents, and a simple current mirroring circuit can achieve that. The current squaring circuit in Fig. 3.2 (b) uses the principle given in Eq. (3.6). The output current in this case is the total current through the FETs M_1 and M_3. The currents through M_1 and M_3 are the same and the input current is the differential between the two branch currents. The output current replaces the $(I_1+I_2)^2$ term and the (I_1-I_2) term is replaced by the I_{in} term. Hence, the relationship can be rewritten in the following form

$$\boldsymbol{I_{out} = \frac{1}{2} K_n (V_2 - V_{tn})^2 + \frac{Iin^2}{2 K_n (V_2 - V_{tn})^2}} \tag{3.8}$$

3.1.2.3 Analog Multiplier Circuits

The next current processing circuit to consider is the multiplication circuit. The schematic of such a circuit is shown in Fig. 3.3. The multiplication circuit is a combination of two current squaring circuits where the two squared outputs are subtracted from each other to create a product of the two original inputs.

$$\boldsymbol{(I_a + I_b)^2 - (I_a - I_b)^2 = 4 I_a I_b} \tag{3.9}$$

The sum, I_x, and difference, I_y, of the currents are produced through a network of current mirrors. The input currents in Fig. 3.3 are

$$\boldsymbol{I_x = I_a + I_b \quad and \quad I_y = |I_a - I_b|} \tag{3.10}$$

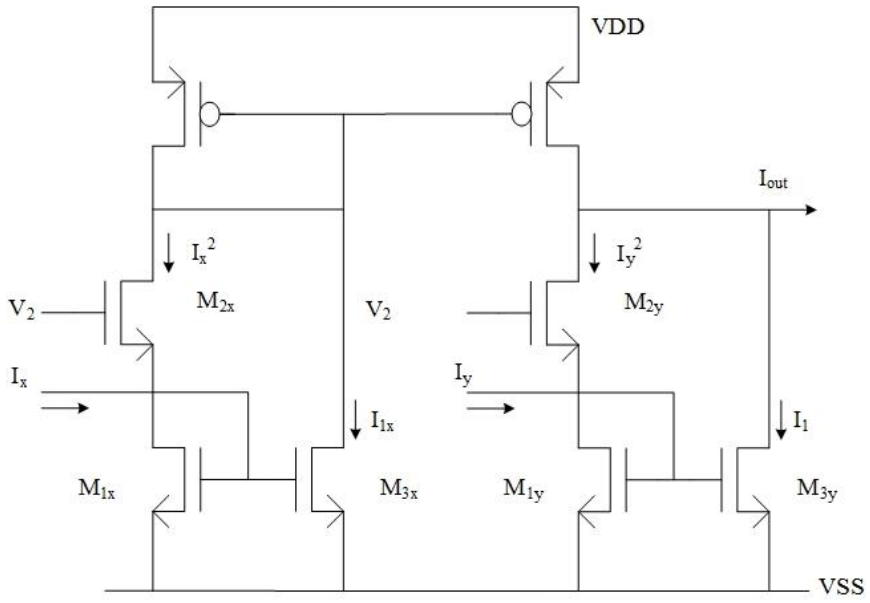


Fig. 3.3 Analog current multiplier.

Fig. 3.4 shows a linear voltage to current converter which can support differential floating inputs [71]. This is realized by cascading the LVIC and the current squaring circuits (Fig. 3.2).

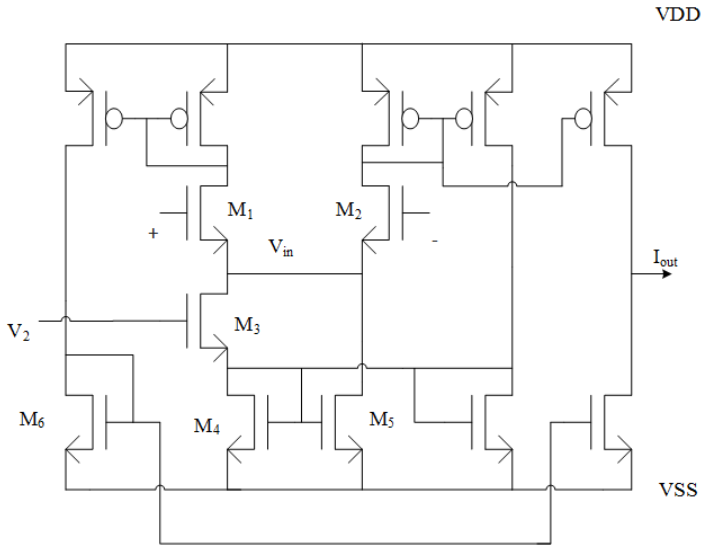


Fig. 3.4 Floating linear voltage to current converter.

Fig. 3.5 shows another floating input linear voltage to current converter that is based on a cross-coupled configuration [72].

Both the floating LVIC circuits provide the advantage of a differential input option for the current converter which often is in the frontend of a system. In many a mixed-signal system, sensor voltage as well as processing and controlling signals are differential in nature. In such cases, these floating input LVICs would be much more applicable.

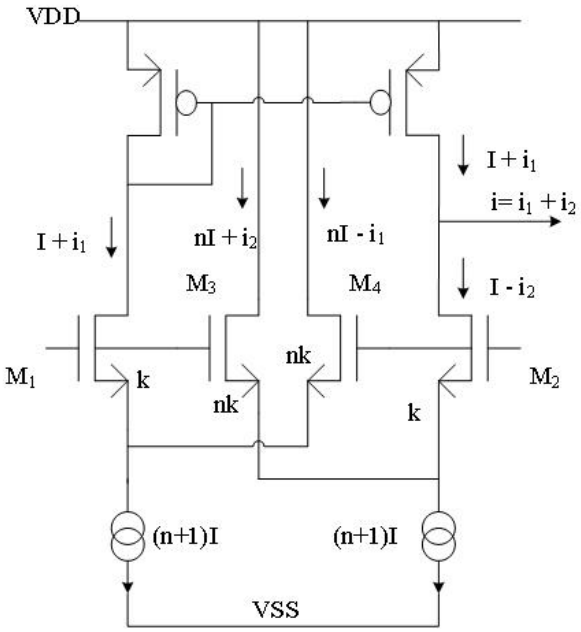


Fig. 3.5 A second floating linear voltage to current converter.

Analog multiplier circuits are pretty common in the form of voltage mixers. Some of these multipliers use the traditional Gilbert cell [73], while others have focused on attributes such as low power [74]. There are also reports of voltage multiplier circuits with a current output such as a four quadrant multiplier in CMOS silicon [74]. That multiplier is based on the two-quadrant multiplier shown in Fig. 3.6. The cross-coupled two-quadrant multiplier is a combination of two of the LVIC circuits seen in Fig. 3.2. The output of the circuit is the difference between the currents on the two legs

$$\boldsymbol{I_{OUT} = I_L - I_R = \ 2K\,(V_2 - 2V_t)\,(V_1 - V_1')} \tag{3.11}$$

where K is the proportional constant deriving from the process parameters and FET aspect ratios, V_t is the NFET threshold voltage, V_2 is the input traditionally denoting the bias voltage for the LVIC circuit and the differential, $V_1 - V_1'$ is the second input voltage.

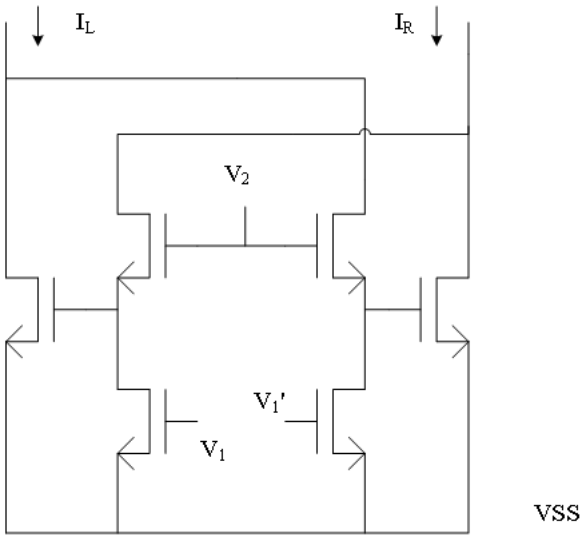


Fig. 3.6 Two quadrant multiplier schematic.

There are other types of analog signal processing circuits – one of them is the current divider [70], [75]. There are also reports of computational circuits based on floating gate MOS transistors [74].

3.2 Amplifier and Comparators

Amplifiers and comparators form the backbone of many mixed-signal circuits. Amplifiers can be found in various forms – operational transconductance amplifiers for g_m-filters and high impedance output closed-loop amplifier networks, buffered op amps for low impedance drive strengths, or switched-capacitor op amps for sigma-delta data converters and switched-capacitor filters. They also vary in complexity, power consumption and performance according to the requirements of the system. General purpose amplifiers are used to level shift, amplify, and limit voltage signals. On the other hand comparators are the decision makers in any control system.

These systems include, but are not limited to, switching, controller and protection circuits. Comparators can be designed to have high or low hysteresis, and smaller or larger time delays based on the requirements of the systems. This section describes some of the most common amplifier and comparator topologies and their operation principles.

3.2.1 Operational Amplifiers

The most common CMOS amplifier is the simple two-stage operational transconductance amplifier with either a PFET input stage or an NFET input stage [69], [76]. The first stage is typically a differential amplifier, while the second stage is a common source amplifier as can be seen in Fig. 3.7.

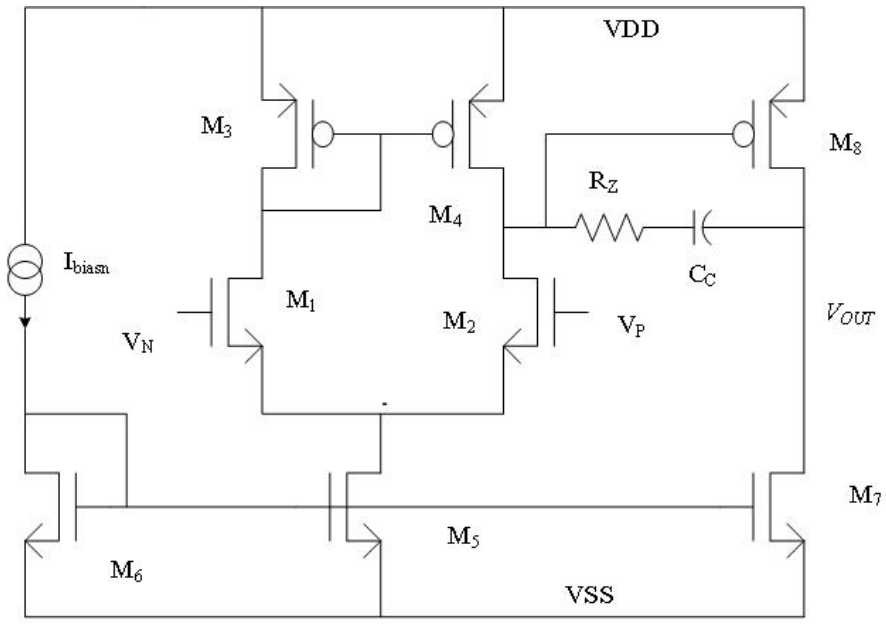


Fig. 3.7 A two-stage operational transconductance amplifier with an NFET input stage.

The FETs M_1-M_4 make up the input differential stage, and the output stage is comprised of the FETs M_7 and M_8. M_5 – M_7 are the current mirrors that help bias the two stages with the external current source, I_{biasn}. The NFETs M_1 and M_2 are the inputs while the PFETs M_3 and M_4 act as the load of the differential stage. M_8 is the amplifying device of the output stage, and M_7 is

the load. The compensation capacitance C_c acts as a Miller capacitance and splits the two poles created in the system into a dominant pole, placed on the output of the first stage and a non-dominant pole, placed on the output of the second stage. This, however, creates a right hand zero which in turn is canceled out by the introduction of the nulling resistor R_z [77].

The above circuit has a high input common mode range due to the threshold voltage of the NFETs in the input differential stage. Rail to rail input common mode stages are possible with the combination of complementary NFET and PFET input stages put together [70]. A traditional general purpose also has a low output impedance, which normally means the addition of a class A or class AB amplifier with a high drive current strength as a third stage. Since for the applications addressed in this work such an op amp was not necessary, this section won't go into the details of such op amps.

3.2.2 Comparators

Comparators are based on the same principles as the amplifiers - both have high gain differential stages – with the biggest difference being the addition of an output buffer stage to facilitate a high/low output and often the presence of a cross-coupled positive feedback decision making stage the helps drive the output to saturation values. The most common comparator is simply a cross couple differential input stage whose output drives a common source amplifier as shown in Fig. 3.8 [78]. The input transistors in this comparator are the NFETs M_1 and M_2. The PFETs M_3, M_4, M_6 and M_7 form the cross-coupled load. The input stage is biased by the external current source I_{bias}. The outputs of the first stage go into a common-source amplifier differential second stage with a single output, V_{out}. The input range of this comparator is typically high due to the NFET inputs. It does not have a buffer stage at the output to facilitate more digital like outputs. A more sophisticated approach to a comparator is shown in Fig. 3.9 and Fig. 3.10.

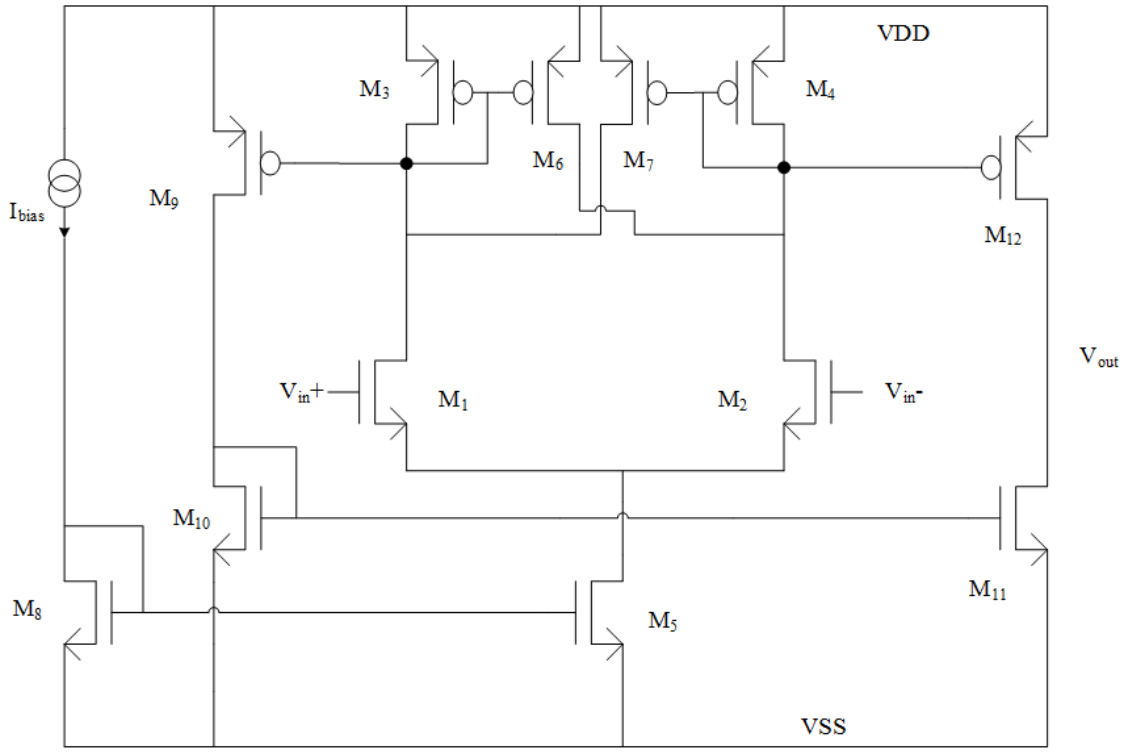


Fig. 3.8 Simple cross-coupled comparator schematic.

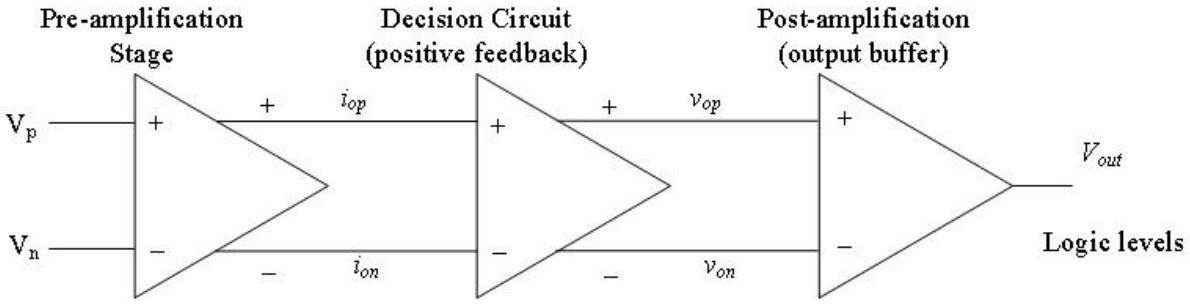


Fig. 3.9. Three stage comparator block diagram.

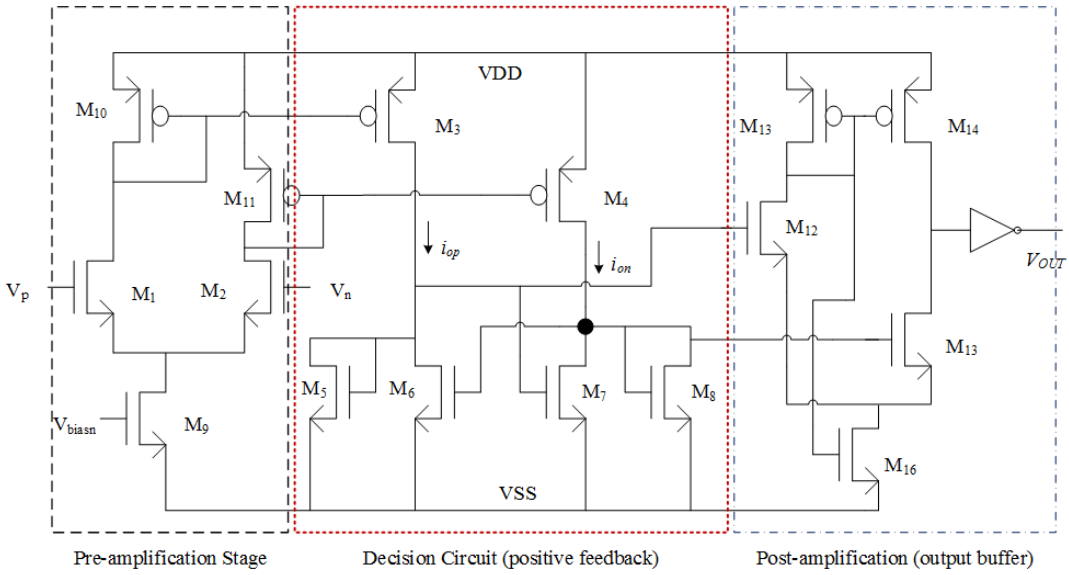


Fig. 3.10 Schematic of a three-stage cross coupled comparator.

The comparator shown in Fig. 3.10 has three stages – a pre-amplification stage to increase the differential level of the input voltages, a cross-coupled decision making circuit such as the one seen in Fig. 3.8, and an output stage that includes a second differential amplifier and an output inverter that provides the digital output [70]. The pre-amplification stage adds more gain to the system, thus decreasing the offset and hysteresis value for the inputs of the comparator. The cross-coupled network is a positive feedback circuit that saturates the output, and the output buffer increases the drive strength of the circuit providing for smaller rise and fall times. The differential input stage is biased by an external bias voltage V_{bias} and this circuit is also limited as a comparatively high common mode input voltage due to the n-type input FETs.

The limitation of the input range can be addressed by the addition of a second PFET input stage and combining the output of the two stages as shown in Fig. 3.11.

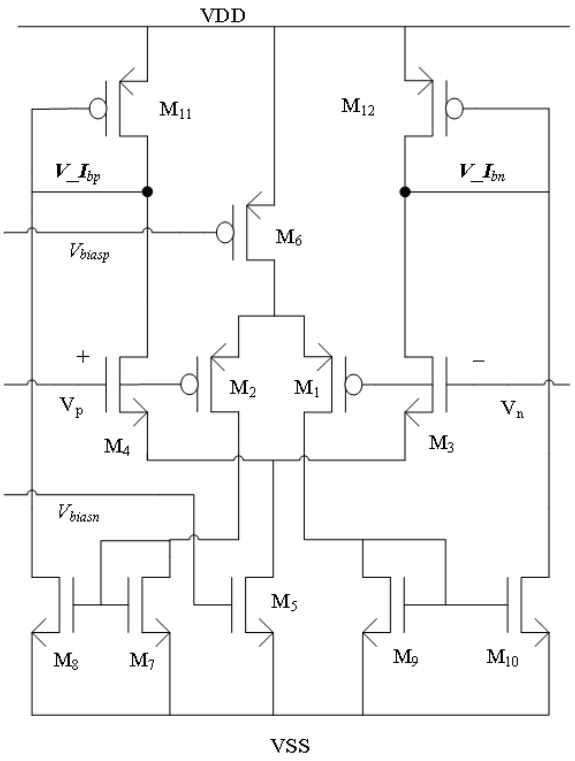


Fig. 3.11 Rail to rail input stage for a voltage comparator.

The two input sets are the NFETs M_1, M_2, and M_5 and the PFETs M_3, M_4, and M_6. The inputs on the PFET stages are converted into current by the NFET current mirrors M_7-M_{10} and supplied to the PFETs M_{11} and M_{12} which are already acting as loads of the NFET input stage. The voltages created on the drain-gate connection of these FETs, V_I_{bp} and V_I_{bn} are now the input to the cross-coupled decision-making stage.

The rail-to-rail input comparator can also be implemented by the using a multiplexer to switch between a PFET and an NFET input stage comparator [79]. And, although a cross-coupled section is found in most comparators, there have been reports of comparators without such a stage [80].

3.3 Data Converters

Data converters are true mixed-signal circuits providing a bridge between the digital and the analog domain. In most real world applications, the sensor and feedback data are gathered through analog circuitry while the control is done by a digital system. And, often digital signals have to be converted to analog voltages or currents to control devices or set conditions. Hence, it is important that the two entities be able to talk to each other. This is accomplished by the use of analog-to-digital converters (ADC) and digital-to-analog converters (DAC). Thus, data converters form a crucial part of a mixed-signal integrated control system. This section touches on the basics of the different types of data converters and describes very briefly the different parameters associated with the data converters and their significance.

3.3.1 Digital-to-Analog Converters

The idea of a digital-to-analog converter is to convert a combination of digital bits to an analog quantity (voltage or current) based on a reference input (voltage or current). For ease of narration, this analog quantity will be referred to as voltage for the rest of the dissertation unless when specifically talking about a current-based data converter. The output voltage of a DAC can be defined as,

$$\boldsymbol{V_{out} = \frac{Dig_{in}}{Dig_{max}} X V_{REF}} \tag{3.12}$$

where the V_{REF} is the reference voltage, Dig_{in} is the digital input and Dig_{max} is the maximum digital code possible. The maximum code is determined by the number of bits available in the data converter, which is also known as the resolution of the data converter. For an n-bit data converter the Dig_{max} is typically $2^n - 1$. Hence, using Eq. (3.12), for a V_{REF} of 5V, a code of 100 in an 8-bit DAC would produce an output voltage of 5 * 100/255 or 1.96 V.

Most digital-to-analog converters are based on some sort of binary weighted passive switching or a ladder network [80] [81]. The passives in this case can be either resistors or capacitors. The binary resistor weighted DAC switches in different values of resistors to control the output of an op amp configured in a closed loop feedback as shown in Fig. 3.12.

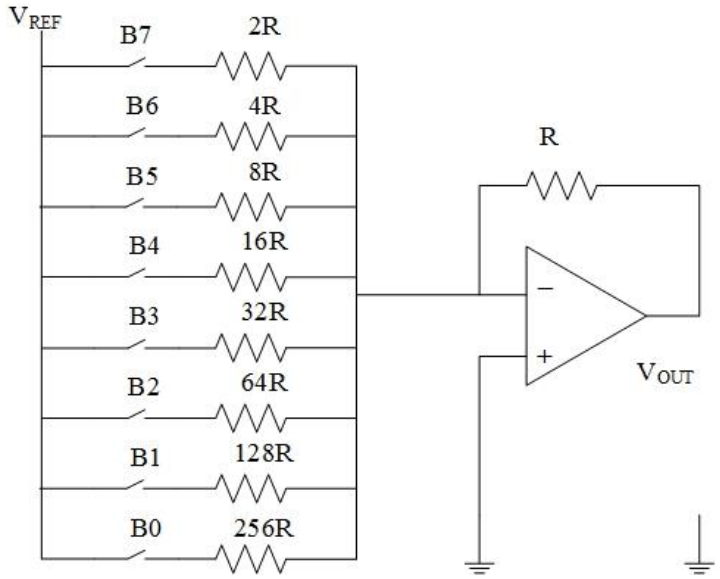


Fig. 3.12 The binary resistor weighted 8-bit DAC.

The converter shown uses the resistors and the switches to determine the ratio of the output to the reference voltage. The output voltage equation for this circuit is given by,

$$\boldsymbol{V_{OUT}} = -\left(\boldsymbol{B7} * \frac{\mathbf{1}}{\mathbf{2}} + \boldsymbol{B6} * \frac{\mathbf{1}}{\mathbf{4}} + \cdots + \cdots + \boldsymbol{B1} * \frac{\mathbf{1}}{\mathbf{128}} + \boldsymbol{B0} * \frac{\mathbf{1}}{\mathbf{256}}\right)\boldsymbol{V_{REF}} \qquad (3.13)$$

where *B0* to *B7* are the bit settings from least significant bit to the most significant bit of the DAC. The same concept is applied for binary weighted capacitor DACs shown in Fig. 3.13 and Fig. 3.14.

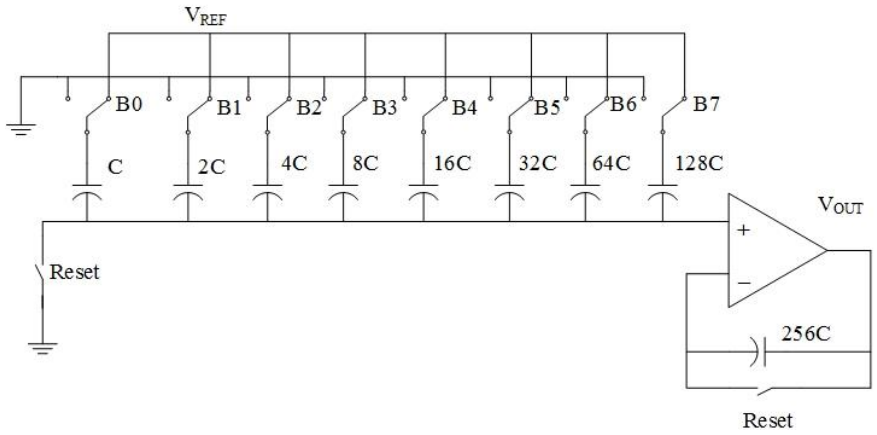


Fig. 3.13. Simple binary weighted capacitor DAC.

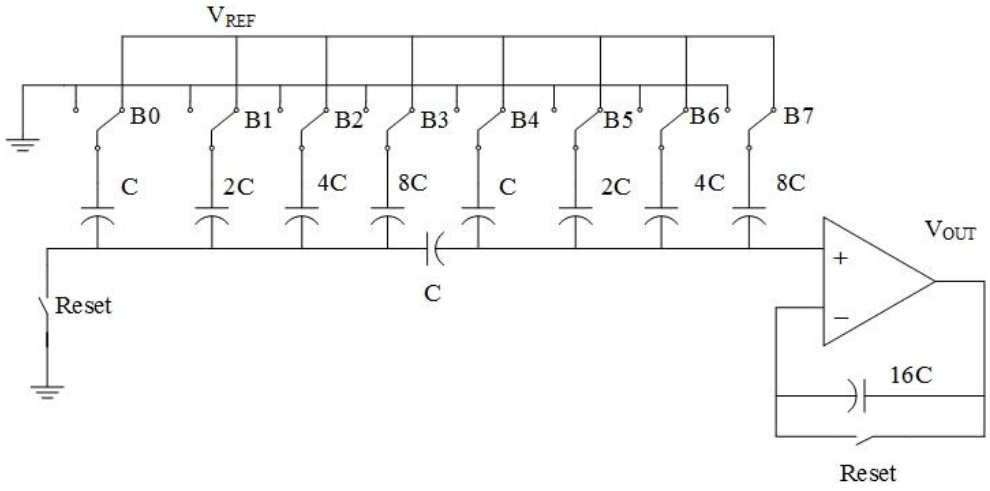


Fig. 3.14. Capacitor-coupled binary weighted capacitor DAC.

The binary weighted capacitor is different from the binary weighted resistor in the sense that impedance of the capacitor is inversely proportional to its capacitance. Hence, the ratio of the capacitors is reversed in order from the least significant bit to the most significant bit. Also, the feedback capacitance on the closed loop op amp is at the highest value, not the lowest as is the case for the resistor DAC. The capacitor DAC also includes reset switches to clear out the output voltage after a conversion. Fig. 3.14 shows a coupled binary weighted capacitor DAC that halves the DAC into two parts and uses the same values of capacitors for both. The desired binary

weighted ratio is achieved by the coupling capacitor between the two halves. This configuration lessens the area of the DAC by using much smaller capacitances. However, the additional coupling capacitance adds some non-linearity to the conversion.

Size of the passives is also an issue in the binary weighted resistor DAC. Hence, a more compact DAC topology, the R-2R ladder DAC, shown in Fig. 3.15, is often used in practical applications.

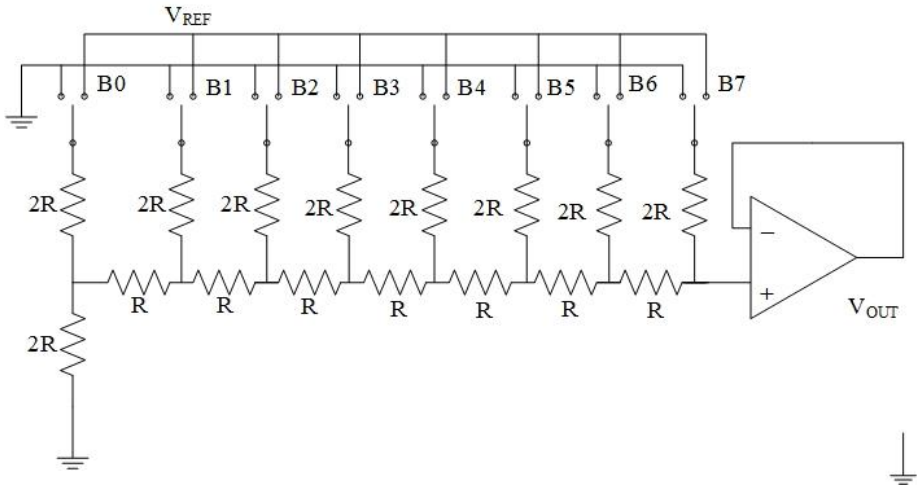


Fig. 3.15 8-bit R-2R ladder DAC.

The R-2R ladder network functions on the principal of the Thévenin equivalent of the voltage and the resistor at each of the bit inputs towards the input to the buffer op amp. To measure the weight of the voltage at each resistor on the eventual output, each bit voltage has to be transformed through the Thévenin's equivalent theorem. For simplicity, a 4-bit DAC is considered to demonstrate the conversion and the weight determination. Fig. 3.16 demonstrates the equivalent determination of the voltage at switch *B0*.

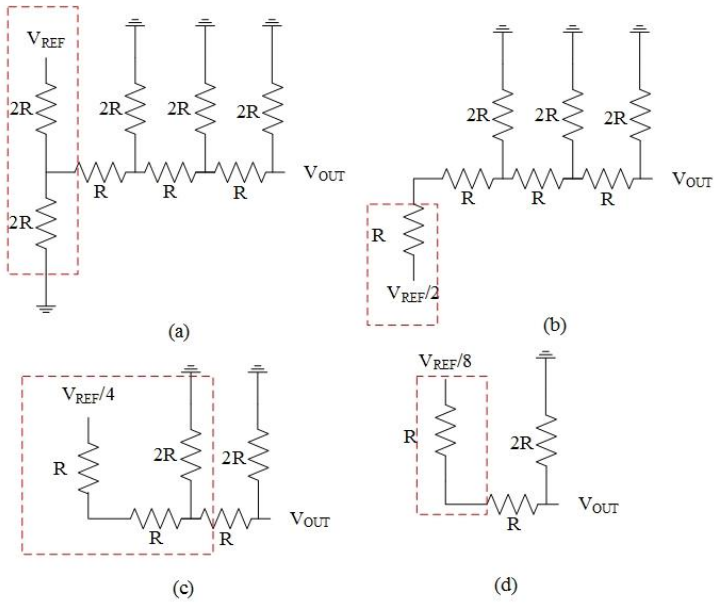


Fig. 3.16. Thévenin equivalent conversion of input at B0 in a 4-bit DAC.

The first step in the transformation is to set all other input voltages to ground. Then using Thévenin's transformation theory, the circuit is simplified from left to right, and the equivalent voltage is halved in every conversion. The last conversion in Fig. 3.16 (d) shows that in this case, V_{OUT} should be $V_{REF}/16$. Thus, the contribution of the input at switch *B0* in a 4-bit DAC to the output is $1/16^{th}$ of the reference voltage. Fig. 3.17 shows a similar transformation for the input at *B2* which comes out to be $1/4^{th}$ of the reference voltage. The R-2R ladder DAC suffers from non-linearity due to the switch resistance and the resistor mismatch.

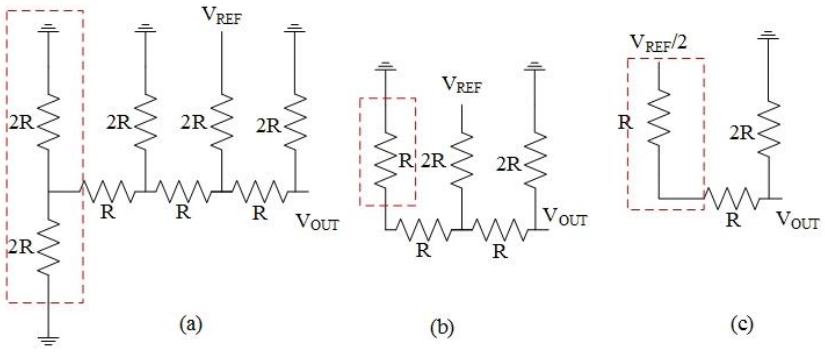


Fig. 3.17. Thévenin conversion of input at B2 in a 4-bit DAC.

Fig. 3.18 shows an 8-bit C-2C ladder DAC. The concept is very similar to the R-2R ladder DAC. Because of the nature of integrated circuits C-2C ladder DACs suffer from the added non-linearity due to the presence of parasitic capacitances on each of the intermediate nodes.

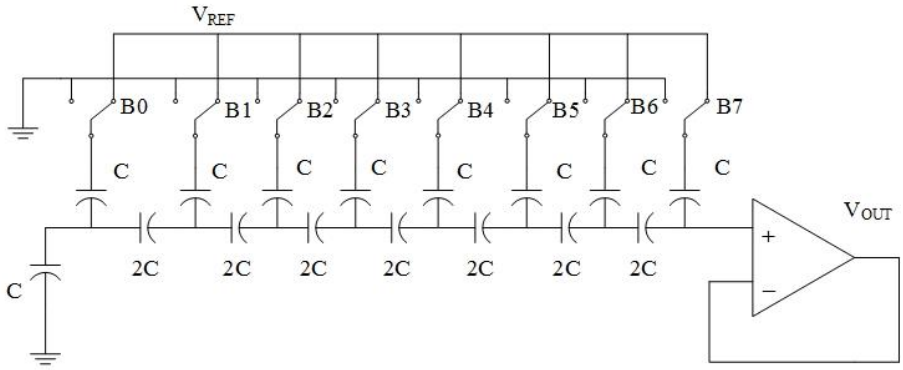


Fig. 3.18. An 8-bit C-2C ladder DAC.

Due to its simplicity and the availability of dependable resistors in the process, the R-2R ladder DAC was selected as the data converter of choice for this work.

3.3.2 Analog-to-Digital Converters

The purpose of the analog-to-digital converter is to convert an analog voltage to a discrete digital signal and represent it with a fixed amount of bits. There are many kinds of ADCs. They differ in size, power consumption, accuracy, noise performance and speed. The four most popular ADCs are the flash ADC, the pipeline ADC, the successive approximation register (SAR) ADC and the sigma-delta (∑-Δ) ADC [80] [81]. These ADCs are briefly described below.

3.3.2.1 Flash ADC

The flash ADC, shown in Fig. 3.19 is the simplest of all the ADCs. It combines a resistor ladder network, comparators, and a digital encoder.

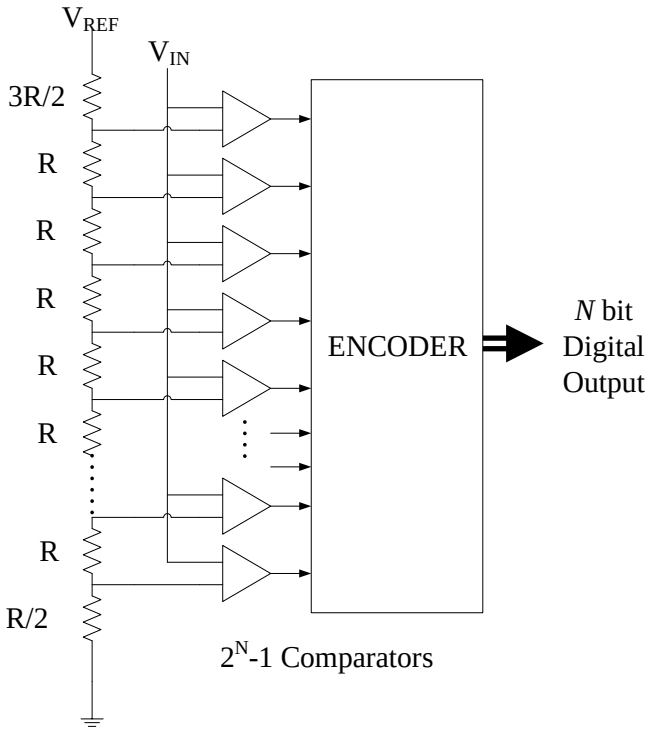
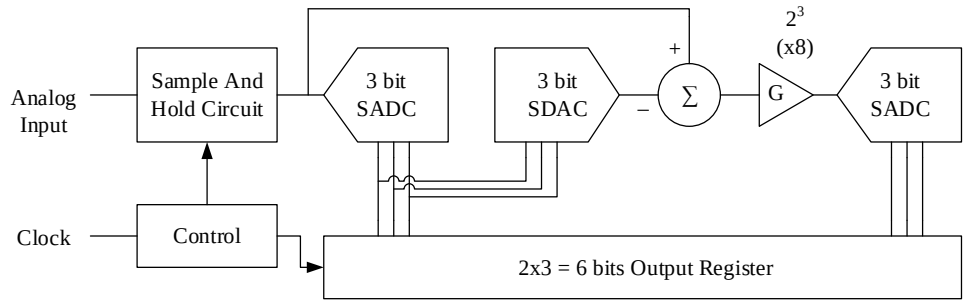


Fig. 3.19. Flash ADC architecture.

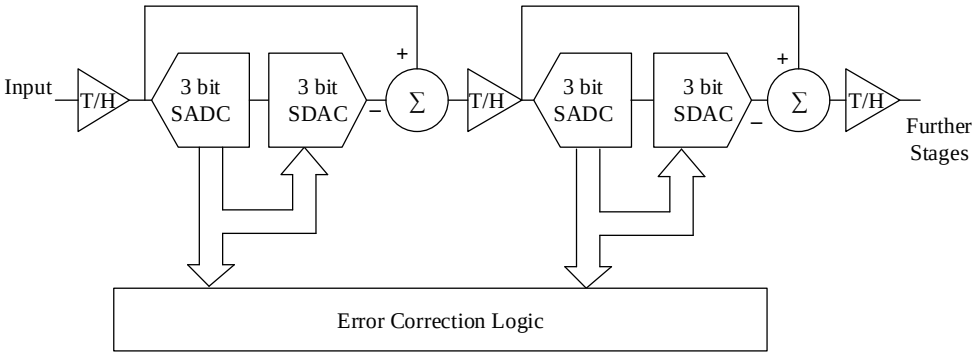
For an n-bit ADC, it divides the full range to $2^n - 1$ levels with a resistor divider. It also uses the same number of comparators to determine exactly where the input voltage fits into the resistor divider network. The comparators below that node will give a high (or low depending on the configuration) output. And the comparators above that node will give the opposite. The outputs are then fed into a 2^n–1-to-n bit encoder. The flash ADC is quick and simple, but it requires a lot of space and power consumption at higher resolutions.

3.3.2.2 Pipeline ADC

The pipeline ADC is designed to combine multiple resolution ADCs to form a larger ADC as shown in Fig. 3.20 [83].



(a) A simple 6 bit Sub-ranging ADC



(b) A simple 6 bit Sub-ranging ADC

Fig. 3.20. Pipeline ADC architectures (a) Simple implementation (b) With error correction.

The pipeline ADC converts the input analog signal a small number of bits at a time. In Fig. 3.20(a), a 6-bit two-stage pipeline ADC is shown. It converts the analog signal into a 3-bit output in its first conversion step. These are going to the MSBs of the digital output. These bits are then converted into an analog value by a 3-bit DAC. This value is subtracted from the original input voltage. This difference is now multiplied by 8 (2^3) to scale the input to the second ADC. Then the second conversion takes place. Thus the lower three bits are obtained. The pipeline ADC shown in Fig. 3.20(b) improves the dynamic response of the circuit by using separate sample and hold circuits for the ADC on each stage.

Pipeline ADCs are particularly useful for combining flash ADCs and reducing space and power consumption though it loses some speed. Whereas an 8-bit flash ADC would require 255 comparators, and a 255 to 8-bit encoder, a pipeline ADC with two flash ADCs would require 30 comparators, two 16 to 4 bit encoders, a 4-bit DAC and some control logic while running only at half the speed. Hence, pipeline ADCs are the choice of ADC for high frequency applications.

3.3.2.3 Successive Approximation Register ADC

The successive approximation register (SAR) ADC is a very popular ADC architecture because of its simplicity and low maintenance. It is also less space and power consuming. The SAR ADC is not the best ADC in terms of either speed or accuracy, but for applications that require mid to high resolution and a few MHz of sampling speed without a very high requirement on accuracy, it is the best available option [82], [83].

The SAR ADC, as shown in Fig. 3.21, typically contains a digital-to-analog converter, a comparator and a digital controller to set the inputs of the DAC. The SAR ADC operates on the principle of a binary search algorithm. Initially, the input to the DAC is set to exactly half. The comparator then decides if input voltage is above or below that point. If the input is higher than the DAC output, the recently changed bit is kept at 1, and the next bit is set to 1. Thus, in one cycle a determination is made on which half the input lies in, and the DAC output is set to the middle value of that half. The comparator then decides if the input is above or below that point. Based on the output of the comparator, the recently changed bit is kept at 1 (if comparator output is high) or set back to 0 (if it is low). Thus, the area of the search is always halved during one clock cycle. For an n-bit ADC, after n cycles, the digital code most accurately representing the input value is determined.

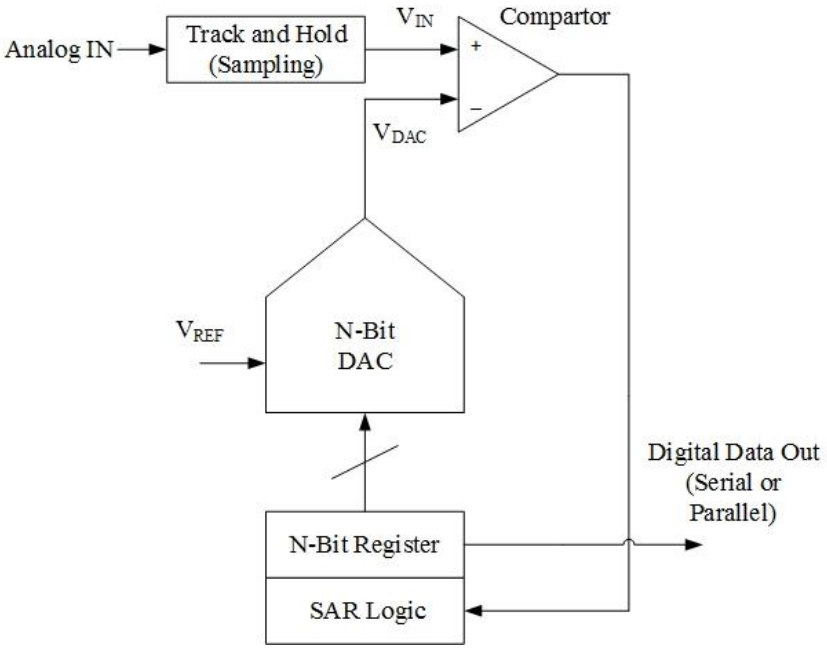


Fig. 3.21. Architecture of an SAR ADC.

3.3.2.4 Sigma-Delta ADC

The sigma-delta ADC, also known as the oversampling ADC, consists of a sigma-delta modulator and a digital decimation filter. The ∑-Δ modulator consists of an integrator and a comparator loop that includes a DAC. The first order ∑-Δ converter, shown in Fig. 3.22, uses a 1-bit ADC and DAC. The output of the integrator has an upward or downward trend based on the output of the DAC and the analog input. For example, if the output of the DAC is high, and the analog input is very low, the input to the integrator would be a high negative value. Thus, the output of the integrator will have a high negative slope, turning the output of the ADC to low quickly. If the analog input is very high the output of the integrator will have a small negative slope, and the output of the ADC will be held at high longer. Thus, the modulator converts the analog input into a series of pulses at different widths. The higher the input is the more the average pulse width of the ADC output will be. This varying pulse width stream of bits is then converted into a digital code by a digital low pass filter or decimation filter.

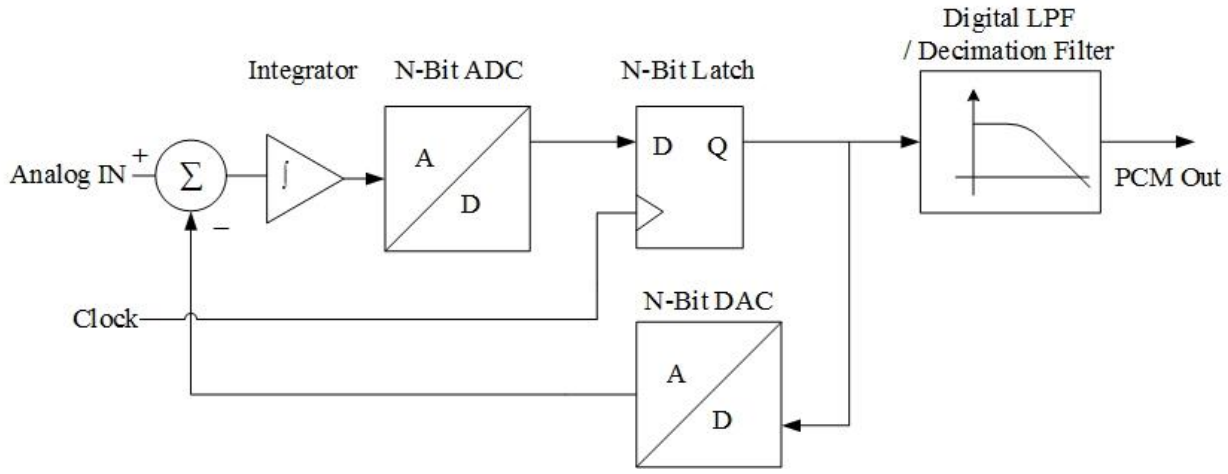


Fig. 3.22. The ∑-Δ ADC architecture.

The ∑-Δ ADC has a very high internal clock sampling frequency and often uses switched-capacitor networks for its integrating network. The oversampling frequency for a first order ∑-Δ ADC can be up to 100 MHz, while the output coming out of the decimation filter will be in the range of kS/s. The high sampling rate pushes the noise to the higher bands and decimation with a very low cutoff frequency eliminates that noise almost completely. Thus, the ∑-Δ ADCs are the data converters of choice when it comes to noise-immune, very accurate systems.

3.3.2.5 Comparison of Data Converters

There are other types of data converters such as time-interleaved data converters [83] and ramp ADCs [85]. The ramp ADC is a hybrid of the SAR ADC and the flash ADC. It compares the output of the DAC with a comparator to determine the nearest digital value to the analog input, however, instead of using a binary search it searches for every combination. Thus, like the flash ADC it is only useful for low resolution.

A brief comparison of the popular ADCs in terms of speed, simplicity, accuracy, noise performance and target application is given in Table 2.1 [83].

Table 3.1. Brief Summary of Typical Analog-to-digital Converters

Type of ADC	Sampling Rate	Accuracy	Resolution	Power Consumed	Typical Applications
Flash ADC	500 MHz and up	Medium	3-6 bits	High	Video, single event acquisition.
Pipeline ADC	5 MHz – 500 MHz	High	Up to 14 bits	Medium	High speed instrumentation, video, software radio
SAR ADC	50 kHz – 5 MHz	High	8-16 bits	Low	Data Acquisition, inexpensive systems
∑-Δ ADC	1 kHz – 100 kHz	Very high	12-18 bits	Low	Industrial measurement, voice-band audio

The typical data converter application targeted in this work was data acquisition at a fairly moderate sampling rate of 50-100 kHz. This led to the choice of designing the SAR analog-to-digital converter in the process.

3.3.3 Data Converter Performance Parameters

The performance of the data converters is measured by several performance parameters. These parameters can be static performance parameters such as accuracy, resolution and linearity or dynamic parameters such as settling time and overshoots during transition. With the target sampling frequency of 100 kHz in mind and the specified clock frequency at 1 MHz, the dynamic parameters are less significant than the static performance parameters. In this section the definition and significance of some of the key static parameters are given [80], [85].

- Full Scale Range (FSR) – The difference between the maximum voltage output and the minimum voltage output, typically zero or negative supply. The full scale range signifies the scope of the output, and input level that can be supported by the converter.
- Resolution – The total number of digital bits available for conversion. The more bits the converter has, the more precise the output will be.

- Least Significant Bit (LSB) – The corresponding value in voltage of a single code. It can also be defined as the analog voltage differential when the digital code changes by a one bit. The LSB is also an indicator of precision. The higher the LSB value is, the coarser the converter measurement will be.
- Differential Non-Linearity (DNL) – Ideally the difference between analog outputs (for a DAC) or inputs (for an ADC) when the digital code changes by 1, should be equal to 1 LSB value. That is very rarely the case. This discrepancy between the ideal value of 1 LSB, and the actual difference between two consecutive analog values is termed as the differential non-linearity. The DNL is the measurement of the code to code variation accuracy.
- Integral Non-Linearity (INL) – The INL is another expression of non-linearity. This refers to the discrepancy between the analog value for a certain digital code and the ideal (or in some cases expected) analog output for that code. The INL signifies the absolute error at a certain point of the conversion cycle. The INL and DNL errors are shown in Fig. 3.23(a).
- Offset and Gain Errors – Often the INL characteristic is measured against a 'best-fit' curve that follows the trend line of the output rather than the ideal transfer curve. The best fit curve follows the ideal curve closely in shape, but almost always with an offset that puts the line either above or below the ideal curve consistently. In such a case, the steady difference between the two lines is called the offset error.

  The best fit line may not possess a transfer characteristic similar to the ideal curve. For example, instead of a change of 1 LSB value for every one bit change, the actual data

converter may show a consistent 0.98 LSB change for each change. Such an error is called a gain error. The gain and offset errors are shown in Fig. 3.23 (b)

The INL, DNL, offset and gain errors are all represented in terms of LSB.

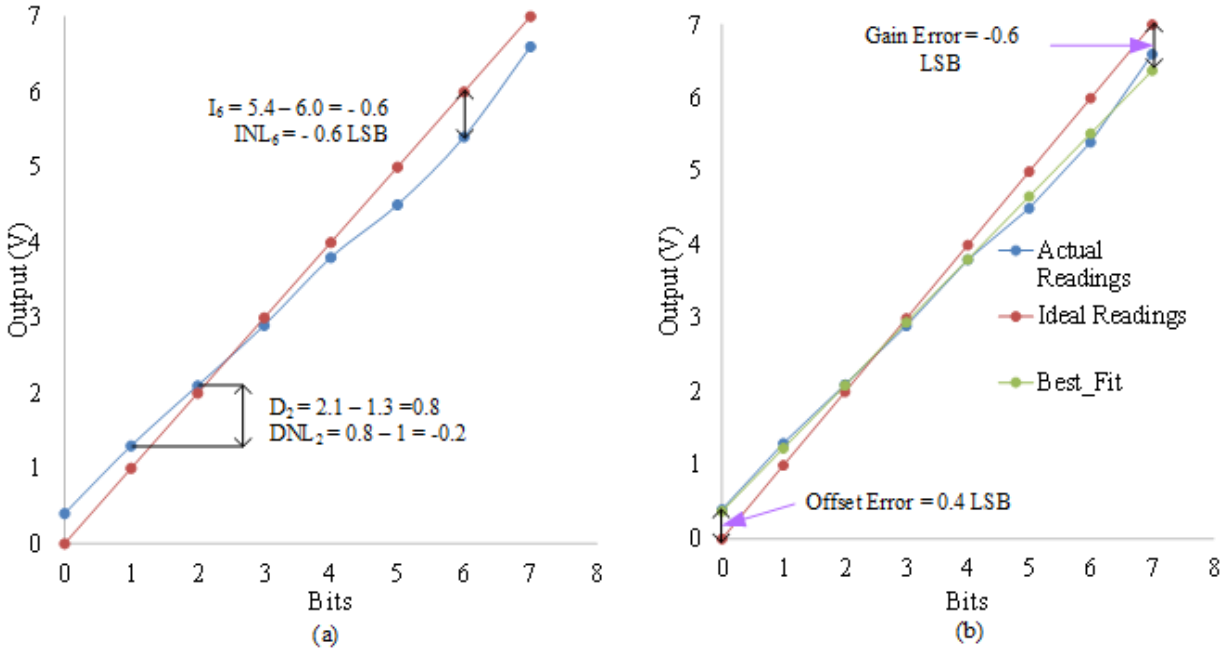


Fig. 3.23 Data converter (DAC) (a) INL and DNL, and (b) Offset and gain errors.

Quantization Error – The quantization error is a term applied only to an ADC. It refers to the difference between the input value and the equivalent of the digital output value. It also is mostly represented in terms of LSB.

The interested reader is encouraged to consult data converter books and application notes to do further reading on the performance parameters of the data converters and how to measure them [80]-[82].

3.4 DC-DC Converter for a Solar Microinverter

The application that was chosen as the target application for the mixed-signal controller developed in this work was the DC-DC flyback converter. The DC-DC flyback converter is a

popular isolated DC-DC converter. It is used for medium to high output voltage levels, 100 V and upwards [87]. The flyback converter was developed by the power electronics lab at the University of Arkansas to operate as the first step of a solar microinverter [88]. The flyback converter was chosen not only for its isolation but also for its typical power rating, which is around 100-200 W, thus making it suitable for a 60 cell PV panel. Larger PV panels with more power output would require a different DC-DC converter topology.

3.4.1 Solar Microinverter Architecture

The solar microinverter is designed to take a DC voltage from the solar panel and turn it into an AC output to be supplied to either the load or fed back into the grid. The term 'microinverter' refers to the comparatively lower power ratings of the inverters required for single solar panels. There are different topologies available for solar microinverters. A review of some of the common topologies can be found in [89]. The general architecture of the solar microinverter involves two power converters – a step-up DC to DC converter that takes the input from the solar panel and transforms it to a higher and stable DC voltage, and a DC to AC inverter that transforms the intermediate DC voltage into a 60 Hz AC signal [90]. A very general diagram of the solar inverter system is shown in Fig. 3.22. While Fig. 3.22 (a) shows the system in generic terms, Fig. 3.24 (b) notes the voltages at the PV panel and the intermediate DC level, as well as the AC output voltage levels for the case of a solar microinverter.

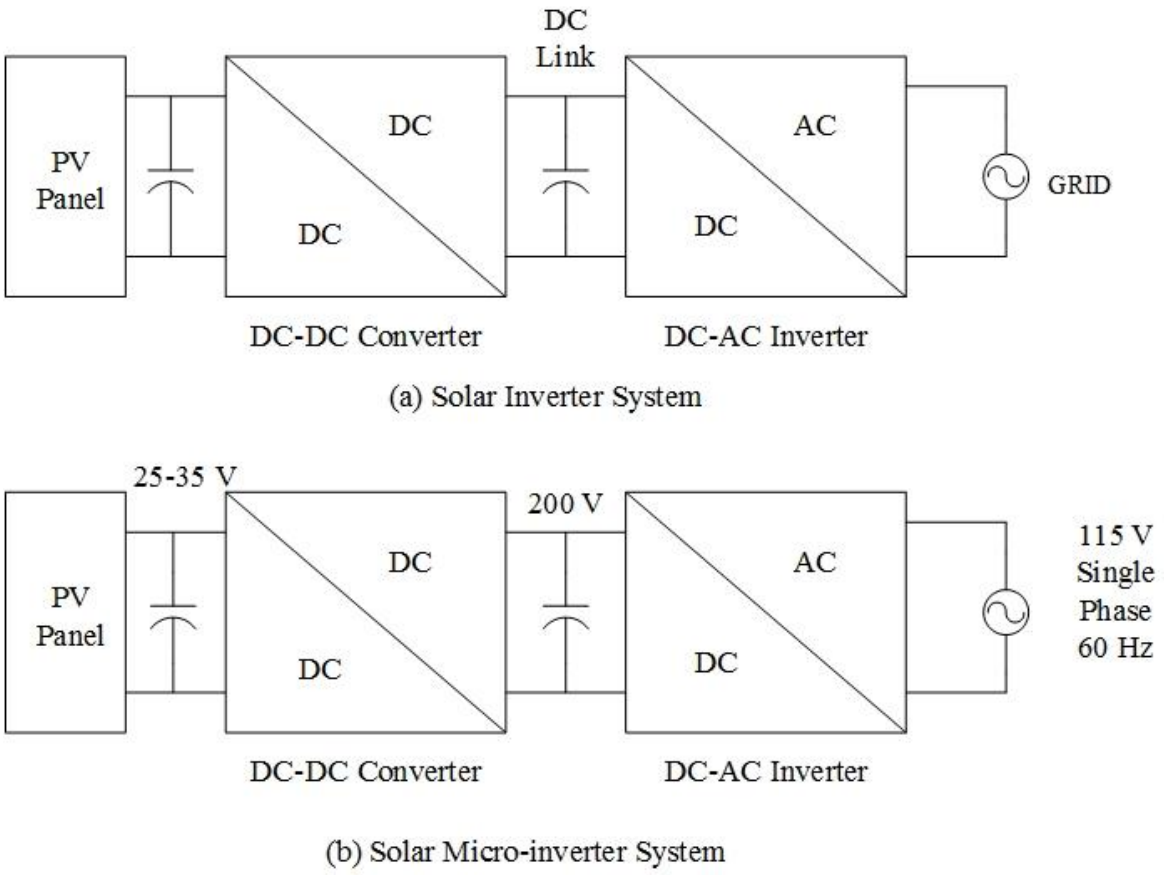


Fig. 3.24 Solar inverter system architecture

The DC-DC converter for the microinverter is chosen to be an isolated converter [91]. Based on its power rating and inherent isolation capability, the flyback converter is a very good candidate for the DC-DC converter in a microinverter system. The interleaved flyback converter offers more power efficiency, better energy transfer and less ripple for microinverter applications [92]. However, since both the control scheme and the integrated controller chip were novel in the context of the DC-DC converter, the simpler topology was selected.

3.4.2 The DC-DC Flyback Converter

Like all switching converters the flyback uses an inductive element to store energy and then supply it to the load. In the case of the flyback converter, this inductive element is a pulse transformer. The general architecture of the flyback DC-DC converter is shown Fig. 3.25.

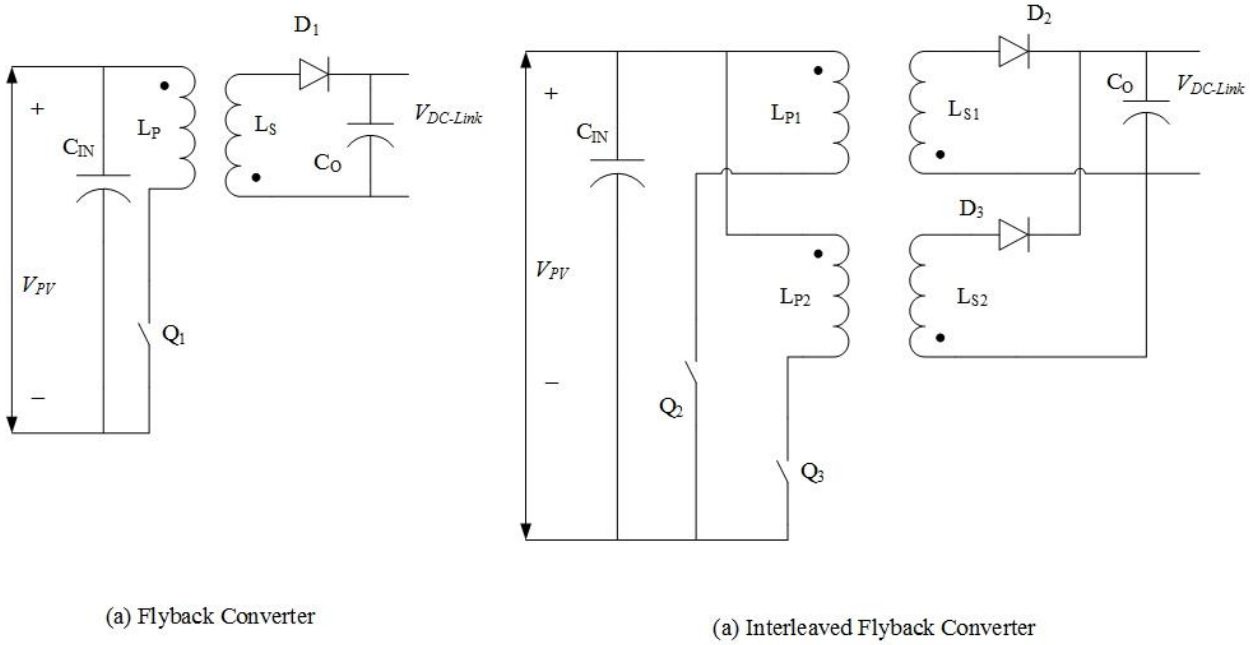


Fig. 3.25 Flyback DC-DC converter architectures (a) Basic flyback (b) Interleaved flyback.

The basic flyback converter is shown in Fig. 3.25 (a). When the switch Q_1 is turned on, the current through the primary side of the transformer, L_P is ramped up and the energy is stored in the coil. During this cycle the voltage on the secondary is reversed to that of the primary and the diode on the secondary, D_1 is turned off. Therefore, no current flows on the secondary side. The load is supplied by the output capacitor, C_O. When the switch Q1 opens, then the inductor Lp sees a negative voltage snap due to V = Ldi/dt as the current drops from its original value to zero. This negative voltage is transferred to the secondary and forward biases the diode allowing current to flow in the secondary and charge the capacitor. Thus, the energy put into the pulse transformer

when Q1 was closed is transferred to the secondary when Q1 is opened. Normally, when the output capacitor voltage goes over a certain value or the secondary current reaches 0, the switch is turned back on and the transformer is charged again. During that sequence the output starts to drop. Thus, the flyback works on two cycles – primary conduction mode when the output capacitor discharges, and the secondary conduction mode when the output capacitor is charged.

The interleaved flyback converter consists of two flyback transformers in parallel and uses two switches, Q_1 and Q_2 to control the transformers. The switches operate complementary to each other, hence, they are never on at the same time. The principle of the converters is the same – store energy in the transformer when the switch is on and supply energy to the load when the switch is off. Only this time, one of the secondary diodes is always conducting. Hence, the output capacitor is always being charged. The charging only stops when the output goes over the rated value. This configuration ensures that energy is stored and transferred on both cycles, thus potentially doubling the energy that can be supplied by the converter [93]. Furthermore, since the output capacitor sees a more frequent charging current, the ripple of the output voltage waveform is considerably lower than in the case of the simple flyback. However, the control of this topology is considerably trickier than the simple flyback converter and, as a first application of the mixed-signal controller, was passed over in favor of the flyback converter.

The solar microinverter system with a PV panel and a flyback converter is shown in Fig. 3.26. The solar panel, given its small size, can be placed on a roof top. The voltage is then sent to the DC-DC converter, which converts it into a stable voltage on the DC link. Fig. 3.26 also includes a controller that takes in sensor outputs for system voltages and currents, as well as a gate driver that takes the output of the controller to drive the power FET.

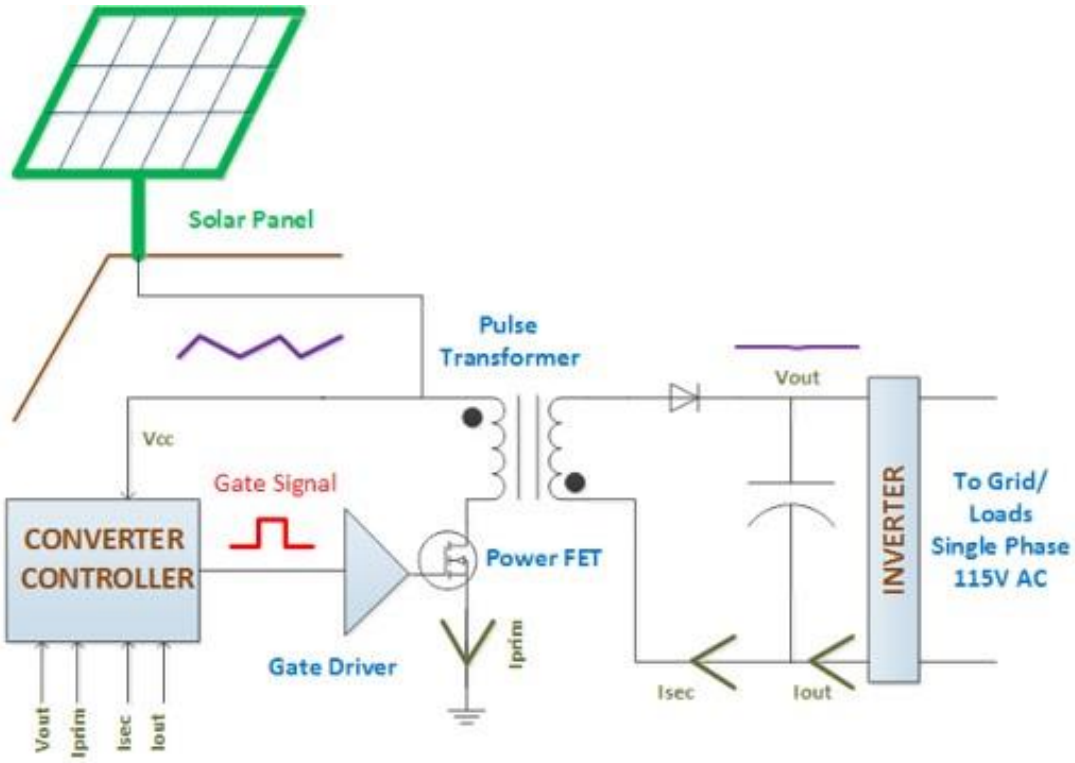


Fig. 3.26 Solar inverter system with PV panel, DC-DC flyback converter and DC-AC inverter.

The typical DC-AC inverter used in a microinverter system is an H-bridge inverter as seen in Fig. 3.27.

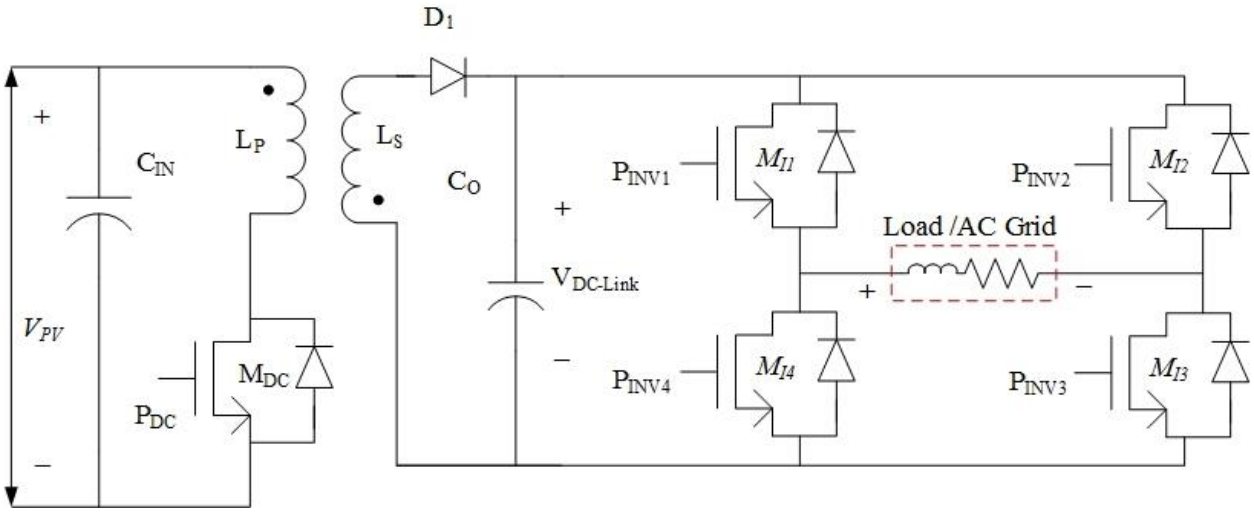


Fig. 3.27 Microinverter with the H-bridge DC-AC inverter.

3.4.3 Sliding Mode Control

There are several control techniques that can be used for the proposed flyback DC-DC converter. The sliding mode control (SMC) is particularly efficient for non-linear systems which have two distinct states of operations, often referred to as variable structure systems (VSS) [94]. The SMC technique is a discontinuous system that controls the system so that it can slide along its natural operation plane or surface. The first step to a sliding mode control is to characterize the natural behavior of the system with differential equations. The controller then treats each state differently which results in a continuous time domain behavior for the system outputs. This makes sliding mode control a very good option for switch mode power supplies (SMPS) [94]–[96].

Recent years have seen the introduction of the sliding mode control to flyback converters as well. Whereas the typical sliding mode controller uses one entity – the output voltage error or the output current error – to control the system, flyback converters have been reported to be controlled by an SMC that takes the output voltage error and the transformer current both into account [98].

One common trait of the sliding mode controllers in flyback converters is the discontinuous mode of operation. In switching converters the inductor current ramps up to a peak value and then starts ramping down. In continuous mode, the current never reaches zero and is always between the maximum and minimum values. In the discontinuous mode, the current reaches zero, and stays there for a while before ramping up. In the boundary conduction mode, the current starts to ramp up as soon as it reaches zero. The nature of the continuous mode may lead to oscillation in the system output for duty cycles of over 50% and is often less favorable than the discontinuous mode in switching converters [87]. However, the discontinuous mode has more ripple in the output. This has led to the application of the boundary conduction mode which has less ripple and is not prone

to system oscillation like the continuous mode. Sliding mode controllers, designed to keep the system on the natural switching surface (NSS) have been reported to adopt boundary control to improve performance of switching converters [97–99].

3.4.4 Governing Equations for the Flyback DC-DC Converter

The sliding mode controller implemented by the power electronics lab to realize the flyback DC-DC converter is a boundary conduction mode natural switching surface controller [88]. The controller expands on the existing flyback sliding mode control and introduces three more entities other than the typical control entity output voltage to ensure boundary mode conduction. These are the output current, the magnetizing current and the input DC voltage. A detailed explanation of the control scheme can be found in [88]. A very brief summary of the control scheme is given here.

A total of four system variables are to be measured – the DC input voltage from the PV panel (V_{CC}), the magnetizing current of the transformer (I_m), the output voltage (V_o) and the output current (I_o). In order to devise a control scheme, normalized values of these entities are used. The voltages are normalized based on the secondary equivalent of the voltage. The rated output voltage is 200 V. The converter uses a 6:1 turns ratio pulse transformer, hence, any voltage on the primary side is equivalent to six times that on the output side.

$$\boldsymbol{v_{on}} = \frac{\boldsymbol{V_o}}{\boldsymbol{V_{o-rated}}} \tag{3.14}$$

$$\boldsymbol{v_{ccn}} = \frac{\boldsymbol{V_{CC}} * \boldsymbol{N_S}/\boldsymbol{N_P}}{\boldsymbol{V_{o-rated}}} \tag{3.15}$$

The normalized currents of the systems are defined in terms of the characteristic impedance, Z_r and the rated output voltage, $V_{o\text{-}rated}$ or V_r. The two normalized currents are given by the equations,

$$\boldsymbol{i_{mn} = I_m * \frac{Z_r}{V_r}} \tag{3.16}$$

$$\boldsymbol{i_{on} = I_o * \frac{Z_r}{V_r}} \tag{3.17}$$

where the magnetizing current, I_m is presented in reference to the secondary side. The characteristic impedance is calculated based on the inductance of the transformer, L_m and the output capacitance, C_o, and the transformer turns ratio, N_S/N_P, and is given as

$$\boldsymbol{Z_r = \frac{N_S}{N_P} * \sqrt{\frac{L_m}{C_o}}} \tag{3.18}$$

The DC-DC flyback converter has two distinct operating conditions – the on-state and the off-state conditions. The system behavior is different during these two conditions. The natural switching surface of the flyback converter is then divided into two portions – the off-state trajectory and the on-state trajectory. A new pair of equations were developed in [88] to represent these two trajectories, as shown below

$$\boldsymbol{\lambda_{off} = v_{on}^2 + \ (i_{mn} - i_{on})^2 - 1 \ - i_{on}^2} \tag{3.19}$$

$$\boldsymbol{\lambda_{on} = i_{mn} + \frac{v_{ccn}}{i_{on}} \ v_{on} - \frac{v_{ccn}}{i_{on}}} \tag{3.20}$$

These two equations are the governing equations for turning the power FET on and off.

The controller turns the FET on or off depending on the value calculated for λ_{off} and λ_{on}, and the value of the output voltage. The conditions of switching the FET are the following,

- When $V_o < V_{o\text{-}rated}$, if $\lambda_{off} < 0$, turn FET on, else turn FET off.
- When $V_o > V_{o\text{-}rated}$, if $\lambda_{on} < 0$, turn FET on, else turn FET off.

The equations all use normalized values for the measured entities. During the implementation of these entities for analog signal processing, the values will change to voltage or current where the rated normalized values are not going to be 1 V or 1 A. If the entities were all

represented by current, including a normalized value for 1, a discrepancy between the dimensions of the entities can be found in both Eqs. (3.19) and (3.20). By replacing 1 with 1^2 in the λ_{off} equation and adding the extra 1 with v_{ccn} in the λ_{on} equation, the dimensions can be corrected. Furthermore, since the values of λ_{off} and λ_{on} are compared to zero, a comparison between the positive and negative elements in the equations can determine the switching FET condition. So, the conditions can be rewritten as,

- When $V_o < V_{o\text{-}rated}$, if $v_{on}^2 + (i_{mn} - i_{on})^2 < 1_n^2 + i_{on}^2$, turn FET on, else turn FET off.
- When $V_o > V_{o\text{-}rated}$, if $i_{mn} * i_{on} + v_{ccn} * v_{on} < v_{ccn} * 1_n$, turn FET on, else turn FET off.

The traditional solution to this scheme is to use a digital controller [88]. However, due to the lack of a second routing metal that makes complex digital circuits area-heavy and prone to parasitics, an analog controller was chosen over the digital controller. The current-mode controller uses the following steps to control the converter

- Convert sensor voltages into current
- Normalize the currents to meet the system specifications
- Use analog circuits to do mathematical operations such as square and multiplication.
- Use two comparators and a control algorithm to FET drive signal to the gate driver.

3.5 Summary

A background of the current-mode analog signal processing circuits was described in this chapter. Analog signal processors offer faster response, and smaller area, and are ideal for low cost applications. However, the decision to use these circuits for control in SiC was mainly driven by the unavailability of complex digital systems in SiC at this moment. After that, a brief discussion on the amplifiers and comparators used for signal processing was presented. A description of the

popular data converter topologies was given next, along with the explanation of some of the key performance parameters and how they led to the design choice made for this research.

Finally, an overview of the flyback DC-DC converter being used in the solar microinverter was presented. The control scheme chosen by the power electronics lab, the natural switching surface control method, was briefly discussed in light of the analog mode control. The system specifications, design procedure and simulation results of these circuits and systems are described in Chapter 4.

CHAPTER 4 DESIGN AND SIMULATION

This chapter discusses the design and simulation results of the circuits and systems developed as part of the work. The chapter is divided into five sections – a brief overview of device parameters, the current conditioning circuits, the amplifier and comparators, the data converters, and the DC-DC converter controller circuits. The four different sections describe the specification, design procedure and the simulation results of each of the circuits.

4.1 Device Parameters and General Guidelines for Circuit Design

The first step in designing a circuit is to set a value for the PFET and NFET. During the design phase, the typical-typical (TT) model type was chosen to be the nominal device type. Hence, the circuits were designed with TT characteristics. The TT model refers to typical NFET and typical PFET devices. Since the wafer shows a spread of device characteristic, the typical devices were chosen to be near the middle of the spread. The design equations were based on the Shichman-Hodges equations for a MOSFET [102]. The necessary threshold voltage and mobility parameters were determined as such

- NFET threshold voltage, Vtn = 2.5 V
- PFET threshold voltage, |Vtp| = 6.5 V
- NFET mobility factor, $kn' = 5.0\ \mu A/V^2$
- PFET mobility factor, $kp' = 0.8\ \mu A/V^2$
- Short channel effect factor, $\lambda = 0.05$

As mentioned in Chapter 2, the models used to design the circuits were binned in terms of device sizes and operating temperature. In order to get the most accurate results from the simulation, the following general guidelines were followed during the design process.

- The nominal device size for most circuit operation was the 20 µm/2 µm device for analog circuits and the 1.2 µm length devices for digital circuits. In cases where smaller device aspect ratios were necessary, smaller devices were used.
- The target nominal current range for a typical 20 µm/2 µm NFET device was 2 - 20 µA, while the target nominal current for a typical 20 µm/2 µm PFET device was 0.5 - 5 µA.
- Where possible, cascode current mirrors were used for NFET current mirrors. Due to the high threshold voltage of the PFETs simple current mirrors were used in the case of PFETs.
- As already mentioned, the design was performed based on the parameters of the TT models at 25 °C. They were then checked over temperature for all the other available models (TF, ST, SF).

4.2 Current Conditioning Circuits

There are three major current conditioning circuits – the linear voltage to current converter, the current squaring circuit and the current multiplier circuit [71]. The basic voltage biasing circuit is common to all three circuits. The design and simulation of all three circuits are described in this section. The key performance metric of the circuits, the conversion gain is defined as:

- I_{out}/V_{in} (µA/V) for the linear V-to-I converter circuit, and,
- I_{out}/I_{in}^2 and I_{out}/I_a*I_b ($\mu A/\mu A^2$) for the multiplying and squaring circuits.

4.2.1 Linear Voltage to Current Converter

The schematics of the linear current converter and the current squarer have already been shown in Fig. 3.2, but for convenience they are given in Fig. 4.1 as well. The output of the current

converter is taken as $I_2 - I_1$. The two governing equations, as already mentioned in Eqs. (3.7) and (3.8)

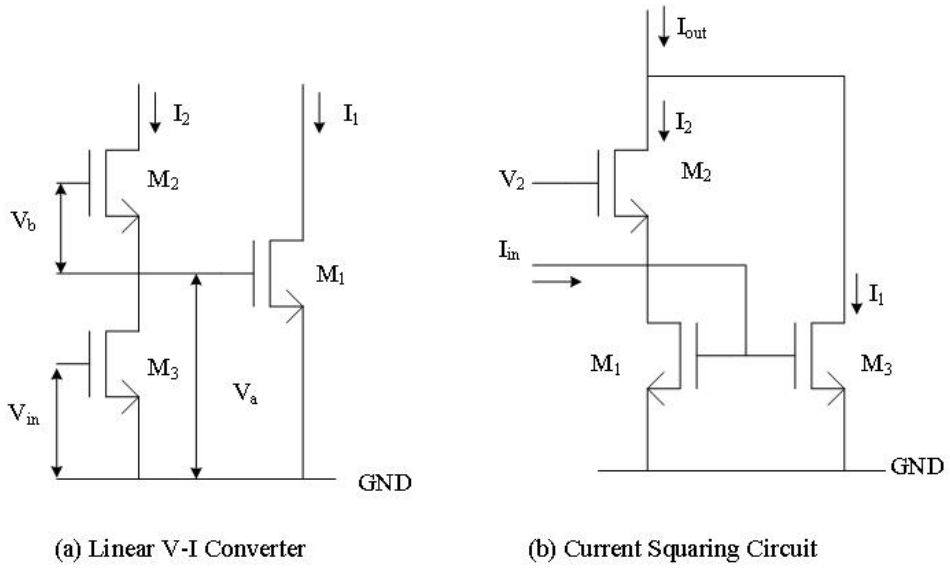
$$\boldsymbol{I_{out} = I_2 - I_1 = \frac{1}{2} k_n' \frac{W}{L} (V_2 - 2V_{tn})(2V_{in} - V_2)} \tag{4.1}$$

$$\boldsymbol{I_{out} = \frac{1}{4} k_n' \frac{W}{L} (V_2 - 2V_{tn})^2 + \frac{Iin^2}{k_n' \frac{W}{L} (V_2 - V_{tn})^2}} \tag{4.2}$$

where k_n' is the NFET mobility factor, and the W/L refers to the aspect ratio of the FETs, which by design are to be equal to each other. From Eq. (4.1), two important restrictions on the value of the bias voltage and the input voltage can be deduced – $V_2 > 2V_{tn}$, and $2V_{in} > V_2$.

Based on these two conditions and the general purpose of the linear voltage to current converter, the following specifications were set

- $V_2 = 2V_{tn} + 1 = 6$ V
- $V_{in\text{-}min} = V_2/2 = 3$ V, $V_{in\text{-}max} = V_2$ (for linearity)
- Current conversion ratio, $\Delta I_{out}/\Delta V_{in} = 20$ µA/V



(a) Linear V-I Converter (b) Current Squaring Circuit

Fig. 4.1. The current converter circuits (a) Linear V-I converter (b) Current squarer.

By differentiating the two sides of Eq. (4.1) the following can be found

$$\frac{dI_{out}}{dV_{in}} = \frac{1}{2}\frac{k_n' W}{L}\,(V_2 - 2\,V_{tn}) * 2$$

$$=> 20 = \frac{1}{2} * 5 * \frac{W}{L} * (6 - 5) * 2$$

$$=> \frac{W}{L} = \frac{20}{5} = 4$$

The FETs M_1, M_2, M_3 were all set to be 8 µm/2 µm in size. The bias generator circuit in Fig. 3.1 (b) is a cascaded NFET pair. The device size was chosen to be the nominal 20 µm/2 µm with two fingers. The current bias is calculated from the standard equation to be 12.5 µA.

PFET current mirrors were used to generate the output current by $I_{out} = I_2 - I_1$. The simulation results from the first pass circuit with 25 °C and 100 °C models are shown in Fig. 4.2.

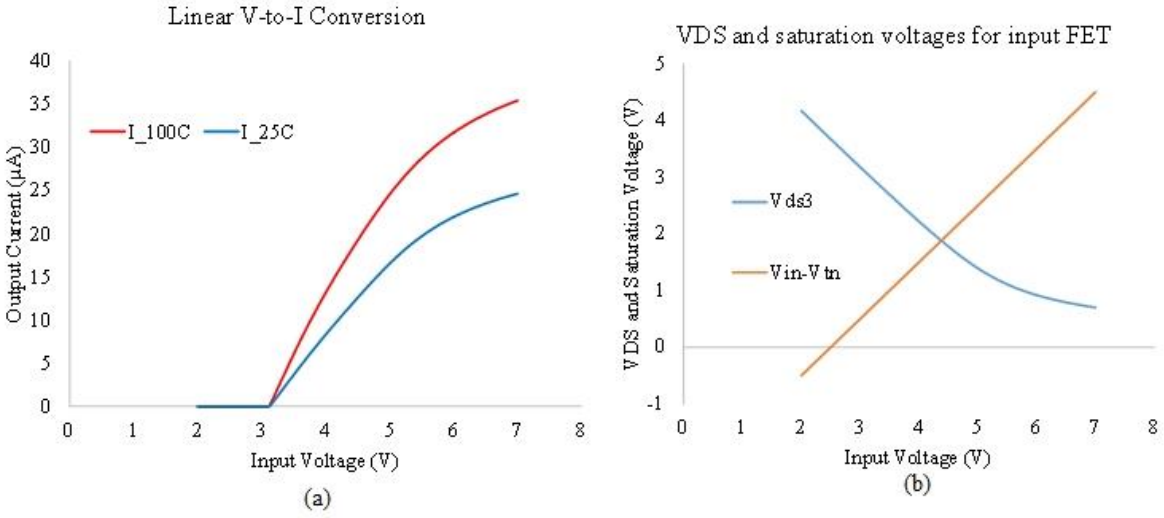


Fig. 4.2. Linear voltage to current converter simulation results with calculated ratios.

As can be seen, the circuit suffers from poor linearity over its input range. An explanation for this can be found in Fig. 4.2 (b), where the drain to source voltage of the input FET is plotted

against its overdrive voltage. As can be seen from the graph, the FET falls out of the saturation region around 4.5 V, which leads to the loss of linearity at higher input voltages.

This issue can be addressed by decreasing the FET aspect ratio of the FET M_3, and doubling the size of the FET M_2 – this would make the FET M_3 pull down its drain voltage less to ground, and also would require a lower gate-source voltage for the FET M_2. To increase the bias voltage, V_2 a little more, the bias current was set to 16 µA. The simulation results are shown in Fig. 4.3.

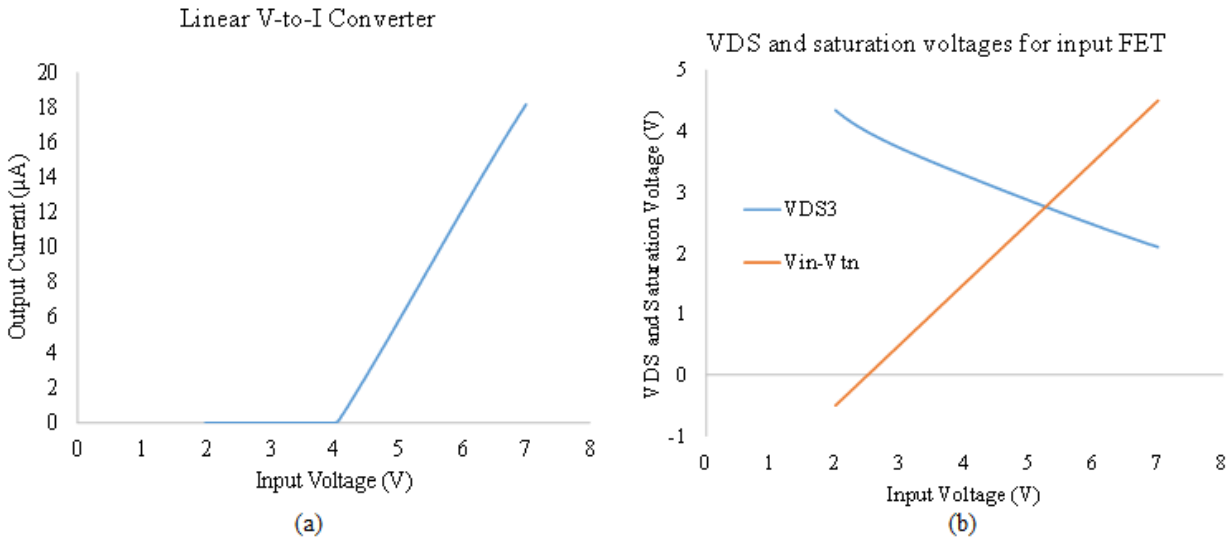


Fig. 4.3. Linear V-to-I simulation results with modified circuit.

The modified simulation results show a bigger region of linear operation for the current converter. The conversion ratio suffers as a result of the smaller input FET, but that can be compensated by using an appropriate current mirror ratio. The simulation results over temperature for the typical FET models are shown in Fig. 4.4. The typical models have two versions of the FET models at 200 °C and 300 °C, as mentioned in Chapter 2, to signify the difference between aged and fresh FETs. The simulation results for the other three models are given in Appendix A. The full circuit for the linear voltage to current converter is shown in Fig. 4.5.

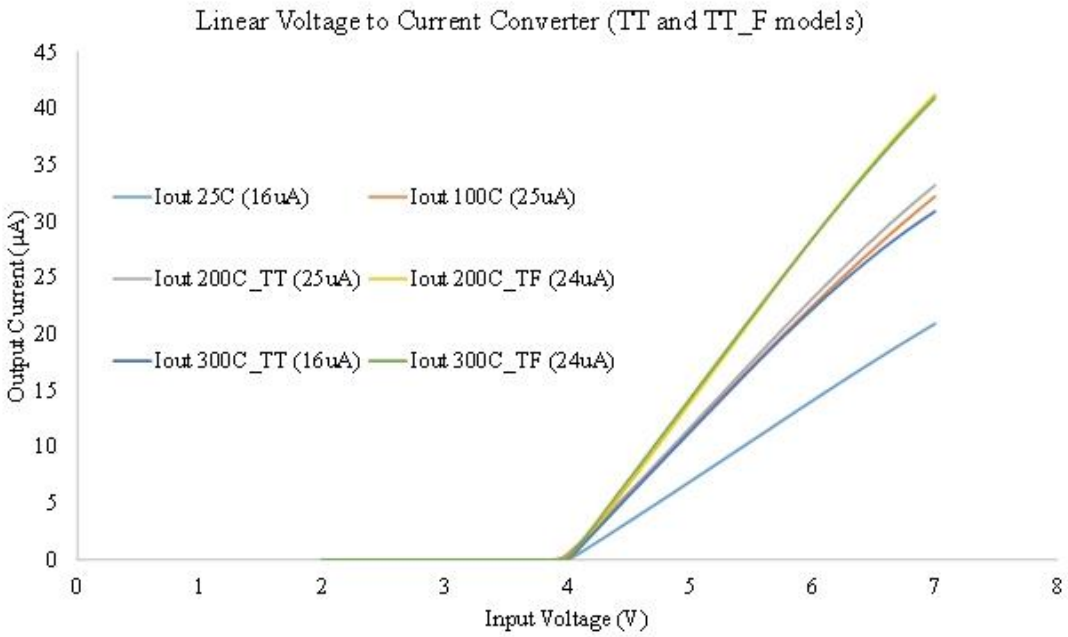


Fig. 4.4. Linear V-to-I converter over temperature for typical models.

The simulation results show a higher current conversion ratio at higher temperatures, especially for the fresh models. This is due to the mobility increase in the FET devices at higher temperatures as already mentioned in Chapter 2. The bias current also has to be changed over temperature to ensure a uniform linear range. These currents are shown in parentheses in the graph.

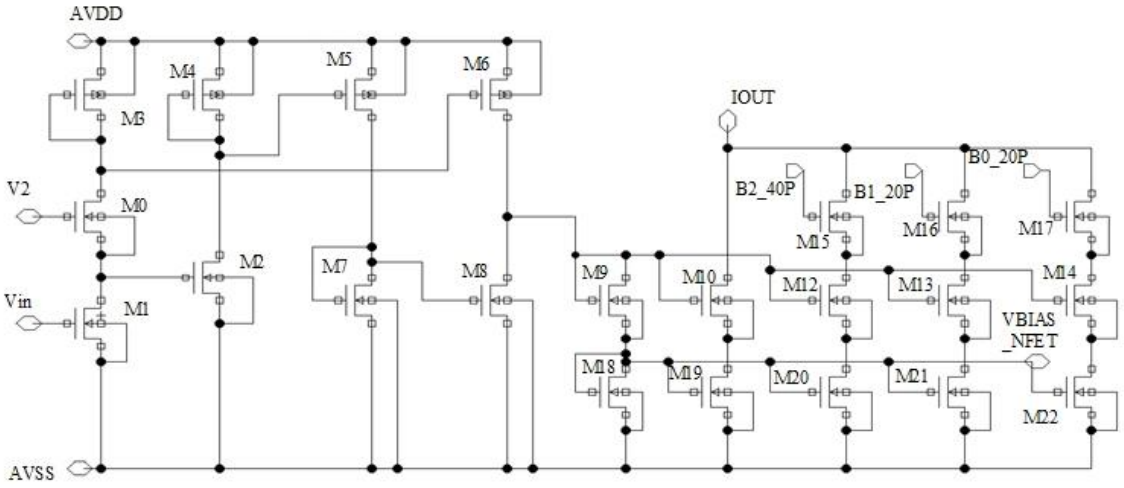


Fig. 4.5. The complete linear to voltage converter with bit settings.

The basic three FET circuit is complemented by a number of current mirrors. The circuit also provides for the option to control the output current level with the addition of three setting pins, B2_40P, B1_20P and B0_20P. The default setting is designed to be 110, which is assumed to be 100%. As is evident from the pin names, the bits add 40%, 20% and 20%, respectively, to the output current. With these settings the current can be controlled from 40% to 120% of the nominal value by the user. The sizes of the FETs used for current mirroring can be found in Appendix A. Adding the bits allows the user to keep the voltage to current conversion gain uniform over temperature. If the bias current were to be supplied from an internal circuit such a scheme could also be used to switch between current levels for that circuit.

4.2.2 Current Squaring Circuit

The current in the biasing circuit seen in Fig. 3.1(a) can be expressed as,

$$\boldsymbol{I_0 = \frac{1}{2}\, k_n' \frac{W}{L} \left(\frac{V2}{2} - V_{tn}\right)^2}$$

$$\text{Or,} \qquad \boldsymbol{I_0 = \frac{1}{8}\, k_n' \frac{W}{L} \left(V_2 - 2V_{tn}\right)^2} \tag{4.3}$$

where W/L is the aspect ratio of the FETs, k_n' is the process mobility coefficient ($\mu_n C_{ox}$) and V_{tn} is the NFET threshold voltage. Assuming the FETs in the current squaring circuit and the FETs in the bias generating circuits share the same W/L ratio, using the relation established in Eq. (4.3), Eq. (4.2) can be rewritten as

$$\boldsymbol{I_{out} = 2 * I_0 + \frac{I_{in}^2}{8 * I_0}} \tag{4.4}$$

The bias current at this point was chosen to be a 10 µA current and, in keeping with the size to current ratio for the FETs, the device chosen for the NFETs were 20 µm/2 µm devices with two fingers each. The bias current choice of 10 µA meant that there would be 20 µA offset to the output and the output would have a current conversion ratio of 0.0125 µA/µA^2. The next step was

the simulation of the circuit over temperature for the all the different types of models. These results are shown in Fig. 4.6.

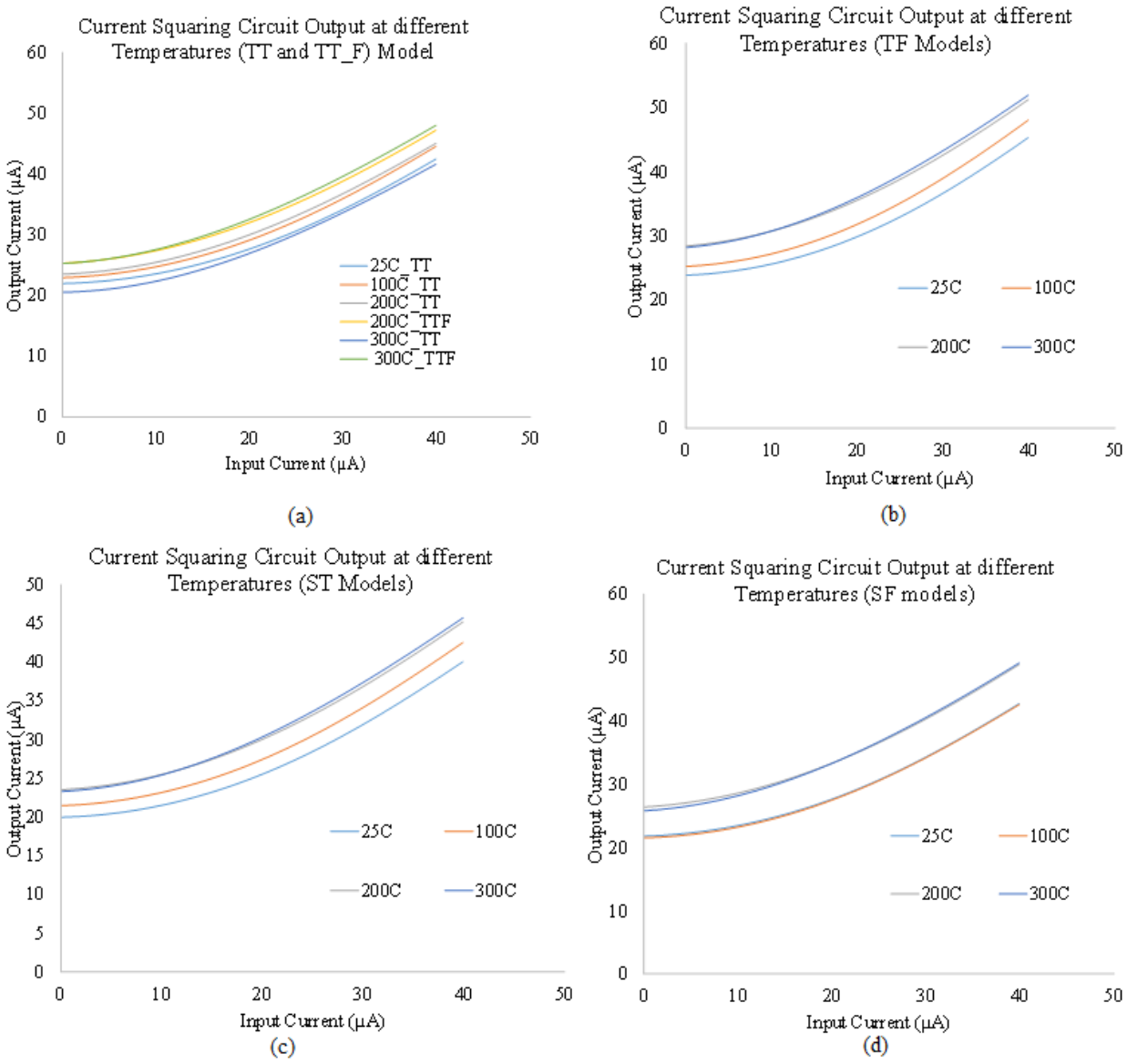


Fig. 4.6. Simulation results for the current squaring circuits over temperature for (a) TT fresh and aged models, (b) TF models (c) ST models and (SF) models.

The input range of the circuit was chosen to be 0 to 40 µA, because that was the upper output limit of the linear voltage to current converter shown in Fig. 4.4. The expected input voltage range to the current converter was 4-6 V, which reflects to a current of 30 µA in the converter

circuit. Hence, an upper limit of 40 µA for the current squarer was a reasonable choice for a maximum target.

As can be seen from the graphs, the current offset for all the models are close to the 20 µA value. The offset current is affected by the PFET current mirrors, and at higher temperatures and for the faster PFET models, the PFET mirrors used in the circuit have a lower threshold voltage, a higher mobility which coupled with the short channel effect increases the output offset current.

The conversion gain for the typical models at the four different temperatures are plotted over the input current range in Fig. 4.7. The conversion gain is considerably higher at the lower values, but settles to a value nearer to the expected 0.0125 µA/µA^2.

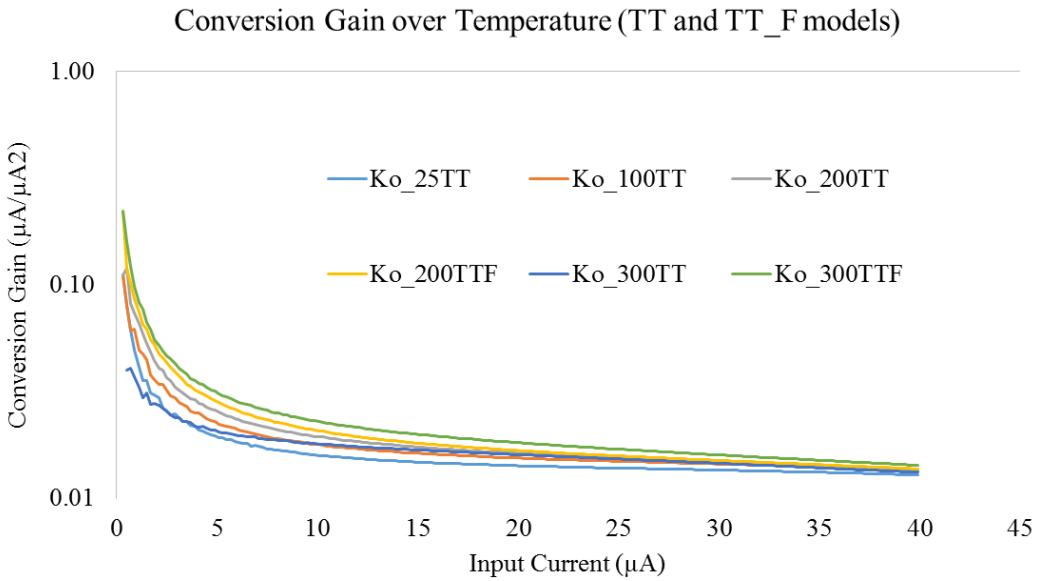


Fig. 4.7. Conversion gain of the current squaring circuit for typical models.

The conversion gains are plotted for the typical models at different temperatures (fresh and aged models at 200 °C and 300 °C). The conversion gains for all the different models are shown in Fig. 4.8. The mean gain conversion for the entire input range for the four types over models at

different temperatures are shown in Fig. 4.8. The conversion gain, around 0.015 μA/μA^2 at room temperature, increases with temperature except for the aged models (TT).

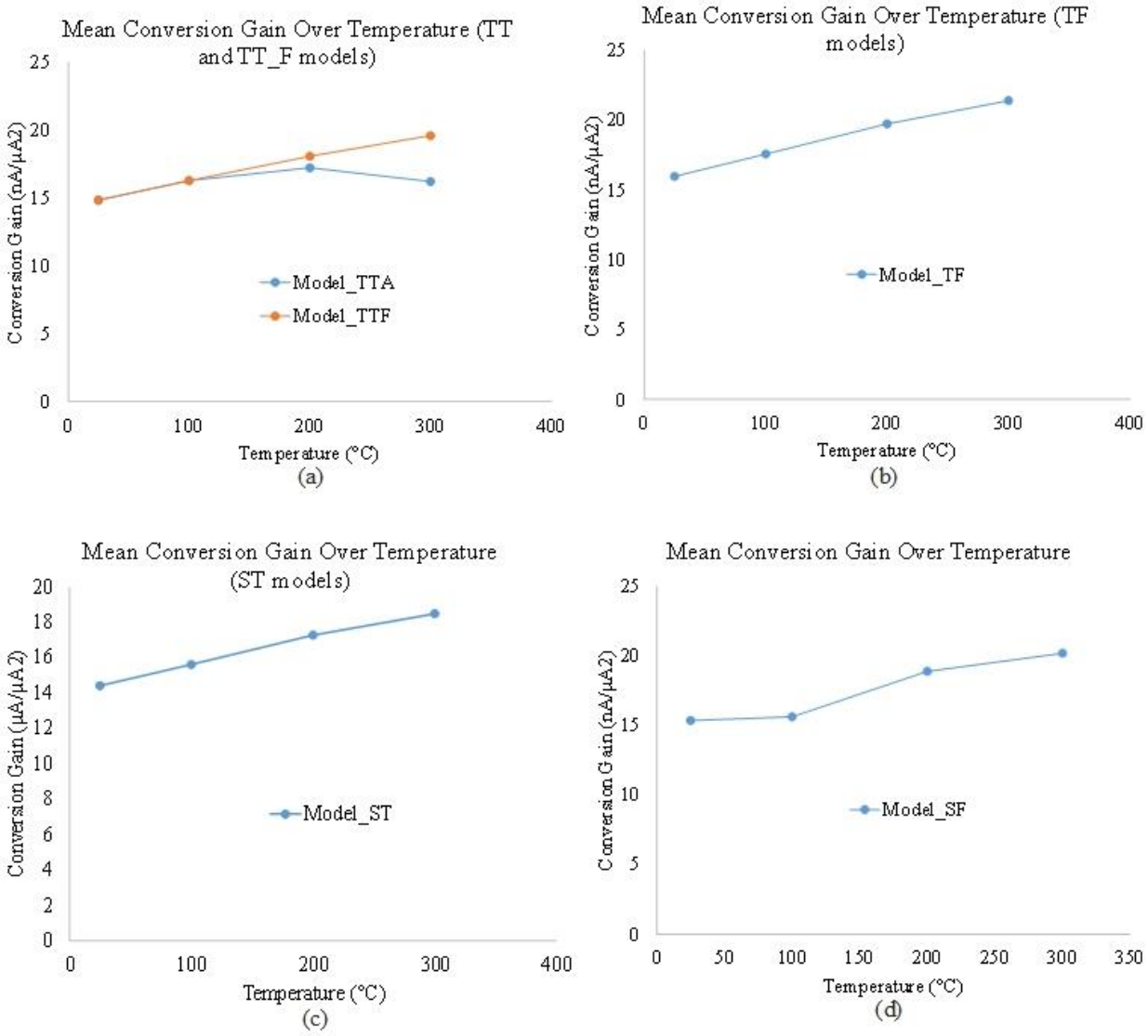


Fig. 4.8. Mean conversion gains over temperature for (a) TT models, (b) TF models, (c) ST models and (d) SF models.

The higher conversion gain can be explained by the faster FETs at higher temperature. The FETs though seem to slow down at higher temperatures due to some aging effect. Even so, the conversion gain is still over 0.015 μA/μA^2 for all conditions.

4.2.3 Current Multiplier Circuit

The current multiplier circuit uses two current squaring circuits to produce the output.

$$(\boldsymbol{I_1 + I_2})^2 - (\boldsymbol{I_1 - I_2})^2 = \boldsymbol{4\, I_1 * I_2} \tag{4.5}$$

A network of current mirrors were used to create the current I_1+I_2 and I_1-I_2. The trick with creating the difference was designing a current network that had to achieve a current of $|I_1 - I_2|$, not $I_1 - I_2$ per say. This is achieved by creating both an $I_1 - I_2$ current and an $I_2 - I_1$ current and adding them together. The current mirror network to achieve this is shown in block diagram in Fig. 4.9. The FET sizes can be found in Appendix A.

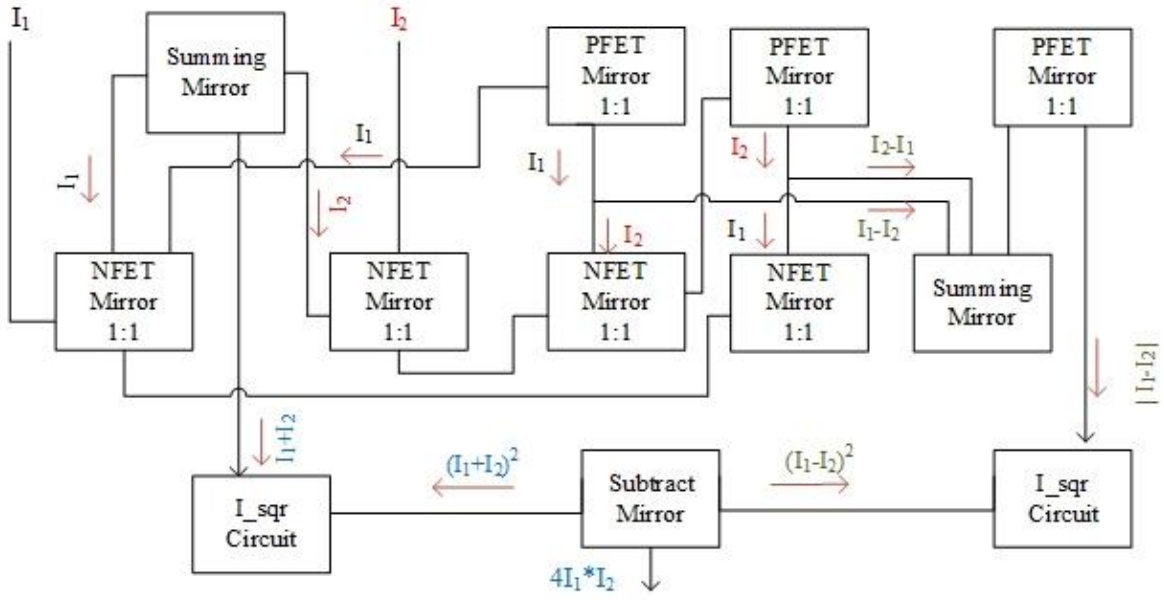


Fig. 4.9. The current mirror network block diagram for the multiplier circuit.

The NFETs mirrors used in the circuit were all cascode current mirrors, so that better output impedance could be achieved. Due to the high threshold voltage of the PFETs, the PFET current mirrors used were all simple current mirrors. The device sizes used for the full circuits are described in brief in Table 4.1.

Table 4.1. Device Sizes for the Multiplier Circuit

Circuit Block	Device Size (µm/µm)	Comment
NFET Mirror	20/2 (m=4)	Ideal for 40 µA of current range
Input PFET Mirror	20/2 (m=6)	Ideal for 30 µA of current range
Summing PFET Mirror	20/2 (m=8)	Ideal for 40 µA of current range
Subtract PFET Mirror	20/2 (m=4)	Ideal for 20 µA of current range
Current Squaring NFETs	20/2 (m=2)	Same from current squaring circuit

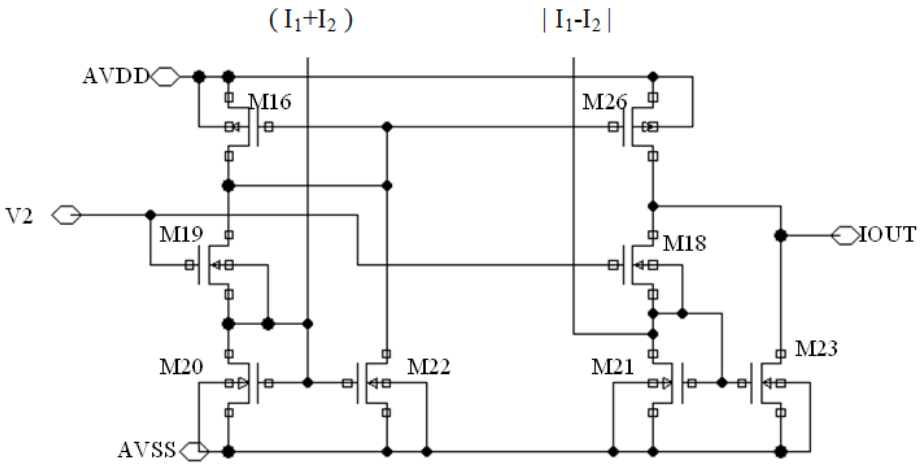


Fig. 4.10. Multiplier circuit last stage with squaring circuits.

The current coming into the drain of the NFET M20, is squared in the form of the current flowing through the NFET M19 and the PFET M16. This current is in turn mirrored by the PFET M26. The other input current, $|I_1 - I_2|$, comes into the drain of the NFET M21, and current flowing through the NFET M18 is the squared form of it. Hence, the current coming out of the pin IOUT, is a current source that is supplying the current $(I_1+I_2)^2 - |I_1 - I_2|^2 = 4\, I_1 * I_2$. Thus, the multiplication operation is achieved. Fig. 4.11 shows the simulation results for the typical FET models at different temperatures. The typical models used here are the non-aged typical models.

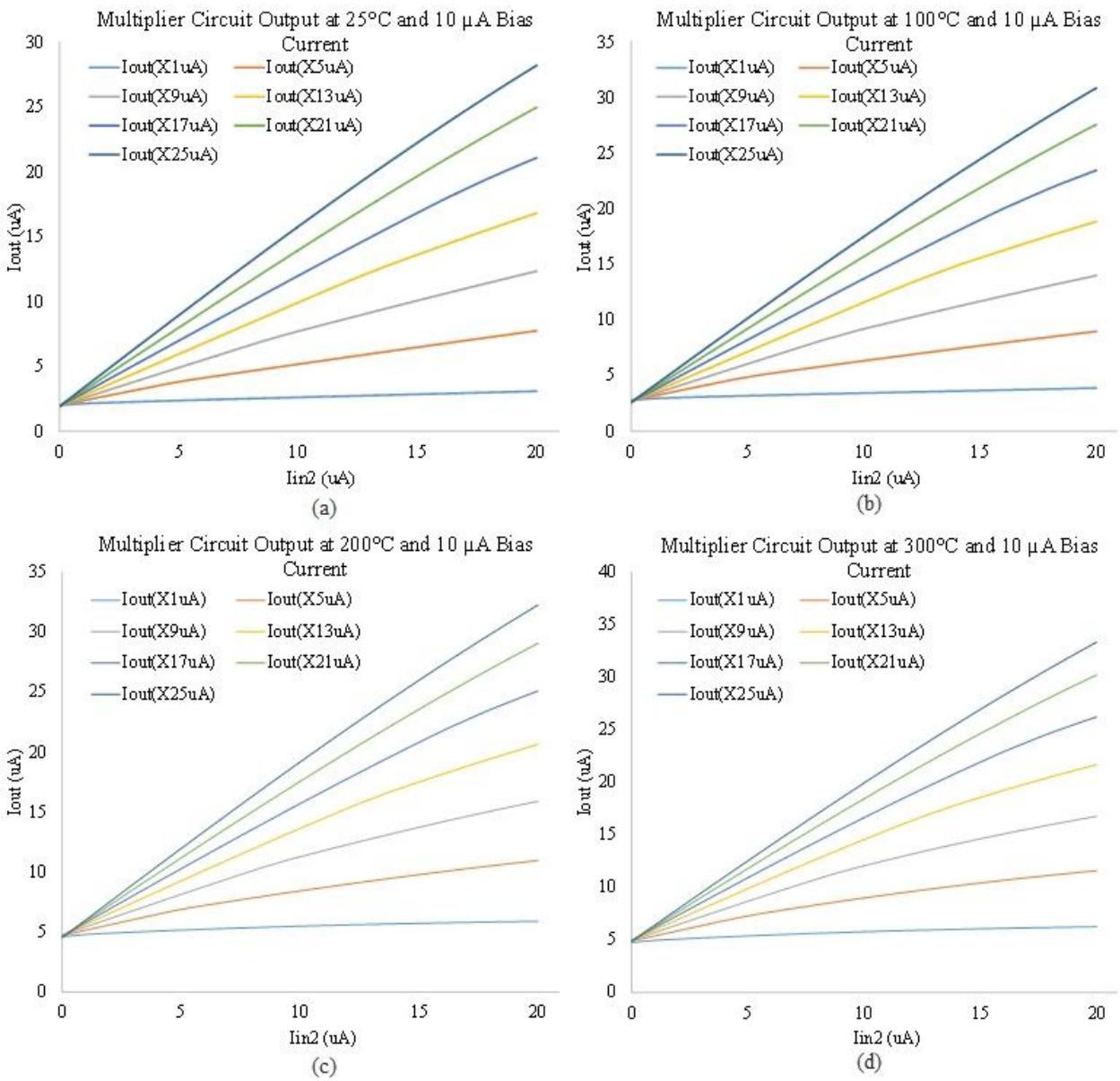


Fig. 4.11. Current multiplier simulation results for the TT models at (a) 25 °C, (b) 100 °C, (c) 200 °C and (d) 300 °C.

The simulations were carried out by setting one of the currents to a specific value (Iin1) and sweeping the other current (Iin2) over a range of 0-20 µA. The simulations were carried out for specific values of Iin1 – 1, 5, 9, 13, 17, 21 and 25 µA to get an idea of the current multiplier response. The simulations show an output offset of around 3-5 µA over temperature. This offset in turn can be handled in the system by using an offset generating circuit that has zero input coming

into the circuit. The conversion gain of the multiplier for the typical FET models are shown in Fig. 4.12. Similar graphs for all the different models can be found in Appendix A.

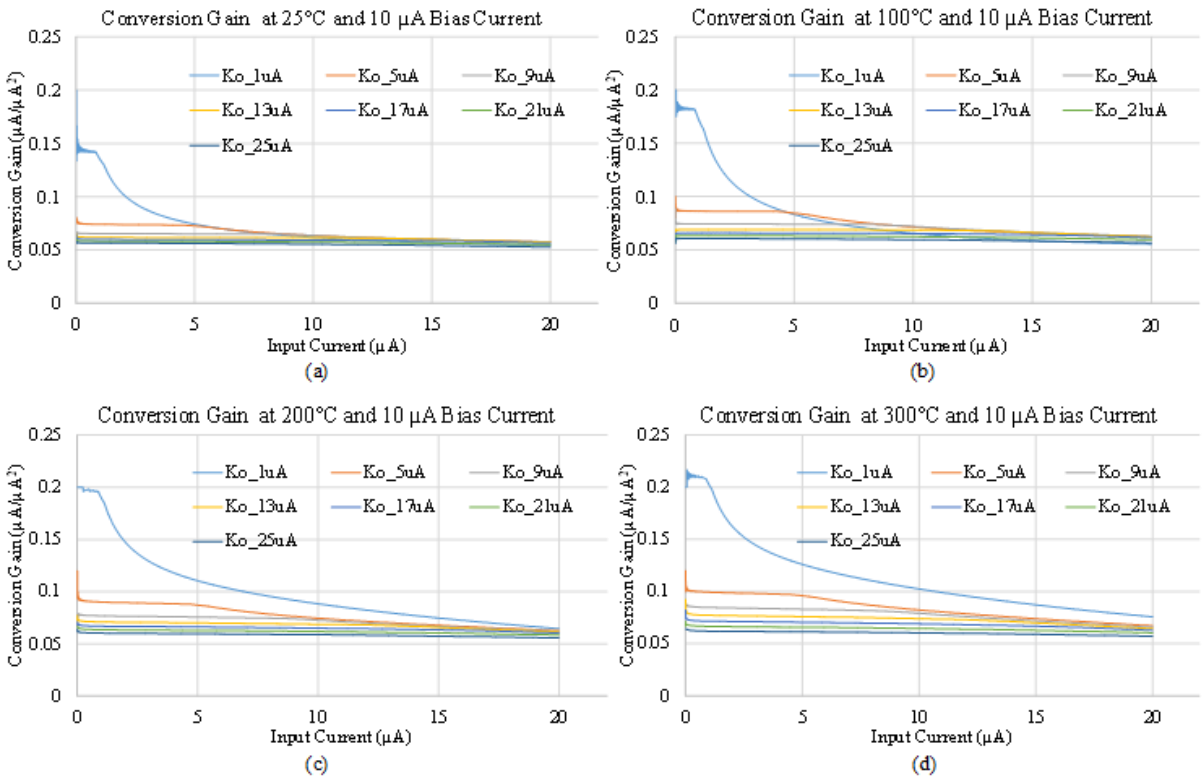


Fig. 4.12. Conversion gain of the multiplier circuit with TT models at different temperatures – (a) 25 °C, (b) 100 °C, (c) 200 °C and (d) 300 °C.

The conversion gain is very high for lower current inputs, but that is to be expected since the non-idealities of the circuits, such as short channel effect, play a larger role at lower inputs. At moderate to high input ranges, the conversion ratio is about 0.06 $\mu A/\mu A^2$, which is four times the conversion ratio for the current squaring circuit. The mean conversion gain for all the models at different temperatures are shown in Fig. 4.13.

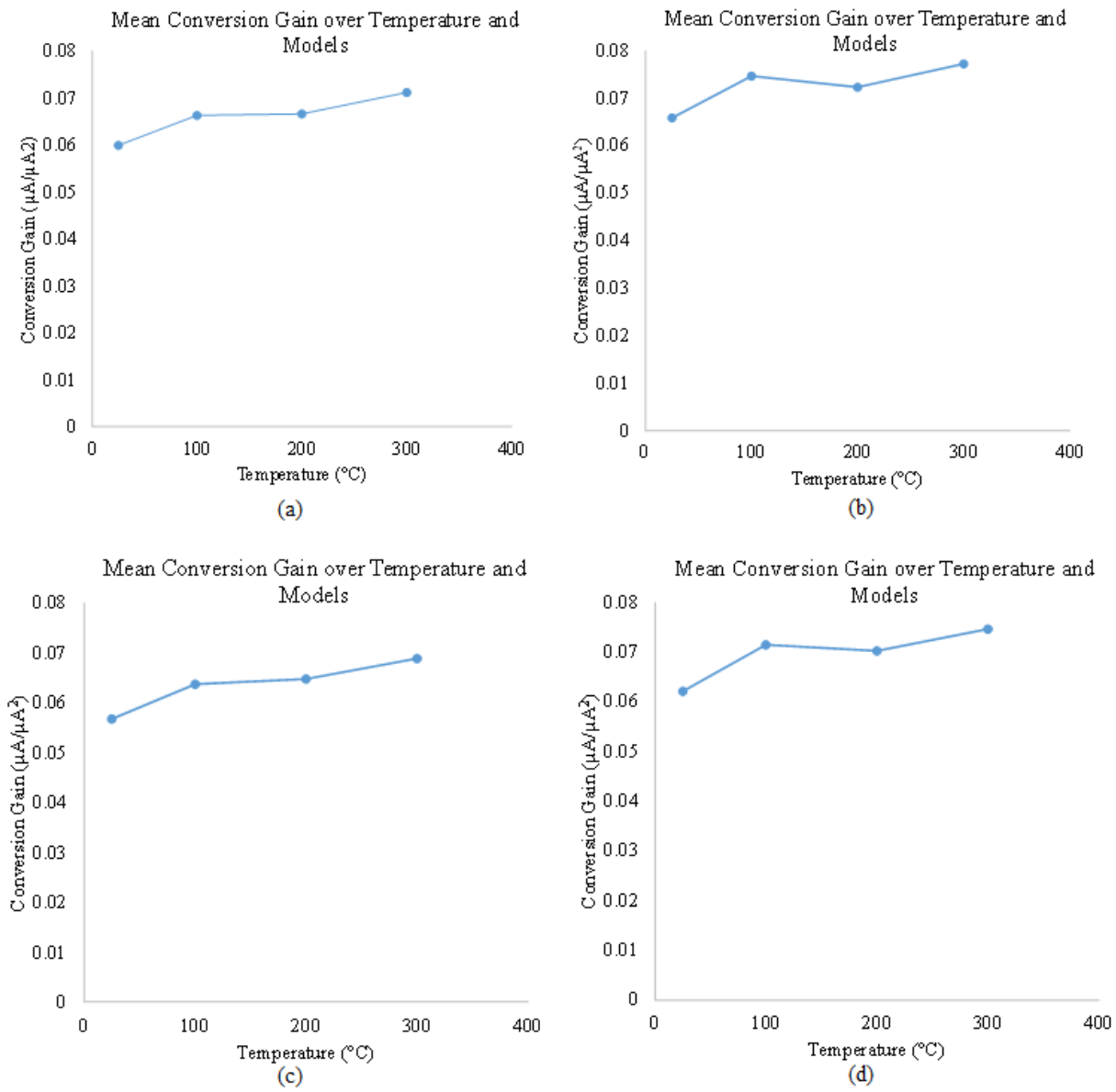


Fig. 4.13. Mean conversion gain of the multiplier circuit over temperature for (a) TT models, (b) TF models, (c) ST models, and (d) SF models.

The mean conversion gain increases with temperature, just like it does for the current squaring circuit. The conversion gain is also higher for fast PFET models, as should be expected.

The linear V-to-I converter, the current squarer and the current multiplier form the basis of the current-mode analog control system.

4.3 Amplifiers and Comparators

The low common-mode operational transconductance amplifier is designed to work with a voltage range that is lower than the 15 V supply. While the use of the PFET input OTA does not provide for high input voltage range operation, it does provide the option to use sensor and system signals that are referred to the ground, and allows for a single-ended signal flow that can be as low as the ground voltage.

The voltage comparator has a higher input voltage range due to the presence of an NFET input stage as well as the PFET input pair. However, due to the vast difference of the FET threshold voltages, complete rail-to-rail operation is not possible. To achieve the current comparator, the first transconductance stage of the voltage comparator is eliminated. The first stage of the voltage comparator converts the input voltages to current sinks. By removing that portion, the inputs to the current comparator can be just the current sinks.

4.3.1 Low Common Mode OTA

The low input common mode OTA was designed to support voltage level shifting for the analog control, sampling circuits and buffers from the data converters. Before the design specifications are given for the circuit, a general overview of the requirement for the system is given below

- The sensor outputs for the DC-DC converter system are expected to be 0-5 V.
- The input range of the voltage to current converter is 4-7 V.
- The input/output range of the data converters is 0-5 V.
- The maximum switching speed of the DC-DC converter was specified as 100 kHz.

- The maximum clock speed for the data converters was specified as ten times the switching speed, i.e. 1 MHz.

4.3.1.1 Design Specifications for the OTA

Based on the applications of the OTA, certain design specifications such as input common mode range, unity gain bandwidth, and slew rate were determined, while the DC gain and phase margin were set more based on the conventional wisdom.

Load capacitance – The target capacitive load for the OTA was chosen to be a 10 pF capacitance. Although this was higher than any load capacitances expected inside the chip itself, the 10 pF load capacitance corresponds closer to the measuring equipment's input capacitance.

Input Common Mode (ICM) range – The input common mode range of the OTA is dictated by the high threshold voltage of the PFET devices. With a supply voltage of 15 V, and a PFET threshold voltage of 6.5 V, the absolute 'theoretical' maximum would be 8.5 V. Allowing for a V_{ds} drop of 1.5 V for the current bias PFET, the maximum ICM was set to 7 V. The minimum common mode can be as low as 0 V, since the PFET V_t is much higher than the NFET V_t.

Unity gain bandwidth (UGBW) – The target unity gain bandwidth was chosen as twice the maximum clock frequency of the data converter which was 1 MHz. This necessitated a minimum unity gain bandwidth of 1 MHz (for the DAC), a desired UGBW of 2 MHz (to provide room for error) and a target of 5 MHz to account for device nonlinearities neglected in the design equations.

Phase margin – The ideal phase margin for an operational amplifier should be around 90° reflecting an OTA with only the dominant pole before UGBW. However, capacitances from large FETs create lower poles that are closer to the UGBW. In such a case, a safe phase margin is

generally understood to be 60°, while an absolute minimum is deemed to be 30°. An extra 'safety' margin of 10° was added to the conventional target to increase the target to 70°.

Slew rate – The slew rate of the OTA is dictated by the required speed of the DAC. For a full voltage range of 5 V, and a clock speed of 1 MHz the required maximum slew rate would be necessary when the output swings full scale in one period, i.e. 5 V/µs.

Open loop gain – The open loop gain (or DC gain) is of less consequence than the previous terms since the OTA is expected to be applied in unity gain or relatively low-gain feedback amplification. Given the SiC FET data, a rough estimate of gains of 100 and 10 from the two stages were made, leading to a specification of a DC gain of 60 dB of the full amplifier.

The target specifications were chosen to be more than the design specifications to account for the device non-idealities not accounted for during the design equation development process. The original system and modified target specifications for design are given in Table 2.1.

Table 4.2. Design Specifications of the PFET Input OTA

OTA Parameter	System Specification	Target Specification	OTA Parameter	System Specification	Target Specification
DC Gain	60 dB	70 dB	Phase Margin	60°	70°
Input Common Mode Range	0 – 7 V	0 – 7 V	Unity Gain Bandwidth	2 MHz (2x switching frequency)	5 MHz
Load	10 pF	10 pF	Slew Rate	5 V/µS	25 V/µS

4.3.1.2 Design Procedure for the PFET input OTA

The schematic of the OTA to be designed is seen in Fig. 4.14 [77]. The OTA uses a current mirror M2, M0 and M6 to provide the currents to the two stages. The input differential pair consists

of the PFETs M1 and M3 and differential loads are the M4 and M5. The input FET of the second stage is M7. C0 is the compensation capacitance, while R1 is the nulling resistor.

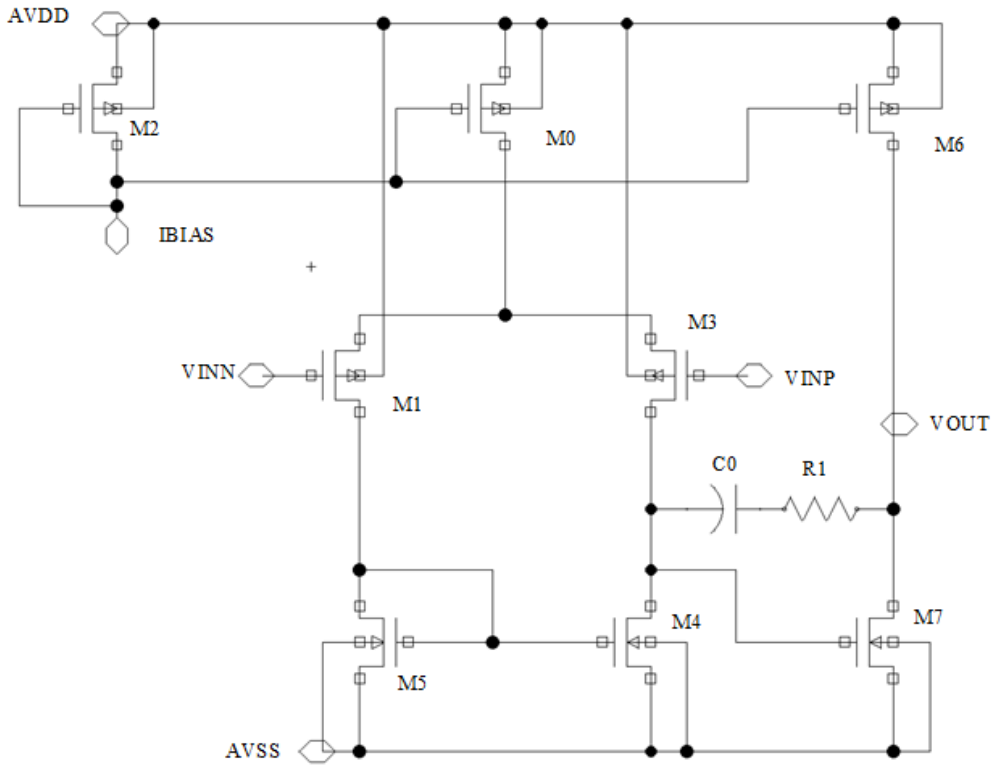


Fig. 4.14. Schematic of the PFET input OTA.

The design sequence for the OTA is based on the equations generated in [77] for the miller compensated op amp with a nulling resistor. Some alterations have been made to fit the need of the system. The first one is the ratio of the zero to the unity gain bandwidth (UGBW). Instead of using a ratio of 10, the ratio chosen was 15 to give a better chance for an OTA that met the system requirement. The phase difference of the OTA at a specific frequency, ω can be written as [77],

$$\boldsymbol{\Phi_M = 180° - \tan^{-1}\left(\frac{|\omega|}{p_1}\right) - \tan^{-1}\left(\frac{|\omega|}{p_2}\right) - \tan^{-1}\left(\frac{|\omega|}{z_1}\right)} \quad (4.6)$$

where p_1 and p_2 are the first and second poles, and z_1 is the left hand zero of the system. The phase margin is the phase difference at the unity gain bandwidth, and the first pole is much smaller than the unity gain bandwidth. So the first term on the right in Eq. (4.5) equals to 90°. With the zero taken to be 15 times the *UGBW*, and the target phase margin as 70°, Eq. (4.5) can be rewritten as,

$$\mathbf{70^\circ = 180^\circ - 90^\circ - \tan^{-1}\left(\frac{|UGBW|}{p_2}\right) - \tan^{-1}\left(\frac{1}{15}\right)}$$

$$\mathbf{\Rightarrow \tan^{-1}\left(\frac{UGBW}{p_2}\right) = 90^\circ - 70^\circ - 3.8^\circ = 16.2^\circ}$$

$$\mathbf{\Rightarrow \frac{p_2}{UGBW} = \frac{1}{tan(16.2^\circ)} = 3.44} \quad (4.7)$$

This relationship dictates the ratio of the load capacitance and the compensation capacitor, which is given by,

$$\mathbf{C_0 > \frac{3.44 C_L}{10}} \quad (4.8)$$

where the second pole is expected to be ten times that of the *UGBW*. Using the load capacitance as 10 pF, the compensation capacitance is then selected as 4 pF.

A step by step design procedure of the OTA is described in Table 4.3. For simplicity, aspect ratios of FETs will henceforth be referred to as S. The FET dimensions calculated are generally rounded up to the nearest multiple of 10 in order to support the use of the nominal 20 µm/ 2 µm FET devices. When deemed fit, differential pairs are set to multiples of 40 or 20 to support an even number of fingers. Fingers that are multiples of four are easier to lay out according to the common centroid and inter-digitation principles and provide the best mitigation against process gradients over the wafer.

Table 4.3. Design Procedure of the Low Input Common Mode OTA

Step	Parameter/ Device	Governing Equations	Design Assumption/ Comment	Value
1	Source Current, I_0	$I_0 = SR \,.\, C_0$	Slew Rate = 25 V/µs C_0 = 4 pF	100 µA
2	M1, M3	$UGBW = \frac{gm_1}{C_0}$ $g_{m1} = \sqrt{2 * I_1 * k'_p S_1}$	$UGBW$ = 5 MHz I_1 = 50 µA	$S_{1,3}$ = 126 (Set to 130)
3	M4, M5	$I_4 = \frac{1}{2}\, k'_n\, S_4 (v_{gs4} - V_{tn})^2$	v_{gs4} = ½ $\|Vtp\|$ = 3.25 V for proper operation [a] I_4 = 50 µA	$S_{4,5}$ = 36 (Set to 40)
4	M0, M2	$I_0 = \frac{1}{2}\, k'_p\, S_0 (v_{sg0} - \|V_{tp}\|)^2$	v_{sg0} = 15 – 7 = 8 V Max. ICM = 7 V	S_0 = 112 (Set to 120)
5	M7	$g_{m7} = 15 * g_{m1}$	$\frac{gm_7}{gm_1} = \frac{z_1}{UGBW}$	g_{m7} = 1502 µA/V^2
		$\frac{g_{m7}}{gm_4} = \frac{S_7}{S_4}$	Assumed $v_{gs7} = v_{gs4}$ $g_m = k'_p S_7 \sqrt{V_{ov}}$	S_7 = 380
6	M6	$I_{6,7} = \frac{1}{2}\, k'_n\, S_7 (v_{gs6} - V_{tn})^2$	$I_6 = I_7$	I_6 = 475 µA
		$\frac{S_6}{S_0} = \frac{I_6}{I_0}$	Current mirror of M0, M2 and M6	S_6 = 570
7	R_z	$R_z = \frac{(C_0 + C_L)}{C_0} * \frac{1}{g_{m7}}$	To nullify the right hand zero	R_z = 2.9 kΩ

[a] Normally this is set by the minimum input common mode voltage. However, since in this case the PFET threshold voltage is far higher than the NFET threshold voltage, the minimum common mode will not affect the sizes.

The results of the AC simulation of the circuit with a common mode input voltage of 5 V are shown in Fig. 4.15. The circuit showed a DC gain just under 60 dB, a unity gain bandwidth of 1.6 MHz, and a phase margin of 71°. Minor modifications were then made to aid layout and phase

margin. The output stage current was lowered to 400 µA, and the nulling resistor was increased to 6 kΩ. The calculated values and the designed dimensions are shown in Table 4.3.

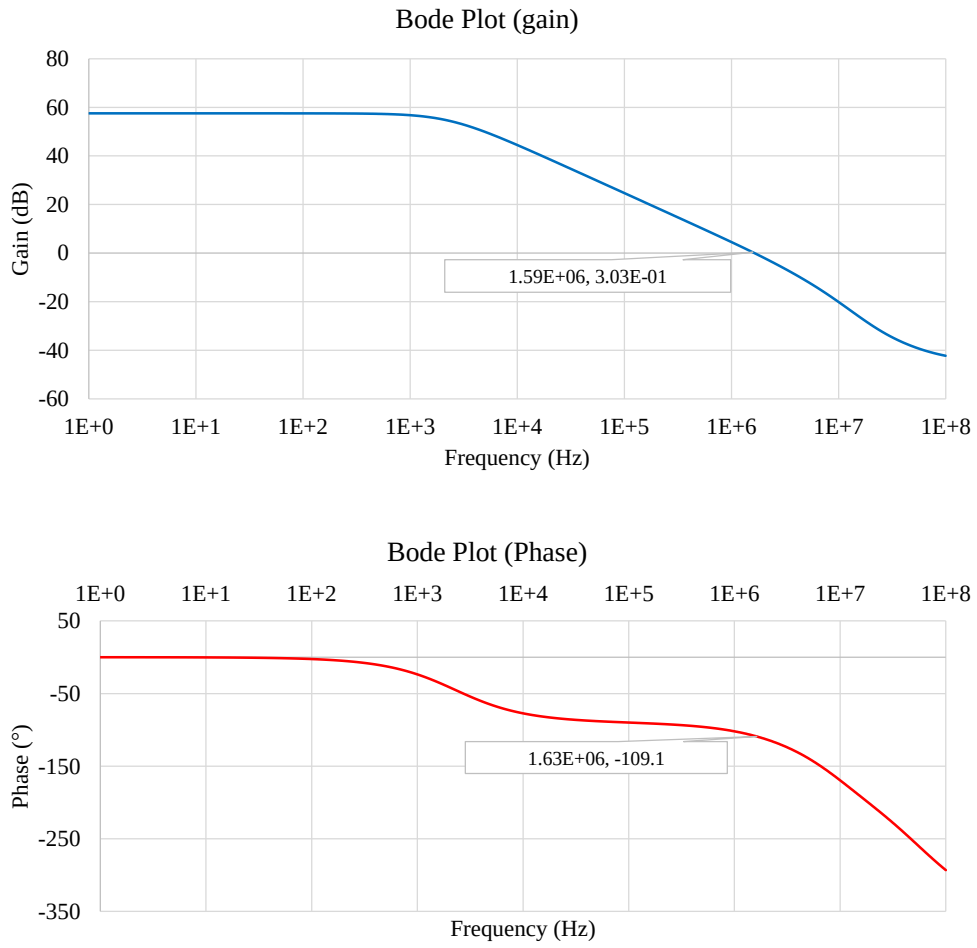


Fig. 4.15. Bode plots for the OTA with calculated values.

Table 4.4. Device Dimensions for the OTA

Device Type	Calculated Spec	Design Dimension	Device Type	Calculated Spec	Design Dimension
M1/M3	130	20 µm/2 µm (m=16)	M6	570	20 µm/2 µm (m=640)
M0/M2	120	20 µm/2 µm (m=16)	M7	380	20 µm/2 µm (m=400)
R_z	2.3 kΩ	6 kΩ	I_6 / I_7	475 µA	475 µA

4.3.1.3 Simulation Results for the Modified OTA

The Bode plots for the modified circuit are shown in Fig. 4.16. The DC gain stays pretty much the same while the gain bandwidth decreases to 1.45 MHz, and the phase margin is improved to 75°. After settling on the design, simulations were run over process corners for the different performance parameters associated with a general OTA.

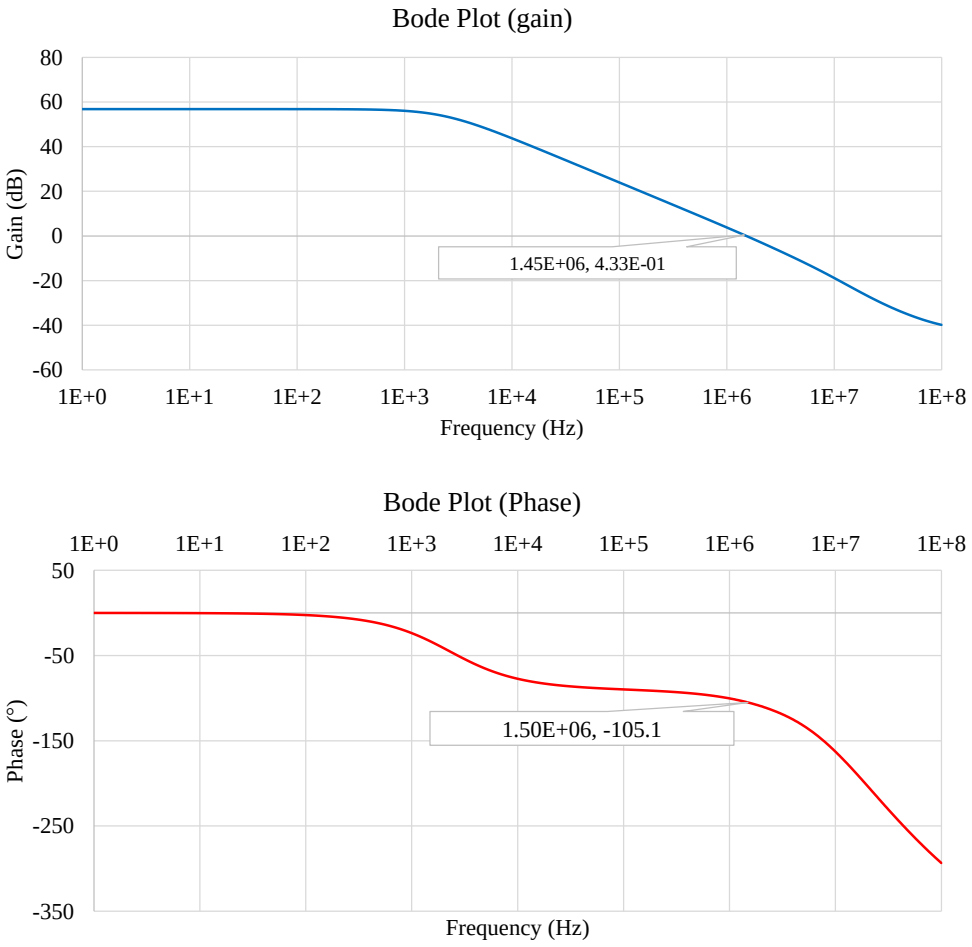


Fig. 4.16. Bode plots for the OTA with minor modifications.

The AC characteristics of the OTA (DC gain, unity gain bandwidth and phase margin) over temperature are shown in Fig. 4.17. The typical models used for simulation are the non-aged

models for 200 °C and 300 °C. As expected performance gets better with temperature for all models.

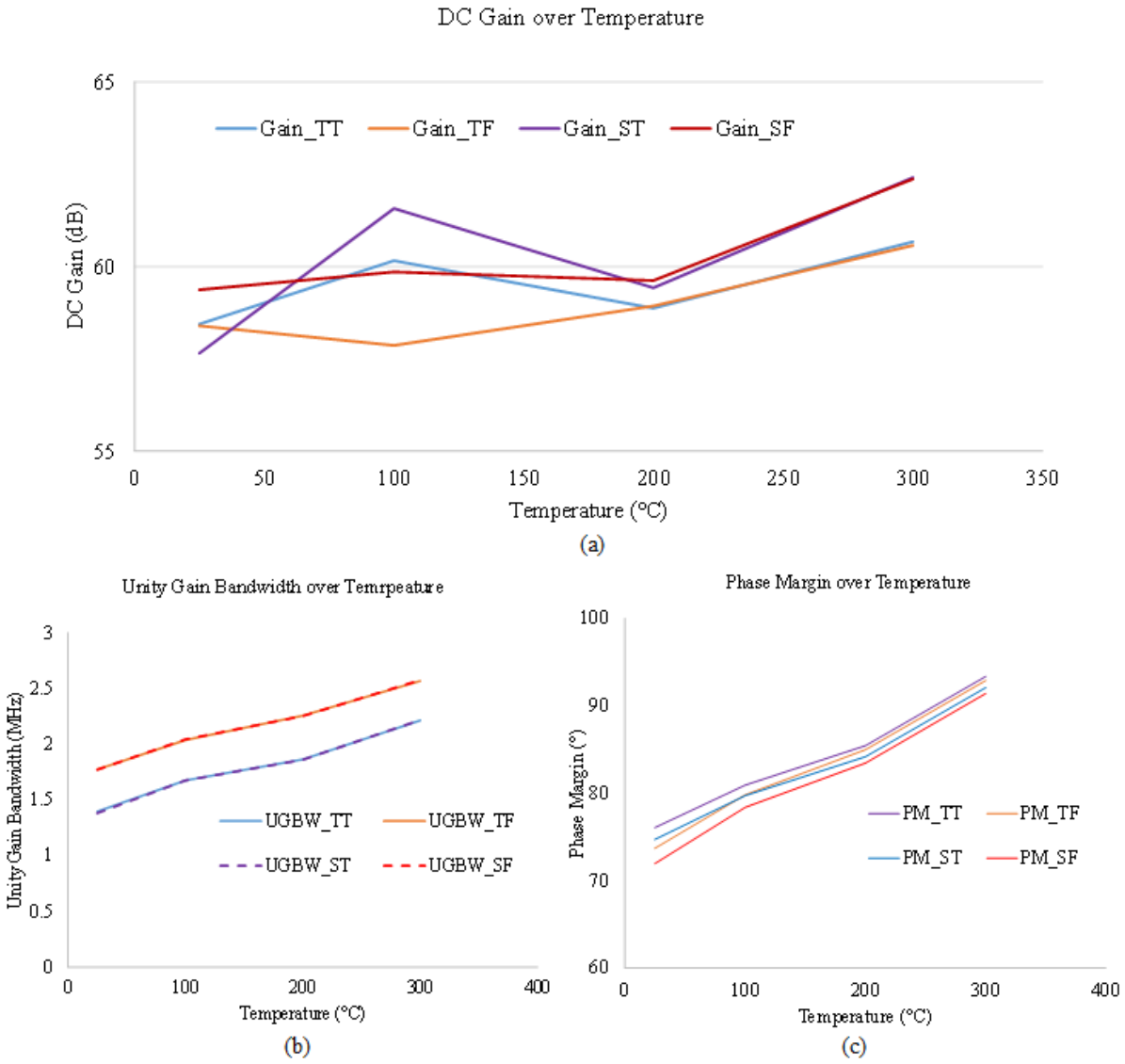


Fig. 4.17. AC characteristics for the OTA over temperature (a) DC gain, (b) unity gain bandwidth, and (c) phase margin.

Over temperature, the DC gain has a range of 58 - 63 dB, the unity gain bandwidth of 1.4 – 2.5 MHz, and the phase margin of 72° – 92°. Some additional characteristics of the OTA are show in Fig. 4.18 (slew rates) and Fig. 4.19 (input common mode).

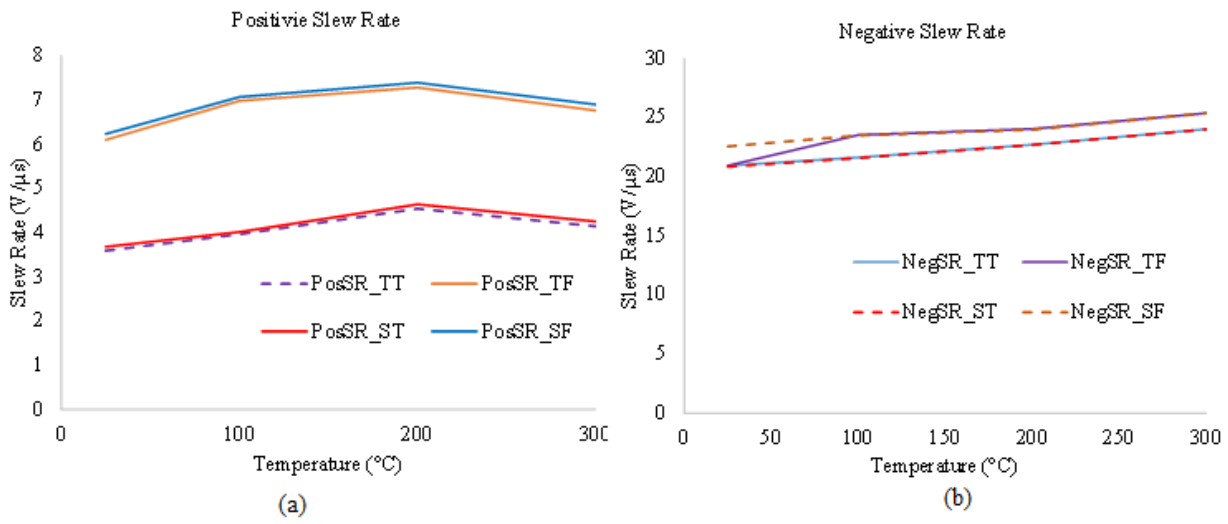


Fig. 4.18. Slew rate of the OTA - (a) Positive slew rate and (b) Negative slew rate

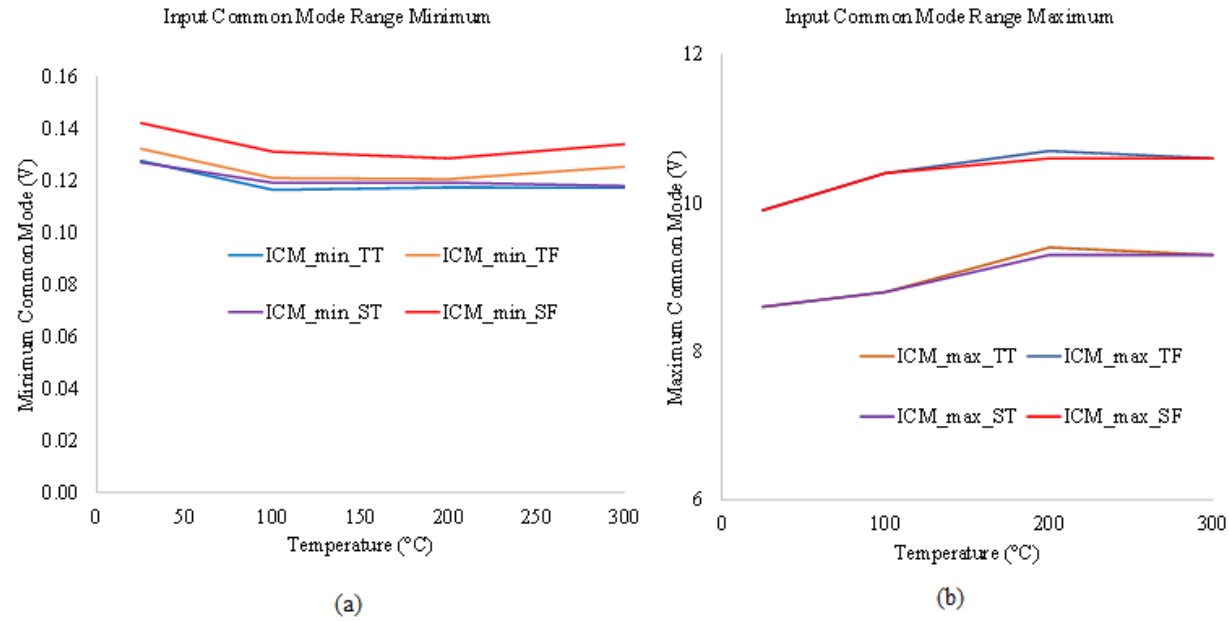


Fig. 4.19. Input common mode range of the OTA - (a) Minimum and (b) Maximum ICM

The positive slew rate of the OTA is around 4 V/µs for the typical PFETs and 6-7 V/µs for fast PFETs, while the negative slew rate is much higher 20 V/µs. Although the positive slew rate is lower than what the design specifications were, given the system requirements of maximum input of 5V, it was not deemed to be of major concern.

The minimum input common mode over temperature for all the models is found to be in the range of 0.11-0.14 V. Although not exactly zero as hoped, this is 2-3% of the full voltage range which is acceptable for a first pass design. The maximum input common mode is very different for the PFET model types. As should be expected the maximum input common mode is much lower for the typical PFET models (8 to 9 V over temperature) than for the fast PFETs (10 – 10.5 V over temperature). This can be explained by the lower threshold voltages of the fast PFETs. Also, as temperature increases the same lessening of the threshold voltage explains the gradual increase in the maximum input common mode.

4.3.2 Three-Stage Comparator with Complementary Input Pairs

The three-stage comparator is comprised of a pre-amplifier, the positive feedback decision making system, and the output stage with the differential amplifier and the digital buffers [70]. The functions of the different stages have already been explained in Chapter 3. The full schematic of the comparator has been broken into two parts and shown in Fig. 4.20. The three main parts are

- Pre-amplification stage – Comprised of the PFET input pair M7 and M11, NFET differential loads and mirrors M2, M3, M5, and M6, the NFET input pair M0 and M4, the PFET load M9 and M12, as well biasing FETs M14, M8, M15 and M1. The inputs to both the PFET and NFET input pairs are transformed into current which are then fed into the load pair M9 and M12. The voltages generated on PFET drain nodes, *Stg1_P* and *Stg1_N* are the inputs to the next stage.
- Positive feedback decision stage – The FETs M21 and M22 are the inputs to this stage, while the FETs M16-M19 make up cross-coupled section. The gate-drain tied M20 provides a self-biased tail current to the decision stage.

- The output stage consists of the post decision differential amplifier (M23-M27) and two back to back inverters (M28-M31) acting as a buffer.

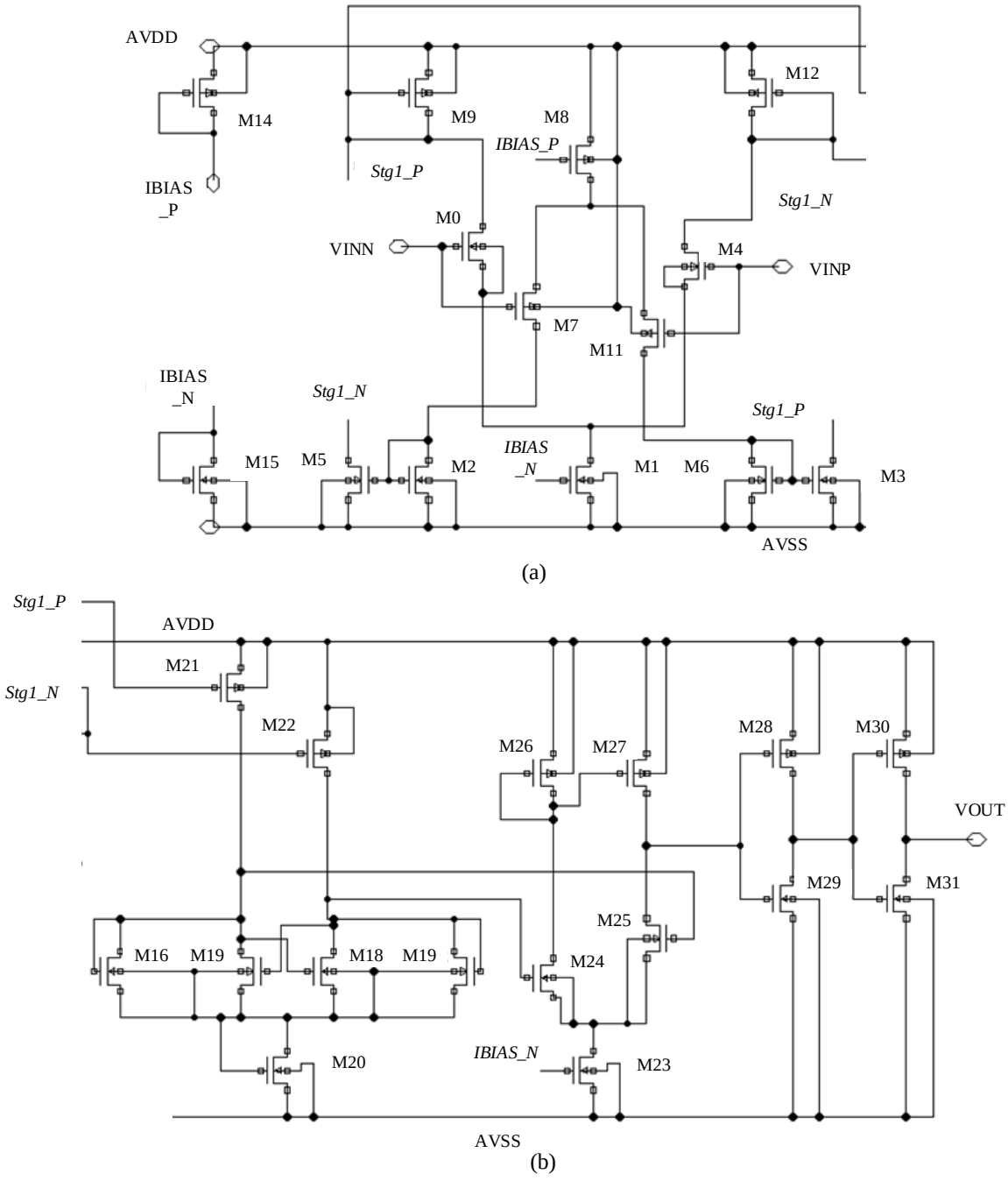


Fig. 4.20. Full Schematic of the comparator in parts (a) Complementary pre-amplification input stage and (b) Positive feedback decision stage and output buffer.

4.3.2.1 Design Specifications

The design specifications were determined based on the maximum clock speed of the converters which was set to be 1 MHz (or 1 μs) for the data converters. Some target specifications were then set at higher performance levels to compensate for non-idealities unaccounted for in design equations. Once again, circuits were over-designed to meet required specifications.

- Rise/Fall times – 50 ns (5% of clock period), design target was set to 25 ns.
- Propagation delay – 200 ns (20% of clock period), design target was set to 150 ns
- Load – capacitive load of 10 pF
- Hysteresis – 30 mV - 1.5 times of the LSB for an 8-bit data converter at 5 V range.

4.3.2.2 Design Procedure for the Voltage Comparator

A detailed design procedure for this particular topology [70] of the comparator is not found in the text books for analog circuit design. Hence, the design was carried out through some intuition and general procedure. A step-by-step description of the design is given in this section. The approach taken here is a back to front approach where the sizes of the FETs are determined from the latter stages to the earlier stages. Hence, the design begins with the output stage buffers. A step-by-step design procedure of the voltage comparator is given in Table 4.5.

Unlike the OTA, the comparator has only a handful of specifications – hysteresis voltage, rise and fall times, and propagation delays. The rise and fall times and propagation delays are derived from the maximum clock frequency, and the minimum clock half period. The hysteresis voltage is calculated based upon the LSB value of the data converters. The comparator is designed in a back to front design procedure, where the digital buffers, M28-M31, are first designed based upon the rise and fall times requirements. The digital buffers themselves pose as outputs to the

post-decision amplifiers and are used as the loads for the design of the output differential stage. The output differential stage, comprising of FETs M23-M27, is designed to have a delay of 10% of the target propagation delay. The tail current FET, M20, in the decision block is also determined by the target propagation delay.

The cross-coupled decision block load devices, M16-M19, are designed based upon the hysteresis voltage specification of 30 mV. The current through the devices has to switch very quickly as their gate voltage changes. The input devices of the decision block, M21 and M22 are designed based upon an assumption of an attenuation of two in the decision block.

Finally, the pre-amplifier block loads and current source and sink devices were designed based upon the requirement of the propagation delay, while the input amplifier FETs, M0, M4, M7 and M11, were designed based upon the target hysteresis voltage. In most cases the saturation voltage for the tail current FETs were chosen similar to be similar to the OTA.

Some general guidelines followed during the design part were to use 24 µm/ 1.2 µm devices for PFETs in digital circuits and either 24 µm/ 1.2 µm or 12 µm/ 1.2 µm devices for NFETs. For analog circuits, the default FET unit was a 20 µm/ 2 µm device. FETs were also sized to have aspect ratios of either 20 or 40. This would in turn help with the common centroid layout of the devices by allowing an even number of fingers. The gate capacitance was estimated through the simulation of supplying a small current, 1 nA, to a to the gate of an NFET whose drain, source and body were connected to ground. The change in the gate voltage over time indicated a total gate capacitance of approximately 38 fF for a 20 µm / 1.2 µm device, which comes out to about 1.6 $fF/\mu m^2$. As such, the gate capacitance was assumed to be 2 $fF/\mu m^2$ for a more conservative approach.

Table 4.5. Design Procedure for the Voltage Comparator

Step	Parameter/ Device	Governing Equations	Design Assumption/ Comment	Value
1a	M31, M30	$\frac{I_{30}}{2} = I_{31_avg} = C_L * \frac{\Delta V}{\Delta t_{rise}}$	Design for rise time $\Delta trise$ = 25 ns ΔV = 12 V (10-90%)	I_{30} = 9.6 mA
		$I_{30} = \frac{1}{2} k'_p S_{30} V_{ovp}^2$	V_{ovp}=15V-|Vtp| = 8.5V	S_{30} = 332 (Set to 360)
		$\frac{S_{31}}{S_{30}} = \frac{1}{3}$	PFET-NFET ratio set to 3:1 in digital circuits	S_{31} = 120
1b	M29, M28	$\frac{S_{28}}{S_{30}} = \frac{1}{3}$	Load ratio set to 3:1 for buffer chain	S_{28} = 120
		$\frac{S_{29}}{S_{28}} = \frac{1}{3}$	PFET-NFET ratio set to 3:1 in digital circuits	S_{29} = 120
2a	M23	$I_{23} = C_L * \frac{\Delta V}{\Delta t_{rise}}$ $C_L = C_{gs28} + C_{gs29}$ $\Delta V = V_{supply}/5$ $\Delta t_{rise} = 0.1 * Delay_{prop}$	C_L = 460 fF, V_{supply} = 15 V $Delay_{prop}$ = 15 ns Δ V = 3 V, Δt_{rise} = 15 ns	I_{23} = 92 µA (Set to 90 µA)
		$I_{23} = \frac{1}{2} k'_n S_{23} (v_{gs23} - V_{tn})^2$	v_{gs23} is set to 3.25 V (similar to OTA design)	S_{23} = 64 (Set to 60)
2b	M26, M27	$I_{26} = \frac{1}{2} k'_p S_{26} (v_{sg26} - \|V_{tp}\|)^2$	v_{sg26} is set to half of the 15 V supply, v_{sg26} = 7.5V Using S_{26} = 160 allows for v_{sg26} = 7.35 V	$S_{26,27}$ = 112 (Set to 160 for more head room)
2c	M24, M25	$Gain_{diff} = g_{m24} * r_{load}$ $r_{load} = r_{ds25} \| \| r_{ds27}$ $r_{ds25} = r_{ds27} = \frac{1}{\lambda I_{d25}}$	$Gain_{diff}$ is set to half of (ΔV in step 2a)/30 mV[a] This leads to gain of 50 r_{load} = 222.2 kΩ	g_{m24} = 225 µA/V

Step	Parameter/ Device	Governing Equations	Design Assumption/ Comment	Value
		$gm_{24} = \sqrt{2 * I_{25} * k'_n S_{24}}$	Common definition for transconductance	S_{24} = 112 (Set to 120)
3a	M20	$I_{20} = C_{L20} * \frac{\Delta V}{\Delta t_{rise}}$ $C_L = C_{gs24} = 960\ fF$	Slew rate assumed to be same as differential stage $SR = \frac{3V}{15ns} = 200\frac{V}{\mu s}$	I_{20} = 192 µA
		$I_{20} = \frac{1}{2}\ k'_n\ S_{20}(v_{gs20} - V_{tn})^2$	v_{gs20} is set to 4 V (~ 1/4th of power supply	S_{20} = 36 (Set to 40)
3b	M16-M19	$\Delta I_{16} = gm_{16}\Delta v_{gs16}$ $\Delta I_{16} = \frac{I_{21}}{10} = \frac{I_{20}}{20}$ $\Delta v_{gs16} = 2 * V_{hyst}$ $gm_{16} = \sqrt{2 * I_{16} * k'_n S_{16}}$	The cross-coupled FETs are expected to change its current by 1/10th of the full range as its gate voltage changes by twice the hysteresis.	$S_{16\text{-}19}$ = 56 (Set to 60)
3c	M21, M22	$gain_{XC} = \frac{gm_{21}}{gm_{16}}$ $gm_{21} = \sqrt{2 * I_{21} * k'_n S_{21}}$	The differential gain of the cross-coupled part is assumed to be 0.5	g_{m21} = 86 µA/V S_{21} = 47 (Set to 60)
4a	M9, M12	$\Delta I_{12} = C_{L12} * \frac{\Delta V}{\Delta t_{rise}}$ $\Delta V = \Delta v_{gs16} * \frac{2}{gain_{XC}}$ $\Delta I_{12} = \frac{I_{12}}{10}$ $C_{L12} = c_{gs21} = 480\ fF$	The voltage differential is taken as the voltage required to generate the required v_{gs16}. The charging current is assumed to be 10% of the total current in M12.	SR = 8 V/µs I_{12} = 39 µA
		$I_{12} = \frac{1}{2}k'_p S_{12}(v_{sg12} - \lvert V_{tp}\rvert)^2$ $V_{ICM_max} = 15 - v_{sg12} - V_{tn}$	V_{ICM_max} is set to 9 V That leads to vs_{g12}= 2 V	$S_{9,12}$ = 24 (Set to 30)

Step	Parameter/ Device	Governing Equations	Design Assumption/ Comment	Value
4b	M1, M8	$I_1 = I_8 = 1.5 * I_{12}$	The source and sink currents are set to 1.5 times of the load current	$I_{1,8}$ = 58 µA
	M1	$I_2 = \frac{1}{2}\, k_n'\, S_2 (v_{gs2} - V_{tn})^2$	v_{gs1} assumed to be 3.25 V (same as M23)	S_1 = 41 (Set to 40)
	M8	$I_{12} = \frac{1}{2} k_p' S_{12} (v_{sg12} - \lvert V_{tp} \rvert)^2$	v_{sg12} set as 2 V (same as M9)	S_2 = 36 (Set to 40)
4c	M0, M4 M7, M11	$gain_{PA} = \frac{gm_0 + gm_7}{gm_{12}}$ $gain_{PA} * gain_{Xc} * gain_{diff} = 100$ $gm_0 = 3 * gm_7$	The total gain of the pre-amp stage is contributed by both the pairs. The NFET pair is assumed to contribute 3 time the PFET par.	$g_{m0,4}$ = 129 µA/V $g_{m7,11}$ = 129 µA/V
		$gm_0 = \sqrt{2 * I_0 * k_n' S_0}$ $gm_7 = \sqrt{2 * I_7 * k_p' S_7}$		$S_{0,4}$ = 60 $S_{7,11}$ = 40
5a	M2, M3, M5, M6	$I_2 = \frac{1}{2}\, k_n'\, S_2 (v_{gs2} - V_{tn})^2$	v_{gs20} set to 1 V	$S_{2,3,5,6}$ = 12 (Set to 20)
5b	M14, M15	Same as M1 and M8		$S_{14,15}$ = 40

[a] 30 mV is the target hysteresis voltage

A transient analysis of the circuit, with a ramp voltage (5 V to 7 V) applied at the positive input with the other input tied to 6 V, was performed. The current biases for the circuits were both set as 60 µA. The comparator transition points, seen in Fig. 4.21 were measured in terms of offset and hysteresis. The results showed a positive transition at 6.007 and a negative transition at 5.977 V. To make the transitions more towards the center of the ramp, i.e. 6 V, certain modifications

were made. These modifications mainly dealt with sizing the transistors to either improve the performance slightly or provide ease for layout. These modifications include

- M16-M19 were doubled in size to 120 to speed up the cross-couple stage while M21-22 were increased from 60 to 80 to provide a better common centroid layout.
- Resizing of the FETs in pre-amplification stage to provide more headroom – M9 and M12 were increased from 30 to 40, M0 and M14 were increased from 60 to 80, and M7 and M11 were increased from 40 to 60.
- To add more balance to the transition points M29 was changed to 20.
- The current biases were increased from 60 µA to 80 µA for faster switching.

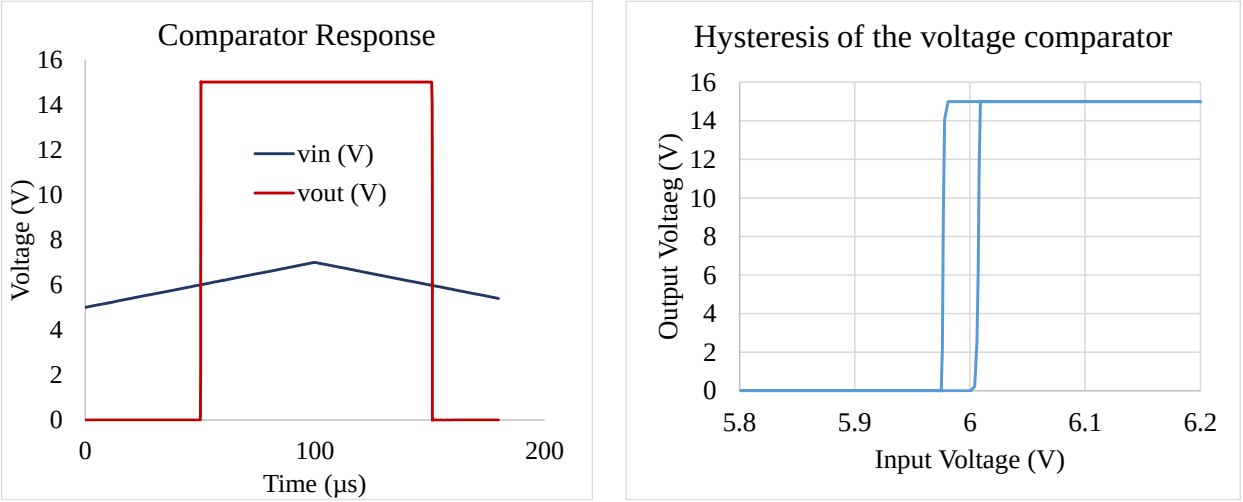


Fig. 4.21. First pass simulation of comparator with calculated values.

Fig. 4.21 shows the first pass simulation of the comparator. As can be seen from the graph, the hysteresis is very close to 30 mV, the desired value. The rise and fall time of the comparator were also close to the desired 50 ns mark. The simulation results for the modified comparator are show in the next section.

4.3.2.3 Comparator Simulation Results over Models and Temperature

The room temperature transient simulation of the comparator with a ramp input is shown in Fig. 4.22. This simulation was carried out with typical models. As can be seen, the comparator's offset performance has improved with the modifications.

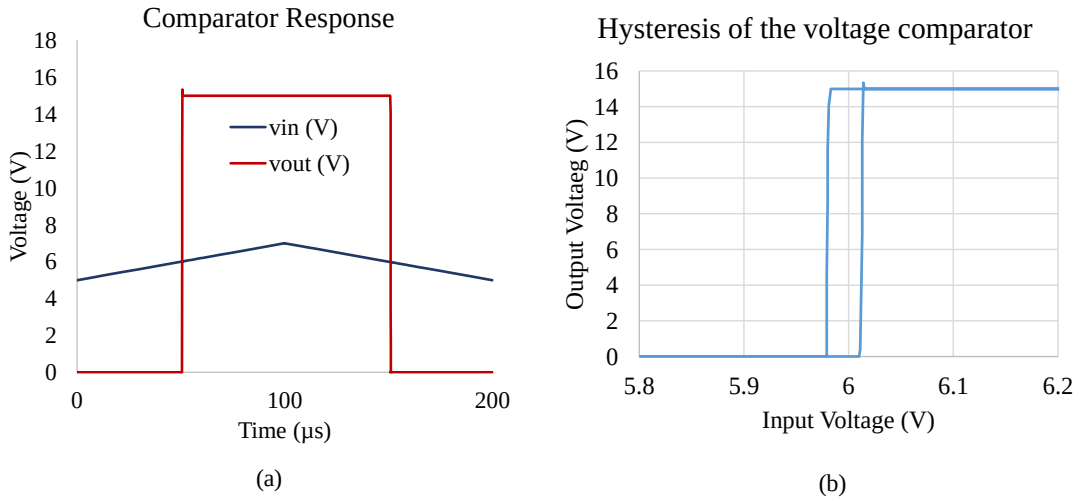


Fig. 4.22. Comparator simulation results with modified schematic.

The comparator propagation delays over temperature and models are shown in Fig. 4.23.

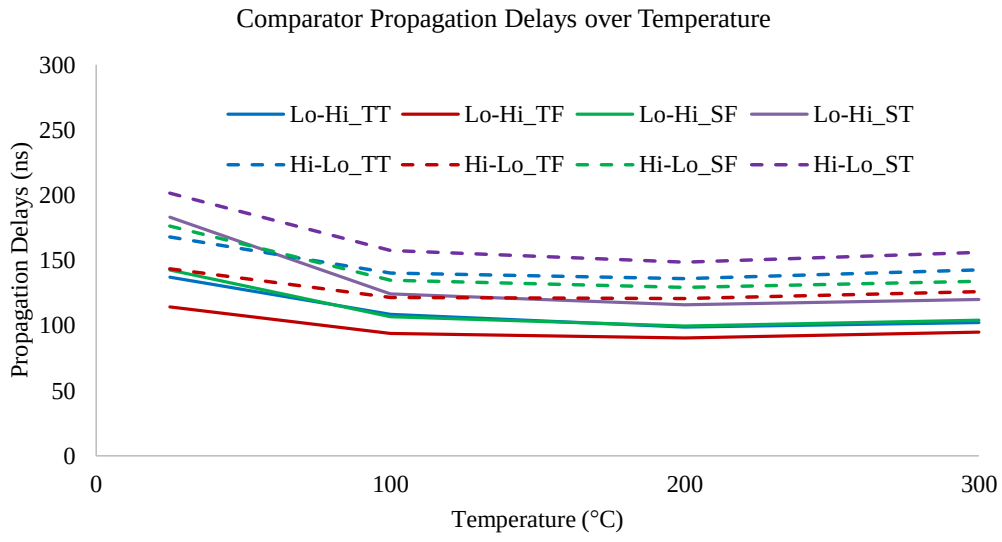


Fig. 4.23. Propagation delays of the comparator

The propagation delay curve shows that the maximum delay is for the slowest model available (ST) at room temperature. The delays, both low to high and high to low, decrease with temperature as the FETs get faster. A similar transient characteristic can be observed in the case of the rise and fall times, as seen in Fig. 4.24.

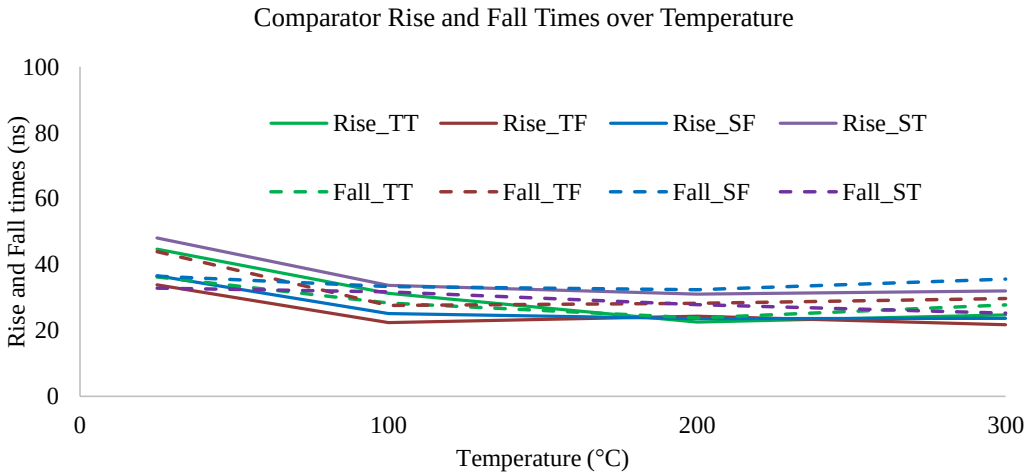


Fig. 4.24. Rise and fall times from the comparator simulation.

The rise and fall times decrease with temperature and are under the design specification of 50 ns for all models over the full temperature range.

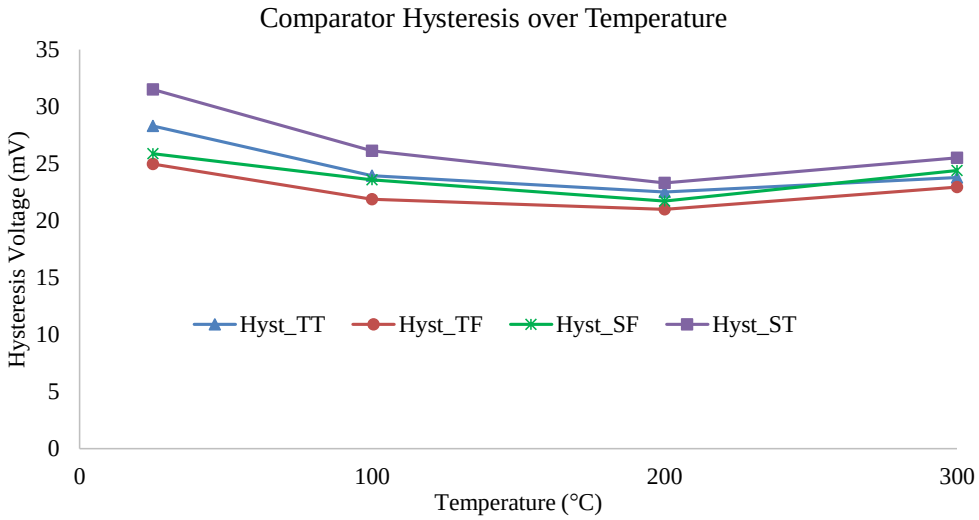


Fig. 4.25. Hysteresis of the comparator for different models over temperature.

The hysteresis values of the comparator for the four different models over the full temperature range are shown in Fig. 4.25. As the temperature increases, the FETs become faster and the resulting hysteresis decreases. The hysteresis is, however, never over 31 mV or under 22 mV, thus still being over the 1 LSB of the data converter.

4.3.3 The Current Comparator

The current comparator is the voltage comparator without the pre-amplification stage. Hence, the design was not changed for the current comparator. The results from the simulations that measure the performance of the current comparator are shown in this section. The current comparator simulation results seen in Fig. 4.26 shows the input current differential going from -0.5 to 0.5 µA. The DC current was set to 4 µA for this simulation. The offset and hysteresis over models and temperatures are shown in Fig. 4.27, the rise and fall times are shown in Fig. 4.28, and the propagation delays of the current comparator are shown in Fig. 4.29.

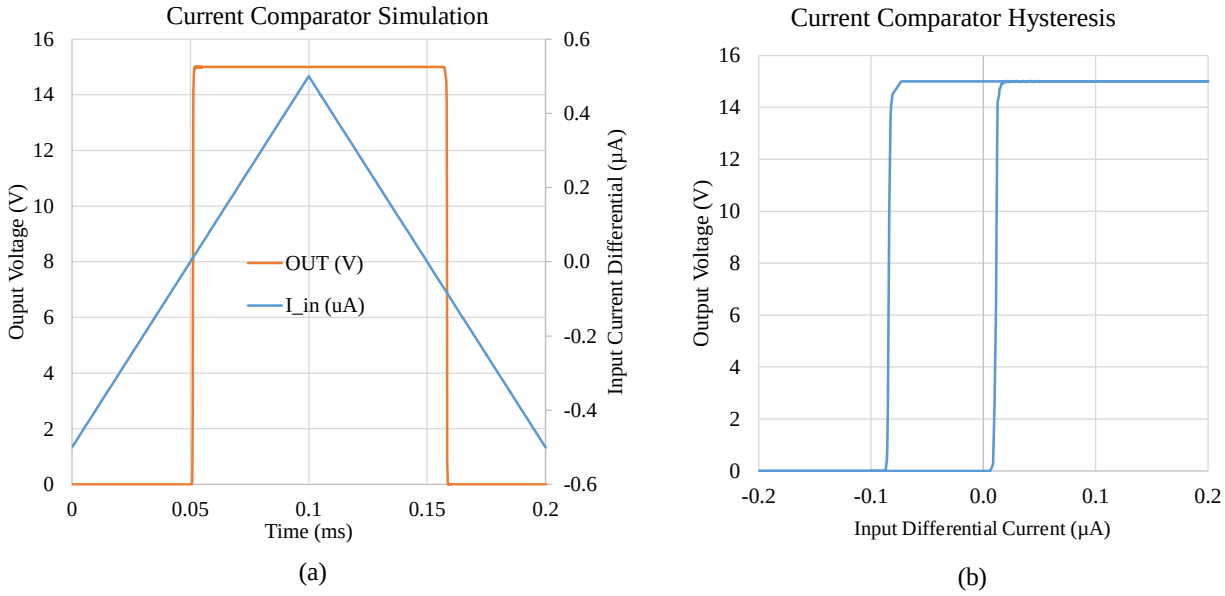


Fig. 4.26. Current comparator simulation at room temperature with TT models.

The current comparator shows a hysteresis of around 90 nA with a bias current of 60 µA, as seen in Fig. 4.26. The comparator also has a built in offset of around -40 nA. The hysteresis value can be reduced by using a higher bias current (80 µA) as is the case in Fig. 4.27.

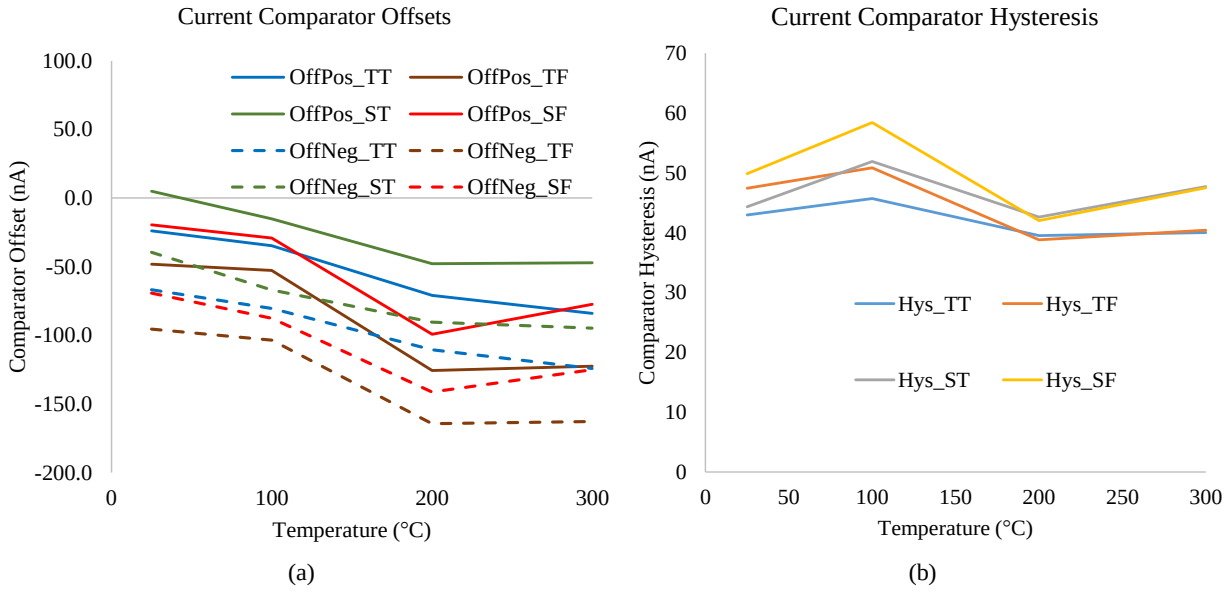


Fig. 4.27. Current comparator results for (a) Offset and (b) Hysteresis.

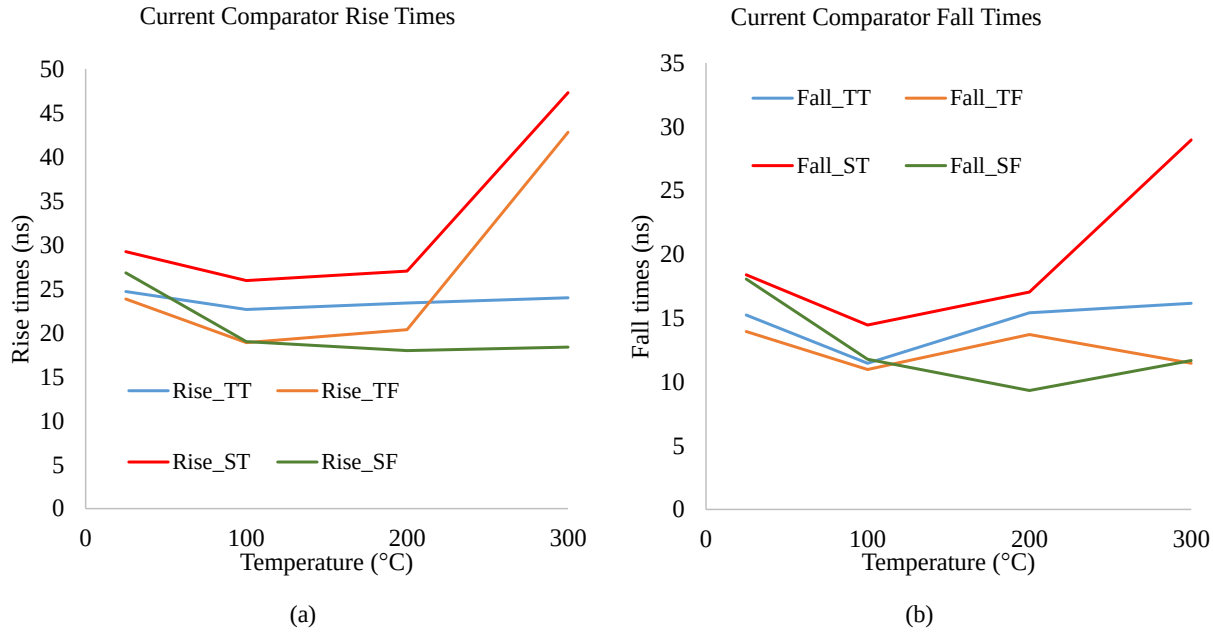


Fig. 4.28. Current comparator transition times - (a) Rise times and (b) Fall times.

The simulation results in Fig. 4.28, show that the built-in offset tends to go more negative over temperature, but is never below -125 to – 130 nA. While this means there will be some offset error in the results, the typical DC current level for the comparator is assumed to be 10-20 µA, which makes the offset error 1% of the input value. The bias current can be changed to compensate for the offset. The hysteresis of the current comparator decreases to around 40-50 nA and remains pretty consistent over all temperatures and models. The rise and fall time (Fig. 4.28) of the circuits are slightly lower than the rise and fall times of the voltage comparator and are simulated to be between 30 - 50 ns for the rise time, and 10 – 30 ns for the fall time.

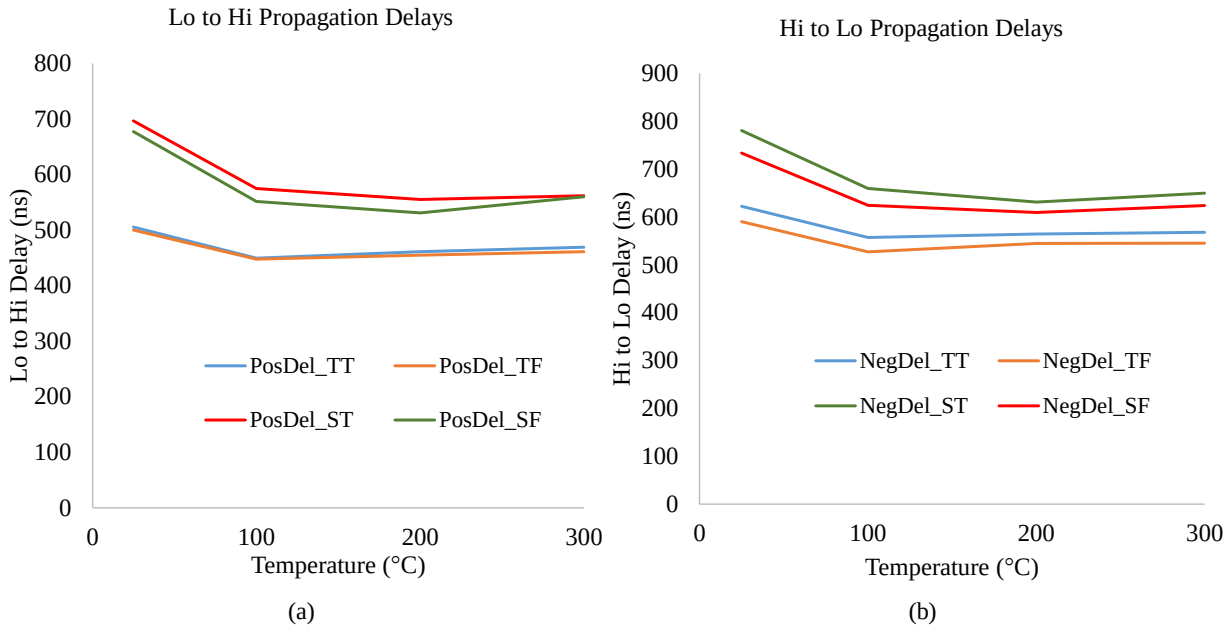


Fig. 4.29. Current comparator propagation delays – (a) Lo to hi, and (b) Hi to lo.

The propagation delays, as seen in Fig. 4.29, are considerably higher than the voltage comparator. This is due to the absence of the pre-amplification stage in the current comparator. However, the values are still under ten times the DC-DC converter switching frequency of 100 kHz. The current comparator is not used in the data converters, hence, the 1 MHz clock requirement is ignored in this particular case.

4.3.4 Propagation Delays of the Comparators

The propagation delay of a comparator is normally dictated by the current of the first amplification stage. The voltage comparator uses an external current to bias the pre-amplification stage and the post decision amplifier, while the current comparator does not have a pre-amplification stage. Hence, the propagation delays of the voltage comparator decreases with the bias current while the propagation delays of the current comparator is unaffected by the bias curernt. As a comparison, the propagation delays of the voltage and current comparators over temperature at different bias currents are given in Table 4.6. As expected, the voltage comparator delays decreases as current goes high while the current comparator delays do not.

Table 4.6. Comparator Propagation Delays for Different Bias Currents

Bias Current	Voltage Comparator Propagation Delay Lo to Hi (ns)				Voltage Comparator Propagation Delay Hi to Lo (ns)			
	25 ℃	100 ℃	200 ℃	300 ℃	25 ℃	100 ℃	200 ℃	300 ℃
80 µA	182	148	136	130	227	191	184	178
90 µA	175	139	127	122	214	178	169	165
100 µA	169	130	120	117	200	166	160	156
110 µA	132	125	116	112	165	157	150	146
	Current Comparator Propagation Delay Lo to Hi (ns)				Current Comparator Propagation Delay Lo to Hi (ns)			
	25 ℃	100 ℃	200 ℃	300 ℃	25 ℃	100 ℃	200 ℃	300 ℃
80 µA	510	451	462	471	625	566	569	572
90 µA	505	450	461	469	622	557	565	568
100 µA	503	446	460	467	617	553	555	565
110 µA	511	447	459	466	611	550	547	555

4.4 Data Converters

The design and simulation results of the 8-bit digital-to-analog and analog-to-digital converters are described in this section [81]. The topologies for both the converters are standard ones, and the converters use circuits, e.g. the comparator and the OTA, that have already been described in the previous section. The SAR ADC uses the R-2R DAC as well. The only other circuit used for the ADC is the digital ADC controller that was developed by Landon Caley.

4.4.1 8-bit R-2R DAC

The 8-bit R-2R DAC schematic is shown in Fig. 4.30 [81]. The input bits are inverted to create complementary gate signals by the row of inverters at the top. Each bit determines whether the node would be connected to the full scale voltage, V_{REF} or ground (VSS).

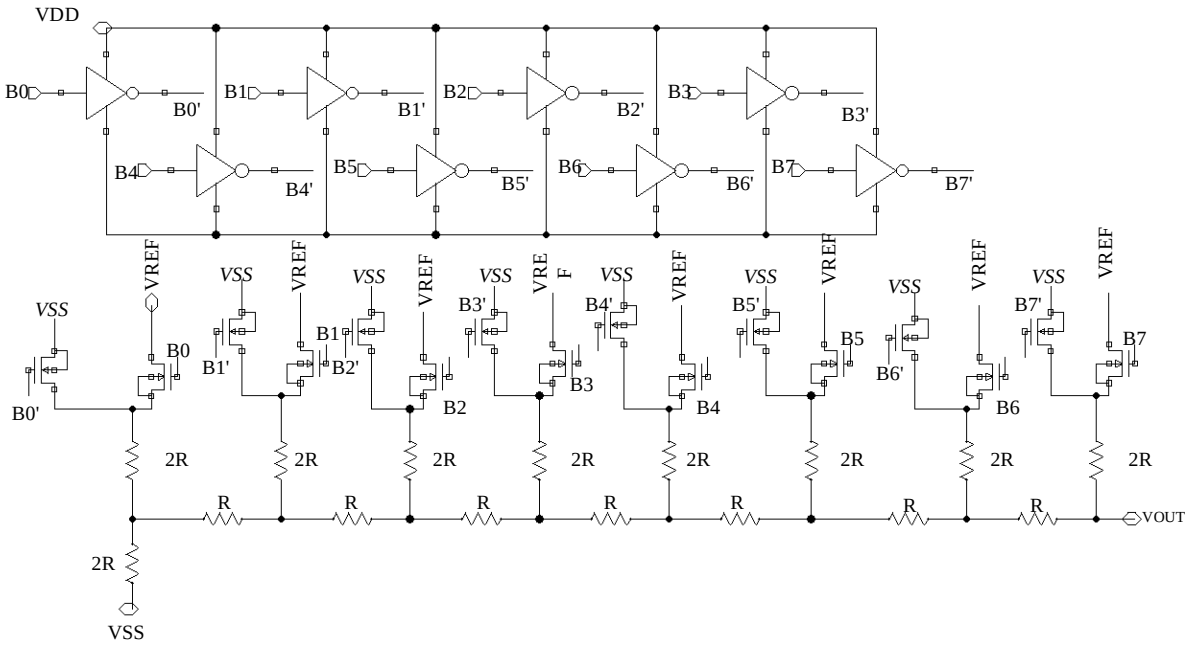


Fig. 4.30. 8-bit R-2R DAC schematic.

The FETs used in this DAC are all NFETs. The NFET was chosen as the switching FET due to its low threshold voltage and the relative low full scale range (5 V) to the power supply (15

V). The sizes of the NFETs connecting a particular node to ground were somewhat smaller because the source of these FETs will always be connected at 0 V. Hence, the FET can be switched at the full gate drive strength. These FETs were sized as 20 µm / 1.2 µm with 8 fingers.

The NFET switches connecting to V_{REF} should see, ideally, a source voltage as high as VREF. Hence, these FETs were sized larger to compensate for the loss of gate drive strength due to body effects. These switches used 12 fingers with the same dimension size per finger.

The maximum current through the DAC comes out to be V_{REF}/R, where R is the unit resistance. Setting a maximum current value 250 µA for the DAC itself, the value for R was found to be 20 kΩ. The inverter used to generate the complementary gate signals was the 3x inverter (3X of an inverter with a 12 µm/1.2 µm PFET and a 4 µm/1.2 µm NFET). The low input common mode OTA described in section 4.3.1 is used in the voltage-follower buffer mode at the output of the DAC to drive system loads. The DAC conversion simulation over the full input code range of 0 to 255 with TT models is shown in Fig. 4.31 (25 °C) and Fig. 4.32 (300 °C).

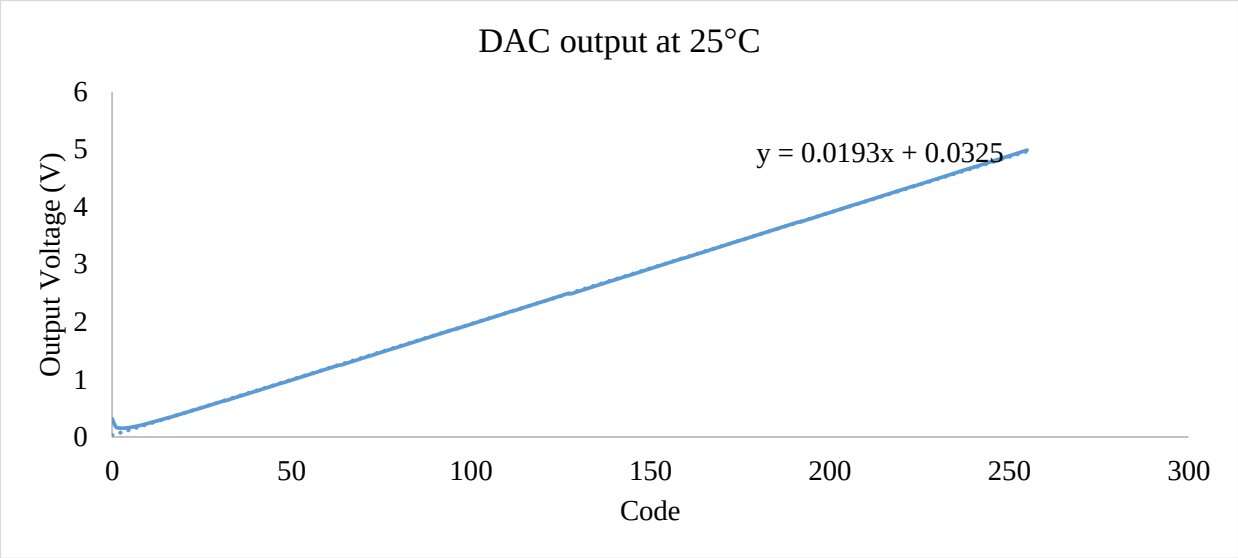


Fig. 4.31. 8-bit DAC simulation for TT models at room 25 °C.

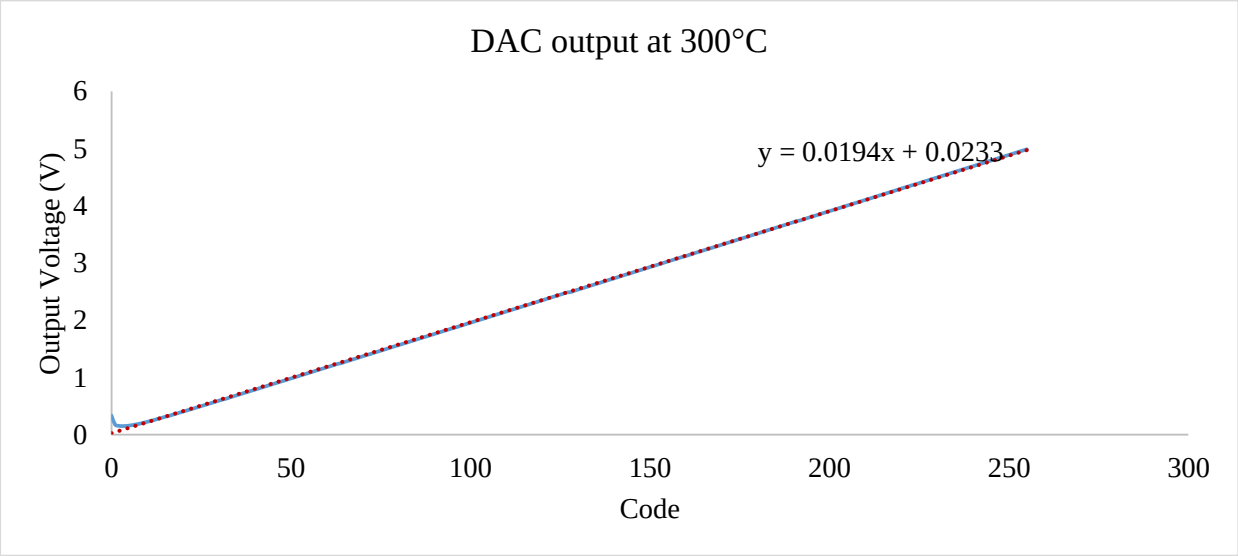


Fig. 4.32. 8-bit DAC simulation for TT models at 300 °C.

The blue solid line on the graphs show the output of DAC, while the dotted line is the trend line of the DAC. The trend line is like an ideal DAC curve. The output of the DAC is limited at the lower end due to the non-zero minimum output voltage of the OTA. Hence, the DAC output is limited at the lower end of the code spectrum. The differential and integral non-linearity errors are very high at the lower end. The DNL and INL graphs for the TT models at 300 °C are shown in Fig. 4.33.

The DNL for both temperatures start at around -9 to -8 LSB before quickly coming to reasonable levels (less than -1 LSB) around the input code of 10 which corresponds to an output of 0.2 V. Given that the minimum output voltage for the OTA was measured to be around 0.13 V over all temperatures, such a behavior should be expected.

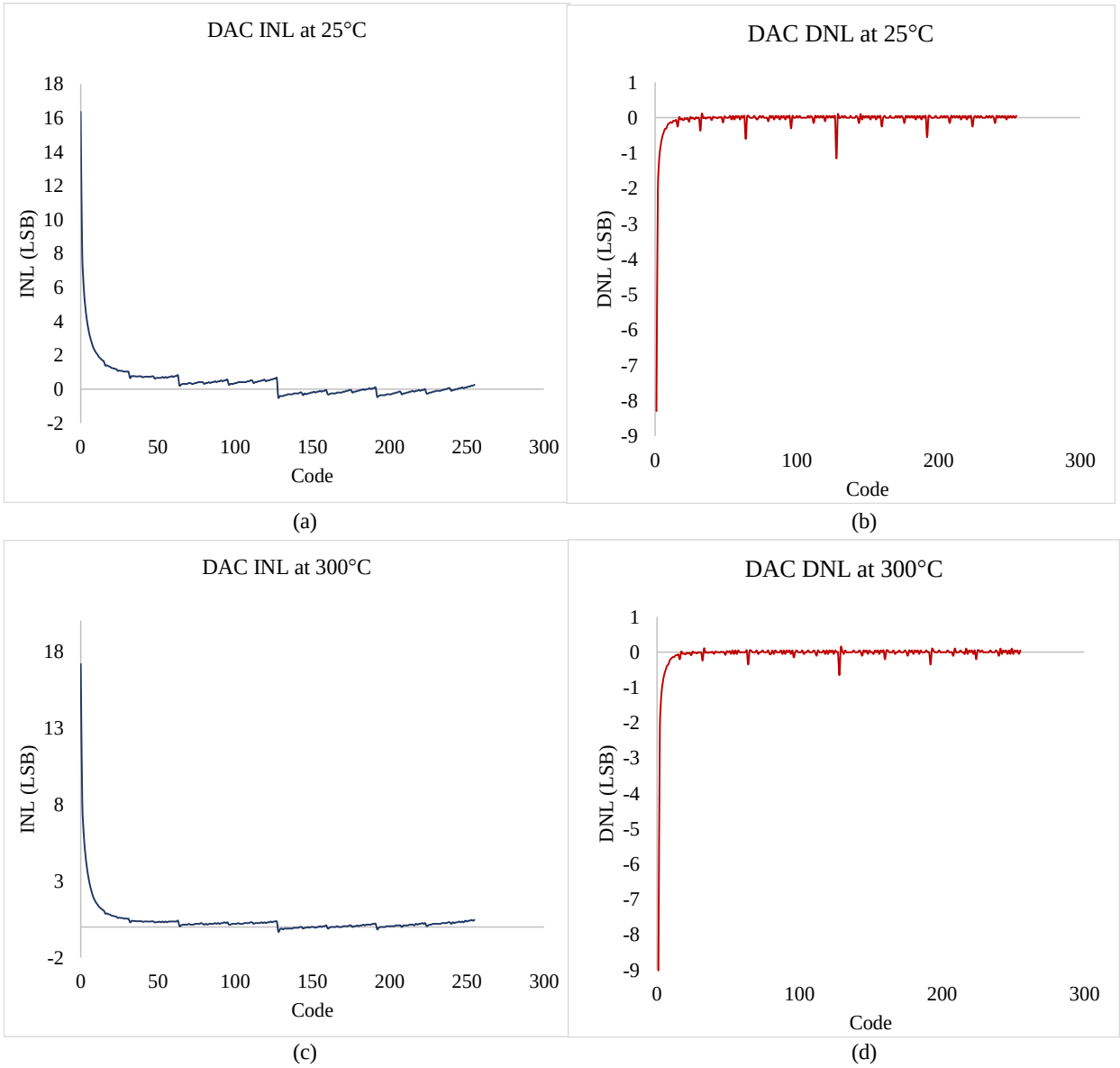


Fig. 4.33. Non linearity errors for TT models (a) INL at 25 °C, (b) DNL at 25 °C, (c) INL at 300 °C, and (d) DNL at 300 °C.

As can be seen from the graph, the maximum absolute error for the DNL occurs at a negative value while for the INL it occurs at a positive value. Hence, the maximum value of the INL and the minimum value of the DNL represent the maximum error for each case. These values, for all temperature and simulated with TT and TF models, are given in Table 4.7. The calculations

for the DNL and INL have been done by ignoring input codes up to 10 (corresponding to an output voltage of 0.2 V), thus ignoring the output limited portion of the DAC.

Table 4.7. Minimum DNL and Maximum INL of the DAC over Models and Temperatures

Models	Maximum INL (LSB)				Minimum DNL (LSB)			
	25 °C	100 °C	200 °C	300 °C	25 °C	100 °C	200 °C	300 °C
TT	2.3	2.3	1.8	1.99	-1.15	-0.85	-0.75	-0.65
TF	2.41	2.42	1.79	1.74	-1.05	-0.85	-0.7	-0.55

If the buffer OTA is removed from the DAC and the output is taken from the resistor divider node, the DAC does not suffer from the minimum voltage limitation. This in important to note because the ADC uses the DAC without the buffer and hence, if the DAC without the buffer does not suffer from the lower end limitation, the ADC can potentially convert low output voltages. The full DAC conversion with TT models at 25 °C is shown in Fig. 4.34.

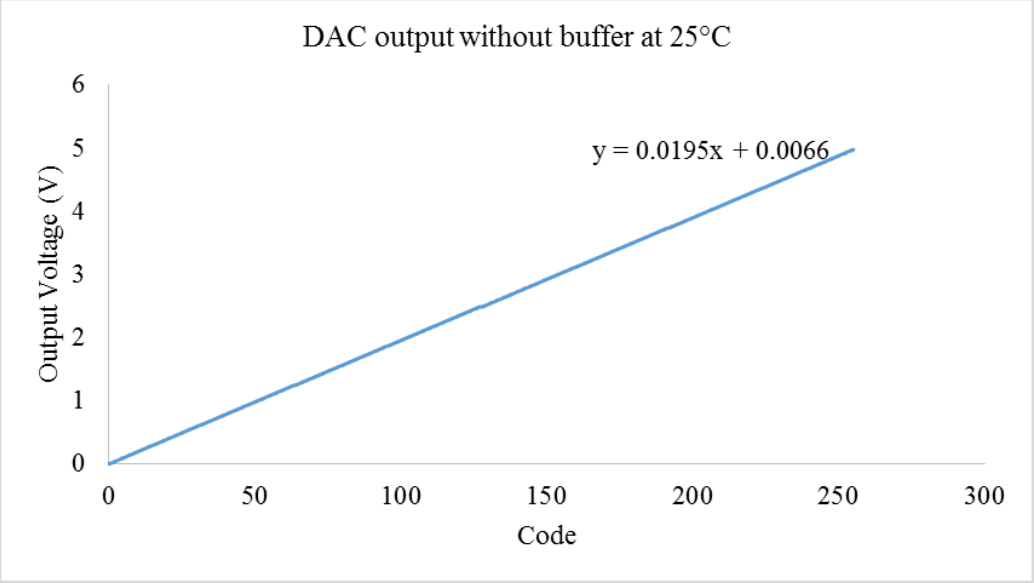


Fig. 4.34. Full conversion of DAC without buffer at 25 °C (TT models).

The resultant maximum INL of this conversion is 0.6 LSB, and the minimum DNL is -1.05 LSB.

4.4.2 8-bit Successive Approximation Register ADC

The 8-bit SAR ADC uses two components already described, the voltage comparator and the 8-bit R-2R DAC. The SAR ADC functions based upon the principles of a binary search, where the desired value is searched by halving the search area during each clock cycle. The schematic of the SAR DAC is shown in Fig. 4.35 [81].

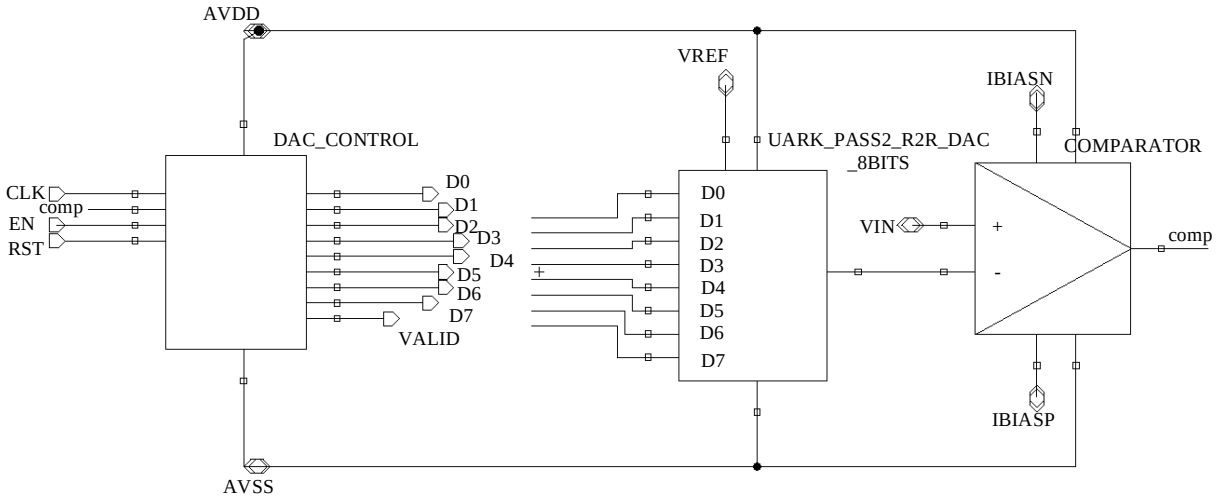


Fig. 4.35. Schematic of the 8-bit SAR ADC.

The digital DAC_CONTROL circuit initially sets all the bits to 0 when RST is set to high. RST is then set to low and the controller is turned on by the signal EN. The controller initially sets the MSB, D7 to high, and the rest of the bits to low. These bits are connected to the 8-bit DAC, which should generate an output that is half the full scale voltage. If the input voltage is higher than the DAC output, the comparator returns a high output. The controller then sets D7 = 1, and changes the next bit (D6) to 1. If not, the controller sets D7 = 0 and changes the next bit (D6) to 1.

Thus, at the end of every cycle the controller changes the next bit to 1, and decides whether to keep the previous bit at 1 or 0. The basic flowchart of the DAC controller is shown in Fig. 4.36.

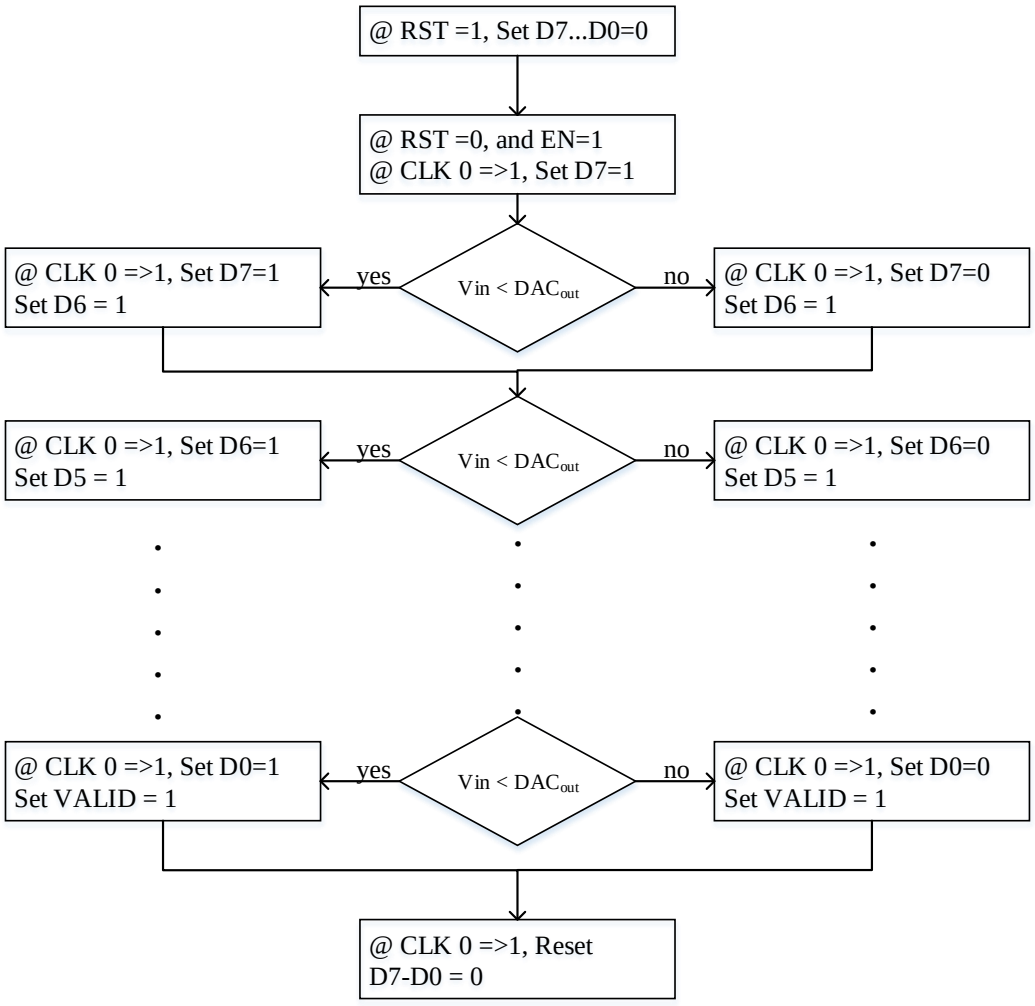


Fig. 4.36. Flowchart of the digital DAC controller.

The full conversion requires ten cycles. The bits are initially set to 1 in a descending order in the first eight cycles. At the ninth cycle, the value of the LSB is set to the appropriate one and a valid signal is sent to system to collect the data. During the tenth cycle the temporary register is cleared of the all the data and the data converter is readied for another conversion. This is also the cycle where the sampling of an accompanying sampling circuit should take place. The Verilog-A code used to generate the digital circuit for this controller can be seen in Appendix B.

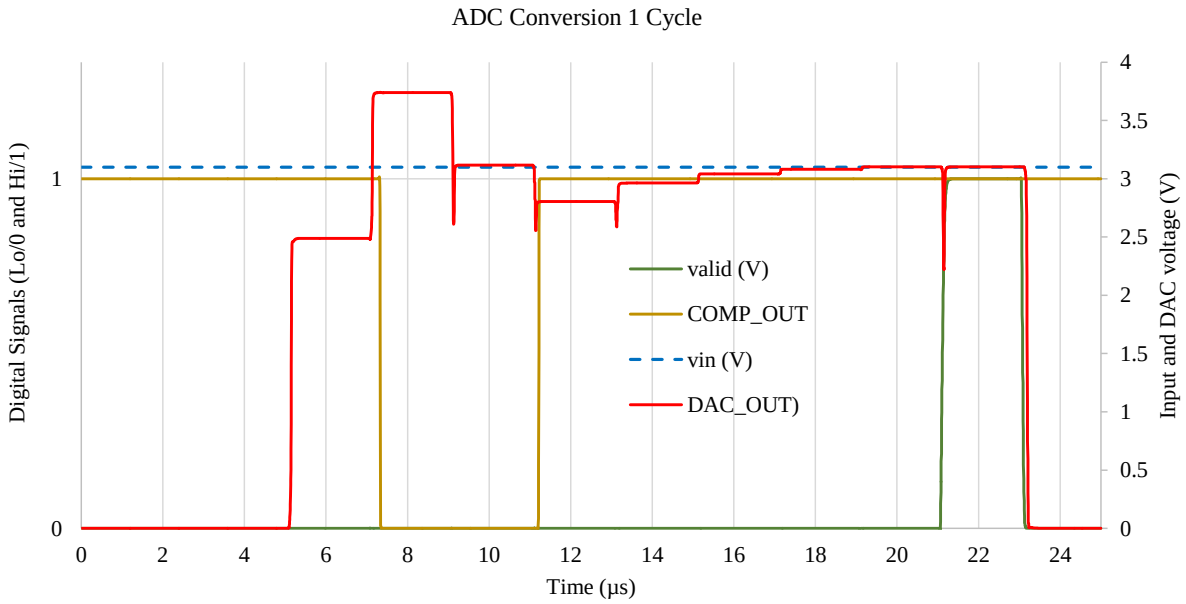


Fig. 4.37. One conversion cycle of ADC.

Fig. 4.37 shows one full conversion cycle of the ADC. The clock speed of this conversion is 500 kHz. The conversion starts at 5 µs in this graph. The MSB, D7 is set to zero and the DAC output goes to 2.5 V. Since the input voltage is set to 3.1 V, the comparator output (yellow) is high. In the next clock pulse, D7 is kept as 1, and D6 is set to 1. This takes the DAC output to 3.75 V and causes the comparator output to go low. The next cycle sees D6 set to 0, and D5 set to 1. The DAC output, now 3.125 V is still higher than the input and the comparator output stays low. This procedure is continued up to when the last bit D0 has been set. Then, the valid signal (green) goes high to signify that the output is ready.

The ADC output over the full range was simulated using a Matlab code that uses the DAC model and the comparator model to generate the ADC output. The simulation was performed in Matlab to find the transition points from code to code. Such a simulation would be very time consuming in the Cadence Virtuoso environment. This simulation is also very useful in

determining the INL and DNL of the ADC. The Matlab codes can be found in Appendix B. The ADC conversion simulation over the full range is shown in Fig. 4.38.

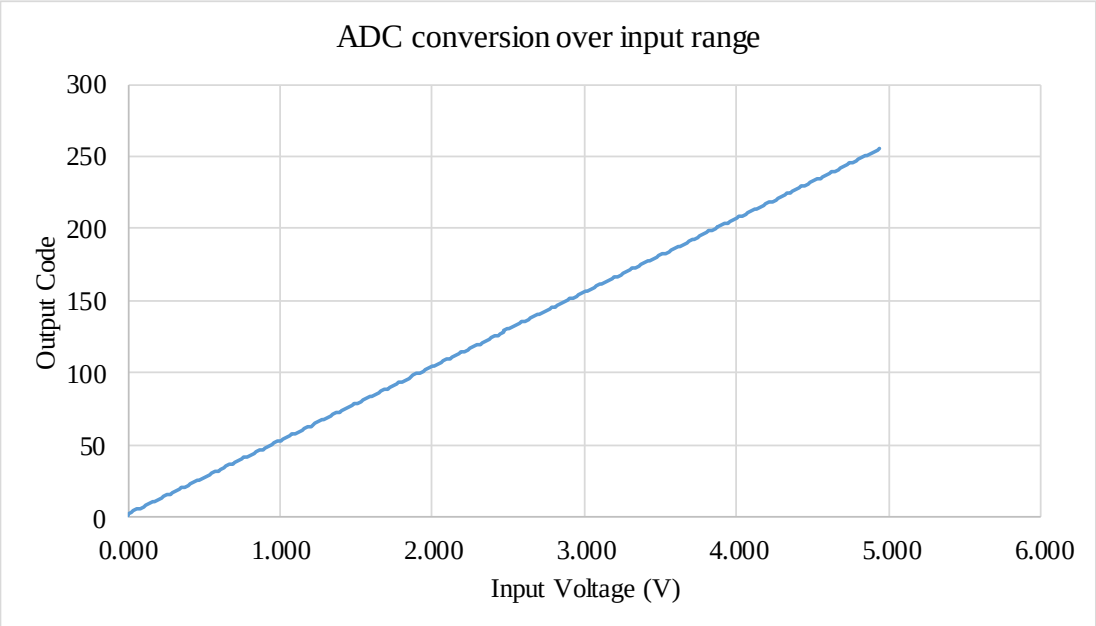


Fig. 4.38. ADC conversion output over full input range.

The non-linearity errors of the ADC are defined by the code's transition points. The output of the ADC shows an offset at the beginning (Fig. 4.38). This contributes to a high INL error for the ADC. By taking the offset error into account, the INL error can be reduced significantly. This can be seen in Fig. 4.39, where the INL without correction ranges from -1 LSB to -3.4 LSB. With offset correction, the INL ranges from 0.6 to -0.8 LSB. Table 4.8 lists the INL with and without offset correction for the TT model at different temperatures.

Table 4.8. ADC INL Values over Temperature with and without Offset Correction

Offset Correction	25 °C	100 °C	200 °C	300 °C
INL (without)	-1.0 to -3.4 LSB	-1.0 to -3.1 LSB	-1.0 to -3.0 LSB	-1.0 to 3.0 LSB
INL (with)	0.6 to -0.8 LSB	0.7 to -0.4 LSB	0.7 to -0.4 LSB	0.8 to -0.2 LSB

Since this is an offset correction, it is not expected to have any bearing on the DNL, as is observed in Fig. 4.39 where the DNLs with and without offset correction are the same.

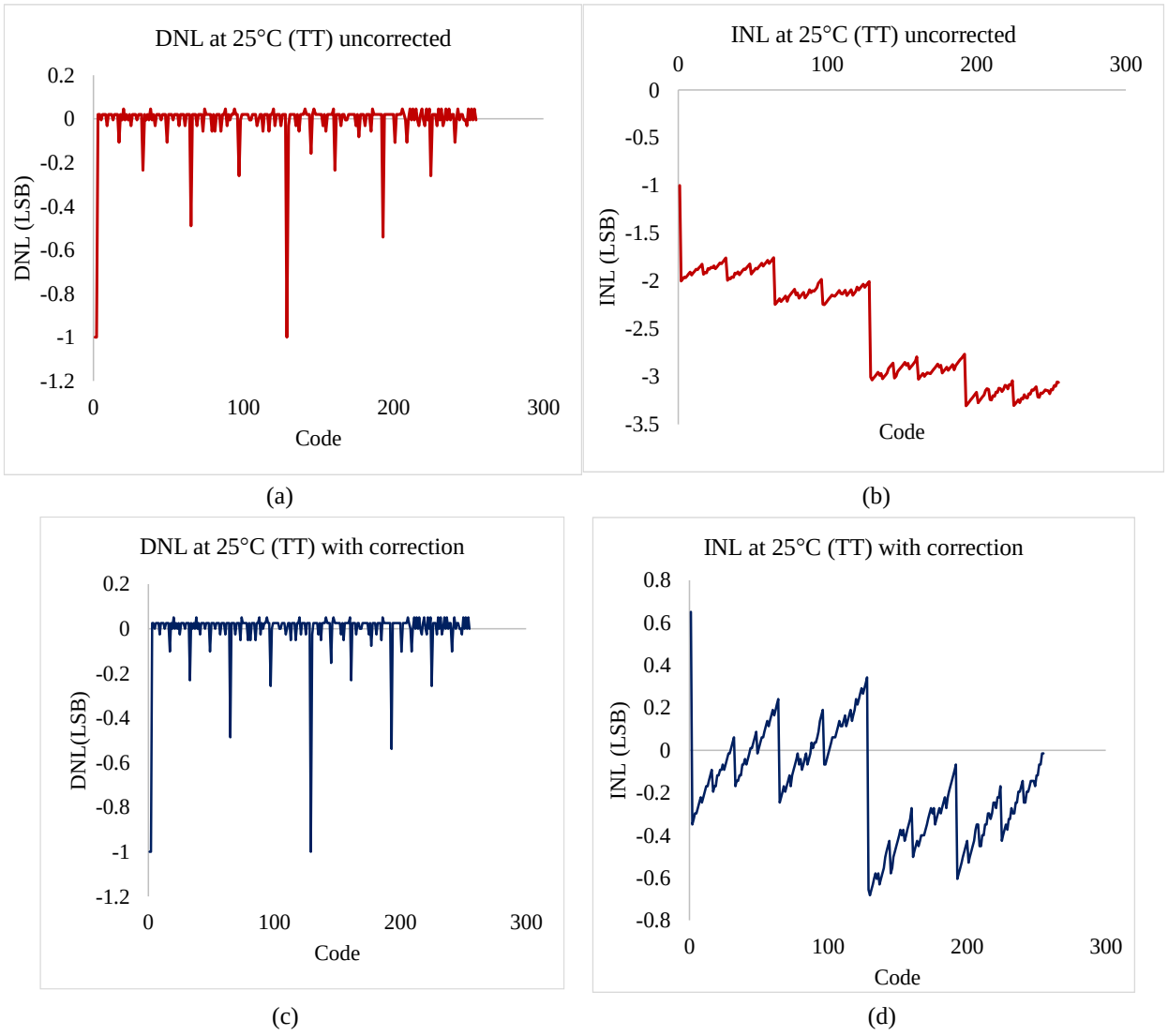


Fig. 4.39. Non linearity errors of the ADC at 25 °C with TT models (a) DNL and (b) INL without offset correction, (c) DNL and (d) with offset correction.

DNL and INL graphs for TT and TF models over the temperature range can be found in Appendix B.

4.5 Flyback Controller System

The DC-DC flyback converter controller using the sliding mode control scheme is the final system under design. As mentioned in section 3.4.3, the sliding mode controller uses normalized values of the system voltage and currents to determine the switching conditions. The sliding mode control for the flyback converter described in [88] was chosen for the integrated chip implementation as part of the solar microinverter project developed under the NSF grant #EPS-1003970. This particular control scheme uses five system voltage and current entities to ensure a more precise boundary condition mode of operation than the traditional sliding mode control. The system voltages are sensed by using a resistor divider network followed by a buffer. The currents were sensed by a hall-effect transducer followed by a buffer. These voltages and currents, their corresponding system variables as well as their expected sensor output voltages are shown in Table 4.9.

Table 4.9. Flyback DC-DC Converter Entities

DC-DC Converter Entity	Control Variable	System Value Range	Sensor Output Range
Solar Panel Input Voltage	V_{CC} / v_{ccn}	0 – 37 V	0 – 5 V
Converter Output Voltage	V_{OUT} / v_{on}	0 – 222 V	0 – 5 V
Primary Current	I_{PRM} / i_{pn}, i_{mn}	0 – 30 A	2.5 – 4.5 V
Secondary Current	I_{SEC} / i_{sn}, i_{mn}	0 – 30 A	2.5 – 4.5 V
Output Current	I_{OUT} / i_{on}	0 – 30 A	2.5 – 4.5 V

The two major passive components in the system are the pulse transformer (6:1 turn ratio) inductance, L_m and output capacitance, C_o.

4.5.1 Flyback Controller

As has been mentioned in section 3.4.4, the flyback DC-DC converter using the sliding mode control works with normalized values of the system variables. In the case of the analog controller developed in this project, these normalized values are generated in terms of current. A block diagram of the sliding mode controller is shown in Fig. 4.40.

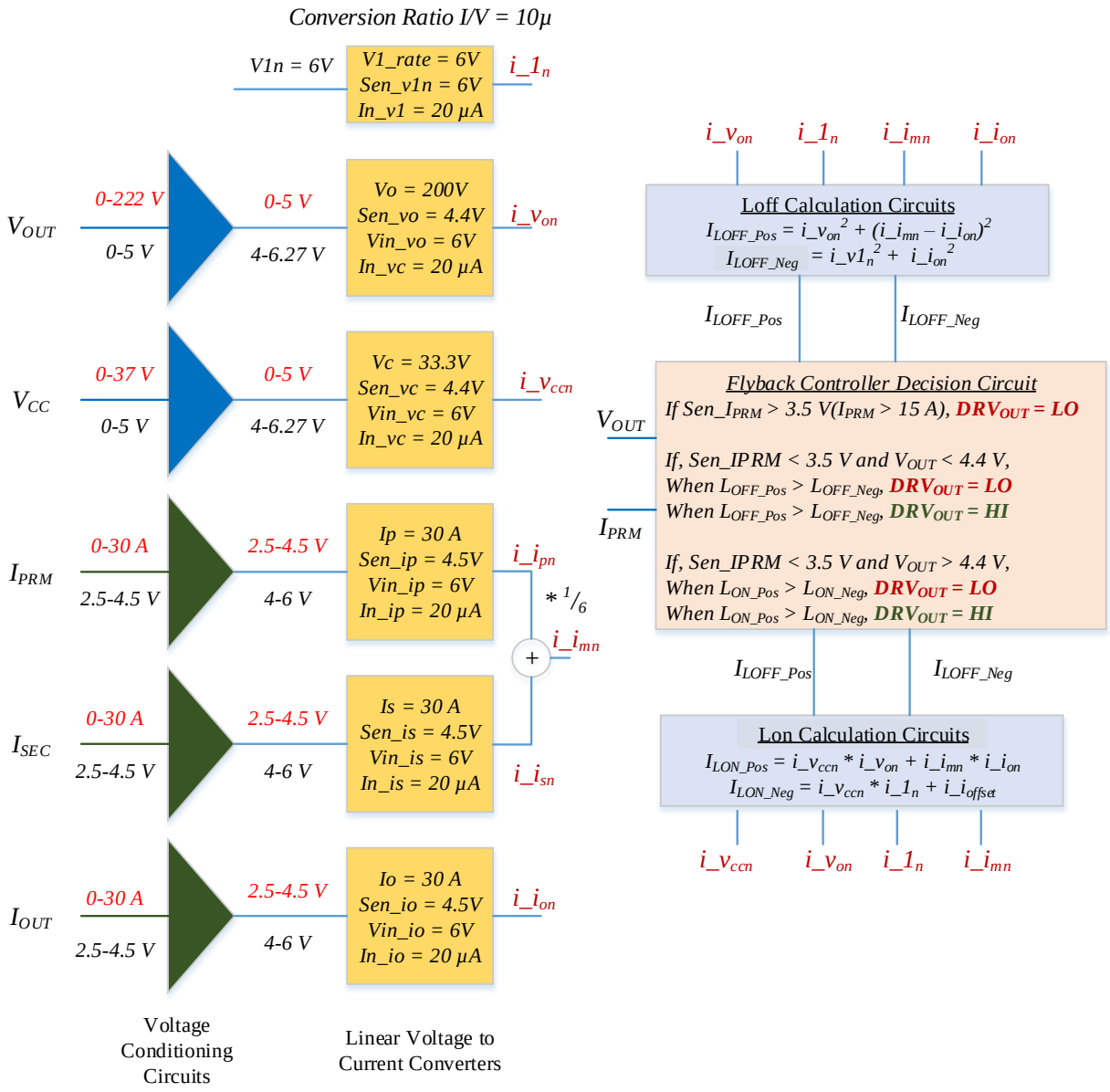


Fig. 4.40. Block diagram of the sliding mode controller with voltage/current ranges.

Fig. 4.40 shows the signal flow and controller algorithm of the sliding mode controller. The outputs of the current sensor are being fed into the voltage conditioning circuits (triangular shaped – blue for output voltage conditioning, and green for output current conditioning). The sensor output voltages are converted into suitable dynamic ranges to be fed into the linear voltage to current converters (square in yellow). The outputs of the V-to-I converter are then sent to the two mathematical circuits – the LOFF calculation circuit that squares the currents and generates the L_{OFF_Pos} and L_{OFF_Neg} currents, and the LON calculation circuit that multiplies the appropriate currents to generate the L_{ON_Pos} and L_{ON_Neg} currents. These currents are then used to determine, depending on the values of V_{OUT} and I_{PRM} whether to turn the power FET on or off. Before circuit schematics and simulation results are shown, each block's operation and the choice for the current and voltage ranges for each of the blocks are described briefly in the following sections.

4.5.1.1 The Voltage Conditioning Circuits

The outputs from the sensors are fed into the voltage condition circuits on the left. This is the input frontend of the circuits. The voltage conditioning circuits (seen in triangular shapes – blue for system voltages and green for system currents) take the values from the sensors and convert them to suitable ranges for the linear voltage to current converters. The low input common mode OTA developed in section 4.3.1 is used in a non-inverting configuration to implement the voltage condition circuits. The red and black numbers preceding the conditioning blocks refer to the input and output ranges of the sensors, e.g. the input range and output range for the current sensors are 0-30 A and 2.5 – 4.5 V, respectively. The ranges, again red and black, after the conditioning blocks refer to the input (red) and output (black) ranges of the blocks themselves, e.g. the VOUT voltage conditioning block converts the 0 – 5 V input range to a 4 – 6.27 V output

range. The choice for the output voltage range is dictated by the input range of next circuit in the signal chain - the linear voltage to current converters.

4.5.1.2 The Linear Voltage to Current Converters

The linear V-to-I circuit described in 4.2.1 is used in this block to generate currents from the sensor voltages. The desired input range for the linear V-to-I circuit is 4 – 7 V, and the voltage to current conversion ratio is 10 µA/V. The LVIC current representing a normalized value of 1 was chosen to be 20 µA, placing it comfortably in the desired input ranges for the current squaring (0 - 40 µA) and multiplying circuit (0 – 25 µA). This led to the following choices regarding the settings for the voltage conditioning circuits –

- The rated output voltage of the system voltage sensors was chosen to be 4.4 V (corresponding to a system output of 200 V and a solar panel input of 200/6 or 33.3 V). The rated output voltage of the conditioning circuits for V_{OUT} and V_{CC} was chosen to be 6 V. This was done to allow for voltages that were over the rated value. Hence, the V_{OUT} and V_{CC} voltage conditioning circuits transform an input range of 0 – 5 V to an output of 4 – 6.27 V.
- The system currents are not expected to reach the normalized value of 1, hence, no change in the dynamic range was necessary for them. However, the signal voltages needed to be shifted from 2.5 – 4.5 V to 4 – 6 V to support the input range of the linear V-to-I converter. This meant that a measured current range of 0 - 30 A corresponds to a 4 – 6 V range on the output of the conditioning circuits for I_{OUT}, I_{PRM} and I_{SEC}.
- A DC reference voltage of 6 V was provided to a sixth linear V-to-I circuit to generate the current denoting the normalized value of 1 for Eqs. (3.19) and (3.20).

- The magnetizing current is determined as the summation of the primary and secondary current, which are exclusive in terms of operating cycles, and is represented in terms of the secondary by,

$$\boldsymbol{i_i_{mn} = i_i_{sn} + \frac{1}{6} * i_i_{pn}} \quad \textbf{(4.9)}$$

4.5.1.3 The LOFF and LON Calculation Circuits

The governing equations for the flyback sliding mode controllers, given in Eqs. (3.19) and (3.20) are presented here again as a refresher.

$$\boldsymbol{\lambda_{off} = v_{on}^2 + (i_{mn} - i_{on})^2 - 1 - i_{on}^2}$$

$$\boldsymbol{\lambda_{on} = i_{mn} + \frac{v_{ccn}}{i_{on}} v_{on} - \frac{v_{ccn}}{i_{on}}}$$

As described in section 3.4.4, the following modifications are necessary in the equations to balance the dimensions of the variable on the right side of the equations, if the variables are to be replaced by normalized current values.

- Change the 1 in Eq. (3.19) to 1^2
- Multiply 1 with the last term in Eq. (3.20)

Since the controller output is determined by whether the values for λ_{off} and λ_{on} are greater or less than zero, Eq. (3.20) can be rewritten to eliminate the division by i_{on}. With this modification and the variables now changed into normalized current values, the governing equations can be rewritten as,

$$\boldsymbol{\lambda_{off} = i_v_{on}^2 + (i_i_{mn} - i_i_{on})^2 - i_1_n^2 - i_i_{on}^2} \quad (4.10)$$

$$\boldsymbol{\lambda'_{on} = \lambda_{on} * i_i_{on} = i_i_{mn} * i_i_{on} + i_v_{ccn} * i_v_{on} - i_v_{ccn} * i_1_n - i_i_{offset}} \quad (4.11)$$

where i_i_{offset} is the compensation current to account for offset generated from the output of the multiplier circuits.

The L_{OFF} calculation block consists of four current squaring circuits, described in section 4.2.2, that convert the normalized linear currents into squared current outputs. The L_{ON} calculation block includes the current multiplier circuits, described in 4.2.3, for the terms in Eq. (4.10), as well as a fourth multiplier circuit with zero input currents to generate the offset compensation current.

4.5.1.4 The Flyback Controller Decision Circuit

The positive and negative variables in the Eq. (4.9) are bundled separately to form the currents L_{OFF_Pos} and L_{OFF_Neg}. Similarly, the currents L_{OFF_Pos} and L_{OFF_Neg} are formed from the entities in (4.10). These two pairs of currents are then sent to two current comparators, described in 4.3.3, to implement the gate driver control as described in section 3.4.4 –

- When $V_o < V_{o\text{-}rated}$, if $v_{on}^2 + (i_{mn} - i_{on})^2 < 1_n^2 + i_{on}^2$, turn FET on, else turn FET off.
- When $V_o > V_{o\text{-}rated}$, if $i_{mn} * i_{on} + v_{ccn} * v_{on} < v_{ccn} * 1_n$, turn FET on, else turn FET off.

The V_{OUT} voltage from system output sensor is compared to a fixed voltage of 4.4 V (denoting a normalized value of 1) to determine which current comparator output to choose from in order to drive the power FET. The primary current, I_{PRM}, is limited by turning the FET off to protect the transformer current. The maximum current to be allowed in the transformer was chosen to be 15 A, which corresponds to an output voltage of 3.5 V for the I_{PRM} sensor. The system output state determination and the primary current limitation were done by using the voltage comparator described in 4.3.2.

The following sections discuss the design considerations and simulations of the sub-blocks described briefly in this section.

4.5.2 Flyback Converter Controller Input Frontend

4.5.2.1 The Voltage Level Shifter

The flyback converter controller input frontend circuitry is comprised of the voltage conditioning circuits and the linear voltage to current converter circuits. The voltage conditioning circuit is a non-inverting closed loop amplifier that uses the low input common mode OTA with feedback resistors. The schematic of the circuit is shown in Fig. 4.41.

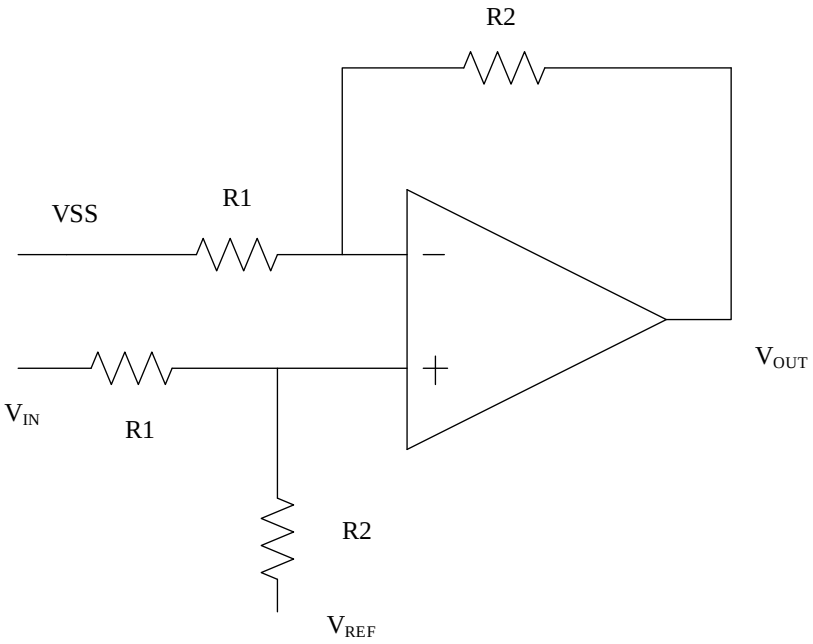


Fig. 4.41. Schematic for the level shifting non-inverting amplifier.

The non-inverting amplifier utilizing the OTA seen in Fig. 4.41 has a reference voltage, V_{REF} that helps set the DC offset voltage of the output. The relationship between the input and output of the circuit is given by the following equation,

$$\boldsymbol{V_{OUT} = V_{IN} * \frac{R2}{R1} + V_{REF}} \tag{4.12}$$

The ratio of *R2/R1* is determined by the ratio of the output voltage range to the input voltage range. V_{REF} is determined by the minimum values of the input and output ranges.

- For the system voltage conditioning circuits, the input voltage range and output voltage are 0 – 5 V and 4 – 6.27 V respectively. Hence, the conversion ratio *R2/R1* is 2.27/5 or 0.45. Since the minimum input voltage of 0 V corresponds to an output voltage of 4 V, the desired V_{REF} is 4 V.
- For the system current conditioning circuits, the input range of 2.5 – 4.5 V is transformed to an output range of 4 – 6 V. Hence, the resistor ratio, *R2/R1* is 2/2 or 1. Considering a minimum input of 2.5 V corresponds to an output voltage of 4 V, the value for V_{REF} is set to 1.5 V.

4.5.2.2 Input Frontend Normalized Values

The complete input frontend block with the major components is shown in Fig. 4.42.

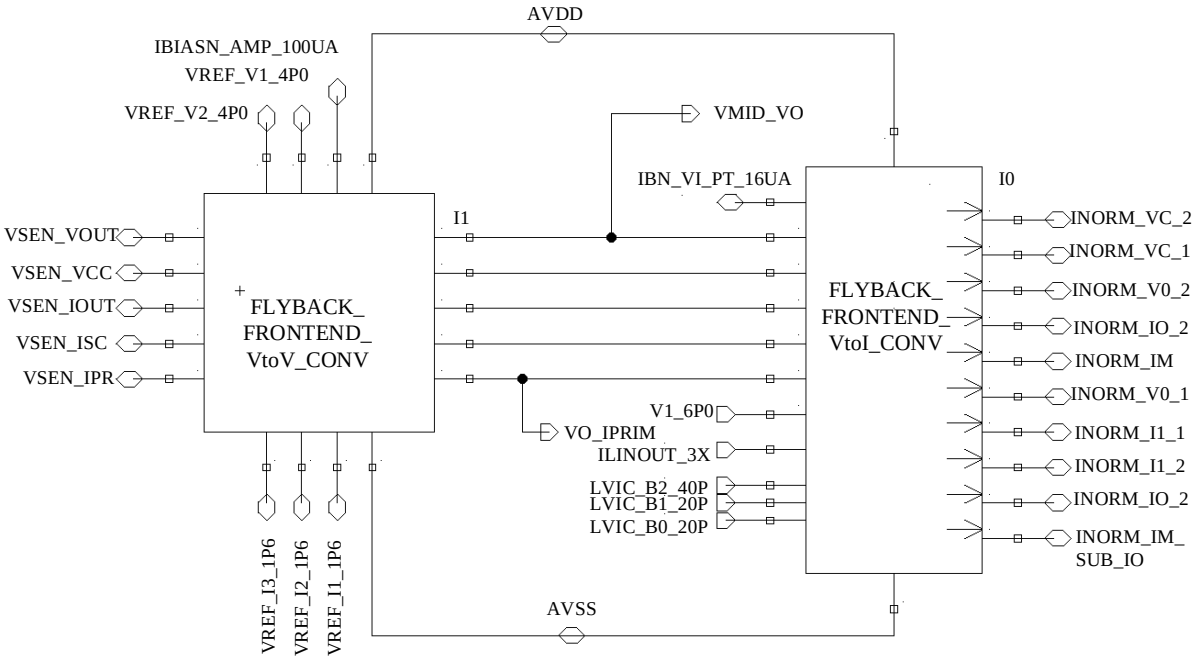


Fig. 4.42. Block diagram and pinouts of the flyback converter input frontend.

The five separate voltage conditioning circuits use five different reference voltages for the different sensor outputs. The OTAs used to implement the non-inverting amplifiers are biased

through an external current source IBIASN_AMP_100UA. The linear voltage to current converters are biased by the bias current pin, IBN_VI_PT_16UA. The current setting bits LVIC_B2_40P, LVIC_B1_20P and LVIC_B0_20P can control the voltage to current conversion ratio. The default setting (noted as 100%) is B2 = 1, B1 = 1 and B0 = 0. The fourth setting pin, ILINOUT_3X is set high when the flyback converter uses a much lower output capacitor.

The current conversion operation for the system voltages is pretty straight forward because the voltage is normalized by the combination of the sensor and voltage conditioning circuits. The linear current conversion for the current sensor outputs are a little different since the normalized current values for i_{mn} and i_{on} are not set as simply as can be done for v_{on} and v_{ccn}. The current conversion ratio to normalize the current is determined the in the following steps.

- The first step is to determine the rated current value. The normalized values of the output and magnetizing currents are given by the Eqs. (3.16) and (3.17). These equations use the natural impedance as the reference impedance. With the inductance, $L_{m,}$ set to 28 µH and the output capacitance, C_o, set as 250 µF, the natural impedance is calculated as 2 Ω from Eq. (3.18).
- The value of the current corresponding to a normalized value of 1 is then calculated as 100 A, by plugging in $V_{o\text{-}rated}$ = 200 V, and Zr = 2 Ω.
- The current sensors along with the conditioning circuits are designed to convert a 0 – 30 A current range to a 4 – 6 V output. Thus, a current measured as 30 A corresponds to a 6 V input to the linear V-to-I converter and an output of 20 µA (equivalent to a normalized value of 1) from it. The ratio between the actual normalized value and the converter normalized value for the currents can then be written as,

$$i_{norm-actual} = \frac{30}{100} * i_{norm-converter}$$

- The controller currents are normalized in reference to the secondary. Hence, the primary side current contributes 1/6th of its value to the magnetizing current due to the 6:1 turns ratio. With this in mind, the primary side current is scaled by a factor of 1/5 while the secondary side currents are scaled by a factor of 6/5. The extra scaling factor changes the ratio between the actual and converter normalized values,

$$\frac{i_{norm-actual}}{i_{norm-converter}} = \frac{30}{100} * \frac{5}{6} = \frac{1}{4}$$

A brief summary of the output range, rated values and the conversion relationships for all the variables in the governing equations is given in Table 4.10.

Table 4.10. Flyback Controller System Variables Normalization Factors

System Entity	Sensor Output Range	Rated Value (Norm = 1)	Normalized value in terms of converter current outputs
Output Voltage	0 – 222 V	200 V	$v_{on} = i_i_{von}$
Panel Voltage	0 – 37 V	33.3 V	$v_{ccn} = i_i_{vccn}$
Output Current	0 – 30 A	100 A	$i_{on} = i_i_{on}$
Magnetizing Current	0 – 30 A	100 A	$i_{mn} = \frac{1}{4} * (i_i_{sn} + \frac{1}{6} * i_i_{pn})$

The expected secondary currents I_{SEC} and I_{OUT} are between 0.5 A (for a 100 W load) and 1.0 A (for a 200 W load) and correspond to inputs of 4.033 V and 4.067 V to the linear V-to-I converter, respectively. This value is situated in the very low end of the input range where the conversion ratio is smaller than usual. Hence, the values for the secondary currents are multiplied

by an additional scaling factor of 2 to compensate for the lower conversion gain. Since the values are all in currents, a network of current mirrors is used to implement the transformation. The current mirror network for the system variables is shown in Fig. 4.43.

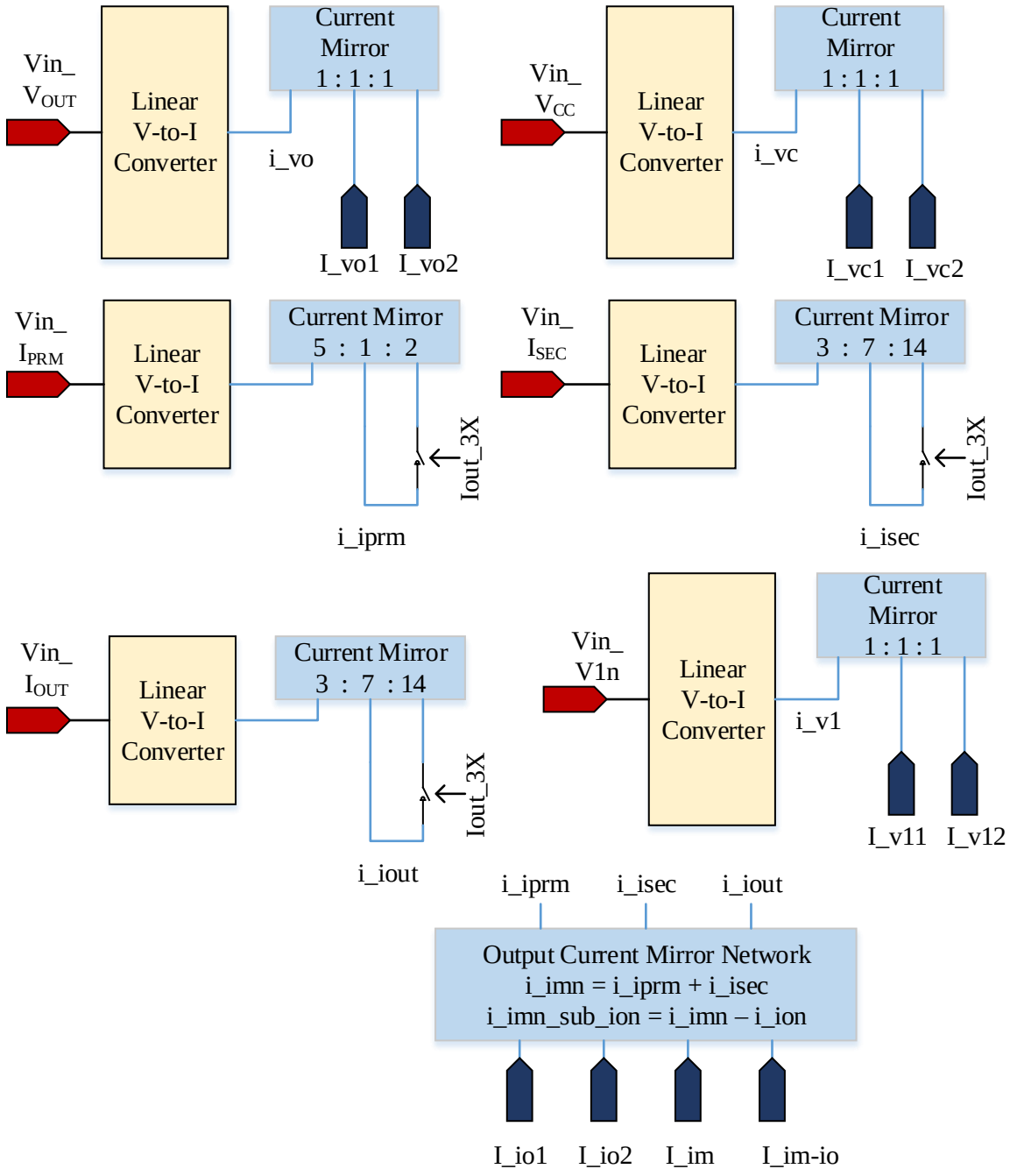
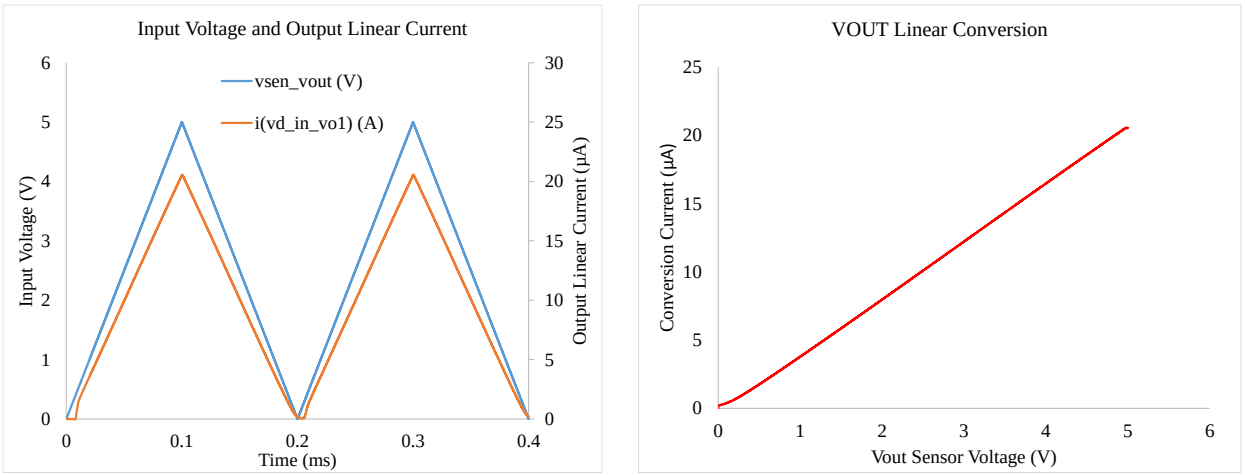


Fig. 4.43. Current mirror network for the input frontend voltage to current converters.

The inputs to the voltage to current converter blocks are the red pins for the five system voltage and current quantities. The three current level setting bits are not shown in the diagram but the switch to multiply the current by 3 times to support a lower output capacitor is shown. The output currents of the normalizing current converters are shown as the blue output pins. All the necessary currents to perform the λ_{off} and λ_{on} calculations are outputs of the circuit.

4.5.2.3 Simulation Results from the Input Frontend

Transient simulations were run for the input frontend where the input to the converter is a ramp triangular input voltage. The simulation results are shown in Fig. 4.44.



(a) (b)

Fig. 4.44. The linear output currents for the Vout sensor (a) Time domain simulation and (b) Output current vs input voltage graph.

The input to the converter is the blue triangular wave at a frequency of 5 kHz in Fig. 4.44 (a). The input ranges from 0 to 5 V and the corresponding current output (orange curve) ranges from 0 to 20 µA. The current value corresponding to a normalized value of 1 is 17.6 µA, instead of the target spec 20 µA. The output current vs input voltage conversion is shown in Fig. 4.44 (b). The simulations were done with TT models at room temperature. Since the performances of the

all the component circuits have been simulated over temperatures and models, the block level simulations with all the models over the full temperature range are not shown here.

The results from the simulation to generate the normalized magnetizing current are shown in Fig. 4.45. The outputs of the primary and secondary side current sensors are the inputs to the circuit. For the purpose of this simulation these signals were provided as triangular waves going from 0 to 5 V. Because of the nature of the conditioning circuits, the linear V-to-I converter only converts voltage to current once the sensor output is over 2.5 V, as is the case seen in Fig. 4.45.

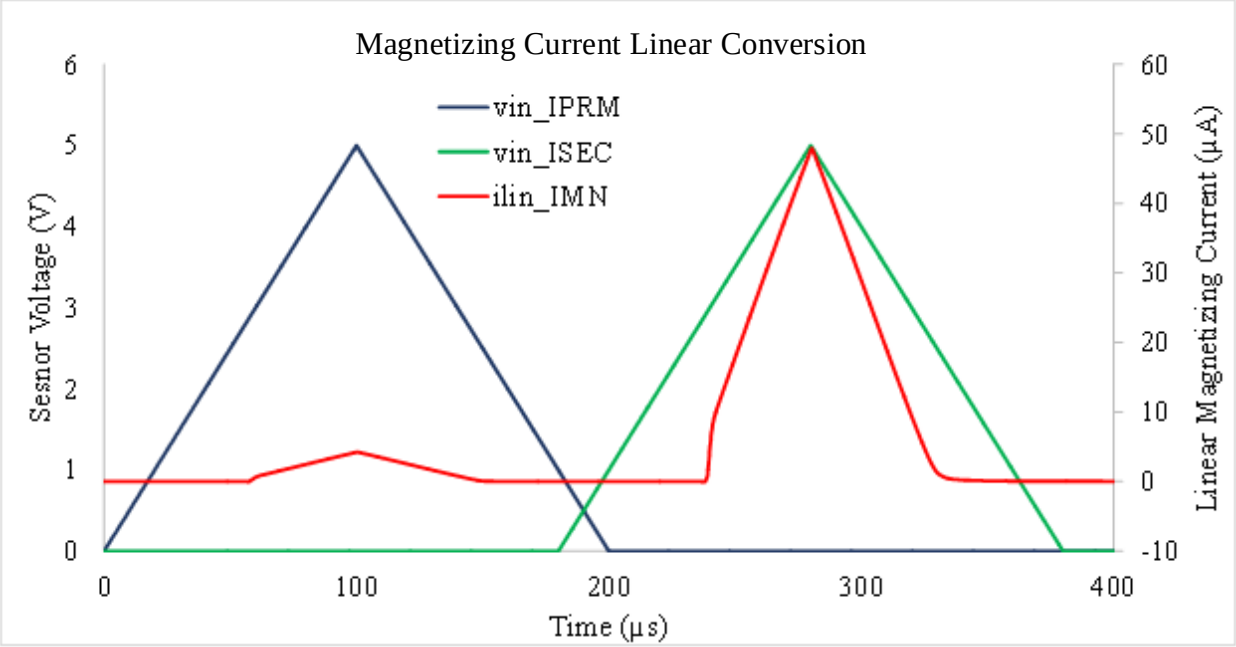


Fig. 4.45. Simulation results for the magnetizing current.

The signals emulating the primary and secondary current sensor are set such as that both of them do not show positive current at the same time. The blue wave denotes the primary current, while the green denotes the secondary current. The red curve is the normalized magnetizing current, i_{mn}. The magnetizing current reaches a peak of 4.2 µA for 5 V as the primary side current

sensor output, *vin_IPRM*. However, due to the scaling factor of 12 associated with the secondary currents, the maximum current reaches 47.5 µA for the same input voltage at *vin_ISEC*.

The simulation results for the other system voltage and current, V_{CC} and I_{OUT}, are exactly the same and hence, are not shown here.

4.5.3 L_{OFF} and L_{ON} Calculation Circuits

The linear current outputs from the input frontend are fed into the current squaring circuits in the L_{OFF} calculation block and the multiplication circuits in the L_{ON} calculation block. Since the input frontend outputs for the system currents are four times the normalized value, after the squaring of the currents, this scaling factor becomes sixteen.

4.5.3.1 L_{OFF} and L_{ON} Calculation Circuit Design and Scaling

The inputs to the LOFF calculation block are the normalized current denoting *von, 1*$_n$, i_{on} and $(i_{mn} - i_{on})$. The current squaring circuit, as discussed previously, has an offset in the output. The following steps were taken in the L_{OFF} calculation block to compensate for the gain error and offset error present in the currents:

- An offset generating current squaring circuit was added to the block. The input to this particular current squaring circuit is zero, hence, the output is only the offset of the circuit. This offset current is then subtracted from each of the four current squaring circuits.
- The outputs of the current squaring circuits for the system voltages were multiplied by three times through a current mirror, while the outputs of the circuits for the system currents were attenuated by a factor of five. Thus, the ratio between the squared values

of the current and voltage normalized values is brought to 16/15. The slight error is ignored due to the relatively low value of the currents denoting i_{on}^2 and $(i_{mn} - i_{on})^2$.

- The reason for multiplying the normalized current values of the system voltages, i_{von} and i_{1n}, was to set the current values for a normalized value of 1 to be around 20 µA, instead of 6 – 7 µA, as would be the case for a current squaring circuit with an input of 7 µA. The choice of 20 µA was determined by the current comparator which had a desired common mode range of 10 – 30 µA.

The block schematic for the LOFF calculation circuit is shown in Fig. 4.46. The current amplification and subtraction are achieved through current mirrors and the FETs used to achieve their implementations are not shown here.

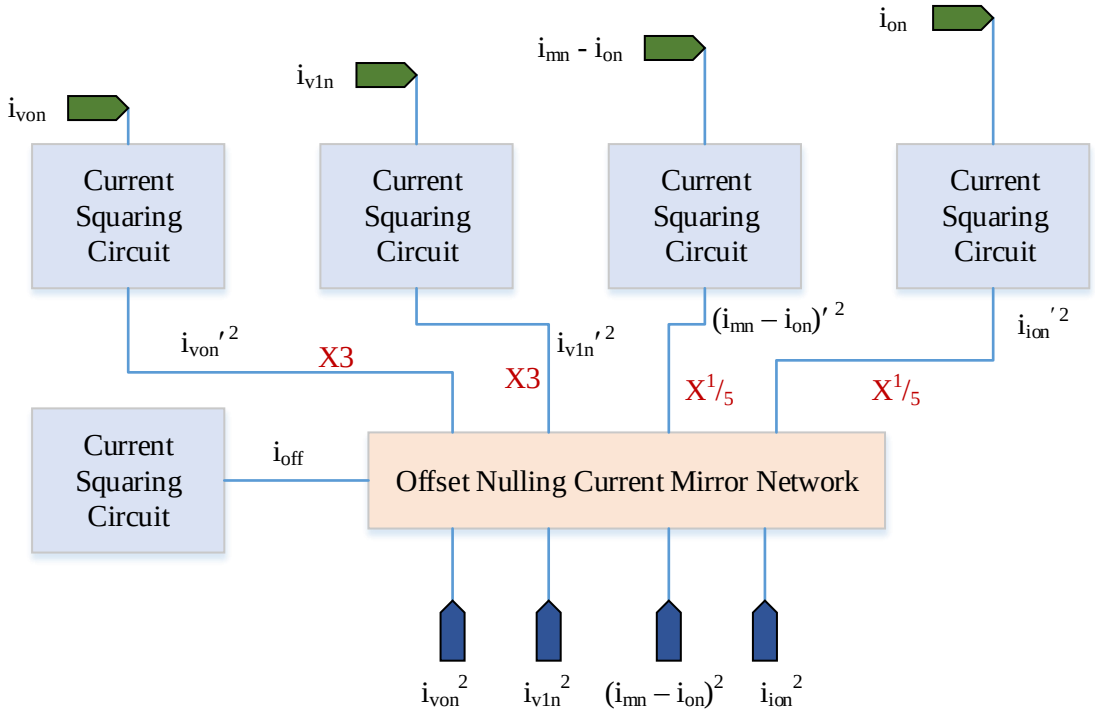


Fig. 4.46. Block level schematic of the L_{OFF} calculation circuit.

The block level schematic shows the four inputs coming into the circuit (green pins at the top). The scaling factor for each of the output currents are noted in red. The offset generated from the fifth current squaring is then subtracted from each of the outputs to generate the desired squared current values (blue output pins).

The LON calculation block consists of four multiplier circuits used to generate the terms in Eq. (4.10) including one that generates the offset current.

4.5.3.2 Simulation Results for the L_{OFF} and L_{ON} Calculation Circuits

The inputs for the L_{OFF} and L_{ON} calculation circuits are the outputs of the input frontend blocks. The same transient simulations that were run to generate the output wave forms shown in Figs. 4.44 and 4.45, were also used to feed the outputs of the input frontend into the L_{OFF} and L_{ON} calculation circuits. In order to simply test the multiplication circuit, during the simulation one of the inputs to the multiplier circuit was kept constant while the other was changed. Some of the resulting graphs from the simulations are shown in Fig. 4.47.

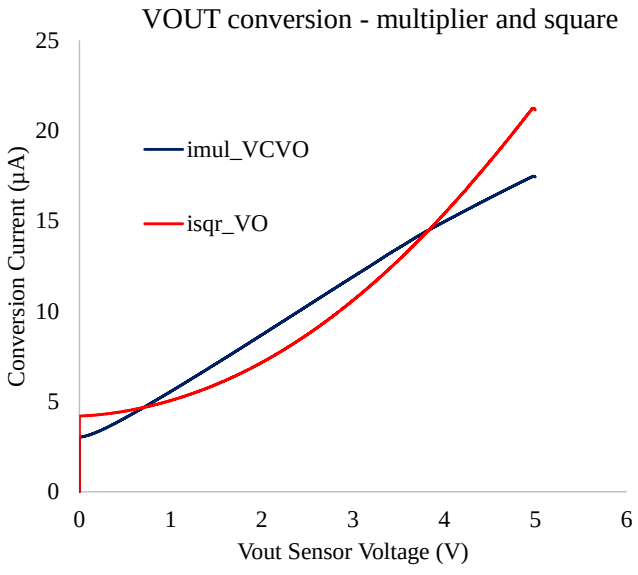


Fig. 4.47. Outputs of current squaring and current multiplying circuits for V_{OUT}.

The outputs of the current squaring circuit and multiplying circuit are plotted against input voltage of V_{OUT}. The squared output has an offset of around 4.5 µA and rises up to 22 µA for an input of 5 V. The multiplier circuit output, *imul_VCVO*, increases linearly from 3 to 17 µA for the input range of 0 – 5 V. The voltage for the solar panel sensor output is held constant at 3.6 V for this simulation.

The conversion simulations for the *VCC* sensor voltage are shown in Fig. 4.48. The output current curves for the linear current, i_{vccn}, and the multiplier output current, i_{vccn}*i_{von}, are shown in the graph. The two currents are denoted by *ilin1_VCC* and *imul_VCxVO* respectively.

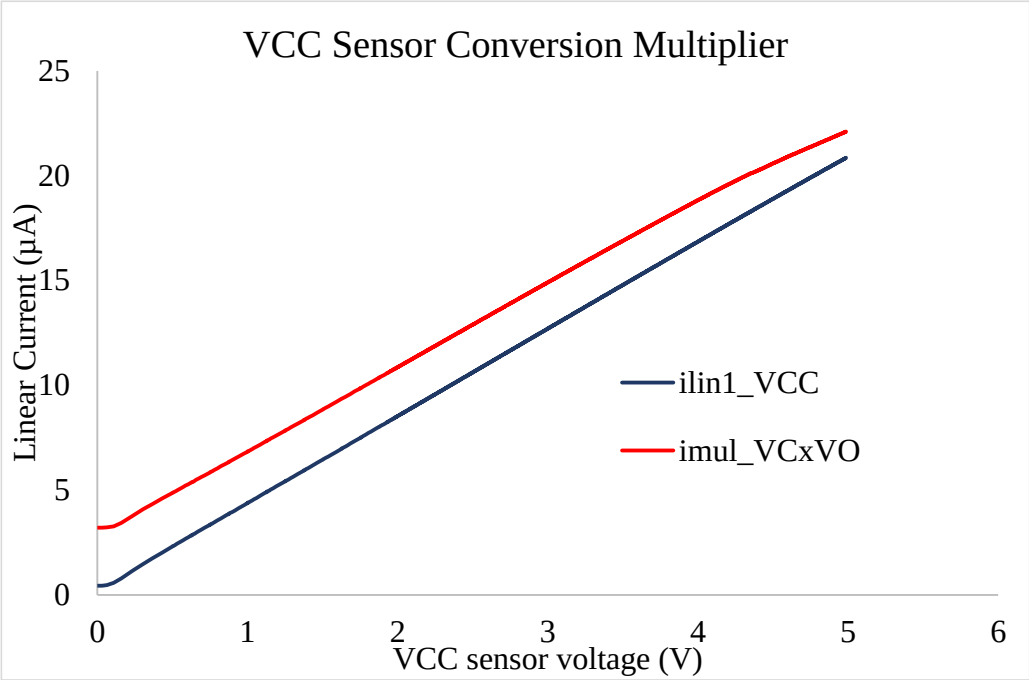


Fig. 4.48. Simulations results for the VCC sensor voltage,

The output voltage, V_{OUT} is set to 4.4 V for the multiplier circuit. As can be seen from Fig. 4.48, the linear output current, i_{vccn} (*ilin1_VCC* in the graph) goes from 0 to 20 µA as the input

voltage goes from 0 to 5 V. The multiplier output current, i_{vccn}*i_{von} (*imul_VCxVO*) has an offset current, similar to the one seen in Fig. 4.47.

The outputs of the current squaring and multiplying circuits for the output current sensor voltage, IOUT, are shown in Fig. 4.49.

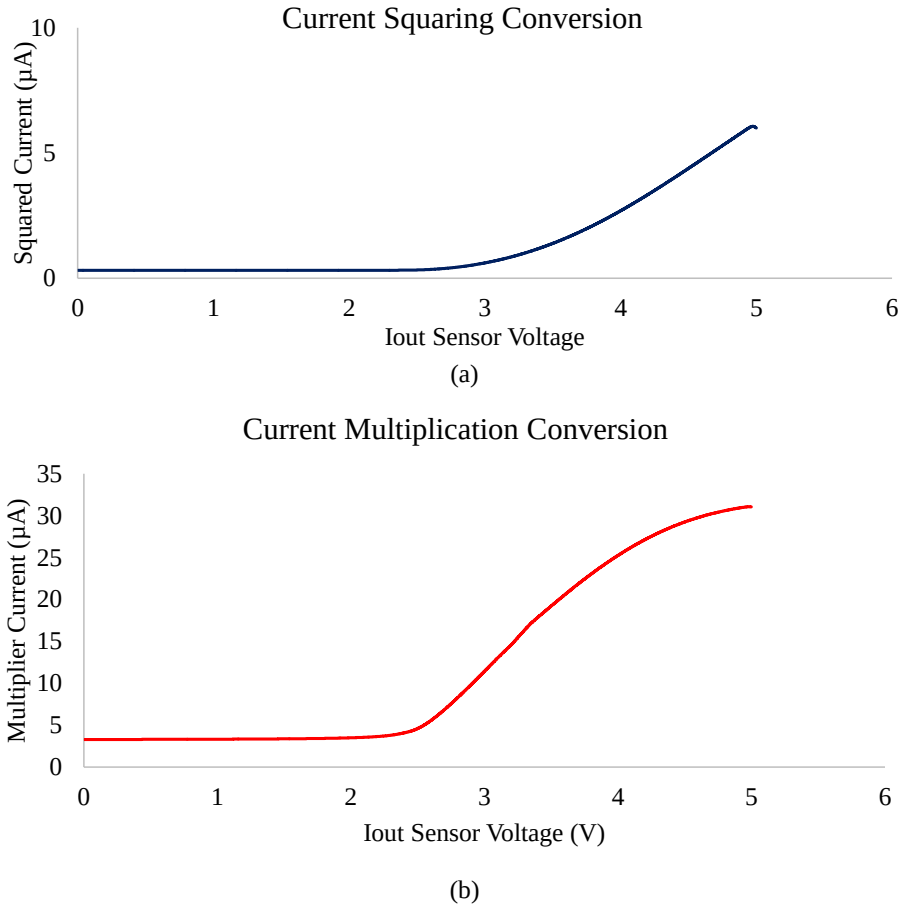


Fig. 4.49. Outputs for the sensor voltage of the output current IOUT (a) Current squaring circuit and (b) Current multiplier circuit,

The multiplier output current, i_{on} * i_{mn}, is generated by keeping the magnetizing current at a constant value and changing the input voltage for the output current as a ramp. The output currents of the current squaring circuit and the multiplier circuit are shown in Fig. 4.49. Due to the nature of the conditioning circuits for the system currents, the input frontend current output stays

at zero until the voltage reaches 2.5 V. Similarly, the output of the squaring circuit and the multiplier circuit stay at the offset values before the input voltage reaches 2.5 V.

The simulation results for the input frontend, LOFF calculation and the LON calculation circuits demonstrate the viability of a current-mode analog signal processing system that can implement the flyback sliding mode controller.

4.5.4 Flyback Decision Circuit

The final circuit of the system is the flyback controller decision circuit as seen in Fig. 4.50.

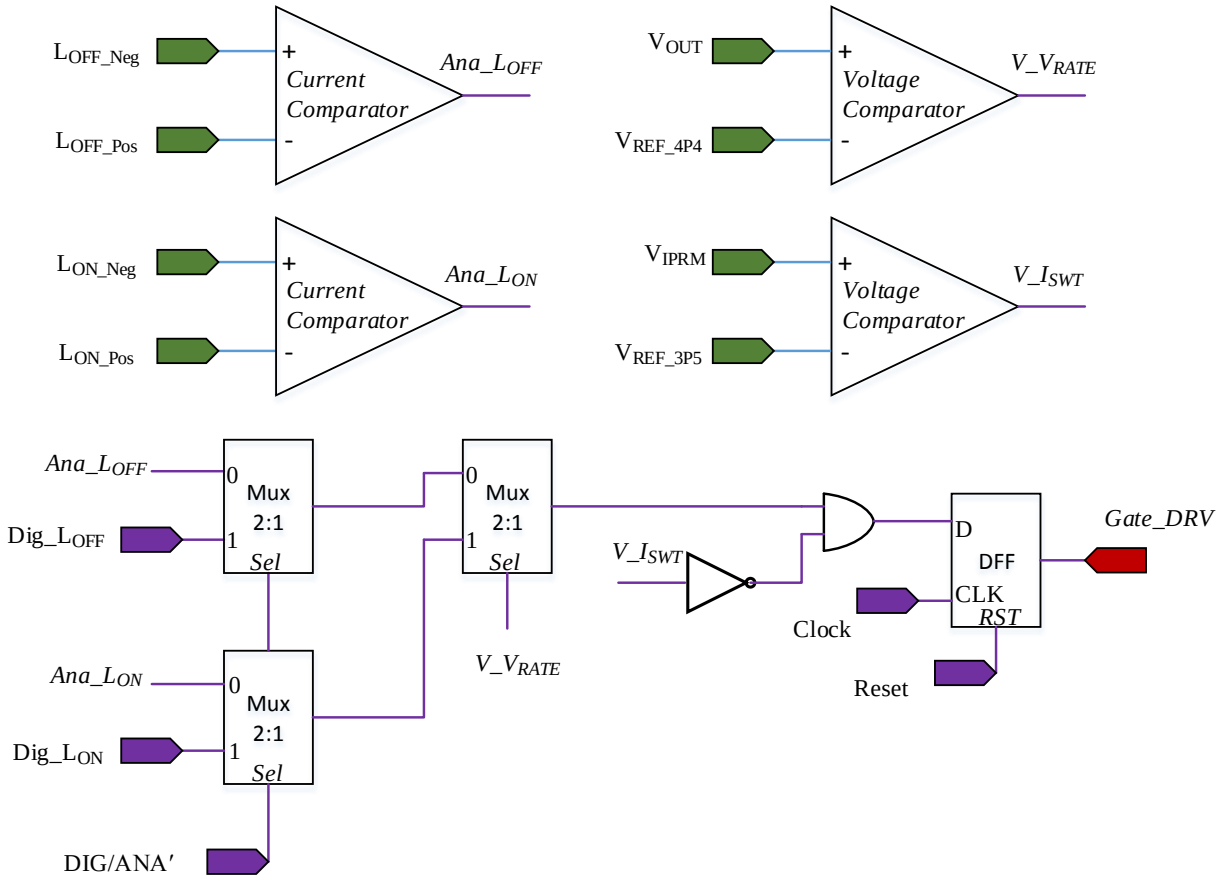


Fig. 4.50. Flyback controller decision circuit.

The inputs to the flyback controller from the analog signal processors are the L_{OFF_Neg}, L_{OFF_Pos}, L_{ON_Neg} and L_{ON_Pos} currents. These are the inputs to two current comparators, the outputs

of which, Ana_L_{OFF} and Ana_L_{ON}, denote the FET driver turn / off decision according to the analog controller. Two 2-to-1 multiplexers are used to choose between the outputs from the analog controller and the digital controller. The selection bit for both muxes is an external digital bit DIG/ANA′. The next step in the control to is to choose between the outputs of the λ_{off} or the λ_{on} comparators. This choice is made by the signal V_V_{RATE} and generated by a voltage comparator that compares the output voltage sensor's output to a fixed reference value which is nominally 4.4 V. When, $V_V_{RATE} = 1$, the L_{ON} signal is chosen, otherwise the L_{OFF} signal is chosen.

The primary side current, as mentioned before, is limited in order to protect the transformer. Nominally, this is set to 15 A which corresponds to a sensor voltage of 3.5 V. Hence, the primary side current sensor output is compared to a fixed reference voltage (can be increased or decreased depending on the target output). When the current goes over the limit, the switch is forcibly turned off and stays turned off until the current falls below the designated value.

The output is loaded into the gate driver circuit through a D flip flop which has a RESET pin. The full controller should always start in a condition where RESET is high, thus making sure that all switches are truly turned off. The clock frequency is typically limited to 500 kHz to 1 MHz.

To test the functionality of the full controller, simulations were carried out with inputs from the sensors being set very close to operating conditions and observing whether the controllers produce expected results or not. Two such simulation results are shown in Tables 4.11 and 4.12 for 25 °C and 200 °C, respectively. The table notes the sensor voltages, the corresponding system values, the ideal normalized values, the linear output currents and normalized values of the entities as considered by the controller.

Table 4.11. Simulation Results Compared with Ideal Normalized Values at 200 °C

Linear V-to-I Conversion and Normalization						
System Entity	Sensor Voltage	System Value	Governing Variable	Ideal Norm. Value	Linear Current Output	Controller Norm. Value
Output Voltage	4.42 V	*200.9 V*	v_{on}	*1.0045*	17.89 µA	1.0045
Input Solar Voltage	3.59 V	*27.2 V*	v_{ccn}	*0.8159*	14.19 µA	0.8125
Output Current	2.567 V	*1.005 A*	i_{on}	*0.01005*	1.12 µA	0.0156
Primary Current	2.5 V	*0 A*	i_{mn}	*0.018*	2.11 µA	0.0302
Secondary current	2.62 V	*1.8 A*				

Mathematical Operation for L_{OFF} and L_{ON} circuits							
Governing Variable	Ideal Norm. Value	Controller Current	Controller Norm. Value	Governing Variable	Ideal Norm. Value	Controller Current	Controller Norm. Value
$i_{mn} - i_{on}$	*0.008*	1.26 µA	0.017	i_{ion}^2	*0.0001*	0.165 µA	0.009
$(i_{mn} - i_{on})^2$	*0.00006*	0.168 µA	0.073	$i_{vccn}*i_{von}$	*0.819*	17.4 µA	0.8145
i_{von}^2	*1.009*	17.24 µA	1.002	$i_{vccn}*i_{1n}$	*0.816*	17.35 µA	0.8122
i_{1n}	*1*	17.81 µA	1	$i_{mn}*i_{ion}$	*0.00018*	1.03 µA	0.00078
i_{1n}^2	*1*	17.21 µA	1	i_{offset}	---	0.963 µA	

Controller Decision for Switching FET							
Ideal Normalized Values			Controller Normalized Value			Decision Outputs	
Entity	Value	State	Entity	Value	State	Entity	State
λ_{off}	0.009	***LO***	λ_{off}	0.033 µA	***LO***	λ_{off}	***LO***
λ_{on}	0.0039	***LO***	λ_{on}	0.117 µA	***LO***	λ_{on}	***LO***

The input reference voltage, v_{1n} (not shown here), is used to generate normalized current values of i_{1n} and i_{1n}^2.

Table 4.12. Simulation Results Compared with Ideal Normalized Values at 25 °C

Linear V-to-I Conversion and Normalization						
System Entity	Sensor Voltage	System Value	Governing Variable	Ideal Norm. Value	Linear Current Output	Controller Norm. Value
Output Voltage	4.36 V	*198.2 V*	v_{on}	*0.991*	17.81 µA	0.9916
Input Solar Voltage	3.61 V	*27.3 V*	v_{ccn}	*0.8204*	14.26 µA	0.8139
Output Current	2.533 V	*0.495 A*	i_{on}	*0.00495*	0.5 µA	0.00696
Primary Current	3.37 V	*13.05 A*	i_{mn}	*0.02175*	1.418 µA	0.0202
Secondary current	2.5 V	*0 A*				

Mathematical Operation for L_{OFF} and L_{ON} circuits							
Governing Variable	Ideal Norm. Value	Controller Current	Controller Norm. Value	Governing Variable	Ideal Norm. Value	Controller Current	Controller Norm. Value
$i_{mn} - i_{on}$	*0.0168*	1.792 µA	0.017	i_{ion}^2	*0.00003*	0.311 µA	0.009
$(i_{mn} - i_{on})^2$	*0.00028*	0.33 µA	0.073	$i_{vccn}*i_{von}$	*0.813*	15.71 µA	0.8118
i_{von}^2	*0.982*	17.24 µA	0.995	$i_{vccn}*i_{1n}$	*0.8204*	15.75 µA	0.8139
i_{1n}	*1*	17.96 µA	1	$i_{mn}*i_{ion}$	*0.00018*	0.809 µA	0.00006
i_{1n}^2	*1*	17.33 µA	1	i_{offset}	---	0.804 µA	

Controller Decision for Switching FET							
Ideal Normalized Values			Controller Normalized Values			Decision Outputs	
Entity	Value	State	Entity	Value	State	Entity	State
λ_{off}	-0.0178	***HI***	λ_{off}	-0.071 µA	***HI***	λ_{off}	***HI***
λ_{on}	-0.0073	***HI***	λ_{on}	-0.035 µA	***HI***	λ_{on}	***HI***

The two tables show operation of the flyback controller at both 25 °C and 200 °C. By varying the current bias, and the LVIC setting bits, the currents can be held at similar levels over

the temperature range. The tables show how accurate the controller is in DC simulations. The numbers in italic represent the corresponding system voltage and current as represented by the sensor voltage inputs, or the ideal normalized values as calculated based upon a 100 W, 200 V output DC-DC converter with a 6:1 turns ratio pulse transformer. The numbers in non-italic represent the internal controller voltage and corresponding currents for the different sensor input voltages and the intermediate mathematical terms. These numbers are also then transformed into normalized values as seen by the controller based upon the current value associated with V_{1N}.

The normalized linear output currents are derived by dividing them by the i_{1n}, the squared currents are normalized by using their ratios to the current i_{1n}^2, and the multiplier current are compared to an extrapolated value of $i_{1n} x\ i_{1n}$. The results show pretty similar normalized values, especially for the medium range of currents. At the lower end, however, the controller current deviates from the ideal values – this can be explained by the fact that at lower current levels leakage current and current produced by the short channel effect have a far more significant role to play. The decision circuit's output statuses also show that controller output follows the ideal output. Different case scenarios were carried out for the different temperatures, and in all cases the controller was found to be providing the current output statues when the λ_{off} or λ_{on} values were over 0.005 or 0.5%. Some of these simulations are given in Appendix A.

4.6 Summary

This chapter has described, in detail, the design and simulation of the various circuits and systems implemented in this project. The first circuits described were the current conditioning circuits such as the linear V-to-I converter and the current squaring circuits. Next the low input common mode OTA and voltage comparator design procedures were described. Simulation results for all these circuits with different model types over the full temperature range were shown.

Next the design and simulation of the 8-bit data converters were explained. The non-linearity errors for both the ADC and the DAC were characterized at the simulation level. The final system described in the chapter was the flyback controller. An all-analog current-mode controller was simulated to implement the sliding mode control. A detailed approach on how to set scaling factor while designing such a circuit was described. Chapter 5 provides the details of the test results on all the various circuits and sub-circuits that have been described in this chapter.

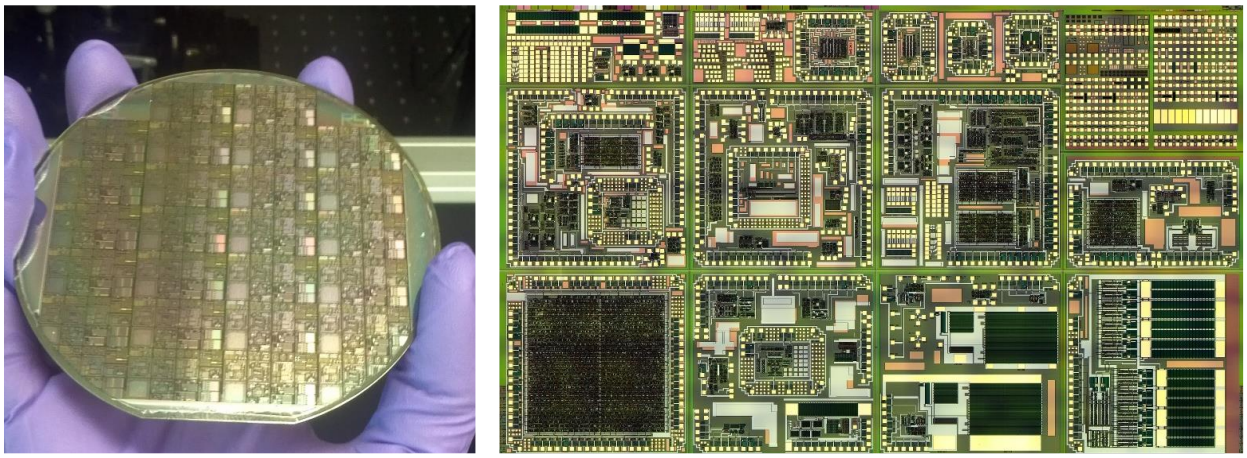
CHAPTER 5 CHIP FABRICATION AND TEST RESULTS

The circuits and systems described in Chapter 4 were sent for fabrication in September, 2014. A total of five wafers were fabricated by Raytheon Systems Limited. This was the second of two fabrication runs. The first run, Vulcan I included basic analog circuits, a PLL, and some digital circuits [55]-[59]. The first three chips of the second run, Vulcan II, were received in late April 2015 and the last two were received in late May 2015. Circuits were tested under probe in the Semiprobe probe station and on a high temperature ceramic leaded package. The results of the circuits and systems tested over temperature are described in this chapter. These include:

- Circuit fabrication and high temperature test setup,
- Results of the current conditioning circuits on the Semiprobe probe station,
- Comparator and amplifier test results at over 450 °C,
- Data converter test results with DNL and INL measurements at 400 °C,
- Flyback controller verification results with sub-circuits test results.

5.1 Chip Fabrication, Packaging and High Temperature Setup

The circuits were put on a 21 mm by 12.5 mm reticle along with other mixed-signal circuits such as two phase-locked loops, an RS-485 transceiver, a ring oscillator, an NFET input stage OTA. The reticle also included both synchronous and asynchronous digital circuits, as well as a CMOS gate driver along with regulation and protection circuits. The circuits were arranged in 5 mm by 5 mm sub-sites with 200 µm dicing lanes. The reticles were fabricated on a 4 inch by 4 inch wafer which consisted of four columns and seven rows. A total of twenty-six partial and full reticles were fabricated in each wafer. The picture of the 4 inch by 4 inch wafer and the die micrograph of the 21 mm by 12.5 mm reticle are shown in Fig. 5.1.



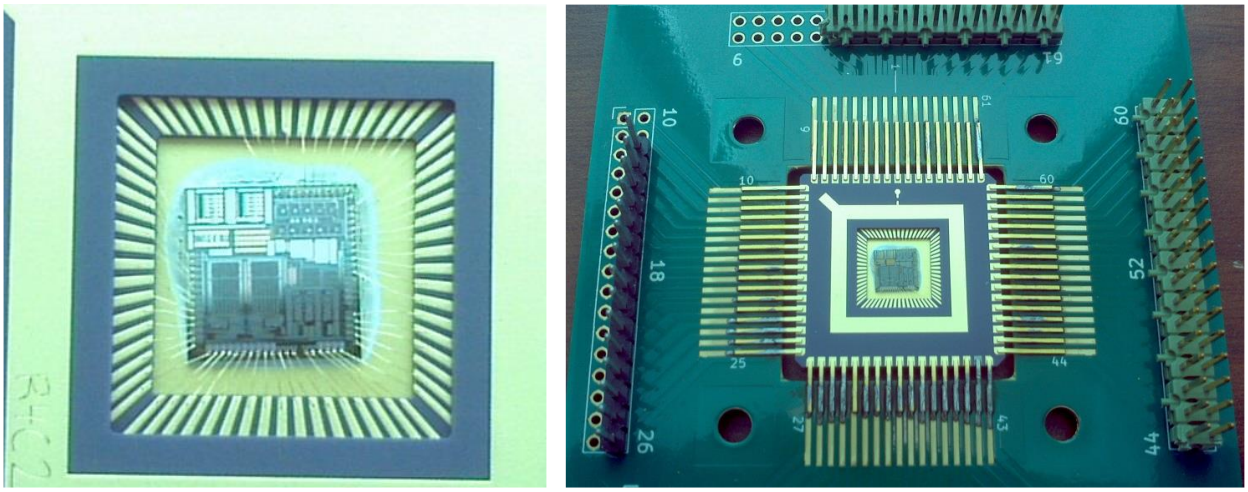
(a) (b)

Fig. 5.1. Pictures of the fabricated SiC wafer (a) Snapshot of the wafer (b) Die micrograph of a single reticle.

The circuits were first tested on the Semiprobe probe station in the MSCAD laboratory for heartbeat measurements. These heartbeat tests were done on wafer level and at room temperature. The 'nominal' wafer was then sub-diced into sub-sites of 5 mm by 5 mm at the High Density Electronics Center (HiDEC) assembly lab. The sub-diced die were then put in a 68 pin leaded ceramic package by using a silver epoxy. The parts were then bonded using ultrasound gold bonding to the 100 µm pads using the K&S 4700 wirebonder at the assembly lab. The bonded packages were finally put on a Rogers-45 board by reflowing the part through the Sikama reflow oven using high temperature solder. The pictures of a bonded die on a package and the package soldered on to a Rogers-45 board are shown in Fig. 5.2.

Pin headers were placed to complete the Rogers-45 breakout board. For high temperature testing, the board was screwed on to four insulating stand-offs on an aluminum structure, with a conducting aluminum stand in the middle to connect to only the package. The aluminum structure was then placed on a hot plate for high temperature testing. A groove was placed on the conductive

stand in the middle right underneath the package thermocouple to control the temperature of the chip. This test setup is shown in Fig. 5.3.



(a) (b)

Fig. 5.2. Pictures of (a) Bonded die on package and (b) LCC package on a Rogers-45 board.

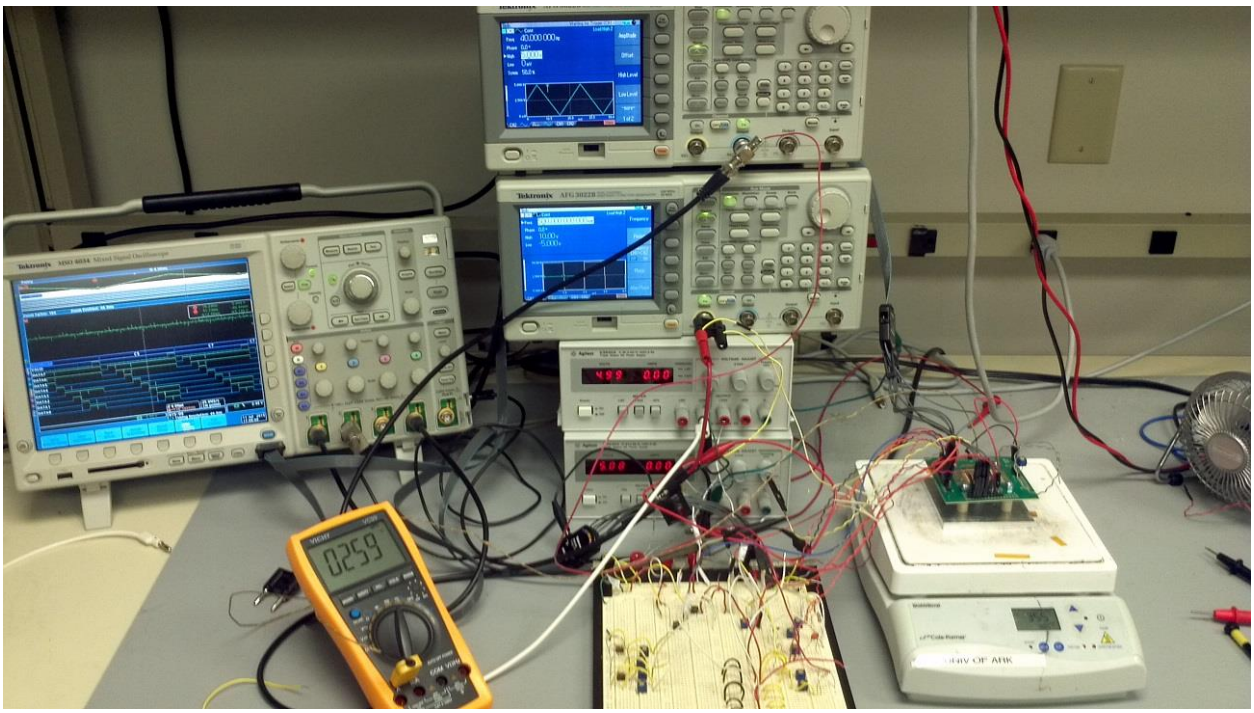


Fig. 5.3. Setup for high temperature testing.

Fig. 5.2 (a) shows a picture of a 5 mm by 5 mm die bonded to the 68 pin ceramic package. The LCC package has a 7.62 mm by 7.62 mm cavity. The 100 µm by 100 µm pads on the edge of the die are bonded using a 1 mil gold wires and ball bonding. Fig. 5.2 (b) shows the package on a board. Male header pins were placed around the border of the board to provide connections to test boards. Fig. 5.3 shows the full test setup for high temperature with this particular setup being for testing an analog-to-digital converter. The Rogers-45 board, mounted on the aluminum structure on top of a hot plate is seen on the right. The wires coming from the header pins are then connected to a test setup that's realized on a second printed circuit board or, as is the case here, on a proto-board. The input signals and power, ground and bias connections are given through external function generators, supplies, resistors and potentiometers. DC outputs are measured by a multimeter, while transient outputs are observed on an oscilloscope. The hot plate can have an external thermocouple connection that lets it control the surface, as is the case here. A second thermocouple is placed in the groove and connected to temperature measuring multimeter shown in Fig. 5.3. A small fan, seen on the very right, was used to cool down the hot plate very quickly.

5.2 Probe Test Results of the Current Conditioning Circuits

The current condition circuits were placed in the available spaces in the middle of the different sub die. These circuits were placed as 'probe-sites' that used the same pads as other more complete circuits but without the ESD diode protection. The location of these circuits in the 21 mm by 12.5 mm reticle are shown in Fig. 5.4. The circuits are placed on the far left sub-site in the middle row. The probe pads are the golden squares, and are 100 µm by 100 µm in dimension. Due to their location and nature, the current conditioning circuits were only tested on the Semiprobe probe station at a temperature range of 25 °C to 300 °C. The Keithley 4200 meter was used to provide stimulus and measure the DC outputs.

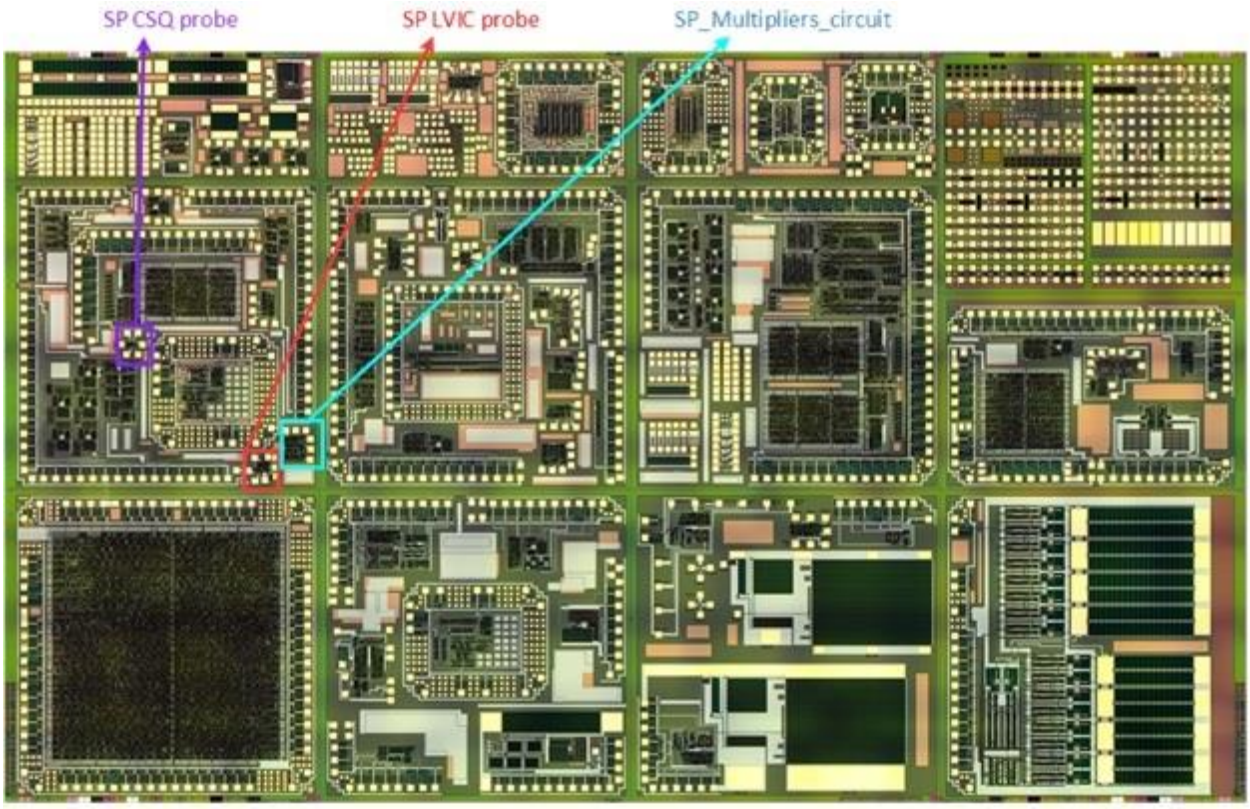


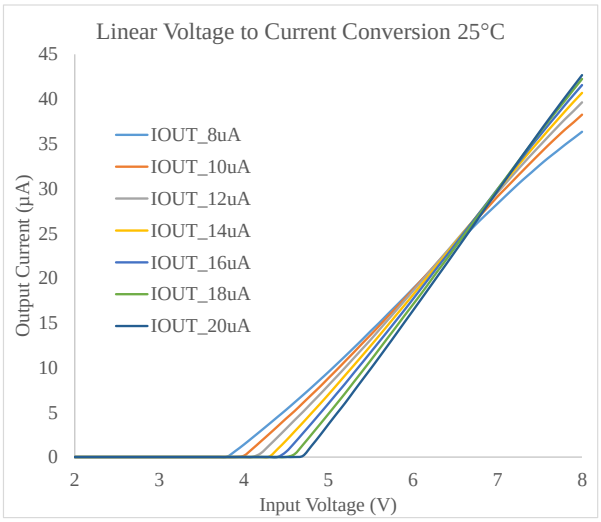
Fig. 5.4 Location of the current conditioning circuits on the full reticle.

5.2.1 Linear Voltage to Current Converter Circuit Test Results

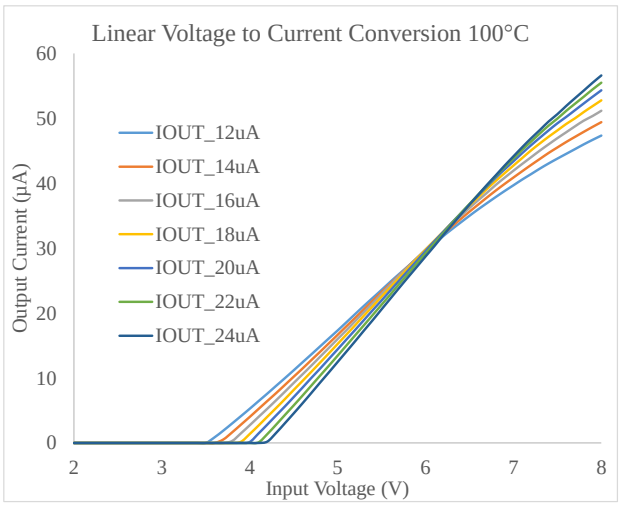
The linear V-to-I converter has a total of eight pins:

- Power and ground pins (AVDD and AVSS), and a current bias pin (*V2*),
- Voltage input pin (*VIN*) and a current sinking output pin (*IOUT*),
- Current setting bit pins – B2, B1 and B0.

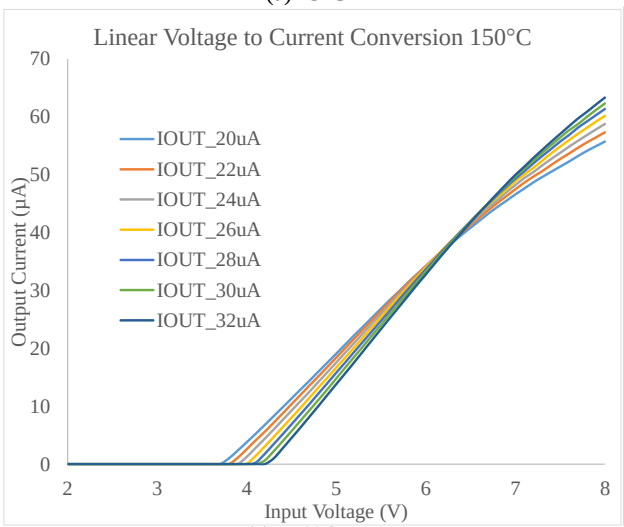
B2 and B1 had pull up resistors connected to the power pin. So by default, unless externally forced, they were set as high, while the pin B0 had a pull down resistor ground setting it to low by default. The bias current, supplied into the pin V2 was swept to set the input voltage minimum at 4 V at all temperatures. The outputs of the linear V-to-I converter at different bias currents for the temperature range of 25 °C to 300 °C are shown in Fig. 5.5.



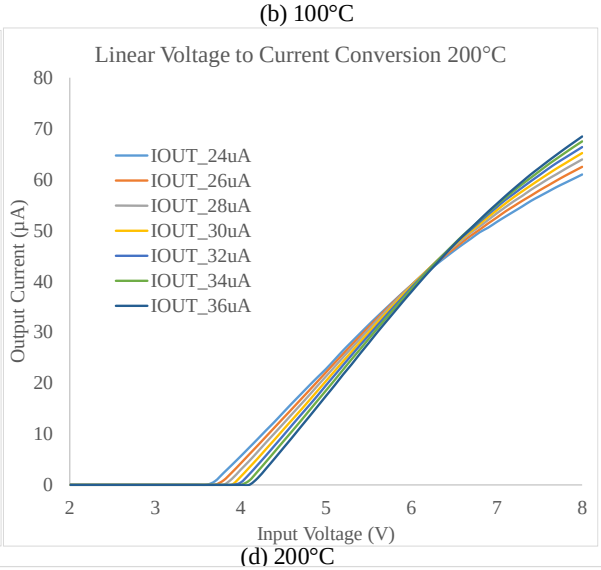
(a) 25°C



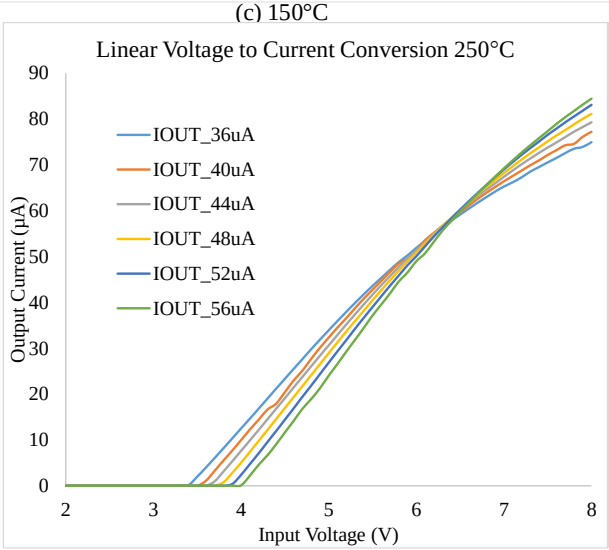
(b) 100°C



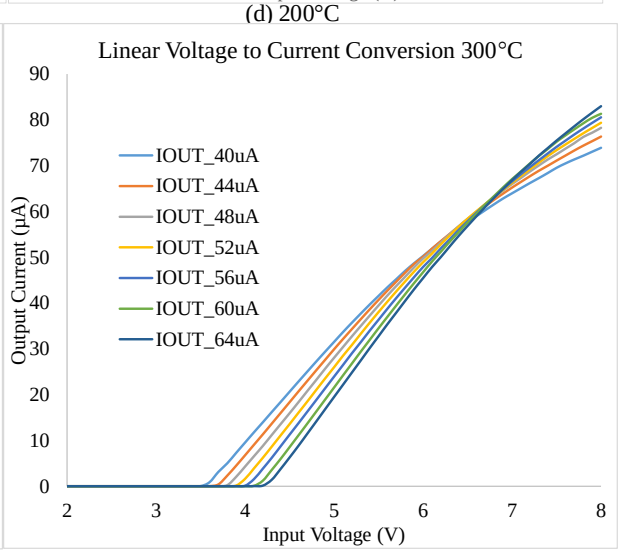
(c) 150°C



(d) 200°C



(e) 250°C

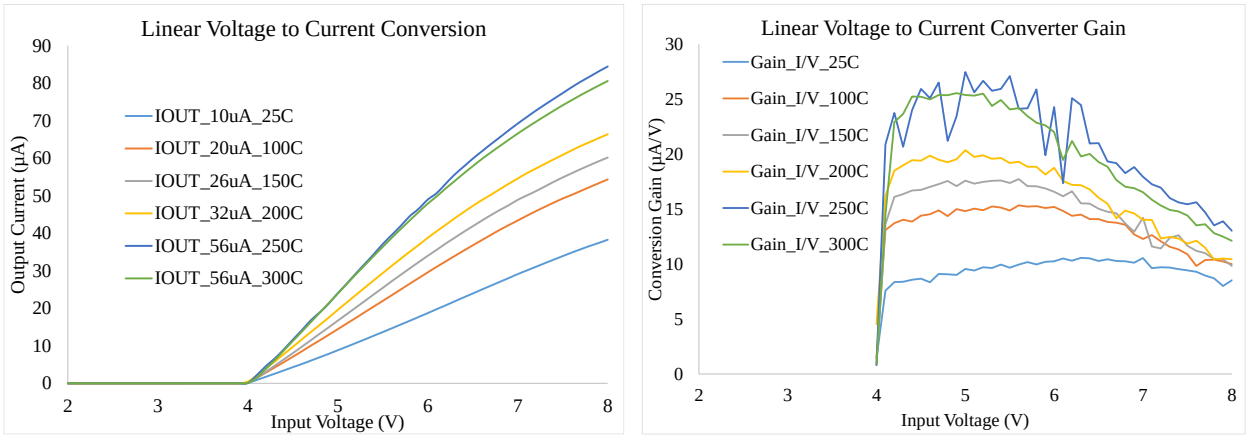


(f) 300°C

Fig. 5.5. Output of the linear V-to-I converter at different bias currents over temperature.

The results in Fig. 5.5 were obtained by setting a constant current to the current bias pin, and applying a ramp voltage to the input of the linear V-to-I converter. The AVDD pin was tied to 15 V while the AVSS was set to ground for all the tests. As can be seen, as the bias current is increased the minimum voltage of the current converter goes higher. This is to be expected, since higher current means higher over-drive voltages and higher drain voltage requirements. Also, in the same vein, a higher value for V2 would increase the proportional co-efficient of the output current according to Eq. (3.7). The conversion gain is proportional to the square root of the bias current, as is the minimum input voltage. Hence, through the nature of the circuit, the outputs converge close to a single point for inputs of 6 to 6.5 V over the temperature range. This can also be specified as the higher input voltage limit for linearity.

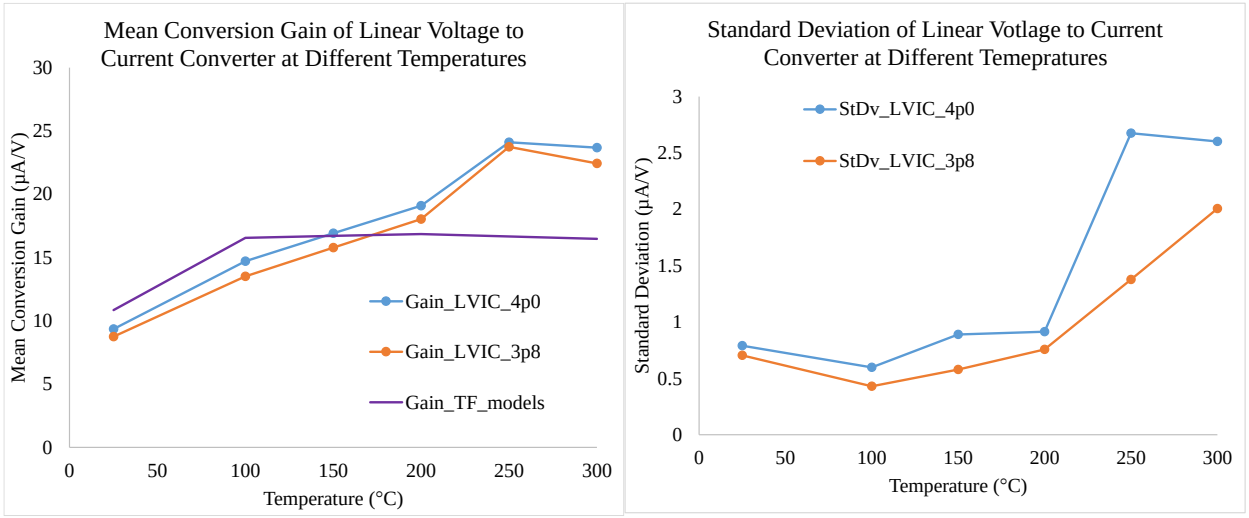
Due to the increase in the bias current, the increased mobility and the reduction in the threshold voltage of the FETs, the conversion gain increases over temperature. The voltage to current converter outputs at different temperatures and bias currents are shown in Fig. 5.6 (a). The conversion gain of the converter over the applicable input voltage range is shown in Fig. 5.6 (b).



(a) (b)

Fig. 5.6 Linear V-to-I characterization (a) Output current vs input voltage and (b) conversion gain of the circuit.

The gain graph at 250 C shows some distortion which is most likely being caused by a non-ideal connection from the probe station. The bias current has to be changed over temperature to ensure an input range minimum of 4 V. The conversion gain not only varies over temperature, but also over input supply range. The linear V-to-I has a very low conversion gain at the bottom end of the range but is mostly stable up to 6 V of input for all temperatures, before decreasing again. This is mainly because of the fact that around that point the amplifying transistor starts to go out of saturation (Fig. 4.3). The mean conversion gains with a unified starting point of 4 V and 3.8 V are plotted over temperature in Fig. 5.7 (a) and the mean standard deviation of the conversion gain over the full supply range is plotted in Fig. 5.7 (b).



(a) (b)

Fig. 5.7. Linear V-to-I performance parameters over temperature (a) Mean conversion gain over input range and (b) Mean standard deviation of the gain over input range.

The material returned in Vulcan II was closest to the BSIM4 TF models from the Vulcan I run. The mean conversion gain of the linear V-to-I converter with the TF models is also plotted over temperature in Fig. 5.7 (a). The mean standard deviation shows about a 10 % value of the

mean conversion gain. While undesirable, this is still acceptable given the nature of the novelty and use of the circuit.

The LVIC circuit measurement results do show considerable deviation in terms of voltage to current gain from simulation results. An investigation of the discrepancy focused on two points – determination of the effect of the circuit parasitics as can be determined by parasitics extracted (PEX) simulation results, and the effect of different bias currents for simulation and measurement. The LVIC circuits were connected to probe pads for characterization and PEX simulations were run with the extracted layout of the LVIC circuits with probe pads. The simulation results show a slight deviation from the schematic simulation results, and hence, at first glance, does not provide a reason behind the high gains measurement. However once corrected for the bias current variation the gain curve from measured values are much closer to the simulated values, as seen in Fig. 5.8.

The mean conversion gains of the two measurement cases as seen in Fig. 5.7 (a) are compared to the simulated results from the PEX simulations (red dotted line) and the LVIC gain after it has been corrected for the bias current (purple).

The difference in bias currents between the measured results and the simulation results is the key contributor to the discrepancy in the gain curve. The voltage to current gain of the LVIC circuit is directly dependent on the term V_2-V_{tn} as per Eq. (4.1)

$$I_{out} = I_2 - I_1 = \frac{1}{2} k_n' \frac{W}{L} (V_2 - 2V_{tn})(2V_{in} - V_2)$$

where V_2 is proportional to the square root of the bias current. Thus, when the conversion gain calculated from simulation are calibrated by the term $\sqrt{(I_{meas}/I_{sim})}$, a more reliable comparison can

be made. From Fig. 5.8, it can be seen that after the correction has been made, the simulation results are much closer to the measured values.

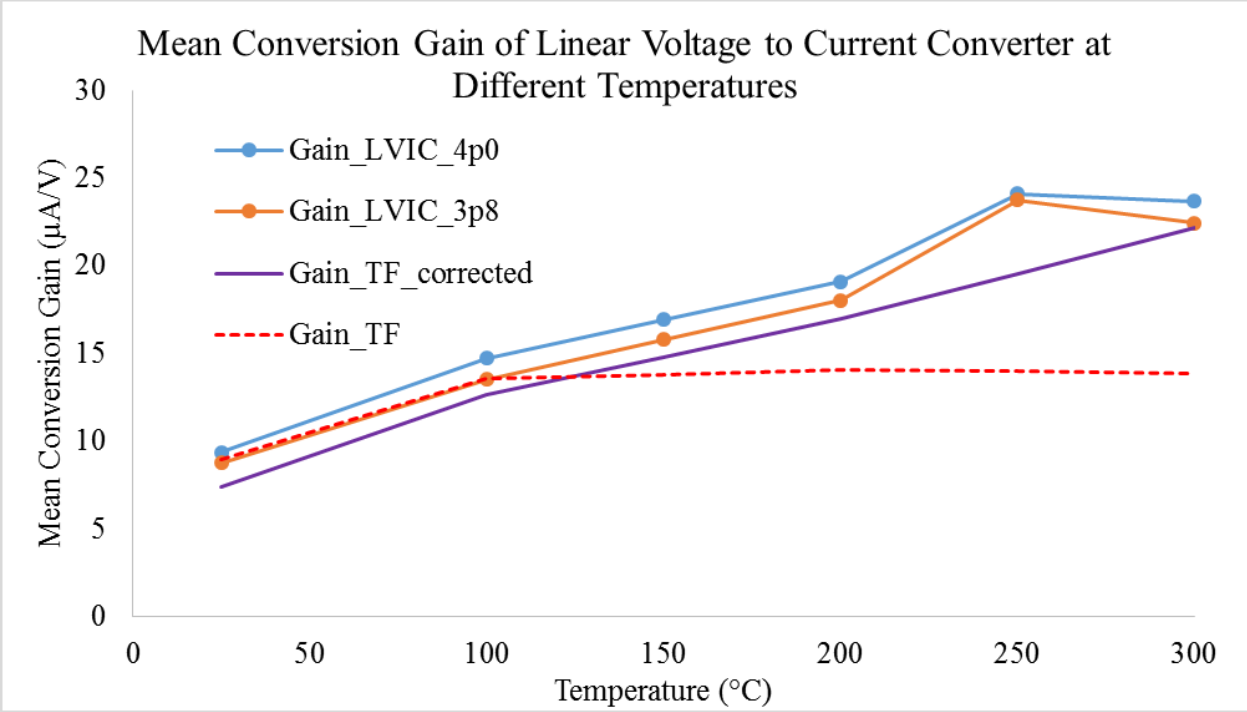


Fig. 5.8. Conversion gain of the LVIC circuit PEX simulations with TF models.

The necessity of high bias currents is the chief reason for this deviation. The high bias current is determined chiefly by the threshold voltages of the devices and the device characteristics of the devices. At higher temperatures, as the threshold voltages decrease for both the PFET and NFET, and as devices become faster, the minimum voltage for the LVIC circuit also starts to go down. In order to keep the lower end of the input range to 4 V, the bias current must be increased to keep the value of V_2 constant, thus maintaining the input range constant over temperature as well. This of course does increase the gain of the circuit as the temperature goes high. However, at this juncture it should also be remembered that the LVIC circuit comes with output gain settings

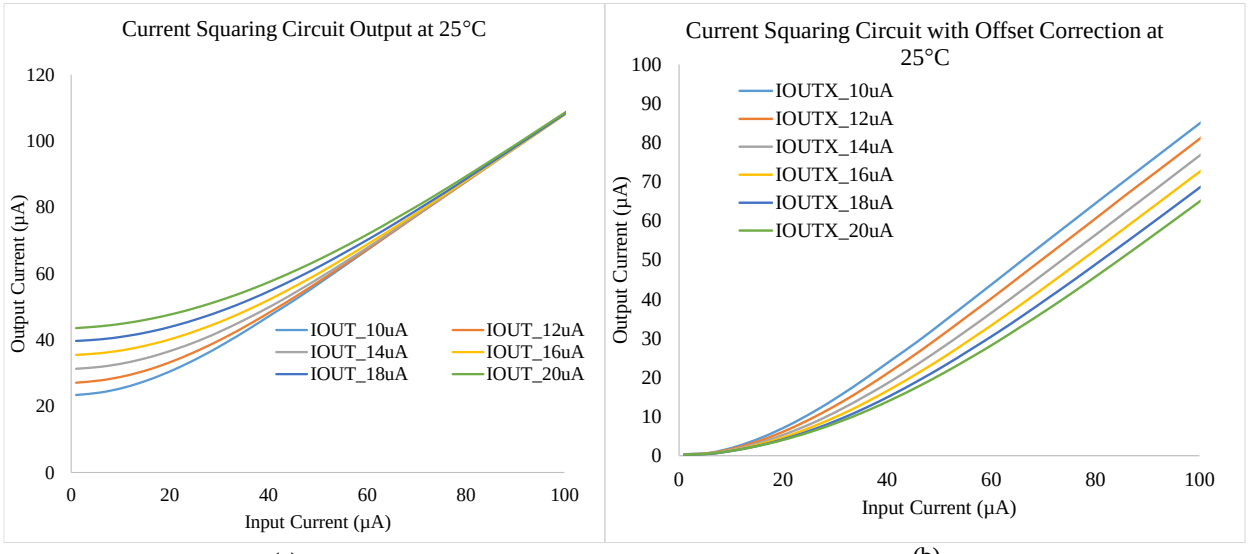
which allow the controller to set the gain from 40% to 120% of the nominal output setting. Hence, the gain can also be adjusted at higher temperatures through either a control feedback loop or a temperature dependent controller.

5.2.2 Current Squaring Circuit Results

The current squaring circuit has six pins

- Power and ground pins (AVDD and AVSS), and the current bias pin (*V2*)
- Input current source pin (*Iin*) and the output current sink pin (*Iout*)
- A bias voltage status pin which is normally unused.

The current squaring circuit was powered by the AVDD and the AVSS pins connected to 15 V and ground respectively. The input current was supplied as a source current from the Keithley 4200 meter. The input current was swept from 0 to 100 µA, while the bias current was set to values ranging from 10 µA to 20 µA at 2 µA intervals. The outputs of the current squaring circuits at temperatures of 25C, 100C, 200C and 300C are shown in Fig. 5.9 - Fig. 5.12.



(a) (b)

Fig. 5.9. Current squaring circuit at 25 °C (a) Without and (b) With offset correction.

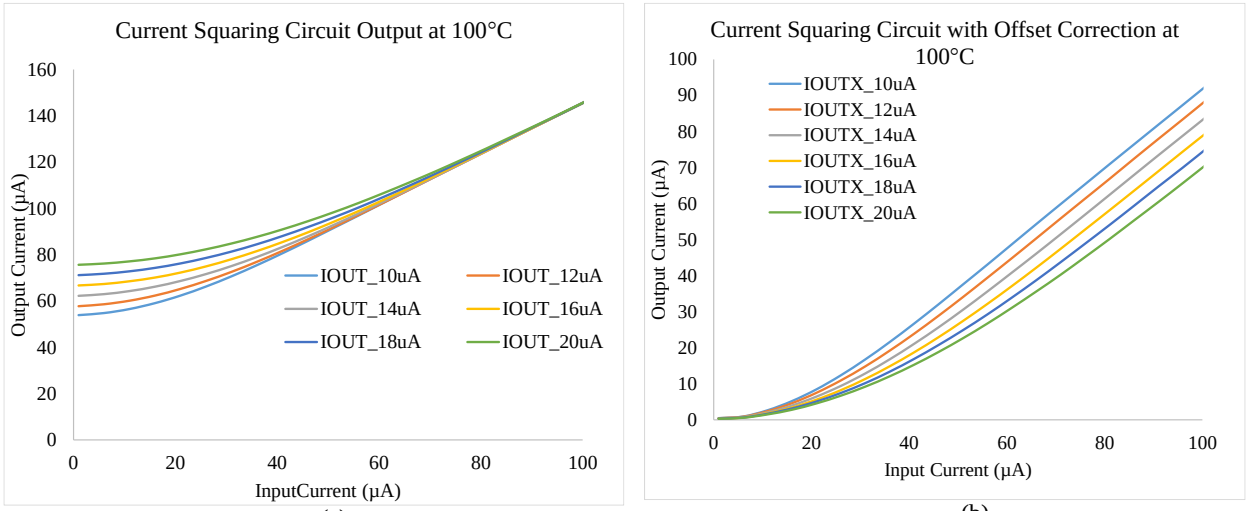


Fig. 5.10. Current squaring circuit at 100 °C (a) Without and (b) With offset correction.

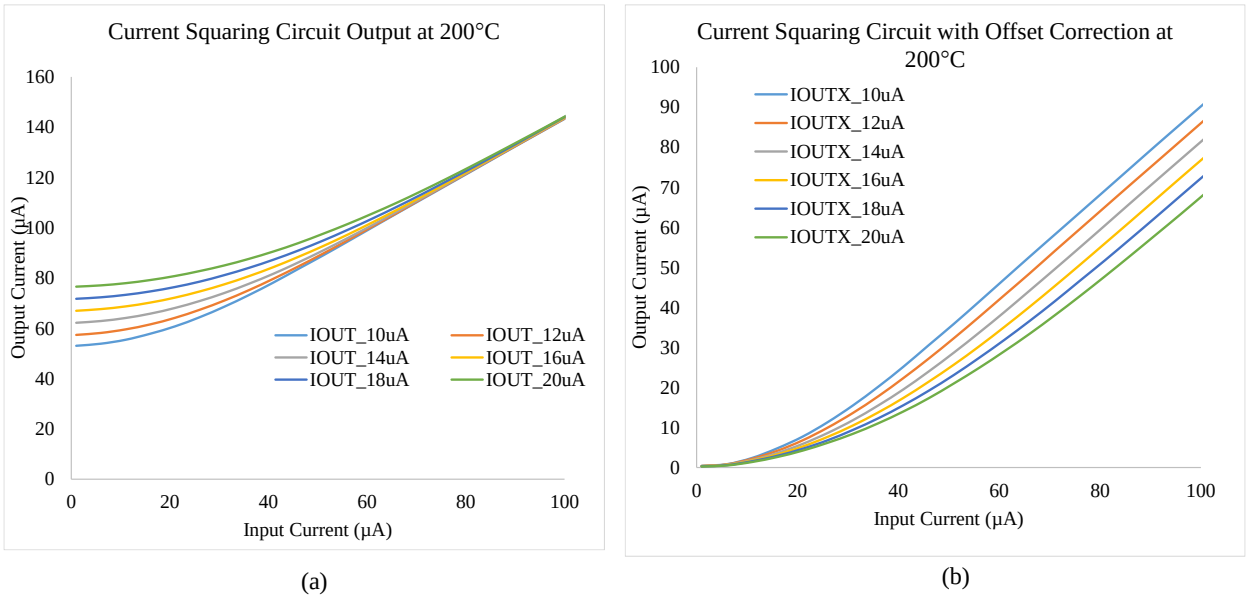


Fig. 5.11. Current squaring circuit at 200 °C (a) Without and (b) With offset correction.

The current squaring circuit output has an inherent offset associated with it due to the effect of the bias current and the voltage, V_2, generated by the bias current as was noted in Eq. (4.2). This can be seen in the graphs on the left in Fig. 5.9 - Fig. 5.12. As the bias current is increased - for all temperatures - the offset increases as well. To properly measure the performance of the circuit, the offset is removed from the output and the conversion gain is measured. From the relationship

developed in Eq. (4.2), the conversion gain is inversely proportional to the bias current as is seen in the graphs on the right side of Fig. 5.9 - Fig. 5.12, which show the lowest conversion gain occurring for a bias current of 20 µA, and the highest gain at 10 µA. The mean conversion gain of the current squaring circuit at different temperatures is shown in Fig. 5.13.

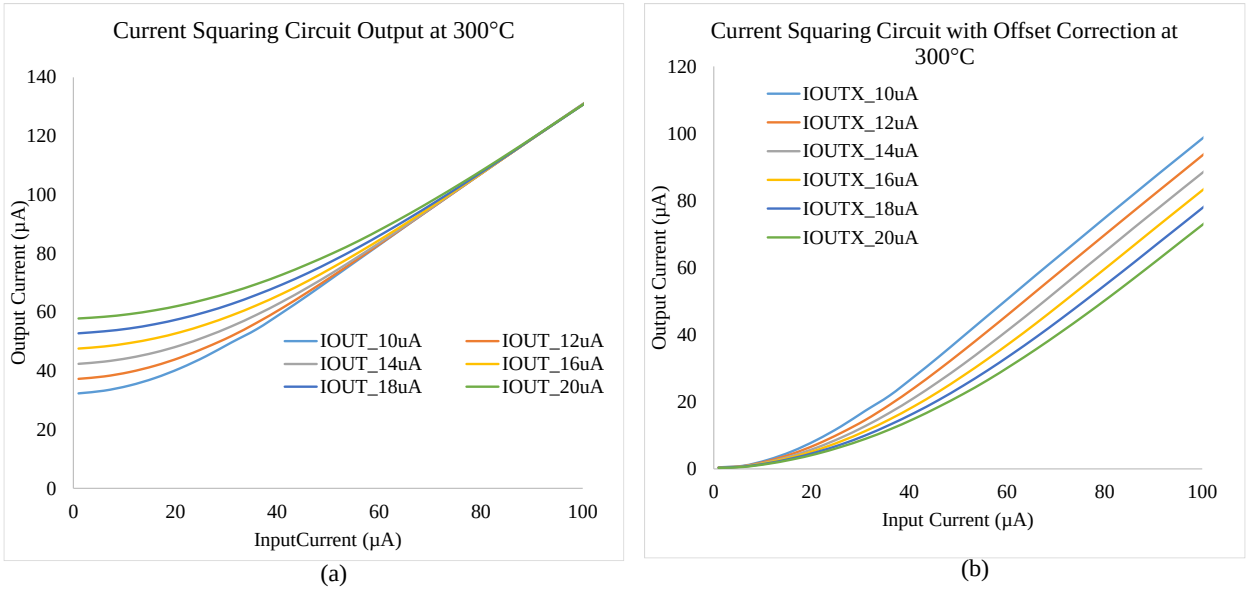


Fig. 5.12. Current squaring circuit at 300 °C (a) Without and (b) With offset correction.

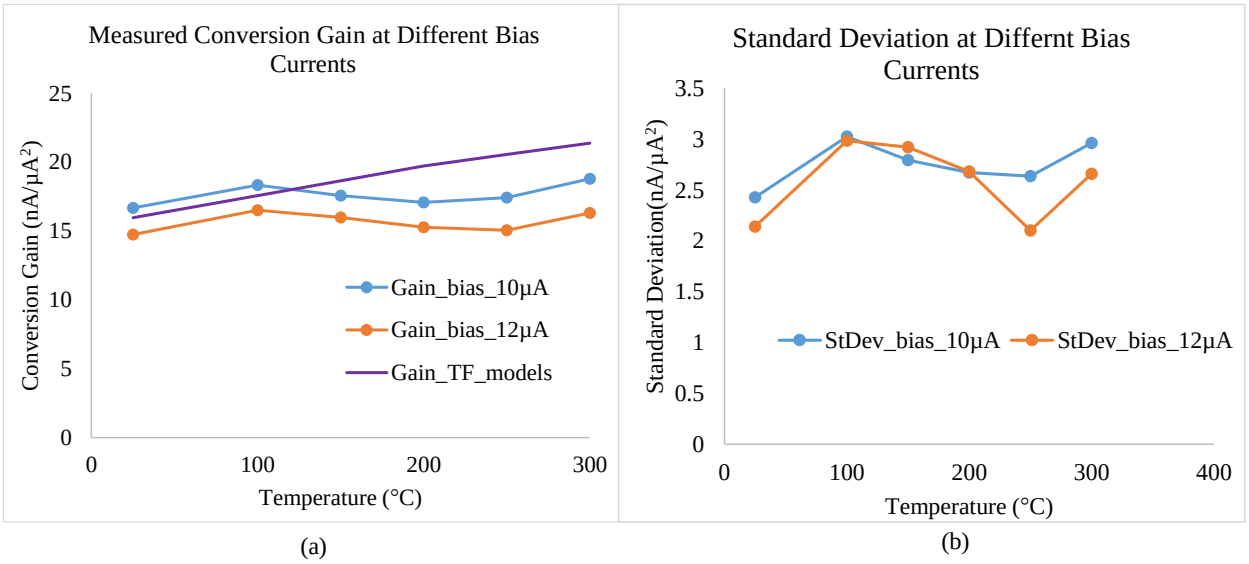


Fig. 5.13. Current Squarer (a) Mean conversion gain and (b) Mean standard deviation.

As already mentioned, the Vulcan II chips tested most closely resembled the TF models based on the Vulcan I run. The conversion gain over temperature for the TF models is shown in Fig. 5.13 (a). The conversion gains for bias currents of both 10 µA and 12 µA are shown in Fig. 5.13 (a). The measured conversion gain of the current squaring circuit is lower than the simulated value, which may point to the temperature aging effect of the devices ignored in the TF models. The conversion gain is not constant over the whole input range and Fig. 5.13 (b) shows the mean standard deviation of the conversion gain over the full input range at different temperatures.

5.2.3 Current Multiplier Circuit

The pins of the multiplier circuits are the following

- Power and ground pins (AVDD and AVSS), current bias pin *V2*.
- Two input current source pins (*Iin1* and *Iin2*) and the output current source pin (*Iout*)

The AVDD and AVSS pins are connected to 15 V and ground respectively. A constant current (nominally 10 µA) is supplied to the bias pin V2. The input current on Iin1 is swept from 1 µA to 25 µA while the other input current, Iin2, is set at different values ranging from 1 µA to 25 µA at intervals of 4 µA, thus emulating the simulation setup in section 4.2.3.

The outputs of the current multiplier circuits for temperatures of 25 °C, 100 °C, 200 °C and 300 °C are shown in Fig. 5.14. The output of the current multiplier circuit increases linearly as the input current Iin1 is swept from 1 µA to 25 µA for a particular value of the other input current Iin2. As the other input current Iin2 is increased or decreased, the slope of the output curve as the current Iin1 is swept increases or decreases as well. Thus, the basic functionality of the current multiplier circuit is verified.

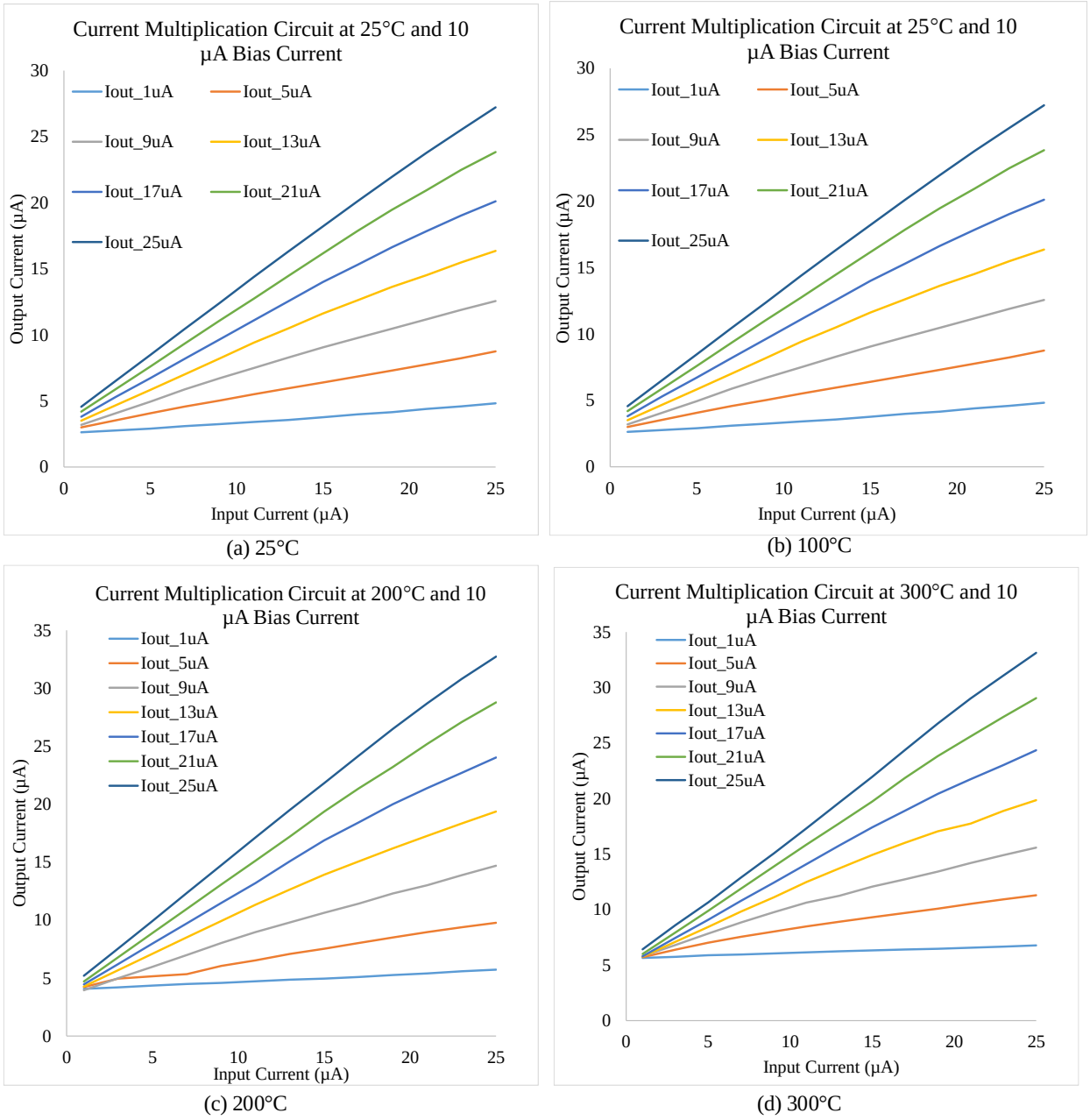
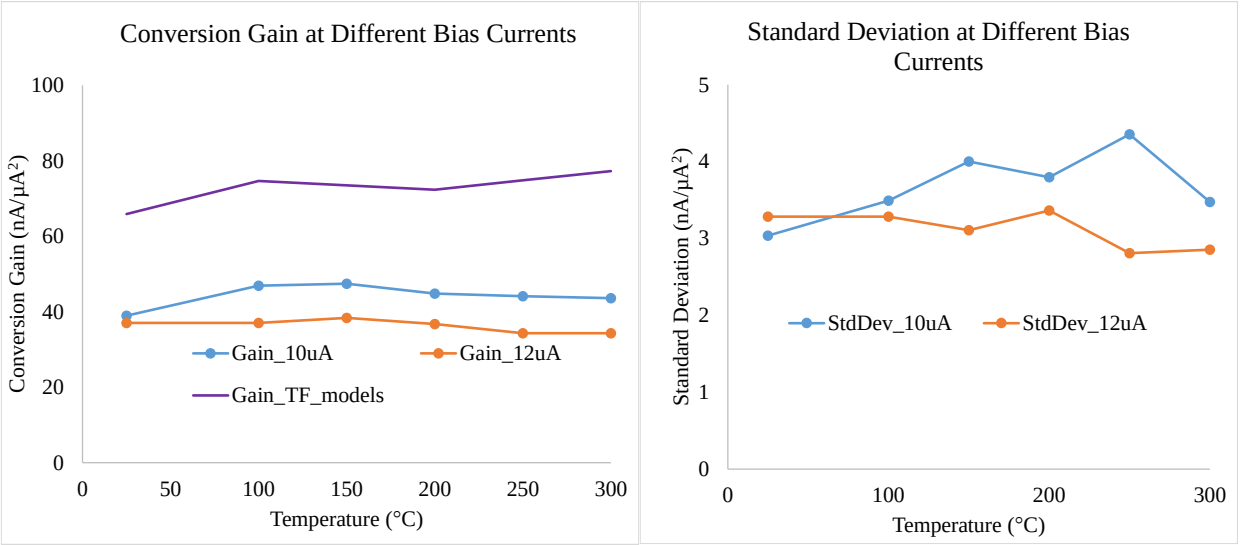


Fig. 5.14. Current multiplier output over (a) 25 °C, (b) 100 °C, (c) 200 °C and (d) 300 °C.

The conversion gain of the current multiplier circuit is shown in Fig. 5.15 (a). The conversion gain changes over the full range, with typically a higher gain in the lower and middle ranges and a lower gain at higher ranges. The mean standard deviation of the gain over the full range is also shown in Fig. 5.15 (b).



(a) (b)

Fig. 5.15. Current multiplier circuit performance (a) Mean conversion gain and (b) Mean standard deviation of the conversion gain over the input range.

The current multiplier circuit's measured gain is consistently lower than the simulated results. From the governing equations it can be assumed that the gain is chiefly governed by the bias current. Since the current is set externally, device nonlinearities are likely the most probable cause for the lower gain. The current multiplier circuit employs current mirrors to subtract the squared values of the sum and difference of the two input current. At lower current levels the output current of the mirrors are much more prone to the short channel effect, and extra current is introduced into the squared value of the difference. This, in turn, when subtracted from the square of a sum, leads to a lower than expected output value. Thus, measured conversion gains are lower than simulation results.

All the three current conditioning circuits, tested up to 300 °C, show satisfactory performance over the intended input ranges – 4-6 V for the linear V-to-I circuits and 0-30 µA for the current squaring and multiplier circuits. This leads to the conclusion that with proper bias settings, an all analog current-mode signal processing and control chip is possible in this process.

5.3 Test Results of the Comparators and Amplifier

This section describes the measured results and graphs from the testing of the voltage and current comparator as well low input common mode operational transconductance amplifier (OTA). Like the current conditioning circuits, the comparators and amplifier were placed as test sites for probing. However, unlike the current conditioning circuits these circuits were packaged in the 68 pin leaded ceramic package which was soldered to the Rogers-45 board. The comparators and the OTA were then tested on a hot plate up to at least 400 °C, and in the case of the voltage comparator as high as 540 °C. The location of the circuits in the full reticle are shown in Fig. 5.16.

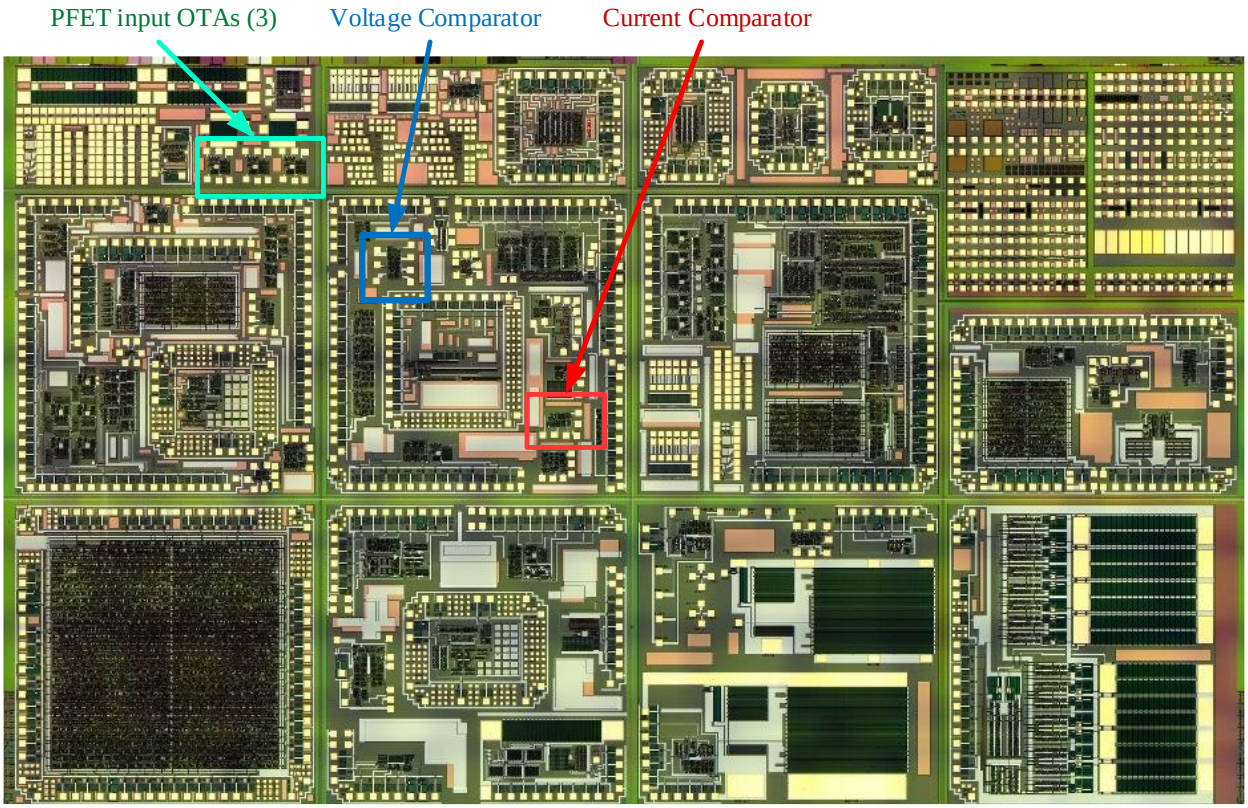


Fig. 5.16. Locations of the comparators and OTA in the Vulcan II reticle.

The circuits were tested by using a combination of the following testing equipment

- Tektronix AFG3022B arbitrary function generator

- Tektronix TDS 540C four channel oscilloscope
- Tektronix MSO4034 and MDO4034-B four channel mixed-signal oscilloscope
- Agilent 34401 $6^1/_2$ digital multimeter
- Fluke – 45 multimeter
- Agilent 3631A triple output power supply
- Agilent 3630 triple output power supply

The Agilent power supplies were used to provide the supply and bias voltages to the circuits. The current biases were set by using a resistor in series with a potentiometer, by which the current through the resistor and into or out of the circuit was controlled. The arbitrary waveform generator was used to generate sinusoidal, triangular and square waves with different pulse widths as necessary. Since the input of the waveform generator is limited to a 10 V maximum, in some cases, when a higher voltage was necessary for the signal, a DC voltage was applied to the negative terminal of the waveform generator output.

5.3.1 Measured Performance of the OTA

The first results presented in this section are those of the amplifier. The OTA pins are

- Power and ground pins (AVDD and AVSS), current sink bias pin (IBIAS)
- Positive and negative input terminal (VINP and VINN), output pin (VOUT)

OTAs and operational amplifiers in general are circuits that have a wide variety of use, e.g. buffers, voltage amplifiers, filters, sampling circuits etc. Hence, the number of performance parameters associated with the OTA is probably higher than most other circuits. Given the nature of use of the OTA in the design in the data acquisition and control systems in this project, the following parameters of the OTA are measured –

- Frequency response – DC gain, unity gain bandwidth, phase margin
- Transient response – Positive and negative slew rates
- DC response – Input common mode and output voltage ranges, offset voltage

5.3.1.1 Frequency Response of the OTA

The frequency response of the OTA was measured by putting the OTA in an open loop configuration and supplying an input sinusoidal difference to the input nodes with a common mode of 3 V. The peak to peak of the output and the input waveform was then used to measure the gain, while the delay between the input and output peaks was used to measure the phase difference. A Bode plot of the OTA at 25 °C is shown in Fig. 5.17. A similar Bode plot, but this time for a temperature of 300 °C, is shown in Fig. 5.18.

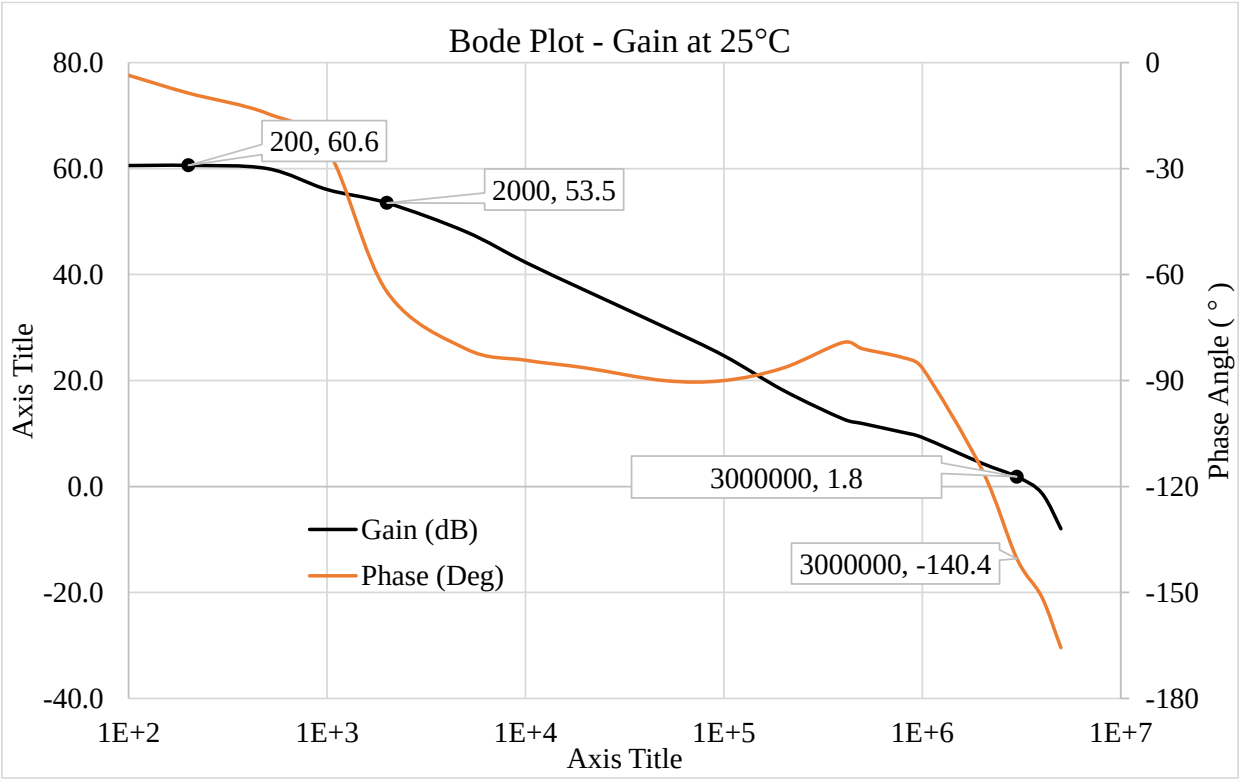


Fig. 5.17. Bode plot (gain and phase) of the OTA at 25 °C.

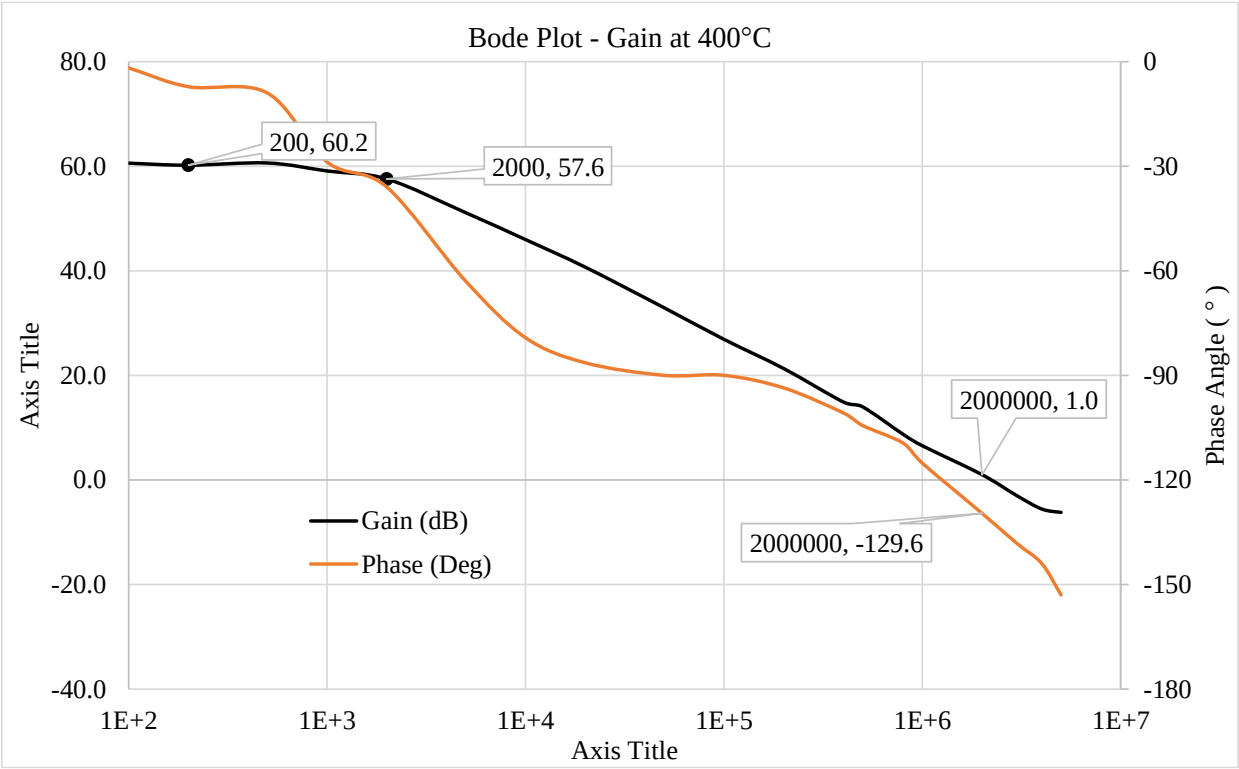


Fig. 5.18. Bode plot (gain and phase) of the OTA at 300 °C.

The Bode plots for both the temperatures show a DC gain of 60 dB. The dominant pole of the OTA is at 1 kHz for 25 °C, while it is at 2 kHz for 400 °C. The UGBW at 400 °C is slightly higher than 2 MHz, while the phase margin is roughly 50°. The same parameters for 25 °C are roughly 3.2 MHz and 36° respectively. The OTA was biased with a current sink of 100 µA over the full temperature range

The DC gain and the unity gain bandwidth over the temperature range of 25 °C to 400 °C are shown in Fig. 5.19 (a) and (b). The DC gain stays pretty stable over the temperature range, never dipping below the design specification of 60 dB. The unity gain bandwidth is also always above 2 MHz, which was the target design specification for the data converters. The phase margin of the OTA is at its lowest, 36°, for 25 °C and increases up to a value over 50° for other temperatures. Although not ideal, the phase margin at 25 °C is still at least higher than 30° which

is generally considered the minimum acceptable value for normal operation. This justifies the decision to 'over-design' the circuit in section 4.3.1.2.

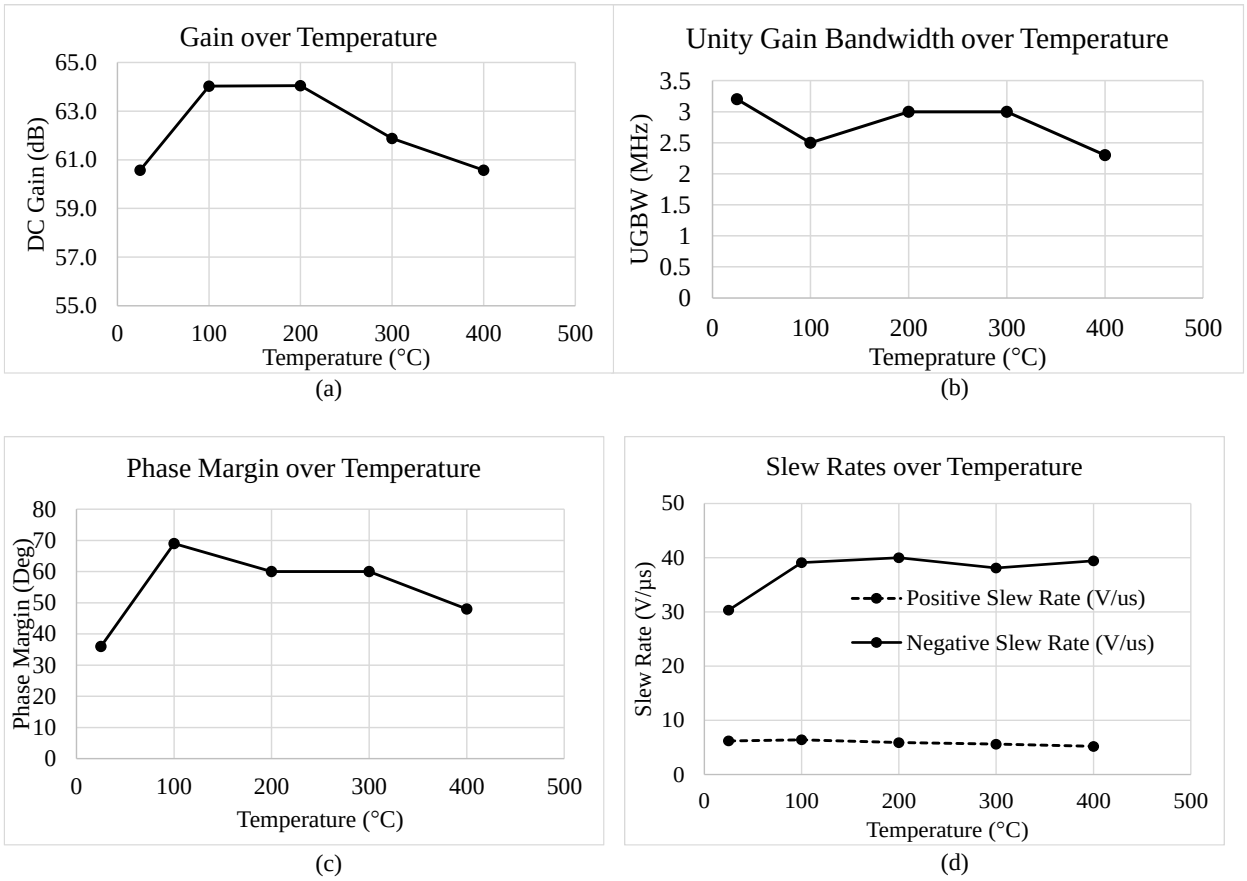


Fig. 5.19. Frequency and transient performances of the OTA over temperature (a) DC gain, (b) Unity gain bandwidth, (c) Phase margin and (d) Slew rate.

5.3.1.2 Transient and DC Responses of the OTA

The transient and DC characteristics were both measured with the OTA connected in a voltage buffer configuration with the negative terminal connected to the output and the function generator output signal applied to the positive input terminal. For the transient characteristics, i.e. the positive and negative slew rates, the function generator output was a 0 to 15 V square pulse. The slew rate is calculated as the slope of the output curve between 10% to 90% of its full range. The slew rate values are shown in Fig. 5.19 (d). The positive slew rate is considerably lower,

between 6.2 V/μs at 25 °C and 5.2 V/μs at 400 °C. The negative slew rate (absolute value is used in Fig. 5.19 is much higher at 30 V/μs for 25 °C to 40 V/μs for 400 °C. This is similar to the simulation results where the pull up network is weaker than the pull down network.

The minimum and maximum of the output voltage of the circuit was also calculated from this test, and they were found to be between roughly 0.4 V to 15 V for all temperatures. The input common mode range and the offset voltage of the OTA were determined by applying a slow ramp signal as the input to the voltage buffer configuration. The limitation of the output signal indicates the minimum and maximum values of the input common mode range, while the offset between the input and the output in the operational region can be deduced as the offset voltage. The DC and transient characteristics of the OTA are listed in Table 5.1 along with parasitic extracted simulation results. The simulation results, shown in italics, were generated with TF models. Since random offsets can only be generated with statistical models, no offset data is available from simulation.

Table 5.1. DC and Transient Characteristics of the OTA over Temperature

Param.	Output Range (V)		Input Common Mode Range (V)		Positive Slew Rate (V/μs)		Negative Slew Rate (V/μs)		Offset (mV)
Temp	*Sim.*	Meas.	*Sim.*	Meas.	*Sim.*	Meas.	*Sim.*	Meas.	Meas.
25 °C	*0.1-15*	0.2-15	*0.1-9.0*	0.1-9.6	*5.5*	6.2	*22.1*	30.3	-13
100 °C	*0.1-15*	0.2-15	*0.1-9.7*	0.2-10.2	*6.0*	6.4	*22.9*	39.1	-5
200 °C	*0.1-15*	0.5-15	*0.1-10*	0.3-11	*6.2*	5.9	*23.5*	40.0	23
300 °C	*0.1-15*	0.4-15	*0.1-10*	0.3-10.8	*6.3*	5.6	*22.5*	38.1	-80
400 °C	---	0.2-15	---	0.2-11.2	---	5.2	---	39.4	-60

The high offset value at higher temperatures indicate two possibilities as the cause of the offset – package and board parasitics that might be contributing to the measurement procedure or, more likely, the need to change the bias current to compensate for the input FETs. A third possibility is the non-uniform release of interface traps from the gate oxide of the differential stage FETs during the heating up procedure that creates the mismatch between devices.

The measured frequency characteristics of the OTA are compared with the parasitic extracted simulated results, using TF models, in Table 5.2. The output impedance of the amplifier is measured by connecting a potentiometer to ground at the output of the amplifier during the open loop frequency test and finding out at which value of the output resistor the gain reduces by half.

Table 5.2. Frequency Characteristics of the OTA over Temperature

Param.	DC gain (dB)		Unity gain bandwidth (MHz)		Phase Margin		Output Impedance (kΩ)
Temp	*Sim.*	Meas.	*Sim.*	Meas.	*Sim.*	Meas.	Measured
25 ℃	*55.9*	60.6	*1.8*	3.2	*73°*	36°	10.3
100 ℃	*55.3*	64.0	*2.1*	2.5	*79°*	69°	6.7
200 ℃	*57.6*	64.0	*2.3*	3.0	*85°*	60°	6.7
300 ℃	*59*	61.9	*2.6*	3.0	*93°*	60°	6.5
400 ℃	---	60.6	---	2.3	---	48°	10.1

5.3.1.3 Discrepancy from Simulated Results

The comparison between the measured results and the parasitic extracted simulation results show higher values for DC gain, unity gain bandwidth and negative slew rates, while the phase margin is considerably less for all temperatures. Two different factors can contribute to this – the

increase in mobility in fabricated devices from the design models, and the decrease of the compensation capacitance from the design value.

FET mobility – the increase in FET mobility means that the transconductance of the FET for a given current and aspect ratio would be higher than expected ($g_m = \sqrt{2I_D k_p' W/L}$) which means the open loop gain of the stages ($A_{v1,2} = g_m r_{ds}$) increases, as evident from Table 5.4. As the gain increases, the unity gain bandwidth increases as well, but the poles that are created by the FET capacitances do not shift in the frequency axis, and thus, the phase response falls comparatively earlier with respect to the UGBW (also seen in Table 5.4). All this leads to a Bode plot where the frequency response drops sooner and the phase margin is lower than expected.

Lower compensation capacitor – the general design equations for the unity gain bandwidth ($UGBW = g_m/C_c$) and slew rate ($SR = I_{tail}/C_c$) both show an inversely proportional relationship to the compensation capacitor. The poly to poly capacitors used in the process are not yet fully characterized and do not have the statistical dependability of mature silicon on-chip capacitors. Hence, a deviation from the estimated value used during design is not very surprising. To verify the effects of the decrease in the capacitor, schematic level simulations were run with the compensation capacitor set to 2 pF, instead of 4 pF. The results simulation results are compared with the measured results in Table 5.3.

Table 5.3. Comparison of OTA Measurements with Modified Schematic Simulations

Temp.	DC Gain (dB)		UGBW (MHz)		Phase Margin		Pos. SR (V/µs)		Pos. SR (V/µs)	
	Sim	Meas	*Sim*	Meas	*Sim*	Meas	*Sim*	Meas	*Sim*	Meas
25ºC	56.6	60.6	3.3	3.2	49°	36°	21.1	6.2	44.4	30.3
100ºC	56	64.0	3.8	2.5	55°	69°	22.5	6.4	46.6	39.1

Temp.	DC Gain (dB)		UGBW (MHz)		Phase Margin		Pos. SR (V/µs)		Pos. SR (V/µs)	
	Sim	Meas	*Sim*	Meas	*Sim*	Meas	*Sim*	Meas	*Sim*	Meas
200ºC	56.2	64.0	4.2	3.0	56°	60°	22.9	5.9	48.1	40.0
300ºC	57.6	61.9	4.7	3.0	57°	60°	22.9	5.6	48.2	38.1

Although the simulation results do not show an exact match with the measured results, the general trend can be ascertained – lower capacitance makes the unity gain bandwidth and slew rates go high and decreases the phase margin. Thus, the discrepancy of the measured results from the simulated ones can be deduced qualitatively, if not completely quantitatively.

5.3.2 Measurement Results of Voltage Comparator

The voltage comparator has the following seven pins

- Power and ground pins (AVDD and AVSS)
- Two current biasing pins (IBIASN and IBIASP) to bias the NFET and PFET input stages
- Positive and negative input pins (VINP and VINN) and an output pin (VOUT)

The circuit was tested at a 15 V power supply. The bias currents were both set to 80 µA for the nominal room temperature of 25 °C. The current is allowed to increase over temperature, as the FETs on the die become faster. The maximum current is 110 µA at 450 °C. The circuit is operational with a bias current range of 60 µA to 120 µA. The voltage comparator was tested for hysteresis voltage, rise and fall times as well as propagation delays. To test the hysteresis, a slow triangular wave was set as the input signal to the positive input pin VINP, while the other negative

input pin was held at a constant voltage. The input ramp voltage (blue) and the output of the comparator are shown in Fig. 5.20.

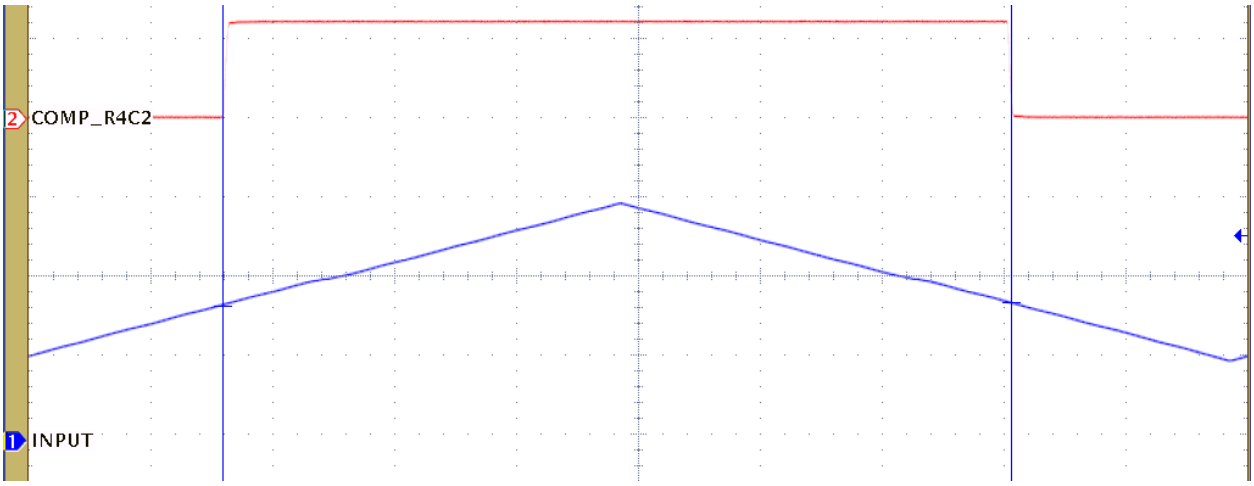


Fig. 5.20. Voltage comparator output with ramp input voltage (hysteresis measurement).

The output switches from zero to the supply voltage (set to 12 V in this particular instance) as the input crosses a threshold. The voltage on the negative pin for this test was held at 3.5V. The crossover voltages for the transition are noted by cursors on the mixed-signal oscilloscope and show a transition at 3.459 V and at 3.513 V, thus indicating a hysteresis of 54 mV.

The rise and fall time of the comparator were measured by applying a square pulse ranging from 2 V to 6 V to the positive input while the negative input is held at 4 V. The input pulse cause the output of the comparator to go from zero to one and back to zero. From the output curve, the rise and fall times of the comparator can be determined, while the transition times between the input and the output edges refer to the propagation delays.

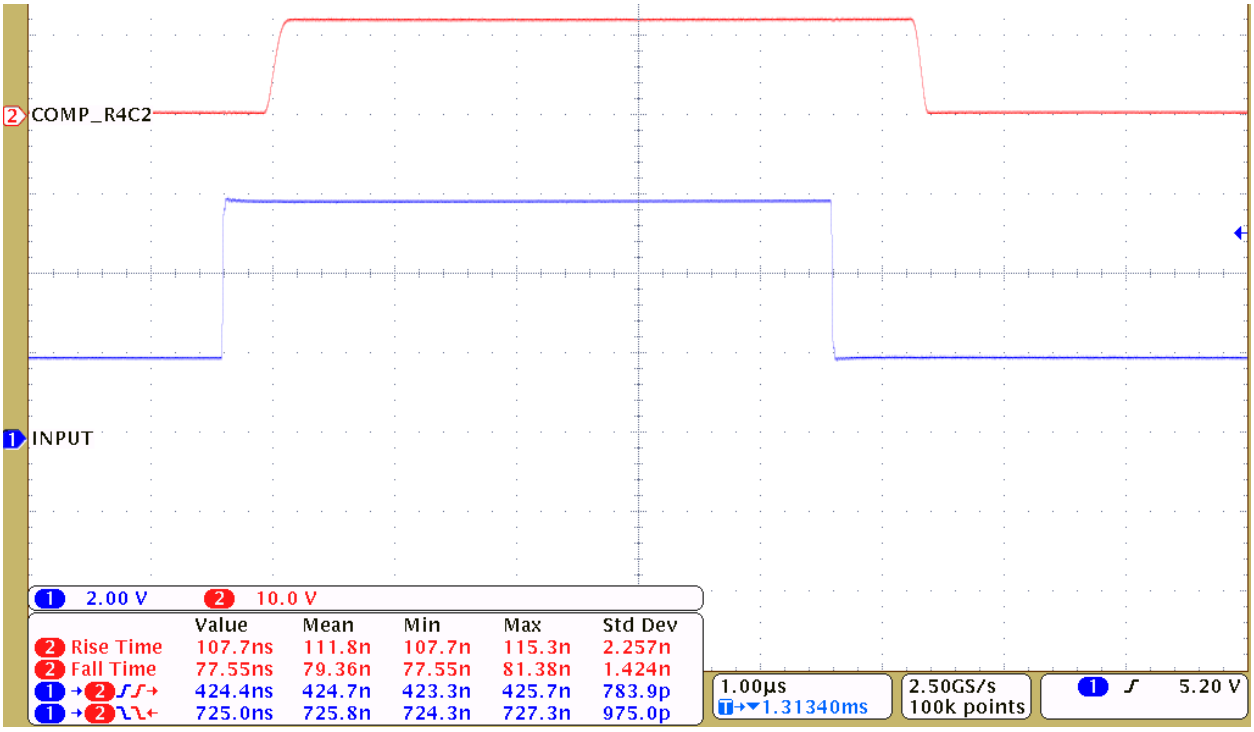


Fig. 5.21. Voltage comparator with square pulse input (timing measurements).

The mixed-signal oscilloscope can calculate the rise and fall times along with the propagation delays as seen in Fig. 5.21. The comparator shown in the figure, working at a 12 V supply, has mean rise and fall times of 111.8 ns and 79.3 ns respectively. The mean propagation delays are 424.7 ns for low to high transition and 725.8 ns for high to low transition.

The comparator was tested over a temperature range of 25 °C to 550 °C for a 12 V and a 15 V supply. The rise and fall times of the comparator for the different supply voltages for the complete temperature range are shown in Fig. 5.22. The rise and fall times of the comparator are much higher for a 12 V supply. This is to be expected since a lower power supply translates to a lower drive strength and a slower circuit.

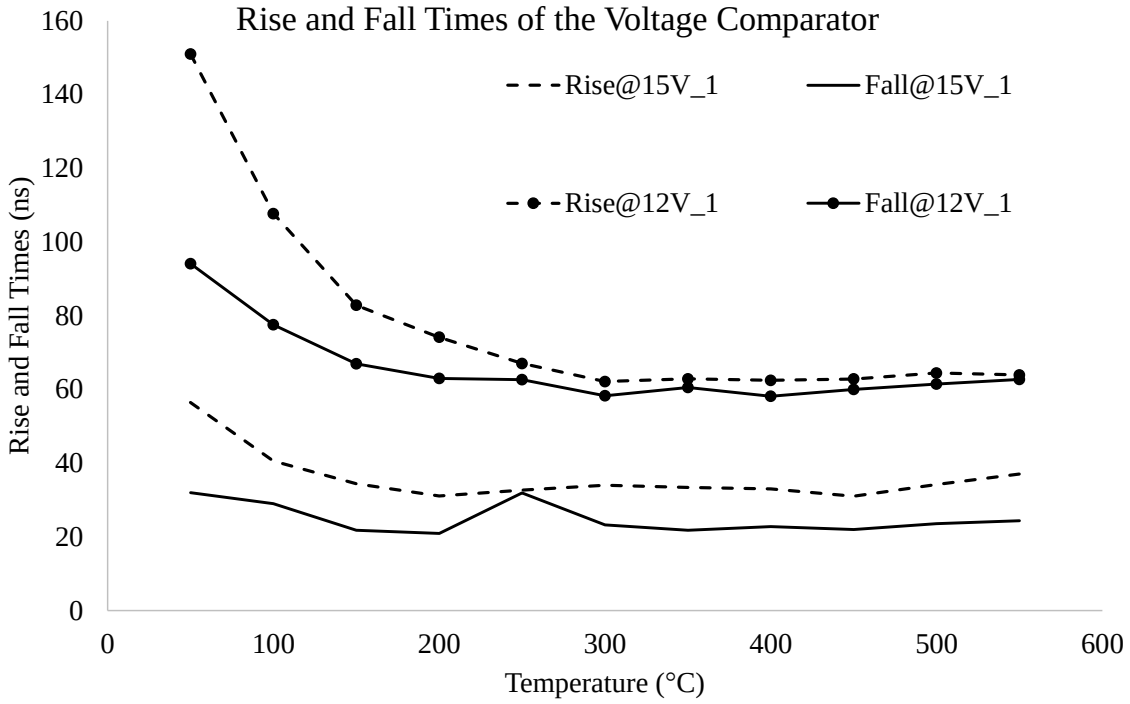


Fig. 5.22. Rise and fall times of the comparator over temperature a 12 V and 15 V supplies.

The rise and fall times also tend to decrease with temperature up to 400 °C. The 'speeding up' of the circuit can be traced to the phenomenon of the release of trapped interface charges at high temperatures. However, at over 450 °C, the scattering effect of the electrons start to take over and as a result the times start to increase again. The fall time for the 15 V supply is under the design specification of 50 ns, while the rise time is over the specification at 25 °C although it drops to 40 ns at 100 °C. The propagation delays for the voltage comparator, taken for an overdrive voltage of 2 V, are shown in Fig. 5.23. The design specification for the propagation delays was 200 ns and simulation results showed propagation delays of less than 150 ns for TT and TF FET models. Measurement for lower over drive voltage will have to be taken later on. Simulation results show, for a bias current of 100 µA, positive and negative propagation delays of 348 ns and 474 ns respectively at 25 °C. At 300 °C, the delays are 281 ns and 355 ns. The delays are still less than half the minimum target clock period and should not affect the circuits and system significantly.

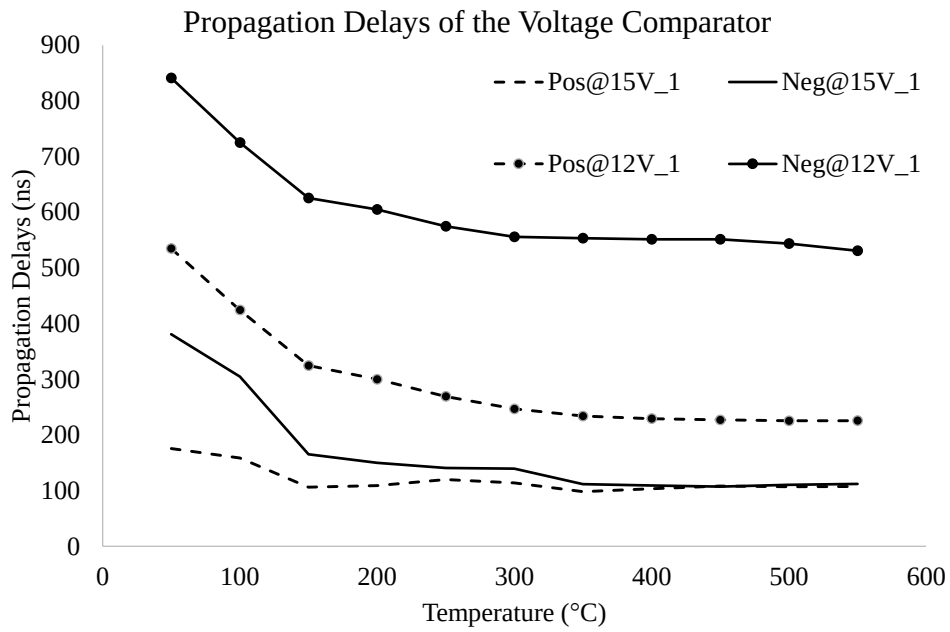


Fig. 5.23. Propagation delays of the voltage comparator.

The propagation delays for the comparators are higher at a supply voltage of 12 V than at 15 V. The low to high propagation delay (*Pos*) is smaller than the high to low (*Neg*) delay, and is under the design specification of 200 ns for all temperatures. The high to low propagation delay of the voltage comparator is higher than the specification of 200 ns at 25 °C and 100 °C, but after that consistently stays underneath the desired specification of 200 ns. This again points to a comparator that is ideally suited for high temperature applications.

Finally the hysteresis voltage of the comparator is measured from the input triangular wave. The hysteresis specification was 30 mV over temperature, and simulation results for typical FETs showed the hysteresis voltage to be so (section 4.3.2.3). The fabricated comparator has a more varied response in terms of hysteresis voltage. As seen in Fig. 5.24, the hysteresis starts off at around 50 mV and in general decreases with temperature.

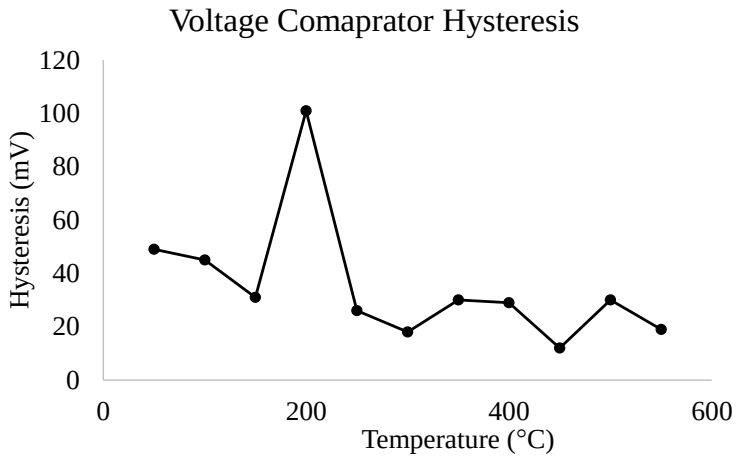


Fig. 5.24. Voltage comparator hysteresis over temperature.

The graph in Fig. 5.24 shows an anomaly at 200 °C, where the hysteresis shoots up to 100 mV, however that is in most likelihood an aberration in the measuring procedure rather than a circuit characteristic. If that point is to be ignored, the hysteresis is near or under the design spec of 30 mV for the temperature range of 150 °C to 550 °C.

A quick comparison of the measured performance parameters of the voltage comparator with simulated values is given in Table 5.4. The simulation results chosen for comparison are the TF models which most closely resembled the Vulcan II device behavior.

Table 5.4. Comparison of Measured and Simulated Results of the Voltage Comparator

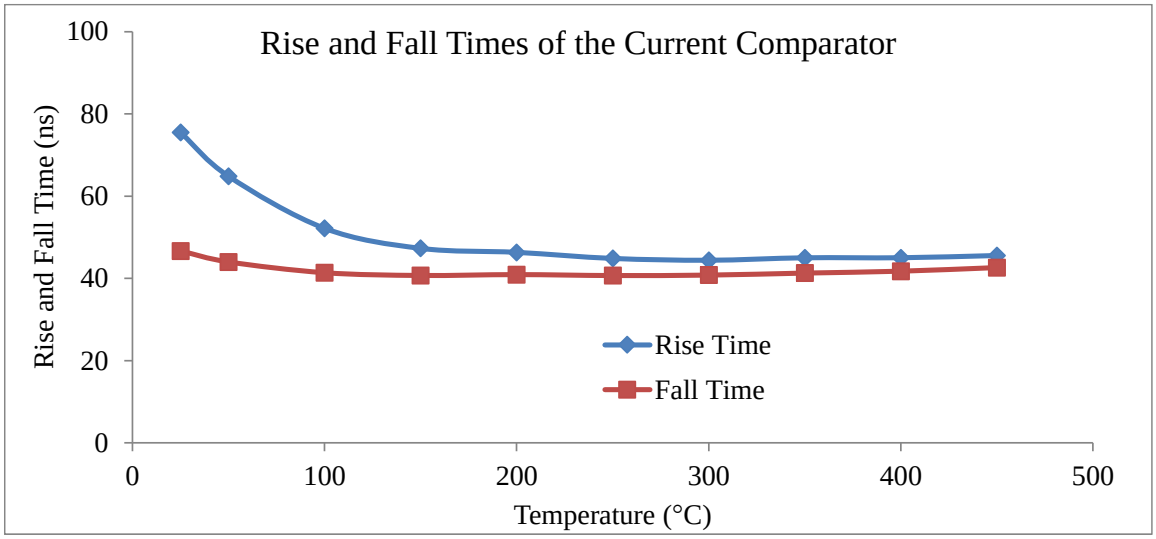
Param.	Rise time (ns)		Fall time (ns)		Lo-to-Hi Prop. delay (ns)		Hi-to-Lo Prop. delay (ns)		Hysteresis (mV)	
Temp.	*Sim.*	Meas.	*Sim.*	Meas.	*Sim.*	Meas.	*Sim.*	Meas.	*Sim.*	Meas.
25 °C	*33.8*	56.5	*43.9*	32	*114*	176	*144*	381	*25*	49
100 °C	*22.4*	40.5	*27.6*	29	*94*	159	*122*	305	*21.9*	45
200 °C	*24.3*	31.1	*28.2*	20.9	*90.4*	109	*121*	150	*21*	101
300 °C	*21.7*	34	*29.7*	23.2	*94.9*	114	*126*	139	*22.9*	18

Param.	Rise time (ns)		Fall time (ns)		Lo-to-Hi Prop. delay (ns)		Hi-to-Lo Prop. delay (ns)		Hysteresis (mV)	
400 °C	---	33	---	22.8	---	103	---	109	---	29
500 °C	---	34.2	---	23.6	---	107	---	111	---	30
550 °C	---	37	---	24.4	---	107	---	112	---	19

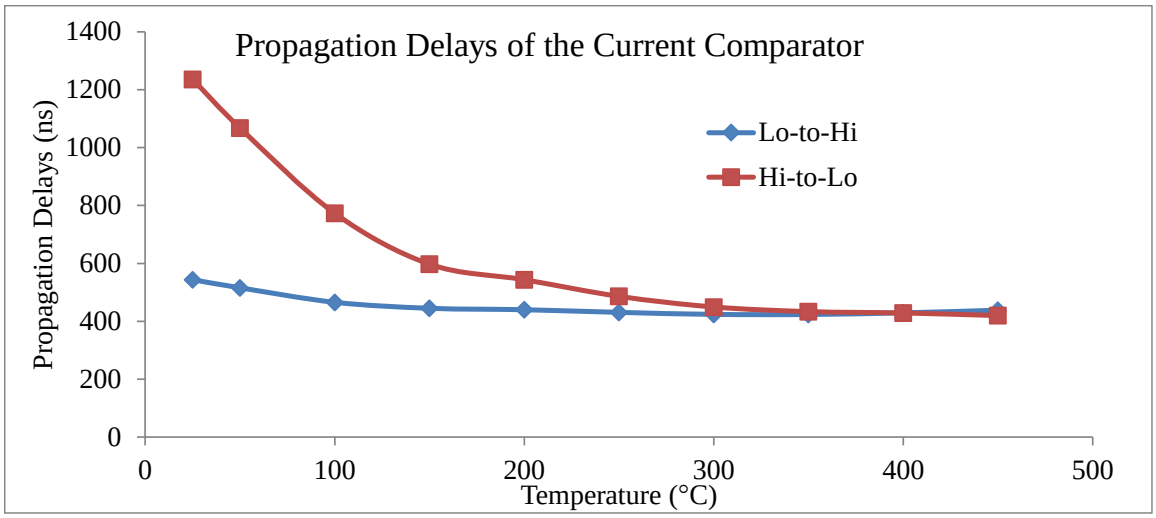
The measured results show a slightly better performance in terms of the fall time, but slower performance for the rise time and the propagation delays. Besides the devices, that slowness can also be attributed a little to the extra capacitances that are introduced in the real world test setup. Overall though, other than the hysteresis voltage anomaly at 200 °C and slower response at low temperatures, the comparator meets the design specifications very well.

5.3.3 Current Comparator Test Results

The current comparator is similar to the voltage comparator in pin configuration with the exception of using only one bias current instead of two. The external currents in the voltage comparators are used to bias the complementary input stages and the post decision differential amplifier stage. Since the current comparator only uses the post decision amplifier stage, only one biasing current is used. The rise and fall times of the current comparator over a temperature range of 25 °C to 450 °C are shown in Fig. 5.25 (a). The propagation delays are shown in Fig. 5.25 (b).



(a)



(b)

Fig. 5.25. Timing properties of the current comparator (a) Rise and fall times and (b) Propagation delays.

The current comparator was tested by setting one of the input currents to a fixed value of 20 µA, while the other current was switched from 10 µA to 30 µA. The rise and fall times of the current comparator are higher than the voltage comparator. Since the positive feedback decision making circuit and the post decision output stage are the same for both the comparators, the timing difference is originating from the input stage. The gain of the transconductance amplifier stage is responsible for the faster response in the voltage comparator. The current comparator does not

have an input amplifier stage, and the lack of this is even more prominent in the case of the propagation delays where the low to high delays are around 500 ns for the whole temperature range, while the high to low delay is 1.2 µs at 25 °C. The delay decreases with temperature as FETs become faster, but never falls below 500 ns. Given the maximum switching speed of 100 kHz for the flyback converter controller, where this current comparator is being used, a 1.2 µs delay, though undesirable, is still acceptable for the operation it was intended for. The measured parameters of the current comparator are compared to the simulated (with TF models) results in Table 5.5. The measured results show a slower current comparator.

Table 5.5. Comparison of Simulated and Measured Parameters of the Current Comparator

Parameters	Rise time (ns)		Fall time (ns)		Lo-to-Hi Prop. delay (ns)		Hi-to-Lo Prop. delay (ns)	
Temperature	*Sim.*	Meas.	*Sim.*	Meas.	*Sim.*	Meas.	*Sim.*	Meas.
25 °C	*23.9*	75.4	*15.2*	46.7	*543*	499	*780*	1236
100 °C	*18.9*	52.2	*11.5*	41.4	*465*	447	*659*	773
200 °C	*20.3*	46.3	*15.4*	40.9	*440*	454	*631*	543
300 °C	*42.8*	44.4	*16.2*	40.8	*423*	461	*650*	449
400 °C	---	45.1	---	41.8	---	429	---	429

The operational transconductance amplifier, the voltage comparator and the current comparator were tested over a wide temperature range and characterized to ensure that they would meet the requirements of the systems designed in this project. Results of the voltage comparator from 25 °C to 450 °C have recently been reported in [103]. The OTA and the voltage comparator

are quite extensively used in data converters and the signal processing of the flyback controller, while the current comparator is only used in the decision stage of the flyback controller.

5.4 Data Converter Test Results

The 8-bit ADC and DAC were packaged in the 68 pin LCC package and mounted on the Rogers-45 board for testing. The high number of power and I/O pins made it unfeasible to test fully on the probe station. Unlike the circuits described so far in this chapter, the data converters used digital I/O pads. The digital input pads, used in the 8-bit R-2R ladder DAC, include a buffer that is powered by the pad ring VDD and VSS (referred to as VDDIO and VSSIO). The digital output pads on the ADC use a buffer chain of four differently sized inverters designed specifically to drive a load capacitance of 10 pF. The locations of the ADC and DAC are shown in Fig. 5.26.

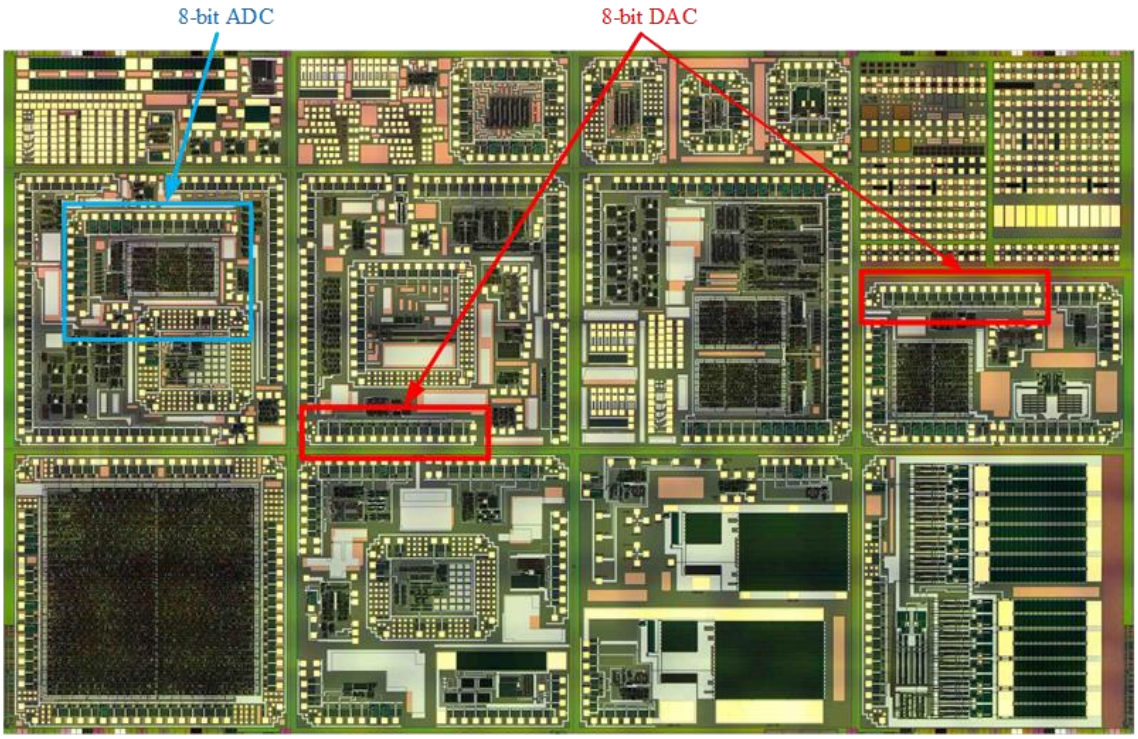


Fig. 5.26. Locations of the DAC and ADC on the full reticle.

5.4.1 Measurements on the R-2R DAC

The pins on the digital-to-analog converter are the following

- Power and ground pins (AVDD and AVSS), buffer current bias pin (IBIAS)
- Eight input digital bits (B7 – B0)
- Reference or full scale voltage (VREF), and output voltage pin (VREF)
- Pad ring power and ground pins (VDDIO and VSSIO)

The R-2R DAC was tested by changing the input digital pins to cycle from a code of 0 to 255. An Altera DE2 FPGA board was programmed to change the bits accordingly. The outputs of the FPGA board were then level shifted from 5 V to 15 V to provide inputs to the SiC DAC. The clock frequency of the FPGA was set to a fairly low value of 800 Hz in order to properly measure the DC non-linearity errors.

A full conversion range for the DAC at different temperatures is shown in Fig. 5.27. The DAC conversion graph shows considerable non-linearity at the lower temperatures, where there are significant jumps at the major transition points (MSBs turning from 0 to 1). The linearity improves as temperature increases. This non-linearity is a product of the resistance in the switching FET and the process resistors used in the DAC. As has been observed in previous measurements, the FETs tend to act slower, i.e. with a higher r_{dson} at lower temperatures. The R-2R ladder DAC ideally assumes a switch resistance of zero. Any switch resistance adds non-linearity in to the circuit performance – the higher the FET resistance, the more the non-linear error. As temperature increases not only does the FET resistance decrease but the high sheet resistance poly resistor also increases in value. Hence, the FET resistance has less of an effect on the DAC conversion which looks much more linear at 400 °C.

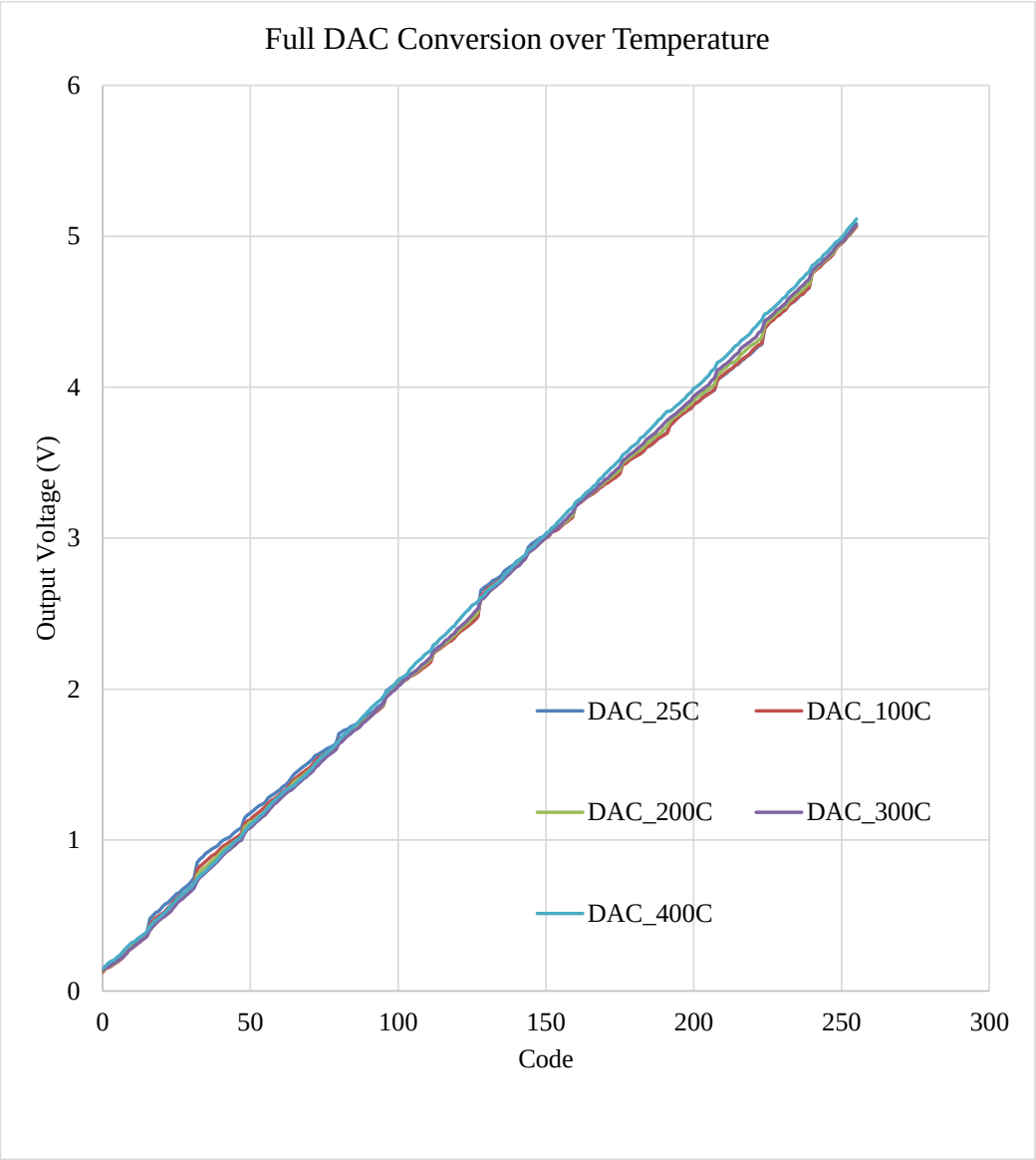
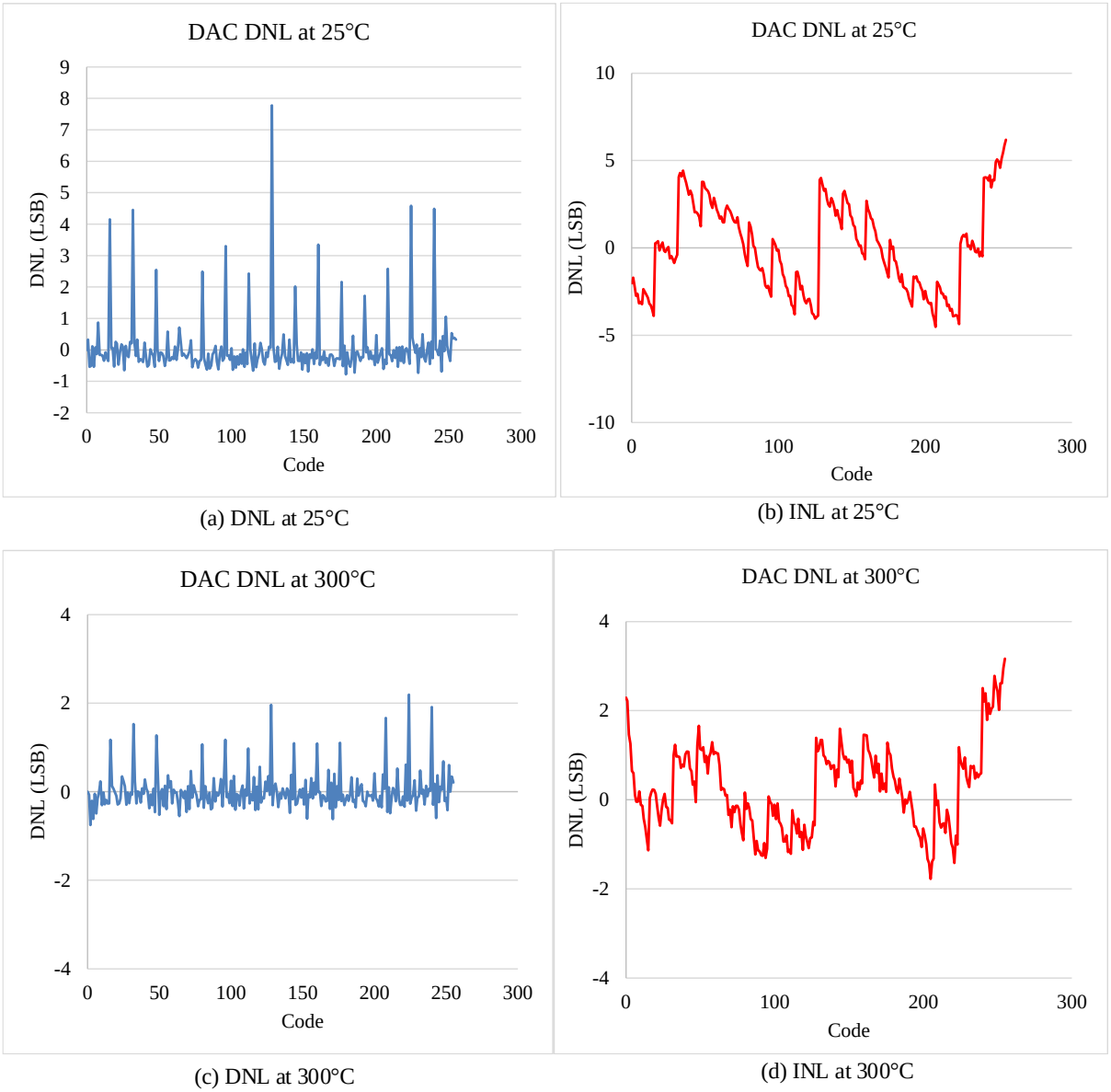


Fig. 5.27. Full conversion range of the DAC over temperature.

The DAC is limited in its output at the lower end due to the output voltage limitation of the OTA used in a voltage buffer configuration on the output of the DAC. The effect of the non-linearity can be best understood by looking at the DNL and INL curves for the DAC at different temperatures. In Fig. 5.28, the DNL curve at 25 °C shows a maximum value of 7.7 LSB, while at 300 °C it is only 2.2 LSB. Similarly, with offset correction the INL at 25 °C ranges from -4.5 LSB to 6.2 LSB, while the INL at 300 °C ranges from -1.8 LSB to 3.2 LSB.



(a) DNL at 25°C

(b) INL at 25°C

(c) DNL at 300°C

(d) INL at 300°C

Fig. 5.28. Non-linearity errors of the DAC over temperature (a) DNL at 25 °C, (b) INL at 25 °C, (c) DNL at 400 °C and (d) INL at 400 °C.

The INL and DNL are measured against the best fit curve according to the DAC response. The performance of the DAC improves significantly over temperature. A brief summary of the DAC performance over temperature is give in Table 5.6. The simulated results of the DAC (Table 4.6) show a maximum DNL of 2.4 LSB and a minimum INL of -1 LSB for TF models.

Table 5.6. DAC Test Results Summary

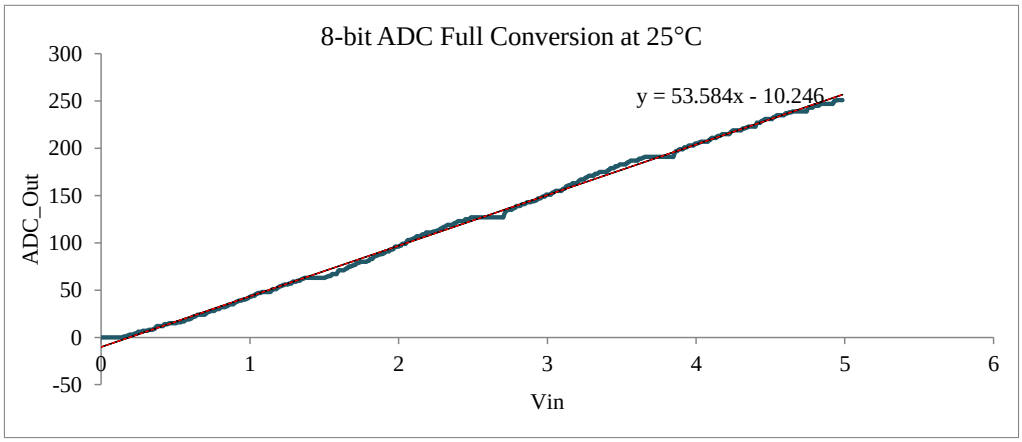
Parameter	DNL (LSB)		INL (LSB)		Offset Error (LSB)	Gain Error (LSB)
Temperature	Min	Max	Min	Max		
25 ℃	-0.8	7.8	-4.5	6.2	9.2	6.2
100 ℃	-0.7	6.3	-3.4	5.6	7.3	5.6
200 ℃	-0.8	3.9	-2.8	4.2	6.2	4.2
300 ℃	-0.7	2.2	-1.8	3.2	4.8	3.2
400 ℃	-1.0	1.2	-0.9	2.7	5.9	2.7

5.4.2 Test Results of the 8-bit ADC

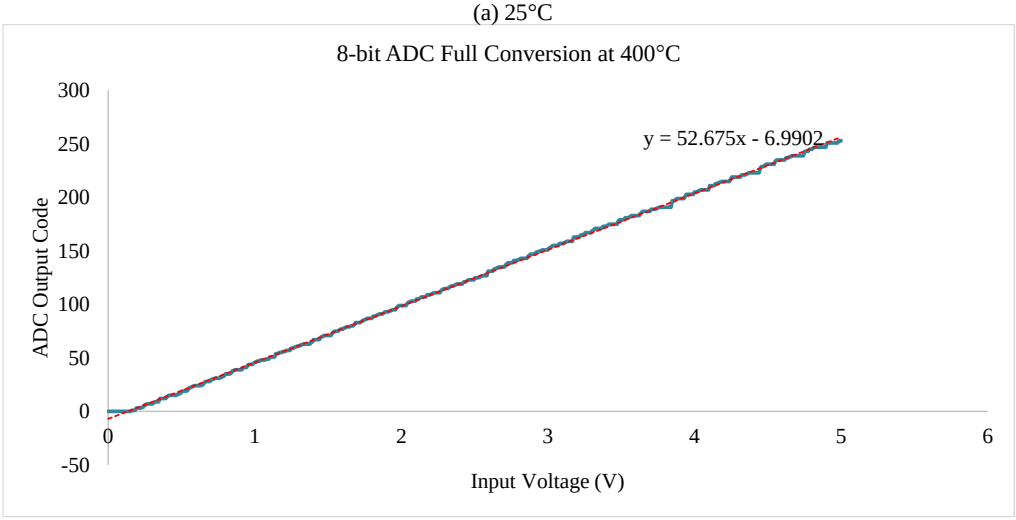
The successive approximation register ADC uses the 8-bit DAC, the voltage comparator and a digital control circuit to convert an analog voltage into an 8-bit digital code in ten clock cycles. The default clock speed chosen for these tests was 500 kHz. To test the circuit, a very slow ramp voltage was applied to the input of the ADC. The outputs were recorded with the mixed-signal oscilloscope. The ramp input and the clock were supplied by two channels of the arbitrary waveform function generator. The pins associated with the ADC are

- Circuit power and ground pins (VDD and VSS), pad ring power and ground pins (VDDIO and VSSIO)
- Input voltage (VIN) and reference/full scale voltage (VREF)
- Bias current pins for the comparator (IBIASP and IBIASN)
- Clock pin (CLK), reset pin (RST), enable pin (EN) and valid pin (Valid)
- Eight output bit pins (D7 – D0)

The clock is applied to the circuit first. The reset pin is initially held to high, disabling the whole circuit. When the reset pin goes low and the enable pin goes high, the conversion begins. On the ninth clock cycle the 'Valid' pin goes high to signal the availability of the output. On the tenth cycle all the values are reset to zero. The digital probes of the mixed-signal oscilloscope were used to observe the digital output nodes D7-D0 and Valid. When Valid went high the corresponding value of D7-D0 was recorded in an event table. The full conversion range for 25 °C and 400 °C are shown in Fig. 5.29.



(a) 25°C



(b) 400°C

Fig. 5.29. Full conversion range of the ADC at (a) 25 °C and (b) 400 °C.

Similar to all the other circuits tested on the Vulcan II run the performance of the ADC improves over temperature considerably. As temperature goes higher, the following improvements are seen in the performance of the ADC - the initial offset gets lower, the full range conversion graph is more linear and there are a lot fewer skipped codes.

A look at the DNL and INL curves for the ADC at the different temperatures can illustrate the improvement of linearity over temperature. Fig. 5.30. Both the DNL (11 LSB at 25 °C) and INL (-7.5 to 7.5 LSB at 25 °C) improve considerably at 400 °C (4 LSB and -3.2 to 2.8 LSB).

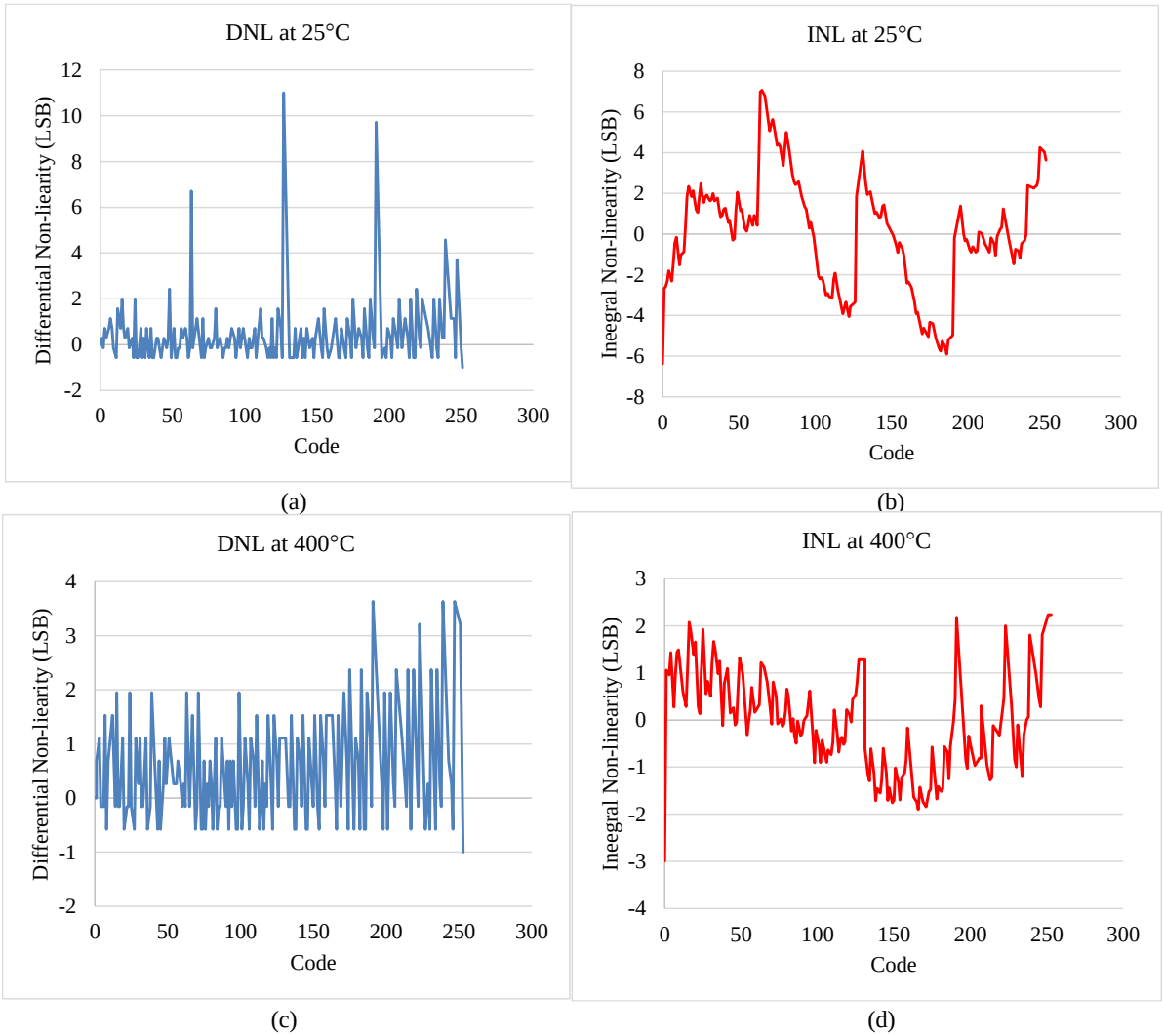


Fig. 5.30. ADC errors (a) DNL and (b) INL at 25 °C, (c) DNL and (d) INL at 400 °C.

The improvement of the ADC over temperature is in part due to two circuits – the DAC which has already been shown to be more accurate at higher temperatures, and the voltage comparator which is more sensitive and faster at higher temperatures.

The test results of the 8-bit ADC are summarized in Table 5.7. The DNL, INL, offset and gain errors have been calculated in reference to the best fit curve of the ADC at different temperatures. The simulated value for the TF models showed a DNL range of -1 to 0.1 LSB and INL range of -0.6 to 0.8 LSB over all temperatures.

Table 5.7. ADC Performance Parameters over Temperature

Parameter	DNL (LSB)		INL (LSB)		Offset Error (LSB)	Gain Error (LSB)
Temperature	Min	Max	Min	Max		
25 °C	-1	11	-6.4	7.1	-10.2	5.8
150 °C	-1	6.2	-4.1	6.1	-1.8	3.8
200 °C	-1	6.9	-3.8	4.7	-5.1	6.9
250 °C	-0.5	4.7	-3.1	3.2	-4.7	4.8
300 °C	-1	4.4	-3.2	2.8	-7.4	2.7
350 °C	-0.6	4.4	-3.5	2.1	-7.9	2.7
400 °C	-0.6	3.6	-3	2.2	-7	2.6

The SAR ADC performs significantly better in terms of linearity at higher temperatures. Given the observations made on the DAC, it can be confidently stated that if the performance of the DAC is improved by decreasing the switching resistance, the performance of the ADC can be significantly bettered at lower temperatures.

The ADC was also tested for an 8 V full scale reference, as well as being evaluated as a 6-bit ADC. Since these were not part of the design specifications of the ADC, a full characterization of it under these conditions is not shown here. The full conversion range along with the DNL and INL values for the full scale 8 V at 400 °C and a clock frequency of 500 kHz is shown in Fig. 5.31.

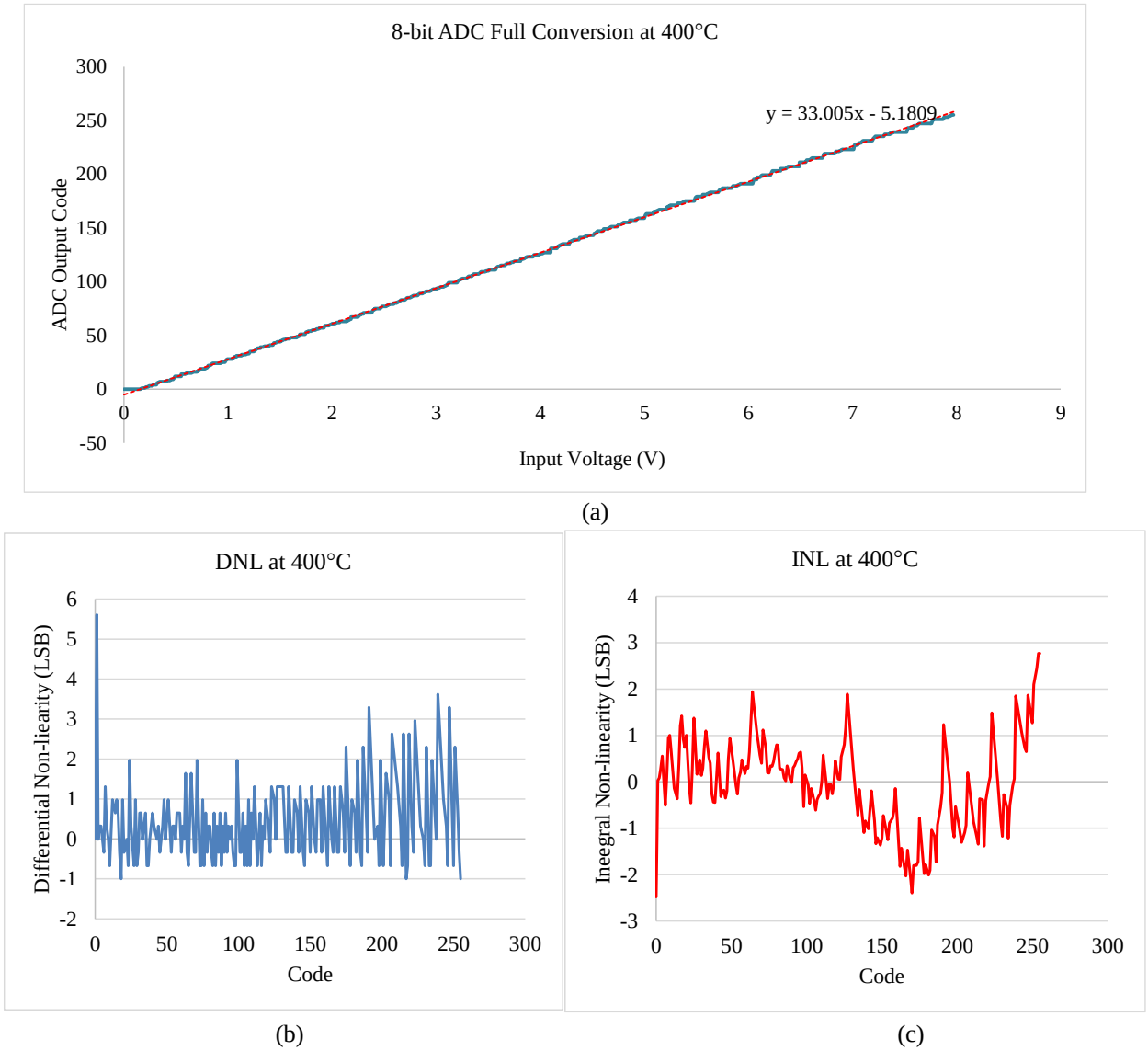


Fig. 5.31. Performance of the 8-bit ADC at 400 °C with 8 V full scale – (a) ADC conversion over full range, (b) DNL and (c) INL.

The performance of the ADC with 8 V full scale is not too dissimilar from the 5 V full scale ADC in terms of linearity. The offset error of the ADC in this configuration at 400 °C is -5.2 LSB and the gain error is -3.6 LSB, which is also comparable to the 5 V range. The big difference is of course the LSB, which is around 19-19.5 mV for the 5 V full scale and 30.3 mV for the 8 V full scale. Thus, although a higher full scale range increases the input range, it suffers from less input sensitivity.

The precision of the ADC is vastly improved, as should be expected, when it is treated as a 6-bit converter. The results, shown in Table 5.8 indicate an ADC than can potentially work to two bits of precision over all temperatures.

Table 5.8. Performance of the ADC as a 6-bit Converter over Temperature

Parameter	DNL (LSB)		INL (LSB)		Offset Error (LSB)	Gain Error (LSB)
Temperature	Min	Max	Min	Max		
25 °C	-1.0	3.0	-2.1	1.8	-3.2	3.6
150 °C	-0.5	1.0	-2.6	1.0	-1.0	2.4
200 °C	-0.4	1.0	-0.2	2	-3.8	2.2
300 °C	-1.0	1.0	-0.4	2.2	-2.1	2.3
400 °C	-0.8	0.8	-1.0	0.2	-2.1	2.5

5.4.3 Non-idealities of the SiC Data Converters

The differential and integral non-linearity errors that are prominent at lower temperature lessen as the operation temperature increases. The source of this non-linearity can be traced to the R-2R resistor ladder. The transmission switches in the resistor ladder add non-ideal resistances to

the R-2R chain. Ideally the switch resistance should be zero but the SiC switches used in the data converters are not of zero resistance and add non-linearity into the circuit.

As temperature increases two things happen at the same time – the resistance of the high sheet poly resistor increases while the SiC FETs become faster, and thus, have a smaller on-resistance. The combined effect of the two is a lessening of the significance of the finite resistance of the switches in the R-2R ladder. At higher temperatures, the data converter outputs are hence significantly improved. Since the SAR ADC uses the R-2R DAC, any non-linearity stemming from the DAC affects the ADC as well.

The value of the LSB for the data converters was set at 19 mV to allow for a high comparator offset, which at this stage of the SiC technology process is prone to be high. As the SiC fabrication process develops and statistical models are available, lower LSBs can be attempted. This can lead to data converters with higher resolutions which can be used in aerospace, industrial, and deep earth drilling applications. As they are right now, the data converters presented here, although designed for 8 bit data conversion and satisfactorily functional up to 400ºC, will be better suited as 6 bit data converters for the full temperature range.

- Decrease the LSB of the data converter – the current selection for LSB (19 mV) was partly done to guard against high offset in the comparator and the buffer op amp. However, as the fabrication technology improves and statistical models are developed lower offsets can be expected, and lower LSBs will also be a possibility
- Use bigger switch FETs and larger poly resistors – bigger switch FETs will lead to smaller switch resistance, and bigger poly resistors will further lessen the significance of the switch FET. Hence, linearity of the DAC and in turns the ADC will improve.

The R-2R DAC has recently been published in [104]. The literature reports two 8-bit data converters for extreme wide and high temperature applications – a radiation hardened 8-bit SiGe BiCMOS DAC for -180ºC to 120ºC operation [105], and an 8-bit DAC in 130 nm bulk Si CMOS for 225ºC operation [106]. These provide the closest comparison to the data converter developed and are similar in resolution. The SiGe DAC has a linearity of ±0.2/0.3 LSB at 27ºC and ±0.6/0.9 at -180ºC. The performance of the SiGe DAC is better than the SiC DAC at room temperature, but at the ends of the range the performances are not too dissimilar (-1.0 / 2.7).

The motive of the bulk Si CMOS DAC at 225ºC was to design a temperature insensitive op amp and the accuracy of the data converter was not the target for the endeavor. The SiC data DAC offer a superior solution to high temperatures over 250ºC and at this point the only solution at temperatures over 300ºC.

5.4.4 Temperature Testing for Different Circuits

At this juncture, a small comment should be made on the different temperature ranges the circuits were tested to. Since all there was no definite temperature to test the circuits up to, the circuits were taken from 25ºC to up to the temperature they were deemed to be safe. The signal processing circuits tested on the probe station were limited due to the range of the Semiprobe probe station. The first circuit tested on packaged was the comparator and was taken up to 540ºC in two cycles of heating and cooling. However, as temperature is increased if differential pair gates are not biased equally, it is highly likely that the gate interface traps will not be released uniformly and the recombination won't be similar either. Hence, large offsets are introduced in various parts of the circuits which led to the breakdown of the comparator circuit itself. Hence, all the other circuits – the amplifier and the data converters were tested up to only 400ºC, so that future testing and characterization could be facilitated.

5.5 The Flyback Controller Measurements

The flyback controller was tested as a demonstration of the current-mode signal processing scheme. The main goal was to test the controller by itself from front to back. The implementation of the controller in the full flyback converter system, although very much desirable, was a secondary goal. The full flyback controller can be divided into three major portions:

- Linear voltage to current converter circuitry,
- The mathematical section that uses current squaring and multiplying circuits,
- The final decision making circuit that signals from the previous stages to determine whether or not to turn on the FET.

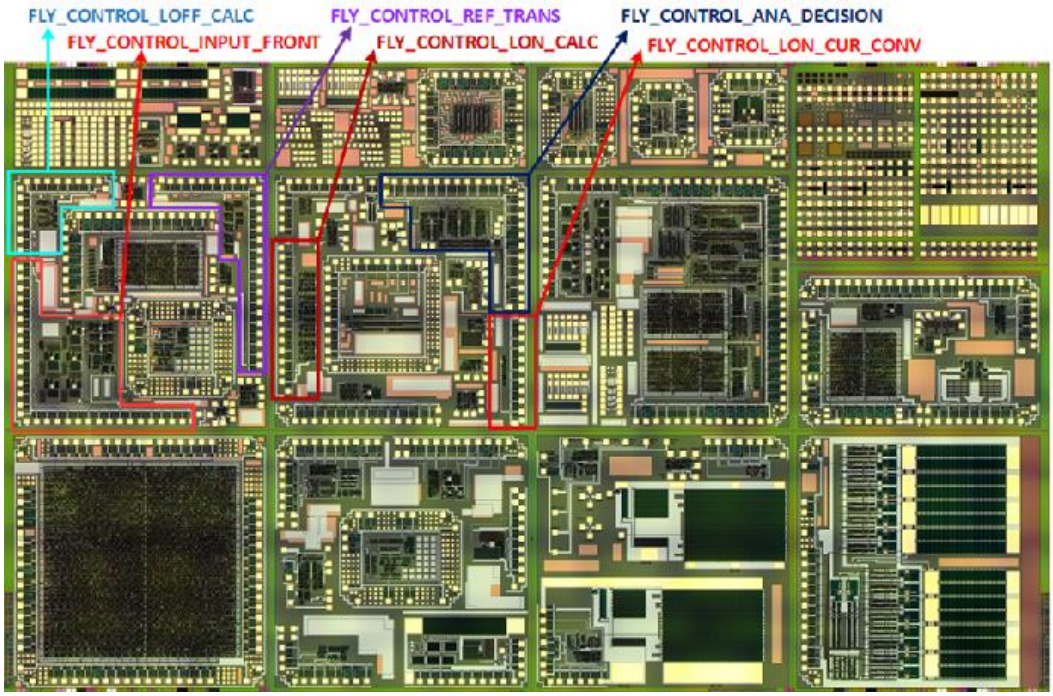


Fig. 5.32. Locations of the flyback controller circuits on the full reticle.

5.5.1 Input Frontend Circuitry

The linear voltage to current conversion or the input frontend stage consists of voltage to voltage converters to condition the sensor output voltages to fit the input of the linear V-to-I

converters. This includes five closed loop non-inverting amplifiers that provide voltage level shifting to the sensor voltages for the output and panel input voltages, V_{OUT} and V_{CC}, as well as the output and transformer currents, I_{OUT}, I_{PRM} and I_{SEC}. The operational transconductance amplifier characterized in section 5.3.1 was used to implement the non-inverting amplifiers. The OTAs were biased by an external current of 100 µA. The sensor voltages were level shifted by using a DC input reference voltage. The linear V-to-I converters convert the conditioned sensor voltages into linear currents. The bias current for the linear V-to-I converter was set to 16 µA.

The bias currents and voltages used in the input frontend circuits were set externally using potentiometers. The SiC reticle includes a voltage and current translator circuit that can take two voltage inputs and four currents and translate them to bias all the other circuits in the design. However, on the test board a provision was available to bias each of the circuits independently. This afforded more control at the input stage and was used throughout the testing phase.

The voltage conditioning and current converting circuits for the system voltage sensor outputs (V_{CC} and V_{OUT}) were set to take an input of 0 V to 5 V and convert the input voltage into a linear output current from 0 µA to 30 µA. The current sensor output range is 2.5 V to 4.5 V. Hence, the voltage conditioning and current conversion circuits used for the current sensor outputs are designed to convert an input of 2.5 V to 4.5 V to an output current of 0 µA to 30 µA. However, due to the transformer, the currents on the secondary side had to multiplied by six, while another provision was set in the system to scale the currents by a factor of three to provide for control with lower output capacitances or current sensors with less current to voltage conversion gain.

The outputs of the current converter circuits are shown in Fig. 5.33. The output current for the output voltage sensor VOUT is shown in Fig. 5.33 (a). The output current starts at 0 V input and reaches a maximum of 36 µA for an input of 5 V.

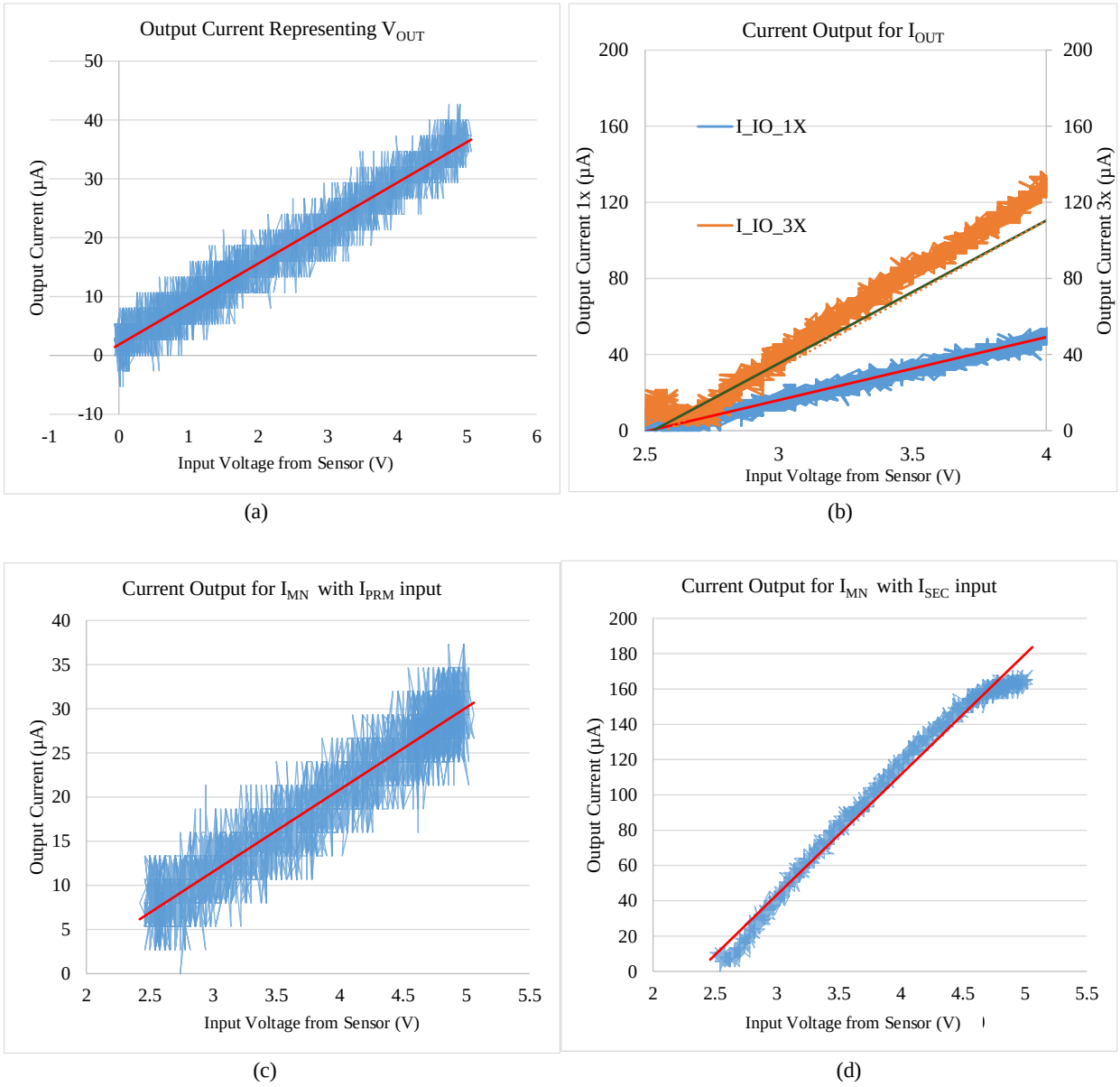


Fig. 5.33. Current converter circuit outputs from the input frontend (a) Current output for the V_{OUT} sensor, (b) Current output for I_{OUT} with 3X and 1X output, (c) I_{MN} output with primary current sensor inputs, and (d) I_{MN} output with secondary current sensor output.

The output current is measured as voltage across a 30 kΩ resistor, and then divided by the resistor to calculate the current. The sampling noise associated with the oscilloscope does not allow for a smooth output, hence, a trend line is added to the graphs to denote the output characteristics more clearly. Fig. 5.33 (b) shows the linear converted output currents for the I_{OUT} sensor with the regular (1X) and three times scaling (3X). The maximum currents of the two options are 120 µA and 40 µA which are expected.

The graphs in Fig. 5.33 (c) and (d) show the I_{MN} output current with the input from the primary side sensor, I_{PRM}, and secondary side current sensor, I_{SEC}, respectively. The current output of the secondary side current is multiplied by six to represent the transformer turn ratio. The output saturates at a value of around 160 µA. The I_{MN} current is 25 µA for an input voltage of 4.5 V on the primary side sensor, while it is 150 µA for an input voltage of 4.5 V on the secondary side sensor. Thus, the six times scaling factor is achieved for the primary and secondary sides.

The outputs of the frontend circuit show an expected relationship – although the output currents have higher conversion gain than the simulation results. The output current for a rated output voltage of 4.4 V is 33 µA, which is higher than the target of 20 µA. This is due to the faster fabricated devices than the TT models the circuits were simulated with. However, since the process shift is over the whole wafer, the quicker devices in the comparators mean that it can operate at higher input current ranges as well. The final input to the input frontend is '*V1N*', a voltage that would translate to a normalized value of 1 in the control Eqs. (3.19) and (3.20). This voltage is set to 6.9 V to generate the rated output current of 33 µA to calibrate the system with the output voltage conversion behavior.

The output currents of the linear V-to-I converters are fed to the two mathematical circuits, the LOFF calculation circuit and LON calculation circuit. The test results of these circuits are described in the next section.

5.5.2 Mathematical Circuits Operation of the Flyback Controller

The circuits used for mathematical operations are the L_{OFF} calculation circuit, the L_{ON} calculation circuit and the L_{ON} current conversion circuit.

5.5.2.1 L_{OFF} Calculation Circuit Test Results

The L_{OFF} calculation system converts the input currents into squared outputs. The outputs of the current squaring circuits are also measured across load resistances of 30 kΩ. The outputs of the current squaring circuits are supplied to the inputs of the L_{OFF} current comparator of the flyback controller. The normalized currents in the L_{OFF} calculation circuit are V_{ON}, I_{ON}, V_{1N} and $I_{MN\text{-}ON}$. The outputs for the V_{ON} and I_{ON} current are shown in Fig. 5.34.

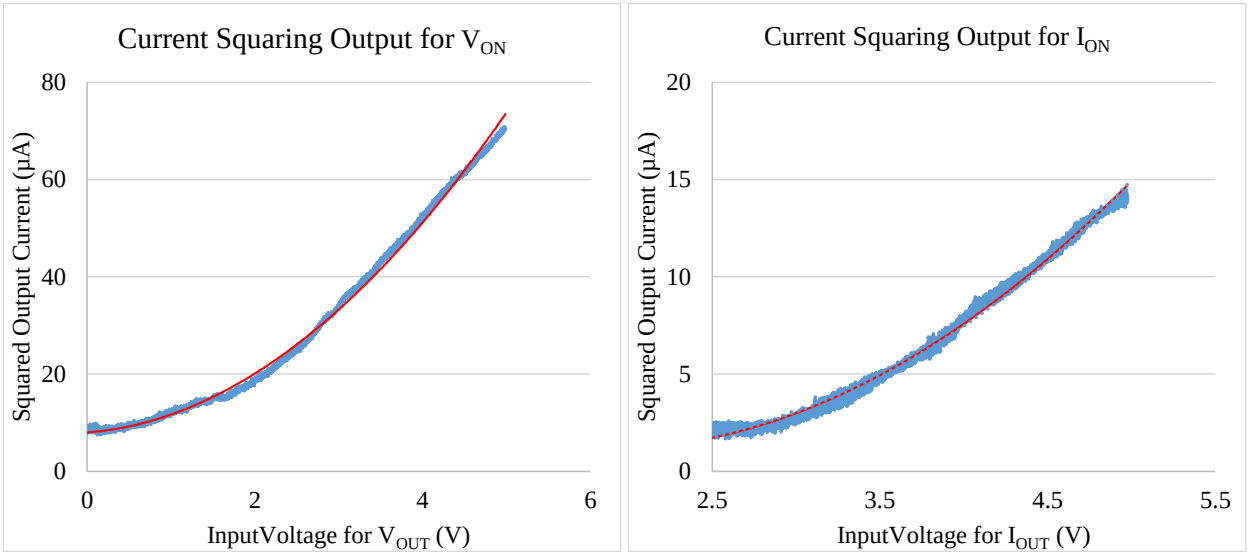


Fig. 5.34. Outputs of the current squaring circuits for (a) Normalized output voltage V_{ON} and (b) Normalized output current I_{ON}.

The 'averaging' function on the Acquire menu was turned on for the measurements of the current squaring circuits in the mixed-signal oscilloscope. Hence, the graphs for the current squaring circuits are much less noisy. The trend line for the squaring circuit (in red) is shown with the output (in blue). The output of the squaring circuit for the V_{OUT} sensor goes from 10 µA to 70 µA for an input range of 0-5 V. The output for the current squaring circuit for I_{OUT} goes from 2.5 µA to 14 µA for an input range of 0-5 V. The offset currents associated with the squaring circuits for the system voltage and current quantities are 10 µA and 2.5 µA respectively. Since the positive and negative inputs of the comparator use one each of the voltage and current entities, the offsets cancel out in the comparison. The outputs of the current squaring circuits for the two other entities, not shown here, show similar behavior.

5.5.2.2 L_{ON} Calculation Circuit and Conversion Circuit

The L_{ON} calculation system has four multiplier circuits – three of them are used to calculate the values for the $v_{on}*v_{ccn}$, $v_{on}*v_{1n}$ and $i_{mn}*i_{on}$. A fourth multiplier circuit is used to generate an offset current to compensate for the current comparators. The outputs of the current multiplier circuits are fed into the L_{ON} current conversion circuit mirrors that convert the current source outputs to current sink outputs that are then connected to the L_{ON} comparator on the flyback controller.

To test the *VCxVO* current multiplier, the sensor voltage for V_{OUT} was set to a fixed value 4.0 V and an input ramp voltage was applied for V_{CC}. The output current was calculated by measuring the voltage across a 30 kΩ resistor. The voltage on V_{OUT} was then changed to different values and the output currents were measured again. The output currents for *VCxVO* with different voltages at V_{OUT} are plotted in Fig. 5.35.

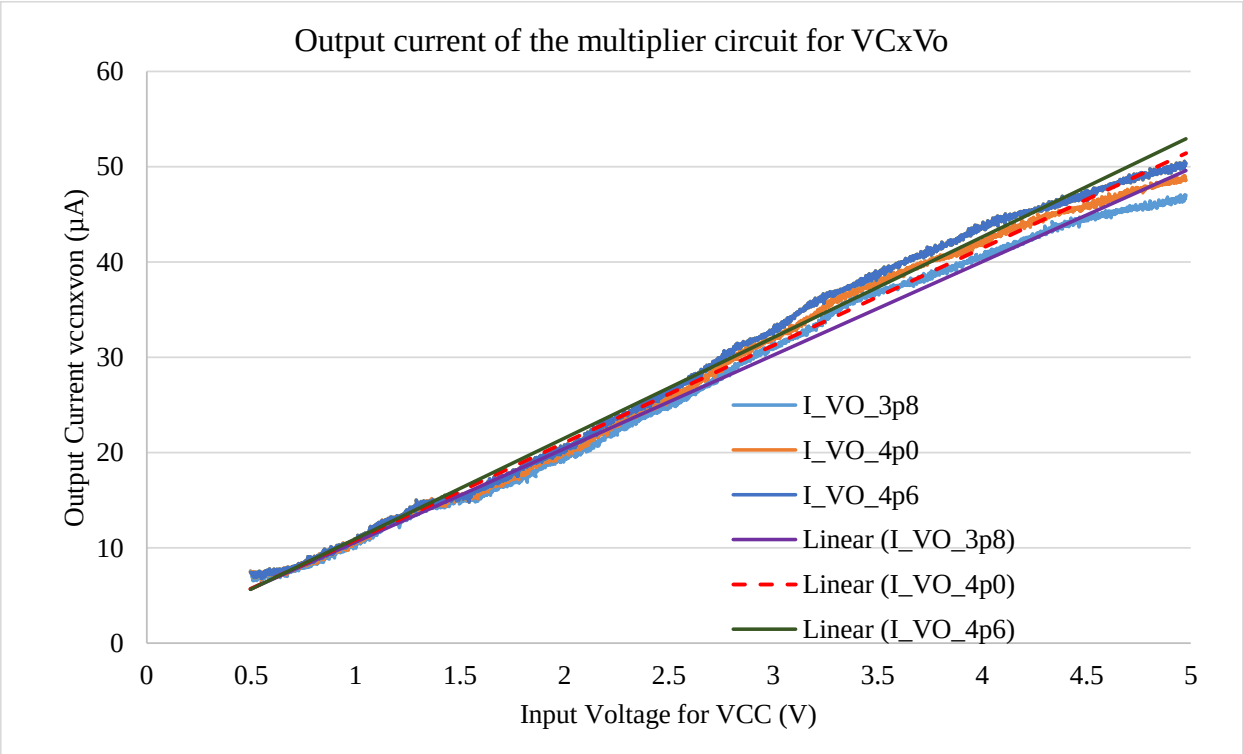


Fig. 5.35. Multiplier circuit outputs for $V_C \times V_O$.

The output currents for the different values of V_{OUT} show higher slope as the voltage on V_{OUT} is increased. This can be seen by plotting the trend line of the outputs. The trend lines all start at the same point before increasing at different slopes. The output currents go from 0 µA to 50 µA over the full range of inputs.

The output current for the *IMxIO* multiplier circuit is plotted in Fig. 5.36. The voltage for the I_{SEC} sensor is swept with a ramp voltage while the sensor voltage for I_{OUT} is held constant during the measurements. The output currents have a higher slope when the sensor voltage of I_{OUT} is held at a higher voltage.

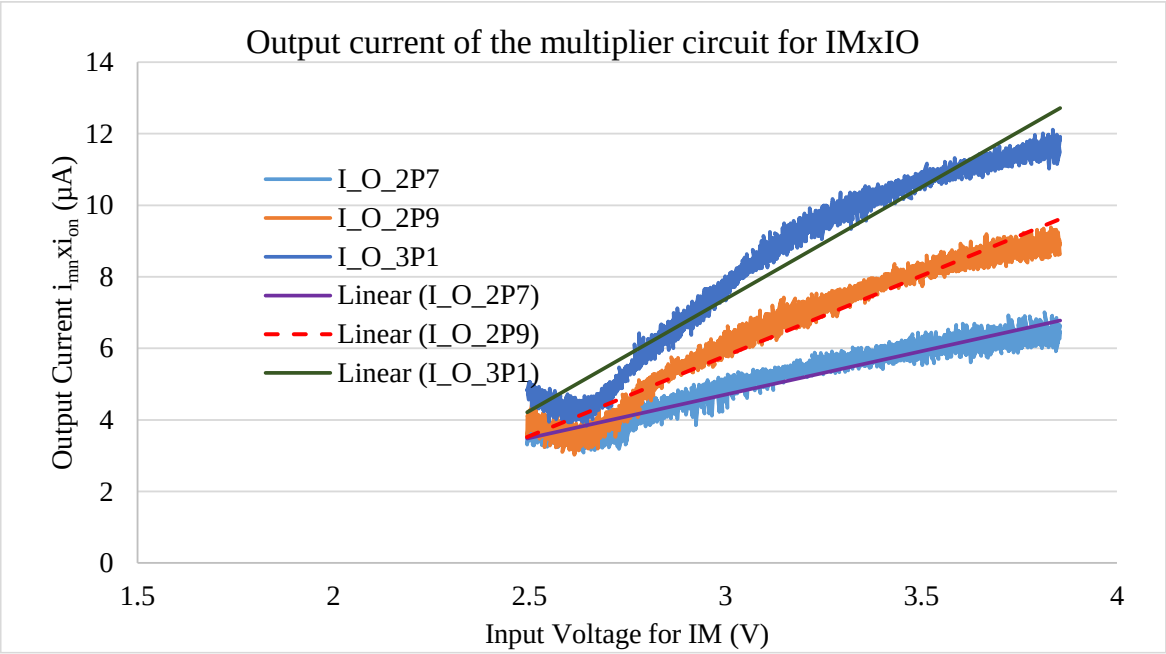


Fig. 5.36. Output currents of the IMxIO circuit over different IOUTs.

The voltage for I_{OUT} was set at 2.7 V, 2.9 V and 3.1 V for the three input sweeps. The slope of the output current gets higher as the sensor voltage is set at higher voltages. The trend lines of the output currents show the higher slopes more clearly.

5.5.3 Flyback Controller Test Results

The flyback controller has the following features:

- Current comparators to determine the switching FETs based on the L_{OFF} and L_{ON} calculation circuit current outputs.
- Voltage comparators to determine if the output voltage V_{OUT} is over or under the rated value and if the primary current I_{PRM} is over the maximum current. When V_{OUT} is under the rated value, the L_{OFF} comparator output is selected, otherwise the L_{ON} comparator output is selected.

- The controller runs on a 1 MHz clock and is initialized with the outputs set to zero by tying the reset pin (RST) to high.
- A provision is set to allow for inputs from a digital controller. The analog controller is selected by setting the DIGANA pin to zero.
- The comparators in the controller are biased by external voltages and currents generated by the combination of resistors and potentiometers.

The controller was tested separately for the L_{OFF} and L_{ON} comparators. The following are the conditions for choosing the L_{OFF} and L_{ON} controller outputs.

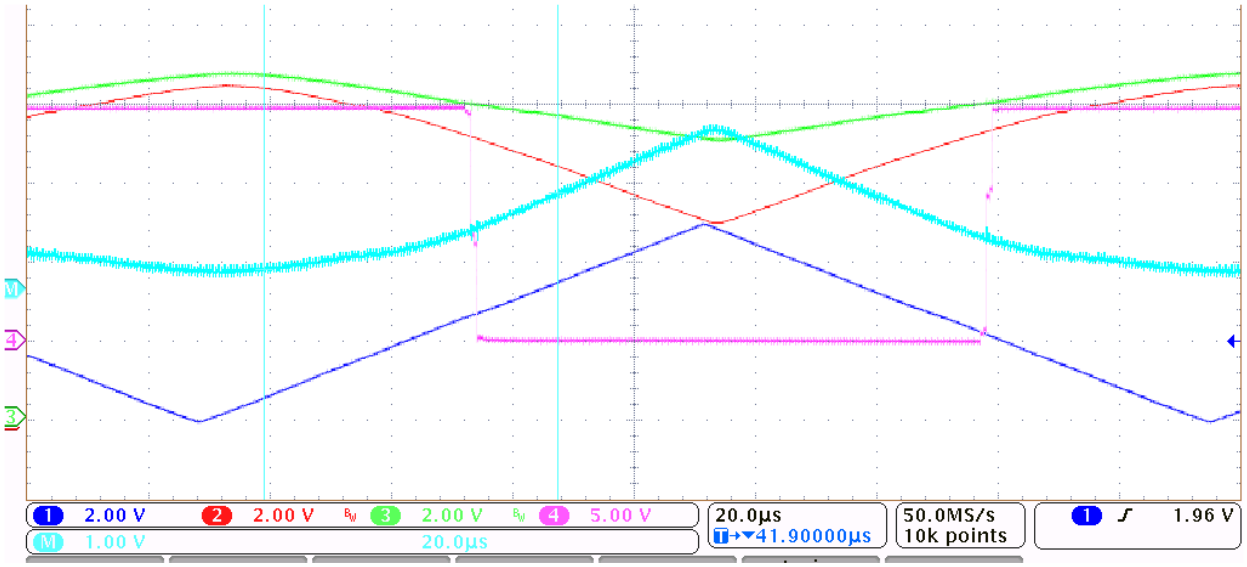
- If $v_{on} < 1$, i.e. $V_{OUT} < 4.4$ V choose the output of the L_{OFF} comparator
- If $v_{on} > 1$, i.e. $V_{OUT} > 4.4$ V choose the output of the L_{ON} comparator
- When primary current is over 15 A, i.e. $V_{IPRm} > 3.5$ V, FET output is zero

5.5.3.1 Testing the L_{OFF} Controller

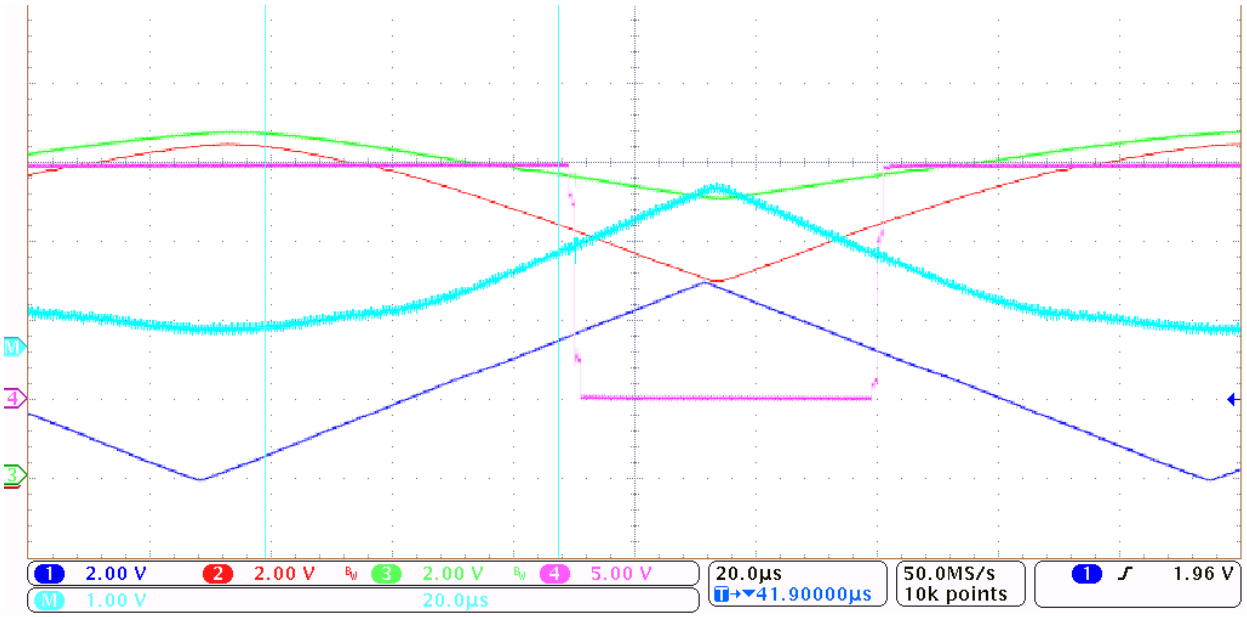
The LOFF controller is tested on the following conditions

- If, $v_{on}^2 + (i_{mn}-i_{on})^2 > v_{1n}^2 + i_{on}^2$, the output is set to low
- If, $v_{on}^2 + (i_{mn}-i_{on})^2 < v_{1n}^2 + i_{on}^2$, the output is set to high
- The currents for i_{on} and $(i_{mn}-i_{on})$ were set to zero by setting the sensor voltages for the current sensors to 2.5 V.
- The output voltage sensor, V_{OUT} was then supplied with an input ramp while the voltage V_{1N} was set to a fixed voltage. The FET drive output was then observed for different values of the reference voltage V_{1N}. The higher the value for V_{1N}, the bigger the duty cycle of the switching output would be for a fixed input ramp.

The output of the controller is plotted (in pink) with a ramp input on the sensor voltage of the system output voltage, V_{OUT}, and the rated voltage, V_{1N} set to 6 V and 6.5 V respectively in Fig. 5.37.



(a)



(b)

Fig. 5.37. Controller output with varying V_{OUT} with (a) V1N = 6 V and (b) V1N = 6.5 V.

The controller output has duty cycle of 55% for a rated reference value of V_{1N} set as 6 V. When the rated reference is increased to 6.5 V, the output pulse width increases to 73%. This relationship extrapolates to the point of 86.5% duty cycle with a reference rated voltage, V_{1N} of 6.9 V, and a V_{OUT} voltage of 4.35 V. These numbers are very close to the expected value from the input fronted measurements where a V_{OUT} value of 4.4 V corresponds to a V_{1N} value of 6.9 V.

The effect of the two other entities, i_{mn} - i_{on} and i_{on} were measured by setting the i_{on} and v_{1n} values to fixed values, and applying an input ramp to v_{on} for different values of i_{mn}. The value for i_{on} was set to 0 µA. As the value of i_{mn} is changed the duty cycle of the output decreases. The results show that as the value of i_{mn} goes higher, the duty cycle of the controller output decreases. A summary of the change in the duty cycle with the different values of V_{1N} and I_{MN} (comprising of I_{PRM} and I_{SEC} tied together) are shown in Table 5.9.

Table 5.9. Summary of Effect of the Voltage Sensor Inputs on L_{OFF} Duty Cycle

Effect of rated reference voltage, with i_{mn} = 0, and i_{on} = 0		Effect of magnetizing current, with V_{1N} = 7 V, and i_{on} = 0	
V_{1N} input (V)	Measured Duty Cycle	I_{MN} input (V)	Measured Duty Cycle
6.0	55%	2.5	87.5%
6.5	73%	2.7	86.1%
7.0	87.5%	3.0	81.4%

As expected from the control condition described earlier in this section, the measured duty cycle increases as the contribution of V_{1N} goes higher, and decreases as the contribution of I_{MN} goes higher. This verifies the operation of the L_{OFF} controller for switching the FET drive output.

5.5.3.2 Testing the LON Controller

The L_{ON} controller turns on when the output voltage V_{OUT} is over the rated voltage. In the case of the flyback converter that refers to an output voltage of 200 V and sensor voltage for the V_{OUT} to be 4.4 V. The L_{ON} controller operates on the following principles

- If, $v_{cn}*v_{on} + i_{mn}*i_{on} > v_{cn}*v_{1n} + i_{off}$, output is set low
- If, $v_{cn}*v_{on} + i_{mn}*i_{on} > v_{cn}*v_{1n} + i_{off}$, output is set high

The L_{ON} portion of the controller was tested by setting the sensor voltage for the supply V_{CC} to a fixed value of 3.7 V (reflecting an expected input of 27 V), and the sensor voltage for the output current I_{OUT} to 2.7 V, which in turn reflects an output current of 0.5 A. A ramp input was applied to the rated reference voltage, V_{1N} under the following two conditions.

- Sensor voltages for I_{PRM} and I_{SEC} were set to 2.5 V, thus eliminating the effect of $i_{mn}*i_{on}$ and i_{off} in the controlling equations. Then the duty cycle was measured for different values of V_{OUT} as V_{1N} was swept 0-5 V. The higher the value V_{OUT} was set, the higher the lower the duty cycle was expected to be.
- Sensor voltages from V_{OUT} was set to a fixed value of 4.5 V. And then the value for I_{MN} (I_{PRM} and I_{SEC} sensor inputs tied together) were set at different values. The higher the value for I_{MN} was set, the lower the duty cycle was expected to be.

Test measurements on the controller show the following

- For the first setup, when V_{OUT} was set to 4.5 V, the duty cycle was 16.8%, while when it was set to 4.2 V, the duty cycle was 14.7%

- For the second setup, as I_{MN} was set to values of 2.5 V, 3.0 V, 3.4 V, 3.6 V and 3.8 V. The corresponding duty cycles were – 16.85%, 16.82%, 15.72%, 14.72% and 14.01%. The effects of the current sensor terms are small due to the relatively low normalized values as can be observed from Table 4.10. Hence, the change in duty cycle is only observed for comparatively higher values of the current sensor voltages.

The flyback controller was verified to work over a range of inputs to the sensor voltages and showed expected behavior. The controller was tested on a PCB where the sub-circuits were connected to each other externally on the board. The verification of the controller from front to back paves the way for the implementation of an analog current-mode controller in SiC ICs.

5.5.4 Limitations of the Flyback Controller

The flyback controller when assembled together on a printed circuit board was found to be functional at relatively lower frequencies. There are two factors that must be addressed before this controller can be developed as a standalone chip for DC-DC power converters. These are the frequency response of the controller and the error and noise propagation through the controller. The first point is discussed with measurement graphs from the mixed-signal oscilloscope while the second point is discussed with standard deviation numbers from the signal processor circuits.

5.5.4.1 Speed Limitation of the Flyback Controller

The flyback controller is divided into the following main stages – the voltage to voltage converter, the voltage to current converter, the squaring and multiplying sections, current transforming current mirrors and the final control circuit. The first stage contains the OTA whose measurements are described in 5.3.1. The OTA was found to have a lower phase margin than was expected. And the phase margin being over the absolute minimum 30° meant that there was no big

risk of positive feedback being introduced to the system, it did mean that at higher frequency, even in a buffer amplifier system, the output would lag the input by a little bit. Thus, at the very onset there is the possibility of the signal being delayed that may reduce the speed of the system.

The controller, in its present form, has all of its sub systems connected to each other on a printed circuit board. Although care was taken to keep the routes as short and efficient as possible, the presence of the measuring resistances and test points all throughout the board adds to the capacitance of each path. The current output of each circuit was measured as the differential voltage across a medium sized resistor (33~44 kΩ). Given that in most cases the current outputs are in the 10s and 20s of μA, the voltage across the resistor would take some time to change with the presence of any significant amount of capacitance on either node. An illustration of the effect of different switching speeds is shown Fig. 5.38.

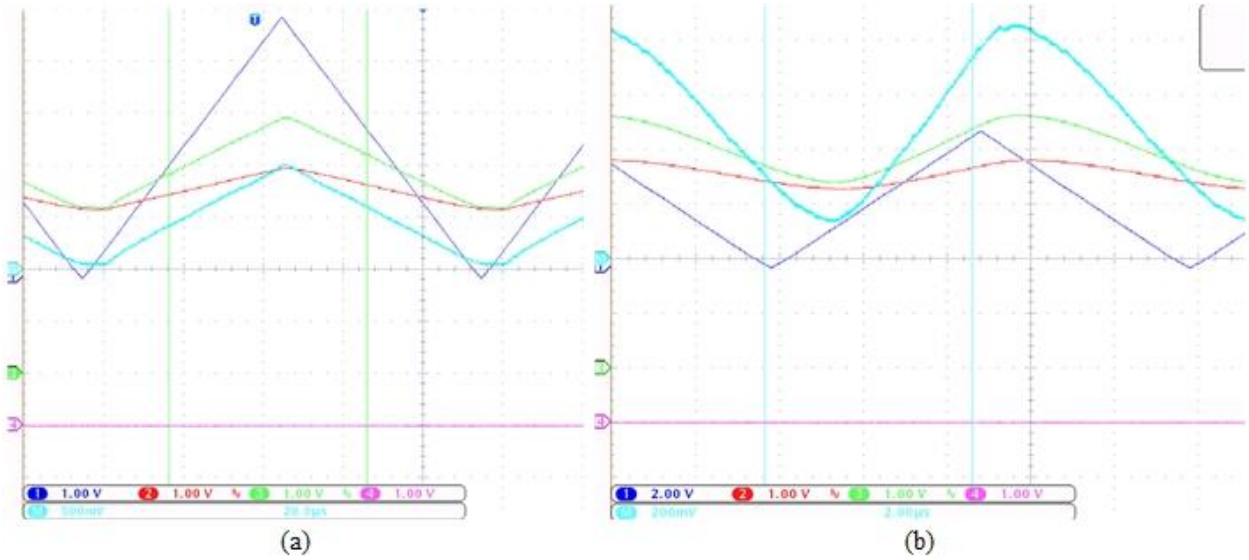


Fig. 5.38. Output current from the LVIC circuit for V_{OUT} at (a) 10 kHz and (b) 100 kHz.

The input voltage to the input frontend is shown in dark blue for both of the graphs. The voltages across the measuring resistance are shown in green and red, with the cyan colored curve denoting the voltage difference representing the current through the resistor.

As can be seen from the graph, the output curve has a much higher delay when the input ramp speed is held at 100 kHz, the target maximum frequency of operation. Part of this due to the phase lag in the OTA, while another part of it can be attributed to the parasitic and stray capacitances in the board. The solution to the first issue is to design an OTA that has a higher bandwidth, and a higher phase margin. This, almost certainly, will necessitate a three stage op amp with an output buffer stage. The second issue will be less limiting when the system is implemented in an all-on-chip solution. This would not only cut down on the parasitic capacitances stemming from pads and connections, but also would make the measuring resistors redundant, thus getting rid of any RC effect.

A third and final point to be made in this section is the note that given the nature of the outputs of the current conditioning circuits, current only flows in one direction in this system. Hence, any natural charge buildup that needs to be reversed quickly can often take longer time. A scheme may be developed to quickly discharge nodes that may be susceptible to excess charge buildup.

5.5.4.2 Effect of Errors and Noise in the System

A noise model for the FETs is not available in the design kit at the moment. However, a rough quantitative estimation of the effect of the error stemming from different circuits may be useful to understand the effect of circuit errors in the whole system.

The linear V to I converter circuit suffers from low conversion gain at the very beginning of its range. Given that the voltage sensors would almost always be operating at the medium to higher range, it is of little concern for the entities, V_{OUT} and V_{CC}. However, the current sensor conditioning circuit are designed in such a way as to start operating from the lowest range. Hence,

the normalization value of the current will suffer from some error. Given that the standard average deviation for all the current conditioning circuit is around 10% of the nominal value, that number will be used throughout this section. The offset of the OTA is taken pessimistically to be 50 mV, which represents a 1% of the full scale. Since the valid current sensor output scale is only 2.5 V to 3.5 V, the offset is 5% of the full scale. Under such circumstances, the outputs of the frontend input would contain the following error

- System voltages - +/- 3% (allowing for a 2% standard deviation in the LVIC)
- System current - +/- 15% (allowing for a 10% standard deviation in the LVIC). However, since the current is on the lower end, the error is more likely to be negative

The system voltage entities are always held at the nominal range by the careful selection of the bias current and output settings of the LVIC circuit. The current squaring circuit and the multiplying circuit both suffer from higher than nominal gain at lower inputs, and lower gain at higher inputs. Hence, this can somewhat counter balance the effect of the system current. However to allow for maximum probable deviation, this particular advantage is ignored. The maximum deviation for the voltage and current entities are calculated as +/- 5% for the voltages (considering the 2% standard deviation), and +27 / -23 % for the currents.

At this juncture it should be noted that the current entities are then scaled to $1/15^{th}$ in reference to the voltage entities. Hence, in reference to the whole system the error in the current is reduced +/- 1.8%. The final part is to account for the current comparator which has an offset of 400 nA for a 20 µA nominal input currents or which roughly translates to a 2% error. Given all the values, the total error in the system can be assumed to be a maximum +/- 9%, which in turn will result in the output going from 200 V to either 182 V or 212 V. That being said, it must

remembered that if the deviation is an issue of scaling, sensing resistor scaling can be done on the board to get the desired output.

A more intricate prospect is the introduction of noise into the system. Spurious noise at or near switching frequency is unlikely to happen because of the relatively low value of even the maximum target frequency. The slowness of the system as has been discussed earlier in this section can act as a natural barrier to the noise in the system. Random spikes can be expected to be absorbed by the node parasitic capacitances, while systematic high frequency noise will most likely be filtered out by the 1 MHz clock frequency that is driving the controller. Except for the current mirrors, the system does not offer much gain in any of the circuits. Sudden changes in current drawn for current mirrors can cause longer settling times and slow down the system. A proper noise analysis should be done before applying this controller to a noise-sensitive high switching frequency converter.

Given the comparative results for 10 kHz and 100 kHz ramp input signals, and the effect of random and high frequency noise, it is recommended that the optimum switching frequency of the controller be around 10 kHz while the maximum be set at around 20 kHz or slightly above, not the 100 kHz as was originally intended. The switching frequency can be increased in time by the improvement of the op amp, the introduction of a scheme to drain stray charges quickly, and reducing the parasitic capacitances of the system.

5.6 Summary

The test results of the circuits and systems developed as a part of this work have been described in detail in this chapter. The tests have shown the first current-mode signal conditioning circuits for high temperature. The first SiC CMOS amplifier operating at 400 °C and the first

voltage comparator working at 550 °C have been demonstrated in this work. The chapter also details the performance of the first ever data converters in SiC. These are also the first data converters working at over 300 °C that have been reported. Finally a demonstration of the integrated controller was shown under test. The integrated controller's operation verifies the viability of the use of the current-mode signal conditioning circuits and the general purpose amplifiers and comparators designed in this work.

CHAPTER 6 CONCLUSION AND FUTURE WORK

This work has developed some of the first general purpose analog and mixed-signal circuits in high temperature SiC. The work has also demonstrated the possibility of a novel current-mode analog signal processing system in future SiC ICs. The current-mode analog processing will remain an attractive solution until three to four metal layers are available in the SiC process instead of just one as is the case right now. The systems and circuits designed and tested as a part of this project will contribute significantly to the development of SiC integrated circuits in the near future.

6.1 Contributions to the State of the Art

The contributions of the this work to the state of the art SiC circuits are three fold

- General purpose analog circuits – This has demonstrated a PFET input CMOS amplifier from 25 °C to 400 °C. The use of the PFET input stage allows for an input common mode range starting from 0 V, which makes it suitable for sensor voltage that start from very low values. The work has also shown the first comparator operational at 550 °C. This opens up the possibility of general purpose control and protection circuitry for very high temperature applications and provides a pathway for system developments in aerospace, aviation, deep earth drilling and other extreme environment applications
- Data Acquisition – The first data converters, both ADC and DAC, in SiC and over 300 °C are reported here. On site data acquisition systems at high temperature can greatly increase the efficiency of systems functioning at high temperatures today. The data acquisition system, coupled with a data transceiver system (developed in the Vulcan II

run) can open up the possibility of using high temperature probes with an off-site controller.

- Integrated Control – The development of the current-mode analog flyback controller demonstrates the possibility of a complex control system in high temperature SiC until powerful and complex digital controllers are available in SiC. The viability of the current-mode signal conditioning circuit is not limited to SiC only, it is a possibility in any developing processes where complex digital controls have not yet been implemented.

6.2 Next Steps for SiC Integrated Circuits

Integrated circuit design in SiC is still in its very early years. And while the development of analog and mixed-signal circuits in this work has opened up a lot of new possibilities, there is still considerable work to be done to make SiC as dependable a solution as Si. Here are some of the steps for the immediate future of SiC IC development

- Amplifiers – The next natural step for the OTA is to add an output buffer stage and turn it into a general purpose operational amplifier. This will make designing filters and signal isolation a possibility in SiC systems. As the PFET threshold voltage decreases, a rail to rail op amp can then also be a possibility.
- Comparators – The next step for the comparator should be the addition of an auto-correcting offset configuration that gets rid of offsets caused by process variation and temperature behavior of FET gates. Also characterization of the rise and fall times, and propagation delays for different over drive voltages need to be performed
- Data Converters – The next step in this would be to decrease the non-linearity effects by designing a more linear DAC. Also, the development of different data converter

topologies such as the C-2C ladder and current steering DACs, as well as sigma-delta and pipeline ADCs is SiC should be investigated in the future.

- Integrated Control – SiC controllers for linear regulators and simple buck converters are already in the works. However more efficient and complex controllers, such as compensated continuous mode converters can be developed in the future. The most significant contribution, however, can be made by integrating a converter controller with the gate driver and protection circuits under development in the same SiC process [107]. An all integrated gate driver and controller can greatly increase the attraction of a SiC solution.

A general theme of the systems designed here is the use of external current and voltage biases. The use of on-chip current and voltage reference [108] developed in Vulcan I and Vulcan II into these circuits and systems can make all-integrated standalone solutions possible which will greatly reduce cost and losses.

6.3 Summary

The future of SiC ICs is very bright, especially in high temperature applications. As humankind explores further into space and delves depper into the earth, and as efficient control technology is developed for engines and furnaces, SiC integrated chips can provide a solution no other IC material is capable of at this point. This work explores those possibilities of innovation and development and successfully demonstrates the viability of SiC integrated circuits and systems for the challenges that lie ahead.

BIBLIGORAPHY

[1] K. Shenai, R. S. Scott, and B. J. Baliga, "Optimum semiconductors for high-power electronics," *IEEE Transactions on Electron Devices*, vol. 36, no. 9, pp. 1811–1823, Sep. 1989.

[2] P. G. Neudeck, R. S. Okojie, and L.-Y. Chen, "High-temperature electronics - a role for wide bandgap semiconductors?," *Proceedings of the IEEE*, vol. 90, no. 6, pp. 1065–1076, Jun. 2002.

[3] J. C. Zolper, "A review of junction field effect transistors for high-temperature and high-power electronics," *Solid-State Electronics*, vol. 42, no. 12, pp. 2153–2156, Dec. 1998.

[4] P. L. Dreike, D. M. Fleetwood, D. B. King, D. C. Sprauer, and T. E. Zipperian, "An overview of high-temperature electronic device technologies and potential applications," *IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part A*, vol. 17, no. 4, pp. 594–609, Dec. 1994.

[5] J. Valle-Mayorga, C. P. Gutshall, K. M. Phan, I. Escorcia-Carranza, H. . Mantooth, B. Reese, M. Schupbach, and A. Lostetter, "High-Temperature Silicon-on-Insulator Gate Driver for SiC-FET Power Modules," *IEEE Transactions on Power Electronics*, vol. 27, no. 11, pp. 4417–4424, Nov. 2012.

[6] M. A. Huque, L. M. Tolbert, B. J. Blalock, and S. K. Islam, "Silicon-on-insulator-based high-voltage, high-temperature integrated circuit gate driver for silicon carbide-based power field effect transistors," *IET Power Electronics*, vol. 3, no. 6, pp. 1001–1009, Nov. 2010.

[7] R. L. Greenwell, B. M. McCue, L. Zuo, M. A. Huque, L. M. Tolbert, B. J. Blalock, and S. K. Islam, "SOI-based integrated circuits for high-temperature power electronics applications," in *2011 Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2011, pp. 836–843.

[8] D. M. Fleetwood, F. V. Thome, S. S. Tsao, P. V. Dressendorfer, V. J. Dandini, and J. R. Schwank, "High-temperature silicon-on-insulator electronics for space nuclear power systems: requirements and feasibility," *IEEE Transactions on Nuclear Science*, vol. 35, no. 5, pp. 1099–1112, Oct. 1988.

[9] H. Ishida, Y. Hirose, T. Murata, Y. Ikeda, T. Matsuno, K. Inoue, Y. Uemoto, T. Tanaka, T. Egawa, and D. Ueda, "A high-power RF switch IC using AlGaN/GaN HFETs with single-stage configuration," *IEEE Transactions on Electron Devices*, vol. 52, no. 8, pp. 1893–1899, Aug. 2005.

[10] J. G. Yang and K. Yang, "GaN-based pin diodes for microwave switching IC applications," *Electronics Letters*, vol. 48, no. 11, pp. 650–652, May 2012.

[11] H. Wang, A. M. Ho Kwan, Q. Jiang, and K. J. Chen, "A GaN Pulse Width Modulation Integrated Circuit for GaN Power Converters," *IEEE Transactions on Electron Devices*, vol. PP, no. 99, pp. 1–1, 2015.

[12] P. G. Neudeck, D. J. Spry, L.-Y. Chen, G. M. Beheim, R. S. Okojie, C. W. Chang, R. D. Meredith, T. L. Ferrier, L. J. Evans, M. J. Krasowski, and N. F. Prokop, "Stable Electrical Operation of 6H-SiC JFETs and ICs for Thousands of Hours at 500," *IEEE Electron Device Letters*, vol. 29, no. 5, pp. 456–459, May 2008.

[13] A. Elasser and T. P. Chow, "Silicon carbide benefits and advantages for power electronics circuits and systems," *Proceedings of the IEEE*, vol. 90, no. 6, pp. 969–986, Jun. 2002.

[14] B. J. Baliga, *Silicon Carbide Power Devices*. World Scientific, 2005.

[15] R. C. Clarke, C. D. Brandt, S. Sriram, R. R. Siergiej, A. W. Morse, A. K. Agarwal, L. S. Chen, V. Balakrishna, and A. A. Burk, "Recent advances in high temperature, high frequency SiC devices," in *High-Temperature Electronic Materials, Devices and Sensors Conference, 1998*, 1998, pp. 18–28.

[16] X. Zhong, X. Wu, W. Zhou, and K. Sheng, "An All-SiC High-Frequency Boost DC-DC Converter Operating at 320 °C Junction Temperature," *IEEE Transactions on Power Electronics*, vol. 29, no. 10, pp. 5091–5096, Oct. 2014.

[17] S. Safari, A. Castellazzi, and P. Wheeler, "Experimental and Analytical Performance Evaluation of SiC Power Devices in the Matrix Converter," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2584–2596, May 2014.

[18] T. Funaki, J. C. Balda, J. Junghans, A. S. Kashyap, H. A. Mantooth, F. Barlow, T. Kimoto, and T. Hikihara, "Power Conversion With SiC Devices at Extremely High Ambient Temperatures," *IEEE Transactions on Power Electronics*, vol. 22, no. 4, pp. 1321–1329, Jul. 2007.

[19] A. Agarwal, M. Das, B. Hull, S. Krishnaswami, J. Palmour, J. Richmond, S.-H. Ryu, and J. Zhang, "Progress in Silicon Carbide Power Devices," in *Device Research Conference, 2006 64th*, 2006, pp. 155–158.

[20] J. Millan, P. Godignon, and D. Toumier, "Recent developments in SiC power devices and related technology," presented at the International conference on microelectronics, 2004.

[21] H. Goronkin and U. K. Mishra, *Compound Semiconductors 1994, Proceedings of the Twenty-First INT Symposium on Compound Semiconductors held in San Diego, California, 18-22 September 1994*. CRC Press, 1995.

[22] R. Raghunathan and B. J. Baliga, "Role of defects in producing negative temperature dependence of breakdown voltage in SiC," *Applied Physics Letters*, vol. 72, no. 24, pp. 3196–3198, Jun. 1998.

[23] A. G. Chynoweth, “Ionization Rates for Electrons and Holes in Silicon,” *Phys. Rev.*, vol. 109, no. 5, pp. 1537–1540, Mar. 1958.

[24] A. G. Chynoweth, “Uniform Silicon p-n Junctions. II. Ionization Rates for Electrons,” *Journal of Applied Physics*, vol. 31, no. 7, pp. 1161–1165, Jul. 1960.

[25] T. Hatakeyama, T. Watanabe, T. Shinohe, K. Kojima, K. Arai, and N. Sano, “Impact ionization coefficients of 4H silicon carbide,” *Applied Physics Letters*, vol. 85, no. 8, pp. 1380–1382, Aug. 2004.

[26] A. Lelis, D. Habersat, F. Olaniran, B. Simons, J. McGarrity, F. B. McLean, and N. Goldsman, “Time-Dependent Bias Stress-Induced Instability of SiC MOS Devices,” in *Symposium B – Silicon Carbide 2006 – Materials, Processing and Devices*, 2006, vol. 911.

[27] A. J. Lelis, D. B. Habersat, G. Lopez, J. M. McGarrity, F. B. McLean, and N. Goldsman, “Bias Stress-Induced Threshold-Voltage Instability of SiC MOSFETs,” *Materials Science Forum*, vol. 527–529, pp. 1317–1320, 2006.

[28] M. Gurfinkel, J. Suehle, J. B. Bernstein, Y. Shapira, A. J. Lelis, D. Habersat, and N. Goldsman, “Ultra-Fast Characterization of Transient Gate Oxide Trapping in SiC Mosfets,” in *Reliability physics symposium, 2007. proceedings. 45th annual. ieee international*, 2007, pp. 462–466.

[29] S. Potbhare, N. Goldsman, A. Akturk, M. Gurfinkel, A. Lelis, and J. S. Suehle, “Energy- and Time-Dependent Dynamics of Trap Occupation in 4H-SiC MOSFETs,” *IEEE Transactions on Electron Devices*, vol. 55, no. 8, pp. 2061–2070, Aug. 2008.

[30] S. Suzuki, S. Harada, R. Kosugi, J. Senzaki, W. Cho, and K. Fukuda, “Correlation between channel mobility and shallow interface traps in SiC metal–oxide–semiconductor field-effect transistors,” *Journal of Applied Physics*, vol. 92, no. 10, pp. 6230–6234, Nov. 2002.

[31] K. Matocha, “Challenges in SiC power MOSFET design,” *Solid-State Electronics*, vol. 52, no. 10, pp. 1631–1635, Oct. 2008.

[32] V. A. Dmitriev and M. G. Spencer, “Chapter 2 SiC Fabrication Technology: Growth and Doping,” in *Semiconductors and Semimetals*, vol. 52, Y. S. Park, Ed. Elsevier, 1998, pp. 21–75.

[33] M. A. Bautista, A. R. de Arellano-López, J. Martínez-Fernández, A. Bravo-León, and J. M. López-Cepero, “Optimization of the fabrication process for medium density fiberboard (MDF)-based biomimetic SiC,” *International Journal of Refractory Metals and Hard Materials*, vol. 27, no. 2, pp. 431–437, Mar. 2009.

[34] S. Round, M. Heldwein, J. Kolar, I. Hofsajer, and P. Friedrichs, “A SiC JFET driver for a 5 kW, 150 kHz three-phase PWM converter,” in *Industry Applications Conference, 2005. Fourtieth IAS Annual Meeting. Conference Record of the 2005*, 2005, vol. 1, pp. 410–416 Vol. 1.

[35] J. Wang, T. Zhao, J. Li, A. Q. Huang, R. Callanan, F. Husna, and A. Agarwal, "Characterization, Modeling, and Application of 10-kV SiC MOSFET," *IEEE Transactions on Electron Devices*, vol. 55, no. 8, pp. 1798–1806, Aug. 2008.

[36] S. Krishnaswami, A. Agarwal, S.-H. Ryu, C. Capell, J. Richmond, J. Palmour, S. Balachandran, T. P. Chow, S. Bayne, B. Geil, K. Jones, and C. Scozzie, "1000-V, 30-A 4H-SiC BJTs with high current gain," *IEEE Electron Device Letters*, vol. 26, no. 3, pp. 175–177, Mar. 2005.

[37] H. A. Mantooth, M. D. Glover, and P. Shepherd, "Wide Bandgap Technologies and Their Implications on Miniaturizing Power Electronic Systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 3, pp. 374–385, Sep. 2014.

[38] J. M. Hornberger, E. Cilio, B. McPherson, R. M. Schupbach, and A. B. Lostetter, "A Fully Integrated 300Â°C, 4 kW, 3-Phase, SiC Motor Drive Module," in *IEEE Power Electronics Specialists Conference, 2007. PESC 2007*, 2007, pp. 1048–1053.

[39] F. Xu, D. Jiang, J. Wang, F. Wang, L. M. Tolbert, T. J. Han, J. Nagashima, and S. J. Kim, "High temperature packaging of 50 kW three-phase SiC power module," in *2011 IEEE 8th International Conference on Power Electronics and ECCE Asia (ICPE ECCE)*, 2011, pp. 2427–2433.

[40] O. S. Saadeh, E. D. Johnson, M. S. Saadeh, A. Escobar Mejia, C. Schirmer, B. Rowden, A. Mantooth, J. Balda, and S. Ang, "A 4 kV Silicon Carbide solid-state fault current limiter," in *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2012, pp. 4445–4449.

[41] U. Schmid, S. T. Sheppard, and W. Wondrak, "High temperature performance of NMOS integrated inverters and ring oscillators in 6H-SiC," *IEEE Transactions on Electron Devices*, vol. 47, no. 4, pp. 687–691, Apr. 2000.

[42] W. Xie, J. J.A. Cooper, and M. R. Melloch, "Monolithic NMOS digital integrated circuits in 6H-SiC," *IEEE Electron Device Letters*, vol. 15, no. 11, pp. 455–457, Nov. 1994.

[43] A. C. Patil, X.-A. Fu, M. Mehregany, and S. L. Garverick, "Fully-monolithic, 600 °C differential amplifiers in 6H-SiC JFET IC technology," in *IEEE Custom Integrated Circuits Conference, 2009. CICC '09*, 2009, pp. 73–76.

[44] J. D. B. Slater, L. A. Lipkin, G. M. Johnson, A. V. Suvorov, and J. W. Palmour, "High temperature enhancement-mode NMOS and PMOS devices and circuits in 6H-SiC," in *Device Research Conference, 1995. Digest. 1995 53rd Annual*, 1995, pp. 100–101.

[45] J.-S. Chen, K. T. Kornegay, and S.-H. Ryu, "A silicon carbide CMOS intelligent gate driver circuit with stable operation over a wide temperature range," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 2, pp. 192–204, Feb. 1999.

[46] M. Tomana, R. W. Johnson, R. C. Jaeger, and W. C. Dillard, "A hybrid silicon carbide differential amplifier for 350 deg C operation," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, vol. 16, no. 5, pp. 536–542, Aug. 1993.

[47] S. Singh and J. A. Cooper, "Bipolar Integrated Circuits in 4H-SiC," *IEEE Transactions on Electron Devices*, vol. 58, no. 4, pp. 1084–1090, Apr. 2011.

[48] A. S. Kashyap, C.-P. Chen, R. Ghandi, A. Patil, E. Andarawis, L. Yin, D. Shaddock, P. Sandvik, K. Fang, Z. Shen, and W. Johnson, "Silicon carbide integrated circuits for extreme environments," in *2013 IEEE Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2013, pp. 60–63.

[49] S. L. Garverick, C.-W. Soong, and M. Mehregany, "SiC JFET integrated circuits for sensing and control at temperatures up to 600 °C," in *2012 IEEE Energytech*, 2012, pp. 1–6.

[50] N. Ericson, S. Frank, C. Britton, L. Marlino, S.-H. Ryu, D. Grider, A. Mantooth, M. Francis, R. Lamichhane, M. Mudholkar, P. Shepherd, M. Glover, J. Valle-Mayorga, T. McNutt, A. Barkley, B. Whitaker, Z. Cole, B. Passmore, and A. Lostetter, "A 4H Silicon Carbide Gate Buffer for Integrated Power Systems," *IEEE Transactions on Power Electronics*, vol. 29, no. 2, pp. 539–542, Feb. 2014.

[51] M. D. Glover, P. Shepherd, A. Francis, M. Mudholkar, H. A. Mantooth, M. N. Ericson, S. S. Frank, C. L. Britton, L. D. Marlino, T. R. McNutt, A. Barkley, B. Whitaker, and A. Lostetter, "A UVLO Circuit in SiC Compatible With Power MOSFET Integration," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 3, pp. 425–433, Sep. 2014.

[52] J. A. Valle-Mayorga, A. Rahman, and H. A. Mantooth, "A SiC NMOS Linear Voltage Regulator for High-Temperature Applications," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2321–2328, May 2014.

[53] D. T. Clark, E. P. Ramsay, A. E. Murphy, D. A. Smith, R. F. Thompson, R. A. R. Young, J. D. Cormack, C. Zhu, S. Finney, and J. Fletcher, "High Temperature Silicon Carbide CMOS Integrated Circuits," *Materials Science Forμum*, vol. 679–680, pp. 726–729, Mar. 2011.

[54] R. A. R. Young, D. Clark, J. D. Cormack, A. E. Murphy, D. A. Smith, R. F. Thompson, E. P. Ramsay, and S. Finney, "High Temperature Digital and Analogue Integrated Circuits in Silicon Carbide," *Materials Science Forum*, vol. 740–742, pp. 1065–1068, Jan. 2013.

[55] P. Shepherd, A. Rahman, S. Ahmed, A. M. Francis, J. Holmes, and H. A. Mantooth, "500 kHz – 5 MHz Phase-Locked Loops in High-Temperature Silicon Carbide CMOS," *Additional Conferences (Device Packaging, HiTEC, HiTEN, & CICMT)*, vol. 2014, no. HITEC, pp. 000076–000083, Jan. 2014.

[56] A. Rahman, P. D. Shepherd, S. A. Bhuyan, S. Ahmed, S. K. Akula, L. Caley, H. Alan Mantooth, J. Di, A. Matthew Francis, and J. A. Holmes, "A family of CMOS analog and

mixed-signal circuits in SiC for high temperature electronics," in *2015 IEEE Aerospace Conference*, 2015, pp. 1–10.

[57] L. Caley, et al., "Delay-Insensitive Asynchronous Silicon Carbide Integrated Circuit Design for High-Temperature Applications," GOMAC 2014, Charleston, SC, Mar 2014.

[58] N. Kuhns, et al. "High Temperature Testing Results of Synchronous and Asynchronous Digital Silicon Carbide Integrated Circuits," GOMAC 2015, St. Louis, MO, Apr 2015.

[59] A. Matthew Francis, T. Moudy, J. A. Holmes, A. Rahman, M. Barlow, S. Ahmed, and A. Mantooth, "Towards standard component parts in silicon carbide CMOS," in *2015 IEEE Aerospace Conference*, 2015, pp. 1–9.

[60] S. M. Fakhraie, H. Farshbaf, and K. C. Smith, "Scalable closed-boundary analog neural networks," *IEEE Transactions on Neural Networks*, vol. 15, no. 2, pp. 492–504, Mar. 2004.

[61] M. S. T. Talaska, R. Dlugosz, and R. Wojtyna, "Current-Mode Analog Kohonen Neural Network," in *14th International Conference on Mixed Design of Integrated Circuits and Systems, 2007. MIXDES '07*, 2007, pp. 250–255.

[62] T. Talaska and R. Dlugosz, "Current-Mode Euclidean Distance Calculation Circuit for Kohonen's Neural Network Implemented in CMOS 0.18 µm Technology," in *Canadian Conference on Electrical and Computer Engineering, 2007. CCECE 2007*, 2007, pp. 437–440.

[63] O. Rossetto, C. Jutten, J. Herault, and I. Kreuzer, "Analog VLSI synaptic matrices as building blocks for neural networks," *IEEE Micro*, vol. 9, no. 6, pp. 56–63, Dec. 1989.

[64] E. A. Vittoz, "Analog VLSI signal processing: Why, where, and how?," *Journal of VLSI Signal Processing*, vol. 8, no. 1, pp. 27–44, Feb. 1994.

[65] M. Shaterian, C. M. Twigg, and J. Azhari, "An MTL-Based Configurable Block for Current-Mode Nonlinear Analog Computation," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 60, no. 9, pp. 587–591, Sep. 2013.

[66] C. Twigg and P. Hasler, "Configurable analog signal processing," *Digital Signal Processing*, vol. 19, no. 6, pp. 904–922, Dec. 2009.

[67] P. Hasler, "Low-power programmable signal processing," in *Fifth International Workshop on System-on-Chip for Real-Time Applications, 2005. Proceedings*, 2005, pp. 413–418.

[68] Y. Zheng, J. Yan, and Y. P. Xu, "A CMOS VGA With DC Offset Cancellation for Direct-Conversion Receivers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 56, no. 1, pp. 103–113, Jan. 2009.

[69] C. Toumaumazou, F. J. Lidgey, and D. G. Haigh, Eds., *Analogue IC Design: The Current-Mode Approach*. The Institution of Engineering and Technology, Michael Faraday House, Six Hills Way, Stevenage SG1 2AY, UK: IET, 1993.

[70] R. J. Baker, *CMOS: Circuit Design, Layout, and Simulation*. John Wiley & Sons, 2011.

[71] K. Bult and H. Wallinga, "A class of analog CMOS circuits based on the square-law characteristic of an MOS transistor in saturation," *IEEE Journal of Solid-State Circuits*, vol. 22, no. 3, pp. 357–365, Jun. 1987.

[72] A. Nedungadi and T. R. Viswanathan, "Design of linear CMOS transconductance elements," *IEEE Transactions on Circuits and Systems*, vol. 31, no. 10, pp. 891–894, Oct. 1984.

[73] J. N. Babanezhad and G. C. Temes, "A 20-V four-quadrant CMOS analog multiplier," *IEEE Journal of Solid-State Circuits*, vol. 20, no. 6, pp. 1158–1168, Dec. 1985.

[74] C. Chen and Z. Li, "A low-power CMOS analog multiplier," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 53, no. 2, pp. 100–104, Feb. 2006.

[75] K. Bult and H. Wallinga, "A CMOS Four-Quadrant Analog Multiplier," *IEEE Journal of Solid-State Circuits*, vol. 21, no. 3, pp. 430–435, Jun. 1986.

[76] W. Liu, S.-I. Liu, and S.-K. Wei, "CMOS current-mode divider and its applications," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 52, no. 3, pp. 145–148, Mar. 2005.

[77] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*. OUP USA, 2011.

[78] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*. Oxford University Press, 2010.

[79] W.-S. Chu and K. W. Current, "A rail-to-rail input-range CMOS voltage comparator," in *Proceedings of the 40th Midwest Symposium on Circuits and Systems, 1997*, 1997, vol. 1, pp. 160–163 vol.1.

[80] A. B. Dowlatabadi and J. A. Connelly, "A generic voltage comparator analog cell produced in standard digital CMOS technologies," in , *IEEE 39th Midwest symposium on Circuits and Systems, 1996*, 1996, vol. 1, pp. 35–38 vol.1.

[81] F. Maloberti, *Data Converters*. Springer Science & Business Media, 2007.

[82] T. C. Carusone, *Analog integrated circuit design*, 2nd ed. Hoboken, NJ: John Wiley & Sons, 2012.

[83] S. Rapuano, P. Daponte, E. Balestrieri, L. De Vito, S. J. Tilden, S. Max, and J. Blair, "ADC parameters and characteristics," *IEEE Instrumentation Measurement Magazine*, vol. 8, no. 5, pp. 44–54, Dec. 2005.

[84] R. H. Walden, "Analog-to-digital converter survey and analysis," *IEEE Journal on Selected Areas in Communications*, vol. 17, no. 4, pp. 539–550, Apr. 1999.

[85] E. Delagnes, D. Breton, F. Lugiez, and R. Rahmanifard, "A Low Power Multi-Channel Single Ramp ADC With Up to 3.2 GHz Virtual Clock," *IEEE Transactions on Nuclear Science*, vol. 54, no. 5, pp. 1735–1742, Oct. 2007.

[86] "IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters," *IEEE Std 1241-2010 (Revision of IEEE Std 1241-2000)*, pp. 1–139, Jan. 2011.

[87] S. Ang and A. Oliva, *Power-Switching Converters, Second Edition*. CRC Press, 2005.

[88] L. A. Garcia-Rodriguez, E. Williams, J. C. Balda, J. Gonzalez-Llorente, and H. Chiacchiarini, "Control of a flyback converter operating in BCM using the natural switching surface," in *2015 IEEE 6th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2015, pp. 1–8.

[89] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *IEEE Transactions on Industry Applications*, vol. 41, no. 5, pp. 1292–1306, Sep. 2005.

[90] D. C. Martins and R. Demonti, "Grid connected PV system using two energy processing stages," in *Conference Record of the Twenty-Ninth IEEE Photovoltaic Specialists Conference, 2002*, 2002, pp. 1649–1652.

[91] L. A. Garcia Rodriguez and J. C. Balda, "A comparison of isolated DC-DC converters for microinverter applications," in *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2013, pp. 2084–2091.

[92] Q. Mo, M. Chen, Z. Zhang, Y. Zhang, and Z. Qian, "Digitally controlled active clamp interleaved flyback converters for improving efficiency in photovoltaic grid-connected micro-inverter," in *2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2012, pp. 555–562.

[93] Y.-C. Hsieh, M.-R. Chen, and H.-L. Cheng, "An Interleaved Flyback Converter Featured With Zero-Voltage Transition," *IEEE Transactions on Power Electronics*, vol. 26, no. 1, pp. 79–84, Jan. 2011.

[94] K. D. Young, V. I. Utkin, and U. Ozguner, "A control engineer's guide to sliding mode control," *IEEE Transactions on Control Systems Technology*, vol. 7, no. 3, pp. 328–342, May 1999.

[95] G. Spiazzi, P. Mattavelli, L. Rossetto, and L. Malesani, "Application of sliding mode control to switch-mode power supplies," *J CIRCUIT SYST COMP*, vol. 05, no. 03, pp. 337–354, Sep. 1995.

[96] R. Giral, L. Martinez-Salamero, R. Leyva, and J. Maixe, "Sliding-mode control of interleaved boost converters," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 47, no. 9, pp. 1330–1339, Sep. 2000.

[97] S. Guo, X. Lin-Shi, B. Allard, Y. Gao, and Y. Ruan, "Digital Sliding-Mode Controller For High-Frequency DC/DC SMPS," *IEEE Transactions on Power Electronics*, vol. 25, no. 5, pp. 1120–1123, May 2010.

[98] M. Seker and E. Zergeroglu, "A new sliding mode controller for the DC to DC flyback converter," in *2011 IEEE Conference on Automation Science and Engineering (CASE)*, 2011, pp. 720–724.

[99] J. M. Galvez, M. Ordonez, F. Luchino, and J. E. Quaicoe, "Improvements in Boundary Control of Boost Converters Using the Natural Switching Surface," *IEEE Transactions on Power Electronics*, vol. 26, no. 11, pp. 3367–3376, Nov. 2011.

[100] K. K. S. Leung and H. S. H. Chung, "Derivation of a second-order switching surface in the boundary control of buck converters," *IEEE Power Electronics Letters*, vol. 2, no. 2, pp. 63–67, Jun. 2004.

[101] G. G. Oggier and M. Ordonez, "Boundary Control of Full-Bridge ZVS: Natural Switching Surface for Transient and Steady-State Operation," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 2, pp. 969–979, Feb. 2014.

[102] H. Shichman and D. Hodges, "Modeling and simulation of insulated-gate field-effect transistor switching circuits," *IEEE Journal of Solid-State Circuits*, vol. 3, no. 3, pp. 285–289, Sep. 1968.

[103] E. H. Snow, A. S. Grove, B. E. Deal, and C. T. Sah, "Ion Transport Phenomena in Insulating Films," *Journal of Applied Physics*, vol. 36, no. 5, pp. 1664–1673, May 1965.

[104] J.-H. Jang, G. Cueva, W. E. Hoke, P. J. Lemonias, P. Fay, and I. Adesida, "Metamorphic graded bandgap InGaAs-InGaAlAs-InAlAs double heterojunction p-i-I-n photodiodes," *Journal of Lightwave Technology*, vol. 20, no. 3, pp. 507–514, Mar. 2002.

[105] Z. Chen and F. F. Dai, "A 3 mW 8-Bit radiation-hardened-by-design DAC for ultra-wide temperature range from -180 °C to 120 °C," in *2011 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2011, pp. 997–1000.

[106] K. S. Greig and V. P. Chodavarapu, "Extreme wide-temperature range 8-bit digital-to-analog converter in bulk CMOS process," in *2014 IEEE 27th Canadian Conference on Electrical and Computer Engineering (CCECE)*, 2014, pp. 1–5.

[107] S.-H. Chang, Y.-K. Fang, S.-F. Ting, S.-F. Chen, C.-Y. Lin, C. S. Lin, and C.-Y. Wu, "Fabrication of very high quantum efficiency planar InGaAs PIN photodiodes through prebake process," *Circuits, Devices and Systems, IEE Proceedings*, vol. 152, no. 6, pp. 637–640, Dec. 2005.

[108] H. S. Lim, V. Aimez, B. S. Ooi, J. Beauvais, and J. Beerens, "A novel fabrication technique for multiple-wavelength photonic-integrated devices in InGaAs-InGaAsP laser heterostructures," *IEEE Photonics Technology Letters*, vol. 14, no. 5, pp. 594–596, May 2002.

APPENDIX A

A.1 Current-mode Circuit Transistor Basics

The current-mode signal processing circuits are based on the basic two level transistor circuit, biasing cirfcuit, and the linear voltage to current converter circuit. The two basic circuits are shown below.

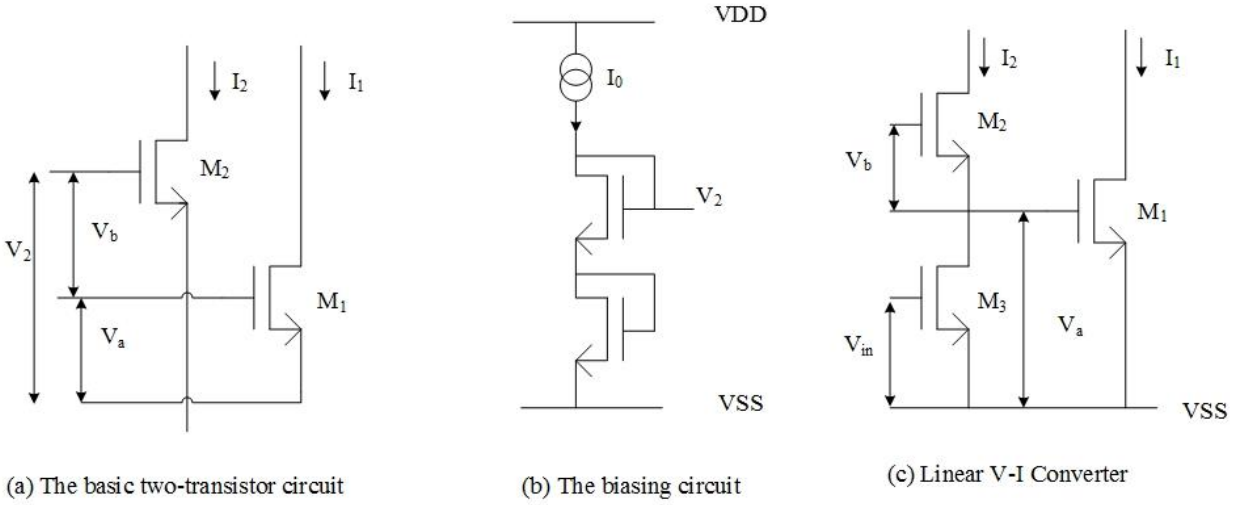


Fig. A1. Transistor basics for current-mode signal processors.

This section describes the relationship between the currents and the input voltage. The currents I_1 and I_2 are represented in terms of the gate to the source voltages of the FETs M_2 and M_1. The process parameter, k_n', coupled with the FET aspect ratio, W/L, is represented by the proportional constant K_n. The relationships established by the derivations here have been used in Chapter 4 to design and simulate the current-mode signal processing circuits.

$$I_1 = K_n(V_a - V_{tn})^2 \qquad I_2 = K_n(V_b - V_{tn})^2$$

To further illustrate the voltage and current relationship, the difference of the voltages are given by the representations, x and y.

$$x = V_a - V_{tn} \qquad y = V_b - V_{tn}$$

$$x + y = V_a + V_b - 2\,V_{tn} = V_2 - V_{tn} \qquad x - y = V_a - V_{tn} - V_b + V_{tn} = V_a - V_b$$

The difference between the currents in the two branches, $I_1 - I_2$, is dependable on the gate voltage of v_a and v_b. The threshold voltage of the FETs is given by V_{tn} and the Sum of the voltages are given by V_2.

$$I_1 - I_2 = K_n(V_a - V_{tn})^2 - K_n(V_b - V_{tn})^2$$

$$\Rightarrow I_1 - I_2 = K_n\,(V_a - V_{tn} + V_b - V_{tn})(V_a - V_{tn} - V_b + V_{tn})$$

$$\Rightarrow I_1 - I_2 = K_n(\,V_2 - 2V_{tn})(V_a - V_b) \qquad \ldots \qquad \text{(A1.1)}$$

$$I_1 - I_2 = K_n(x + y)(x - y)$$

$$I_1 + I_2 = K_n x^2 + K_n y^2$$

$$\Rightarrow I_1 + I_2 = K_n\,(x^2 + y^2\,)$$

$$\Rightarrow I_1 + I_2 = \tfrac{1}{2}\,K_n\,(x + y)^2 + \tfrac{1}{2}\,K_n\,(x - y)^2$$

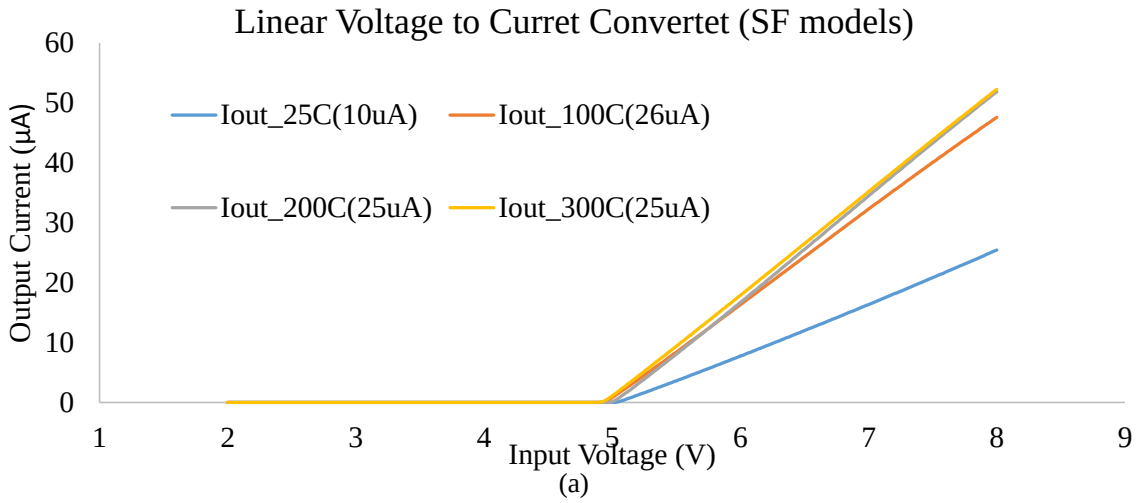
$$\Rightarrow I_1 + I_2 = \tfrac{1}{2}\,K_n\,(V_2 - 2V_{tn})^2 + \tfrac{1}{2}\,K_n\,\frac{(I_1 - I_2)^2}{\left(K_n(x+y)\right)^2}$$

$$\Rightarrow I_1 + I_2 = \tfrac{1}{2}\,K_n\,(V_2 - 2V_{tn})^2 + \frac{(I_1 - I_2)^2}{K_n(V_2 - 2V_{tn})^2} \qquad \ldots \qquad \text{(A1.2)}$$

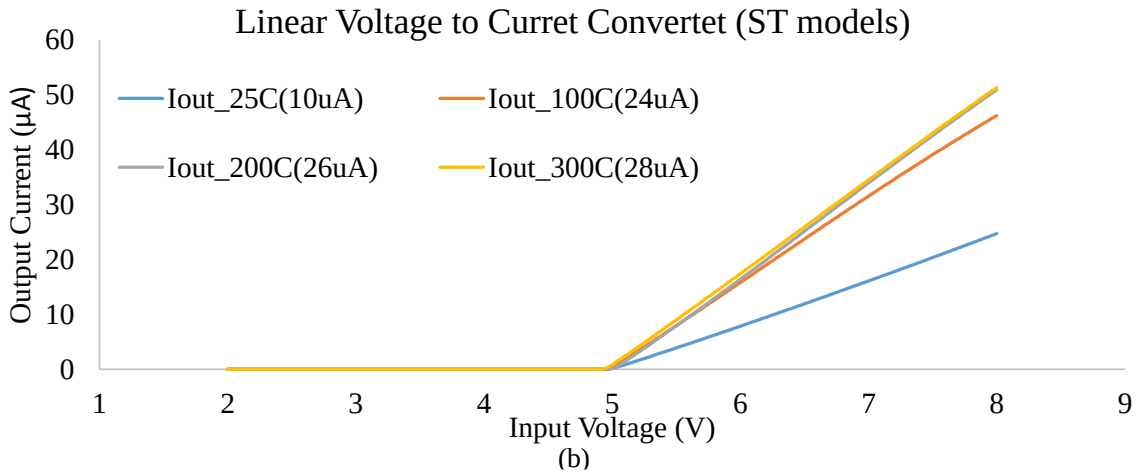
Eqs. (A1.1) and (A1.2) represent the two governing equations for the basic transistor circuits and linear voltage to converter.

A.2 Linear Voltage to Current Converter Simulation

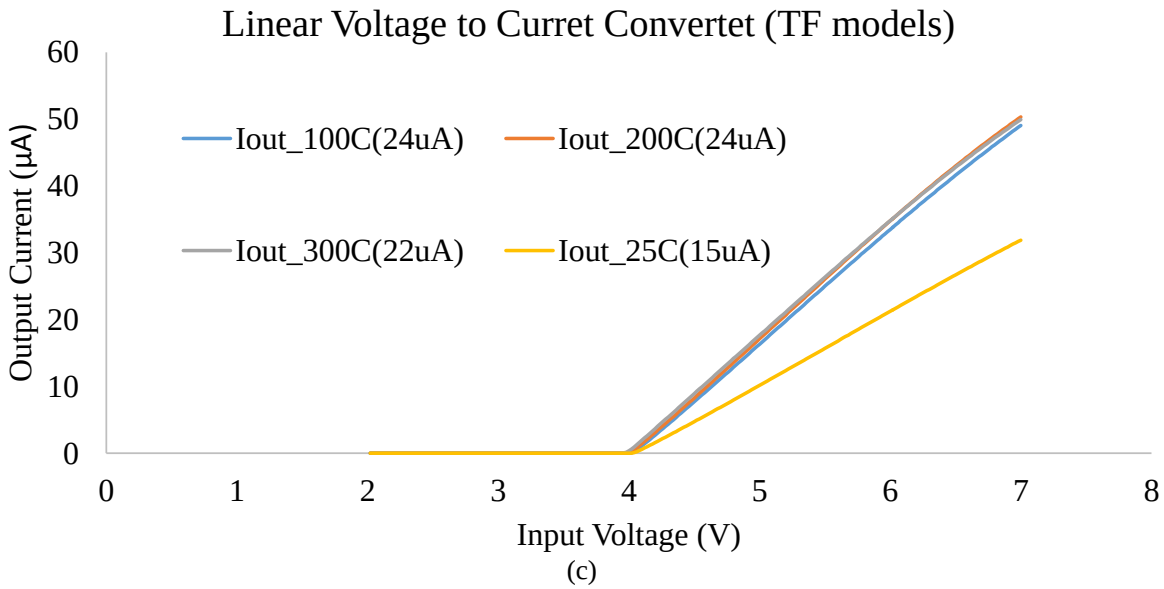
The linear voltage to current converter simulations for the typical models (TT) have been shared in Chapter 4. Simulation results for other model types (TF, SF, ST) over temperature are shown in Fig. A.2.



(a)



(b)



(c)

Fig. A2. LVIC circuit simulation results over temperature with (a) SF, (b) ST and (c) TF models.

The simulation results show a linear current response for all the different models. The LVIC circuit with slow NFET models have a higher threshold – this is to be expected since the slow models refer to a higher threshold voltage for the NFETs. This leads to higher minimum value of the input range of the linear V to I converter. The TF model does not suffer from a limitation on the minimum of the input range.

A.2.1. FET Sizes for the Current Mirrors in the LVIC Circuit

As a refresher here is the full linear voltage to current converter circuit with the collection of current mirrors to set the different current conversion gains (40% to 120%)

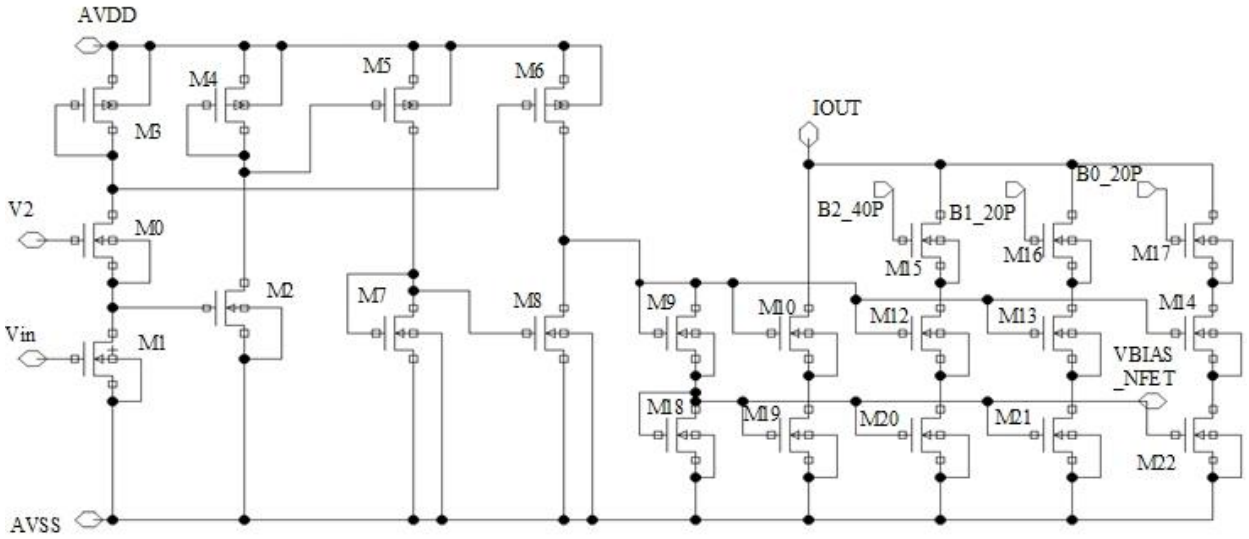


Fig. A3. Linear voltage to current converter with different circuits.

Table A1. FET sizes for the complete linear voltage to current converter circuit

FET	W/L Ratio	No. of fingers	FET	W/L Ratio	No. of fingers	FET	W/L Ratio	No. of fingers
M0	8 µ/2 µ	2	M1	8 µ/4 µ	1	M2	8 µ/2 µ	1
M3-M6	12 µ /2 µ	2	M7,M8	12 µ /5 µ	1	M9,M18	20 µ /2 µ	7
M10,M12, M19,M20	20 µ /2 µ	4	M13,M14, M21,M22	20 µ /2 µ	2	M15,M16 M17	20 µ /2 µ	2

A.3 Current Multiplier Circuit Simulations

The current multiplier circuit has current squaring circuits the sizes of the FETs of which have already been described. The PFET current mirrors are simple current mirrors with devices of 20 µm / 2 µm ratio and six fingers. The NFET current mirrors are simple cascode current mirrors with devices of 20 µm / 2 µm and four fingers.

The simulation results of the current multiplier over all temperatures for the device models of TF, ST and SF are shown in the following pages. The simulation results for the TT models have already been shown in section 4.2.3.

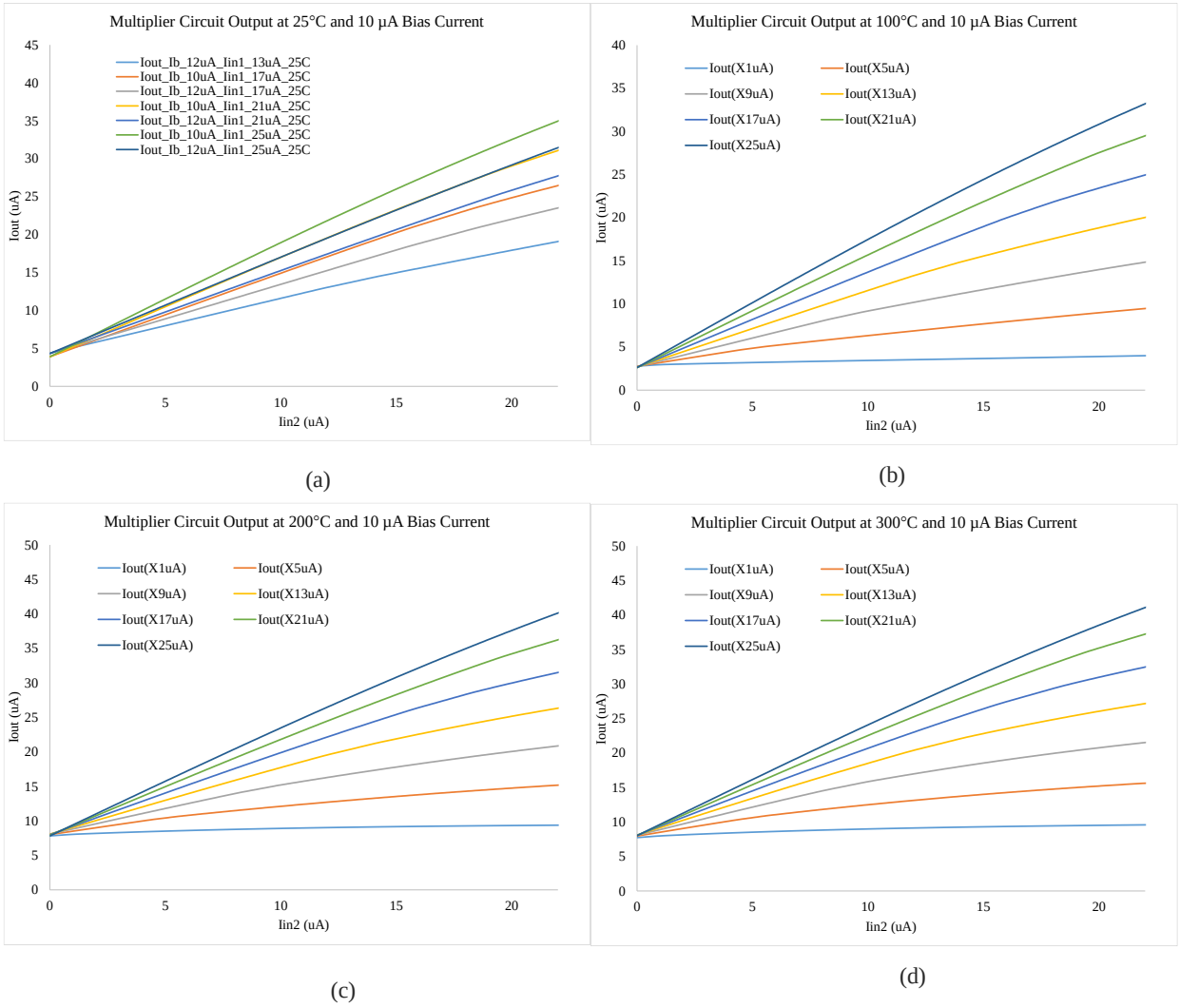


Fig. A4. Multiplier circuit simulation over temperature for TF models.

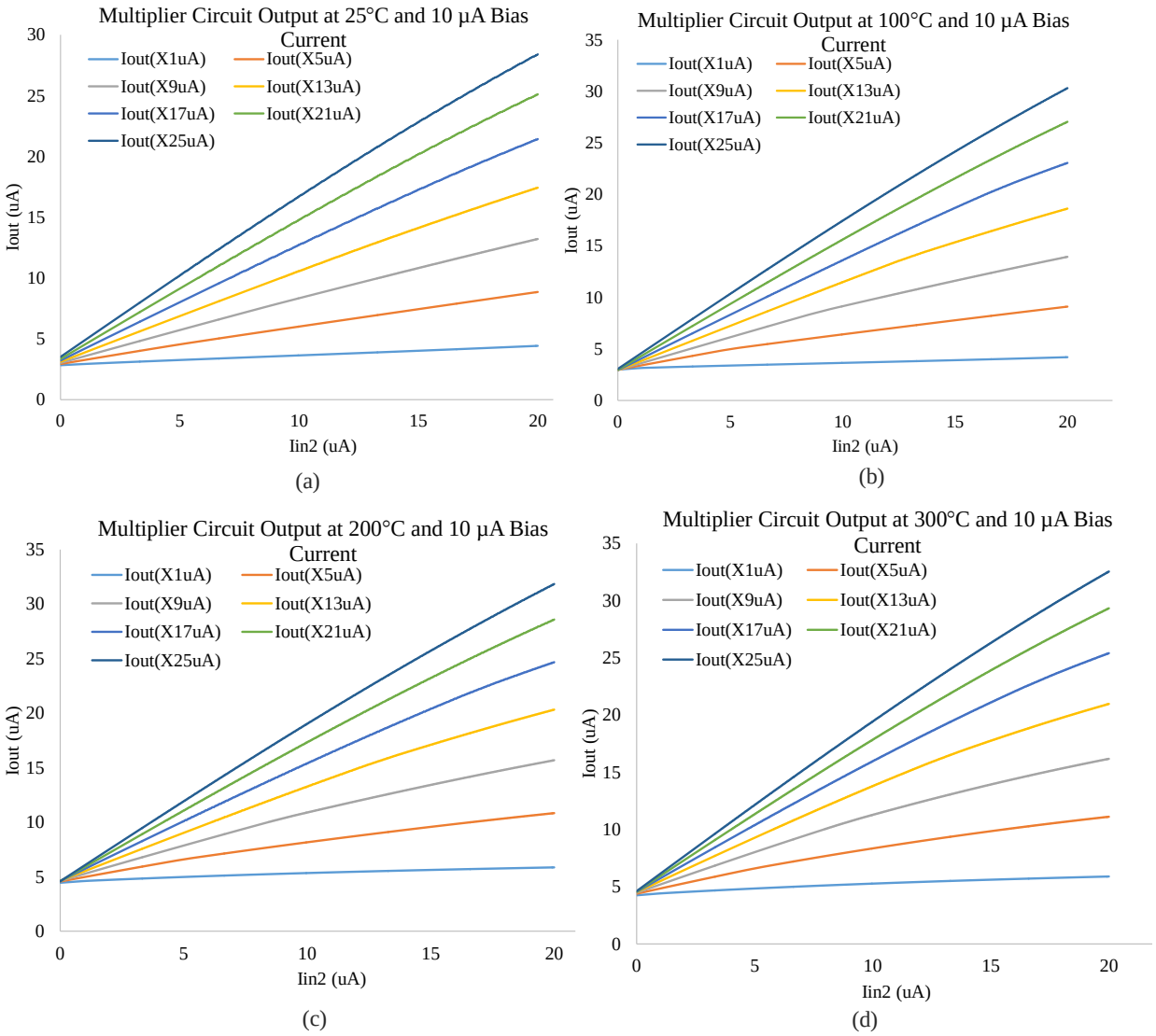


Fig. A5. Multiplier circuit simulation over temperature for ST models.

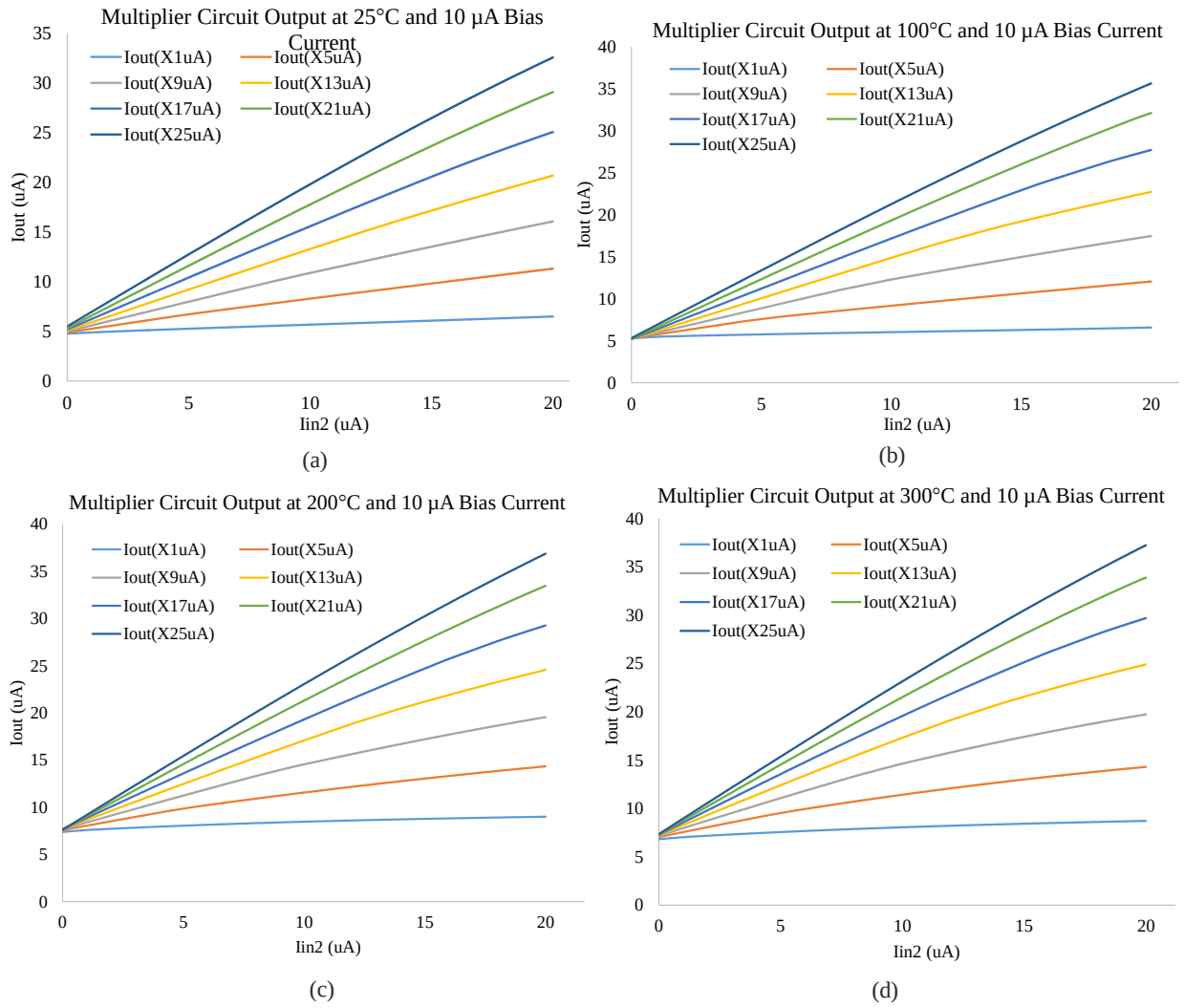


Fig. A6. Multiplier circuit simulation over temperature for SF models.

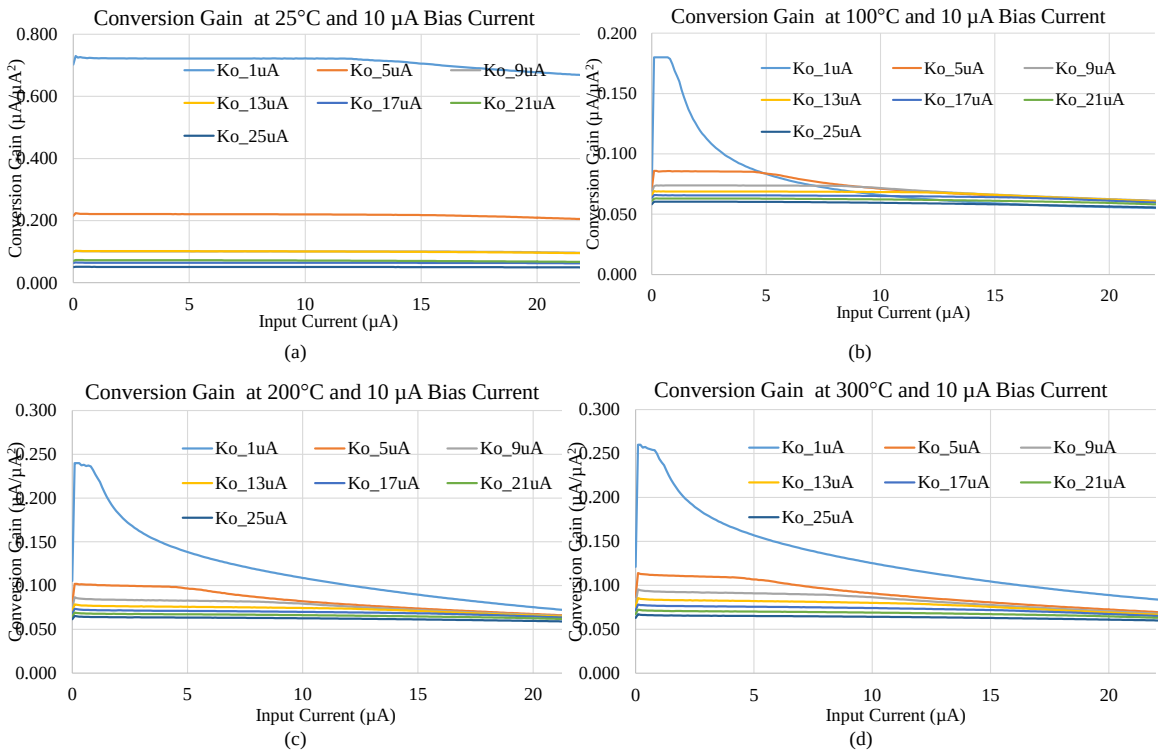


Fig. A7. Conversion gains for the multiplier circuit over temperature with TF models.

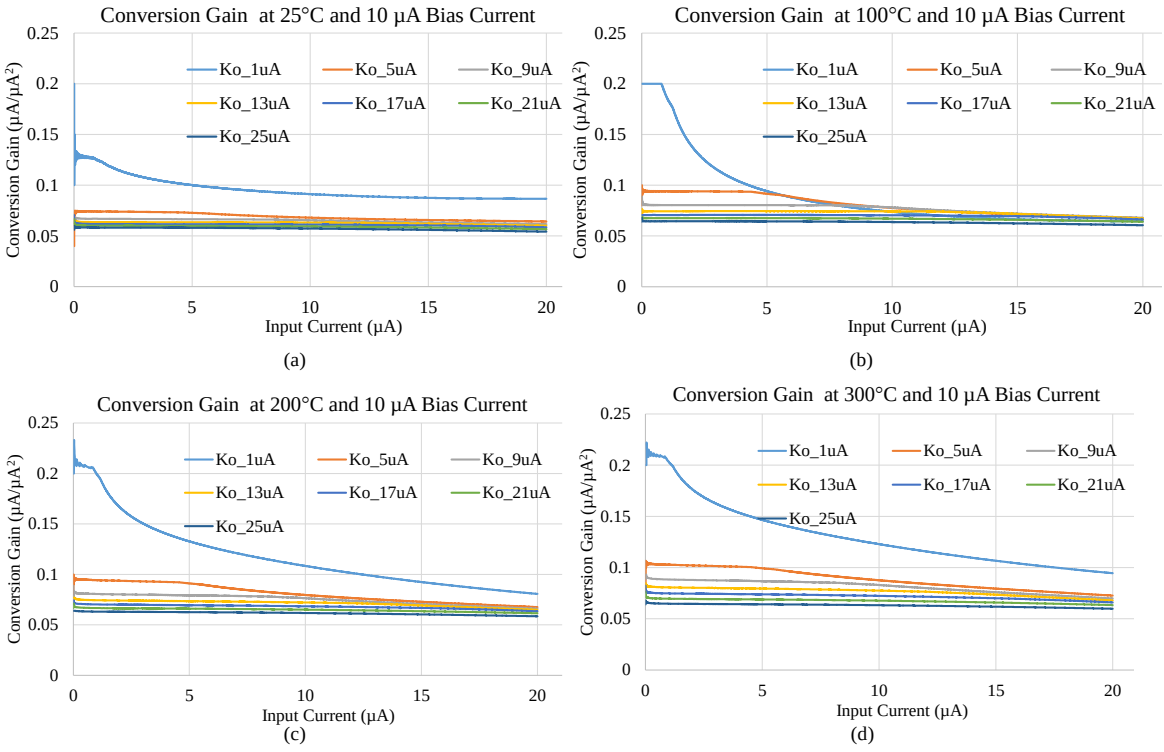


Fig. A8. Conversion gains for the multiplier circuit over temperature with SF models.

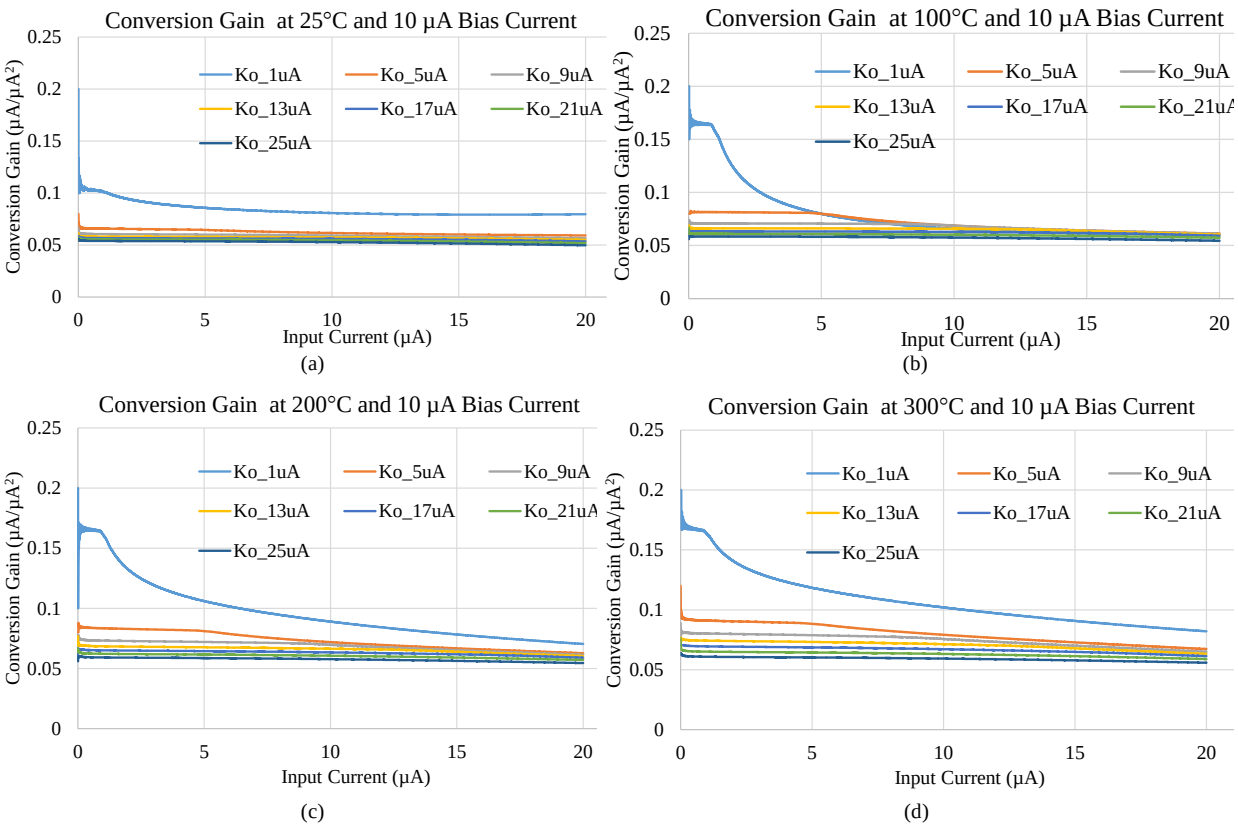


Fig. A9. Conversion gains for the multiplier circuit over temperature with ST models.

A.4. Simulation Results of the Full Flyback Controller

The full flyback controller was simulated over temperature with different test conditions. The inputs to the controller are voltage values representing the outputs of the sensors for the voltages and currents of the systems. Similar tables are seen in section 4.5.4. The simulation results show a 1% accuracy for DC simulated values.

Table A2. Flyback controller simulation results for 100 °C

Linear V-to-I Conversion and Normalization						
System Entity	Sensor Voltage	System Value	Governing Variable	Ideal Norm. Value	Linear Current Output	Controller Norm. Value
Output Voltage	4.36 V	198.2 V	v_{on}	0.991	17.21 µA	0.9902
Input Solar Voltage	3.61 V	27.3 V	v_{ccn}	0.8205	14.19 µA	0.8135
Output Current	2.533 V	0.495 A	i_{on}	0.00495	0.01 µA	0.0001
Primary Current	3.37 V	13.5 A	i_{mn}	0.0218	1.45 µA	0.0213
Secondary current	2.5 V	0 A				

Mathematical Operation for L_{OFF} and L_{ON} circuits							
Governing Variable	Ideal Norm. Value	Controller Current	Controller Norm. Value	Governing Variable	Ideal Norm. Value	Controller Current	Controller Norm. Value
$i_{mn} - i_{on}$	0.0168	1.26 µA	0.017	i_{ion}^2	0.0002	0.255 µA	0.015
$(i_{mn} - i_{on})^2$	0.00028	0.168 µA	0.073	$i_{vccn}*i_{von}$	0.813	16.91 µA	0.808
i_{von}^2	0.982	17.24 µA	1.002	$i_{vccn}*i_{1n}$	0.8204	17.02 µA	0.8134
i_{1n}	1	17.38 µA	1	$i_{mn}*i_{ion}$	0.00011	0.986 µA	0.00004
i_{1n}^2	1	16.97 µA	1	i_{offset}	---	0.963 µA	

Controller Decision for Switching FET							
Ideal Normalized Values			Controller Normalized Value			Decision Outputs	
Entity	Value	State	Entity	Value	State	Entity	State
λ_{off}	-0.017	***HI***	λ_{off}	-0.214 µA	***HI***	λ_{off}	***HI***
λ_{on}	-0.007	***HI***	λ_{on}	-0.017 µA	***HI***	λ_{on}	***HI***

Table A4. Flyback controller simulation results for 300 °C

Linear V-to-I Conversion and Normalization						
System Entity	Sensor Voltage	System Value	Governing Variable	Ideal Norm. Value	Linear Current Output	Controller Norm. Value
Output Voltage	4.42 V	200.9 V	v_{on}	1.0045	19.01 µA	1.004
Input Solar Voltage	3.59 V	27.2 V	v_{ccn}	0.8159	15.27 µA	0.8205
Output Current	2.567 V	1.005 A	i_{on}	0.01	1.303 µA	0.0172
Primary Current	2.5 V	0 A	i_{mn}	0.018	2.42 µA	0.0325
Secondary current	2.62 V	1.8 A				

Mathematical Operation for L_{OFF} and L_{ON} circuits							
Governing Variable	Ideal Norm. Value	Controller Current	Controller Norm. Value	Governing Variable	Ideal Norm. Value	Controller Current	Controller Norm. Value
$i_{mn} - i_{on}$	0.0079	1.255 µA	0.0165	i_{ion}^2	0.0001	0.112 µA	0.006
$(i_{mn} - i_{on})^2$	0.00006	0.112 µA	0.068	$i_{vccn}*i_{von}$	0.819	15.54 µA	0.8226
i_{von}^2	1.009	18.53 µA	1.002	$i_{vccn}*i_{1n}$	0.816	15.5 µA	0.8205
i_{1n}	1	18.93 µA	1	$i_{mn}*i_{ion}$	0.00018	0.355 µA	0.0006
i_{1n}^2	1	18.41 µA	1	i_{offset}	---	0.304 µA	

Controller Decision for Switching FET							
Ideal Normalized Values			Controller Normalized Value			Decision Outputs	
Entity	Value	State	Entity	Value	State	Entity	State
λ_{off}	0.009	***LO***	λ_{off}	0.12 µA	***LO***	λ_{off}	***LO***
λ_{on}	0.004	***LO***	λ_{on}	0.09 µA	***LO***	λ_{on}	***LO***

APPENDIX B

The Verilog and Matlab codes used to simulate the analog-to-digital converter are given in this section. Also, the simulated DNL and INL values of the ADC over temperature with TT and TF models are shown here as well.

B.1 Verilog Code for ADC Controller

The Verilog code for the SAR ADC controller is given below

```
// VerilogA for test_circutis, sar_adc_controller, veriloga

`include "constants.h"
`include "disciplines.h"

module sar_adc_controller(vd0, vd1, vd2, vd3, vd4, vd5, vd6, vd7, venable, vclk, vcomp, vdd, vcomplete, vcount);
input vcomp, vclk, venable;
output vd7, vd6, vd5, vd4, vd3, vd2, vd1, vd0, vcomplete, vcount;
inout vdd;
electrical vd7, vd6, vd5, vd4, vd3, vd2, vd1, vd0, vcomp, vclk, vdd, venable, vcomplete, vcount;

parameter real trise = 0.01u from [0:inf);
parameter real tfall = 0.01u from [0:inf);
parameter real tdel = 0.02u from [0:inf);
parameter real vlogic_low = 0;
```

```
real vlogic_high, vtrans, vtrans_clk;
integer d[0:7];
integer i;
integer count;
integer ven, vdone;

analog begin
// setup initial conditions
 vlogic_high = V(vdd);
 vtrans=(vlogic_high+vlogic_low)/2;
 vtrans_clk=vtrans;
 if (V(venable) > 0)
  ven = 1;
 else
  ven = 0;

// start of operation on clock, first setting up the enable command
@ (cross( V(vclk) - vtrans_clk, +1)) begin
  if (V(venable) > 0)
   ven = 1;
  else
   ven = 0;
```

```
// settting up the logic
  if (count == 0) begin
    d[7] = 1;
    count = count + 1*ven;
  end
  else if (count == 1) begin
    d[6] = 1;
    if (V(vcomp) > 1)
     d[7] = 1;
    else
     d[7] = 0;
    count = count + 1*ven;
  end
  else if (count == 2) begin
    d[5] = 1;
    if (V(vcomp) > 1)
     d[6] = 1;
    else
     d[6] = 0;
    count = count + 1*ven;
  end
  else if (count == 3) begin
    d[4] = 1;
```

```
  if (V(vcomp) > 1)
   d[5] = 1;
  else
   d[5] = 0;
  count = count + 1*ven;
end
else if (count == 4) begin
  d[3] = 1;
  if (V(vcomp) > 1)
   d[4] = 1;
  else
   d[4] = 0;
  count = count + 1*ven;
end
else if (count == 5) begin
  d[2] = 1;
  if (V(vcomp) > 1)
   d[3] = 1;
  else
   d[3] = 0;
  count = count + 1*ven;
end
else if (count == 6) begin
```

```
  d[1] = 1;
  if (V(vcomp) > 1)
   d[2] = 1;
  else
   d[2] = 0;
  count = count + 1*ven;
end
else if (count == 7) begin
  d[0] = 1;
  if (V(vcomp) > 1)
   d[1] = 1;
  else
   d[1] = 0;
  count = count + 1*ven;
end
else if (count == 8) begin
  count = count + 1;
  vdone = 1;
end
else begin
 for (i=7;i>=0;i=i-1) begin
   d[i] = 0;
 end
```

```
   count = 0;
   vdone = 0;
  end
end

//Transitions
     V(vd0) <+ transition(vlogic_high*d[0]*ven + vlogic_low*!d[0], tdel, trise, tfall);
     V(vd1) <+ transition(vlogic_high*d[1]*ven + vlogic_low*!d[1], tdel, trise, tfall);
     V(vd2) <+ transition(vlogic_high*d[2]*ven + vlogic_low*!d[2], tdel, trise, tfall);
     V(vd3) <+ transition(vlogic_high*d[3]*ven + vlogic_low*!d[3], tdel, trise, tfall);
     V(vd4) <+ transition(vlogic_high*d[4]*ven + vlogic_low*!d[4], tdel, trise, tfall);
     V(vd5) <+ transition(vlogic_high*d[5]*ven + vlogic_low*!d[5], tdel, trise, tfall);
     V(vd6) <+ transition(vlogic_high*d[6]*ven + vlogic_low*!d[6], tdel, trise, tfall);
     V(vd7) <+ transition(vlogic_high*d[7]*ven + vlogic_low*!d[7], tdel, trise, tfall);
     V(vcomplete) <+ transition(vlogic_high*vdone*ven + vlogic_low*!vdone, tdel, trise, tfall);
     V(vcount) <+ transition(vlogic_high*count + vlogic_low*!vdone, tdel, trise, tfall);

end
endmodule
```

B.2 Matlab Code for SAR ADC Characterization

The Matlab code to determine the INL and DNL of the SAR ADC from a dataset of the R-2R DAC is given below. The code must have corresponding analog voltages from the DAC over the full range of the input to properly function.

```
function [inl,dnl] = inldnl(x, delta)
% INLDNL   compute INL and DNL from converter output x
%      x       output from ADC
%      delta    spacing between codes. Default: 1
%
% AsSumptions & limitations:
%      - uniform quantizer
%      - TUT input to produce x: linear ramp

if nargin == 0
  error('must specify ADC output');
end
if nargin == 1
  delta = 1;
end

% compute histogram
[counts,centers] = hist(x, min(x):delta:max(x));
```

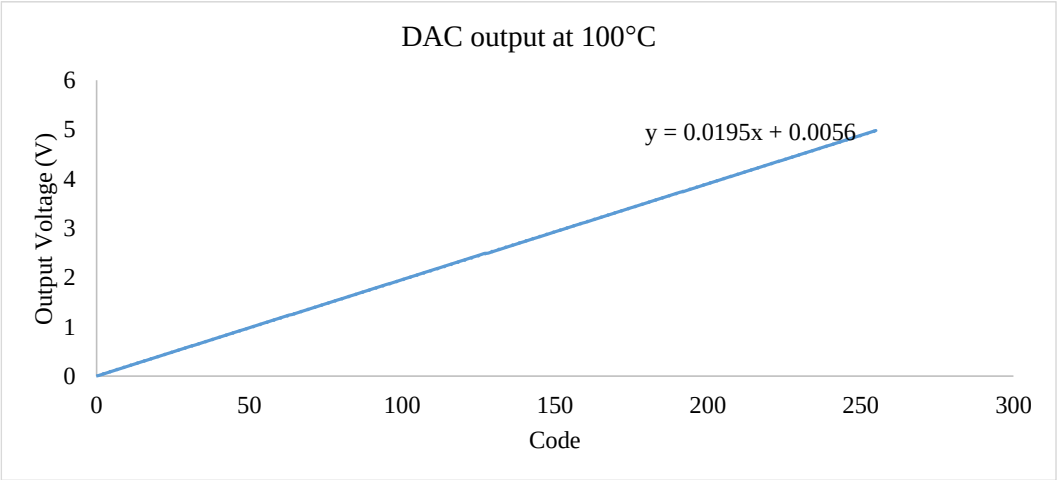
```
% eliminate end bins
counts(1)   = [];
counts(end) = [];

dnl = counts/mean(counts) - 1;
inl = cumSum(dnl);
inl = inl - linspace(inl(1), inl(end), length(inl));

if nargout==0
  % plot result
  N = length(dnl);
  if N > 16
    fmt = 'r-';
  else
    fmt = 'ro:';
  end
  subplot(2,1,1);
  plot(1:N, dnl, fmt, [1 N], [1 -1; 1 -1], 'b:');
  fixfig;
  xlabel('bin');  ylabel('DNL  [in LSB]');
  maxdnl = ceil(max(dnl));
  axis([1 N floor(min(dnl)) maxdnl+1]);
  text(0.1*N+1, maxdnl+0.2, ...
```

```
    sprintf('avg=%.2g,   std.dev=%.2g,   range=%.2g', ...
    mean(dnl),  std(dnl),  max(dnl)-min(dnl)));
  title(sprintf('DNL and INL of %.1g Bit converter (from histogram testing)', ...
    log2(N)));
  subplot(2,1,2);
  plot(1:N, inl, fmt, [1 N], [1 -1; 1 -1], 'b:');
  fixfig;
  xlabel('bin');  ylabel('INL  [in LSB]');
  maxinl = ceil(max(inl));
  axis([1 N floor(min(inl)) maxinl+1]);
  text(0.1*N+1, maxinl+0.2, ...
    sprintf('avg=%.2g,   std.dev=%.2g,   range=%.2g', ...
    mean(inl),  std(inl),  max(inl)-min(inl)));
end
```

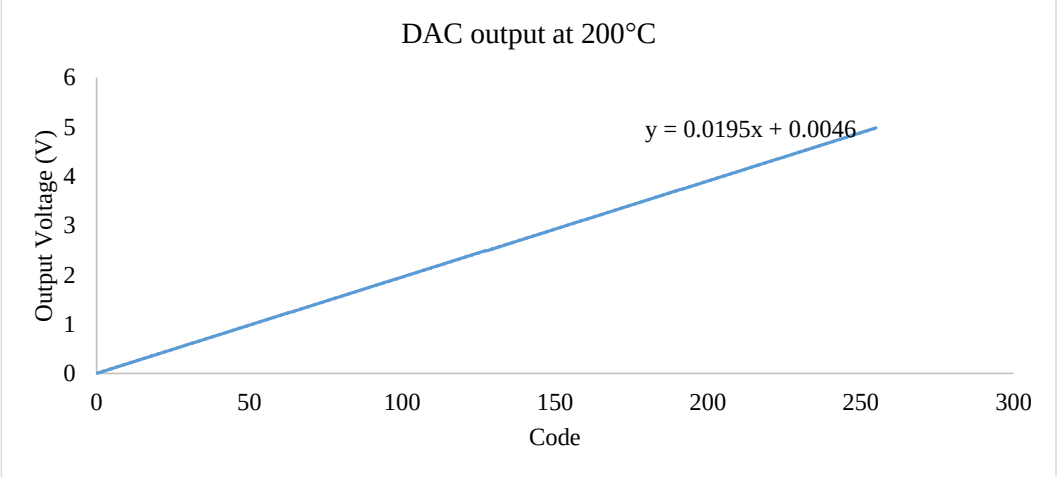
B.3 Further INL and DNL Simulation Results for 8-bit SAR ADC and R-2R DAC

Some of the simulation results have already been shown in section 4.4.2. A Summary of the results were then presented in a table for comparison. The results in section 4.4.2 were obtained with TT models. This section demonstrates some more simulation results of both the DAC and the ADC with TF models

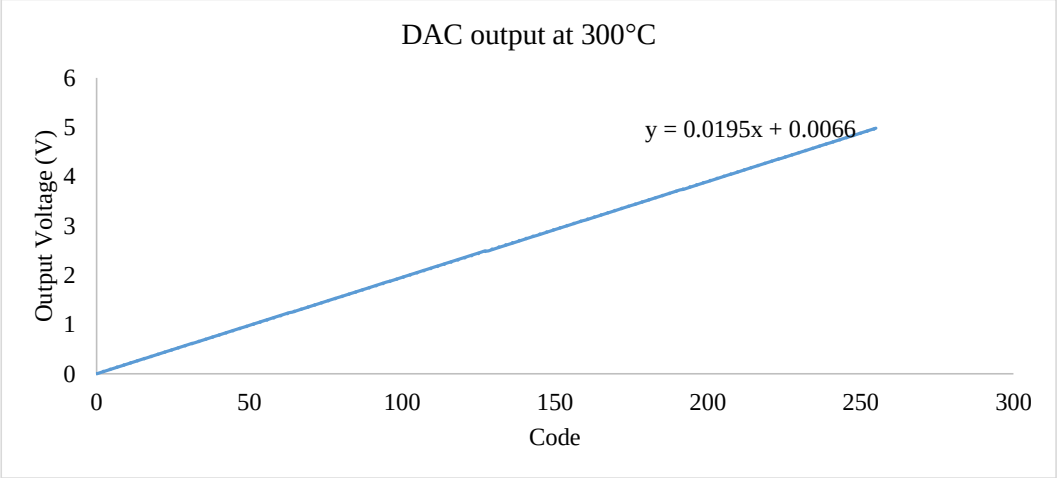
The DAC full scale conversion results are shown for 100C, 200C and 300C for the TF models. The DNL and INL results for all temperatures



(a)



(b)



(c)

Fig. B1. DAC full conversion over temperature with TT models.

The DAC INL results are shown here, while the DAC DNL results are shown in the next page.

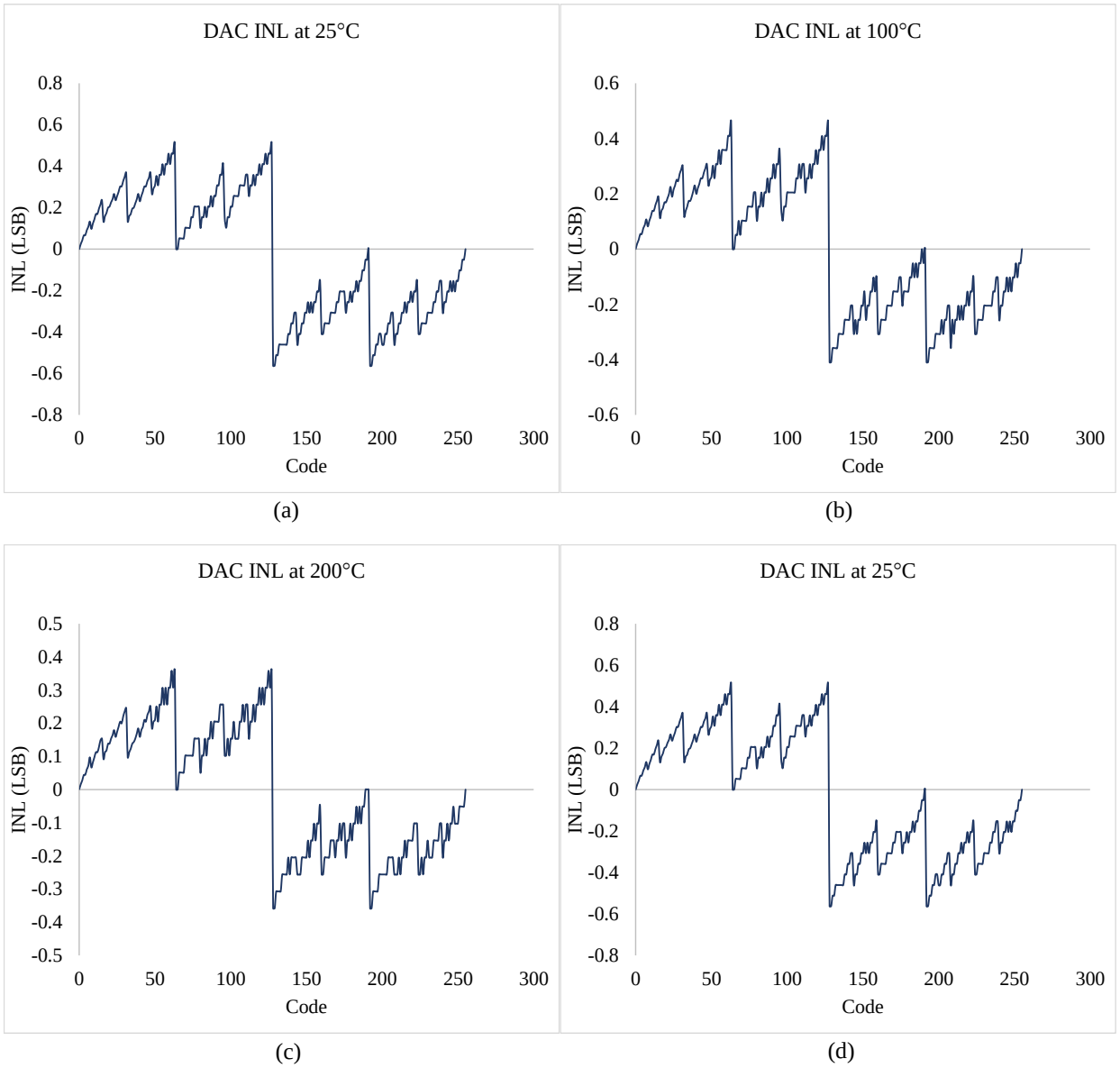


Fig. B2. DAC INL simulation results at different temperatures.

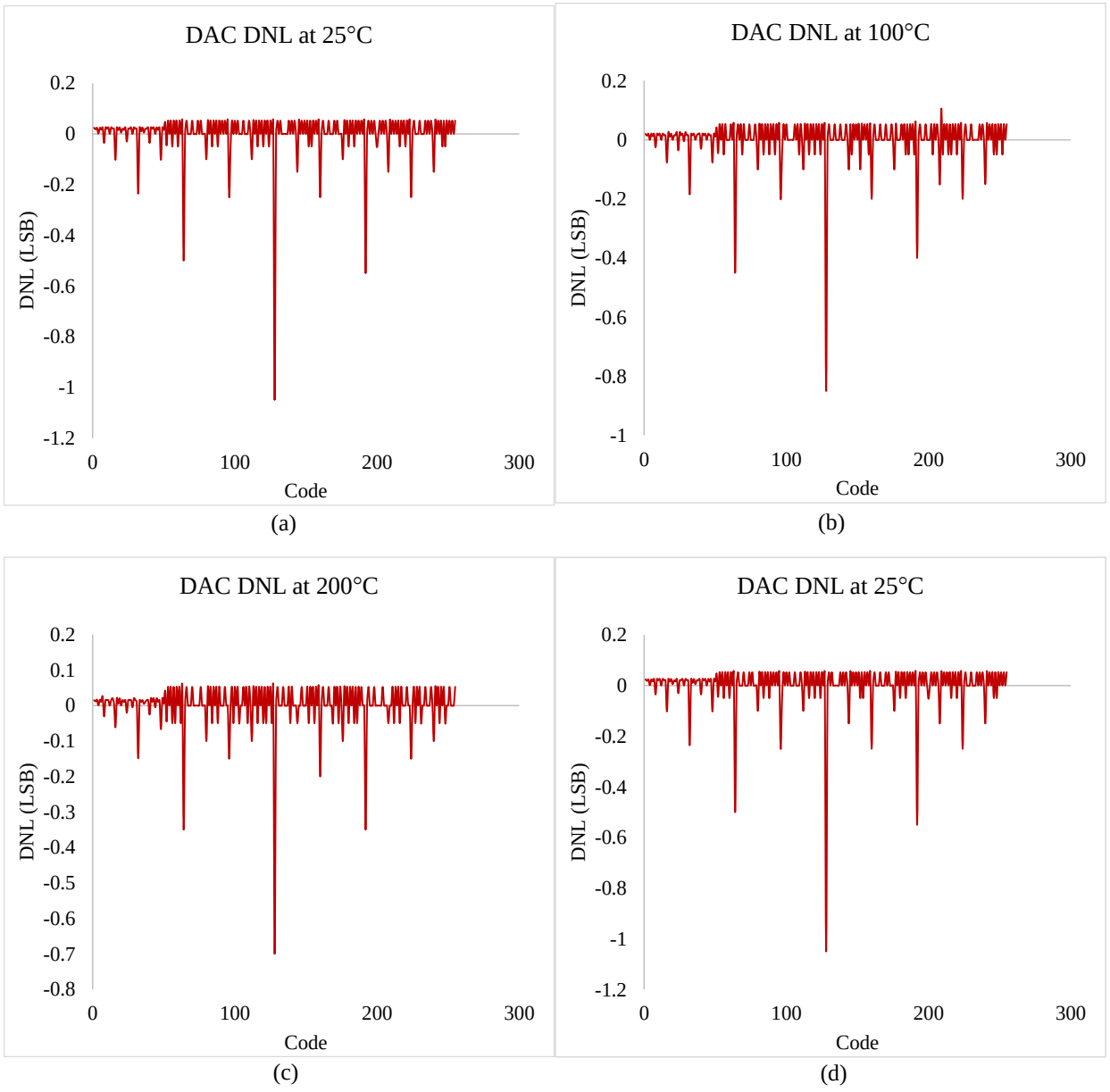
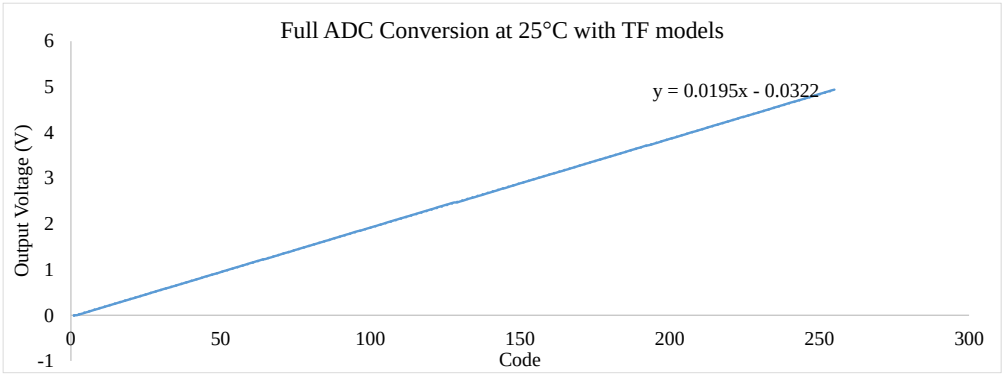
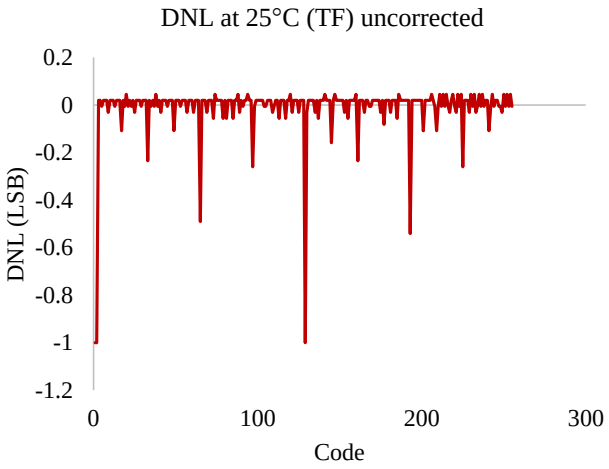


Fig. B3. DAC DNL simulation results over temperature with TF models.

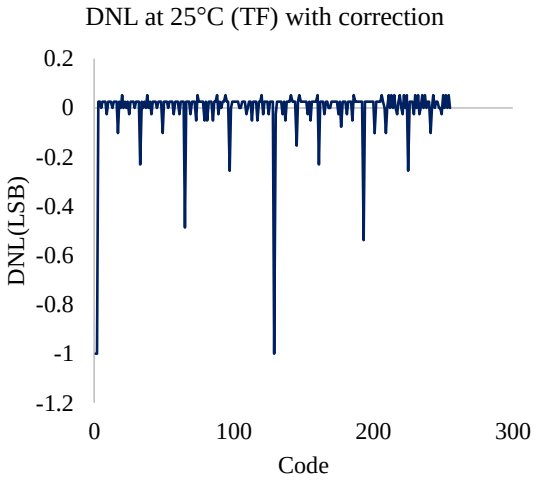
The simulation results of the SAR ADC with TF models are shown in the following pages. These include the full conversion, uncompensated DNL and INL measurements, and offset and gain corrected DNL and INL measurements for all available temperatures.



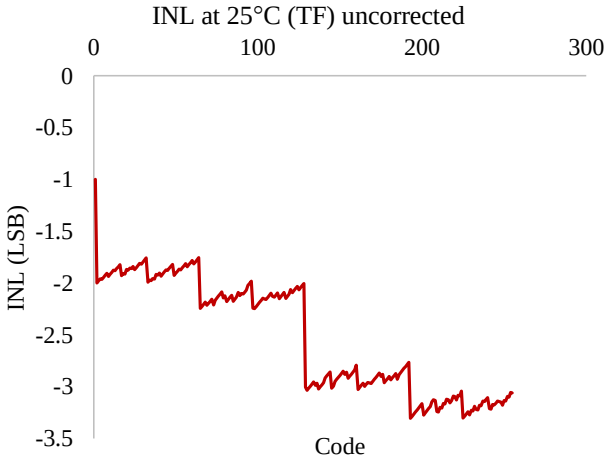
(a)



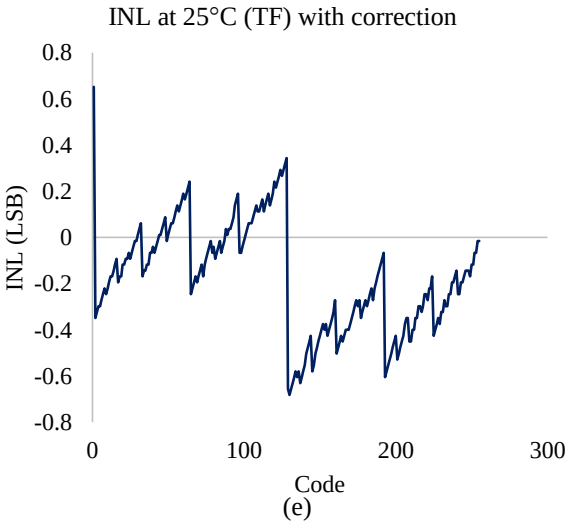
(**b**)



(c)

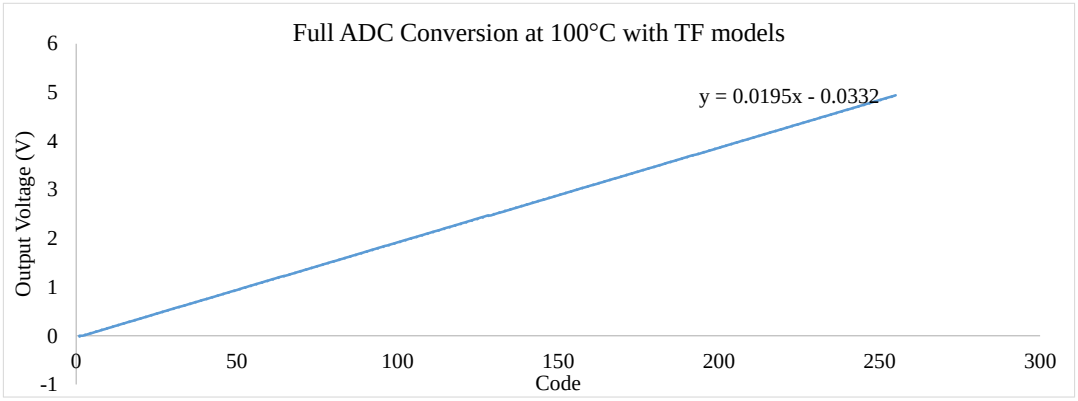


(d)

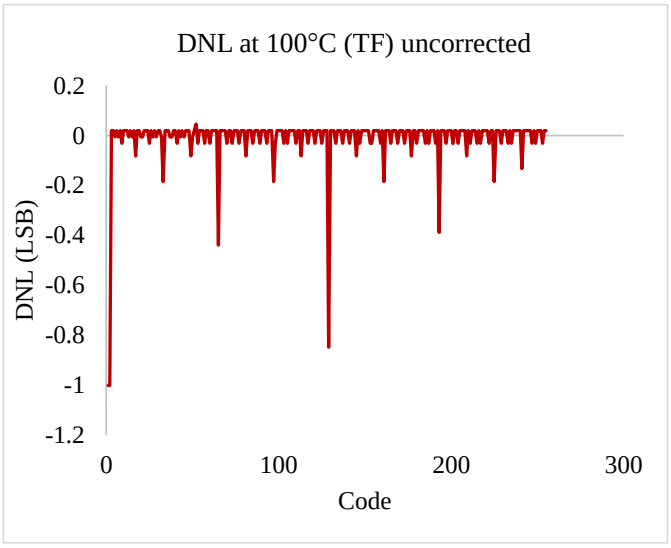


(e)

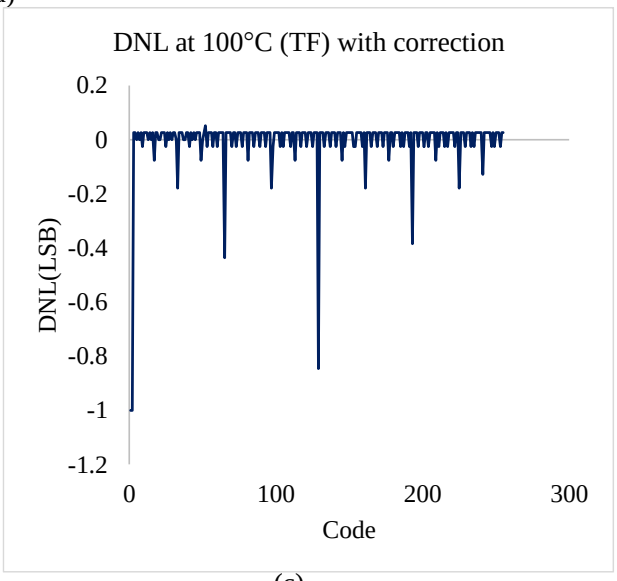
Fig. B4. ADC conversion simulation results at 25 °C.



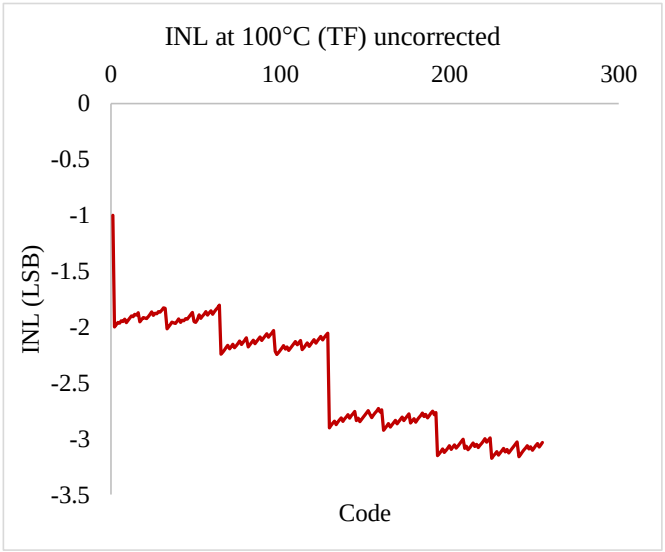
(a)



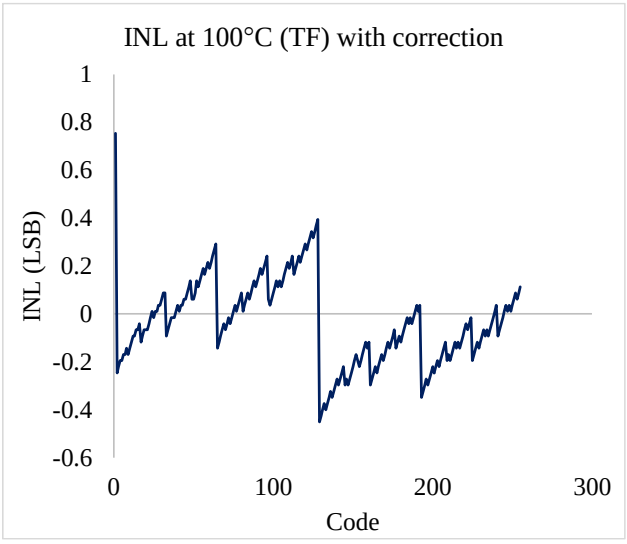
(**b**)



(c)

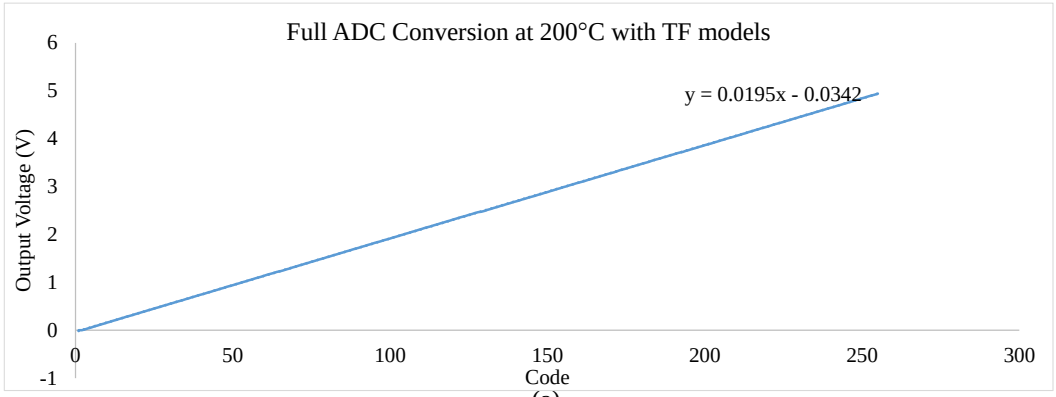


(d)

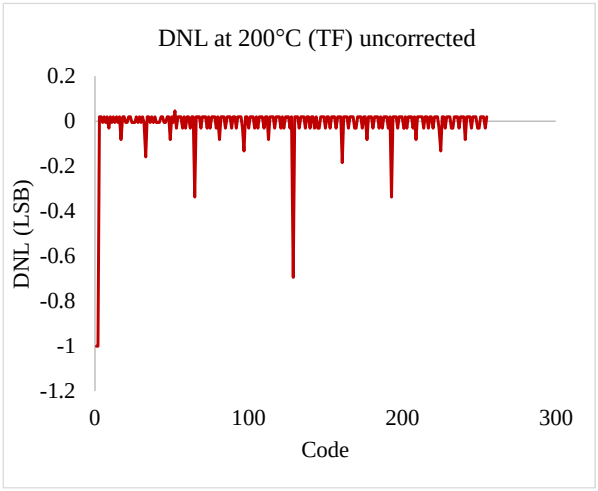


(e)

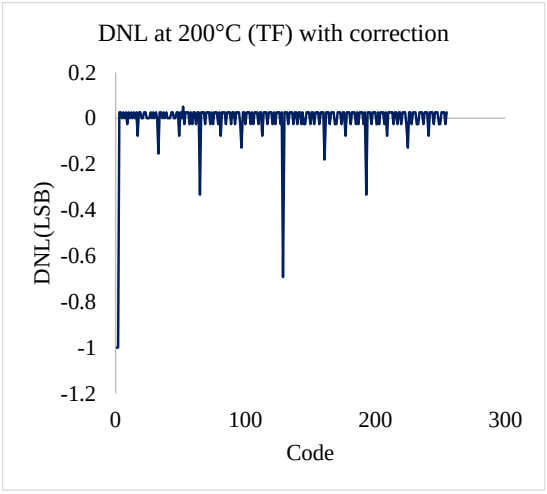
Fig. B5. ADC conversion simulation results at 100 °C.



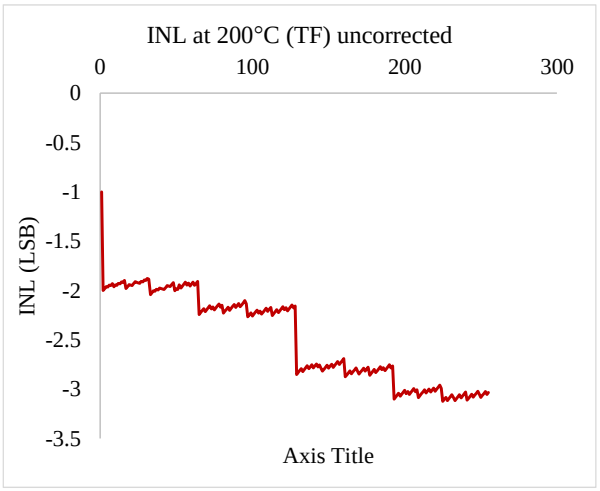
(a)



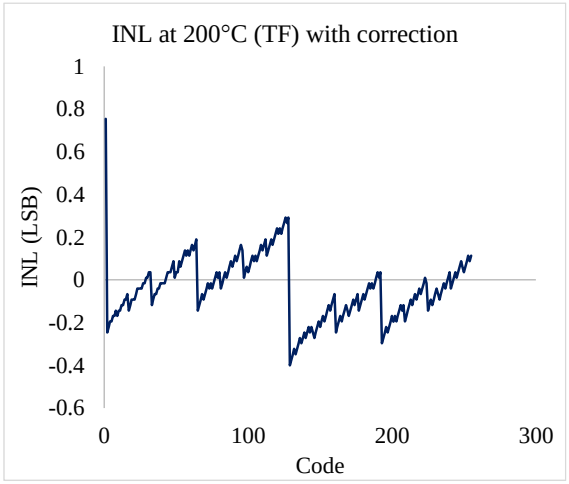
(**b**)



(c)

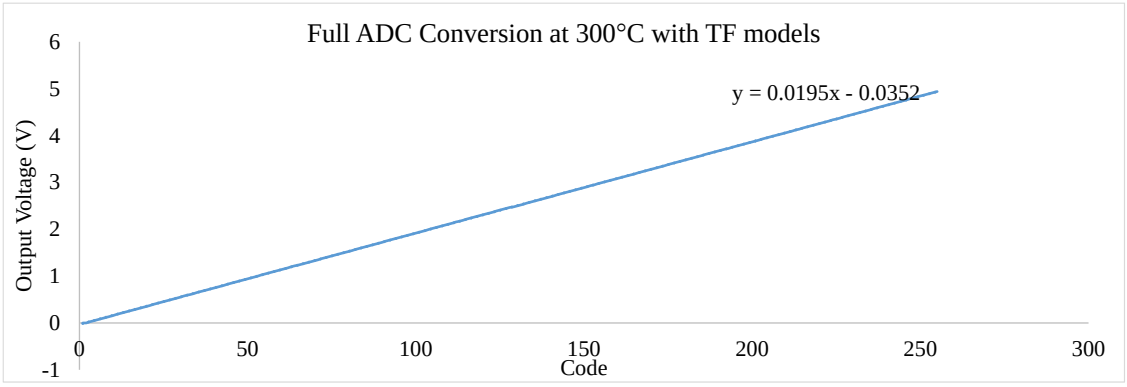


(d)

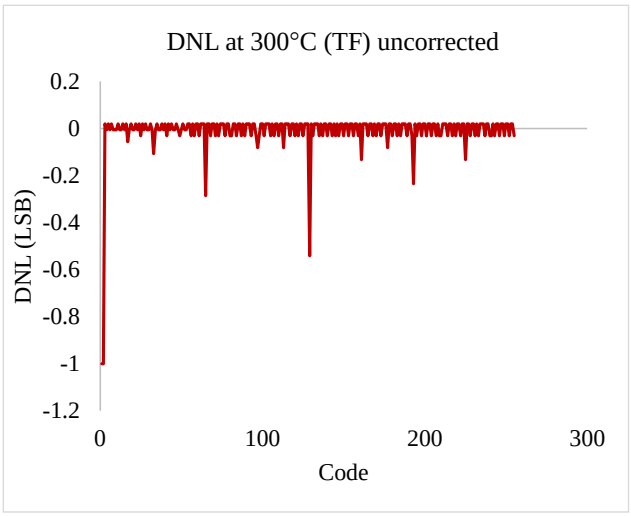


(e)

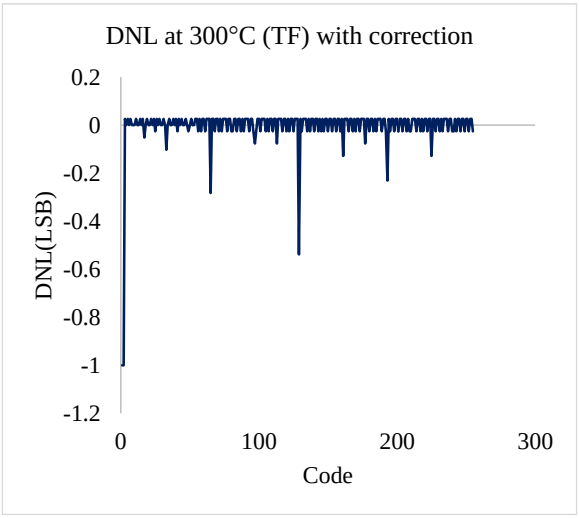
Fig. B6. ADC conversion simulation results at 200 °C.



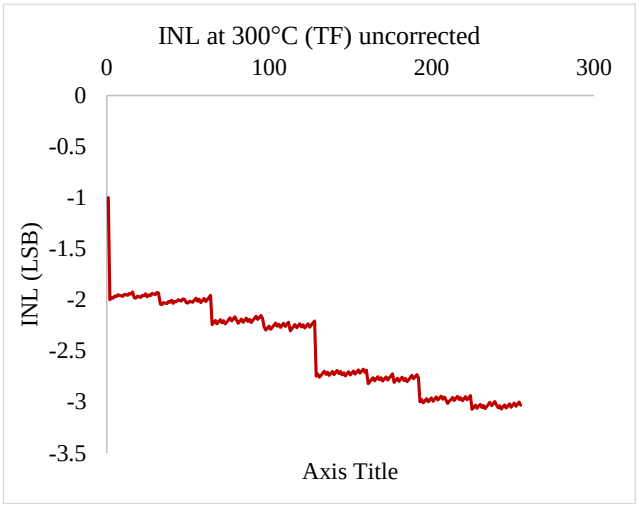
(a)



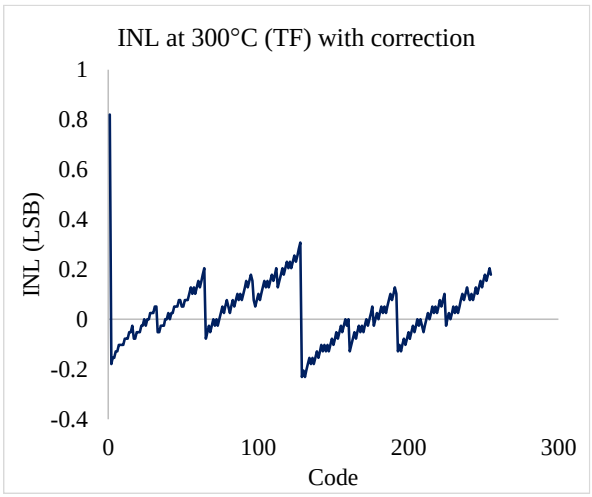
(**b**)



(c)



(d)



(e)

Fig. B7. ADC conversion simulation results at 300 °C.