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Wideband Low Noise Oscillator suitable for Injection Locking

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"One, remember to look up at the stars and not down at your feet. Two, never give up work. Work gives you meaning and purpose and life is empty without it. Three, if you are lucky enough to find love, remember it is there and don't throw it away."

- Stephen Hawking

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Abstract

There is a growing need to design compact and low power transceiver circuits. The increasingly crowded frequency spectrum leads to increased challenges associated with transceiver design. In particular, it becomes imperative that the oscillator circuits have a low phase noise.

RC oscillators have the ability to produce wideband oscillations with reduced area and low power consumption. However, a serious drawback is its high phase noise, which leads to poor circuit performance.

To improve the performance of an RC oscillator, it is common for it to be integrated into a frequency synthesizer. The most common approach of a synthesizer is the Phase-Locked Loop (PLL). This approach leads to an increase in the area and complexity of the circuit. Another approach to a synthesizer is an Injection-Locked Oscillator (ILO), which achieves similar performances to a PLL without the disadvantages referred to above.

In this thesis, an ILO based on an RC oscillator, using a Spin Torque Oscillator (STO) as a reference generator, is presented. The circuit is implemented in two different Complementary Metal-Oxide-Semiconductor (CMOS) technologies: 130 nm CMOS and 180 nm CMOS. The STO used as reference has characteristics similar to a nanometric device developed at the International Iberian Nanotechnology Laboratory (INL). In addition, the ILO operates in a wide frequency band ranging from 100 MHz to 3 GHz, has a power consumption ranging from 2.94 mW to 6.81 mW for 130 nm CMOS technology, whereas in 180nm CMOS technology it consumes between 4.86 mW and 13.96 mW.

Thus, the work developed in the course of this thesis serves as proof of concept for the manufacture of a fully integrated hybrid ILO using the STO technology in conjunction with CMOS circuits.

Keywords: CMOS, RC Oscillator, Injection Locking, Phase Noise, Radio Frequency, Wideband.

Resumo

É cada vez maior a necessidade de projetar circuitos transceptores compactos e de baixa potência. O espectro de frequências cada vez mais sobrelotado leva a que haja desafios acrescidos associados ao projecto dos transceptores. Em particular, torna-se imperativo que os circuitos osciladores tenham um baixo ruído de fase.

Os osciladores RC têm a capacidade de produzir oscilações com uma grande largura de banda enquanto apresentam baixos consumos de potência e áreas reduzidas. Porém, uma desvantagem séria é o seu elevado ruído de fase, que leva a baixos desempenhos do circuito.

Para melhorar o desempenho de um oscilador RC, é comum este ser integrado num sintetizador de frequência. A abordagem mais comum de um sintetizador é a malha de captura de fase (PLL). Esta abordagem implica um aumento na área e complexidade do circuito. Outra abordagem para um sintetizador é um oscilador sincronizado por injeção (ILO), que atinge desempenhos semelhantes a uma PLL sem as desvantagens referidas anteriormente.

Nesta tese, é proposto um ILO, baseado num oscilador RC, que usa um nano-oscilador por trasferência de spin (STO) como gerador de referência. O circuito é implementado em duas tecnologias distintas: CMOS 130nm e CMOS 180 nm. O STO usado como referência tem caracteristicas semelhantes a um dispositivo nanométrico desenvolvido no Laboratório Ibérico Internacional de Nanotecnologia (INL). Para além disso, o ILO opera numa banda larga de frequências desde os 100 MHz até aos 3 GHz, tem consumo de potência de 2.94 mW a 6.81 mW para a tecnologia CMOS 130 nm, enquanto que na tecnologia CMOS 180 nm consome entre 4.86 mW a 13.96 mW de potência.

Assim sendo, o trabalho desenvolvido no decorrer desta tese serve de prova de conceito para o fabrico de um ILO híbrido e totalmente integrado que use a tecnologia do STO em conjunto com circuitos CMOS.

Palavras-chave: CMOS, Oscilador RC, Sincronização por Injeção, Ruído de fase, Radiofrequência, Banda Larga.

Contents

List of Figures

List of Tables

Acronyms

AC	Alternating Current.
ADC	Analog to Digital Converter.
BPF	Band-Pass Filter.
CCO	Current Controlled Oscillator.
CMOS	Complementary Metal-Oxide-Semiconductor.
CNR	Carrier to Noise Ratio.
CS BPF	Channel Select Band-Pass Filter.
DC	Direct Current.
DSP	Digital Signal Processing.
FoM	Figure of Merit.
GMR	Giant Magnetoresistance.
GSM	Global System for Mobile communications.
HF	High Frequency.
I/Q	In-Phase and Quadrature.
IF	Intermediate Frequency.
ILO	Injection-Locked Oscillator.
INL	International Iberian Nanotechnology Laboratory.
IR BPF	Image Rejection Band-Pass Filter.
ISM	Industrial, Scientific and Medical.
LF	Loop Filter.
LNA	Low Noise Amplifier.

LO	Local Oscillator.
LPF	Low-Pass Filter.
LTE	Long-Term Evolution.
MOS	Metal-Oxide-Semiconductor.
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor.
MTJ STO	Magnetic Tunnel Junction Spin Torque Oscillator.
NF	Noise Figure.
NMOS	N-Channel Metal-Oxide-Semiconductor.
PD	Phase Detector.
PLL	Phase-Locked Loop.
PMOS	P-Channel Metal-Oxide-Semiconductor.
PSD	Power Spectral Density.
PSS	Periodic Steady-State.
QAM	Quadrature Amplitude Modulation.
RF	Radio Frequency.
RMS	Root Mean Square.
SHF	Super High Frequency.
SNR	Signal-to-Noise Ratio.
SoC	System on a Chip.
SSB	Single-Sideband.
STO	Spin Torque Oscillator.
STT	Spin Transfer Torque.
SV STO	Spin Valve Spin Torque Oscillator.
TMR	Tunneling Magnetoresistance.
UHF	Ultra High Frequency.
UMTS	Universal Mobile Telecommunications System.
VCO	Voltage Controlled Oscillator.
VCRO	Voltage Controlled Ring Oscillator.

VHF Very High Frequency.

CHAPTER 1

INTRODUCTION

1.1 Background and Motivation

Connectivity is a growing need in today's society, especially through wireless technologies, which forces the industry to produce compact devices with greater autonomy. To meet these requirements, it becomes imperative that the electronic circuits which allow the transmission and reception of signals, known as transceivers, have lower areas along with lower power consumption and voltage supply. Therefore, it is desirable to use CMOS technology, which enables design of circuits that possess such characteristics while also being able to operate at high frequencies [1]. CMOS technology is also advantageous to fully integrate the transceiver, allowing manufacturers to put the entire electronic System on a Chip (SoC).

In a transceiver there are two types of circuit that are constantly switched: transmitter and receiver. The transmitter's main features are modulation, upconversion and power amplification while the receiver is responsible for low noise amplification, down-conversion and demodulation. Due to the wide variety of existing communication standards, the frequency spectrum is overcrowded. This makes the receiver's Radio Frequency (RF) blocks specifications more demanding than the transmitter's, since requirements such as integrability, band selectivity and interference rejection become critical on the receiving end. For this reason, receivers are the most critical circuits of transceivers, which explains the major concern in the scientific research of receiver improvements. Commonly, transceiver designers define RF front-end as being a part of the receiver circuit that processes the incoming signal in its analog form, thus being the interface between the antenna and the Analog to Digital Converter (ADC).

As previously mentioned, upconversion and down-conversion are processes of frequency translation that are inherent to any transceiver. These operations are performed by

mixers, which are blocks that generally have two inputs: the signal to be down-converted or up-converted and a periodic wave generated by a Local Oscillator (LO). For this reason, in addition to mixers, oscillators are key building blocks for any transceiver.

An oscillator is a circuit whose main function is to convert a Direct Current (DC) power at its input into an Alternating Current (AC) signal, which has a periodic waveform [2]. According to its output, an oscillator can be classified as quasi-linear or harmonic, if it produces a sine wave, or it can be a strongly non-linear or relaxation oscillator, if it generates a non-sinusoidal wave. It is also common to classify these types of circuits according to the networks of passive elements that they use to obtain oscillations. If the circuit uses passive networks made up of inductors and capacitors then this is known as an LC oscillator. If the passive networks are constituted by resistors and capacitors, then the circuit is an RC oscillator. In addition, it is common practice to design the oscillator so that its output frequency is controlled within a certain range by an input voltage. In these cases the circuit is known as a Voltage Controlled Oscillator (VCO).

The growing demand for wireless communication among a wide variety of mobile electronic devices means that integrability, low cost and low power consumption are increasingly critical requirements. To meet these needs, RC oscillators are the most suitable topology to implement the LO because of their small areas and wide tuning range.

The main constraint on the performance of oscillators is their phase noise, which means that the focus of research over the last few years has been an attempt to improve it through various techniques such as the use of a noise filter in harmonic oscillators [3], class-D oscillator topologies [4, 5], as well as coupled quadrature oscillators [6, 7] and complementary VCO with implicit common-mode resonance [8].

The techniques described above were applied to LC oscillators, which are the ones with the best phase noise performance. As for RC oscillators, the most common method to reduce their phase noise is the use of frequency synthesizers.

A widely known frequency synthesizer structure is the PLL, where the VCO is enclosed in a feedback loop, along with other blocks, in order to minimize the phase difference between a reference signal and the VCO output. Since it is a feedback loop, the design of a PLL must be careful and complex in order to avoid stability issues and high synchronization times. Furthermore, the implementation of this frequency synthesizer leads to an increase in both the circuit die area and the power consumption of the transceiver [1].

Frequency synthesizers based on injection locking are another type of phase noise improvement technique for RC oscillators. In these synthesizers, the direct injection of the reference signal into a VCO node is sufficient for synchronization, achieving a performance comparable to that of a PLL without having the same disadvantages [9, 10]. The main advantage of this type of synthesizer is that it is a simple structure that requires neither additional blocks nor feedback and the concerns associated with it. However, a drawback to this approach is that, unlike a PLL, the reference signal must operate in the

same frequency range as the VCO.

The generation of the reference signal can be performed by a crystal oscillator [11] or by a STO [12]. Crystal-based wave generators produce a fixed frequency, which leads to a low flexibility of the synthesizer. For this reason, an ILO with a crystal reference generator does not have considerable advantages over a PLL, which can be programmed to perform frequency hopping by adjusting a frequency division block present in its feedback loop. In addition, crystal oscillators have a reduced frequency of operation, up to a few hundred MHz, making it impossible to use them as a reference for an ILO operating in the GHz range.

On the other hand, the reference signal generator may be an STO, which is a relatively new nanostructure under ongoing research [13–15]. The manufacture of these nanostructures is compatible with CMOS processes. In addition, an STO is capable of producing oscillations in the GHz frequency range with large tunability. For these reasons, the use of an STO as a reference generator has the potential to allow implementation of a fully integrated ILO with high phase noise performance and wide tuning range.

This thesis aims to implement a CMOS ILO based on an RC oscillator, as presented in [16]. In this work, it is considered that the reference signal is based on an STO with characteristics similar to those of a frequency sensor developed at the INL, located in Braga (Portugal) [17]. The referred frequency sensor is a nanometric device that generates a DC voltage proportional to the frequency of an RF signal that is transmitted through the device. In addition, this structure shows an adjustable frequency range starting from hundreds of MHz ([100-600 MHz] for operation in the gyrotropic mode), up to a few GHz ([1-12 GHz] for operation in azimuthal mode), while it has a power consumption ranging from $1\mu W$ to $15\mu W$.

1.2 Main Contributions

This work presents the design of a fully integrated ILO with an STO as a reference generator. The proposed circuit was implemented in two different CMOS technologies:

- 130 nm CMOS with a 1.2 V supply voltage, which is a low cost technology.
- 180 nm CMOS with a 1.8 V supply voltage, since this technology is compatible with the manufacturing process of the STO under consideration [13, 14].

These oscillators feature high phase noise performance and a wide tuning range of [100 MHz - 3 GHz], covering the whole Global System for Mobile communications (GSM) frequency band and the vast majority of the Universal Mobile Telecommunications System (UMTS) and the Long-Term Evolution (LTE) bands. The reference signal used in simulations has similar characteristics to those of a nanometric device developed at the INL. Thus, this work serves as proof of concept for the manufacture of a hybrid circuit with this technology in conjunction with CMOS devices.

1.3 Thesis Organization

This dissertation is structured in seven chapters, including this introduction, organized as follows:

Chapter 2 – Background on RF receivers using CMOS technology

This chapter presents a brief review of the most important concepts of the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) theory, thus providing the reader with a basis for understanding one of the basic functional units of most RF circuits. Furthermore, the different types of noise present in receivers and how to measure its impact on circuit performance are concepts presented in this chapter. In addition, an overview of the main wireless receiver architectures is provided.

Chapter 3 – CMOS Oscillators

This chapter presents fundamental concepts about the operation of oscillator circuits, including the main parameters for measuring their performance. An overview of the main CMOS oscillator implementations is also provided, concluding with a reference to the state-of-the-art oscillators for each topology type (LC and RC).

Chapter 4 – Injection Locking

The main techniques of phase noise reduction are referred to in this chapter, starting with a greater focus on the most efficient technique: the use of frequency synthesizers. Subsequently, the phenomenon of injection locking is further explored and discussed.

Chapter 5 – Reference Signal Generators

In this chapter, the two types of circuits that produce reference signals for frequency synthesizers are described: the crystal oscillator and the STO. In addition, both types of reference generator are discussed, in order to identify the most suitable for the implementation of a fully integrated wideband ILO.

Chapter 6 – Injection Locked RC Oscillator with STO as reference generator

This chapter presents the design of an ILO based on an RC oscillator. This ILO uses an STO as a reference generator.

Two different implementations of the ILO are made using 130 nm CMOS and 180 nm CMOS technologies. In addition, for each of these technologies, an implementation of the free-running RC oscillator is made.

Moreover, the results of the simulations applied to the implemented circuits are presented and discussed.

Chapter 7 – Conclusions and Future Work

In this last chapter the conclusions of the work developed in the course of this thesis are drawn. Some suggestions are also given to further complement what has been achieved in this research topic.

Chapter 2

Background on RF receivers using CMOS technology

When a system uses air as its communication channel, it must be taken into account that, due to the characteristics of the channel, the received signals will be greatly attenuated and will suffer strong interferences. This means that in a wireless communication system, the receiving antenna will pick up a signal with extremely low amplitude and a considerable amount of noise. All of these constraints have a greater impact on receiver design than on the transmitter. In addition, it is common in these systems for signals to propagate at high frequencies, allowing the size reduction of antennas and more information to be transmitted using higher bandwidth. Thus, the RF front-end is a crucial part of a receiver, since it is responsible for amplifying the received signal with minimal introduction of noise and for downconverting this signal, so that it can be processed by a digital system. For these reasons, the main functional blocks of a wireless receiver are the Low Noise Amplifier (LNA), the LO and the mixer.

The reception of highly noisy signals leads to specific problems in the design of the receiver LO, since it must be designed to have a narrow spectral component so that the receiver has good channel selectivity and good interference rejection [1].

As mentioned in the introductory chapter, CMOS technology enables the design of low-area circuits capable of operating at high frequencies, together with low power consumption [1]. It is these advantages that make this the most popular technology for designing RF microcircuits. Consequently, the MOSFET is one of the basic functional units of the vast majority of RF circuits. Therefore, this chapter starts with a review of the basic concepts that involve MOSFET operation. Furthermore, this chapter has the following main objectives: an introduction to noise and its impact on the performance of RF circuits implemented with CMOS technology. Finally, an overview of the main architectures of wireless receivers is presented.

2.1 Types of MOSFET

There are two types of Metal-Oxide-Semiconductor (MOS) transistors: n-channel devices (N-Channel Metal-Oxide-Semiconductor (NMOS)), which use electrons to conduct current, and p-channel devices (P-Channel Metal-Oxide-Semiconductor (PMOS)) that use holes for the same effect. In addition, NMOS transistors conduct with a positive gate voltage, whereas PMOS devices conduct with a negative gate voltage. Since these transistors have complementary characteristics, microcircuits that use both NMOS and PMOS devices are called CMOS circuits.

There are many symbols that are used to represent a MOSFET according to the type of channel it has. Fig. 2.1 illustrates some symbols that are commonly used to represent NMOS transistors.

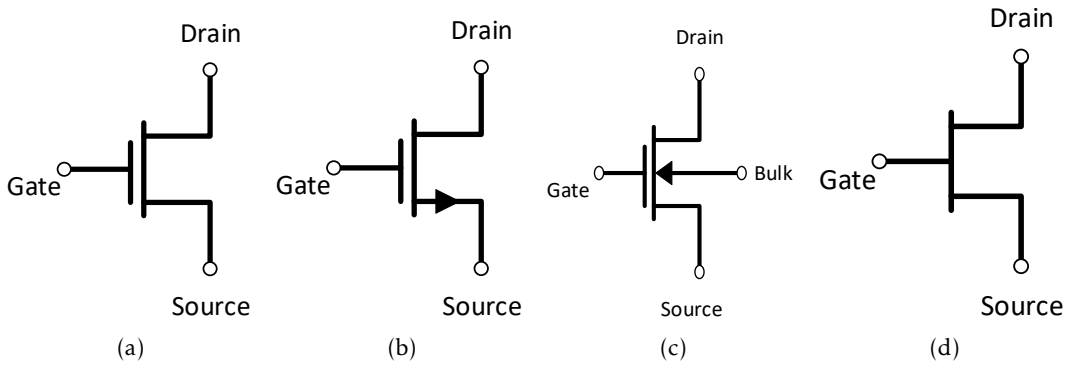

Figure 2.1: Commonly used symbols for NMOS transistors (adopted from [18]).

As shown by Fig. 2.1(c), a MOSFET is a four-terminal device, with the Bulk being a terminal that represents the device's substrate. In NMOS transistors, their p^- type substrate is normally connected to the lowest potential in the circuit. In such cases the Bulk terminal is normally omitted, as shown in Figs. 2.1(a), 2.1(b) and 2.1(d). Likewise, PMOS devices have a n^- type substrate, which is usually connected to the highest voltage in the microcircuit. Fig. 2.1(b) is the most commonly used symbol for NMOS transistors in analog design. In this representation, an arrow points outward on the source terminal indicating the direction of current in this transistor's channel.

Fig. 2.2 illustrates some symbols that are widely used to represent PMOS transistors.

2.2 MOSFET Large-Signal Behaviour

2.2.1 Basic Operation

It is possible to understand the basic operation of the MOSFET by simply studying the behavior of an NMOS transistor.

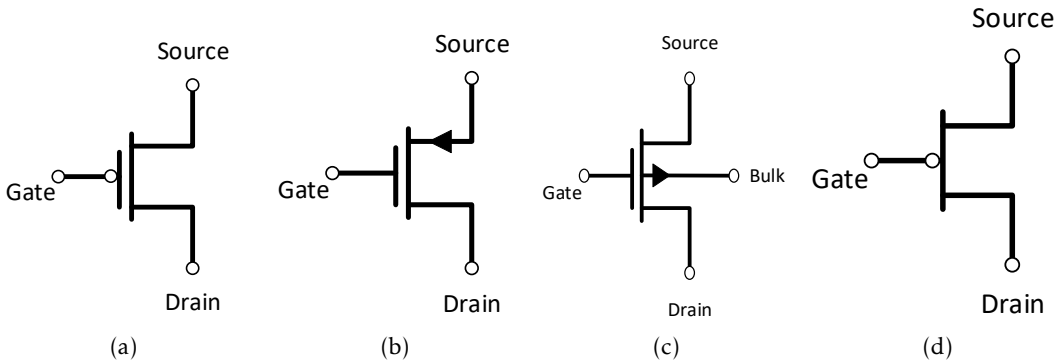

Figure 2.2: Commonly used symbols for PMOS transistors (adopted from [18]).

The voltage between the gate and the source terminals, V_{GS}, is an important parameter in the definition of the current conduction state of an NMOS transistor. For values of V_{GS} satisfying the condition $V_{GS} \leq 0$, it is assumed that the transistor is off and there is no current flowing between drain and source.

The gate-source voltage, at which the concentration of electrons immediately under the gate is equal to the concentration of holes in the substrate p^-, further away from the gate, is widely known as the transistor threshold voltage and denoted V_{tn} (for NMOS transistors). When $0 < V_{GS} \leq V_{tn}$, small amounts of subthreshold current can flow from drain to source, as this region is in depletion [19]. Under these conditions, the transistor is in weak inversion and is said to be operating in the subthreshold region.

When $V_{GS} > V_{tn}$, a channel is created in the substrate region located between drain and source. This channel is formed by inverting the substrate surface of type p^- to type n^-. Thus, the induced channel is also known as the inversion layer [19]. Under these conditions, a positive current, I_D, flows from drain to source and as V_{GS} increases in value so does the charge density in the channel. For this reason, there is usually a distinction between moderate inversion ($V_{GS} > V_{tn}$) and strong inversion ($V_{GS} >> V_{tn}$).

The charge density in the channel is proportional to the difference $V_{GS} - V_{tn}$, which is often referred to as the effective voltage or the overdrive voltage. In this thesis, the effective voltage will be denoted, as indicated in Eq. (2.1), as V_{Dsat} (representing the V_{DS} saturation voltage).

$$V_{Dsat} \equiv V_{GS} - V_{tn} \tag{2.1}$$

In Fig. 2.3 the characteristic $i_D - v_{GS}$ of a 65 nm technology NMOS transistor is shown in blue. The NMOS transistor whose characteristic is studied in Fig. 2.3 has the following channel dimensions: a channel width, $W = 4\mu m$, and a channel length, $L = 2\mu m$. Furthermore, it was simulated with Cadence® SpectreRF and BSIM3v3 MOSFET models. This characteristic was obtained by setting the voltage between the drain and source, $V_{DS} = 1.2V$. The study of Fig. 2.3 allows to understand the i_D-v_{GS} characteristic of a

generic NMOS transistor, where the modes of operation of the device corresponding to each range of V_{GS} values are indicated.

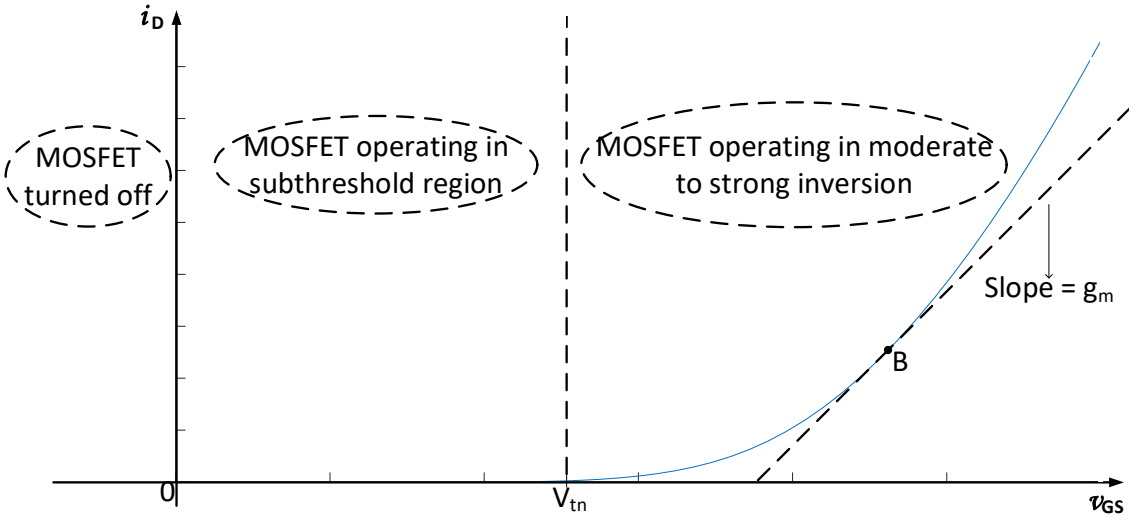

Figure 2.3: $i_D - v_{GS}$ curve of an NMOS transistor.

In this figure, there is also a graphical representation of the transistor transconductance, g_m, which can be understood as the slope of the straight line tangent to the $i_D - v_{GS}$ curve at the bias point, B. Thus, g_m is defined in Eq. (2.2).

$$g_m = \frac{\partial i_D}{\partial v_{GS}} \tag{2.2}$$

Rearranging the graph of Fig. 2.3 to analyze i_D as a function of $v_{Dsat} = v_{GS} - V_{tn}$, results in Fig. 2.4, where it is possible to verify that the tangent of bias point B crosses the horizontal axis near $\frac{V_{Dsat}}{2}$.

A simpler MOSFET model than the BSIM3v3 used to simulate the NMOS studied in Fig. 2.4 and which is widely used in the community of CMOS circuit designers is known as the quadratic model, since it takes a quadratic variation between i_D and v_{GS}. In addition, the quadratic model assumes the approximation defined in Eq. (2.3).

$$g_m = \frac{I_D}{\frac{1}{2} V_{Dsat}} \tag{2.3}$$

In fact, g_m is one of the key parameters in transistors design, since it is a factor of great importance in defining the intrinsic gain of a transistor [19].

The gain of a system translates into the ratio between the amplitude of the output signal and the amplitude of the input signal, measuring the ability of the system to affect the amplitude of an input signal, ideally without the introduction of distortions [19].

If the system under discussion produces at its output a signal of amplitude equal to that of the input signal, the system has unity gain. If the system outputs a higher amplitude signal than the input signal, then the gain of this system is greater than unity,

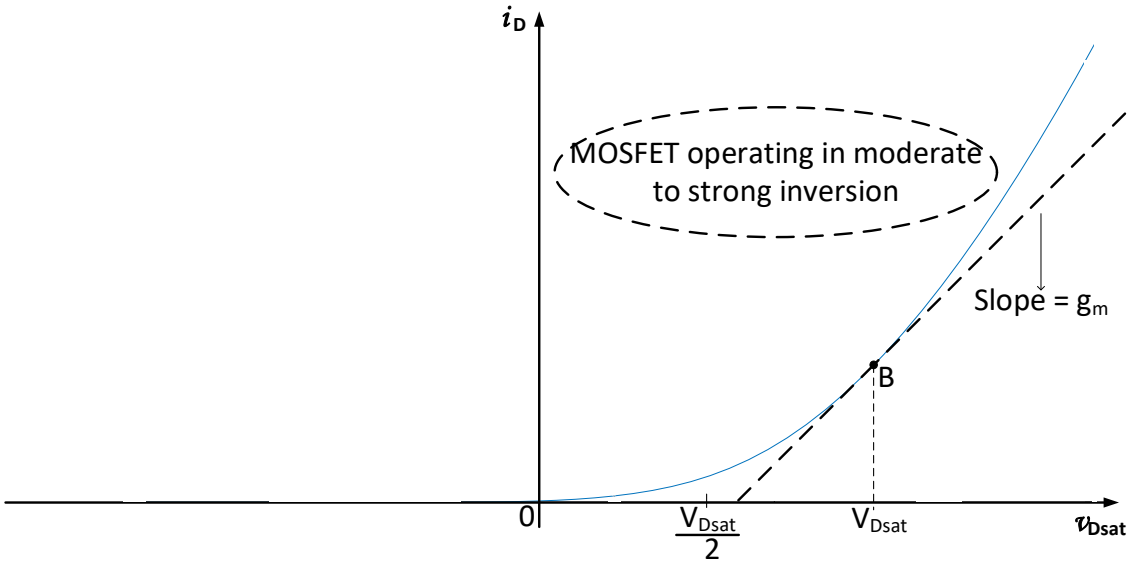

Figure 2.4: $i_D - v_{Dsat}$ curve of an NMOS transistor.

the input signal is said to be amplified, and the system can be classified as an amplifier. When the amplitude of the input signal is greater than that of the output signal, then the input signal is said to be attenuated and the system has a gain that is less than unity.

Usually, in RF electronic circuits, three different types of gain are considered: current gain (defined in Eq. (2.4), voltage gain (see Eq. (2.5)) and power gain (expressed by Eq. (2.6)).

$$A_i = \frac{i_{out}}{i_{in}} \tag{2.4}$$

$$A_v = \frac{v_{out}}{v_{in}} \tag{2.5}$$

$$A_P = \frac{P_{out}}{P_{in}} \tag{2.6}$$

The Gain is a feature of great importance in transceiver subcircuits responsible for compensating the losses and noise introduced by the channel. This is especially critical in the case of wireless systems, where air is the channel used and the amplitudes of received signals are very weak, usually in the microvolt range.

For clarity, the gain is usually expressed in dB. In these cases, the voltage and current gains expressed in dB, $A_{v,i}|_{dB}$, are defined as in Eq. (2.7) while the power gain in dB, $A_p|_{dB}$, is expressed in Eq. (2.8).

$$A_{v,i}|_{dB} = 20\log|A_{v,i}| \tag{2.7}$$

$$A_p|_{dB} = 20\log|A_p| \tag{2.8}$$

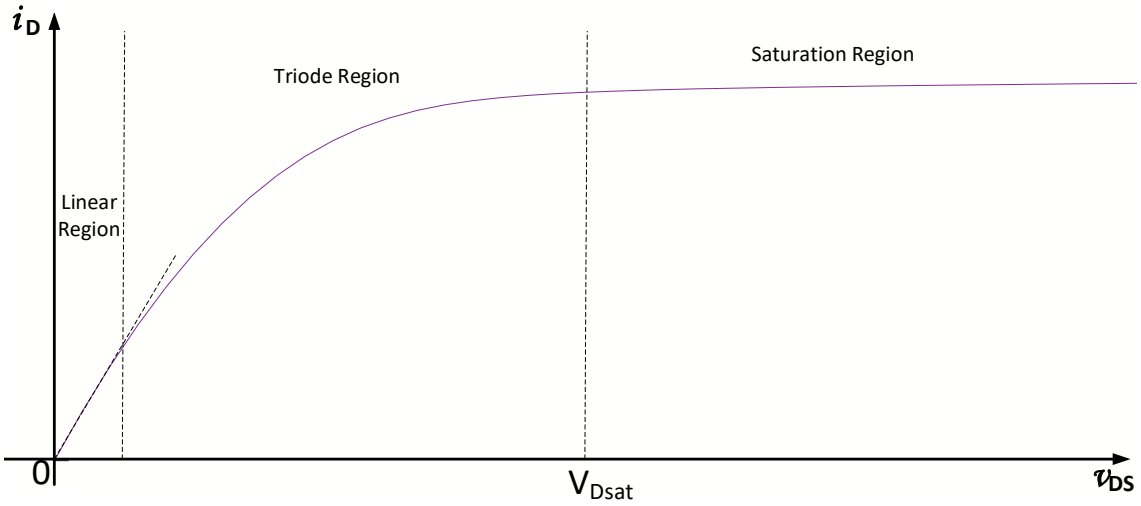

Figure 2.5: $i_D - v_{DS}$ curve of an NMOS transistor.

As soon as the inversion layer is created ($V_{GS} > V_{tn}$), the current in the channel, I_D, is able to flow with significant values. Under these conditions, the I_D value varies nonlinearly as a function of V_{DS}. Considering this, the quadratic model for MOSFET predicts a linear approximation by sections to the $i_D - v_{DS}$ characteristic as described in Fig. 2.5. The graph shown in this figure was obtained using the same transistor as in Fig. 2.3 and considering $V_{GS} > V_{tn}$.

By making these approximations, the model predicts three regions of operation of the NMOS transistor, dependent on the value of V_{DS}, such that in each operating region I_D is approximated by an equation:

1. For $V_{DS} \approx 0^+$, the NMOS transistor operates in the linear region, where the device exhibits a resistive behavior and the channel current assumes the expression given by Eq. (2.9).

$$I_D = \mu_n C_{ox} \frac{W}{L} V_{Dsat} V_{DS} \tag{2.9}$$

Where:

μ_n – mobility coefficient of n-type carriers (electrons);

C_{ox} – Gate-oxide capacitance per unit area. This is a technology-dependent parameter described by Eq. (2.10).

$$C_{ox} = \frac{K_{ox}\varepsilon_0}{t_{ox}} \tag{2.10}$$

Where:

K_{ox} – relative permittivity of SiO_2;

ε_0 – permittivity of free space;

t_{ox} – thickness of the thin oxide under the gate.

For simplicity, it is common to use the transconductance parameter, k_n, defined in Eq. (2.11).

$$k_n = \mu_n C_{ox} \tag{2.11}$$

2. When V_{DS} increases to values close to V_{Dsat}, $0^+ < V_{DS} < V_{Dsat}$, then I_D is described by Eq. (2.12) and the transistor is said to be operating in the triode region.

$$I_D = k_n \frac{W}{L} V_{Dsat} V_{DS} - \frac{(V_{DS})^2}{2} \tag{2.12}$$

3. With the increase in V_{DS} value, I_D increases until the channel becomes pinched off near the drain terminal. The pinch-off occurs at approximately $V_{DS} = V_{Dsat}$ [18].

   When $V_{DS} > V_{Dsat}$, the current I_D stops increasing due to the channel pinch-off and the NMOS transistor operates in the saturation region. In this operating zone, also known as active region, I_D is approximated by Eq. (2.13).

$$I_D = \frac{k_n}{2} \frac{W}{L} (V_{Dsat})^2 \tag{2.13}$$

2.2.2 Channel-Length Modulation

Apparently, according to Eq. (2.13), I_D is independent of V_{DS}. This only remains true for a first-order approximation, since the largest source of error is due to the reduction of the channel length, L, with increasing V_{DS} values. The increase of V_{DS} to values larger than V_{Dsat} causes the depletion region around the drain junction to increase its width in a square root relationship with respect to V_{DS} [18]. This expansion in width of the drain depletion region results in the reduction of the effective channel length. Consequently, the decrease in effective channel length causes the drain current I_D to increase, resulting in a phenomenon known as channel-length modulation.

In order to take into account the channel-length modulation effect, and thus obtaining a more accurate approximation, I_D in the saturation zone must be defined as shown in Eq. (2.14).

$$I_D = \frac{k_n}{2} \frac{W}{L} (V_{Dsat})^2 (1 + \lambda V_{DS}) \tag{2.14}$$

Where λ is a device parameter, dependent on both the technology used to manufacture the transistor and the channel length, L, selected by the circuit designer. The value of λ is much larger for current submicron technologies than for older technologies [19].

2.2.3 Body Effect

The large signal equations described so far assume that the source terminal is at the same voltage as the body (the substrate or bulk in an NMOS device). Nonetheless, there are often situations where the source is at a different voltage than the body. In these situations, the value of I_D in the saturation zone is affected, since the potential difference between body and source influences the amount of charge in the channel and conduction through it.

The influence of the body potential on the channel is termed the body effect and is modeled as a slight increase in threshold voltage, V_{tn}. The body effect must be considered since it is often important in analog circuit design.

When considering the body effect, it is possible to show that the threshold voltage of an NMOS transistor becomes defined by Eq. (2.15) [18].

$$V_{tn} = V_{tn0} + \gamma\left(\sqrt{V_{SB} + \left|2\phi_F\right|} - \sqrt{\left|2\phi_F\right|}\right) \tag{2.15}$$

Where:

V_{tn0} – threshold voltage with zero V_{SB} (source-to-body voltage);
γ – body-effect constant, measured in $\sqrt{V}$ and defined in Eq. (2.16);
ϕ_F – Fermi potential of the body, as explained in Eq. (2.17).

$$\gamma = \frac{\sqrt{2qN_AK_S\varepsilon_0}}{C_{ox}} \tag{2.16}$$

Where:

q – electron charge;
N_A – number of acceptors;
K_s – relative permittivity of silicon;

$$\phi_F = \left(\frac{kT}{q}\right) \times \ln\left(\frac{N_A}{n_i}\right) \tag{2.17}$$

Where:

n_i – carrier concentration of intrinsic silicon;
k – Boltzmann's constant;
T – temperature in Kelvin.

2.2.4 NMOS-PMOS Duality

Once the large-signal behavior of an NMOS transistor is understood, it is possible to understand the large-signal operation of a PMOS device considering three essential differences:

1. PMOS use holes to conduct channel current, I_D. Holes have an electrical charge symmetrical to that of the electrons used in NMOS devices. In practical terms, this

means that, for a PMOS transistor, the positive current I_D is considered to flow from source to drain, in the opposite direction to that defined by the current in an NMOS device;

2. PMOS devices conduct with a negative gate-to-source voltage. In fact, this is done considering that V_{tp} is negative and reversing the direction of all the voltages contained in the equations applied to the large-signal behavior of NMOS transistors. Thus, the condition required for conduction on a PMOS device becomes $V_{GS} < V_{tp} \Leftrightarrow V_{SG} > \left|V_{tp}\right|$, where V_{tp} is now a negative quantity;

3. The holes used in PMOS devices are substantially slower than the electrons used in NMOS. This is described by the hole mobility constant, μ_p, which ranges from $0.25\mu_n$ to $0.5\mu_n$ [19].

2.3 MOSFET Small-Signal Modelling

2.3.1 Low-Frequency Small-Signal Model

Considering the changes to be made to convert the large signal equations of an NMOS transistor to those of a PMOS device, the same can be done with respect to the small-signal behavior of a transistor. In this regard, the most widely used low-frequency small-signal model for an NMOS transistor operating in the saturation region is depicted in Fig. 2.6.

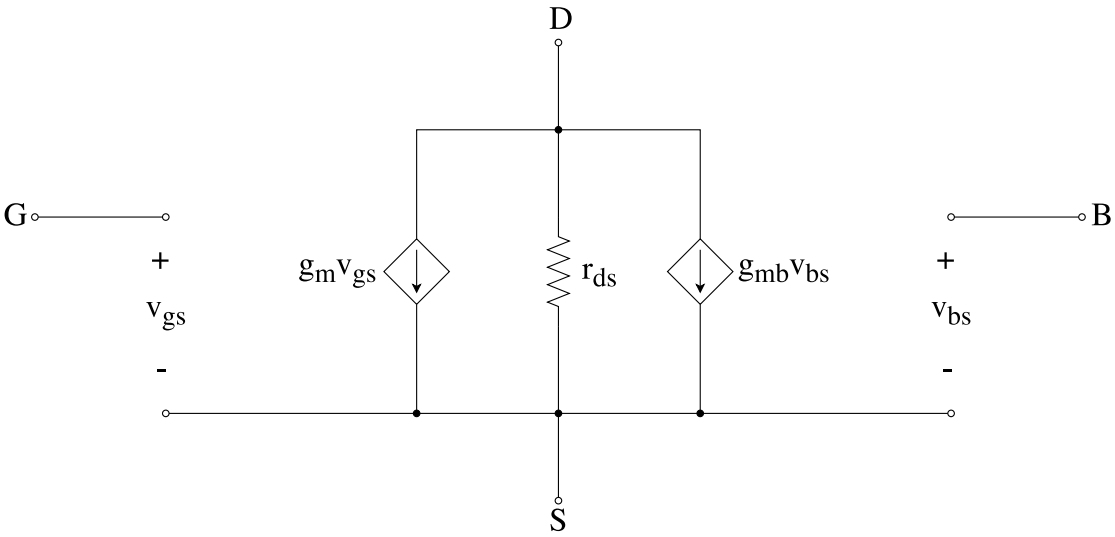

Figure 2.6: Low-frequency small-signal model for NMOS transistor (adapted from [19]).

The most important component of this model is the voltage-controlled current source, $g_m v_{gs}$. To model the implications of the body effect, there is another voltage-controlled current source, $g_{mb} v_{bs}$, where g_{mb} represents the body transconductance and is defined in Eq. (2.18).

$$g_{mb} = \frac{\partial i_D}{\partial v_{BS}} \tag{2.18}$$

Typically, g_{mb} has values in the range from $0.1 \times g_m$ to $0.3 \times g_m$ [19].

Through Eq. (2.14), it is known that there is a linear dependence of the drain current relative to V_{DS}. This dependence was modeled by a finite resistance between drain and source, rds, given by Eq. (2.19) [19].

$$r_{ds} = \frac{|V_A|}{I_D} \tag{2.19}$$

Where $V_A = 1/\lambda$.

2.3.2 High-Frequency Small-Signal Model

Due to the topology of the transistor, a MOSFET model closer to reality must take into account the parasitic capacitances between its terminals, namely: C_{gd}, C_{db}, C_{bs} and C_{gs}. These capacitances must be considered, especially when the device is subject to higher frequency signals. Thus, Fig. 2.7 represents the high-frequency small-signal model for an NMOS transistor.

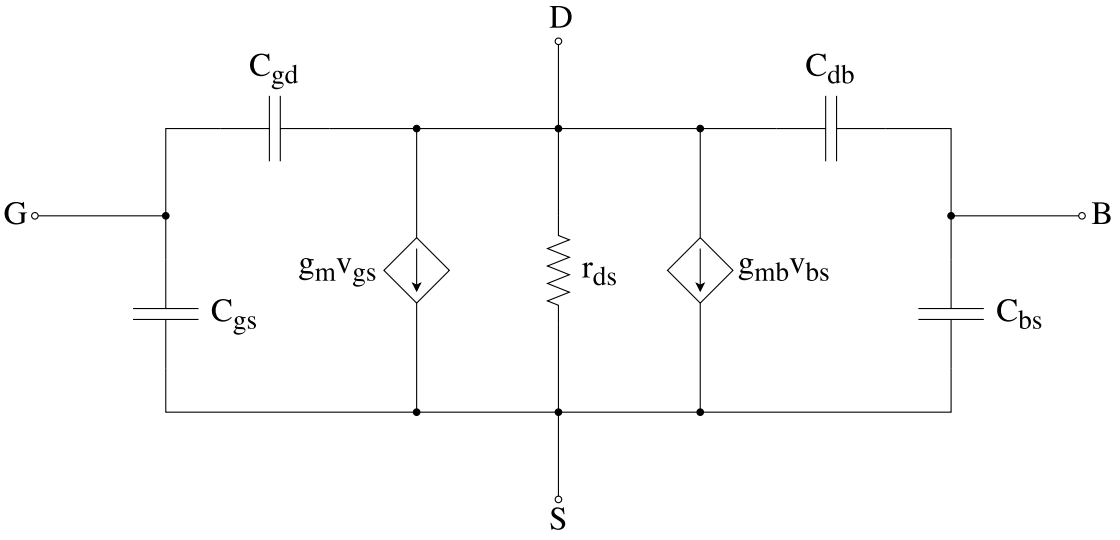

Figure 2.7: High-frequency small-signal model for an NMOS transistor.

Among the parasitic capacitances of this model, C_{gs} is the one with the highest value. It is possible to demonstrate that C_{gs} is given by Eq. (2.20) [18].

$$C_{gs} = \frac{2}{3} WLC_{ox} + WL_{ov}C_{ox} \tag{2.20}$$

Where L_{ov} is the effetive overlap distance and is usually empirically derived.

As for the C_{gd} capacitance, which is sometimes referred to as the Miller capacitance, its value is expressed by Eq. (2.21) and is important when there is a large voltage gain between gate and drain [18].

$$C_{gd} = WL_{ov}C_{ox} \tag{2.21}$$

The capacitances C_{db} and C_{bs} are defined by complex technology-dependent equations (see [18]). The precise definitions of these capacitances will not be part of the scope of this thesis.

2.4 Noise

Noise is a process that is present in all electronic circuits and has a random nature. This is because it represents external interferences to the circuit as well as physical phenomena related to the nature of the materials. Since noise is detrimental to circuit's performance, it is crucial to analyze and minimize its impact, which can be done through statistical models and methods created for this purpose [20].

2.4.1 Thermal Noise

One of the main sources of noise in CMOS circuits is thermal noise, which is the result of thermal excitation of the charge carriers present in a conductor. This type of noise occurs in all elements that, operating at a temperature above absolute zero, have a resistive behavior (including semiconductors).

The spectrum of this type of noise is white (flat) and is proportional to the absolute temperature [18].

The average thermal noise power generated in a resistor is defined by Eq. (2.22).

$$\overline{V_n^2} = 4kTR\Delta f \tag{2.22}$$

Where:

k – Boltzmann's constant;

T – absolute temperature in Kelvin;

Δf – system bandwidth, which is usually assumed to be $\Delta f = 1Hz$ so that the noise power is expressed per unit of bandwidth.

Thus, based on Eq. (2.22) thermal noise in a resistor can be modeled in two ways, as illustrated by Fig. 2.8.

Firstly, thermal noise in a resistor can be modeled by a Thevenin equivalent, comprising a voltage source with a Power Spectral Density (PSD) of $\overline{V_n^2}$ in series with a noiseless resistor (see Fig. 2.8(a)). On the other hand, the Norton equivalent, consisting of a current source with a PSD of $\overline{I_n^2}$ in parallel with the same noiseless resistor, may serve the same purpose (see Fig. 2.8(b)) [1].

(a) (b)

Figure 2.8: Models of a resistor thermal noise (adopted from [21]).

As discussed in the previous chapter, the linear dependence of the drain current of a MOSFET relative to V_{DS} indicates that there is a resistive component in the behavior of these devices, which is modeled by the r_{ds} resistor present in its small signal models. Therefore, due to the movement of carriers in the channel, MOS transistors also exhibit thermal noise which can be modeled by a MOSFET with a current source connected between its drain and its source [20], as depicted in Fig. 2.9.

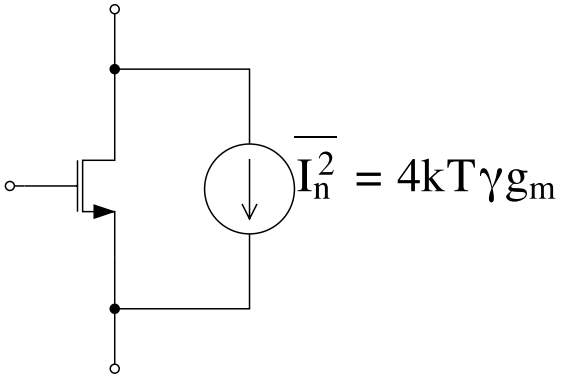

Figure 2.9: Thermal channel noise model for a MOSFET (adopted from [21]).

The average thermal noise current generated by a MOSFET is defined by Eq. (2.23).

$$\overline{I_n^2} = 4kT\gamma g_m \tag{2.23}$$

Where γ is called the excess noise factor. For long-channel transistors $\gamma = 2/3$, although this value is higher for short-channel devices [22].

If the MOSFET is operating in the deep triode region, then it acts as a resistor controlled by the gate-source voltage, V_{GS}. In this case, $V_{DS} \approx 0$, $\gamma = 1$ and the resistor that the transistor represents in this region has the value: $R_{on} \approx r_{ds} = 1/g_{ds}$. Thus, similarly to the case of resistors, the thermal noise current generated by a MOSFET operating in this region is given by Eq. (2.24).

$$\overline{I_n^2} = 4kTg_{d0} \tag{2.24}$$

Where g_{d0} is the drain-to-source conductance, g_{ds}, for $V_{DS} = 0$.

2.4.2 Flicker Noise

The other main source of noise in CMOS circuits is the flicker noise. This is a type of noise that is present in all active devices when a DC current is flowing and it originates from a phenomenon that occurs at the interface between the silicon substrate (Si) and the gate (SiO_2). With the movement of charge carriers at the Si-SiO_2 interface, the random phenomenon occurs, which leads to some of carriers being trapped and others being released, introducing a "flicker"noise into the drain current [20].

The flicker noise of a MOSFET is theoretically modeled as a voltage source in series with its gate, having a PSD as exposed by Eq. (2.25).

$$\overline{V_{nf}^2} \approx \frac{K_f}{C_{ox}WLf} \tag{2.25}$$

Where K_f is a process dependent constant, although it is independent of the biasing conditions.

From Eq. (2.25), it can be seen that this PSD is linearly dependent on $1/f$, and it is for this reason that flicker noise is also commonly called $1/f$ noise. Furthermore, this equation also shows that the flicker noise is inversely proportional to transistor's dimensions. Finally, it is important to note that the constant K_f has a lower value for p-channel devices, which results in PMOS transistors having lower flicker noise than NMOS devices.

Combining the two main sources of noise in CMOS circuits presented so far, it is possible to conclude that the power spectrum of noise in a MOSFET is illustrated by Fig. 2.10.

In Fig. 2.10 the $1/f$ corner is shown, which indicates that for frequencies higher than the corner frequency, f_c, the thermal noise becomes the most important contribution for this PSD.

To find the value of the corner frequency, f_c, it is first necessary to convert the flicker noise voltage into a current, as indicated by Fig. 2.8(b), replacing $R = (1/g_m)$. After this, the flicker noise current that resulted from this conversion is equated to the current given by Eq. (2.23), resulting in the expression shown in Eq. (2.26).

$$f_c = \frac{K_f}{WLC_{ox}} \frac{g_m}{4KT\gamma} \tag{2.26}$$

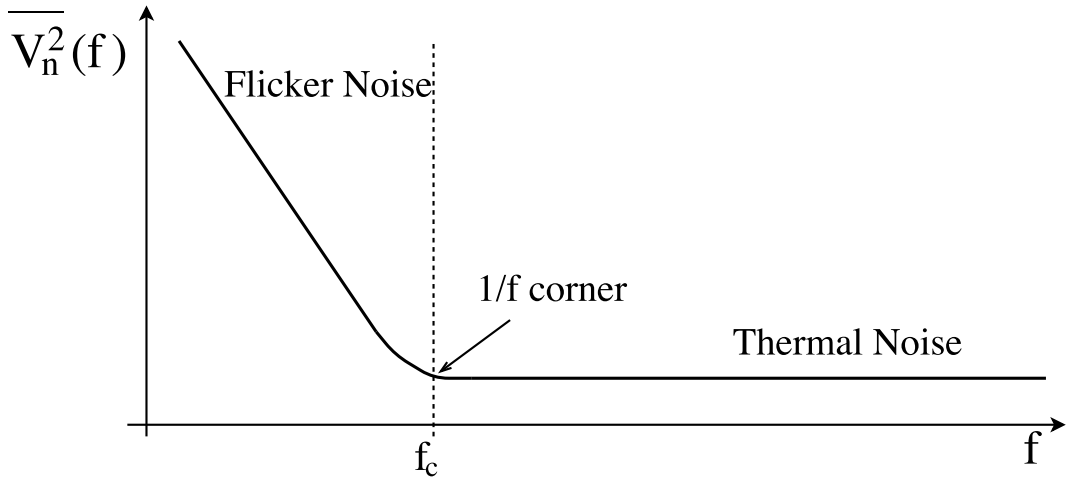

Figure 2.10: Power spectrum of noise in a MOSFET (adapted from [21]).

2.4.3 Noise Figure

The noise factor is the most widely used measure to determine the noise generated by a circuit and, to understand it, the system must be interpreted as a two-port network as shown in Fig. 2.11.

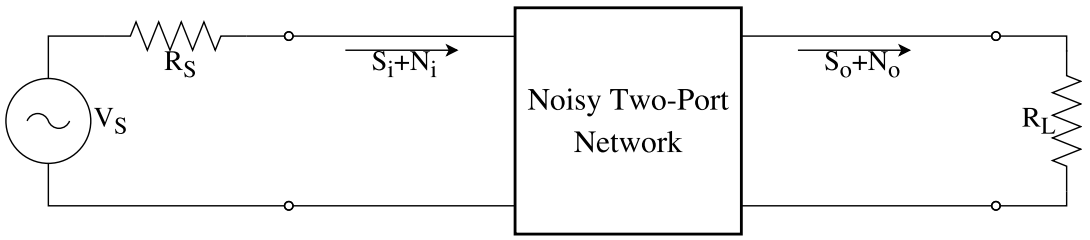

Figure 2.11: Noisy two-port network representation (adopted from [21]).

The noise factor, F, is defined by the ratio depicted in Eq. (2.27).

$$F = \frac{N_o}{N_i G_A} \tag{2.27}$$

Where:

N_o – available power noise at the circuit's output;

N_i – available power noise at the circuit's input, wich is defined as the noise power resulting from a matched resistor at $T_o = 290K$ [23];

G_A – available power gain of the circuit.

If the output and input ports are adapted then the power gain of the system is given by Eq. (2.28).

$$G_A = \frac{S_o}{S_i} \tag{2.28}$$

By making this substitution in Eq. (2.27), it is possible to conclude that F measures the degradation of the two-port network's Signal-to-Noise Ratio (SNR), as demonstrated in Eq. (2.29).

$$F = \frac{S_i/N_i}{S_o/N_o} = \frac{SNR_i}{SNR_o} \tag{2.29}$$

It is common for the noise factor to be expressed in dB and when this happens it acquires the name of Noise Figure (NF), defined by Eq. (2.30).

$$NF = 10\log\frac{SNR_i}{SNR_o} \tag{2.30}$$

In an ideal case, where the network would be noiseless, then the noise factor would have the value $F = 1$, resulting in a noise figure of $NF = 0$dB.

2.5 Receiver Architectures

Within the different approaches that exist to implement receivers, there are three main architectures that will be addressed in this section: heterodyne, homodyne and low-IF.

2.5.1 Heterodyne Receiver

The heterodyne receiver, which consists of a two-step down-conversion of the received signal, is shown in Fig. 2.12.

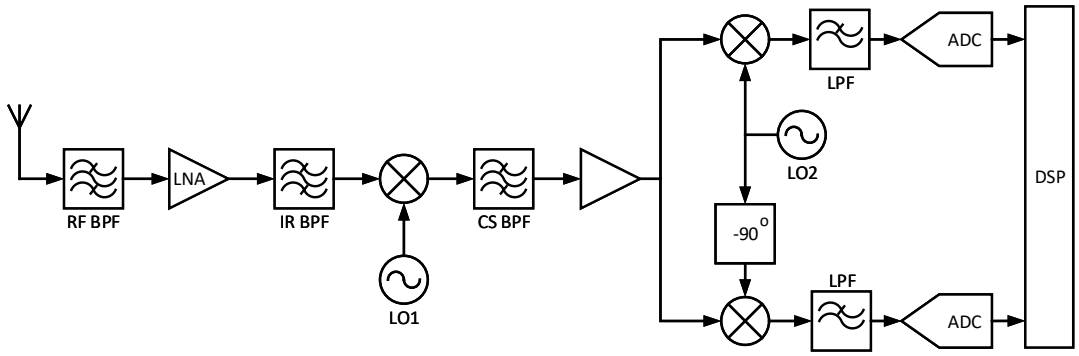

Figure 2.12: Heterodyne receiver architecture (adapted from [2]).

This is a widely adopted architecture in wireless communication receivers, also known as the Intermediate Frequency (IF) receiver.

From the information captured by the antenna, the Band-Pass Filter (BPF) selects the frequency band that contains the signal of interest. After this signal is amplified by the LNA, it will be filtered by the Image Rejection Band-Pass Filter (IR BPF), whose function is to eliminate the image that can be generated in the down-conversion process. The need for this filter arises from the fact that two different input frequencies can generate the same IF (see Fig. 2.13).

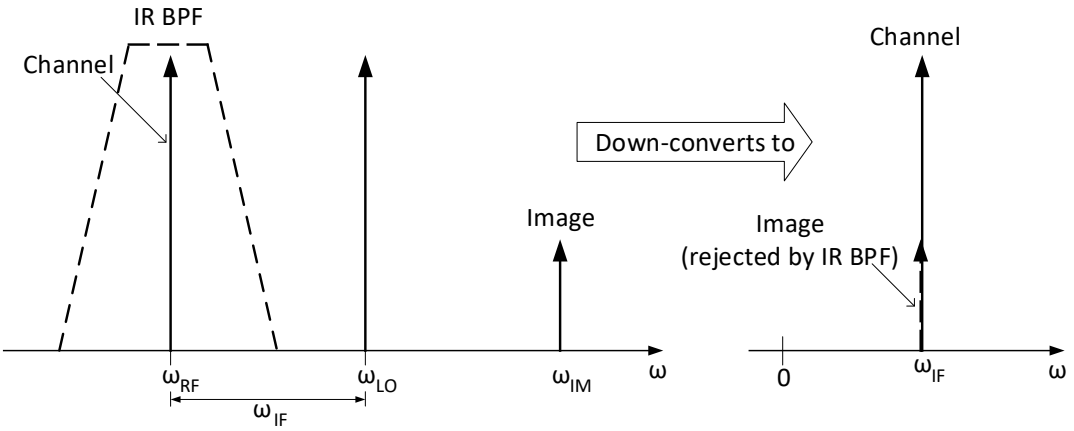

Figure 2.13: Image rejection in heterodyne receivers (adapted from [2]).

The down-conversion process, performed by the Mixer, is possible thanks to an inherent property of multiplying two sinusoidal signals, also known as mixing. Thanks to this property, the output signal of the mixer, $v_{IF}(t)$, results from the multiplication of the two pure sinusoidal waves at its input, $v_{LO}(t)$ and $v_{RF}(t)$. This mathematical relation is given by Eq. (2.31).

$$v_{IF}(t) = v_{RF}(t) \cdot v_{LO}(t) = \frac{1}{2} V_{RF} V_{LO} [\cos(\omega_{RF} t - \omega_{LO} t) + \cos(\omega_{RF} t + \omega_{LO} t)] \tag{2.31}$$

Where:

$v_{RF}(t) = V_{RF} \cos(\omega_{RF} t)$ is the receiver's input signal;

$v_{LO}(t) = V_{LO} \cos(\omega_{LO} t)$ is the sine wave produced by the LO;

And $\omega_{IF} = \omega_{RF} - \omega_{LO}$.

Through Eq. (2.31) it is possible to clarify the importance of the IR BPF eliminating a signal $v_{IM} = V_{IM} \cos(\omega_{IM} t)$ before it reaches the input of the mixer. This is because, if $\omega_{IM} = 2\omega_{LO} - \omega_{RF}$ then the mixing between v_{IM} and v_{LO} will generate two signals at the frequencies $\omega_1 = \omega_{LO} - \omega_{RF}$ and $\omega_2 = 3\omega_{LO} - \omega_{RF}$. Meaning that $|\omega_1| = |\omega_{IF}|$. Thus, if the IR BPF was not present in this architecture, the signal with frequency ω_1 would deteriorate to the signal of interest by overlapping the frequency ω_{IF}.

The choice of IF is an important point to consider in the design of this architecture, since there is a trade-off between a high IF that facilitates the design of the IR BPF and a low IF that facilitates the suppression of interferers [2]. It is also important to note that the filters mentioned here require a high quality factor, only possible to achieve with reactive components, making it difficult to implement this architecture as a good solution for applications where low-cost and low-area are the main priorities.

Subsequent to the first mixing procedure, the Channel Select Band-Pass Filter (CS BPF) eliminates the interferers that are down-converted along with the signal of interest, which is then amplified. After this amplification, the information is again down-converted generating an In-Phase and Quadrature (I/Q) signal at a baseband frequency, which is

then cleared of interferers by the Low-Pass Filter (LPF). Finally, the signal is converted to the digital domain by the ADC so that it can proceed to Digital Signal Processing (DSP). Therefore, a key advantage of this architecture is the compatibility it has with modern modulation schemes that require I/Q signals for full recovery of the information.

2.5.2 Homodyne Receiver

In the homodyne receiver architecture, after the RF signal is picked up by the antenna, filtered by the RF BPF and amplified by the LNA, there is a single down-conversion from the RF frequency to the baseband. This is achieved by using a LO to generate a signal with the same frequency as the RF input. Therefore, this topology is also called the direct-conversion or zero-IF receiver and is illustrated in Fig. 2.14.

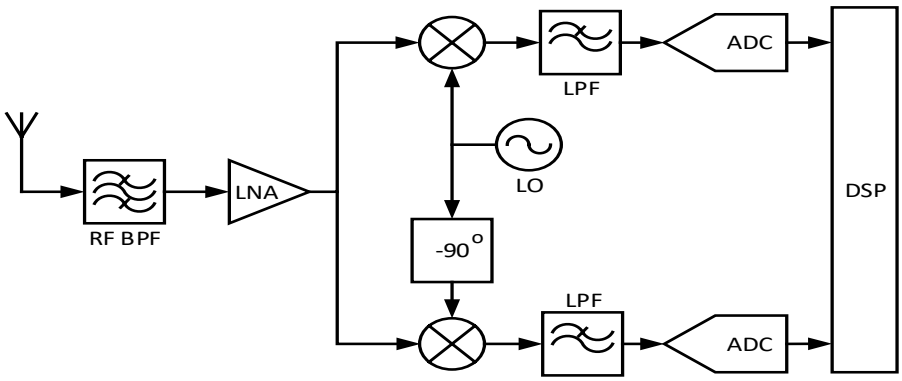

Figure 2.14: Homodyne receiver architecture (adapted from [2]).

The fact that only one LPF is required to make a correct channel selection and that there is no external IR BPF leads to quality factor requirements for these filters that are less demanding. In addition, these characteristics allow the receiver full integration, making this architecture a solution for obtaining low-cost, low-area and low-power receivers. However, as will be evidenced by the disadvantages briefly presented below, this topology is a less appropriate solution than the heterodyne receiver in applications whose demands are more stringent [2].

Firstly, it is important to note that this circuit is more vulnerable to flicker noise, since this type of noise can corrupt the baseband signals used in this receiver.

Another drawback of this circuit relates to mismatches between the I/Q mixers and errors in the 90° phase shift circuit. This leads to imbalances in the gain and phase outputs of the I/Q mixers, which can corrupt the signal constellation used in modern modulation schemes such as Quadrature Amplitude Modulation (QAM). To overcome this problem it is necessary to implement high frequency blocks with very high precision, which is a difficult task.

It is also important to note the problem that arises if two interferers, with frequencies ω_1 and ω_2 such that $\omega_2 - \omega_1 \approx 0$, are close to the channel of interest. In this case, the

mixing of these interferers results in a second-order term that will be down-converted to near the baseband, distorting the signal.

Another problem that can occur in this receiver is the coupling of the LO signal to the antenna that will eventually radiate this information, a phenomenon known as LO leakage. This is due to the capacitances and resistances between the LO and RF ports of the mixer and the LNA ports. This means that this problem has the potential to interfere with other receivers using the same wireless standard unless a differential LO is used and the mixer outputs cancel common mode components [2].

As a consequence of LO leakage, a phenomenon known as LO self-mixing occurs. In this process a DC component is generated at the mixer's output, which can saturate baseband circuits and prevent signal detection [2]. Therefore, in order to overcome this limitation, the homodyne receiver requires DC offset removal techniques.

Finally, it should be noted that, in order to create the necessary conditions for converting the baseband signal of interest to the digital domain, the LPF must be highly linear and have low noise contributions. These requirements, which enable the LPF to suppress out-of-channel interferers, are difficult to implement.

2.5.3 Low-IF Receiver

The low-IF receiver has a design approach that blends the characteristics of the two receiver topologies previously mentioned, in order to combine the advantages of each of them in a single architecture. On the one hand, the low-IF receiver has the high performance and flexibility that are typical in the heterodyne architecture, on the other hand it can be fully integrated as the homodyne receiver.

Like the heterodyne architecture, the low-IF receiver also avoids the problems related to direct conversion mentioned in the previous subsection by using an intermediate frequency, which in this case has a low value. However, the use of an IF implies that the low-IF receiver will also have to deal with the image problem described by Fig. 2.13. To overcome this limitation while avoiding the use of a high quality factor IR BPF, the low-IF receiver requires special techniques to cancel the image frequency. To accomplish this purpose, there are two main image rejection architectures, one proposed by Hartley and the other suggested by Weaver.

The Hartley architecture is illustrated in Fig. 2.15, consisting of a solution that begins by mixing the I/Q outputs of the LO with the RF signal. Thereafter, the resulting signal is filtered by the LPF and one of the I/Q outputs is then shifted 90° and added to the other output signal. This last operation results in an IF signal with no image frequency.

The reason why the output of this architecture has no image frequency is explained mathematically. First, assume that the RF input signal with an associated image frequency is described by Eq. (2.32).

$$x_{RF}(t) = V_{RF}\cos(\omega_{RF}t) + V_{IM}\cos(\omega_{IM}t) \tag{2.32}$$

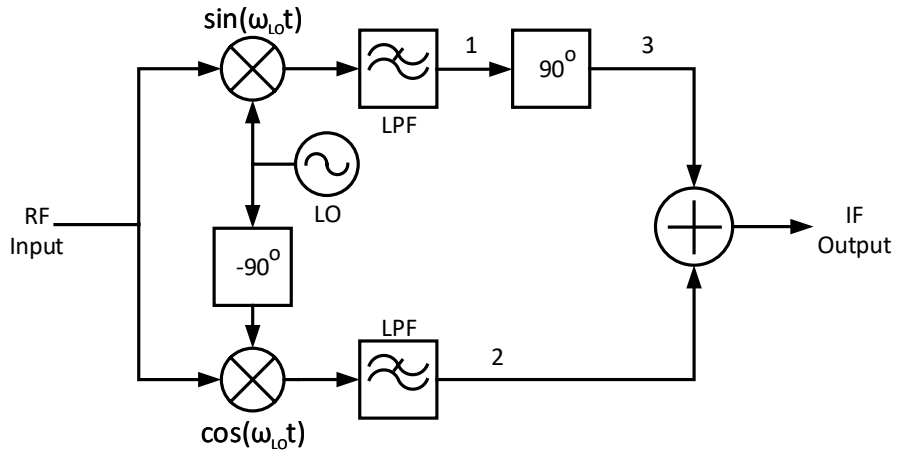

Figure 2.15: Hartley image rejection architecture for Low-IF Receiver (adopted from [2]).

Thus, at point 1 of Fig. 2.15, there is the signal $x_1(t)$, described by Eq. (2.33), and at point 2 the signal is defined by Eq. (2.34)

$$x_1(t) = -\frac{V_{RF}}{2}\sin\left[(\omega_{RF} - \omega_{LO})\,t\right] + \frac{V_{IM}}{2}\sin\left[(\omega_{LO} - \omega_{IM})\,t\right] \tag{2.33}$$

$$x_2(t) = \frac{V_{RF}}{2}\cos\left[(\omega_{LO} - \omega_{RF})\,t\right] + \frac{V_{IM}}{2}\cos\left[(\omega_{LO} - \omega_{IM})\,t\right] \tag{2.34}$$

At point 3, the signal expressed in Eq. (2.33) is shifted by 90°, which is equivalent to a substitution of $[\sin(\alpha)]$ for $[-\cos(\alpha)]$, resulting in the signal given by Eq. (2.35).

$$x_3(t) = \frac{V_{RF}}{2}\cos\left[(\omega_{RF} - \omega_{LO})\,t\right] - \frac{V_{IM}}{2}\cos\left[(\omega_{LO} - \omega_{IM})\,t\right] \tag{2.35}$$

The result of the sum between $x_1(t)$ and $x_3(t)$ is an IF output with no image frequency component, defined by Eq. (2.36).

$$x_{IF}(t) = V_{RF}\cos\left[(\omega_{RF} - \omega_{LO})\,t\right] \tag{2.36}$$

This circuit has two major limitations that can lead to incomplete image cancellation: high sensitivity to LO quadrature errors and mismatches between the two I/Q signal paths.

The image rejection architecture proposed by Weaver, shown in Fig. 2.16.

The main difference between this circuit and the Hartley architecture is that the 90° phase shift is replaced by a second mixing operation that is applied to the I/Q signals. The introduction of the new down-conversion to a lower frequency than the first IF leads to the elimination of an image frequency that may arise in the first mixing process, having the same effect as the 90° phase shift of the Hartley architecture. Despite this, the circuit remains vulnerable to images that may arise in the second mixing process, in case the signal of interest is not down-converted to the baseband. In addition, the Weaver architecture has the same limitations as the Hartley topology.

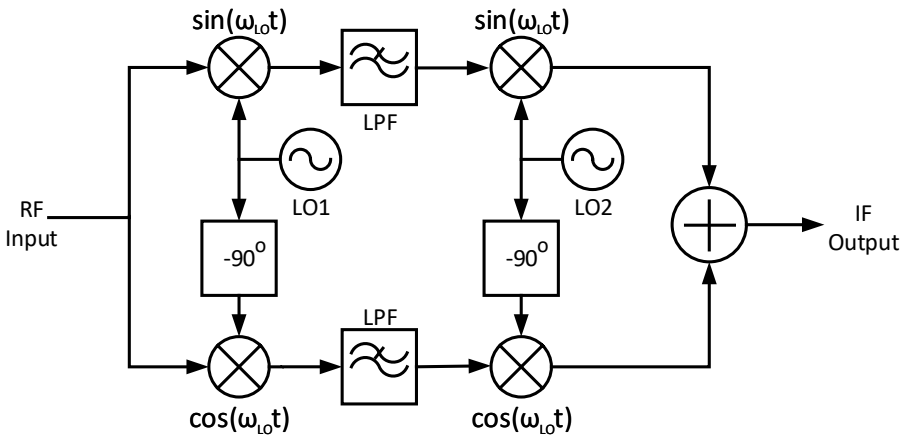

Figure 2.16: Weaver image rejection architecture for Low-IF Receiver (adopted from [2]).

Chapter 3

CMOS Oscillators

An oscillator is a circuit whose main feature is to generate a periodic waveform from a DC source. According to its output, if an oscillator produces a sine wave it can be classified as harmonic or quasi-linear. In case the circuit generates a different waveform, it can be categorized as a strongly non-linear oscillator.

As for its application, oscillators are used in RF transceivers to perform frequency translation operations, and are also useful in the modulation process, providing a clock signal for digital circuit synchronization. Therefore, because of their wide use, oscillators are vital elements for any wireless communication circuit.

This chapter begins by presenting fundamental concepts about the operation of an oscillator circuit, as well as some parameters that measure its performance. Subsequently, the main CMOS implementations of harmonic and non-linear oscillators are concisely explained. Finally, a reference is made to the state-of-the-art oscillators of the different topologies discussed in this chapter.

3.1 Basic Concepts

3.1.1 Positive Feedback Loop

As previously mentioned, a sinusoidal oscillator is intended to generate a sinusoid with a fixed frequency, f_0, initial phase, θ_0, and amplitude, V_0, in its output, v_{out}. Thus, Eq. (3.1) defines the output voltage, v_{out}.

$$v_{out}(t) = V_0 cos(\omega_0 t + \theta_0) \text{ , where } \omega_0 = 2\pi f_0 \tag{3.1}$$

Sinusoidal oscillators can be modeled as positive feedback systems consisting of an amplifier block, with transfer function given by $H(s)$, and a frequency selective network,

$\beta(s)$. This is depicted in Fig. 3.1, where $V_{in}(s)$ is the input signal originated from a DC source, V_f is the feedback signal and $s = j\omega$.

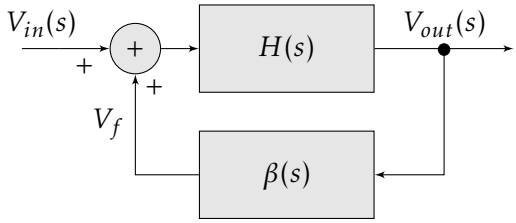

Figure 3.1: Positive feedback loop modeling a sinusoidal oscillator.

Thus, the transfer function of a sinusoidal oscillator is expressed by Eq. (3.2) and its loop gain, $L(s)$, is given by Eq. (3.3).

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{H(s)}{1 - H(s)\beta(s)} \tag{3.2}$$

$$L(s) = H(s)\beta(s) \tag{3.3}$$

3.1.2 Barkhausen Criterion

As mentioned in [24], the "Barkhausen conditions", usually known as Barkhausen criterion, are the necessary conditions for an oscillator to maintain steady-state oscillation. These conditions apply to the loop gain, $L(s)$, and are described by Eq. (3.4), known as the gain condition, and by Eq. (3.5), which is the phase condition.

$$|L(s)| = 1 \tag{3.4}$$

$$arg\,[L(s)] = 2k\pi \ , k \in \mathbb{Z} \tag{3.5}$$

Since the above conditions only refer to a steady state, it is important to consider a condition that guarantees an autonomous startup of the oscillator, triggered by its internal noise. Thus, for the circuit to start oscillating it is necessary to meet the requirements of the "start-up condition" [24], defined in Eq. (3.6).

$$|L(s)| > 1 \tag{3.6}$$

3.1.3 Phase Noise

Ideally, in the frequency domain, a sinusoidal oscillator should generate a dirac centered on its oscillation frequency, ω_o. This implies that all the output signal power is concentrated only at the frequency ω_o. However, real oscillators suffer from frequency instabilities, referred to as phase noise. Considering the output spectrum, this translates

into the appearance of sidebands around ω_o and its harmonics, as depicted in Fig. 3.2. These sidebands decrease with increasing offset frequency from ω_o or its harmonics, as white noise becomes dominant at a certain offset frequency [24].

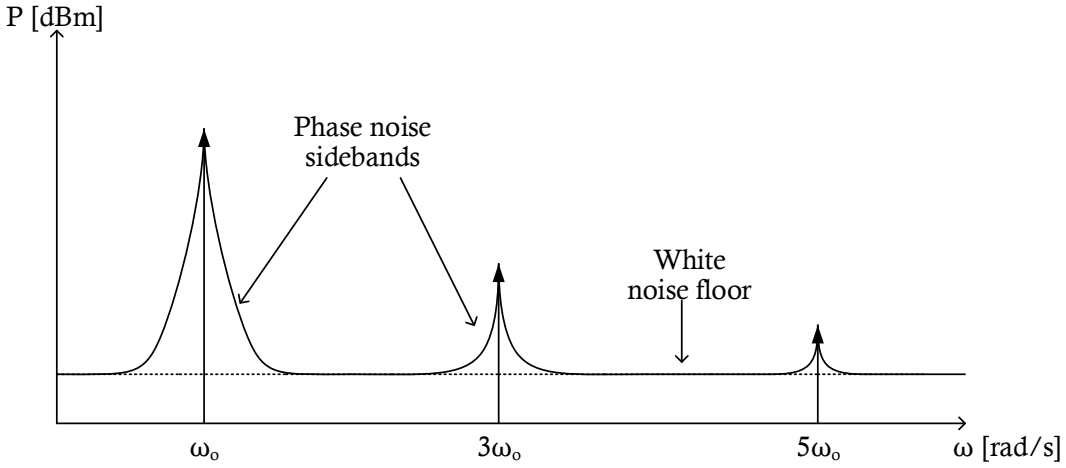

Figure 3.2: Real oscillator spectrum (fundamental and two harmonics) with phase noise (adapted from [24]).

The frequency instabilities of an oscillator are usually characterized by the Single-Sideband (SSB) phase noise to carrier ratio, $\mathcal{L}$, expressed in decibels below the carrier per hertz (dBc/Hz) and defined in dB by Eq. (3.7).

$$\mathcal{L}(\Delta\omega) = 10\log\left(\frac{P(\Delta\omega)}{P(\omega_o)}\right) \tag{3.7}$$

Where $P(\omega_o)$ is the carrier power and $P(\Delta\omega)$ is the SSB noise power at an offset value, $\Delta\omega$, from the carrier frequency, considering a 1Hz bandwidth. This concept is clarified by Fig. 3.3, where $f_o = \omega_o/(2\pi)$ and $\Delta f = (\Delta\omega)/(2\pi)$.

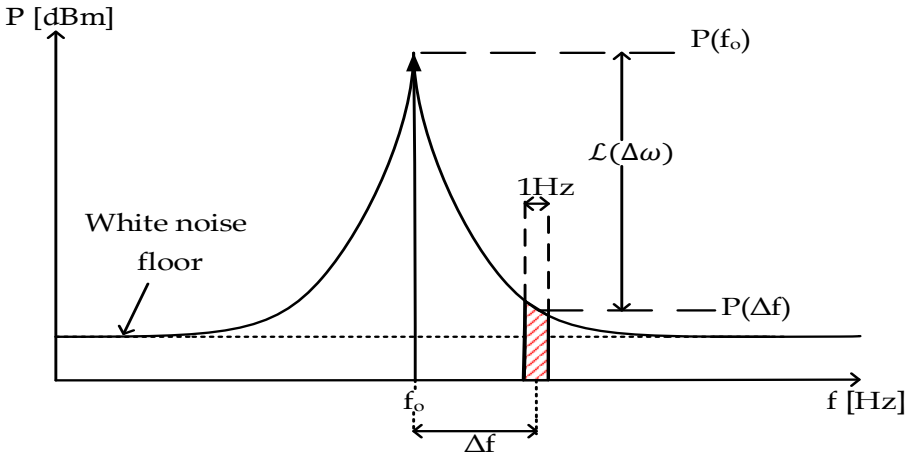

Figure 3.3: Phase noise to carrier ratio, $\mathcal{L}(\Delta\omega)$, definition.

Although, in Eq. (3.7), $P(\Delta\omega)$ refers to sideband noise regardless of its source, it should be noted that practical oscillators have amplitude stabilization mechanisms which lead to a strong reduction of amplitude noise without affecting phase noise [25]. Thus, in the above equation phase noise is the dominant factor and therefore, in literature, $\mathcal{L}(\Delta\omega)$ is simply referred to as "phase noise".

Alternatively, it's possible to characterize phase noise using the Carrier to Noise Ratio (CNR) which, in dB, simply has the symmetric value of $\mathcal{L}(\Delta\omega)$ as defined in Eq. (3.8).

$$CNR(\Delta\omega) = -\mathcal{L}(\Delta\omega) \tag{3.8}$$

In the time domain, phase noise is referred to as jitter. In digital applications, which require oscillators to produce square waves, jitter is a major concern since it causes the exact moment of a zero-crossing of the square wave to be stochastic [24].

Considering the carrier's SSB PSD, through an asymptotic analysis it is possible to divide the phase noise into three regions [25], as shown in Fig. 3.4.

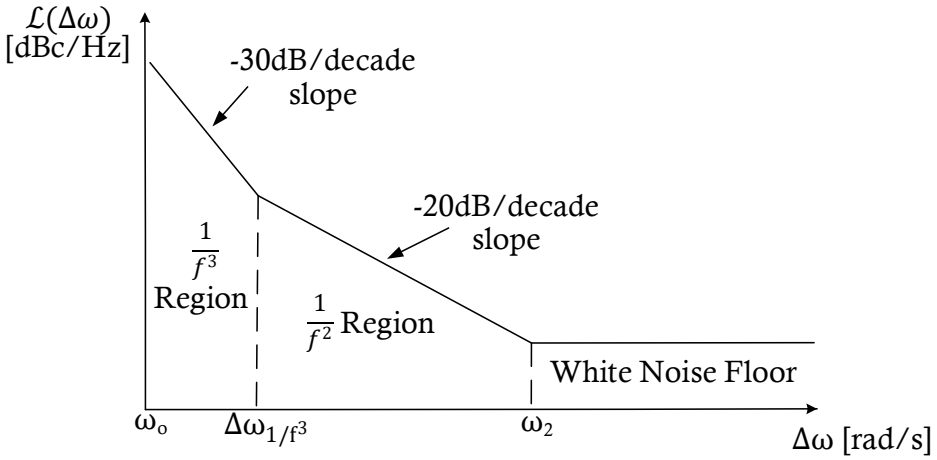

Figure 3.4: Asymptotic SSB phase noise (adapted from [2]).

The $\frac{1}{f^3}$ region, with frequency bandwidth between ω_o and ω_{1/f^3}, has a -30 dB/decade slope due to flicker noise of the oscillator's active devices.

There is also the $\frac{1}{f^2}$ region, where $\Delta\omega$ is between the frequencies ω_{1/f^3} and ω_2, presenting a slope of -20dB/decade. This is due to the white noise inside the oscillator, which causes a frequency modulation of the output signal.

Finally, the white noise floor, for offset frequencies above ω_2, represents the white noise introduced by neighboring circuits connected to the oscillator.

Using the asymptotic approximation illustrated in Fig. 3.4, it is possible to understand the most used phase noise model in the scientific community: Leeson-Cutler's semi-empirical equation, proposed in [26–28]. Thus, as described in [29], Eq. (3.9) defines a predictive model of $\mathcal{L}(\Delta\omega)$.

$$\mathcal{L}(\Delta\omega) = 10\log\left[\frac{2FkT}{P_S}\left(1+\left(\frac{\omega_o}{2Q\Delta\omega}\right)^2\right)\left(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right] \tag{3.9}$$

Where:

F – Empirical fitting parameter, called excess noise factor [25];

k – Boltzmann constant;

T – Absolute temperature;

P_S – Power of the carrier signal;

ω_o – Oscillation frequency;

Q – Oscillator's quality factor. Will be addressed in the next section;

$\Delta\omega$ – Frequency offset from the carrier;

$\Delta\omega_{1/f^3}$ – Corner frequency between $\frac{1}{f^3}$ and $\frac{1}{f^2}$ regions of the SSB phase noise spectrum (represented in Fig. 3.4).

3.1.4 Quality Factor

Ideally, an oscillator would be a circuit capable of maintaining the steady state using only ideal reactive elements. The operation of an ideal oscillator is illustrated in Fig. 3.5, where I_0 is an impulse applied to the circuit and V_{out} is the oscillator output, with an amplitude given by the strength of the initial impulse.

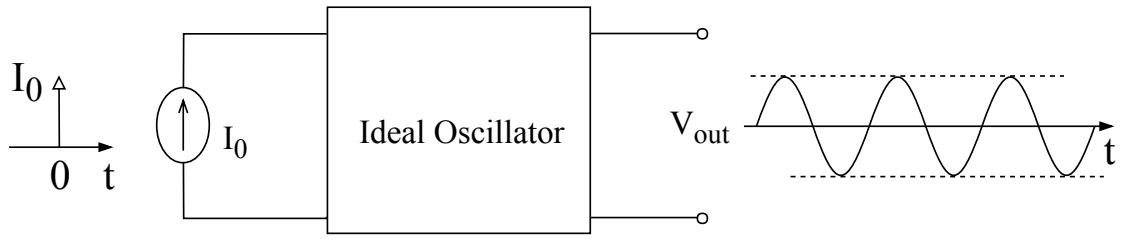

Figure 3.5: Ideal oscillator operation (adapted from [1]).

In fact, oscillator circuits have losses, which can be modeled by a resistor in parallel with an ideal oscillator, as shown in Fig. 3.6. The presence of the parallel resistor, R_P, in the circuit has the physical meaning of damping the amplitude of the output signal, V_{out}, preventing the circuit from reaching steady-state oscillations (see Fig. 3.6(a)).

To compensate for the losses represented by R_P, thus recreating the ideal scenario illustrated in Fig. 3.5, it is necessary to introduce an active circuit with an input resistance of $-R_P$, as indicated in Fig. 3.6(b). In this figure, it is assumed that the initial impulse is represented by the internal noise of the circuit.

Analyzing from another perspective, the circuit of Fig. 3.5 represents a device that perfectly stores the initial impulse energy. This being a circuit that is capable of maintaining, on its own, an output signal of constant amplitude over time.

On the other hand, the energy consumption required for real oscillators, modeled by Fig. 3.6(b), to maintain the steady state can be measured indirectly by its quality

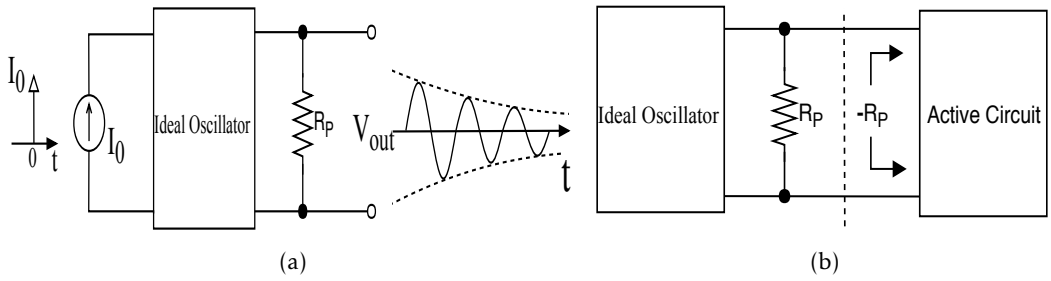

Figure 3.6: High-level models for real oscillators: (a) Lossy oscillator operation (adapted from [1]), (b) Loss cancellation by an active circuit (adapted from [1]).

factor (Q). Essentially, the quality factor is an indicator of "how close to ideal an energy-storing device is" [1].

As shown in Fig. 3.7, there is an inverse proportionality relationship between the quality factor of an oscillator and its bandwidth, centered on ω_o, which concentrates most of the output signal power. This indicates that there is a close relationship between Q and phase noise.

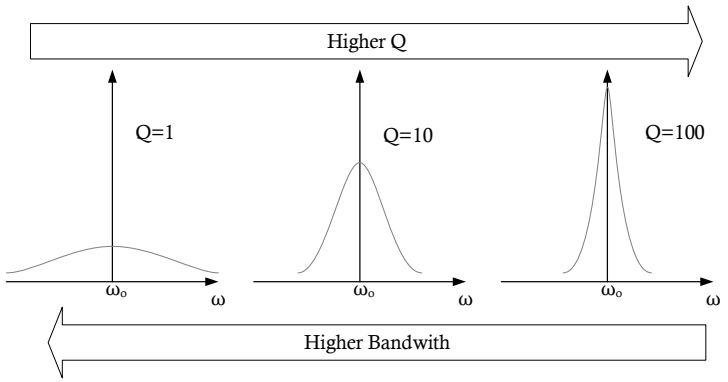

Figure 3.7: Variation of the carrier spectrum depending on the value of the quality factor.

Considering second-order systems, there are three possible definitions for Q:

1. The first definition takes into account a resonant circuit with oscillation frequency, ω_o, and whose bandwidth, B, is measured at -3dB of the output signal [27]. Considering this, Q can be expressed by Eq. (3.10).

$$Q = \frac{\omega_o}{B} \tag{3.10}$$

The concept of Q defined in the previous equation is summarized by Fig. 3.8.

This definition of Q is best suited for filters and oscillators characterized by second order resonant circuits [2].

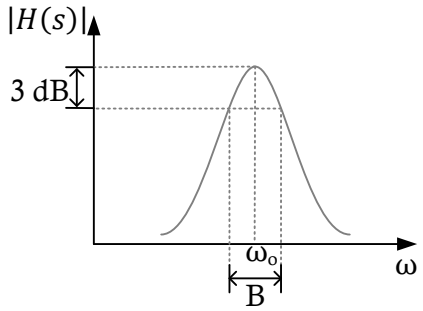

Figure 3.8: Definition of Q of a second-order system according to its bandwidth (adapted from [2]).

2. The second definition of Q quantifies the ability of a generic circuit to retain stored energy per oscillation cycle [30]. This is expressed by Eq. (3.11), which presents a ratio between the maximum energy stored per period of oscillation and the energy dissipated in that period, through resistive devices.

$$Q = 2\pi \frac{\text{Maximum energy stored in a period}}{\text{Energy dissipated in a period}} \tag{3.11}$$

Typically this definition is applied to RLC circuits where the energy can either be stored by a capacitor, C, or by an inductor, L, and the energy is dissipated by the resistor, R. The following is a practical example.

Considering the inductor as the energy storing element, then its stored energy, W_L, per oscillation period, T_o, is expressed in Eq. (3.12).

$$W_L = \int_0^T i(t) L \frac{di(t)}{dt} dt = L I_{rms}^2 \tag{3.12}$$

Where I_{rms} is the root-mean-square current in the inductor.

Considering that the resistive loss in the inductor is modeled by a series resistance, R_S, then the energy dissipated per period by this resistor, W_R, is defined by Eq. (3.13).

$$W_R = R_S I_{rms}^2 T_o \tag{3.13}$$

Thus, the value of Q becomes that expressed by Eq. (3.14).

$$Q = 2\pi \frac{L I_{rms}^2}{R_S I_{rms}^2 T_o} = 2\pi f_o \frac{L}{R_S} = \frac{\omega_o L}{R_S} \tag{3.14}$$

On the other hand, if the capacitor is considered as the energy storing element, then its stored energy, W_C, per oscillation period is defined by Eq. (3.15).

$$W_C = \int_0^T v(t) C \frac{dv(t)}{dt} dt = C V_{rms}^2 \tag{3.15}$$

Where $V_{rms} = \frac{I_{rms}}{\omega_o C}$ is the root-mean-square voltage in the capacitor and I_{rms} is the root-mean-square current across the capacitor.

Considering that the losses in the capacitor are modeled by a series resistor, then W_R definition remains the same as defined by Eq. (3.13). Therefore, in this case, the value of Q is that given by Eq. (3.16).

$$Q = 2\pi \frac{C V_{rms}^2}{R_S I_{rms}^2 T_o} = 2\pi f_o \frac{\frac{C I_{rms}^2}{(\omega_o C)^2}}{R_S I_{rms}^2} = \frac{1}{\omega_o C R_S} \tag{3.16}$$

3. Finally, this third definition of Q, called open-loop Q and proposed in [31], considers the oscillator as a feedback system. In this definition, presented in Eq. (3.17), the amplitude, A, and phase, θ, of the open-loop transfer function, $H(s)$, are considered.

$$Q = \frac{\omega_o}{2} \sqrt{\left(\frac{dA}{d\omega}\right)^2 + \left(\frac{d\theta}{d\omega}\right)^2} \tag{3.17}$$

This definition is often considered to calculate the quality factor of a two-integrator oscillator [2].

3.1.5 Tuning Range

In various applications it is desirable for the oscillator to operate in a range of oscillation frequencies. In such cases, it is possible to change the operating frequency by varying an electrical magnitude of the circuit. If the oscillation frequency changes according to a voltage variation, the circuit is said to be a VCO. On the other hand, if the magnitude that controls the oscillation frequency is a current then the circuit is a Current Controlled Oscillator (CCO).

Whether it is a CCO or a VCO, an important feature to compare the performance of these circuits is the tuning range, which is a ratio defined by Eq. (3.18).

$$\text{Tuning range} = 2 \times \frac{f_{max} - f_{min}}{f_{max} + f_{min}} \tag{3.18}$$

It is common for the tuning range to be displayed as a percentage. In this case, the calculation of the tuning range is given by Eq. (3.19).

$$\text{Tuning range} = 2 \times \frac{f_{max} - f_{min}}{f_{max} + f_{min}} \times 100\ [\%] \tag{3.19}$$

3.2 Harmonic Oscillators

An oscillator is harmonic if it produces oscillations through a resonant mechanism, whose operating principle is a mutual energy transfer between two reactive elements. The resonant mechanism can be implemented by an LC network, formed by an inductor (L) in parallel with a capacitor (C). In CMOS technology, the most widely used harmonic oscillator implementations use these LC networks together with active circuits and are thus known as LC oscillators.

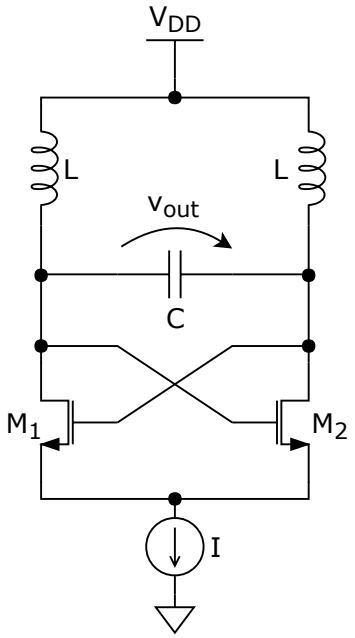

Figure 3.9: Cross-coupled LC oscillator.

The most common implementation of an LC oscillator is illustrated in Fig. 3.9. This circuit is also known as a cross-coupled oscillator because of the presence of the cross-coupled differential pair formed by the transistors M_1 and M_2. The high phase noise performance of the cross-coupled oscillator makes it widely used in the production of periodic RF signals.

The cross-coupled differential pair has the main function of compensating losses in the LC tank. This is achieved if the differential pair is operating in the linear region, as indicated in Fig. 3.10, implementing a negative resistance [32].

In order to calculate the equivalent resistance of the cross-coupled differential pair, it is necessary to analyze its small signal model as shown in Fig. 3.11.

Analyzing Fig. 3.11, it is confirmed that the cross-coupled differential pair has an equivalent resistance of negative value, as defined by Eq. (3.20).

$$R_x = \frac{v_x}{i_x} = -\frac{2}{g_m} \tag{3.20}$$

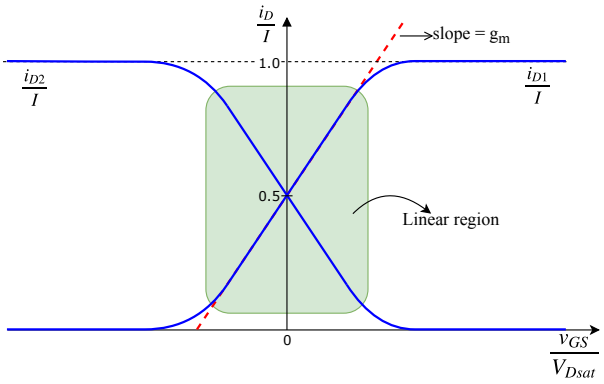

Figure 3.10: Voltage to current transfer characteristic of a differential pair (adapted from [19]).

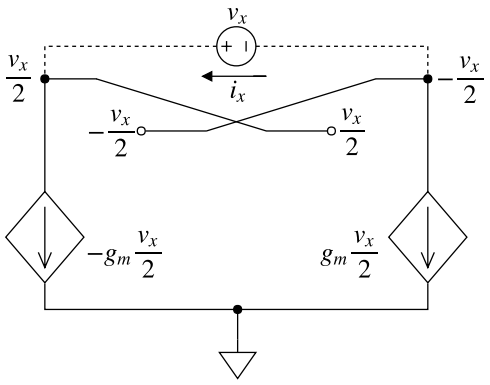

Figure 3.11: Small-signal model of a cross-coupled differential pair.

In terms of behavior, the LC oscillator can be modeled as shown in Fig. 3.12.

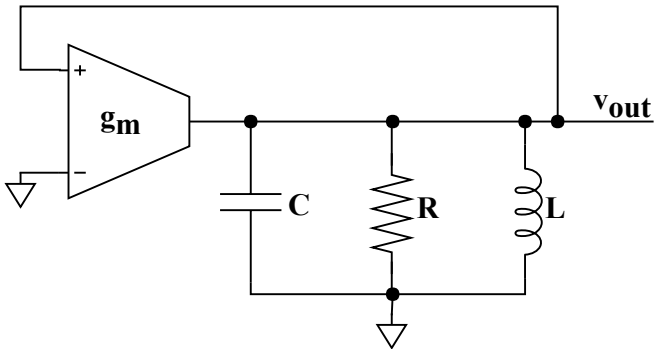

Figure 3.12: LC Oscillator behavioral model (adapted from [2]).

Since the LC oscillator is quasi-linear, the Barkhausen criterion can be applied. Thus, the circuit will oscillate if the conditions described by Eq. (3.4) and Eq. (3.5) are met. In the case of the model shown in Fig. 3.12, the transfer function $H(s)$ is given by Eq. (3.21) and $\beta(s)$ is given by the impedance of the parallel RLC circuit, as described by

Eq. (3.22) [2].

$$H(s) = g_m \tag{3.21}$$

$$\beta(s) = \frac{R}{1 + j\left(\frac{\omega}{\omega_o} - \frac{\omega_o}{\omega}\right)Q} \tag{3.22}$$

where

$$\omega_o = \frac{1}{\sqrt{LC}} \tag{3.23}$$

$$Q = R\sqrt{\frac{C}{L}} \tag{3.24}$$

For the resonant frequency, $\omega = \omega_o$, it follows that the Eq. (3.22) results in $\beta(s) = R$ and that the loop gain is given by Eq. (3.25).

$$L(s) = \left|H(s)\beta(s)\right| = g_m R = 1 \tag{3.25}$$

Although the condition described by Eq. (3.25) is necessary to obtain oscillations, it is not sufficient. This is due to the need to fulfill the start-up condition defined by Eq. (3.6), which in this particular case is translated into Eq. (3.26).

$$g_m > \frac{1}{R} \tag{3.26}$$

Integrated inductors have low quality factors, which typically are not sufficient to meet the requirements of the LC oscillator. For this reason, one of the main disadvantages of this oscillator is the large area occupied by its inductors, which leads to an increase in the manufacturing cost of the circuit.

3.3 RC Oscillators

There is another category of oscillators that use a hysteresis mechanism to produce periodic waves. Since these oscillators do not use LC networks, they are devoid of inductors, which allows drastic reduction of the area occupied on a chip. Moreover, since their networks of passive elements are exclusively composed of capacitors and resistors, these circuits are also known as RC oscillators.

Due to the absence of a resonant mechanism, no energy is preserved per oscillation period. Consequently, the quality factor of RC oscillators is closer to unity, resulting in a lower spectral purity when compared to LC oscillators [24].

The hysteresis mechanism of an RC oscillator is implemented by a non-linear element, which can be modeled by a Schmitt-trigger. For this reason, these oscillators generally have a strongly non-linear behavior that can be modeled by Fig. 3.13.

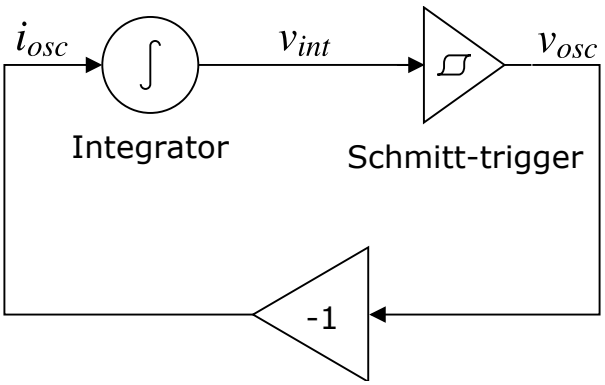

Figure 3.13: Non-linear oscillator behavioral model (adapted from [16]).

The integrator shown in the model is typically implemented by an RC impedance, converting an input current, i_{osc}, into an output voltage, v_{int}. Invented by Otto H. Schmitt, the Schmitt-trigger is a circuit whose transfer function is given by Fig. 3.14, where v_{int} is the input voltage of the circuit and v_{osc} is its output voltage.

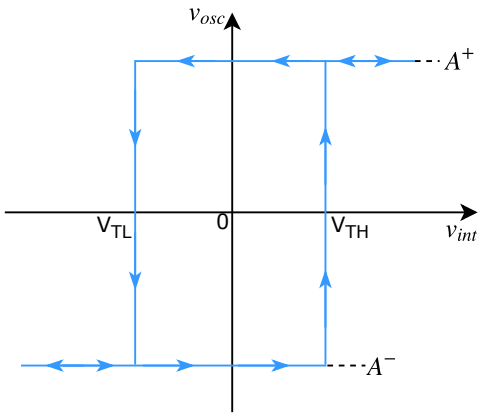

Figure 3.14: Schmitt-trigger transfer function (adapted from [19]).

As demonstrated by Fig. 3.14, if the circuit is in the state $v_{osc} = A^-$ it is possible to change to the state $v_{osc} = A^+$ by applying an input $v_{int} > V_{TH}$. On the other hand, if the circuit is in the state $v_{osc} = A^+$ then the change to the state $v_{osc} = A^-$ only occurs if $v_{int} < V_{TL}$. For input voltages in the range $V_{TL} < v_{int} < V_{TH}$, the output will depend on the previous state of the circuit, since it is determined by the previous value of the trigger signal (the signal that caused the last state change). For that reason this circuit can be seen as a memory element.

After this analysis to its transfer function, it is clear that the Schmitt-trigger serves as a comparator with hysteresis, limiting the amplitude of the oscillator modeled in Fig. 3.13. The inverter closing the negative feedback loop allows a periodic change in the polarity of the integrator input current, i_{osc}, ensuring steady-state oscillations [16].

These oscillators can be fully integrated due to their reduced areas. As a consequence, these circuits have low manufacturing cost. Other advantages of these oscillators are their wide tuning range and the ability to produce I/Q signals with low quadrature error [2].

In the following subsections, the main CMOS implementations of RC oscillators will be discussed.

3.3.1 Relaxation Oscillators

The most common relaxation oscillator is shown in Fig. 3.15.

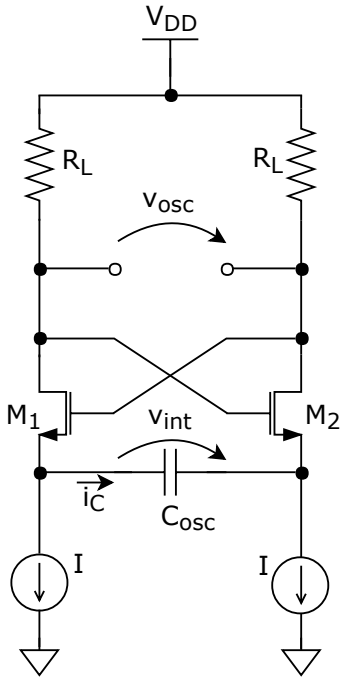

Figure 3.15: CMOS Relaxation oscillator.

In this topology, the capacitor, C_{osc}, is the practical implementation of the integrator presented in the model of Fig. 3.13. This is because C_{osc} is responsible for converting the DC current into a voltage through its integrator effect, defined by Eq. (3.27).

$$v(t) = \frac{1}{C}\int_{t_0}^{t} i(\tau)d\tau + v(t_o) \tag{3.27}$$

The input of the integrator is the capacitor current, i_C, with the output being a voltage, v_{int}.

The two transistors connected as cross-coupled inverters, together with the load resistors, R_L, form a latch modeled by an inverting Schmitt-trigger [2], whose transfer function is illustrated by Fig. 3.16.

Regarding the Schmitt-trigger, its input is the integrator voltage, v_{int}, and its output is i_C. Furthermore, it is assumed that there is a hard switch whenever there is a change in the sign of $v_{gs1} - v_{gs2}$ [2].

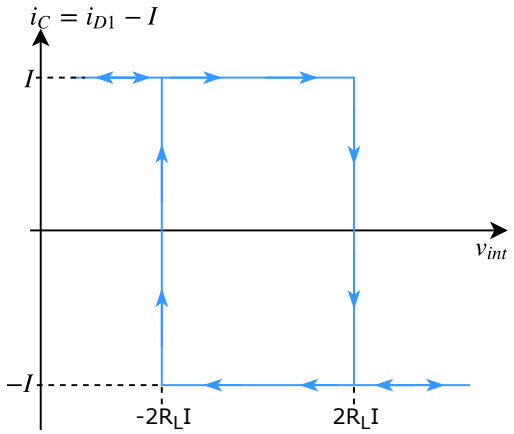

Figure 3.16: CMOS Inverting Schmitt-trigger transfer function (adapted from [2]).

As a result of this feedback loop between Schmitt-trigger and integrator, and as the model of Fig. 3.13 indicates, the circuit presents oscillation thanks to a periodic charge/discharge sequence of the capacitor. It is said that the oscillator works in relaxation mode if the transistors are designed with small dimensions, leading to reduced parasitic capacitances.

A valid approximation for the waveforms of this oscillator is illustrated in Fig. 3.17, where it is observed that the integration constant is given by $\frac{I}{C_{osc}}$.

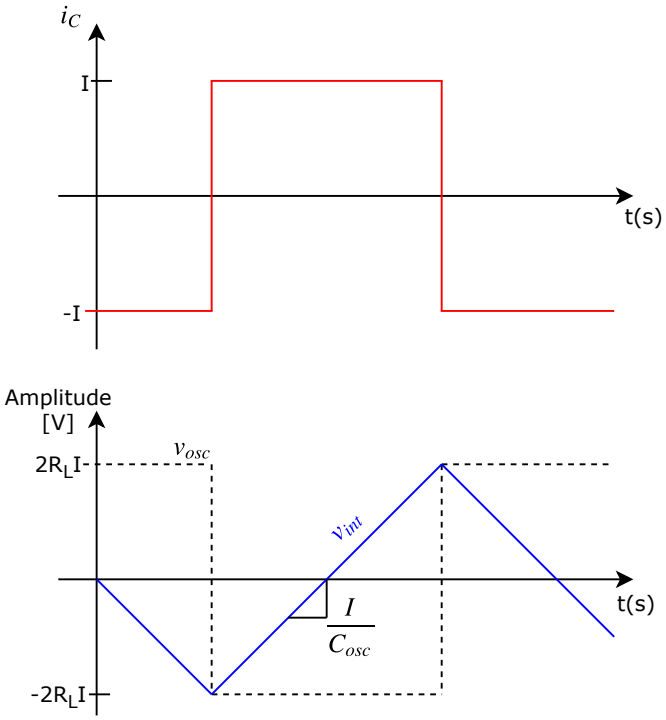

Figure 3.17: Relaxation oscillator waveforms.

The fact that the Schmitt-trigger operates as a hard-limiter prevents linearization of the circuit. Thus, the analysis of this oscillator must be made through a first order approximation when studying the integration time.

First, it must be assumed that the frequency of operation can be determined by the amount of charge accumulated in the capacitor during half oscillation period, as defined by Eq. (3.28).

$$q = C_{osc} V_{osc} \tag{3.28}$$

It is observable in Fig. 3.17 that $V_{osc} = 2R_L I - (-2R_L I) = 4R_L I$. In addition, it is known that the current in a capacitor relates to its stored charge as shown by Eq. (3.29).

$$\int_{t_1}^{t_2} I dt = CV = q \tag{3.29}$$

Knowing that $t_2 - t_1 = \frac{T_{osc}}{2}$ then Eq. (3.29) results in Eq. (3.30).

$$\frac{1}{2} \int_0^{T_{osc}} dt = 4C_{osc} R_L \tag{3.30}$$

Consequently, an approximation of f_{osc} is given by Eq. (3.31).

$$f_{osc} \approx \frac{1}{8R_L C_{osc}} \tag{3.31}$$

It is important to note that the approximation given by Eq. (3.31) is only valid for conditions in which the Schmitt-trigger functions as a hard-limiter, generating square waves with amplitude approximately equal to $4IR$. Thus, as the oscillation frequencies increase, the approximation loses its accuracy. For very high frequencies, this approximation of f_{osc} becomes invalid as the parasitic capacitances of the circuit filter the higher harmonics resulting in an approximately sinusoidal output signal whose amplitude is less than $4IR$ [2].

3.3.2 Ring Oscillators

A CMOS Ring oscillator typically contains an odd number of inverters connected in series in a feedback loop, as shown in Fig. 3.18.

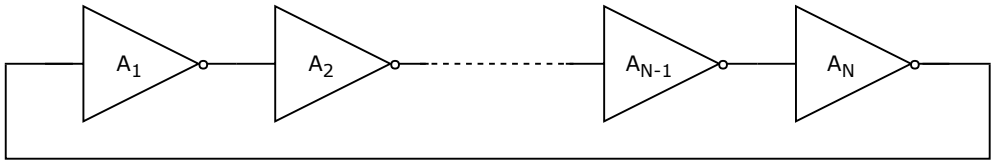

Figure 3.18: Ring oscillator (adopted from [21]).

The odd number of inverters results in a loop phase of -180^{o}, which allows an alternation of polarity.

In terms of high-level behavior, each inverter can be regarded as a gain stage followed by an integrator and a limiter, resulting in the model of Fig. 3.19.

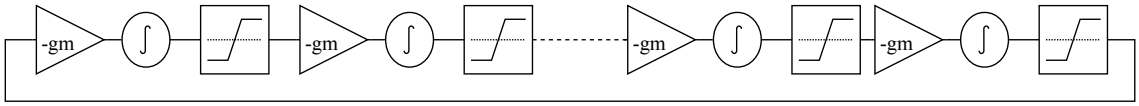

Figure 3.19: Ring oscillator high-level model.

Each inverter can be implemented in CMOS technology using a pair of transistors PMOS/NMOS with an output parasitic capacitance. Thus, a CMOS implementation of a ring oscillator is shown in Fig. 3.20.

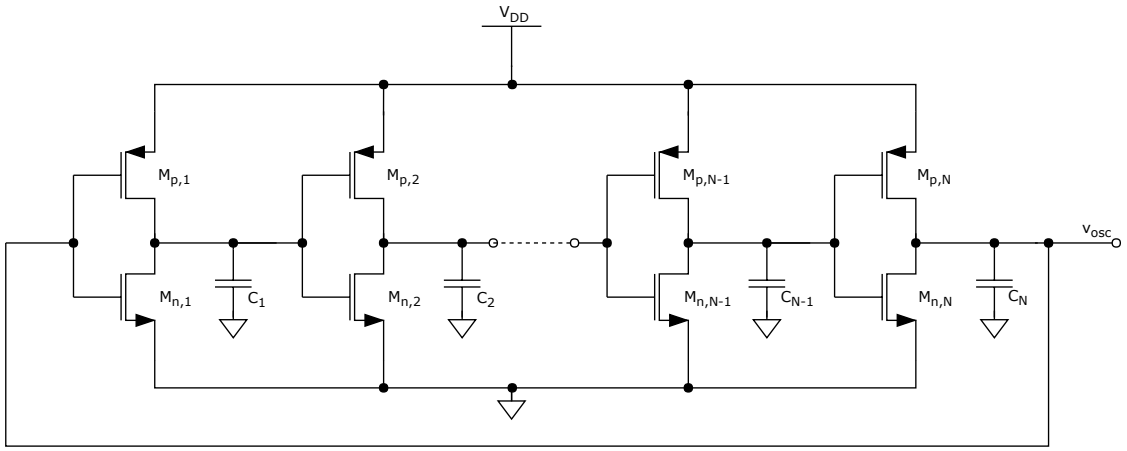

Figure 3.20: CMOS Ring oscillator.

The charge/discharge cycle of each parasitic capacitance is made by a current dependent on the resistance of the transistors. Whenever one of the MOSFET stops conducting, the capacitance can be charged up to the supply voltage or completely discharged to the reference node.

Thus, considering t_d as the time delay of each inverter, the output of this oscillator is a square wave whose oscillation frequency depends on the number of inverters, N, and the charge time of the output capacitor, as indicated by Eq. (3.32).

$$f_{osc} = \frac{1}{2N t_d} \tag{3.32}$$

Its simplicity makes this oscillator capable of reaching high frequencies with low energy consumption [16]. For this reason, the ring oscillator is typically the RC topology that achieves better performance results.

3.3.3 Two-Integrator Oscillator

It is possible to obtain oscillations for a circuit having two integrators together with an amplitude stabilization mechanism in a feedback structure. This circuit, known as a two-integrator oscillator, is an RC topology with an interesting characteristic: depending on some conditions, it may present a non-linear behavior or a quasi-linear behavior. In addition, this oscillator has inherent quadrature outputs, reaches high frequencies and has a wide tuning range [2].

In terms of high-level behavior, the two-integrator oscillator can be modeled as shown by Fig. 3.21. In this model each integrator is followed by a limiter whose mode of operation will dictate whether the circuit behaves as a non-linear or quasi-linear system.

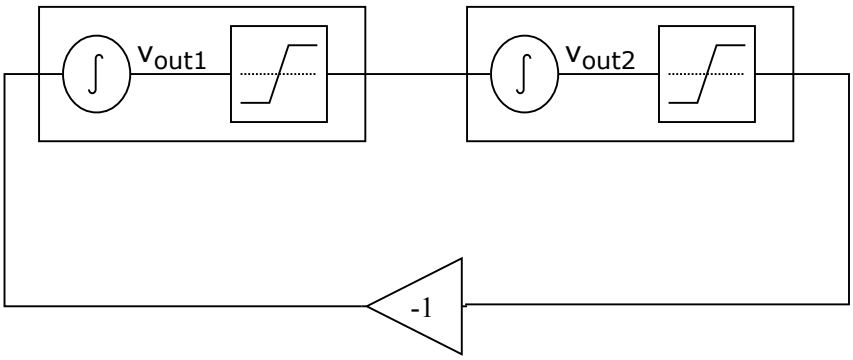

Figure 3.21: Two-integrator oscillator high-level model.

The CMOS implementation of a two-integrator oscillator is shown in Fig. 3.22.

The two integrators have a direct-coupling indicated by the red wires. In addition, there is a cross-coupling indicated by the blue wires providing quadrature outputs. The individual current sources, I_{level} and I_{tune}, enable independent control of the output amplitude and oscillation frequency, respectively.

3.3.3.1 Non-linear Operation

If in the model of Fig. 3.21 the block succeeding each integrator operates as a hard-limiter, then the oscillator has a non-linear behavior. In this scenario, the output of each integrator determines the polarity of the next integrator's input [33].

In this mode of operation, the limiter has at its output a square wave while the output of each integrator is a triangular wave with oscillation frequency given by Eq. (3.33).

$$f_{osc} = \frac{K_i}{2V_{OUT}} \tag{3.33}$$

Where K_i is the integration constant and V_{OUT} is the output amplitude [2].

As for the integrators, the output amplitude of each depends on the initial conditions of both and their integration constants, resulting in Eq. (3.34) and Eq. (3.35) [2].

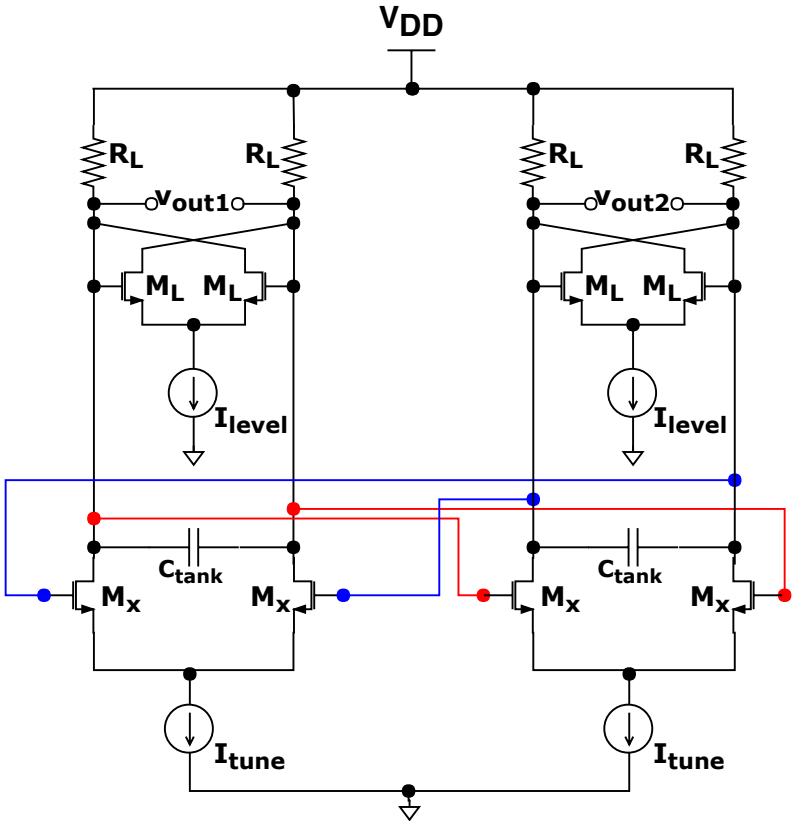

Figure 3.22: CMOS Two-integrator oscillator.

$$V_{OUT1} = 2\left(V_{INT1} + \frac{K_{i1}}{K_{i2}} V_{INT2}\right) \tag{3.34}$$

$$V_{OUT2} = 2\left(V_{INT2} + \frac{K_{i2}}{K_{i1}} V_{INT1}\right) \tag{3.35}$$

Replacing one of the previous equations in Eq. (3.33) it follows that the oscillation frequency is given by Eq. (3.36)

$$f_{osc} = \frac{1}{4\left(\frac{V_{INT1}}{K_{i1}} + \frac{V_{INT2}}{K_{i2}}\right)} \tag{3.36}$$

3.3.3.2 Quasi-linear Operation

In case the block succeeding each integrator operates as a soft-limiter, then the oscillator has an approximately sinusoidal output, presenting a quasi-linear behavior. In this scenario, the circuit can be modeled as a linear feedback system, as illustrated in Fig. 3.23.

The M_L transistors compensate the losses of the oscillator if the condition described by Eq. (3.37) is fulfilled.

$$\frac{1}{g_{mL}} = R_L \tag{3.37}$$

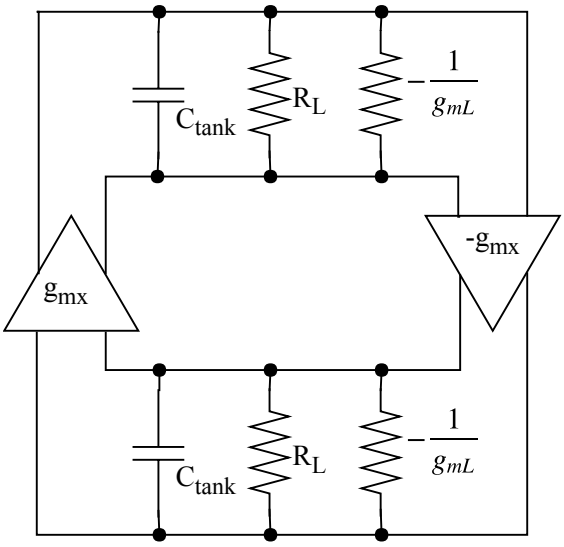

Figure 3.23: Two-integrator oscillator linear model (adopted from [2]).

Under these conditions the Barkhausen criterion can be applied to this oscillator, with its loop gain given by Eq. (3.38).

$$|L(s)| = \left(\frac{g_{mx}}{\omega C_{tank}}\right)^2 \tag{3.38}$$

Solving the condition given by Eq. (3.4), it is possible to obtain the oscillation frequency defined by Eq. (3.39).

$$\omega_{osc} = \frac{g_{mx}}{C_{tank}} \tag{3.39}$$

For this oscillator to have quasi-linear behavior, the differential pairs must work in the linear region. This implies that all transistors are always conducting, which leads to higher power consumption. Under these conditions, it is also verified that in practical terms the output amplitude can be approximated by Eq. (3.40) [2].

$$V_{OUT} \cong R_L I_{level} \tag{3.40}$$

3.4 State of the Art of CMOS Oscillators

The main constraint on the performance of oscillators is their phase noise, which means that the focus of research over the last few years has been an attempt to improve it through various techniques such as the use of a noise filter in harmonic oscillators [3], class-D oscillator topologies [4, 5], as well as coupled quadrature oscillators [6, 7] and complementary VCO with implicit common-mode resonance [8].

LC oscillators are used in applications where phase noise requirements are more demanding due to the high quality factor of their inductors.

In Tab. 3.1 a comparison is made between the state-of-the-art LC oscillators. To perform this comparison, a Figure of Merit (FoM) given by Eq. (3.41) is used.

$$FoM = \mathcal{L} + 10log_{10}\left(\left(\frac{\Delta f}{f_o}\right)^2\left(\frac{P_{DC}}{P_{ref}}\right)\right) \tag{3.41}$$

Where:

f_o - fundamental frequency; $\mathcal{L}$ is the phase noise measured at an offset from the fundamental frequency, Δf; P_{DC} is the oscillator power consumption and P_{ref} is the reference power, which in this case was considered to be 1 mW.

In this table, f_o is the oscillation frequency considered for the phase noise measurement.

Table 3.1: Performance comparison for state-of-the-art CMOS LC oscillators

Reference	Year	Topology	Tech [nm]	f_o [GHz]	Tuning range [%]	Δf [MHz]	$\mathcal{L}(\Delta f)$ [dBc/Hz]	P_{DC} [mW]	FoM [dBc/Hz]
[3]	2016	Wideband VCO with active inductor based noise filter	130	2	66.6	1	-120	2.1	-182.8
[6]	2017	Coupled quadrature oscillator with phase shifter	180	3.038	-	1	-123.2	6	-185.1
[4]	2014	Class-D Quadrature VCO	130	2.4	27	10	-145.69	1.92	-190.5
[7]	2018	Series-coupled Quadrature VCO	130	2.45	13.2	1	-130	3.4	-192.5
[8]	2016	Complementary VCO with implicit common-mode resonance	28	4.837	13.8	1	-119	0.5	-195.7
[5]	2014	Class-D Quadrature VCO	65	5	5	3	-137.1	2.1	-198.3

RC oscillators are best suited when full integration is the major concern due to their low areas. When considering quadrature outputs, coupled relaxation oscillators can be a good alternative to their coupled LC counterparts, as coupling reduces RC oscillator's phase-noise and quadrature errors [2].

Theoretical analysis suggest that the relaxation oscillator is the RC topology with the highest achievable performance [34], however, practical implementations indicate that ring oscillators have an advantage in this matter. This can be seen in Tab. 3.2, where the performance of state-of-the-art RC oscillators is compared.

Table 3.2: Performance comparison for state-of-the-art CMOS RC oscillators

Reference	Year	Topology	Tech [nm]	f_o [GHz]	Tuning range [%]	Δf [MHz]	$\mathcal{L}(\Delta f)$ [dBc/Hz]	P_{DC} [mW]	FoM [dBc/Hz]
[35]	2012	Quadrature Relaxation Oscillator	130	2.9	-	10	-115	8.64	-154.9
[36]	2017	Pulse-gate Voltage Controlled Ring Oscillator (VCRO)	130	1.872	145.4	1	-98.41	2.94	-159.16
[37]	2016	VCRO	65	5.3	94.7	1	-89.2	2.2	-160.2
[38]	2015	I/Q Cross-Coupled Relaxation VCO	130	2.5	8.3	10	-118.3	3.29	-161
[39]	2018	VCRO	180	1.22	33.3	1	-108.7	8.5	-161.1
[40]	2014	Quadrature Relaxation Oscillator	130	2.4	–	10	-122.9	3.08	-165.6
[41]	2016	Time-Interleaved VCRO	65	1.7	68.5	1	-100.4	0.65	-166.9
[42]	2013	VCRO	65	0.4	25.3	1	-111	0.158	-171

The ILO proposed in this thesis intends to combine, in a single circuit, the advantages of RC oscillators with levels of phase noise performance that approximate those of the LC oscillators.

Chapter 4

Injection Locking

Among the various techniques to improve the phase noise of an oscillator there are two main types: design techniques and frequency synthesizers. This latter option is the one that achieves better phase noise performance results.

A very promising frequency synthesizer is the ILO, which uses the properties of the physical phenomenon called injection locking to achieve synchronization of the oscillator output with a reference signal directly injected into the VCO.

This chapter begins with a brief discussion of the most common models of frequency synthesizers. Following, the fundamental principles of the phenomenon of injection locking are explained. Finally, the different synchronization models to describe the behavior of an ILO are discussed.

4.1 Frequency Synthesizers

The fundamental principle of a frequency synthesizer is to produce an output wave with a precise frequency. In order to achieve this goal, these types of circuits force a VCO to approximate the frequency of its output to a reference signal with high precision. There are two main approaches to designing a frequency synthesizer: the PLL and the ILO.

4.1.1 Phase-Locked Loop

A widely used frequency synthesizer structure is the PLL, shown in Fig. 4.1.

Typically, this synthesizer is a negative feedback loop composed of three mandatory blocks: a Phase Detector (PD), a Loop Filter (LF) and a VCO [1].

The PD compares the phases of its two input signals, obtaining this difference in its output.

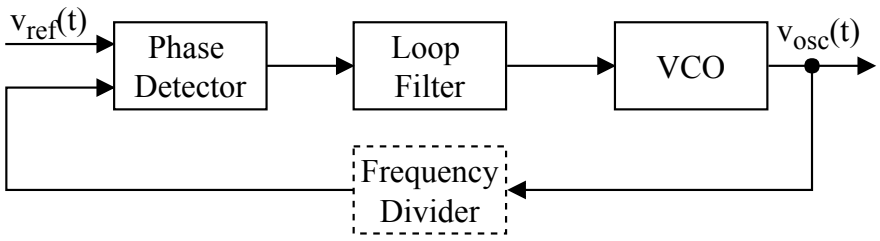

Figure 4.1: PLL Block diagram.

The LF block is usually implemented by an RC network. Thus, this block generates a DC voltage in its output resulting from an average of the PD output. Consequently, the VCO input will be a DC voltage proportional to the phase difference between its output and the reference signal.

The feedback loop will lead to phase error cancellation. In these conditions, the output of the PD stops affecting the VCO, it is said that the loop is locked, and the condition described by Eq. (4.1) is verified.

$$\phi_{osc}(t) - \phi_{ref}(t) \approx Constant \tag{4.1}$$

The gain and phase margins of the loop are defined by the LF. This means that this block establishes the compromise between the PLL bandwidth (also known as the locking range) and its stability. In addition, the LF introduces a low-frequency pole which prevents the existence of ripple in the VCO input signal, thus avoiding undesired frequency modulation. However, this pole's frequency should not be too low, as this would greatly increase the loop settling time. These trade-offs make the design of a PLL a challenging task.

It is common to see a PLL with an additional block: a digital frequency divider. The need to introduce this block stems from the fact that there are several communication standards operating in the GHz frequency range whereas the reference generators typically used in PLLs, the crystal oscillators, have maximum operating frequencies in the range of a few hundreds of MHz.

Thus, when introducing a frequency divider the PLL becomes flexible, allowing the transceiver to handle various standards. This advantage compensates for the other drawbacks associated with a PLL, such as increasing the circuit's complexity, area and consumed power.

4.1.2 Injection-Locked Oscillator

Another type of frequency synthesizer is the ILO shown in Fig. 4.2, where $v_{ref}(t)$ denotes a periodic signal that serves as reference and V_{ctrl} represents a DC voltage that controls the oscillation frequency. Using the properties of the injection locking phenomenon, the internal structures of the oscillator have similar behavior to the PD and LF blocks of a

PLL. Therefore, the VCO synchronizes its output with a reference signal (v_{ref}) directly injected into one of its nodes.

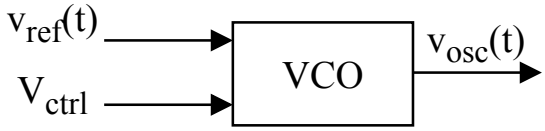

Figure 4.2: Frequency synthesizer with direct injection into a VCO.

This circuit has a simple implementation, as it requires neither additional blocks nor feedback and the concerns associated with it. Thus, this synthesizer overcomes the limitations of a PLL while achieving competitive performances [9, 10].

However, for this approach to work, the reference signal must operate in the same frequency range as the VCO.

4.2 Injection Locking Effect

One characteristic of oscillators is their sensitivity to charge variations. If, for example, a given stimulus disrupts the internal charge/discharge cycle in an RC oscillator, the phase noise can be affected, as illustrated in Fig. 4.3.

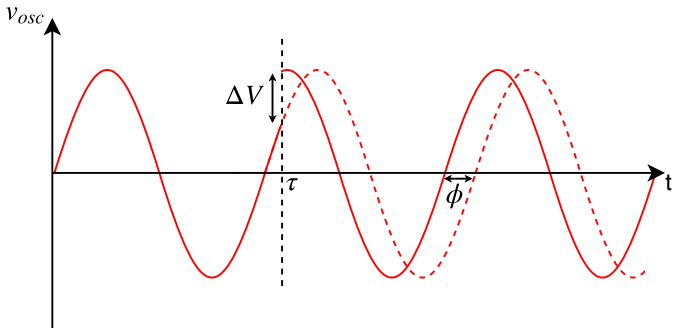

Figure 4.3: Oscillator phase-shift due to charge variation at instant τ (adopted from [16]).

In fact, phase noise is the most common type of charge variation, where phase shifts of the oscillator are induced in a stochastic way.

However, if the charge variation is produced by a periodic stimulus, positive consequences can be obtained. Under these conditions, if the stimulus has certain characteristics of frequency and magnitude, a frequency shift in the transient response of the oscillator is triggered. Consequently, the synchronization between the output signal and the periodic stimulus is forced [43, 44], as shown in Fig. 4.4.

When the oscillator reaches synchronization, the circuit is said to be an ILO and a correlation between its phase noise and that of the reference signal is observed [43]. This

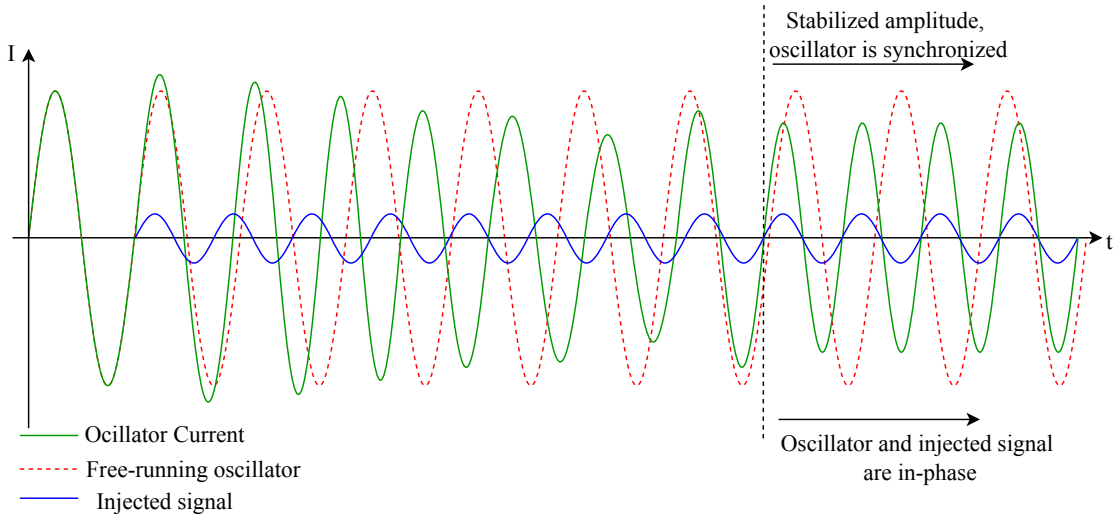

Figure 4.4: Syncronization of an oscillator using a periodic stimulus (adapted from [16]).

means that if the reference signal presents better frequency stability than the output of the free-running oscillator, the ILO will show an improvement in phase noise performance over the original circuit.

Due to these properties, the injection locking phenomenon allows the implementation of high performance, low cost and low power frequency synthesizers. Nevertheless, the maximum offset frequency for which an ILO still obtains synchronization, also known as locking range, is narrow. This limitation is one of the main causes for the lack of large scale adoption of the ILO as an alternative to a PLL.

4.3 Synchronization Models

Usually, an ILO is implemented in a simple way. For example, considering an LC oscillator as VCO, then to obtain an ILO the reference signal can be given by a current injected between the two drain nodes of the cross-coupled differential pair [45]. This circuit is illustrated in Fig. 4.5.

Despite the simplicity in implementing an ILO, its modeling and analysis is quite complex due to the highly non-linear nature of the synchronization process. Thus, to study the mechanisms of an ILO there are two types of approach, which will be explained in this section: A frequency-based analysis and a phase-domain approach.

4.3.1 Frequency-domain Models

From Eq. (4.1), it is possible to extract information that allows the construction of a frequency model of the synchronization mechanism of an ILO. From this study, relationships between important parameters such as injection level and frequency offset are obtained.

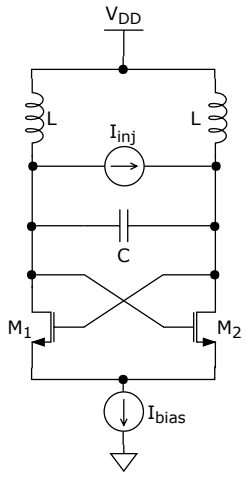

Figure 4.5: Injection-locked LC oscillator (adapted from [45]).

4.3.1.1 Adler's Model

Considering the aforementioned injection-locked LC oscillator, it is possible to model its high-level behavior through a feedback loop composed of a non-linear gain block and a linear filter whose purpose is to eliminate frequencies far from the oscillation frequency [43]. This model is illustrated in Fig. 4.6.

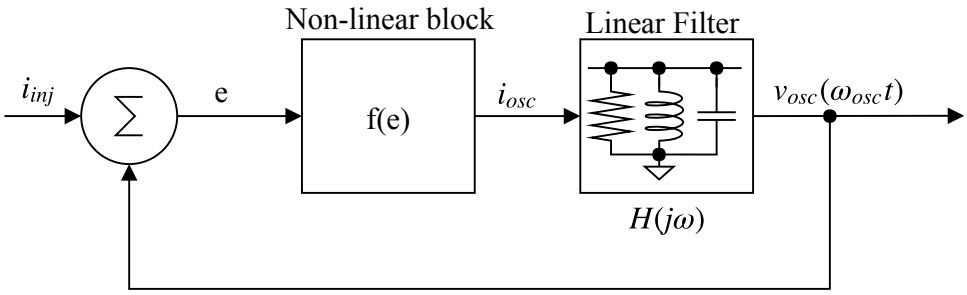

Figure 4.6: Injection-locked LC oscillator high-level model (adapted from [46]).

The non-linear block present in this model shows that the current flowing across the tank, i_{osc}, is assumed to be a non-linear function of the injected current, i_{inj}. The non-linearities of the circuit make it difficult to describe its temporal behavior, including the magnitude of the tank current. However, it is possible to extract information about the synchronization mechanism with a simpler analysis if the following concepts are considered:

- An LC oscillator can be assumed as a linear system. Therefore, the harmonic content generated by the non-linear block can be ignored, analyzing only the behavior of the circuit at its oscillation frequency ω_0.

- The characterization of a signal resulting from the sum of two other signals with different amplitudes, frequencies and phases is simplified by the use of phasors. A similar process would be much more complex using analytical methods. Thus, phasors can be used to study the synchronization mechanism.

Through the use of phasors it is possible to describe the synchronization process as shown in Fig. 4.7.

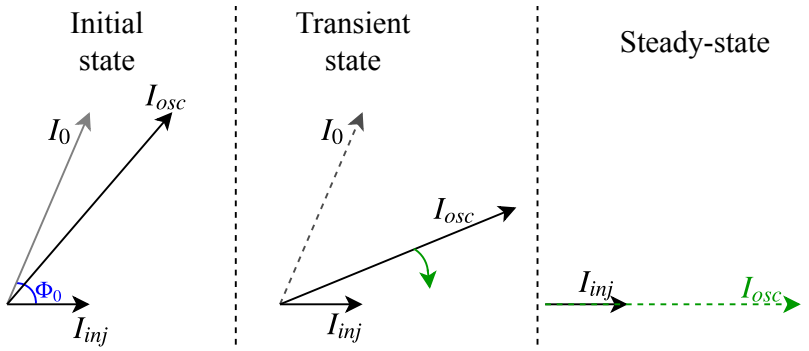

Figure 4.7: Phasor diagram illustrating synchronization of an ILO (adapted from [16]).

Where:

I_{inj} – Instantaneous amplitude of the injection current;

I_{osc} – Instantaneous amplitude of the current flowing across the tank;

I_0 – Initial value for I_{osc}, in the absence of injection current.

In the phasor diagram of Fig. 4.7 it is found that, after the injection of the signal i_{inj}, the current i_{osc} suffers a phase shift, which means that the zero phase shift condition given by Eq. (3.5) is no longer valid. To compensate for this, the oscillator will shift the oscillation frequency, causing its phase to approach that of the reference signal as shown in the transient state. Thus, after the initial state where the oscillator operates at the free-running frequency, ω_0, there is a frequency translation that occurs until the oscillator frequency, ω_{osc}, coincides with the frequency of the injected signal, ω_{inj}. In this case, the phase shift is suppressed and the oscillator is considered to have reached a steady-state, with $\omega_{osc} = \omega_{inj}$.

Taking this into account, it is possible to calculate the phase variation as indicated by Eq. (4.2) [43].

$$\frac{d\phi(t)}{dt} = \Delta\omega - \frac{\omega_0 I_{inj}}{2QI_0}\sin(\phi_0) \tag{4.2}$$

Where Q is the resonant network quality factor and ϕ_0 is the initial phase-difference between the oscillator current and the injected signal. When in steady state, the oscillator has zero phase shift and the equality described by Eq. (4.3) is valid.

$$\frac{d\phi(t)}{dt} = 0 \tag{4.3}$$

If the currents i_{osc} and i_{inj} are orthogonal, then $\phi_0 = 90°$ and Eq. (4.2) can be simplified. Hence the expression that defines the locking range, shown in Eq. (4.4).

$$\omega_L = \frac{\omega_0 I_{inj}}{2QI_0} \tag{4.4}$$

Regarding this last expression, there are important notes to consider:

- This model assumes that the reference signal has a sinusoidal waveform;
- The expression of Eq. (4.4) is only valid for weak injection, where $I_{osc} \gg I_{inj}$;
- The locking range is directly proportional to the power of the injected signa;
- The injection level automatically establishes a maximum limit for the bandwidth where synchronization is possible;
- The quality factor is inversely proportional to the locking range. This relationship allows an adjustment of the oscillator quality factor to overcome any limitations in the frequency and amplitude tunability of the reference generator;
- Although information about the locking range has been obtained, the evolution over time of the amplitude of current i_{osc} is unknown.

After the synchronization process is complete, the output signals from the reference generator and the oscillator have the same frequency, with residual phase differences. Thus, the phase noise of the oscillator will be improved due to the existing correlation with the spectrum of the injected signal, as shown in Fig. 4.8.

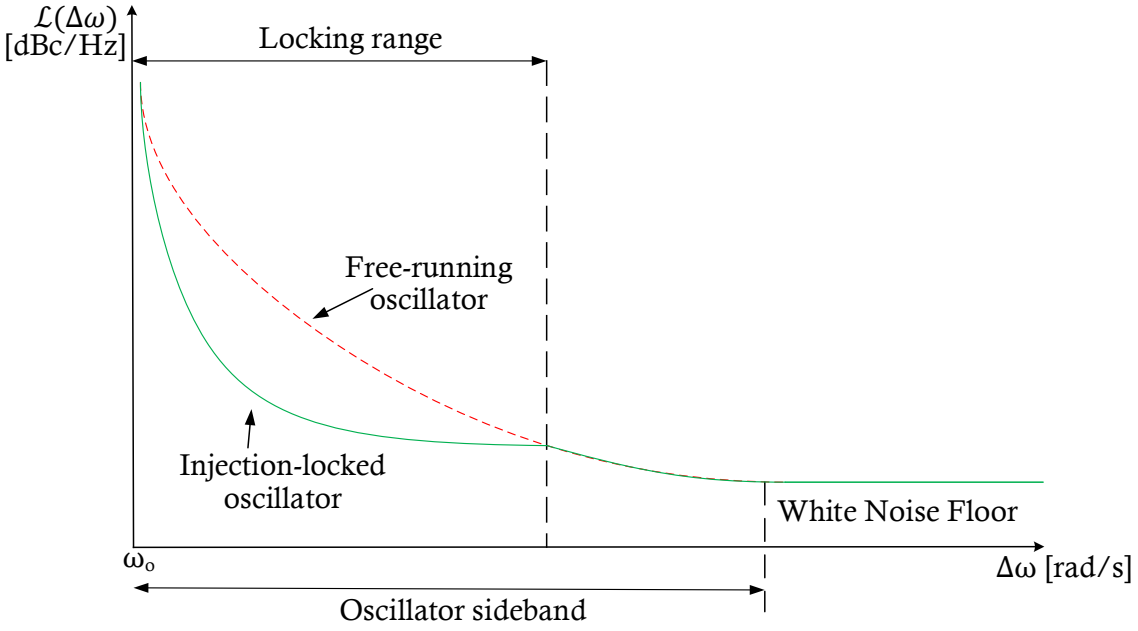

Figure 4.8: Phase noise improvement within the locking range (adapted from [16]).

Observing Fig. 4.8, it is confirmed that the locking range establishes the maximum limit for the bandwidth where the injected signal can condition the ILO phase noise. In this frequency band, the ILO behaves like an LPF that filters the phase noise of the reference signal. Under these conditions, the phase noise of the circuit is described by Eq. (4.5) [46].

$$\mathcal{L}_{sync}(\Delta\omega) = \mathcal{L}_{free}(\Delta\omega)\frac{\Delta\omega^2}{\Delta\omega^2 + \omega_L^2} + \mathcal{L}_{inj}(\Delta\omega)\frac{\Delta\omega_L^2}{\Delta\omega^2 + \omega_L^2} \tag{4.5}$$

Analyzing the expression shown in Eq. (4.5), it is confirmed that there is a direct proportionality between the locking range and the bandwidth where the oscillator phase noise improvement occurs.

By observing the synchronized oscillator, the Adler's model presents a simplified and intuitive description of the synchronization mechanism. Therefore, this model is solely based on frequency, not taking information about the transitory regime, the settling time and the locking time. In addition, this model only applies to resonators, which prevents its direct application in oscillators based on hysteresis mechanisms. It is possible to obtain generalizations of this model, although they involve increased costs in the complexity and design process [47].

4.3.1.2 Miller's Model

The generalized Miller model, shown in Fig. 4.9, is a variation of the Adler's model that allows the modeling of synchronizations with different frequency ratios between the output and reference signals [46].

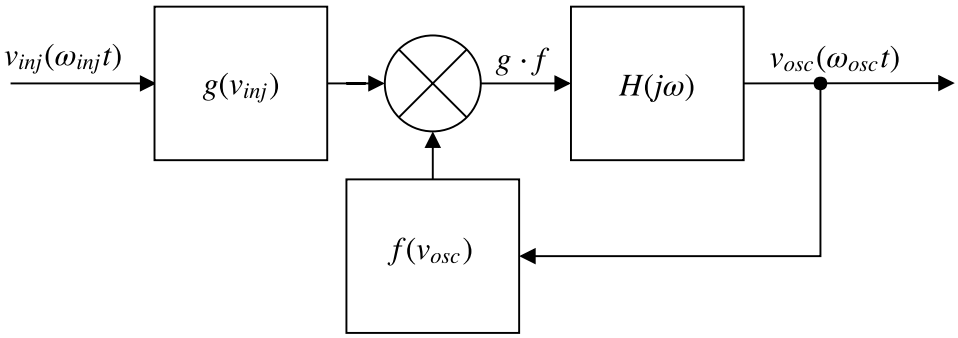

Figure 4.9: Miller injection model (adapted from [46]).

In this model two memoryless non-linear functions, $g\left(v_{inj}\right)$ and $f\left(v_{osc}\right)$, can be defined by Eq. (4.6) and Eq. (4.7).

$$g\left(v_{inj}\right) = \sum_{n=0}^{\infty} g_n \cdot v_{inj}^n \tag{4.6}$$

$$f\left(v_{osc}\right) = \sum_{m=0}^{\infty} f_m \cdot v_{osc}^m \tag{4.7}$$

The block $H(j\omega)$ behaves as a BPF centered on the oscillation frequency and whose input is given by the products of the mixing operation $g \cdot f$, defined in Eq. (4.8).

$$g\left(v_{inj}\right) \cdot f\left(v_{osc}\right) = \sum_{n=0}^{\infty} G_n \cdot \sin\left(n\omega_{inj}t\right) \sum_{m=0}^{\infty} F_m \cdot \sin\left(m\omega_{osc}t\right) \tag{4.8}$$

If any of the products resulting from Eq. (4.8) are in the filter passband, then synchronization is triggered [44]. Thus, according to this model it is possible to classify the synchronization according to the frequency ratio:

- If $n\omega_{inj} = \omega_{osc}$, then it is a sub-harmonic synchronization;
- On the other hand, it is possible that the circuit is under fundamental synchronization, with $\omega_{inj} = \omega_{osc}$;
- There is also the possibility of super-harmonic synchronization, where $\omega_{inj} = m\omega_{osc}$.

For any kind of synchronization to occur the free-running oscillator frequency, ω_0, must meet the condition described by Eq. (4.9).

$$m\omega_0 \approx n\omega_{inj} \tag{4.9}$$

If the frequency of the oscillator shifts until it meets the condition described by Eq. (4.10), then a synchronization of order n:m occurs [44].

$$\omega_{osc} = \frac{n}{m}\omega_{inj} \tag{4.10}$$

Using harmonic synchronization, it is possible to implement frequency dividers, as shown in Fig. 4.10.

In this frequency divider, the cross-coupled differential pair of transistors acts as a mixer, whose conversion gain will determine the amplitude of the injected current. In addition, the locking range of this ILO is given by Eq. (4.11) [45].

$$\omega_L = \frac{\omega_0}{2Q} \cdot \frac{4}{\pi} \cdot \frac{I_{inj}}{I_0} \tag{4.11}$$

4.3.2 Phase-domain Models

Using computational tools, it is possible to produce synchronization macro-models based on the phase domain. A practical example of the utility of these models lies in the design of PLLs as they simplify its analysis and simulation, allowing designers to focus on system-level requirements such as loop stability.

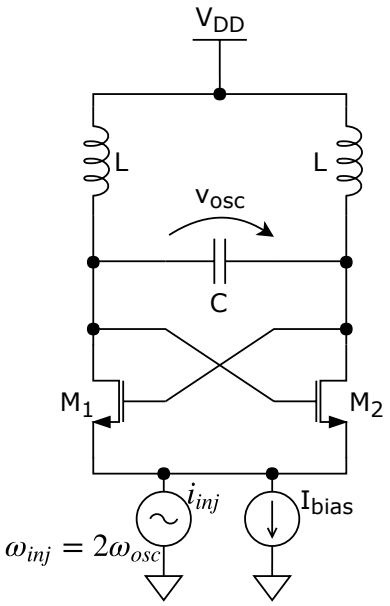

Figure 4.10: Injection-locked divider (adapted from [45]).

A phase model is based on the description of how the oscillator generates phase shifts in its output in response to certain stimuli. Moreover, these types of models allow greater transparency regarding the nonlinearities and temporal behavior of the circuit. Consequently, it is possible to describe the oscillator in a simple way using a hardware description language, such as Verilog [16]. The fact that these models are produced using simulation-assisted processes leads to these being more accurate and applicable to any oscillator topology or injection type.

Briefly, the phase domain models have the following characteristics:

- They involve complex and time-consuming processes;
- Allow a greater extraction of information than the frequency models;
- Are suitable for any topology.

On the other hand, the frequency domain models are distinguished by being:

- Obtained using simple methods;
- Unclear regarding information on settlig time;
- Not general, having to be adjusted according to the topology.

It is well known that RC oscillators achieve synchronization in a few periods. Thus, in this type of oscillators it is less relevant to define time-based parameters such as settling time or locking time, which means that the use of phase models can be ignored [48]. In addition, RC topologies such as the two-integrator oscillator are capable of operating in

two modes: quasi-linear and non-linear, leading to a wide variety of time patterns, which indicates that phase modeling would result in erroneous estimates of phase shifts across the tuning range.

Since the purpose of this thesis is to analyze the phase noise improvement of an RC oscillator within the locking range, the simplicity of frequency models makes them the best option to analyze the ILO developed in this work. For these reasons, this thesis does not describe in detail the theory of phase modulation. However, for an in-depth study of the different phase models, such as the input sensitivity function based approach or the phase-transfer model, it is possible to consult [49] and [50], respectively.

CHAPTER 5

REFERENCE SIGNAL GENERATORS

There are two types of reference signal generators that can be used in frequency synthesizer implementations: the crystal oscillator and the STO. This chapter addresses the operating principles of each of these reference generators. In addition, a discussion is made on the characteristics of each of these two types of circuit, comparing its advantages and disadvantages.

5.1 Crystal Oscillator

The primary reason for the use of crystals in timing reference circuits is their piezoelectricity property [11]. According to this phenomenon, when a voltage is applied to an electrode placed near or on the crystal, it undergoes a mechanical distortion, as illustrated in Fig. 5.1.

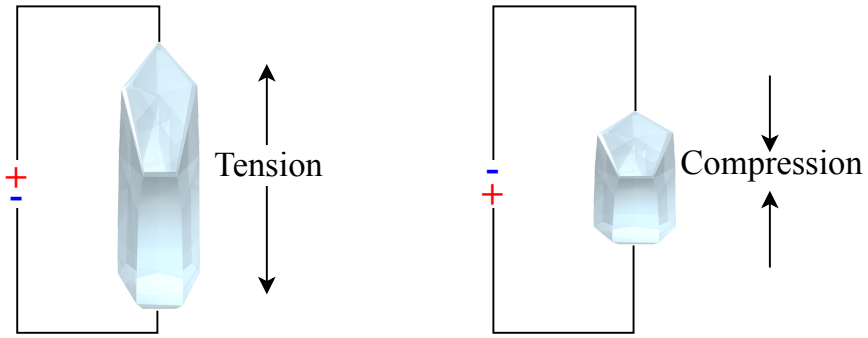

Figure 5.1: Piezoelectric phenomena on a crystal (adopted from [16]).

Due to the elastic properties of the crystal, it will return to its initial state, generating an opposing voltage. Thus, the crystal vibrates if it is submitted to an electric field.

Quartz crystals, with electrodes connected on each side, are the most widely used for this type of reference generator. These crystals have a precise resonance frequency due to a low dependence of its elastic constants and its excellent temperature stability. To represent a crystal, the symbol shown in Fig. 5.2 is used.

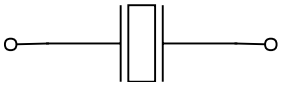

Figure 5.2: Electrical symbol for a crystal.

As the crystal generates an opposing voltage so as to return to its original shape, then the crystal can be modeled by an RLC circuit, as depicted in Fig. 5.3.

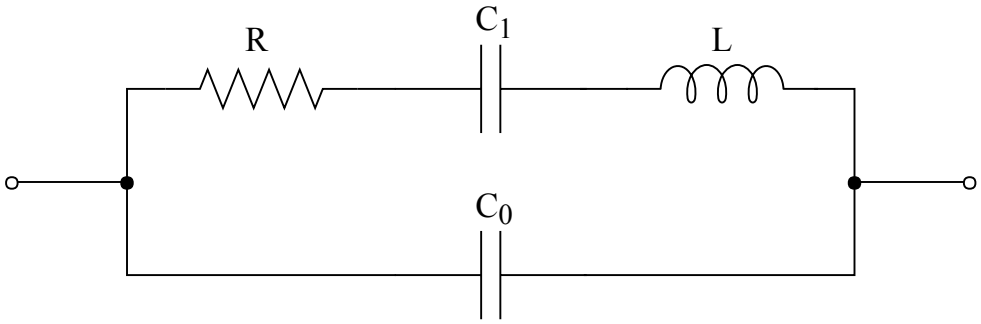

Figure 5.3: Electrical model of a crystal.

In the model shown above, the series branch composed of R, L and C_1 represents the thin piece of quartz, while C_0 represents the shunt capacitance of the electrodes in parallel with the holder capacitance [51]. Therefore, the Laplace transform of the equivalent impedance of the circuit of Fig. 5.3 is given by Eq. (5.1).

$$Z_{xo}(s) = \left(R + \frac{1}{sC_1} + sL\right) \| \left(\frac{1}{sC_0}\right) \tag{5.1}$$

Consequently, it is observed that the crystal has two resonant frequencies, where the reactances cancel each other [51]: the series resonant frequency, ω_s, expressed in Eq. (5.2); and the parallel resonant frequency, ω_p, defined by Eq. (5.3).

$$\omega_s = \frac{1}{\sqrt{LC_1}} \tag{5.2}$$

$$\omega_p = \omega_s \left(1 + \frac{C_1}{2C_0}\right) \tag{5.3}$$

Due to the constituent elements of the model of Fig. 5.3, depending on the circuit where it is applied, the crystal may exhibit either a capacitive behavior or an inductive behavior, as shown in Fig. 5.4.

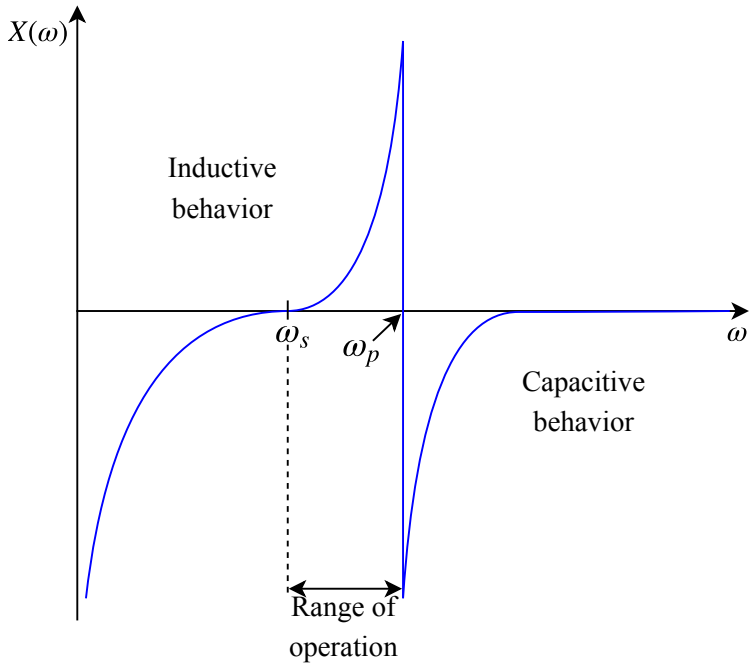

Figure 5.4: Crystal reactance vs frequency (adapted from [16]).

The range of operation between ω_s and ω_p, shown in Fig. 5.4, can be slightly adjusted if load capacitances are added.

The series resonant frequency ω_s, also known as the crystal fundamental frequency, is defined by the cut of the quartz piece, being strongly insensitive to temperature variations. As a consequence, crystals have Q factors in the range of 10000 to 100000 for operating frequencies in the MHz range, which is much higher than the typical Q factors of integrated inductors (around 10 for operating frequencies in the GHz range).

In order for the crystal to oscillate it is necessary to place it in a feedback loop together with an amplifier, as exemplified in Fig. 3.1 for the harmonic oscillators [11]. Therefore, the crystal oscillator must have a topology as shown in Fig. 5.5, this being a circuit with great frequency stability and very low phase noise.

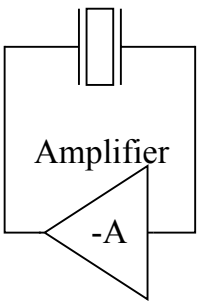

Figure 5.5: Crystal oscillator high-level model.

The dependence ratio between the fundamental frequency and the cut of the crystal

implies that the manufacturing process will limit the maximum frequency of the oscillator, since small and thin crystals are required for high frequencies . The crystal oscillators present in the vast majority of mobile devices use conventional AT-cut crystals and operate at a fundamental frequency in the range of 20 to 50 MHz [52]. Operating at a higher frequency involves two possibilities: the use of harmonic oscillation; or the use of other crystal technologies with higher fundamental frequencies but with substantially lower Q factors [52].

If harmonic oscillation is used to achieve higher operating frequencies, there are two possibilities: change the cut and shape so that the crystal vibrates at various frequencies, odd multiples of the fundamental frequency, called overtones; or to produce crystals of non-uniform thickness, which will generate harmonics of the fundamental frequency. However, regardless of the chosen option, the circuit will only reach frequencies in the range of a few hundred of MHz [11] and will require additional LC circuits for selectivity. Thus, crystal oscillators have frequencies that are far below the GHz range used by a vast number of communication standards.

In addition, the inability to make significant adjustments in its operating frequency is another major drawback of a crystal oscillator.

5.2 Spin Transfer Torque Nano-Oscillator

An STO is a nano-scale device that uses spintronic principles to implement an integrated CCO, with operating frequencies in the microwave range and an extremely wide tunability. The transfer of angular momentum to the magnetization of a thin magnetic layer is the basis for the STO operation [53].

There are two key principles of spintronics that allow for the implementation of an STO: Spin Transfer Torque (STT) and magnetoresistance. The STT phenomenon provides the STO with a magnetic compensation mechanism, while the magnetoresistance effect functions as an hysteresis mechanism on the nanometric device.

5.2.1 Spin Transfer Torque

Inside a multi-layered magnetic structure, it is possible to transfer the angular momentum of electrons, also known as spin, between the different magnetic layers. Consequently, a torque is exerted on the local magnetization. Through the use of a spin-polarized current, it is possible to guarantee the precession of magnetization (torque transfer) of a nanometric magnetic layer, in which case the structure is said to be under the STT effect. In most cases, an STO has a multi-layer structure as illustrated in Fig. 5.6.

This structure has a thin non-magnetic layer, called spacer, that separates the other two magnetic layers. At the bottom of the structure is the polarized layer, which has this name due to having a fixed magnetization, M_p, while at the top is the free layer, whose magnetization is free to rotate, M_{free}.

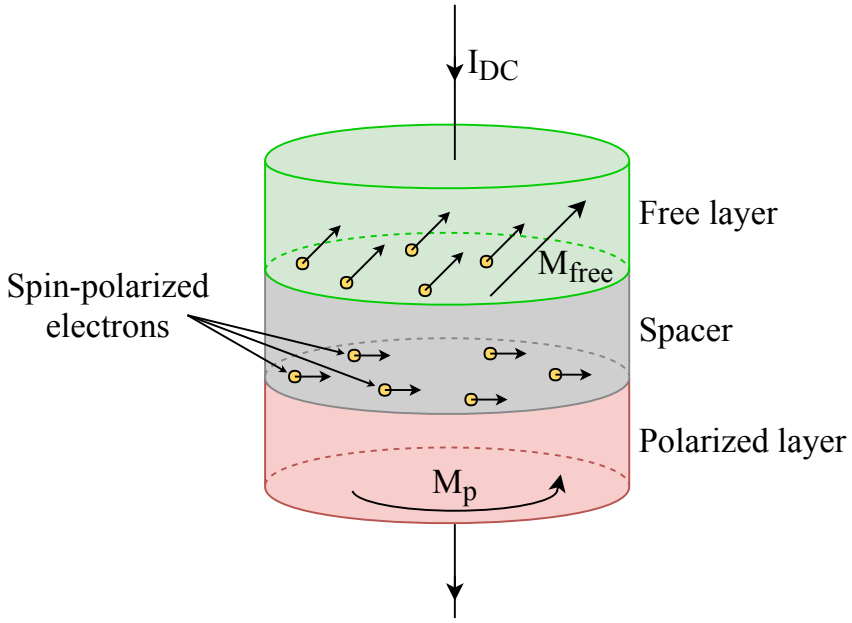

Figure 5.6: STO physical struture (adapted from [12]).

The injection of an unpolarized current, I_{DC}, triggers the STT effect. The direction of I_{DC}, shown in Fig. 5.6, indicates that the electrons reach the polarized layer first, causing a spin-polarized current to be generated there. Consequently, there is a transfer of spin from the electrons into the free layer, producing a torque in the local magnetization. A compensation for the magnetization damping in the spacer will be made by the exerted torque.

On the other hand, this compensation of the magnetization damping is not enough for the STO to reach a steady state [53]. For the circuit to oscillate, the magnetization on the free layer must undergo a rotation whose orientation alternates periodically. The magnetoresistance effect is what makes this alternation possible [54].

5.2.2 Magnetoresistance

The magnetoresistance effect describes a mechanism in which the electron transport is affected by the magnetic state of the structure, functioning as a dual phenomenon of the STT, where the magnetic state is affected by the electron transport [54]. More specifically, the magnetoresistance effect describes how the resistance of the spacer layer is affected by the relative orientation of the magnetization of the magnetic layers. This is illustrated in Fig. 5.7, where it is possible to identify two scenarios: a parallel and an anti-parallel state.

If the structure has its magnetic layers with aligned polarizations, then the device is in a parallel state where the magnetic precession is made with low resistance. On the other hand, when the structure is in an anti-parallel state, there is an increase in

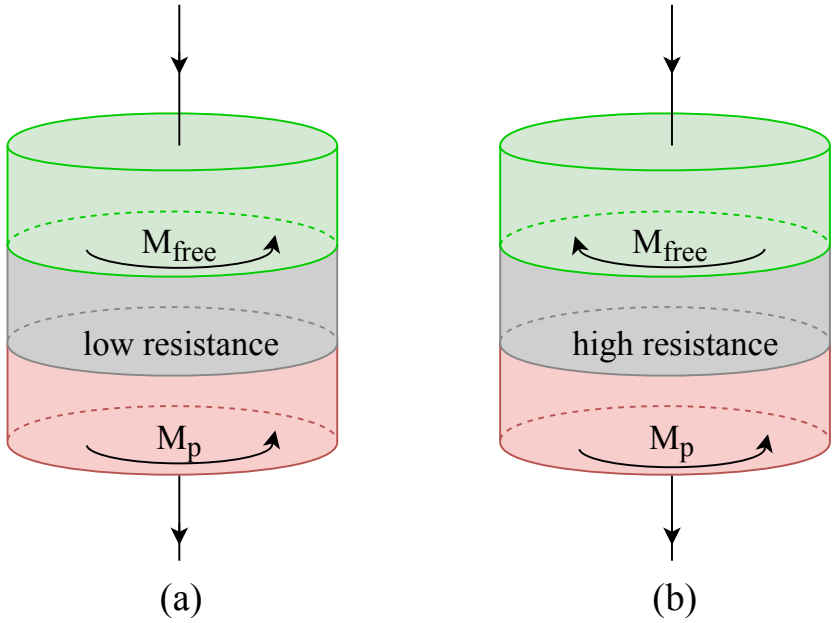

Figure 5.7: Magnetoresistance effect: (a) Parallel state; (b) Anti-parallel state (adapted from [12]).

the scattering of conduction electrons, which translates into a high resistance in the spacer [54]. Therefore, an STO can only produce steady-state oscillations by combining the STT and magnetoresistance phenomena.

5.2.3 Types of Spin Torque Oscillators

There are two types of magnetoresistance, which in turn is what defines the classification of an STO. If the spacer layer is a thin insulator, the structure is said to have a Tunneling Magnetoresistance (TMR) and is classified as a Magnetic Tunnel Junction Spin Torque Oscillator (MTJ STO). On the other hand, if a metal spacer is used, the device has a Giant Magnetoresistance (GMR) and is known as a Spin Valve Spin Torque Oscillator (SV STO). Both types of STO have the following characteristics:

- Can be tuned either by a magnetic field or by a current;
- They have high tuning ranges (dependent on the variation of the magnetoresistance) with values higher than 30 %;
- They are low footprint structures (less than $100\mu m$);
- They have a low-cost of production;
- Its manufacturing process is compatible with CMOS technology.

However, there are some drawbacks associated with this emerging technology, such as:

- Very low output powers, with typical amplitudes comparable to the Root Mean Square (RMS) of CMOS noise (in the order of $nV/\sqrt{Hz}$);
- Spectral impurities that are translated into frequency fluctuations;
- Low yield.

Considering the operation of both types of STO, it is usually observed that the SV STO presents higher oscillation frequencies and better spectral purity, whereas the MTJ STO offers the highest values of output power [12]. In fact, because of its larger magnetoresistance, the MTJ STO can provide an output power in a range between -60 dBm to -40 dBm [55]. On the other hand, this type of STO presents Q factors with values typically around 100, since they have frequency fluctuations within closer offsets (<10 MHz). As for the SV STO, it has a smaller magnetoresistance, resulting in output powers in the order of -70 dBm, although they obtain a better frequency stability and consequently higher Q factors, whose theoretical limit goes up to 18000.

5.3 Discussion

Taking into account the reference generators presented in this chapter, it is possible to compare their main characteristics as shown in Tab. 5.1.

Table 5.1: Reference generators comparison.

Reference Generator	Advantages	Disadvantages
Crystal Oscillator	High Q (in the MHz Range); Mature technology; Low cost.	Low frequency (in the MHz range); Low tunability; Not compatible with CMOS.
Spin Torque Oscillator	Low area; High frequency (in the GHz range); Compatible with CMOS; Large tuning range; High Q (in the GHz range).	Low output power; Frequeny fluctuations; Low yield.

Looking at Tab. 5.1, it becomes clear that the crystal oscillator has several limitations that make it difficult to be used in an ILO. First, its incompatibility with the CMOS process precludes the full integration of an ILO that has this type of reference generator. In addition, the crystal oscillator has operation frequencies in the MHz range, which hamper its use as reference generators for applications in a large number of communication standards. Finally, it is important to note that the crystal oscillator has low tunability, with even narrower ranges than typical values for LC oscillators.

On the other hand, despite its disadvantages, the STO seems to be the more suitable reference generator for the implementation of a fully integrated ILO. The fact that the STO is a technology in early stages of development suggests that there is a large margin for its disadvantages to be mitigated. Among the several advantages of using an STO

as a reference generator, some deserve to be highlighted. Firstly, it is the compatibility between the CMOS and the STO manufacturing processes that allows full integration of an ILO that uses this type of reference generator. In addition, the high frequency and tunability of the STO enables the implementation of a multi-standard receiver. Finally, the fact that this type of reference generator is current biased allows the use of a biasing structure common to both the STO and the CMOS VCO.

Between the two types of reference generator, the STO is the most advantageous solution for implementing a cheap, multi-band and fully integrated ILO. Therefore, it is expected that the hybrid oscillator that results from this implementation has a phase noise performance with values between those of an LC oscillator and those of a crystal oscillator, in addition to having a wide tuning range in the order of GHz.

Chapter 6

Injection Locked RC Oscillator with STO as reference generator

Based on the theory discussed in the previous chapters, it is time to implement an ILO based on an RC oscillator, using an STO as a reference generator. Subsequent to this implementation, the theoretical predictions that the implemented ILO will achieve an improvement in phase noise performance relative to that of the free-running RC oscillator should be confirmed. To achieve these goals, this chapter begins by addressing which RC topology is best suited for the free-running oscillator. Next, the proposed circuits are presented, which describe the implementations of the free-running oscillator and the ILO in both 130 nm and 180 nm CMOS technologies. After that, the design guidelines for each implementation are presented, followed by circuit simulations. Finally, a discussion about the simulation results for each implementation is made.

6.1 Chosen Topology for the RC Oscillator

Knowing that the free-running oscillator will have an RC topology, it is important to define which one is best suited for this purpose. Within the RC topologies, the ring oscillator has been the most investigated circuit in recent years. This great interest is due to factors such as its higher practical phase noise performance compared to other RC oscillators, and its simplicity of implementation and analysis. However, the relaxation oscillator has a set of features that make it more suitable for implementing an ILO. In particular, a relaxation oscillator has:

- Different injection points with unique characteristics, such as nodes that contain only even-order harmonics. With this greater possibility of choice, it is possible to introduce different signal injection schemes;

- Theoretically, the best achievable noise performance among RC oscillators [34]. This feature should allow the correction of phase noise without compromising frequency or total power consumption.

Before choosing the RC oscillator topology best suited to the purpose of this thesis, it is convenient to know that the target specifications for the implementation of the ILO are as follows:

- Minimum oscillation frequency: 100 MHz;
- Tuning range should be as wide as possible, including the 2.4 GHz frequency (Industrial, Scientific and Medical (ISM) band);
- Image cancellation using I/Q Outputs;
- $\mathcal{L}(1MHz) < -100$ dBc/Hz (better than the typical phase noise values for RC oscillators in the GHz range).

Considering the specifications described above, it becomes clear that the RC topology that should be chosen is the two-integrator oscillator, because it has the following characteristics:

- The structure of this circuit is comparable to that of a relaxation oscillator. Therefore, it is possible to extrapolate the observations and conclusions applied to it;
- It is an oscillator with an inherent wideband in the GHz range;
- It is a topology with inherent I/Q outputs, avoiding an increase in circuit complexity to obtain it;
- It is a circuit whose amplitude of oscillation can also be tuned, thus having another degree of freedom;
- It is an oscillator capable of operating in a quasi-linear mode for high frequencies, resulting in a spectrum with few harmonics, mostly composed of one component at the oscillation frequency and another at twice that frequency. This feature allows to minimize unwanted modulation effects that could affect the observations to the circuit in situations where a physical prototype would not have a perfect shielding.

6.2 Proposed Circuits

This section begins by introducing the implementation of the free-running oscillator based on the RC topology defined in the previous section. Subsequently, the implementation of the ILO is presented, comprising the addition of an injection block to the free-running oscillator and synchronization with the reference signal generated by the

STO. Afterwards, the fundamental concepts that justify the use of the implemented injection block are discussed. To close this section, the design guidelines used for each circuit implementation are presented.

6.2.1 Free-Running Oscillator

As a starting point and for subsequent comparison, a two-integrator oscillator based on Fig. 3.22 is designed. The implementation of this circuit in the 130 nm and 180 nm CMOS technologies used in this thesis constitutes the free-running oscillator shown in Fig. 6.1.

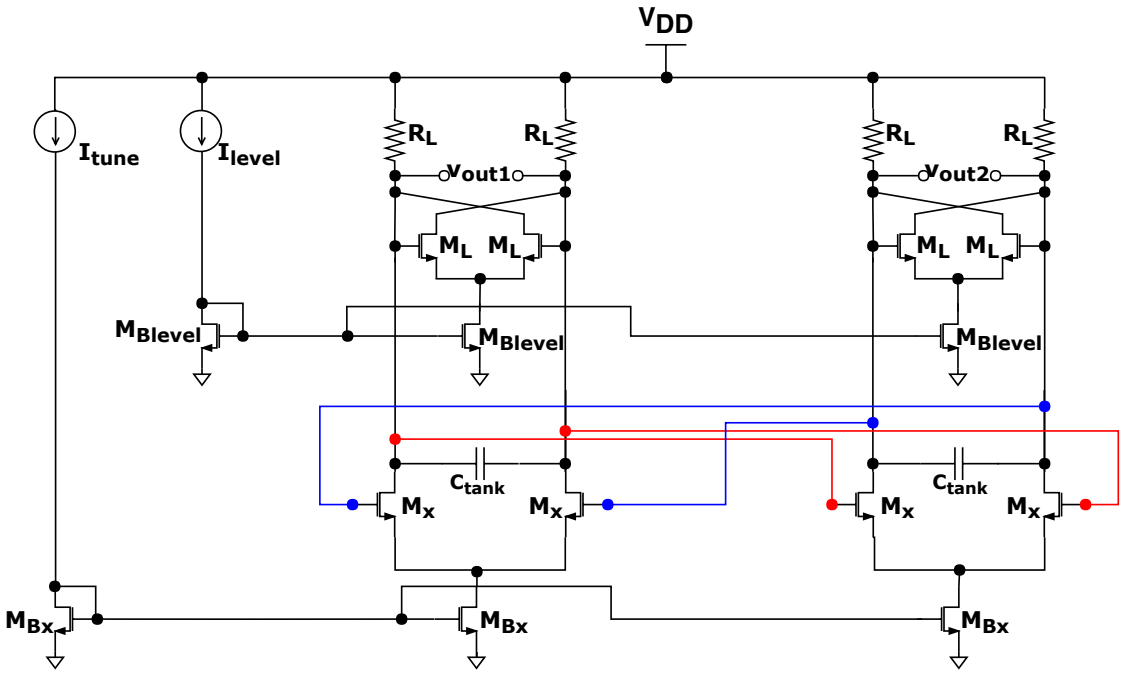

Figure 6.1: Free-running oscillator implementation.

The circuit shown in Fig. 6.1 is implemented with the aim of achieving low power consumption and a reduced area.

6.2.2 Injection-Locked Two-Integrator Oscillator

The proposed circuit for implementation of a fully integrated wideband ILO is shown in Fig. 6.2.

Observing the circuit of Fig. 6.2, it is seen that an injection block has been added, which is formed by the transistors M_I and M_{Binj} in conjunction with the RC network composed of R_{Filter} and $C_{decoupling}$. The injection block is biased with a voltage that is generated internally by the transistors in diode configuration, M_{Binj}. In addition, the ideal sinusoidal source v_{sync}, which represents the STO, is also part of the injection block.

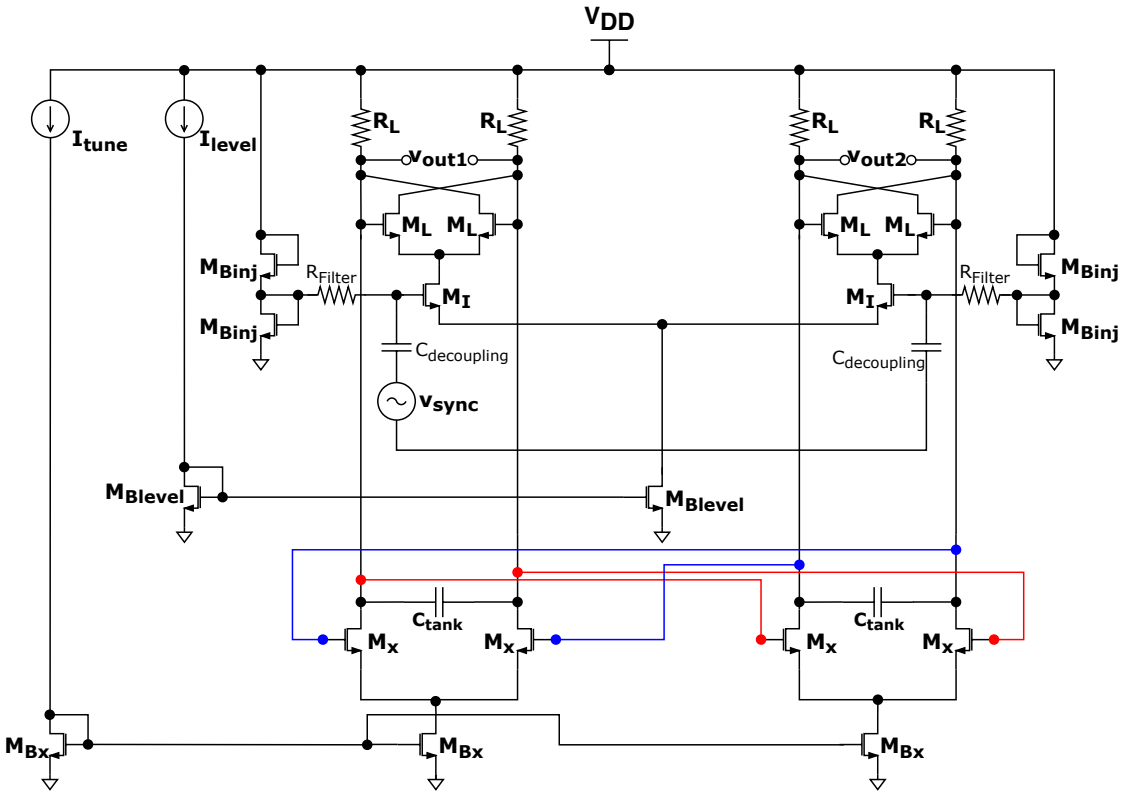

Figure 6.2: Two-integrator ILO.

The RC network, constituted by R_{Filter} and $C_{decoupling}$, behaves like an LPF that ensures that there is the largest possible transfer of AC power to the differential pair transistors M_I, allowing only the DC component of v_{sync} to pass to the node between the two biasing transistors M_{Binj}.

6.2.3 Injection Block

The injection interface is implemented by the differential pair of transistors M_I, which is driven by v_{sync}. Thus, for signal injection to occur, it is necessary to connect the drain of M_I to a node of the free-running oscillator. Considering the ILO represented in Fig. 6.2, the signal is injected into the common-source node of the cross-coupled differential pair, M_L, because of its special characteristics:

- Firstly, in this node there are only small voltage variations, which causes the modulation effects to be weak;
- Furthermore, since this node is not critical, the impact of parasitic effects is low;
- Ideally, this node contains only even order harmonics. Since the oscillator operates in quasi-linear mode, then its spectrum is expected to contain only one weak second order harmonic.

It is also true that the operating point of the circuit may remain unchanged with the introduction of this injection block. For this to happen, it suffices that the total current flowing through the common-source of the cross-coupled differential pair, M_L, remains constant, that is, by setting I_{level} of the ILO in such a way that I_D of its tansistor M_L is equal to I_D of the transistor M_L of the free-running ocillator.

An advantage of using an even order injection scheme such as this is that it uses only one differential pair, contrary to the odd-order injection block which requires two differential pairs in order for the charges of each stage of the oscillator to be balanced. Consequently, the second-order injection scheme has a lower consumption in terms of area and energy, being also less prone to quadrature errors due to mismatch [16].

One limitation of even-order injection is that it has a narrower locking range than an odd-order injection. However, it is possible to assume that increasing the gain of the injection block can overcome this disadvantage. In addition, since the free-running oscillator has a lower operating frequency than the injected signal, the even-order interface will help mitigate the impact of possible frequency drifts of the STO [16].

6.2.4 Reference Generator

As described in the introductory chapter, to generate the ILO reference signal, we considered an STO with characteristics similar to a frequency sensor developed at INL and presented in [17].

The device proposed in [17] has a variable resistance, which has a relative value that is determined by the frequency of the input signal. The great advantage of this spintronic-based frequency sensor is that it can detect a wide range of input signal frequencies with finite bandwidth.

The above-mentioned frequency sensor has three modes of operation:

- A mode of operation on High Frequency (HF)/Very High Frequency (VHF) bands based on sub-harmonic modulation, with the input signal having 1-10 MHz bandwidth around its resonant frequency and resolution in the order of hundreds of kHz. This operating region is known as modulation mode;

- Another operating region is the gyrotropic mode where the device operates in the VHF/Ultra High Frequency (UHF) bands and is based on direct gyrotropic excitation with an input signal having around 100 MHz bandwidth and 200 kHz of resolution;

- There is also the azimuthal mode, where the frequency sensor operates on UHF/Super High Frequency (SHF) and is based on indirect spin wave excitation with the input signal having around 1 GHz bandwidth and a resolution of a few MHz.

Considering the device proposed in [17], for each of the modes of operation described above, the variation of the resistance according to the frequency of the input signal is shown in Fig. 6.3.

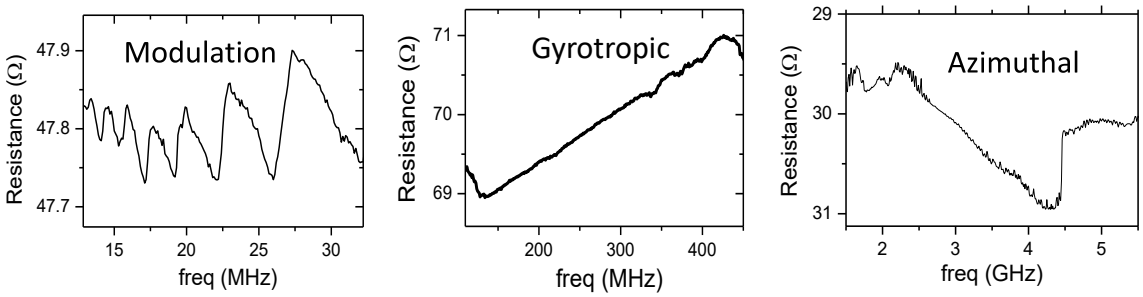

Figure 6.3: Operation modes of a spintronic-based frequency sensor developed at INL.

It is possible to summarize the characteristics of this spintronic-based frequency sensor in Tab. 6.1.

Table 6.1: Comparison of the operation modes of a spintronic-based frequency sensor developed at INL.

	Modulation mode	**Gyrotropic mode**	**Azimuthal mode**
Input signal frequency range	1-100 MHz	100-600 MHz	1-12 GHz
Input signal bandwidth	1-10 MHz	100-300 MHz	1-3 GHz
dR/df	40 Ω/kHz	7 Ω/kHz	0.7 Ω/kHz
Min Resolution	≈ 100 kHz	≈ 1 MHz	≈ 10 MHz
Measurement time	0.1-1 μs	1-10 ns	1-10 μs

In addition, it is important to note that this device is based on the same technology as an STO (spintronics and Magnetic Tunnel Junction), presenting power consumptions between 1 μW and 15 μW for oscillation frequencies in the range of [100 MHz - 600 MHz]. Therefore, it is a device with a very reduced output amplitude.

Given these characteristics, it has been considered reasonable to simulate the STO as a sinusoidal voltage source capable of generating a signal with a frequency range between 100 MHz and 600 MHz (gyrotropic mode) as well as between 1 GHz and 12 GHz (azimuthal mode).

6.2.5 Design Guidelines

To achieve the practical goal of this thesis, the starting point is the implementation of the free-running oscillator shown in Fig. 6.1. To implement this two-integrator oscillator, the following constraints must be taken into account:

- The transistors should operate in moderate to strong inversion, which means that their V_{Dsat} must at least be somewhere between 75 to 100 mV;

- The differential pairs must operate in the linear region, as indicated in Fig. 3.10;
- The output voltage, V_{OUT}, defined in Eq. (3.40), must not exceed $2V_{DSAT}$ of the transistors of the differential pairs. This condition ensures that M_L and M_x operate in the linear region;
- To ensure practical realization in integrated circuits, the resistors must meet the condition: $R_L \leq 10\ k\Omega$;
- In order to avoid a great sensitivity to parasitics, the capacitance of C_{tank} must at least have values in the order of 100 fF.

Thus, the free-running oscillator is implemented according to the following design methodology:

1. Firstly, the transistors of the differential pairs (M_x and M_L) are designed with small dimensions. Subsequently, these can be increased to obtain a correct biasing;
2. As for the transistors of the current mirrors, their channel length (L) is set at 180 nm. For the transistors of the differential pairs, the value is set at L = 360 nm, in order to avoid channel modulation effects in the two CMOS technologies in which the circuit is implemented;
3. Establish a fixed value for the resistor, $R_L = 600\ \Omega$, and size the channel width (W) of M_L in order to compensate circuit losses;
4. Set the capacitance value to $C_{tank} = 100$ fF. Subsequently this capacitor undergoes minor adjustments to guarantee the desired oscillation frequency;
5. The channel width of the transistor M_x is sized so that the circuit oscillates at a frequency of 100 MHz, with a tuning current I_{tune} in the order of the few tens of μA;
6. Increase the oscillation frequency by increasing I_{tune}. Thus, by observing the maximum value of I_{tune} that allows steady-state oscillations, the widest tuning range possible is obtained.

The next step is the ILO implementation, which follows the design methodology described below:

1. The injection block is added to the circuit;
2. The transistors M_I are sized with maximum width and L = 180 nm. Consequently, the W/L ratio of these transistors is maximized, which allows to increase the injected current and the locking range;

3. The transistors M_{Binj} are sized with L = 360 nm and a relatively small W in order to obtain reduced area and correct biasing of the injection block;

4. The RC network of the injection block introduces a pole $\omega_p \approx 1/(R_{Filter}C_{decoupling})$ in the node where it is applied. This means that the higher the values of R_{Filter} and $C_{decoupling}$, the closer this network is to an ideal LPF behavior. Consequently, the values are set to $R_{Filter} = 10\ k\Omega$ and $C_{decoupling} = 10$ pF, since values greater than this order are impractical in integrated circuits;

5. The signal of the current mirror M_{Blevel} is applied to the common-source of the differential pair M_I. Subsequently, the value of I_{level} is adjusted so that M_L has the same drain current, I_D, as the corresponding transistor in the free-running oscillator;

6. Finally, the v_{sync} signal is injected at twice the frequency of the free-running oscillator, with an amplitude starting at $10\mu V$ (-90 dBm in a 50 Ω system).

Following the methodologies described in this section, both circuits are implemented in two different CMOS technologies, using Cadence® SpectreRF and BSIM3v3 MOSFET models. Firstly, the implementation is done in 130 nm CMOS technology, with a supply voltage of 1.2 V. For this technology, the free-running oscillator dimensions are shown in Tab. 6.2.

Table 6.2: Free-running oscillator sizing on 130nm CMOS technology.

I_{tune}	I_{level}	R_L	M_L	M_{Blevel}	C_{tank}	M_x	M_{Bx}
[40μA – 1.11 mA]	300μA	600 Ω	$W = 10\mu m$ $L = 0.18\mu m$	$W = 90\mu m$ $L = 0.36\mu m$	102 fF	$W = 20\mu m$ $L = 0.18\mu m$	$W = 55\mu m$ $L = 0.36\mu m$

Many dimensions of the ILO are similar to those of the free-runnning oscillator, requiring only a few adjustments in the I_{tune} and I_{level} currents along with the design of the injection block. Thus, in the sizing of the ILO, only values that differ from the free-running oscillator are shown in Tab. 6.3.

Table 6.3: ILO sizing on 130nm CMOS technology.

I_{tune}	I_{level}	M_{Binj}	R_{Filter}	M_I	$C_{decoupling}$
[39.85μA – 1.16395 mA]	690μA	$W = 10\mu m$ $L = 0.36\mu m$	10 $k\Omega$	$W = 115.2\mu m$ $L = 0.18\mu m$	10 pF

Finally, repeating the same methods, both circuits are implemented in 180 nm CMOS technology, with a supply voltage of 1.8 V. Thus, the dimensions of the free-running oscillator, indicated in Tab. 6.4, and the sizing of the ILO, represented in Tab. 6.5, are obtained.

Table 6.4: Free-running oscillator sizing on 180 nm CMOS technology.

I_{tune}	I_{level}	R_L	M_L	M_{Blevel}	C_{tank}	M_x	M_{Bx}
[45.03μA – 1.9539 mA]	300μA	600 Ω	$W = 17\mu m$ $L = 0.18\mu m$	$W = 90\mu m$ $L = 0.36\mu m$	99 fF	$W = 17.3\mu m$ $L = 0.18\mu m$	$W = 55\mu m$ $L = 0.36\mu m$

Table 6.5: ILO sizing on 180nm CMOS technology.

I_{tune}	I_{level}	M_{Binj}	R_{Filter}	M_I	$C_{decoupling}$
[45.26μA – 1.8254 mA]	768μA	$W = 10\mu m$ $L = 0.36\mu m$	10 $k\Omega$	$W = 100\mu m$ $L = 0.18\mu m$	10 pF

6.3 Circuit Simulations

It is now necessary to confirm, at the practical level, the theoretical assumptions that motivated this work. Taking this into account, both the free-running oscillator and the ILO are simulated for the two technologies chosen for their implementation.

In both 130 nm and 180 nm CMOS technologies, circuit implementations undergo similar procedures to be simulated. Therefore, this section begins by presenting only the procedures used in the 130 nm CMOS technology. Subsequently, the results of the simulations in both technologies are presented in table form, to facilitate the comparison of circuit performances.

Firstly, after sizing the free-running oscillator, the variation of its operating frequency according to the range of its tuning current, indicated in Tab. 6.2, is observed. This results in a frequency band of f_{osc} = [100 MHz - 3 GHz], which also occurs in the 180 nm CMOS implementation for the range of I_{tune} indicated in Tab. 6.4. Once the tuning range is known, through transient simulation it is possible to see how the tuning current and the amplitude of the oscillator output voltage vary according to the frequency of operation, as shown in Fig. 6.4.

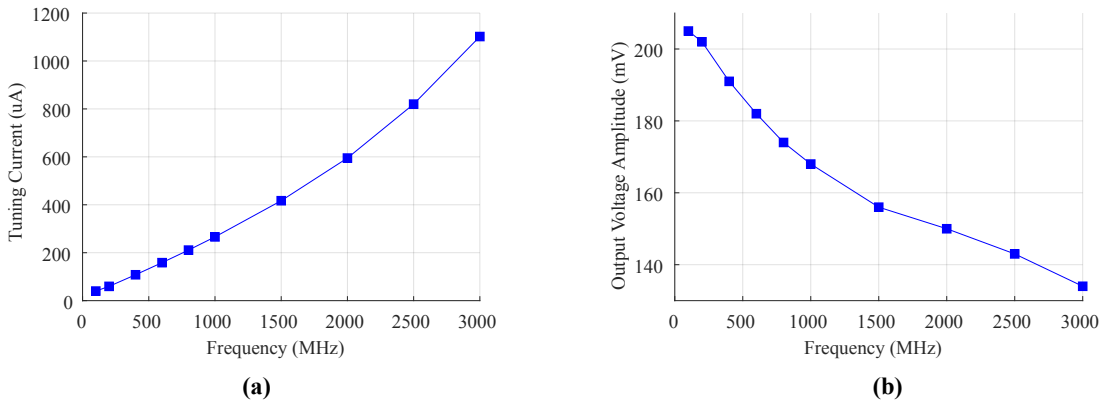

Figure 6.4: Voltage and current variation according to the frequency of the free-running oscillator implemented in 130 nm CMOS: (a) Tuning Current, (b) Output Voltage.

The free-running oscillator begins to oscillate at a frequency of 100 MHz, as can be confirmed by a transient simulation and is shown in Fig. 6.5, where one of its output voltages is in red and its frequency is in yellow.

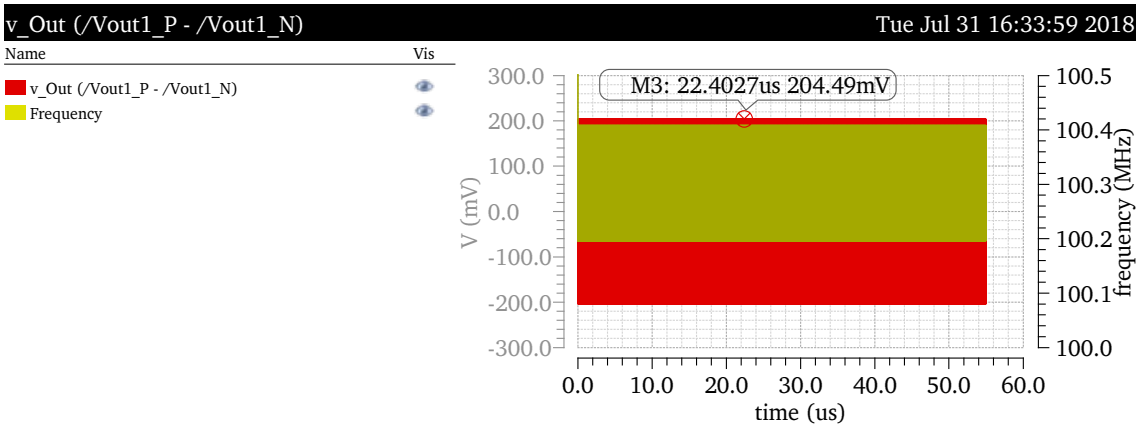

Figure 6.5: Free-running oscillator transient response in 130 nm CMOS technology: single output voltage at f_{osc} = 100 MHz.

In Fig. 6.5 it is observed that the free-running oscillator has an amplitude of approximately 205 mV while having $f_{osc} \approx 100$ MHz, although in fact it varies between 100.2 and 100.4 MHz.

In the case of the ILO, it is known that if there is a large difference between the free-running frequency and that of the STO, there will be no synchronization, resulting in a amplitude modulation of the output signal. On the contrary, if synchronization is successful, the ILO output signal will have a constant amplitude, as shown in Fig. 6.6. Taking this into account, the ILO is designed using super-harmonic synchronization, with the frequency of the STO output signal given by $f_{inj} = 2f_{osc}$.

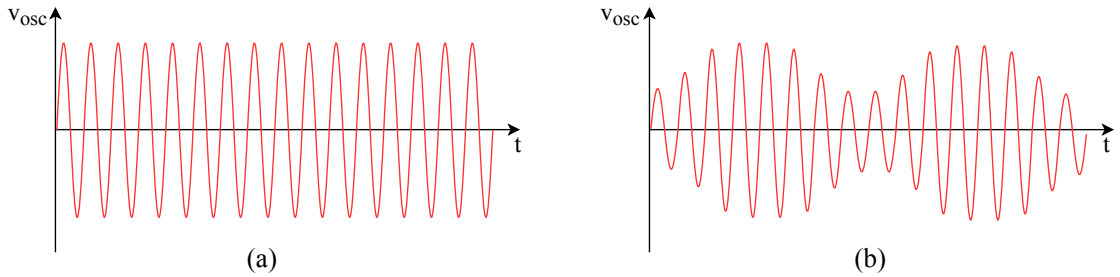

Figure 6.6: Output of the oscillator under injection: (a) Successful synchronization, (b) Failed synchronization (adapted from [16]).

The Periodic Steady-State (PSS) analysis is a simulation that determines the periodic operating point of the circuit, converging only if there is a beat frequency driving the circuit. Thus, the convergence of the PSS analysis indicates that the ILO synchronization was successful. When applying this simulation to the ILO, it is necessary to take into

account that this circuit is not considered by SpectreRF as being a pure oscillator due to the presence of an input source, v_{sync}. Therefore, it is necessary to parameterize the PSS analysis as indicated in Annex I, also knowing that its beat frequency must be given by the expected synchronization frequency. In addition, for the PSS to converge, a steady state must be guaranteed after the reference signal is injected, which implies setting the *tstab* parameter as being considerably larger than the oscillation period.

In Fig. 6.7, the spectral content of the ILO designed to have f_{osc} = 100 MHz is shown. This spectrum was obtained through a PSS analysis and, consequently, proves that there is synchronization at the desired frequency. In addition, this is a parametric analysis, where the amplitude of v_{sync} is varied to take the values {10 μV, 100 μV, 1 mV and 10 mV}, and it turns out that in any case synchronization is achieved.

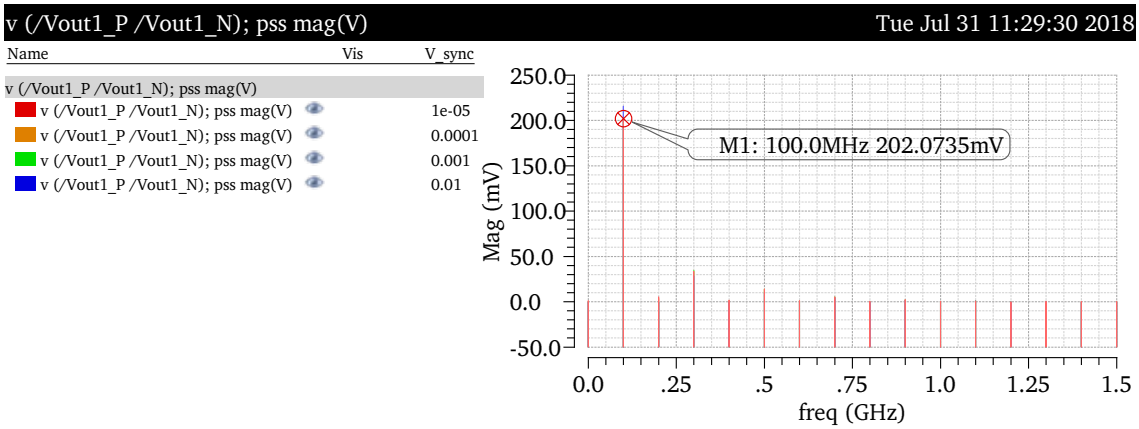

Figure 6.7: PSS analysis of the ILO in 130 nm CMOS technology: single output voltage at f_{osc} = 100 MHz.

In order to clarify the consequences of synchronization, a transient analysis of the ILO designed to operate at 100 MHz is performed, the results of which are shown in Fig. 6.8. This simulation is done using a parametric analysis, where v_{sync} is varied in the same way as shown in Fig. 6.7. In addition, it can be seen in Fig. 6.8 that the ILO obtains a higher frequency stability than the free-running oscillator when both circuits are designed to operate at 100 MHz. In fact, Fig. 6.5 shows that for any considered value of the reference signal amplitude, V_{sync}, the operating frequency has a very high accuracy being centered at f_{osc} = 100 MHz and with possible variations of less than 40 Hz.

The higher frequency stability obtained by the ILO in Fig. 6.8 is closely related to a better phase noise performance than that of the free-running oscillator. To confirm this relationship, a phase noise analysis of the free-running oscillator operating at 100 MHz is performed, as illustrated in Fig. 6.9, where it can be seen that the phase noise of the circuit at a 1 MHz offset frequency is approximately -82.62 dBc/Hz. Subsequently, a phase noise simulation of the ILO oscillating at 100 MHz is performed, as shown in Fig. 6.10, where it is verified by parametric analysis that increasing the amplitude of v_{sync} leads to further improvements in circuit performance. Taking, for example, the phase

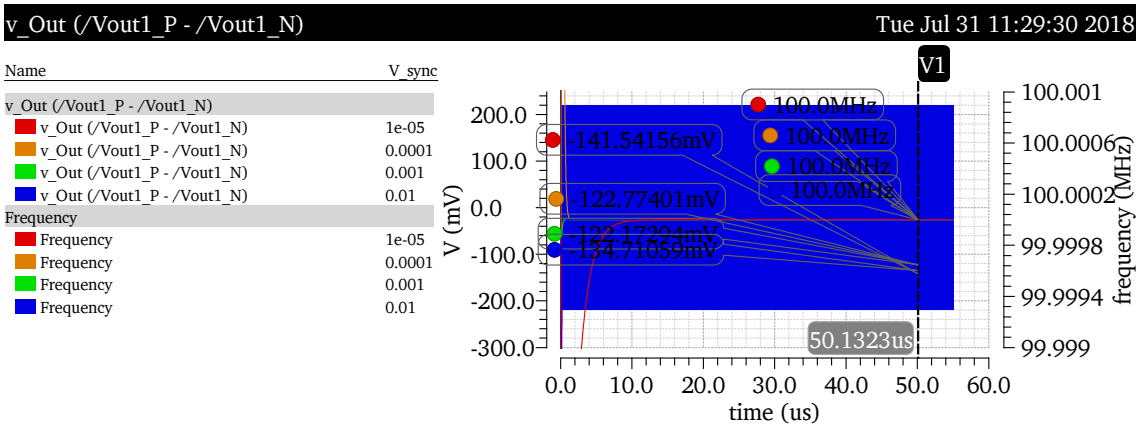

Figure 6.8: ILO transient response in 130 nm CMOS technology: single output voltage at f_{osc} = 100 MHz.

noise values at an offset of 1MHz, it can be seen in Fig. 6.10 that in order to have a phase noise improvement, it suffices that the STO signal has a power of -90 dBm, which leads to $\mathcal{L}(1MHz) \approx -87.99$ dBc/Hz.

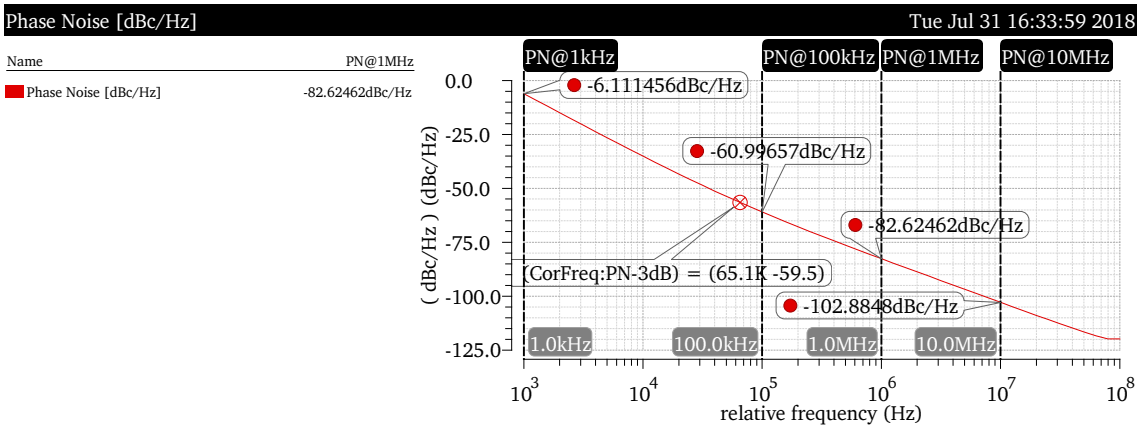

Figure 6.9: Free-running oscillator phase noise in 130 nm CMOS technology: single output voltage at f_{osc} = 100 MHz.

The same sequence of simulations described so far is applied to various operating points, with progressively higher frequencies. Thus, the transient analysis of the free-running oscillator operating at the upper limit of the tuning range (f_{osc} = 3 GHz) is shown in Fig. 6.11.

It is observed that the 130 nm implementation of the free-running oscillator operating at $f_{osc} \approx 3$ GHz, whose transient analysis is presented in Fig. 6.11, has an amplitude of approximately 134 mV (significantly lower than in the operation at 100 MHz shown in Fig. 6.5). In addition, it can be seen in Fig. 6.11 that in fact the free-running oscillator operates with a frequency around 3.001 GHz, which represents a 1 MHz offset from the desired value for f_{osc}.

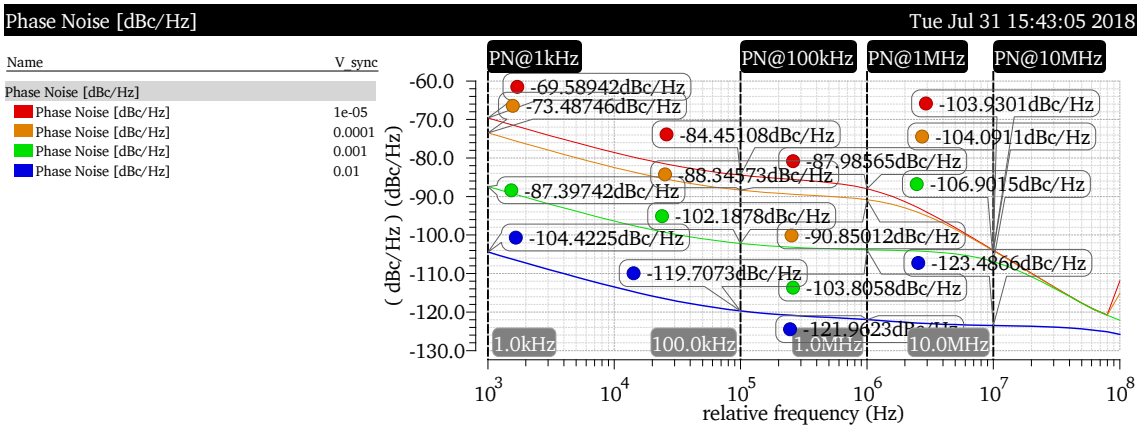

Figure 6.10: ILO phase noise in 130 nm CMOS technology: single output voltage at f_{osc} = 100 MHz.

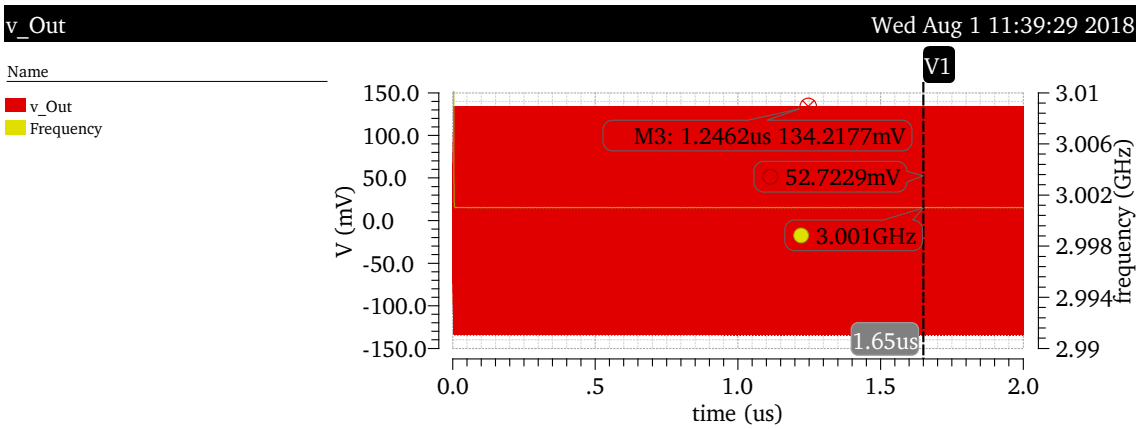

Figure 6.11: Free-running oscillator transient response in 130 nm CMOS technology: single output voltage at f_{osc} = 3 GHz.

Through a PSS analysis, it is confirmed that the ILO achieves synchronization at 3 GHz, as depicted in Fig. 6.12.

The synchronization of the ILO has an impact on the transient regime, resulting in greater accuracy and stability of the operating frequency, as shown in Fig. 6.13. In fact, for $V_{sync} = 10\mu V$, it is observed that the oscillation frequency is about 110 kHz above the desired value of 3 GHz, which represents a much smaller deviation than the difference of 1 MHz shown in Fig. 6.11. Increasing the value of V_{sync} leads to a reduction in the difference between f_{osc} and the desired oscillation frequency of 3 GHz. As proof of this, when V_{sync} = 10 mV the ILO oscillates precisely at 3GHz. In addition, it can be seen in Fig. 6.13 that the amplitude of the output signal of the ILO is approximately 160 mV. This represents a reduction in output amplitude when comparing the two operating points with f_{osc} = 100 MHz and f_{osc} = 3 GHz, demonstrating that the ILO presents, like the free-running oscillator, an inverse proportionality between the operating frequency and

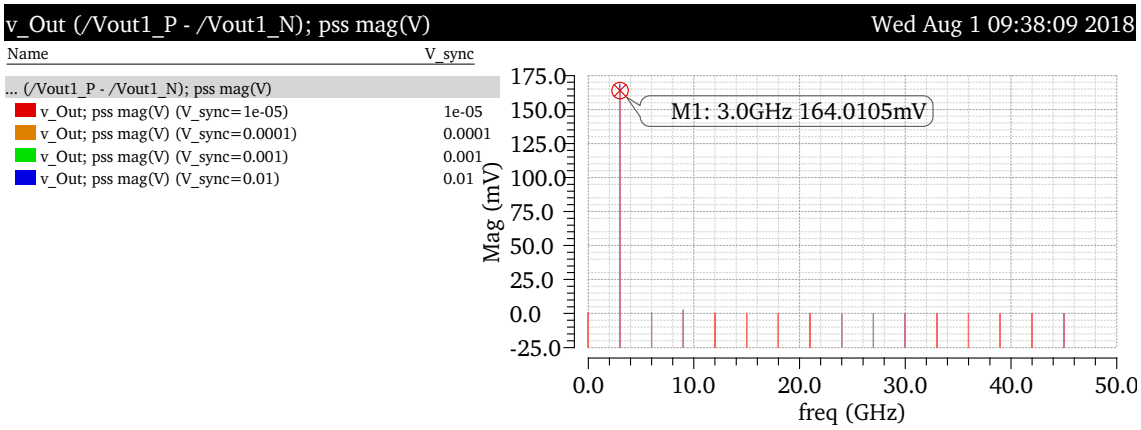

Figure 6.12: PSS analysis of the ILO in 130 nm CMOS technology: single output voltage at f_{osc} = 3 GHz.

the output amplitude.

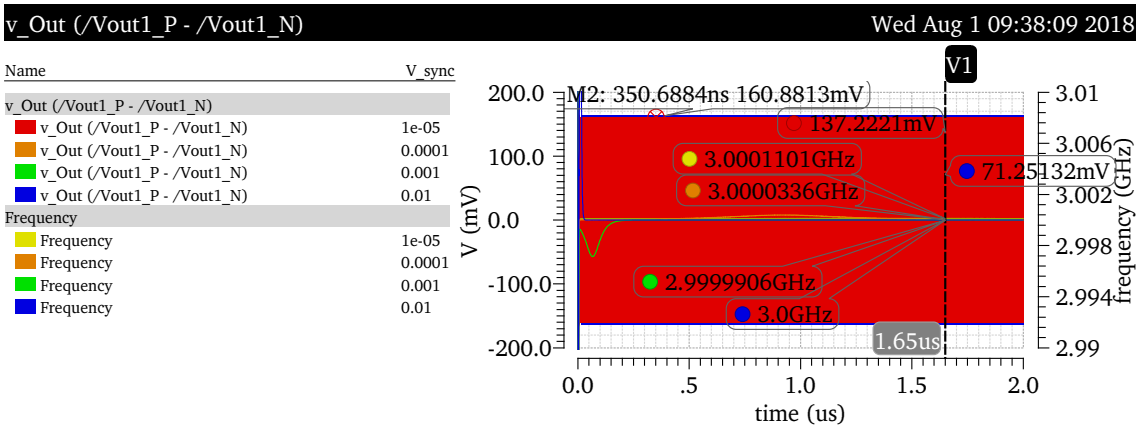

Figure 6.13: ILO transient response in 130 nm CMOS technology: single output voltage at f_{osc} = 3 GHz.

Afterwards, the performance of both circuits is evaluated. Firstly, the phase noise of the free-running oscillator is analyzed, as shown in Fig. 6.14.

It can be seen in Fig. 6.14 that the free-running oscillator, operating at f_{osc} = 3 GHz, presents a phase noise at a 1 MHz offset frequency of $\mathcal{L}(1MHz)$ = -80.39 dBc/Hz.

Subsequently, it is confirmed that the synchronization of the ILO leads to improved values of phase noise, as depicted in Fig. 6.15.

Considering the ILO operating at 3 GHz, its phase noise values at an offset of 1 MHz, presented in Fig. 6.10, show that a significant performance improvement can be achieved if the power of the injected signal is only -90 dBm, leading to $\mathcal{L}(1MHz) \approx$ -100.94 dBc/Hz.

Analyzing Figs. 6.10 and 6.15, which show the phase noise of the ILO, it is confirmed that the circuit performance is directly proportional to the amplitude of v_{sync}. In order to clarify this relationship, the phase noise of the ILO at a frequency offset of 1 MHz is

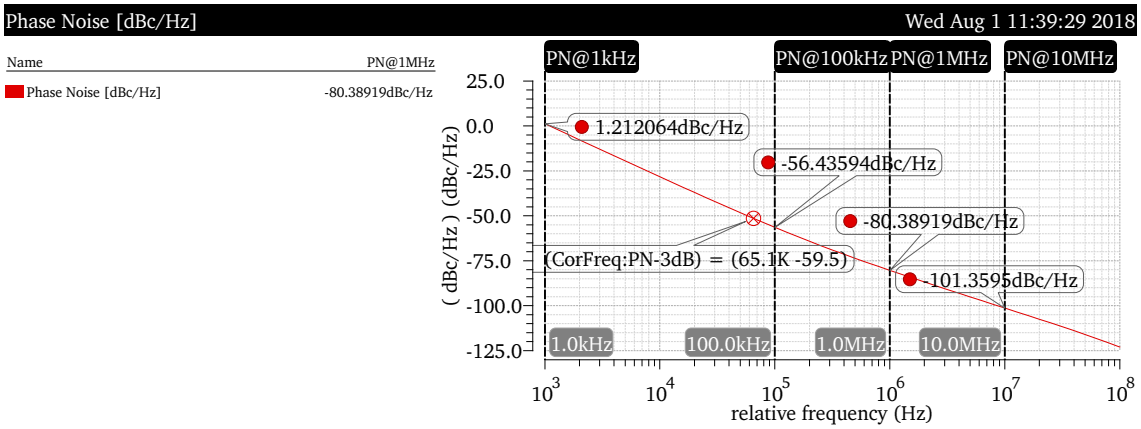

Figure 6.14: Free-running oscillator phase noise in 130 nm CMOS technology: single output voltage at f_{osc} = 3 GHz.

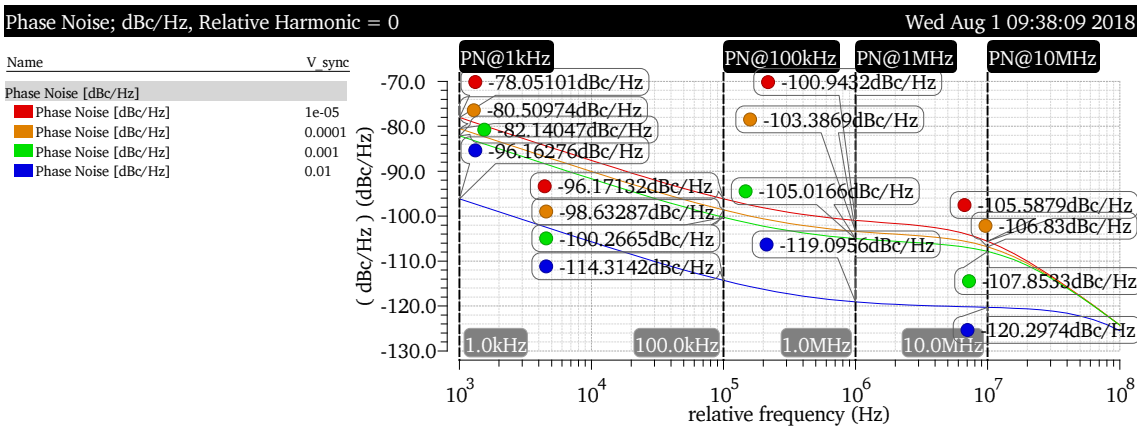

Figure 6.15: ILO phase noise in 130 nm CMOS technology: single output voltage at f_{osc} = 3 GHz.

analyzed for the various amplitudes of v_{sync} within the following set of values: {10 μV, 100 μV, 1 mV, 10 mV}. Repeating this analysis for several ILO operating frequencies results in Fig. 6.16, where the considered values for f_{osc} were: 100 MHz, 600 MHz, 1 GHz, 2 GHz and 3 GHz.

Although only images related to implementation in 130 nm CMOS technology have been presented, it is important to note that the entire process described so far in this section is repeated and applied to the implementations of the circuits in 180 nm CMOS technology. In both technologies, similar behaviors are observed regarding phase noise and tuning range. Taking this into account, the phase noise results for the free-running oscillator and ILO implementations at various operating frequencies are presented in Tab. 6.6.

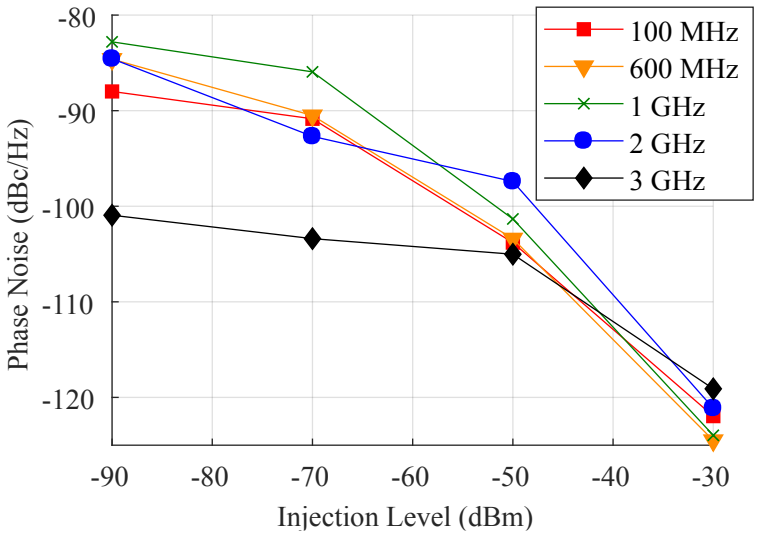

Figure 6.16: $\mathcal{L}(1MHz)$ vs Injection Level for the ILO in 130 nm CMOS.

Table 6.6: Phase noise at 1 MHz offset frequency: Comparison between free-running oscillator and ILO.

	Free-running oscillator	ILO with $V_{sync} = 10\mu V$	ILO with $V_{sync} = 100\mu V$	ILO with $V_{sync} = 1$ mV	ILO with $V_{sync} = 10$ mV
f_{osc} = 100MHz, tech: UMC 130 nm	-82.62 dBc/Hz	-87.99 dBc/Hz	-90.85 dBc/Hz	-103.81 dBc/Hz	-121.96 dBc/Hz
f_{osc} = 100MHz, tech: UMC 180 nm	-80.97 dBc/Hz	-82.90 dBc/Hz	-92.42 dBc/Hz	-102.53 dBc/Hz	-121.14 dBc/Hz
f_{osc} = 600MHz, tech: UMC 130 nm	-83.57 dBc/Hz	-84.61 dBc/Hz	-90.51 dBc/Hz	-103.40 dBc/Hz	-124.50 dBc/Hz
f_{osc} = 600MHz, tech: UMC 180 nm	-85.30 dBc/Hz	-89.69 dBc/Hz	-91.91 dBc/Hz	-101.56 dBc/Hz	-122.59 dBc/Hz
f_{osc} = 1GHz, tech: UMC 130 nm	-81.65 dBc/Hz	-82.80 dBc/Hz	-85.94 dBc/Hz	-101.33 dBc/Hz	-123.97 dBc/Hz
f_{osc} = 1GHz, tech: UMC 180 nm	-82.02 dBc/Hz	-90.86 dBc/Hz	-95.89 dBc/Hz	-100.20 dBc/Hz	-120.79 dBc/Hz
f_{osc} = 2GHz, tech: UMC 130 nm	-80.14 dBc/Hz	-84.57 dBc/Hz	-92.69 dBc/Hz	-97.41 dBc/Hz	-121.13 dBc/Hz
f_{osc} = 2GHz, tech: UMC 180 nm	-76.59 dBc/Hz	-102.63 dBc/Hz	-102.80 dBc/Hz	-105.08 dBc/Hz	-112.24 dBc/Hz
f_{osc} = 3GHz, tech: UMC 130 nm	-80.36 dBc/Hz	-100.94 dBc/Hz	-103.39 dBc/Hz	-105.02 dBc/Hz	-119.10 dBc/Hz
f_{osc} = 3GHz, tech: UMC 180 nm	-78.28 dBc/Hz	-104.28 dBc/Hz	-104.40 dBc/Hz	-106.69 dBc/Hz	-113.72 dBc/Hz

In order to get a clearer view of oscillator performance, the FoM defined in Eq. (3.41) is used. Consequently, using the FoM, Tab. 6.7 presents a comparison between the performances of the free-running oscillator and the ILO in both 130 nm and 180 nm CMOS technologies.

Table 6.7: FoM comparison between the free-running oscillator and the ILO.

	P_{DC} free-running oscillator	P_{DC} ILO	FoM for free-running oscillator	FoM for ILO with $V_{sync} = 10\mu V$	FoM for ILO with $V_{sync} = 100\mu V$	FoM for ILO with V_{sync} = 1 mV	FoM for ILO with V_{sync} = 10 mV
f_{osc} = 100MHz, tech: UMC 130 nm	1.30 mW	2.94 mW	-121.48 dBc/Hz	-123.30 dBc/Hz	-126.16 dBc/Hz	-139.12 dBc/Hz	-157.27 dBc/Hz
f_{osc} = 100MHz, tech: UMC 180 nm	2.10 mW	4.857 mW	-117.74 dBc/Hz	-116.03 dBc/Hz	-125.55 dBc/Hz	-135.66 dBc/Hz	-154.27 dBc/Hz
f_{osc} = 600MHz, tech: UMC 130 nm	1.75 mW	3.40 mW	-136.70 dBc/Hz	-134.85 dBc/Hz	-140.75 dBc/Hz	-153.64 dBc/Hz	-174.74 dBc/Hz
f_{osc} = 600MHz, tech: UMC 180 nm	2.82 mW	5.595 mW	-136.36 dBc/Hz	-137.77 dBc/Hz	-139.99 dBc/Hz	-149.64 dBc/Hz	-170.67 dBc/Hz
f_{osc} = 1GHz, tech: UMC 130 nm	2.14 mW	3.81 mW	-138.34 dBc/Hz	-136.99 dBc/Hz	-140.13 dBc/Hz	-155.52 dBc/Hz	-178.16 dBc/Hz
f_{osc} = 1GHz, tech: UMC 180 nm	3.60 mW	6.341 mW	-136.45 dBc/Hz	-142.83 dBc/Hz	-147.86 dBc/Hz	-152.17 dBc/Hz	-172.76 dBc/Hz
f_{osc} = 2GHz, tech: UMC 130 nm	3.29 mW	5.04 mW	-140.98 dBc/Hz	-143.56 dBc/Hz	-151.68 dBc/Hz	-156.40 dBc/Hz	-180.12 dBc/Hz
f_{osc} = 2GHz, tech: UMC 180 nm	6.09 mW	8.874 mW	-134.76 dBc/Hz	-159.16 dBc/Hz	-159.33 dBc/Hz	-161.61 dBc/Hz	-168.77 dBc/Hz
f_{osc} = 3GHz, tech: UMC 130 nm	4.94 mW	6.81 mW	-142.96 dBc/Hz	-162.15 dBc/Hz	-164.60 dBc/Hz	-166.23 dBc/Hz	-180.31 dBc/Hz
f_{osc} = 3GHz, tech: UMC 180 nm	11.64 mW	13.962 mW	-137.16 dBc/Hz	-162.37 dBc/Hz	-162.49 dBc/Hz	-164.78 dBc/Hz	-171.81 dBc/Hz

6.4 Discussion

In order to experimentally validate the injection locking in a two-integrator oscillator, two CMOS technologies were used: UMC 130 nm and UMC 180 nm. The resulting ILO reference signal was always injected at twice the free-running oscillation frequency. The results of the simulations demonstrate that phase noise correction is obtained with a reference power starting with values as low as -90 dBm. The phase noise improvement is achieved across the entire frequency band [100 MHz - 3 GHz], which represents a tuning range of 187.1% and implies that the circuit being studied is a wideband oscillator covering the whole GSM (2G) frequency band and multiple UMTS (3G) and LTE (4G) frequencies.

Since the ILO topology has inherent I/Q outputs, meeting all the objectives proposed at the beginning of this chapter depends only on the goal of $\mathcal{L}(1MHz) < -100$ dBc/Hz to be achieved. In Tab. 6.6 it is observed that:

- When the reference power is -90 dBm or -70 dBm, $\mathcal{L}(1MHz) < -100$ dBc/Hz is only achieved for the implementation in UMC 180 nm with $f_{osc} \geq 2$ GHz and the ILO in UMC 130 nm with $f_{osc} = 3$ GHz;
- When the reference power is -50 dBm, the goal of $\mathcal{L}(1MHz) < -100$ dBc/Hz is met in practically the entire frequency band, with the exception of the implementation in UMC 130 nm with $f_{osc} = 2$ GHz;
- When the reference power is -30 dBm, the target of $\mathcal{L}(1MHz) < -100$ dBc/Hz is fulfilled in both CMOS technologies by a large margin across the entire band.

It should also be noted in Tab. 6.6 that, considering $V_{sync} = 10\ \mu V$, the phase noise of the ILO shows a more significant improvement for $f_{osc} = 3$ GHz than for $f_{osc} = 100$ MHz.

This is because, at the maximum oscillation frequency, the output signal has a significantly lower amplitude than in the case where the oscillator operates at 100 MHz, directly affecting the injection strength $\frac{V_{sync}}{V_{out}}$.

As for the two-integrator ILO performance values, described by the FoM and presented in Tab. 6.7, it would be expected that the ILO FoM would be higher than the free-running oscillator in all scenarios. However, there are three cases where, for a reference power of -90 dBm, the ILO FoM is lower than the free-running oscillator, namely:

- Regarding the implementation in UMC 130 nm:

  When f_{osc} = 600 MHz;

  When f_{osc} = 1 GHz.

- Regarding the implementation in UMC 180 nm:

  When f_{osc} = 100 MHz.

In these three cases, because the oscillator is under a very weak injection, the phase noise improvement is not enough to compensate for the increase in power that is required for the implementation of the ILO.

Considering $V_{sync} \geq 100\ \mu V$ (reference power ≥ -90 dBm) and f_{osc} = 3 GHz, the proposed ILO has a FoM that is competitive with the state-of-the-art CMOS RC oscillators presented in Tab. 3.2. In fact, if the reference signal is -30 dBm (only 10 dBm above the maximum value of most MTJ STOs) and considering f_{osc} = 3 GHz, the ILO presented in this thesis has a higher FoM than any state-of-the-art RC oscillator shown in Tab. 3.2. In addition, the 187.1% tuning range is the largest among the state-of-the-art CMOS oscillators presented in this thesis, evidencing the ability of this ILO to cover multiple communication standards.

Chapter 7

Conclusions and Future Work

7.1 Conclusions

RC oscillators have several advantageous characteristics, including their low area and cost, high tuning ranges and capability to be fully integrated. Therefore, over the past few years there has been a widespread interest in developing mechanisms that improve the performance of RC oscillators by correcting their poor phase noise levels. The injection locking was presented and discussed as a way to improve the performance of an RC oscillator with high frequency of operation, leading to the resulting circuit to be known as an ILO. The use of the injection locking, instead of the typical approach of using a PLL structure, allows to achieve the desired phase noise improvement and a performance comparable to that of a PLL without causing such a large impact on total cost, area, power consumption and circuit complexity.

Choosing the reference generator is one of the key factors in the design of an ILO. In chapter 5 the two possible options for reference generators were presented and discussed: crystal oscillator and STO. Although the crystal oscillator has the highest Q factors, this characteristic causes its tuning range to be reduced, adding this disadvantage to having a maximum frequency limited to the MHz band. It was therefore concluded that the STO would be the best option for reference generator because it has higher operating frequencies (in the order of GHz), high tuning ranges and compatibility with the CMOS process, which allows the implementation of a fully integrated wideband ILO capable of covering multiple communication standards.

The possibility of improving the phase noise of an RC oscillator through injection locking has been validated by simulations. An ILO was first implemented in UMC 130 nm technology due to its low cost. Afterwards, the proposed circuit was implemented in UMC 180 nm, since the STO considered in this work was implemented in a technology

compatible with the 180 nm CMOS process. The proposed ILO was based on a two-integrator oscillator to which was added a second-order injection scheme that allows to avoid unwanted modulation effects. However, since a second-order injection has a weaker impact than injecting the reference signal at the fundamental frequency, the injection block had to be designed with maximum gain. The results of the simulations showed that, compared to the free-running oscillator, a reference power of -90 dBm was sufficient for the proposed ILO to present phase noise correction throughout its wide frequency range ([100 MHz - 3 GHz]).

It was observed that with a reference power of -50 dBm, the ILO already had phase noise and FoM values comparable to several state-of-the-art CMOS RC oscillators presented in chapter 3, especially for oscillation frequencies in the order of GHz. In addition, it was also observed that a reference power of -30 dBm led to the ILO having phase noise and FoM values among the best state-of-the-art RC oscillators. Typical MTJ STOs have output power in the range of -60 dBm to -40 dBm. Thus, the proposed circuit served as proof of concept for the implementation of a wideband ILO that uses a reference generator implemented by a MTJ STO with characteristics similar to the frequency sensor proposed in [17], as described in the introductory chapter.

7.2 Future Work

As a way of complementing what has been achieved in this thesis, the following suggestions for future work can be followed:

- The 180 nm CMOS implementation of the ILO proposed in this thesis was based on the design of the circuit developed in 130 nm CMOS, for ease of implementation. By minimizing the power consumption of the 180 nm CMOS implementation, it is expected that the circuit will have better FoM results;
- Another possible way to improve circuit performance would be to design it so that it has a lower output voltage. Theoretically, this will make the injection strength greater for the reference power values practiced in this ILO. Following this line of research, there may even be room for significant improvements in phase noise with a reference power $\leq$ -40 dBm;
- Implement the ILO in the specific 180 nm CMOS technology that is compatible with the STO process. Perform the layout and fabricate a fully integrated wideband ILO prototype.

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ANNEX I

PROCEDURES TO ENSURE CONVERGENCE OF THE PSS ANALYSIS OF AN INJECTION-LOCKED OSCILLATOR IN SPECTRERF

SpectreRF does not consider an Injection-Locked Oscillator (ILO) to be a pure oscillator circuit due to the presence of an input source to inject the reference signal. Therefore, to confirm the synchronization of the ILO and to study its phase noise characteristic, it is necessary to adjust some parameters of the simulator and configure the PSS analysis in order to achieve convergence.

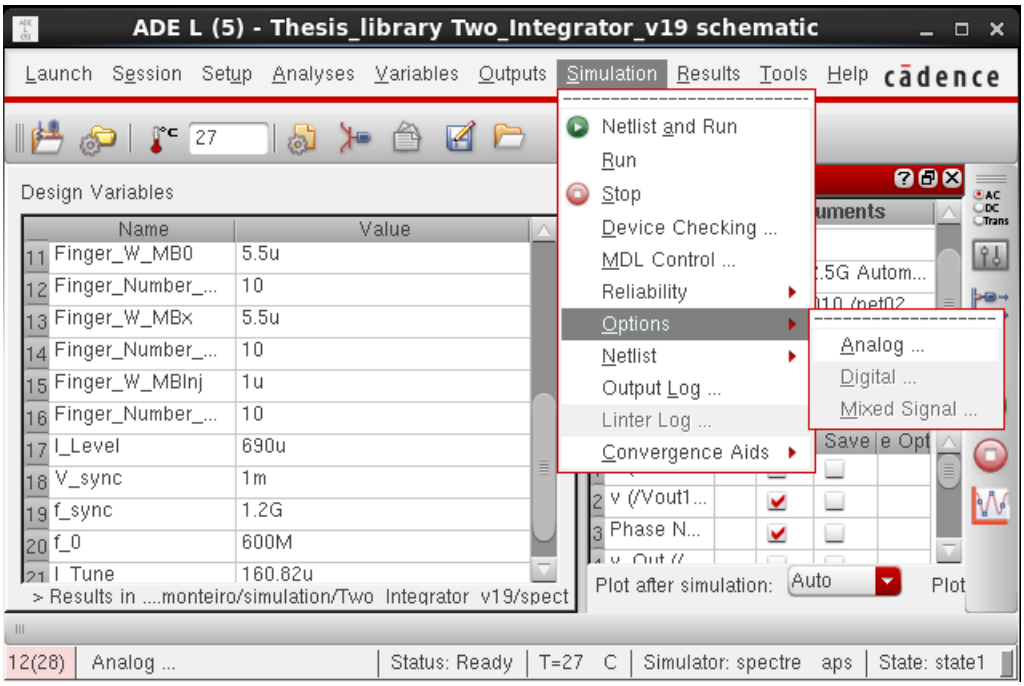
In practical terms, the procedures described in this annex were applied to an ILO based on a two-integrator oscillator. However, these procedures can be applied to a generic ILO or other type of oscillator that is having convergence problems in the PSS analysis.

The entire process described in this annex is based on the information contained in the application note entitled *Oscillator Noise Analysis in SpectreRF*, which is made available online by Carleton University, as described by the reference [56].

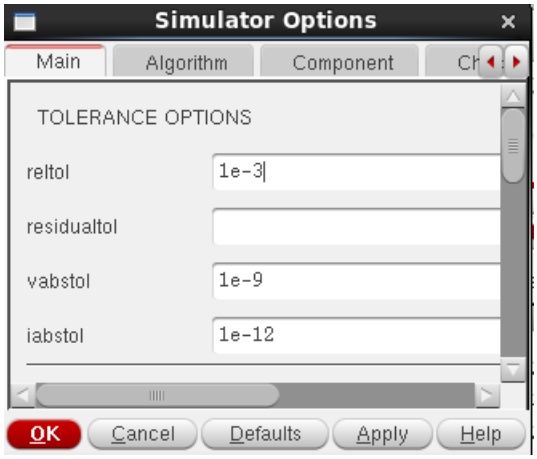
For a correct configuration of the PSS analysis, it will be necessary to relax its **steadyratio** parameter. To compensate for this relaxation, the tolerances of the simulator must be tightened. In ADE L, the simulator options can be accessed by selecting tab '**Simulation** -> **Options** -> **Analog ...**', as shown in Fig. I.1(a).

Since the considered ILO works with a reference signal having voltages beginning on the order of μV, the tolerance **vabstol** is set to the value of 1 nV, as shown in Fig. I.1(b), instead of the default value that would be **vabstol** = $1\mu V$.

Regarding the PSS analysis, most circuits can achieve convergence by manipulating the parameters **tstab** and **steadyratio**. Thus, **tstab** must be large enough for the oscillation amplitude to reach a value close to its steady-state level as well as for most other



(a)



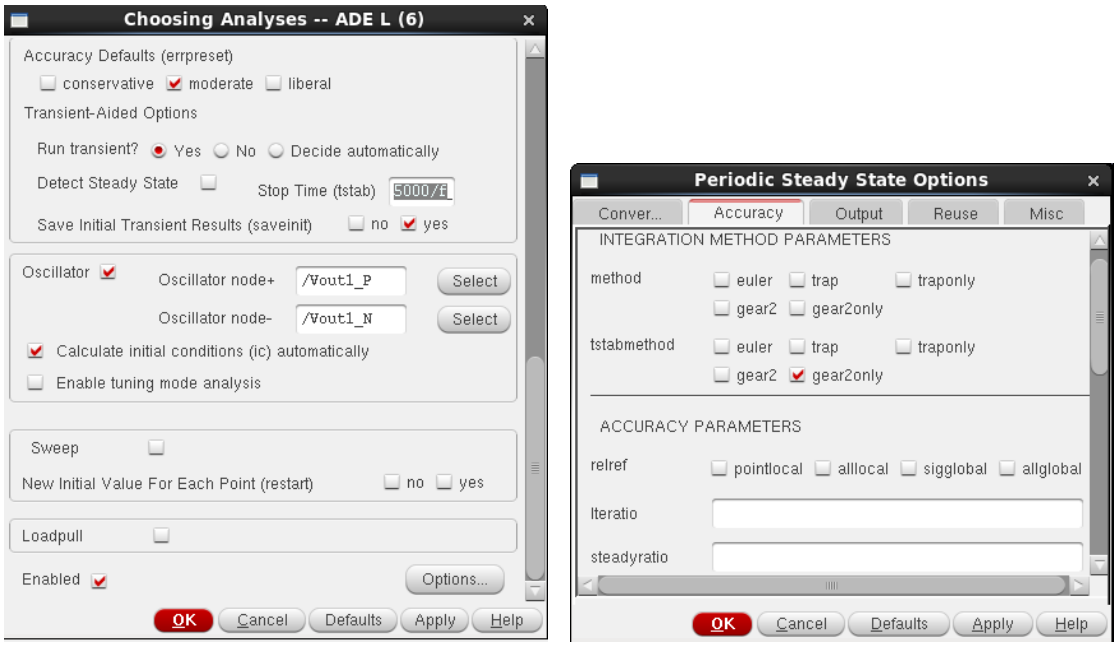
(b)

Figure I.1: Changing simulator tolerances in SpectreRF: (a) Access to the simulator options, (b) Changing tolerance options.

transients to have died out [56]. In practical terms, the integration method chosen for the PSS analysis was **gear2only**, which is usually recommended [56].

In the practical case considered, the free-running oscillator (a two-integrator oscillator) was first analyzed for later comparison with the ILO. Thus, the PSS configuration was made using the oscillation frequency, f_{osc} as the beat frequency, selecting the accuracy defaults as **moderate** and the parameter **tstab**= $5000/f_{osc}$ so that the analysis is performed under conditions similar to those of the ILO. In addition, the box 'Oscillator'was selected,

the circuit outputs were indicated and it was asked to 'calculate initial conditions automatically', as shown in Fig. I.2(a). By selecting 'Options...', the **Accuracy** tab could be chosen, where **tstabmethod** was selected as **gear2only**, as depicted in Fig. I.2(b).



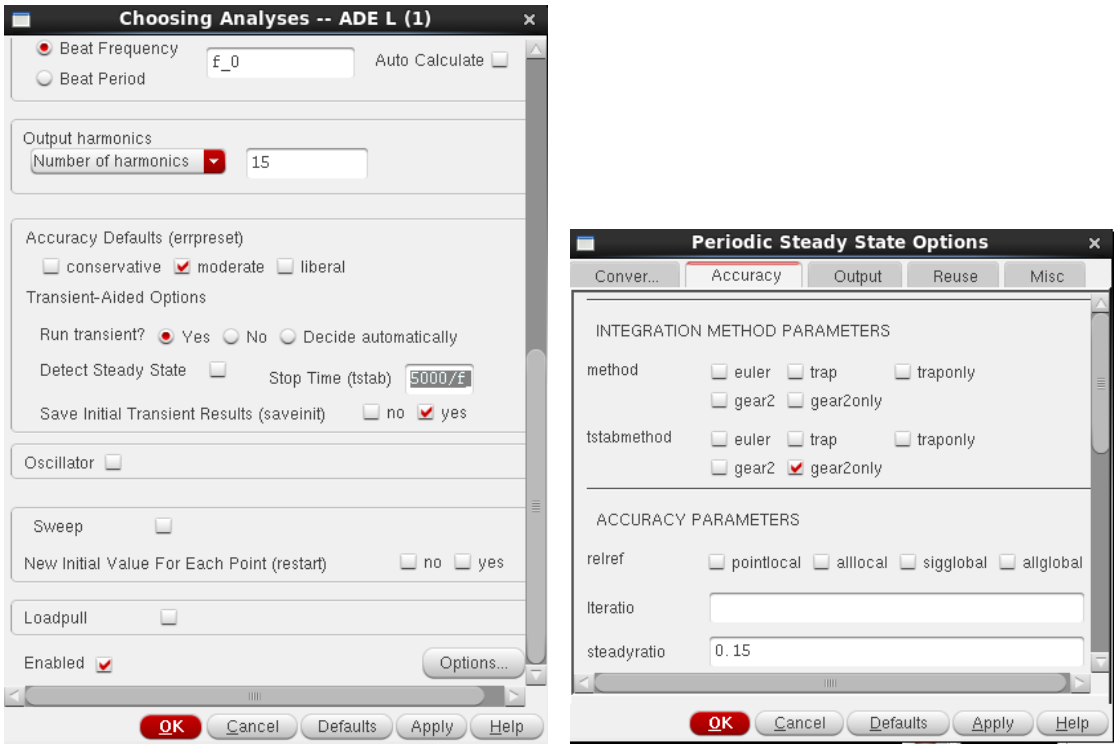
(a) (b)

Figure I.2: Configuring the PSS analysis of the free-running oscillator operating at f_{osc} = 3 GHz: (a) Basic configuration (b) Changing accuracy options.

As for the ILO, when configuring its PSS analysis, the box must be left unchecked, since the presence of an independent input source to inject the reference signal makes it impossible for SpectreRF to consider that the circuit is a pure oscillator. In addition, to let all transients associated with the injection of the reference signal die out, the parameter **tstab** must be set as much larger than the oscillation period, T_{osc}. In practical terms, it was defined that **tstab**= $5000T_{osc}$ and **moderate** accuracy defaults were chosen, as can be seen in Fig. I.3(a).

Considering in this example that the ILO operates at f_{osc} = 600 MHz, by selecting 'Options...', the **Accuracy** tab could be chosen, where **tstabmethod** was selected as **gear2only** and the **steadyratio** was set to 0.15, as depicted in Fig. I.3(b). In general terms, it is often necessary to define the **steadyratio** parameter with a value between 0.1 and 1 so that the circuit reaches convergence in its PSS analysis, which means that any value less than 1 should be acceptable [56].

The purpose of the comparative study between the ILO and the free-running oscillator considered in the practical example was to analyze its phase noise characteristic along its frequency band. For this, it was necessary to perform a PSS analysis at several operating points of both circuits, with f_{osc} taking several values scattered throughout the oscillation



(a) (b)

Figure I.3: Configuring the PSS analysis of the ILO operating at f_{osc} = 600 MHz: (a) Basic configuration (b) Changing accuracy options.

frequency range of the circuit [100 MHz - 3GHz].

The lower the value of the **steadyratio** parameter, the greater the accuracy of the PSS analysis. Therefore, in the study of the free-running oscillator, the default value of **steadyratio** was always used in all the operating points considered for the PSS analysis, since this circuit did not present problems of convergence and the default value of **steadyratio** is significantly less than 0.1.

Regarding the ILO, the circuit was implemented in two different CMOS technologies: 130 nm and 180 nm. For each technology, several operating points were analyzed in which f_{osc} took the following values: {100 MHz, 600 MHz, 1 GHz, 2 GHz and 3 GHz}. At each operating point considered, the value of the **steadyratio** parameter of the PSS analysis was chosen according to an iterative process, in which the objective was to find the lowest value of **steadyratio** for which the PSS analysis of the ILO would converge. As a result, the **steadyratio** values shown in Tab. I.1 were obtained.

Table I.1: Values of the **steadyratio** parameter of the PSS analysis at several operating points of the ILO.

	tech: CMOS 130 nm	tech: CMOS 180 nm
f_{osc} = 100 MHz	steadyratio = 0.28	steadyratio = 0.4
f_{osc} = 600 MHz	steadyratio = 0.15	steadyratio = 0.15
f_{osc} = 1 GHz	steadyratio = 0.15	steadyratio = 0.13
f_{osc} = 2 GHz	steadyratio = 0.14	steadyratio = 0.25
f_{osc} = 3 GHz	steadyratio = 0.19	steadyratio = 0.25