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Design of a Limiting Amplifier for an Optical Receiver

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To Joaquim and António

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Abstract

The HEP experiments that take place at CERN's LHC demand a multi-gigabit optical link for an efficient transmission of the resulting generated data. An optoelectronic link arises as the best solution given its possibility of working at high data rates and due to fiber's imunnity to electromagnetic noise. The design of this optical link is particularly demanding due to the stringent data rate specifications (5Gb/s), the BER specification ($10^{-}12$) and the constraints imposed by radiation. In HEP, radiation is always a constraint so, the Optical Receiver circuit must be hardened in order to tolerate that kind of environment - radiation-tolerant.

The core of a standard optoeletronic receiver includes a Photodiode, a Transimpedance Amplifier (TIA) and a Limiting Amplifier (LA). This thesis proposes the study and implementation of one of these blocks (LA), as the main focus, as well as the analysis and design of all three other blocks.

The two major design constraints regarding the LA are the bandwidth and minimising its power consumption, which were overcome by using two bandwidth enhancement techniques. The circuit yields a bandwidth of 4.8 GHz with a power consumption under 19 mW.

Another fundamental block is the Output Buffer. The major request for this block was maintaining relatively low transition times and improving the signal's integrity. It has a differential output swing around 400 mV with Pre-emphasis levels larger than 130%.

The third block is the Received Signal Strength Indicator (RSSI). From a system point of view it is useful to have a measure of the input signal's power so that the communication channel is used in its full potential. With a power consumption smaller than 600 µW the RSSI presents an input dynamic range larger than 50 dB. The fourth block implements a Squelch function, in order to suppress unwanted output toggling due to noise.

All these elements were developed in a TSMC 65 nm CMOS process with a 1.2 V supply voltage.

Keywords: CERN, LHC, Optical Receiver, Radiation-tolerant, LA, RSSI, Output Buffer, Squelch.

Resumo

As experiências de física de alta energia, que ocorrem no LHC do CERN, exigem uma ligação de alta velocidade, para uma transmissão eficiente dos dados gerados pelas mesmas. Um canal de transmissão optoeletrónico surge como sendo a melhor solução devido à possibilidade de trabalhar com altos ritmos de transmissão e à imunidade ao ruído eletromagnético da fibra ótica. Este projeto é exigente devido às especificações associadas ao ritmo de transmissão (5Gb/s) e ao BER ($10^{-}12$) bem como às restrições impostas pela radiação. Dado que, neste tipo de ambiente, a radiação é sempre um constrangimento, o Recetor Ótico deverá ser capaz de tolerar e apresentar imunidade à mesma.

O núcleo do Recetor Ótico inclui um Fotodíodo, um Amplificador de Transimpedância e um Amplificador Limitador. Esta tese propõe o estudo e implementação de um destes elementos de base, o Amplificador Limitador, como elemento principal, e de outros três blocos.

Os dois principais requisitos da especificação do Amplificador Limitador foram a largura de banda e a minimização do consumo de potência, objetivos cumpridos usando uma combinação de técnicas de aumento de largura de banda. Apresenta uma largura de banda de 4.8 GHz com um consumo de potência inferior a 19 mW.

Outro bloco essencial é o Buffer de Saída. O requisito principal neste bloco foi alcançar tempos de transição baixos, aumentando a integridade do sinal. O Buffer apresenta uma excursão sinal diferencial que ronda os 400 mV com níveis de *Pre-emphasis* superiores a 130%.

O terceiro bloco é um Indicador de Potência de Sinal Recebido. Com um consumo inferior a 600 µW apresenta uma gama dinâmica superior a 50 dB. O quarto elemento assegura uma função de *Squelch*, suprimindo o ruído na saída, quando não há transmissão.

Todos estes elementos foram desenvolvidos em tecnologia CMOS 65 nm da TSMC com uma tensão de alimentação de 1.2 V.

Palavras-chave: CERN, LHC, Recetor Ótico, Tolerante à radiação, Amplificador Limitador, Indicador de Força de Sinal Recebido, Buffer de Saída, *Squelch*.

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Acronyms

AC Alternating Current.

AM Amplitude Modulation.

BER Bit Error Ratio.

CDR Clock and Data Recovery.

CERN *Conseil Européen pour la Recherche Nucléaire*.

CML Current-Mode Logic.

CMOS Complementary Metal-Oxide-Semiconductor.

CMRR Common-Mode Rejection Ratio.

DC Direct Current.

DR Dynamic Range.

FOX Field Oxides.

FWR Full-Wave Rectifier.

GBW Gain–Bandwidth Product.

HBD Hardness-by-Design.

HEP High Energy Physics.

ISI Intersymbol Interference.

JTOL Jitter Tolerance.

KCL Kirchhoff's Current Law.

KVL Kirchhoff's Voltage Law.

LA Limiting Amplifier.

LHC Large Hadron Collider.

MOM Metal Oxide Metal.

MOSFET Metal-Oxide Semiconductor Field-Effect Transistor.

NMC Negative Miller Capacitance.

NMOS Negative Channel Metal-Oxide Semiconductor.

PCB Printed-Circuit Board.

PM Phase Modulation.

PMOS Positive Channel Metal-Oxide Semiconductor.

PRBS Pseudo-Random Binary Sequence.

PVT Process Voltage and Temperature.

RC Resistor–Capacitor.

RSSI Received Signal Strength Indicator.

SEE Single-Event Effects.

SNR Signal-to-Noise ratio.

SRF Self-Resonant Frequency.

TIA Transimpedance Amplifier.

TID Total Ionizing Dose.

VGA Variable Gain Amplifier.

CHAPTER 1

Introduction

This Chapter's purpose is to contextualize the Limiting Amplifier sub-block and its function in an Optical Receiver to be implemented in a 65 nm Complementary Metal-Oxide-Semiconductor (CMOS) technology with a 1.2 V power supply for a high-speed optical link (as well as other sub-blocks such as: a Received Signal Strength Indicator, a Squelch circuit and an Output Buffer with Pre-emphasis capability). It will be explained what motivated this project in the first place, and the main goals to be achieved during this work.

The European Organization for Nuclear Research, known as *Conseil Européen pour la Recherche Nucléaire* (CERN) performs experiences at the Large Hadron Collider (LHC), so the need for a way to efficiently transfer the huge amount of data generated by these experiences to the counting room is imminent. Due to the radioactive nature of these experiences the most practical way to do this is using optical fiber, since it has a high tolerance to radiation and is practically immune to magnetic fields and electromagnetic noise. Therefore, it is necessary to have a high speed radiation-tolerant Optical Receiver, and the most economical way to do it is having all the blocks embedded in the same Integrated Circuit (IC). Albeit there are many CMOS Optical Receivers in the market, they cannot be used in this particular situation since they are not radiation-hardened. This receiver requires a very large bandwidth in order to fulfill the data acquisition system requirements.

The core of the Optical Receiver consists of three major sub-blocks: the Photodiode and the corresponding bias circuit, the Transimpedance Amplifier and the respective Offset Cancelation block, and finally, the Limiting Amplifier. Fig 1.1 shows a simplified schematic of the Optical Receiver's architecture.

Without going into many details about the function and the design of each sub-block, a brief explanation will be given. The Photodiode is responsible for detecting the light

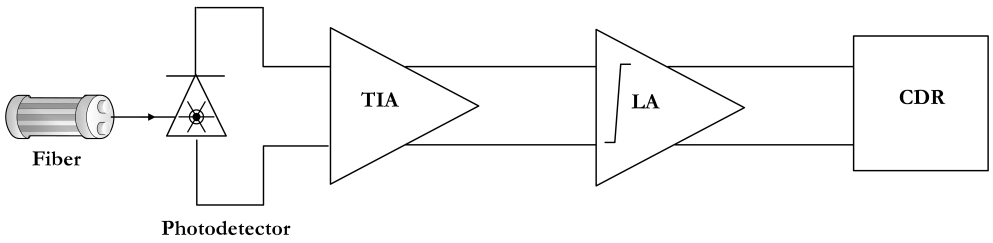


Figure 1.1: Simplified block diagram of a standard Optical Receiver.

signal in the fiber, working in the reverse bias region in order to maximize its sensitivity, which is made possible due to the existence of a biasing circuit (which includes a step up voltage converter to produce a 2 V power supply) that adjusts the voltage across the photodiode in order to maintain it in this region. The TIA converts the input current from the Photodiode into a voltage signal, and cancels the offset of the signal to avoid saturation in the following amplification stages. After that, the Limiting Amplifier provides additional voltage gain, boosting the signal swing in order to achieve a clear digital signal, so it can be properly detected by the Clock and Data Recovery (CDR).

1.1 Motivation

In order to conveniently transmit the data originated from the LHC experiments to the counting room, it is necessary to have a communication channel that allows for high data rates, and must consequently have a sufficiently large bandwidth. When a signal is propagating in an electrical line (e.g. coaxial cable) it will start with sharp rising and falling "edges" but, as the distance increases, these edges will be softened due to the loss-related distortion and dispersion. This phenomenon is illustrated in Fig. 1.2.

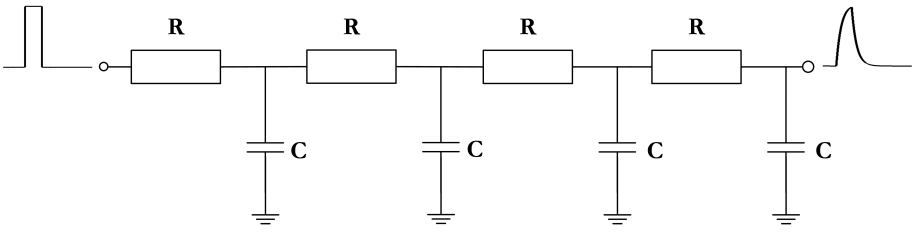


Figure 1.2: Softening of the edges in an electrical line - RC model for lossy line.

The "softening" of the edges makes precise extraction of timing information harder. In optical fibers, for the same communication distances this effect is not as noticeable, since the dispersion and loss is smaller than in electric wires [1] .This makes optical communication suited for higher data rates, which are necessary to fulfill the data acquisition system requirements for the LHC experiments.

There is also a major advantage that makes optical fiber the most efficient type of communication channel for this particular application. It can be used in environments with large Electromagnetic Interference and Radio-Frequency Interference which is the case of the surrounding environment of the LHC, where radiation is not the only source for disturbance or system failures: the electromagnetic environment in the tunnel and service areas is rich in interference sources [2]. Hence, the use of optical fiber implies the existence of an Optical Receiver, which consists of the blocks mentioned earlier plus an off-chip CDR circuit (which is not to be implemented in this project). Although there are many wideband Optical Receivers available in the market there is a need for a special circuit. Due to the beam interactions with residual gases, collimators or other equipment in the experiences, there is a lot of ionizing radiation with a broad energy spectrum. This ionization can permanently damage the electronic components by altering the device parameters. For example, it can change the value of the transistors' threshold voltages and leakage currents and, in the case of the Photodiode, it can brutally increase its Direct Current (DC) leakage current, leading to a decrease in the Photodiode bias voltage (due to high voltage drops in the biasing circuit). The permanent changes in the electronic devices caused by radiation are called Total Ionizing Dose (TID) effects. Additionally, radiation can also cause exceptional and isolated events. These are called Single-Event Effects (SEE), such as: Single-Event Upsets (SEUs), Single-Event Functional Interrupts (SEFIs), Single-Event Transients (SETs), and Single-Event Latchups (SELs) [3].

For these reasons, the associated electronic components need to be capable of sustaining high radiation doses (2 MGy[1]) [4] and survive in this environment. In order to use microelectronics in this kind of environment, it is mandatory to mitigate the radiation effects. This can be achieved by using the Hardness-by-Design (HBD) methodology, thus making the circuit radiation-hardened. HBD techniques can be done at the transistor level, the component level, and the system level, guarantying TID and SEE toleration.

These "special" conditions create the necessity for a more complex Optical Receiver with some particular design constraints, and singular specifications that make it different from the other products available in the market. This constitutes the main motivation for this investigation project.

[1] The gray (symbol: Gy) is a derived unit of ionizing radiation dose in the International System of Units (SI). It is defined as the absorption of one joule of radiation energy per kilogram of matter.

In this context, the Limiting Amplifier appears as a fundamental block for the Optical Receiver's body. Its main function is to create a clear digital signal at a fixed swing (independent of the input voltage swing) that can be adequately detected by the CDR circuit. The correct operation of this block is of the utmost importance for the overall system performance, since it has to satisfy the input sensitivity of the attached Clock and Data Recovery circuit for proper data reconstruction. In other words, the amplitude of the LA's output signal has to be greater than this value (CDR's input sensitivity), and the rise and fall time both have to allow correct detection of the zero crossings. So, the incorrect or poor behaviour/operation of the Limiting Amplifier can negatively impact the system performance, increasing the Bit Error Ratio (BER)[2], therefore causing incorrect bit detections [5], Chapter 7.

1.2 Thesis Organization

This thesis is organized in four Chapters. Them being: Introduction, Literature's Review, Implementation in CMOS and Conclusions and Future Work.

The first one (namely this one) contextualizes the overall Optical Receiver and its necessity. It briefly explains why optical communication is suited for this application. It also defines the functions and responsibilities of each core block in the overall Optical Receiver.

The second Chapter is the Literature's Review and its purpose is to study and understand the major issues and constrains when designing a Limiting Amplifier. It also presents some possible techniques used to overcome those issues - bandwidth enhancement techniques. Practical examples of application of this techniques are provided as well as a comparision chart. In addition to that, each of the other blocks and their tasks are shortly discussed. Furthermore, and due to the environment in which the Optical Receiver will work, the effects of radiation in modern CMOS process are also addressed, especially the TID effects.

The third Chapter is the Implementation in CMOS and it covers the design and implementation of all four blocks. It is devided in four sections, one for each block. Which one contains a theoretical analysis of the block, - for some blocks mathematical models were also developed and presented, as well as a comparison with real simulation results - the schematics of all the master circuits used and its components' dimensions, the relevant electric simulations regarding that particular block and also the layout of some integrant sub-blocks.

The last Chapter presents the most relevant conclusions regarding each Chapter and the four blocks designed. The aspects that could have been improved or made differently are also addressed in this Chapter.

[2]Bit Error Ratio is defined as $\frac{\#bit\ errors}{\#bits\ received}$.

Lasty, the Appendix includes some layouts that were executed and that are not going to be discussed in detail during this thesis.

CHAPTER 2

LITERATURE'S REVIEW

2.1 Limiting Amplifier

The current signal originated in the Photodiode is converted into a voltage signal by the TIA. However, this signal typically suffers from a low output swing (only a few milivolts for the minimum input current - 10 µA) which is clearly not sufficient to satisfy the sensitivity of the CDR. Therefore, the Limiting Amplifier or Limiter[1] has to boost the signal's swing, bringing it to logic levels with an amplitude of around 500 mV. Then, the CDR receives this boosted signal and decides the binary nature of the voltage, and thusly of the input optical signal.

LAs have to provide high voltage gain and a large bandwidth. An open-loop configuration of a cascade of broadband stages is typically used to fulfil these requirements. Altough, sometimes, the use of some broadband techniques is required, in order to increase the bandwidth of each stage (since in a cascade of broadband stages the bandwidth decreases with the number of stages limiting the overall LA bandwidth). This subject is going to discussed in more detail, since the last amplification stages work in large signal mode, invalidating the concept of small-signal bandwidth (the large-signal speed in a cascade of gain stages is limited by the speed of a single gate, and not by the complete cascade). Sometimes the LA also incorporates an Offset Cancelation block so is does not saturate due to the DC component, avoiding a premature detection of the signal.

LAs must often drive off-chip loads, so it is necessary to use an Output Buffer for impedance matching[2] (typically 50 Ω) while providing large currents and reasonable

[1] In optical communications it is commonly known as a Limiting Amplifier, in RF community it is called a Limiter.

[2] Impedance matching is the practice of designing the input impedance of an electrical load, or the output impedance of its corresponding signal source to maximize the power transfer, or minimize signal reflection from the load.

output swings to the load.

Automatic Gain Control (AGC) is another method that allows to keep constant signal amplitude independent of the input swing. However, compared with LAs, Automatic Gain Control needs more setting-up time, more complex analog circuits and larger chip area. For these reasons, Limiting Amplifiers are more commonly used for wideband Optical Receivers.

2.1.1 Performance Parameters

Let us now discuss the main performance parameters that must be taken into account when designing a Litimiting Amplifier for an Optical Receiver. As mentioned before, the LA plays an important role on the Optical Receiver, allowing for the correct detection of the signal, and so it must satisfy the demanded requirements.

2.1.1.1 Bandwidth

Limiting Amplifiers are designed to have greater bandwidth than the TIAs (a common value is $1.5B_{TIA}$), because they need to be capable of clipping the signal provenient of the TIA, and generate a signal with high slew rate and near to zero transition times. Typically, a Limiting Amplifier's bandwidth is designed to be equal to the data rate, which implies that the bandwidth of each stage (LAs are usually built as a cascade of gain cells) has to be bigger than this value. If the LA's bandwidth were to be lower than the signal's bandwidth, this would affect the edge timing and amplitude at the sampling instant, lowering the eye opening and contributing to Intersymbol Interference (ISI) [5]. This effect is illustrated in Fig. 2.1.

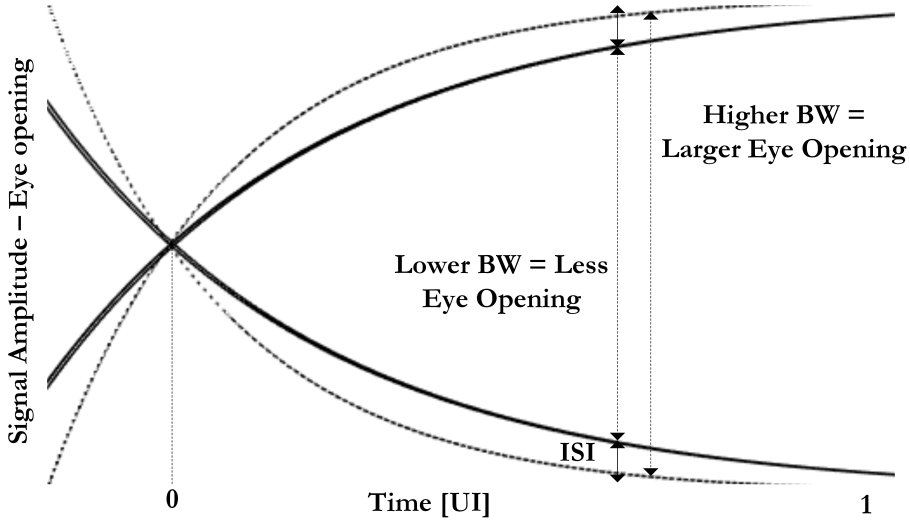


Figure 2.1: Eye diagram for two different bandwidths and resulting ISI. Adapted from [5], Chapter 3.

An eye diagram is a useful tool for understanding signal impairments in the physical layer of high-speed digital data systems, verifying transmitter output compliance, and revealing the amplitude and time distortion elements that degrade the BER for diagnostic purposes. By taking high-bandwidth instantaneous samples of a high-speed digital signal, an eye diagram is the sum of samples from superimposing the 1s, 0s, and corresponding transition measurements [6]. The data rate is used to trigger the horizontal sweep, and represented in UI, which stands for Unit Interval and is defined as the minimum time interval between condition changes of a data transmission signal, also known as the pulse time or symbol duration time. In this context, the eye opening corresponds to one bit period and is typically called the UI width of the eye diagram.

2.1.1.2 Noise

The referred input noise is relevant in Limiting Amplifiers for three main reasons. Firstly, the large bandwidth of these amplifiers yields a large integrated noise. Secondly, the design of TIAs with high transimpedance gain is more difficult at high speeds, making the noise contribution of the LA more significant. Lastly, the amplitude noise in the Limiting Amplifiers is modulated as phase errors (due to the non-linear behavior of this amplifier) causing jitter noise (this will be discussed in more detail in Section 2.1.3) and consequently impacting the signal detection. The amplitude noise can also affect the vertical opening of the eye diagram, reducing its quality factor, and therefore increasing the BER. The smaller the eye width at the sampling instant, the bigger the probability of a 1 bit to mistaken by a 0 and vice-versa.

2.1.1.3 Gain

The first amplifier stage (assuming a cascade of gain stages) must employ a large gain, in order to minimize the noise contribution of the following stages. If the TIA's noise is already large sometimes a downscaling technique is used, as a way to reduce the noise and the loading effect.

2.1.1.4 Drive Capability

The Output Buffer is responsible for driving the output loads, delivering large currents to off-chip 50 Ω loads. These large currents force the transistors of the Output Buffer to have large dimensions, leading to large gate capacitances. Therefore, the buffer will exhibit a high input capacitance heavilly loading the preceding stage, possibly becoming the bottleneck for the bandwidth in the communication channel. This means that the last gain stage has to be able to drive a large capacitive load, while mantaining a wide bandwidth.

2.1.1.5 Jitter

Jitter is one of the most important performance parameters in Limiting Amplifiers. Due to the non-linear behaviour of the last LA's stages (working in large signal operation), the amplitude variations (such as amplitude noise) are modulated as time shifts, resulting in an Amplitude Modulation (AM)-Phase Modulation (PM) conversion. This causes a deviation of the zero crossings from the ideal position, which is defined as jitter.

2.1.1.6 Offset Voltage

Typically, an offset cancellation circuit is added to the first amplifying stages to prevent the offset (due to the device mismatch) from saturating the amplifier, thusly preventing incorrect signal detection.

2.1.2 Cascade of Gain Stages

Let us consider a simple open-loop configuration where N broadband gain stages are placed in cascade in order to provide large output swing and large voltage gain. Each amplifier block can be seen as an ideal voltage amplifier with gain A_0 followed by an Resistor–Capacitor (RC) circuit (composed by an output resistor R_{out} and a load capacitor, C_L). Such an architecture is depicted in Fig. 2.2. It is important to understand that this model only provides a small signals' analysis of the Limiting Amplifier, which is not enough to understand its behaviour (the saturation effect is not taken into consideration) and it is necessary to study the large-signal operation of the Limiting Amplifier, since the last stages of amplification tend to work in this mode of operation (mostly when the input current is above the minimum value).

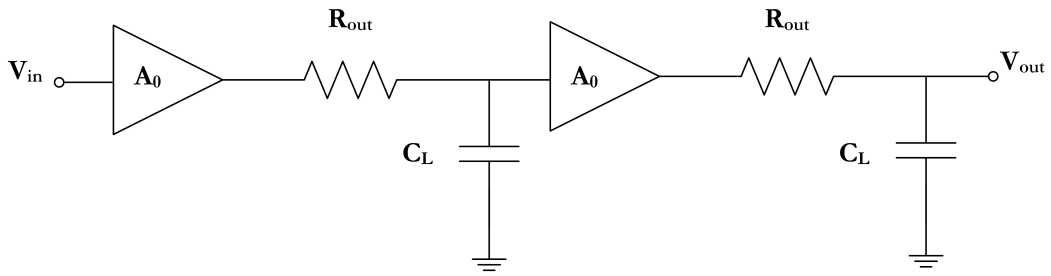


Figure 2.2: Simplified small signals' model of a cascade of two gain stages.

The corresponding transfer function, for a cascade of two stages, is given by expression 2.1.

$$H(s) = \left(\frac{A_0}{1 + \frac{s}{\omega_0}} \right)^2 \tag{2.1}$$

where $\omega_0 = (R_{out} C_L)^{-1}$ is the frequency (in rad/s) of the poles and corresponds to the -3dB[3] bandwidth of each amplification stage. One can assume that the -3dB bandwidth of the system is a reasonable measure of its speed (and consequently, of the maximum bit rate). Replacing $s = j\omega_{-3dB}$ in expression 2.1 and solving for ω_{-3dB}:

$$\left| \left(\frac{A_0}{1 + \frac{\omega_{-3dB}}{\omega_0}} \right)^2 \right| = \frac{A_0^2}{2} \Leftrightarrow \left(\frac{A_0}{\sqrt{1 + (\frac{\omega_{-3dB}}{\omega_0})^2}} \right)^2 = \frac{A_0^2}{2} \tag{2.2}$$

The -3dB bandwidth of the system, ω_{-3dB}, is given by expression 2.3.

$$\omega_{-3dB} = \omega_0 \sqrt{\sqrt{2} - 1} \tag{2.3}$$

By scaling this logic to the N identical stages is possible to obtain a generic expression of the -3dB bandwidth of the system as a function of the number of stages, given by expression 2.4.

$$\omega_{-3dB} = \omega_0 \sqrt{\sqrt[N]{2} - 1} \tag{2.4}$$

Fig. 2.3 illustrates the ratio between the bandwidth of each stage, and the total bandwidth as a function of the number of cascaded stages. In other words, how large each stage's bandwidth has to be, in order to achieve a determinated value for the overall system's bandwidth.

One can see that, beyond 5 cascaded stages, the bandwidth required by an individual stage to achieve a given system's bandwidth is almost 3 times bigger, suggesting that it may be unpractical to build a Limiting Amplifier with more than 5 stages (depending on the gain specifications). Analyzing expression 2.4 it is possible to conclude that, in order to have a given system bandwidth, each stage of amplification must accomplish a larger bandwidth (e.g., for $N = 3$ the bandwidth of each stage has to be almost twice the overall bandwidth).

The DC gain of the cascade can be defined as $A_{tot} = A_0^N$ (where A_0 is the gain of each stage, considering equal gain for all the stages) which means that it may be useful to to distribute the gain over a large number of stages. On the other hand, when using low gain in the first stages (as a way to maximize the bandwidth) the last stages accumulate all the noise, resulting in an increased Signal-to-Noise ratio (SNR).

[3]The -3dB bandwidth is defined as the separation between zero frequency - where the amplitude spectrum attains its peak value - and the positive frequency at which the amplitude spectrum drops to $\frac{1}{\sqrt{2}}$ of its peak value. Or, alternately, drops to half of its peak power.

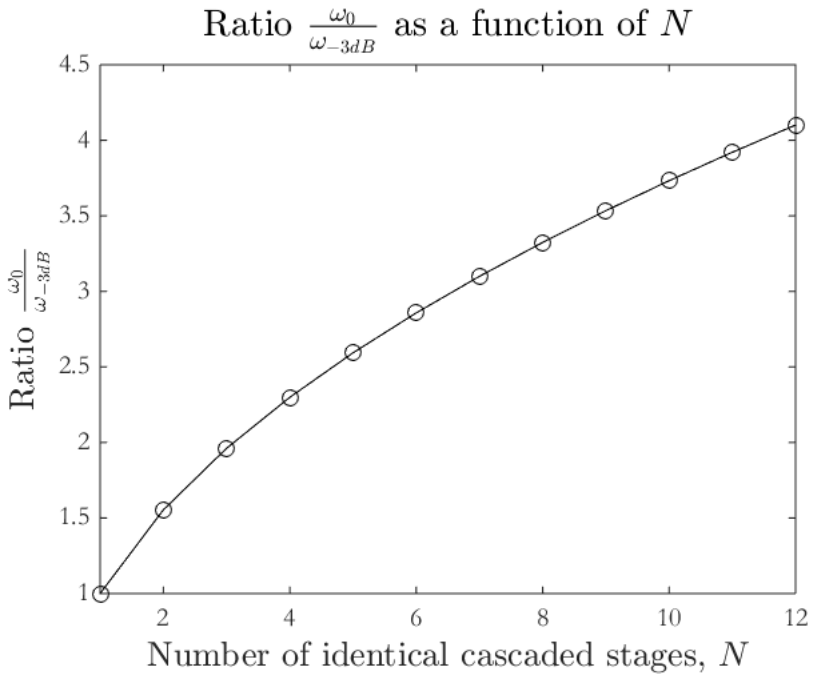


Figure 2.3: Ratio $\frac{\omega_0}{\omega_{-3dB}}$ as a function of the number of cascaded stages, N.

There is a clear tradeoff between gain and bandwidth, if each stage of amplification has a small gain and a very large bandwidth, then N has to be large enough to fulfil both the overall gain specifications, A_{tot}, and the bandwidth requirements at the same time. This hints that there is an optimum value for N (for a specific system gain, A_{tot}) that allows the maximization of the overall system bandwidth. Let us define $B = A_0\omega_0$ as the Gain–Bandwidth Product (GBW) which is considered to be constant for a certain technology (for a given power consumption). So, for N stages $A_{tot} = \left(\frac{B}{\omega_0}\right)^N$ and $\omega_0 = \frac{B}{\sqrt[N]{A_{tot}}}$. Replacing these parameters in expression 2.4, is possible to obtain:

$$\omega_{-3dB} = B\frac{\sqrt{\sqrt[N]{2}-1}}{\sqrt[N]{A_{tot}}} \tag{2.5}$$

As demonstrated in [7], Chapter 5, the optimal value the number of cascaded stages, N_{opt}, is given by:

$$N_{opt} = 2\ln A_{tot} \tag{2.6}$$

One should note that this value is independent from the GBW and of the technology for that matter. The optimum gain per stage is given by $A_0 = \sqrt{e}$ as derived in [5], Chapter 7.

Fig. 2.4 shows the evolution of the normalized bandwidth $\frac{\omega_{-3dB}}{B}$ as a function of N for two different system gains, $A_{tot} = 100$ and $A_{tot} = 200$. For $A_{tot} = 100$ the maximum bandwidth is achieved for $N = 9$ and for $A_{tot} = 200$ for $N = 10$. There is a common result for both graphics: for $N \geqslant 6$ the increase in the bandwidth is not significant (smaller than 10% in both cases). This is the main reason why typically, amplifiers with more than 5 stages are not implemented (also because low gain stages contribute to more noise in the latter stages). Let us also define ω_{-3dB} as $2\pi R_b$, where R_b denotes the bit rate. From the graph in Fig. 2.4 we see that the maximum bandwidth is of approximately $0.17B$ (for $A_{tot} = 100$) and $0.16B$ (for $A_{tot} = 200$) which implies that B has to be greater than $2\pi \times (6R_b)$ (approximately for both cases). But, as mentioned before, this value does not need to be as large, because the latter stages have larger input swings and, for that reason, the Limiting Amplifier works in large-signal mode. In other words, when the input signal's amplitude is sufficiently large, one branch of the circuit is OFF while the other carries the total current, experiencing a fully switched state. In this mode of operation the small signals' analysis is not valid. Note: a differential topology is assumed in further calculations.

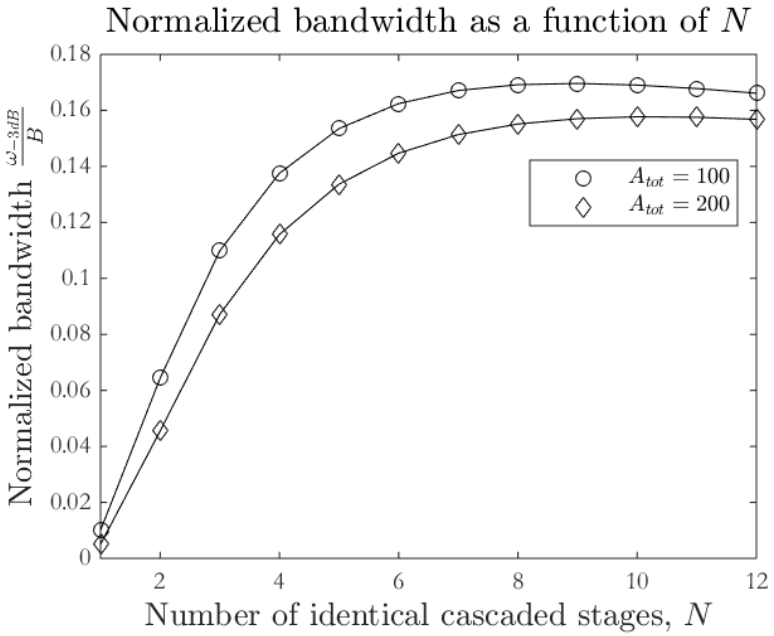


Figure 2.4: Normalized bandwidth as a function of the number of cascaded stages for $A_{tot} = 100$ and $A_{tot} = 200$.

This means that each LA's stage can work in two distinct operation regimes: one is a linear region where both transistors are ON and can be defined by the small signals' model of the circuit, and a non-linear region or saturation regime where one of the transistors is OFF and the other one drives all the current, where a small signals' analysis cannot be applied. Fig. 2.5 illustrates this effect in a cascade of differential pairs, manifesting itself strongly in the third stage.

Due to the existence of non-linear behaviour, and the fact that one transistor will completely steer all the tail current I_T, the last two stages experience different zero crossing time instants. This proves that the small signals' model is not valid in this regime of operation.

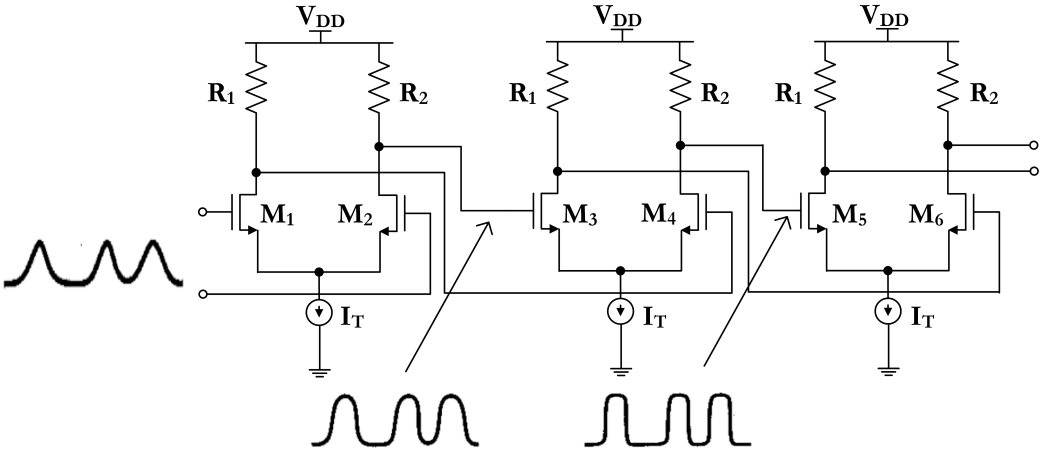


Figure 2.5: Non-linear behavior in a cascade of differential pairs. Adapted from [7], Chapter 5.

Let's consider a simple differential pair as represented in Fig. 2.6. Now, let us consider that V_{in1} and V_{in2} are large enough, and that the circuit displays a very large transconductance in equilibrium, so that it will work in large signal operation even around the zero crossing times of the input signal (defined by ΔT). As a consequence, M_1 and M_2 will be able to drive the tail current, I_T, during ΔT creating a "sharper" signal. However, the speed of the output signal is limited by a time constant $\tau = R_1 C_1$ creating a delay on the time response. The input signals, V_{in1} and V_{in2}, as well as the drain currents of M_1 and M_2 (I_{D1} and I_{D2}), and the output voltages (V_{out1} and V_{out2}) are represented in Fig. 2.7.

This means that, in a cascade of identical stages (assuming of course, a differential architecture), when one amplifier saturates, the rise and fall times of the output signal are limited only by its time constant, and what occurs in previous stages does not influence the rise and fall times. In other words, the speed is bound only by one stage, similar to what happens in a cascade of digital gates [5], Chapter 3.

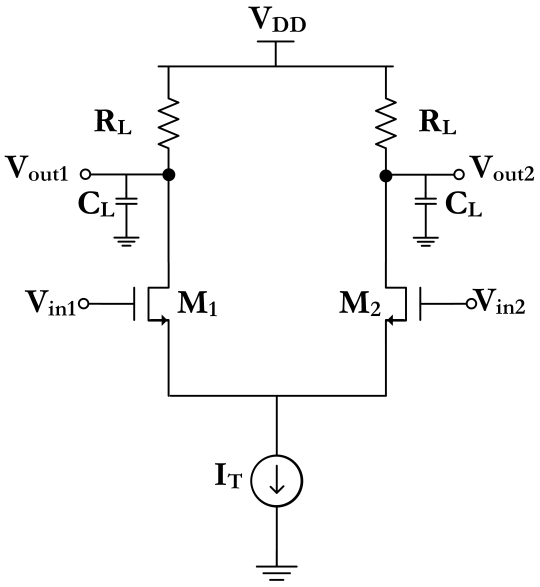


Figure 2.6: Differential pair.

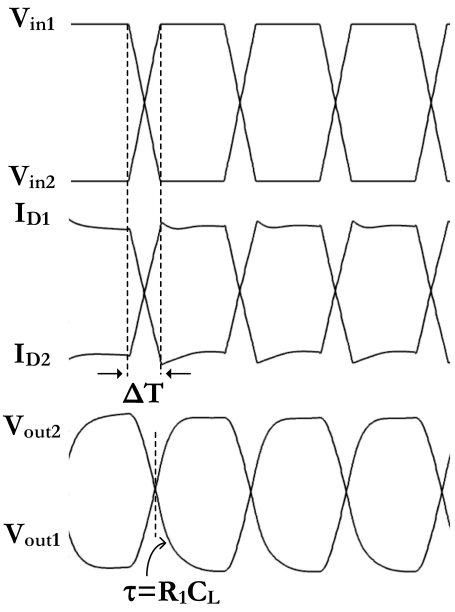


Figure 2.7: Delay in a differential pair. Adapted from [7], Chapter 5.

2.1.3 AM/PM Conversion

There is also an interesting phenomenon illustrated in Fig. 2.7. There is an AM to PM conversion. The amplitude variations are being converted to a time delay, which is equivalent to a phase error (this effect is due to the saturation of the differential pair which resembles a non-linear low-pass circuit). Observing Fig. 2.7, one can see that the drain currents I_{D1} and I_{D2} cross the zero at the same time as the input signals. But the output voltages are experiencing a delay in the zero crossing instant, when compared to the input waves. Although the currents do not suffer from phase modulation, the variation of the input signal's amplitude (assuming a sinusoidal wave) passing through a frequency-dependent load (RC circuit) causes phase deviation in the first and third harmonics of the output voltage [7], Chapter 5.

This effect can prove itself really harmful when the input signal contains random amplitude noise, causing the output signal to have random shifts in its zero crossings leading to excessive jitter noise. Fig. 2.8 illustrates the contribution of the amplitude noise in the unwanted phase errors, where the amplitude noise causes a delay, ΔT_0, from the ideal zero crossing instant, t_0. Jitter plays an important role for the correct operation of the Clock and Data Recovery circuit. The total amount of jitter that the CDR can tolerate before the synchronization in lost (meaning, before the maximum BER is exceeded) is called Jitter Tolerance (JTOL).

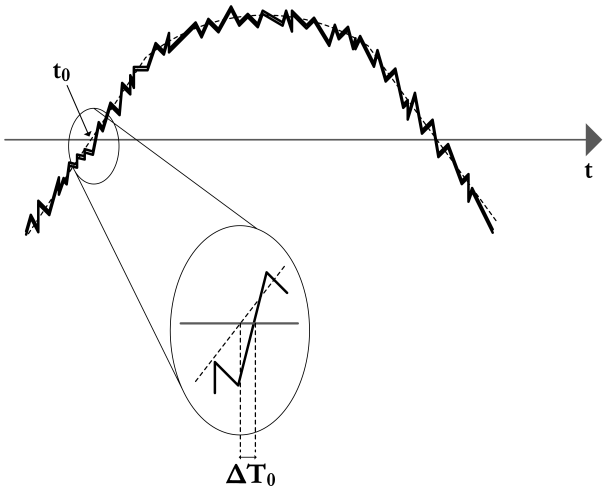


Figure 2.8: Effect of random amplitude noise on jitter. Adapted from [7], Chapter 2.

2.1.4 Broadband Techniques

Sometimes a cascade of simple differential pairs with resistive loads is not enough to satisfy the system's stringent bandwidth requirements, resulting in the need for some bandwidth enhancement techniques. In this Chapter, the state of the art of these techniques and architectures will be discussed, as well as both their advantages and disadvantages.

2.1.4.1 Inductive Peaking

The bandwidth of a gain stage is always bounded by the capacitive load, usually at the output node, that along with R_L consists in a large time constant. For a simple common-source stage, as illustrated in Fig. 2.9 a), the pole at the output is defined by $\omega_0 = \frac{1}{R_L C_L}$. It is possible to include an inductor at the output node, Fig 2.9 b), in order to partially cancel the load capacitance, and consequently extend the bandwidth.

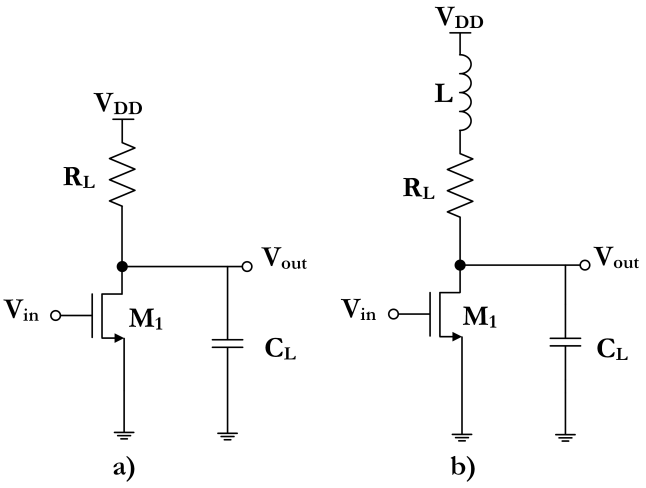


Figure 2.9: a) Common source stage without Inductive Peaking. b) Common source stage with Inductive Peaking.

However, implementing an inductor in an integrated circuit can be a challenging task. On-chip inductors have an higher quality factor (Q), low noise and low voltage headroom consumption, albeit occupying a large area and leading to more parasitic capacitances. Furthermore, it is usually difficult to realize a spiral inductor with a high inductance but keeping the Self-Resonant Frequency (SRF)[4], well outside the pass-band at the same time [8].

The inductive load can be done by on-chip spiral inductors (passive inductors) [9], conventional active inductors [10], [8], [4] and conventional active inductors using a voltage boosting technique [11].

When chip area is an important factor, inductors can be implemented by active devices, having a lower Q but being able to work at higher frequencies. Active inductors require a large voltage headroom which can make its implementation very hard for low supply voltages. Reference [8] presents a differential topology with inductive loads in every LA stage, known as shunt peaking. This architecture is presented in Fig. 2.10. In this topology the active inductors are implemented by the transistor and resistor pairs: $[M_{ail1}, R_{g1}]$ and $[M_{ail2}, R_{g2}]$.

[4] At frequencies below the SRF, the model appears to be inductive; at frequencies above the SRF it appears to be capacitive and at the SRF it is resistive.

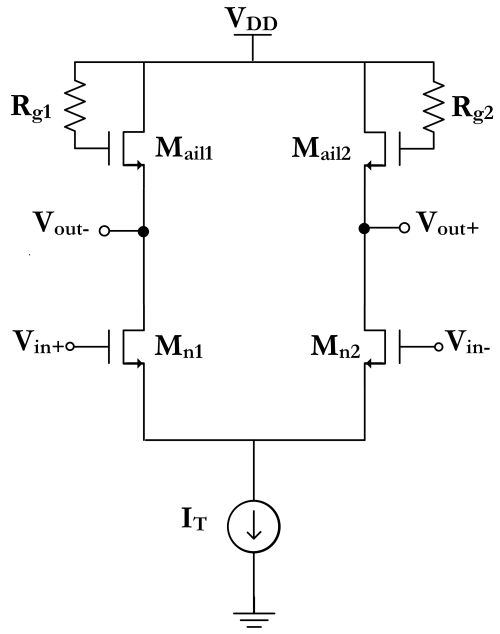


Figure 2.10: Differential pair with active inductive load. Adapted from [8].

The active inductor circuit is represented in Fig. 2.11 a). Fig. 2.11 b) represents the simplified equivalent small signals' model (neglecting the body effect, the gain-drain and bulk-source capacitance, and channel-length modulation). Applying Kirchhoff's Current Law (KCL) to the node V_x in Fig. 2.11 b) and solving for V_x it is possible to calculate the impedance seen from the source of the transistor by doing $Z_{out}(s) = \frac{V_x}{i_x}$:

$$Z_{out}(s) = \frac{R_{g1}C_{gs} + 1}{g_m + C_{gs}s} \tag{2.7}$$

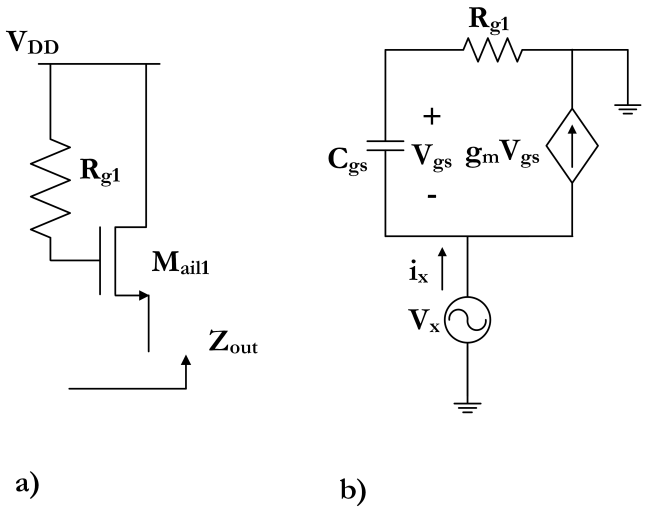


Figure 2.11: a) Active inductor. b) Small signals' model of an active inductor.

The frequency response of the equivalent normalized impedance is represented in Fig. 2.12 a). It is possible to see that the frequency behaviour almost equals the one of a passive inductor - except for the existence of a pole. The reader should note that neglecting the effect of the other parasitic capacitances and the body effect eliminates the existence of a second pole, that would cause a decrease in the impedance at higher frequencies, as depicted in Fig. 2.12 b).

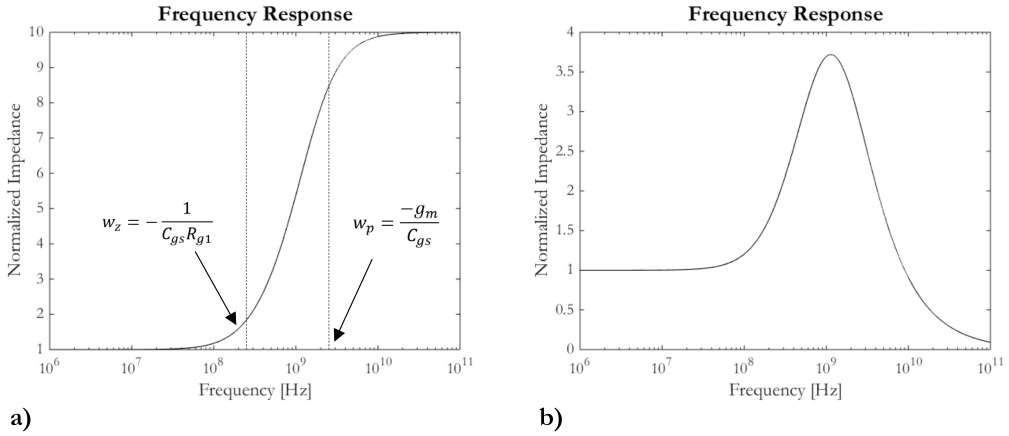


Figure 2.12: a) Frequency response of the normalized impedance of an active inductor (simplified). b) Frequency response of the normalized impedance of an active inductor (complete).

Reference [8] shows that it is possible to obtain a flat frequency response for the shunt peaking amplifier, as well as an increase of about 70% in the bandwidth before the peaking occurs. Another advantage of this particular topology is that the DC gain exhibits an extremely weak dependence on process, temperature and bias, because the ratio of the Negative Channel Metal-Oxide Semiconductor (NMOS) transistors M_{n1} and M_{ail1} determines the gain.

A different topology for the gain cell is presented in [10]. The active inductor is implemented by a simple high-Q two-transistor but, instead of being connected in series - like it is commonly done with a Positive Channel Metal-Oxide Semiconductor (PMOS) active load - it is connected at the output node supressing the load capacitance effect, therefore increasing the bandwidth. The peculiarity of this circuit is that transistors that implement the inductors are biased using a controlled voltage which allows to tune the inductance by changing this parameter. Hence, obtaining different frequency responses for different values of the biasing voltage without degenerating the voltage headroom of the active inductor [10]. This gain cell was used in a fully differential Limiting Amplifier for an Optical Receiver implemented in a 0.18 µm CMOS technology.

2.1.4.2 Capacitive Degeneration

Capacitive Degeneration is another bandwidth enhancement technique that consists in degenerating the transistors of a differential pair by placing a capacitor and a resistor in parallel, connected between the sources of the transistors, Fig. 2.13. This causes an increase in the effective transconductance of the circuit at higher frequencies, compensating for the decrease in the voltage gain due to the pole at the output node.

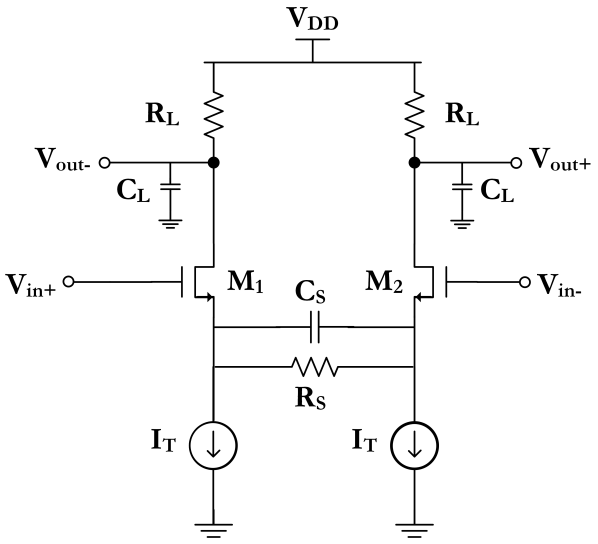


Figure 2.13: Differential pair with Capacitive Degeneration.

Aplying a single-ended analysis in this circuit (considering the half-circuit), it is possible to calculate the transfer function for the equivalent transconductance, G_m, and the corresponding poles and zeros, as demonstrated in [12]:

$$G_m(s) = \frac{g_m(R_S C_S s + 1)}{R_S C_S s + 1 + g_m \frac{R_S}{2}} \tag{2.8}$$

The corresponding zero and pole are given by Eq. 2.9 and Eq. 2.10, respectively.

$$\omega_z = \frac{1}{R_S C_S} \tag{2.9}$$

$$\omega_p = \frac{1 + g_m \frac{R_S}{2}}{R_S C_S} \tag{2.10}$$

The zero of the effective transconductance can be placed in order to cancel the output node pole, therefore extending the circuit's bandwidth up to the transconductance pole. This is the key idea behind this technique, and surely this increase in the bandwidth implies a decrease in the DC gain by the same amount. Fig. 2.14 a) illustrates the frequency response of the normalized equivalent transconductance, and the position of the corresponding zero and pole. Fig. 2.14 b) represents the frequency response of the voltage gain, when the degeneration zero is matched to the dominant pole at the output node.

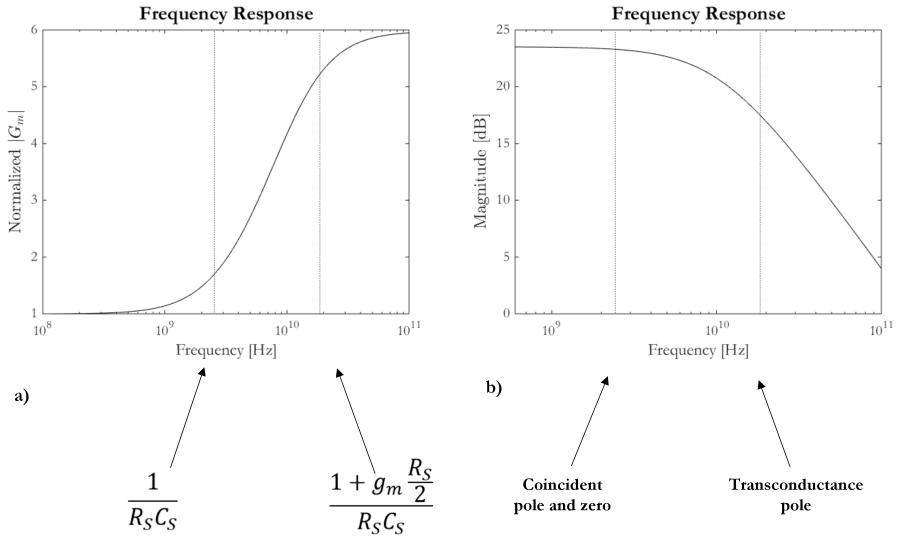


Figure 2.14: a) Frequency response of the normalized equivalent transconductance, G_m. b) Frequency response of the voltage gain.

Capacitive Degeneration can also be used to cancel DC offset locally, instead of placing Alternating Current (AC) coupling between each stage (which occupies a lot of chip area) or using external feedback loops that can bring stability issues specially in high frequency circuits. This particular apllication of Capacitive Degeneration was used in [13], where the DC offset is reduced whithout impacting the high frequency gain.

2.1.4.3 Negative Miller Capacitance

The ideia behind Negative Miller Capacitance (NMC) is exploiting the Miller[5] effect to reduce the input capacitance of one amplifier stage, thus reducing the load effect in the previous stage and improving the overall bandwidth. Fig. 2.15 shows a gain stage employing NMC technique.

It it possible to perceive, by observation only, that the capacitors C_M are connected to the opposite output node, thusly suffering from a 180° phase shift between the signals in both nodes, and adding up to the gain-drain overlap parasitic capacitance of transistor M_1 and M_2 with a negative sign.

For better understanding of this effect, let us consider a high level schematic of a two-stage amplifier with negative miller capacitors, Fig. 2.16. Where $C_{P,X}$ is the input capacitance of each stage and $C_{M,X}$ are the capacitors used to take advantage of the Miller effect, and A is the voltage gain of the amplifier. The effective capacitance seen at the input of each stage is given by:

$$C_{effec,X} = C_{P,X} + (1 - A)C_{M,X} \tag{2.11}$$

[5] Miller effect is when a capacitor is connected between the input and output of a high-gain inverting amplifier, appearing to be much larger at the input than it actually is.

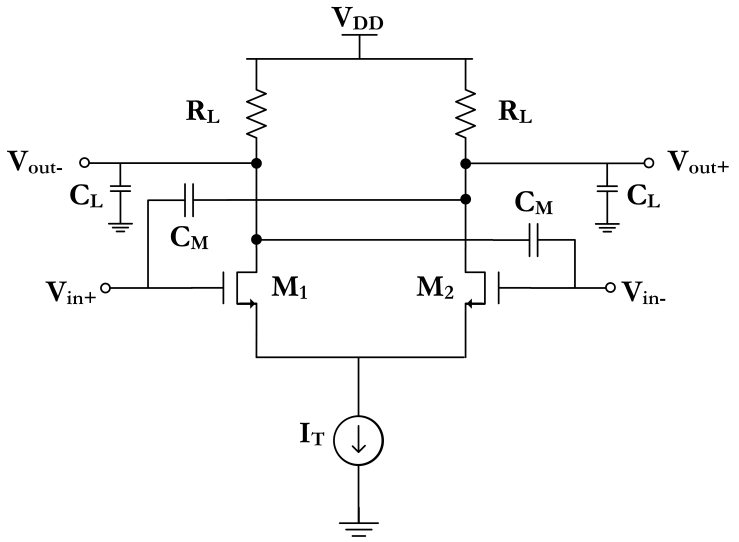


Figure 2.15: Gain stage with Negative Miller Capacitance.

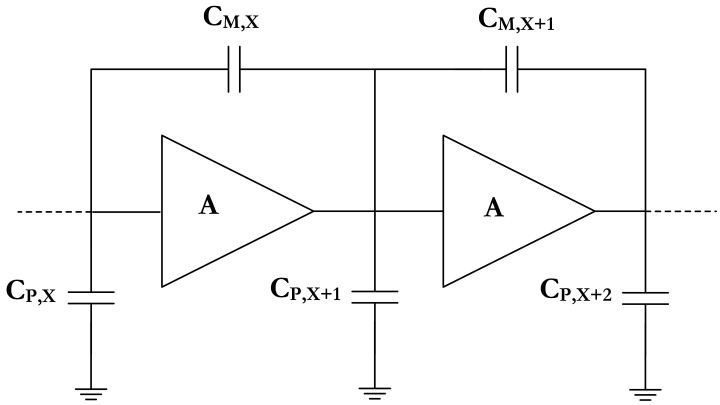


Figure 2.16: Two-stage amplifier with negative miller capacitors.

This means that if A is bigger than 1, the Miller capacitance - $(1-A)C_{M,X}$ - becomes negative, decreasing the effective capacitance seen at the input node and therefore reducing the load effect in the preceding stage and increasing the bandwidth.

The problem with this technique is that it is normally used to cancel the gate-drain overlap capacitance, which in deep submicron technologies working at high speed, tends to be smaller than 50 fF, making it difficult to create a capacitor that could accurately equal this value.

References [14], [15] and [13] are examples of the utilization of this technique in LAs.

2.1.4.4 Miller-Effect Suppression using Cascode Transistor

In a source-coupled differential pair, which AC half-circuit is illustrated in Fig. 2.17, the Miller effect is responsible for bringing the input pole to lower frequencies, making it the dominant pole, thusly limiting the bandwidth. As demonstrated in [16] Chapter 4, the dominant pole is given by:

$$\omega_p = \frac{1}{R_s(C_{gs} + C_{gd}(1 + g_m R_L))} \tag{2.12}$$

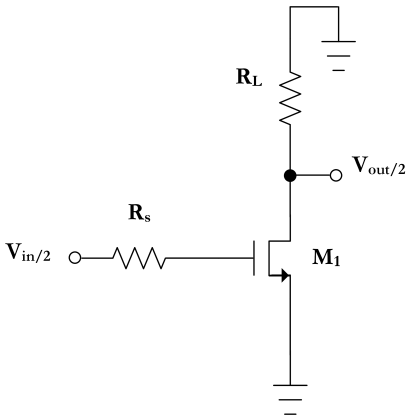


Figure 2.17: AC half-circuit of a source-coupled differential pair.

Miller effect increases the gate-drain overlap capacitance by $1 + g_m R_L$, this effect is more critical for high voltage gain amplifiers. One way to mitigate this effect is using cascode transistors, as depicted in Fig. 2.18.

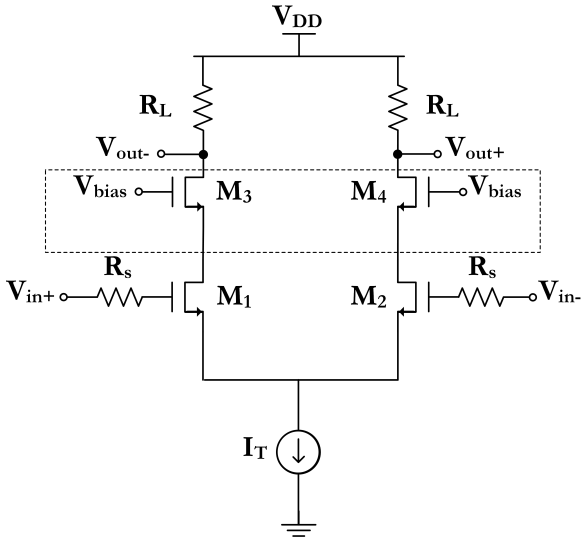


Figure 2.18: Source-coupled differential pair with cascode transistors.

To understand this technique let us consider the left equivalent AC half-circuit of Fig. 2.18. The impedance seen from the source of the cascode transistor M_3 is essencially $\frac{1}{g_{m3}}$, which means that the voltage gain from the input to M_1's drain is $\frac{g_{m1}}{g_{m3}}$. If M_1 and M_3 have equal dimensions, this value is equal to 1, and the capacitance perceived by the input would be smaller and given by the following expression:

$$C_{in} = C_{gs} + C_{gd}\left(1 + \frac{g_{m1}}{g_{m3}}\right) \tag{2.13}$$

If M_1 is equal to M_3 then expression 2.13 can be approximated to $C_{gs} + 2C_{gd}$. This value being much smaller than the one in a normal source-coupled differential pair, therefore killing the Miller effect. This way, the load effect in the preceding stage is reduced, allowing for an increase in the system's bandwidth. This practice has two major disadvantages: the decrease in the voltage headroom - which makes it hard to implement for low supply voltages - and the addition of a high frequency pole by transistor M_3.

Reference [17] shows an example of utilization of a cascode structure in a output stage for a power amplifier in 250 nm SiGe BiCMOS technology. In reference [18] a cascode structure is used in a pre-amplifier (equivalent to a transimpedance amplifier) for an Optical Receiver, decreasing the input capacitance.

2.1.4.5 Cherry-Hooper Amplifier

The Cherry-Hooper amplifier takes advantage of local feedback to improve speed which is a suitable solution for wideband multi-stage amplifiers. It allows for an independent tuning of the gain and bandwidth of the amplifier. Its basic architecture is composed by two stages, the first one converts the input signal to a current and the second one, that has a shunt feedback resistor, converts that current into a voltage. Fig. 2.19 a) shows a single-ended version of a Cherry-Hooper amplifier.

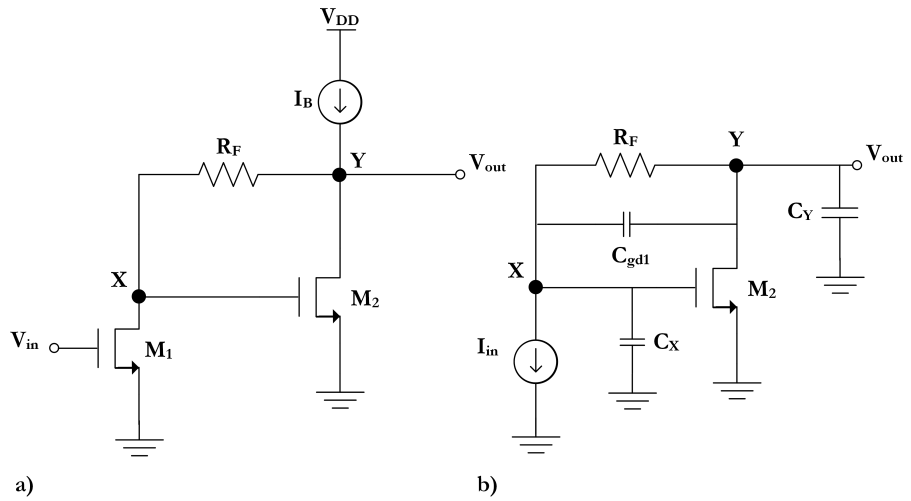


Figure 2.19: Single-ended Cherry-Hooper amplifier: a) complete b) simplified. Adapted from [7], Chapter 5.

By observation of Fig. 2.19 a) it is possible to comprehend that the feedback path is established by resistor R_F that senses the voltage at the output node, Y, and "responds" with a proportional current to node X. One should note that there are two paths to the output, one through M_2 and the other through R_F, which means that it is important to minimize the signal flowing through the feedback resistor, since it opposes the one created by M_2.

Let us consider a simplified schematic of the circuit, as represented in Fig. 2.19 b). Where I_B is considerer an ideal current source (infinite impedance) and I_{in} represents the drain current of transistor M_1. It is possible to determine the two poles of this circuit, as demonstrated in [7], Chapter 5 (assuming they are equal):

$$\omega_{p1} = \omega_{p2} = \frac{2g_{m2}}{C_X + C_Y + g_{m2}R_F C_{gd2}} \tag{2.14}$$

So, these poles will be in much higher frequencies than the ones without feedback, $\omega_{p1} = (R_F C_X)^{-1}$ and $\omega_{p2} = (R_F C_Y)^{-1}$, since R_F is typically much larger than g_{m2}^{-1}. Although differential Cherry-Hooper structures allow for high frequency operation it struggles with low supply voltages.

References [19], [20], [4] and [13] are examples of the utilization of this circuit topology in multi-stage amplifiers. Reference [19] presents an architecture of a modified Cherry-Hooper with source-follower feedback (the feedback path is implementd by a source-follower instead of a simple resistor) fabricated in a 0.35 µm CMOS technology. They were able to obtain a gain of 9.4 dB and 880 MHz bandwidth while consuming 6.0 mA from a 3.3 V supply.

2.1.4.6 Gilbert Gain Cell

The Gilbert Gain cell was invented by Barrie Gilbert in 1968, and was developed to be specifically used in cascaded amplifiers as a gain cell. The purpose was to develop a cascadable circuit form (a "gain cell") that could provide DC-coupled temperature-insensitive sub-nanosecond current gain with the virtual absence of voltage swings, and theoretically perfect transfer function characteristic [21]. The Gilbert gain cell is represented in Fig. 2.20 (with Bipolar Junction Transistors).

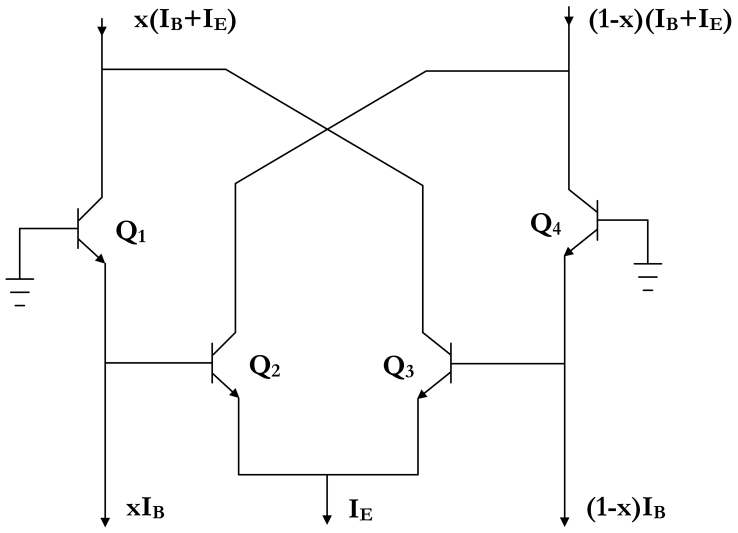


Figure 2.20: Gilbert gain cell. Adapted from [21].

This topology has many advantages. First, the "inner" stage can operate with a voltage gain smaller than 1, yet the outer stage can achieve a gain greater than unity. Also, this cell is perfectly suited for cascade assemblies, since the output of one stage can directly drive the next. And lastly, the bias voltage circuit for each stage has to supply only the base current for that stage, which is not signal dependent. Therefore, this cell may be used in low-power applications where 0.5/1V is sufficient.

Reference [22] is an example of this circuit's employment as a Variable Gain Amplifier (VGA) inserted in a Automatic Gain Control block to be used in an 3.3 GHz Optical Receiver implemented in standard 0.18 µm CMOS.

2.1.4.7 Inverse Scaling Technique

Inverse Scaling is a technique where the dimensions of the transistors (the $\frac{W}{L}$ ratio) and the tail current are scaled down from one stage to the other, whereas the load resistor's dimensions are scaled up. Fig. 2.21 illustrates this procedure.

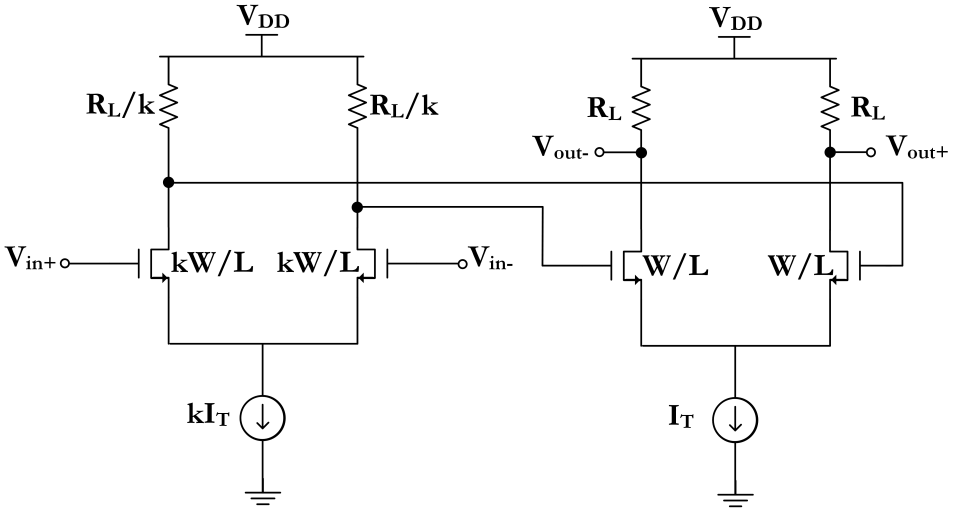


Figure 2.21: Inversely scaled differential pairs (by a factor of k).

This technique concedes an increase in the bandwidth while keeping the GBW constant. This is because the GBW of each stage is defined as $\frac{g_m}{C_{tot}}$ where C_{tot} is the load capacitance of each stage [5]. By reducing the dimensions of the driven stage (compared to the driving stage) the transconductance is reduced by the scaling factor , k - as are the input capacitances - thus diminishing the load effect in the previous stage, and enabling a bandwidth enhancement.

In reference [11] this technique is used in a Limiting Amplifier cascade for a 3 GHz Optical Receiver implemented in a 0.25 µm CMOS process. A cascade of 4 gain stages scaled by a factor of 2 allowed a reduction in the power consumption by about 50% without compromising the noise and offset characteristics of the amplifier (this is because

the noise and offset are mainly moduladed by the first amplifying stage, which is not scaled).

2.1.4.8 f_T Doublers

As mentioned before - in a cascade of identical amplifiers - the load effect from a certain stage exerted in the previous one is the most limiting factor when it comes to the overall system's bandwidth. Mainly for Output Buffers that must provide large currents to off-chip loads. f_T[6] Doublers are a way to reduce the input capacitance of an amplifier without altering the corresponding voltage gain. Fig. 2.22 illustrates this circuit (considering that all the transistors have the same dimensions).

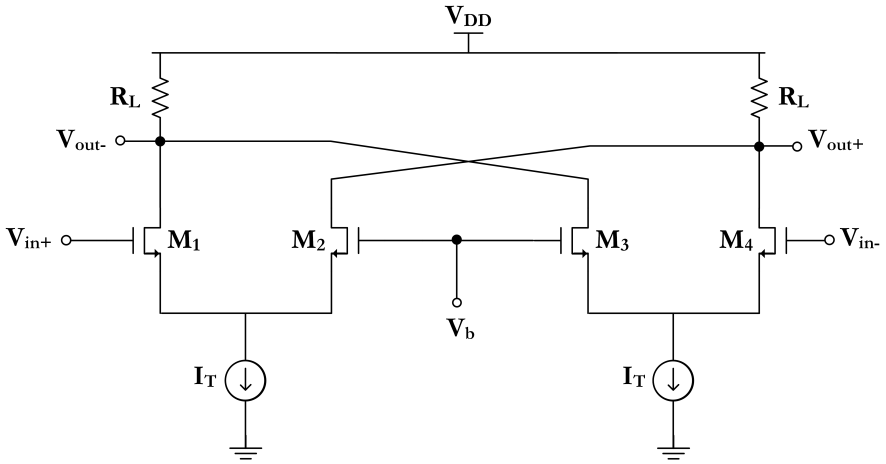


Figure 2.22: f_T Doubler. Adapted from [7], Chapter 5.

One can see that the small signals' gain remains the same as in a source-coupled different pair, but the input capacitance is reduced by half of its value. Let us consider the left half of the f_T Doubler, as represented in Fig. 2.23. In a small signals' analysis, only one of the transistors, M_1 in this case, has an AC signal at its gate. Whereas the other one, M_2, has its gate grounded. Therefore, the effective capacitance seen from the gate of transistor M_1 is the series connection of the two identical parasitic capacitances, C_{gs}.

The input capacitance is reduced to $\frac{C_{gs}}{2}$ and that is why this circuit is called f_T Doubler, because the transit frequency will double its value (ignoring the gate-drain parasitic capacitance).

Reference [13] uses an f_T Doubler to drive the output load for measurement purposes in a wideband RF-VGA using 0.13 µm CMOS. The former architecture also uses off-chip

[6]The f_T (transit frequency) of a transistor, is intended to provide some measure of the maximum operating frequency at which a transistor might be proven useful (that is, no longer producing any gain). It is the most common (though not the only) measure of transistor intrinsic speed. As with intrinsic gain, it is measured in the common-source configuration because of its broad relevance to both analog and digital design. It may be defined as $f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})}$.

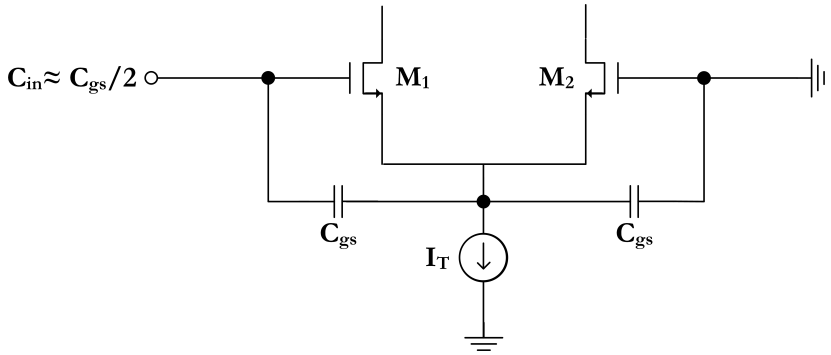


Figure 2.23: Input capacitance of f_T Doubler. Adapted from [7], Chapter 5.

inductors to enhance the bandwidth, the main disadvantage being power dissipation, which is 10 mA. The power dissipation of this kind of circuits is doubled when compared to the normal source-coupled differential pair, also, the currents that flow through the load resistors are doubled which can possibly put the transistors into triode region. Reference [14] also uses a f_T Doubler as an Output Buffer for a 3.125 GHz Optical Receiver implemented in a 0.18 µm CMOS process.

2.1.4.9 Comparison of Techniques and Referenced Topologies

This part aims to sumarize the set of broadband techniques presented in this Section as well as compare the performances of the different referenced topologies (where some of this techniques where used).

Table 2.1 presents a brief summary of the main characteristics of each one of the bandwidth enhancement techniques presented in this Section, namely their strengths and weaknesses. It helps to understand which one of the techniques is suitable for different applications with different requirements.

Table 2.2 compares the performance parameters of different state of the art topologies referenced along this work.

Table 2.1: Comparison of bandwidth enhancement techniques.

Technique	Advantages	Drawbacks/Issues
Inductive Peaking (Active Inductor)	Transistors can replace inductors; Low chip area	Voltage Headroom; Gate oxide stress; Non-flat frequency response
Inductive Peaking (Passive Inductor)	High Q; Low noise; Almost no voltage headroom consumption	Area; Non-flat frequency response
Capacitive Degeneration	Easy implementation	Gain reduction
NMC	Kills the Miller Effect (reduces the loading effect)	Voltage Headroom; High frequency pole added by the cascode
Cherry-Hooper Amplifier	Easy implementation	Gain reduction; Technique is not of much use when working in large-signal operation
Gilbert Gain Cell	Low power consumption; The output of one stage can directly drive the next	Large headroom consumption
Inverse Scaling	Reduced power consumption; Constant GBW	Noise increase
f_T Doublers	The voltage gain remains the same; Suited for Output Buffers	Power dissipation; Output capacitance is doubled

Table 2.2: Comparison of referenced LAs/VGAs.

Reference	**Process** [µm]	**BW** [GHz]	**Gain** [dB]	**Input Sensitivity** [mV_{pp}]	**Supply Voltage** [V]	**Power** [mW]
[9]	0.18	4.5	32	20	1.62-1.98	12.15-14.85
[10]	0.18	1.8	44	2	1	3.7
[8]	0.6	1.25	40	5	5	130
[4] ■	0.13	5	40	N/A	2.5	47
[11]	0.25	2.5	32	2.2 ♦	2.5	53
[13]	0.13	0.8-3	35	N/A	1.2	32
[14]	0.18	3.125	45	5	1.8	95
[15]	0.9	34.7	32	N/A	1.2	97
[19]	0.35	2.1	39	N/A	1.8	79.2
[20]	0.18	6.8	26	25	3.3	45

■ Radiation-tolerant;
♦ For a BER of 10^{-12}.

2.1.5 Offset Cancelation Techniques

Often, specially in high gain amplifiers, it is necessary to include some offset cancelation block, in order to avoid saturation of the amplifier's output swing by undesired low frequency components. The offsets in differential stages may be originated by device mismatch, low-frequency noise contributions, and drift due to thermal variations. An external feedback loop or AC coupling between the LA's stages can be the solution to these problems (allowing a pass-band frequency response instead of a low-pass). Some offset cancelation techniques will be further discussed in this part. Note: altough the Offset Cancelation Block is not part of this thesis it is mentioned in this study due to its importance for the correct operation of the LA.

2.1.5.1 AC Coupling

AC coupling consists of using a high-pass circuit to filter out the undesirable DC components. Normally, AC coupling is placed between LA's stages. This circuit is depicted in Fig. 2.24. This circuit exhibits high-pass behaviour, as demonstrated by its transfer function:

$$H(s) = \frac{sRC}{1 + sRC} \tag{2.15}$$

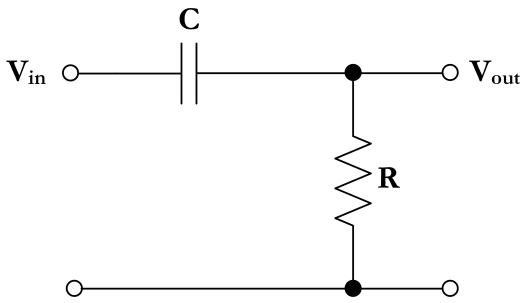


Figure 2.24: AC coupling circuit.

One can see that this high-pass function filters the frequency components below the cut-off frequency $f_c = \frac{1}{2\pi RC}$. This frequency has to be carefully chosen, since it cannot be lower than the signal frequency when the bit pattern is a sequence of zeros or ones. In order to have a low cut-off frequency, it is necessary to have a large RC product. Sometimes to achieve a sufficiently large RC product it is necessary to have large capacitors which cost a lot of chip area. This is the main disadvantage of this offset compensation technique. Furthermore, the parasitic resistance and capacitance of the large coupling capacitors deteriorates signals at higher frequencies. In reference [13], AC coupling is placed between the pre-amplifier and the VGA to compensate for the difference in the DC operating points.

2.1.5.2 Feedback Loop

This technique consists in doing a feedback loop, where the feedback loop transfer function is given by a single pole low pass filter, which can be implemented by an RC circuit. The block diagram representative of this technique is presented in Fig. 2.24.

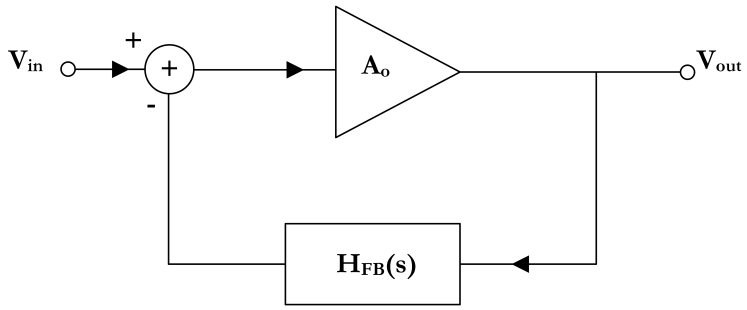


Figure 2.25: DC offset cancelation loop. Adapted from [12].

Where $H_{FB}(s)$ is the transfer function of the low pass filter and A_o is the gain of the auxiliary amplifier. The RC filter will sense the DC offset and cancel it via the feedback loop with the auxiliary amplifier. The resulting closed loop transfer function will exhibit high pass behaviour, thusly filtering the low frequency components. Like AC coupling, in order to have a low cut-off frequency, it is necessary to have a large resistor or a large capacitor which enlarges the chip size. An alternative would be using off-chip resistors, or capacitors needing an aditional pin and increasing the total application dimension. One should be aware that using an external feedback loop can bring stability issues, specially in high frequency circuits.

Reference [23] shows an implementation of a continuous time feedback for DC offset cancellation in a VGA. For the implementation of the RC filter, and in order to minimize the chip area, the Miller effect and a linear range operation MOS transistor were used to realize a large-value floating capacitor and resistor, respectively. They were able to obtain a high pass cut-off frequency of 500 Hz and a DC offset of 2 mV at the output of the VGA.

References [8] and [10] are examples of utilization of low frequency feedback loops for DC offset cancelation in Limiting Amplifiers.

2.1.5.3 Feedforward Offset Removal

Another way to cancel the offset is to isolate the DC component using a low pass RC filter, and using this signal as a common-mode signal for an amplifier. If this amplifier uses a differential pair as an input stage, then the DC offset will be strongly atenuated due to the high Common-Mode Rejection Ratio (CMRR) - characteristic of the differential pair - that results in a high pass filter with a cut-off frequency of $\frac{1}{2\pi RC}$. This technique also implies the use of large resistors and capacitors occupying a lot of chip area.

In reference [14], a feedforward-type offset cancellation is used in 3.125 GHz Limiting Amplifier for an Optical Receiver system fabricated in a commercial 0.18 µm CMOS process. One advantage is that the feedforward approach possesses instantaneous response for offset cancellation process.

2.2 Output Buffer with Pre-emphasis Capability

As mentioned before, Output Buffers are necessary to drive off-chip loads with suficiently large output swings, in order to minimize the reflections in the line which result in ISI.

A commonly used topology for Output Buffers in high speed optical links is the "open-drain" differential pair. This achitecture is depicted in Fig. 2.26.

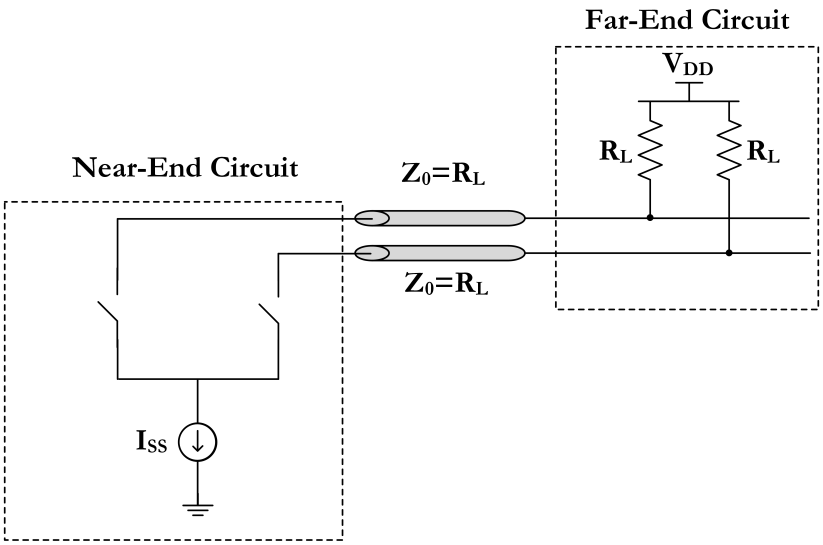


Figure 2.26: "Open-drain" Output Buffer, transmission line and off-chip load.

The circuit generates a differential current that is absorbed by the load resistor at the far end. This circuit creates a voltage swing of $I_{SS}Z_0$ where Z_0 is equal to the load resistor R_L to provide impedance matching, and producing no reflected signal. The signal then travels through the line, reaching the loads after some delay, ΔT.

Reference [13] uses an "open-drain" f_T Doubler to drive off-chip loads in a wideband RF-VGA implemented in 0.13 µm CMOS. References [19] and [4] are examples of differential pair Output Buffers' implementations.

Sometimes, the line has a low-pass behaviour, so it is necessary that the buffer has Pre-emphasis capability. Otherwise, it can cause significant ISI in the received signal, creating difficulties for the CDR and consequently increasing the BER. Fig. 2.27 illustrates this phenomenon.

Pre-emphasis function consists in amplifying the high frequency components of the signal more than the low-frequency components (equalisation), improving the signal's

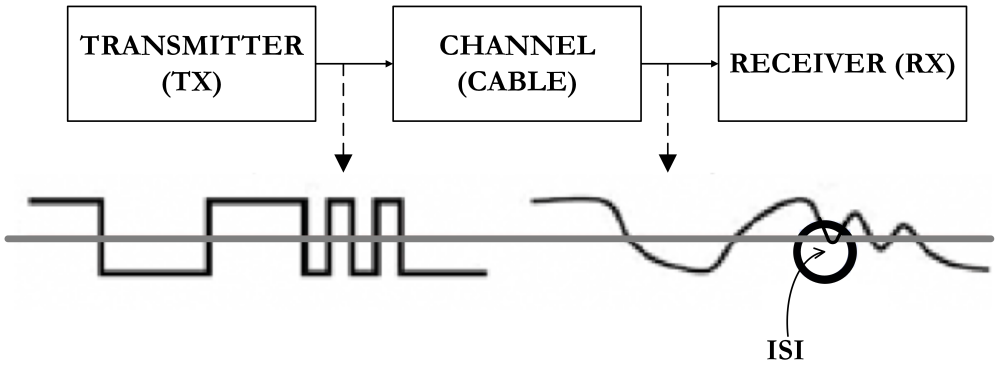


Figure 2.27: Effect of low-pass line in an electrical signal resulting in ISI. Adapted from [24].

integrity. This can be done, for example, with a simple high-pass filter or by emphasizing transitions and deemphasizing "no transitions". Fig. 2.28 illustrates a Pre-emphasis function done with the second method.

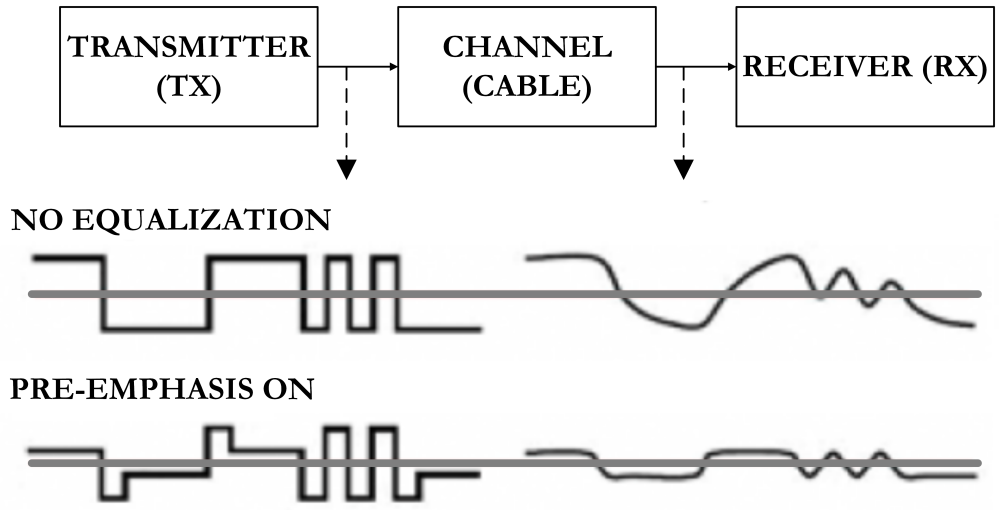


Figure 2.28: Signal with and without Pre-emphasis. Adapted from [24].

Reference [25] presents a Pre-emphasis circuit that detects the transition edge of the input signal, and generates a boosted current on the rising and falling edges. When there are no data transitions, the circuit produces no extra current. This circuit was used in a Laser Diode Driver, and implemented in a 0.35 µm CMOS digital process. This architecture is equivalent to a first order high-pass gain and allows for the equalisation of the low-pass filtering caused by packaging and parasitic capacitances. In addition, the "boost" current and the delay time are tunable to adjust the Pre-emphasis magnitude

under different working ambiences.

2.3 Received Signal Strength Indicator and Squelch

The Received Signal Strength Indicator is a block used to estimate the received signal strength/power. Its output it usually used to adjust the transceiver's gain and improve the SNR (in a certain way, this can be seen as a feedback loop across the entire communication channel, where the transceiver adjusts its power according to the received signal's power). This circuit is commonly realized in a logarithmic form because the wide dynamic variation of the received signal can be represented within a limited indication range.

A commonly adopted architecture for the RSSI is based on sucessive-detection [26]. Basically, it is composed by several Full-Wave Rectifiers (FWR) and a low-pass filter, which are in combination with the Limiting Amplifier. It is based on a piecewise linear approximation, each piece of the linear section is obtained by rectifying the signal from each stage of the Limiting Amplifier. Then, the rectified waves are summed and low-pass filtered to obtain a DC indicating voltage representative of the received signal's strength.

In addition to this block, it is interesting, for industrial and commercial applications, to a have a Squelch function, which is used to "mute" the receiver (turn off the output) when no signal is being sent, therefore supressing the output toggling due to noise. This can be achieved using the indicating signal created by the RSSI, comparing it to a predefined threshold value, and forcing the output value to be constant.

Reference [27] presents a Squelch circuit where the Output Buffer is turned ON or OFF, by a control signal (generated by the RSSI). When the input signal is lower than the set-up threshold, the level detector activates a Loss-of-Signal indicator that is used by the Squelch to automatically force the output to a logic 1, and no data is propagated through the system.

2.4 Radiation Effects on CMOS Technology

In order to o use microelectronics' circuits in High Energy Physics (HEP) experiments they need to be hardened against the radioactive environment in which they are inserted. Therefore, it is of the greatest importance to study the radiation effects in modern CMOS process. These effects are divided into two main types:

- Total Ionizing Dose Effects
- Single-Event Effects

The former are caused by continued exposure to radiation, and are characterized by permanent changes in electronic devices. The latter are exceptional isolated events caused when a high-energy particle strikes a p-n junction.

This Section aims to succinctly explain some of these effects and discuss some state of the art techniques to make the circuits radiation-hardened.

2.4.1 TID Effects on Modern CMOS Process

TID radiation effects on CMOS devices are mainly related to the ionization in the oxides and the consequent effects of this ionization. This phenomenon has a large impact, specially in the gate oxides (which can result in the deterioration of some of the transistor performance parameters), in the transistor edges (causing leakage current between two adjacent transistors), and in the isolation oxides resulting in loss of interdevice isolation.

2.4.1.1 Gate Oxide Effects

The TID irradiation effects on the gate oxide of a Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET) biased positively at the gate electrode can be understood as a four-step process [28]. The four "stages" are illustrated in Fig. 2.29.

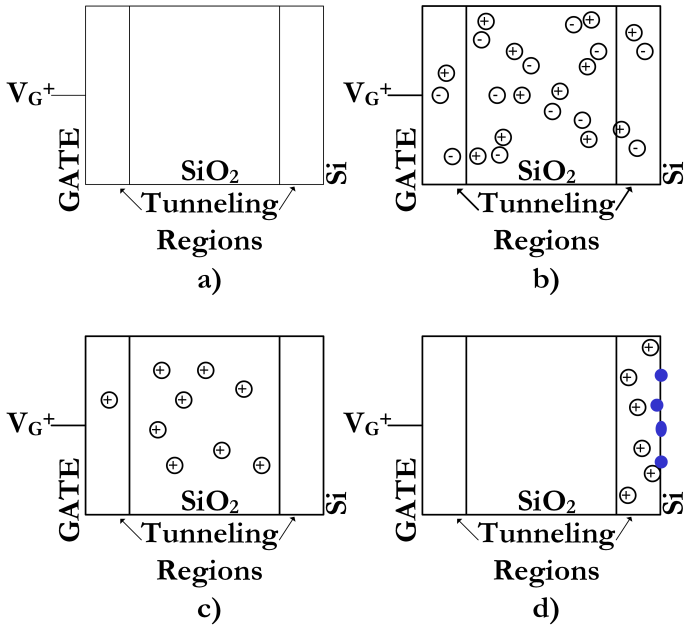


Figure 2.29: Charge distribution in a gate oxide at three times after exposure to a pulse of irradiation at t = 0 for a thick gate oxide. (a) $t = 0^{-}$, (b) $t = 0^{+}$, (c) $t = 0^{++}$, and (d) $t \gg 0^{++}$. Adapted from [28].

In the first step, the energy particle incides in the oxide, ionizing the lattice atoms, creating electron-hole (e-h) pairs. As it passes through the solid, the particle loses energy at a constant rate due to inelastic Coulomb scattering (Fig. 2.29 b)). At the gate oxide, a fraction of these e-h pairs will recombine, the remaining electrons and holes are separated by the applied electric field (the amount of recombination is dependent from the concentration of the e-h pairs). Due to the high mobility of electrons, they will move towards the gate and get out through the metal contact. Holes, on the contrary, have

low mobility, and are transfered to the Si/SiO_2 interface via a complicated trap-hopping mechanism. At this time, the only charges remaining in the gate oxide are holes. Some of the remaining holes are trapped in the gate oxide (these trapped positive charges can be neutralized over time by electron tunneling from the silicon, for example) allowing for a significant recovery) creating a net positive charge, and others will move to the Si/SiO_2 where they will create an interface trap. Note: the transport of the remaining holes is highly disseminated in time, occuring over many decades after the radiation pulse.

Some of the holes may be trapped within the oxide, leading to a net positive charge, others may move to the Si/SiO_2 interface, where they can create an interface trap by capturing electrons (Fig. 2.29 d)). For NMOS transistors, the interface states act as negative charges in the gate-oxide of a NMOS transistor, or positive charges in the gate-oxide of a PMOS transistor.

This new "parasitic" charges, in gate oxide and/or at the gate-oxide/silicon interface cause a shift in the MOSFET threshold voltage (ΔV_T), affecting device's performance. This shift in the threshold voltage is calculated by integrating the additional charge density, ρ, over the oxide thickness, t_{ox} [28]:

$$\Delta V_{ot,it} = \frac{-1}{C_{ox} t_{ox}} \int_0^{t_{ox}} x\rho(x)dx \tag{2.16}$$

Where ΔV_{ot} is the voltage shift due to radiation-induced trapped-hole and is always negative (for both NMOS and PMOS transistors). And ΔV_{it} is the voltage shift due to the interface-state charge being negative for PMOS transistors and positive for NMOS transistors. The total radiation-induced drift in threshold voltage for a given transistor will be the sum of ΔV_{ot} and ΔV_{it}.

For a MOSFET:

$$\Delta V_T \propto \frac{\Delta Q_T}{C_{ox}} \propto t_{ox}^2 \tag{2.17}$$

Where ΔQ_T denotes the total oxide trapped charge composed by ΔQ_{ot} and ΔQ_{it}. Relation 3.2 suggests that, if the technology continues to shrink endlessly, the threshold voltage shifts would also decrease to lower and lower values as the square of the oxide thickness, but this is not entirely true since, when the oxide thickness is comparable or smaller then the characteristic tunneling length for the holes, the shift in the threshold voltage will be negligible.

2.4.1.2 Radiation-Induced Leakage Currents

The continuous scaling of CMOS technology allows a proportional scale in the thickness of the gate oxide, reducing the probability of TID effects. However, the thick Field Oxides (FOX) used to electricly isolate devices from each other are not able to scale as progressively as the technology does, featuring a thickness range between 100 and 1000 nm. Thus, being much more susceptible to ionizing radiation effects. In an NMOS device,

positive charges (holes) get trapped in the field oxide (by the process explained before) and since the substract is P-type, they invert the underlying P doped region forming a conducting channel. Creating two conductive paths (under the region called "bird's beak"[7]), Fig. 2.30, that resemble parasitic transistors placed in parallel with the main device, altering the effective transistor's width.

This phenomenon does not affect PMOS devices since the N-type substrate cannot be inverted by the positive trapped charge [29].

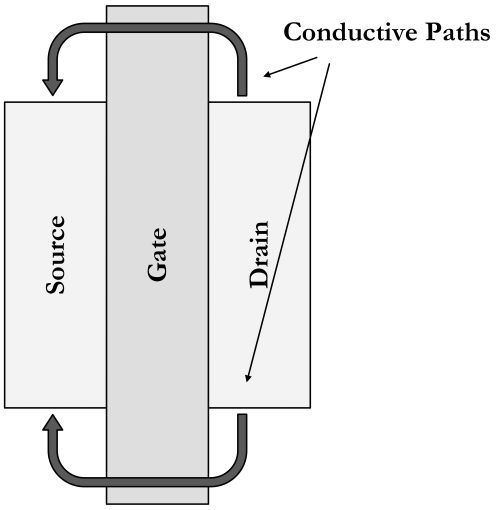


Figure 2.30: Parasitic conductive paths.

The small parasitic transistors increase the drain current, due to the superposition of all the current contributions and can scale the drain current up to several orders of magnitude. This also results in a shift in the effective threshold voltage, sometimes large enough to create a source-drain current in the transistor at OFF state ($V_G = 0$). Fig 2.31 illustrates the decrease of the threshold voltage and the consequent increase of the subthreshold current.

Another contribution from radiation-induced leakage currents is the loss of interdevice isolation. This is due to the fact that leakage parasitic paths are created between adjacent transistors (for example, between the n+source/drain of two adjacent NMOS transistors) resulting in interdevice leakage. This can result in signal corruption, reduced margins, and additional supply current.

[7] The bird's beaks are present in CMOS technology when the isolation between devices is done employing Local Oxidation of Silicon (LOCOS). In deep submicron technologies this isolation has been replaced by Shallow-Trench Isolation (STI). However, this new kind of isolation does not prevent the formation of post-irradiation conductive paths [24].

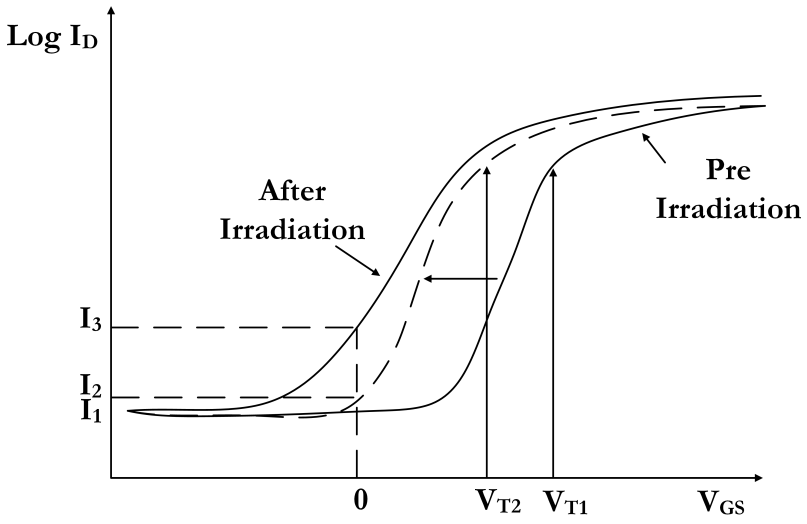


Figure 2.31: Increase of the subthreshold current in a NMOS as consequence of the decrease of the effective threshold voltage.

2.4.1.3 Hardness-by-Design Techniques to Mitigate TID Effects in Modern CMOS Process

Hardness-by-Design is a method for designing radiation-tolerant microelectronic components without the use of special manufacturing processing techniques (Hardening-by-Process). In this Section, some design techniques used to mitigate TID effects will be addressed.

As explained in Section 2.4.1.2, when a NMOS device is irradiated, positive charges build up in the FOX, inverting the P-doped substract and forming parasitic condutive channels along the FOX sidewalls. One simple solution to this problem is using an enclosed layout. This arrangement is illustrated in Fig. 2.32.

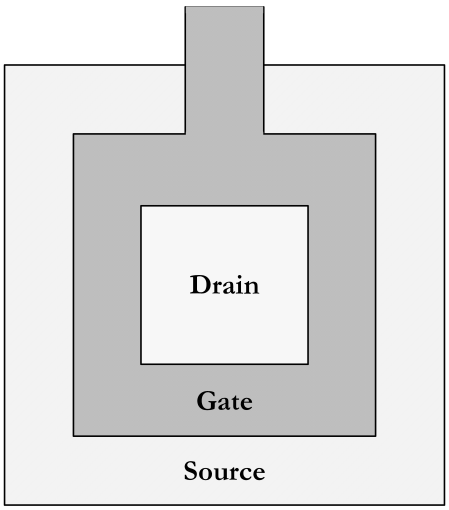


Figure 2.32: MOSFET with an enclosed layout.

Using this approach, no parasitic conductive path can be formed between the source

and the drain, since there is no thick oxide layer running along the main channel. This creates an "edgeless" transistor, therefore eliminating the radiation-induced leakage currents. However, when compared to standard-edged transistors, edgeless transistors have increased gate and source/drain capacitances and also occupy more chip area than a regular transistor [28].

One efficient way to supress the radiation-induced interdevice leakage is using a p+ diffusion ring in the FOX between two adjacent NMOS transistors, which is illustrated in Fig. 2.33. This structure avoids the inversion of the p+ substract by increasing the local threshold voltage (the electric field necessary to draw the negative charges from the substract is higher, since the distance increased). Since the p+ diffusion ring must surround a transistor, the correspondent area penalty will depend on the design of the transistor (standard-edged, edgeless, etc) that is being surrounded, as well as the number of transistors enclosed by a single ring [28].

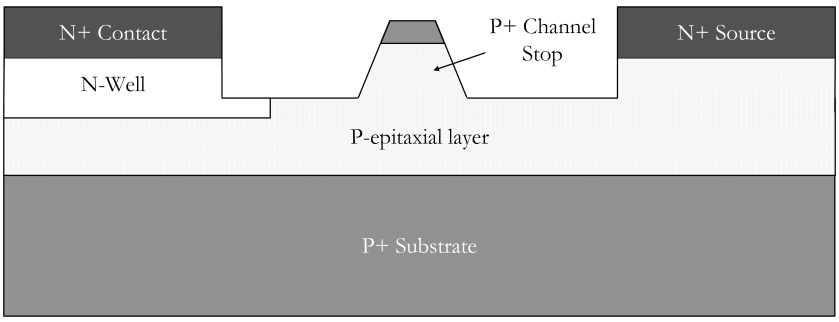


Figure 2.33: Cross-section of a CMOS process with a p+ channel stop designed into the FOX isolation. Adapted from [28].

These are two examples of commonly used techniques for mitigating TID effects on modern CMOS technologies in radioactive environments.

CHAPTER 3

IMPLEMENTATION IN CMOS

3.1 Limiting Amplifier

3.1.1 Modelation

Before presenting the architecture chosen for each Limiting Amplifier's gain cell (assuming an open-loop configuration of cascaded gain stages), let us analyse in more detail the bandwidth enhancement techniques used to improve the broadbrand response of the LA. Namely, capacitive degeneration and negative Miller capacitance. Note: All the figures with NMOS and PMOS with undefined bulk have their bulk connected to ground and V_{DD}, respectively.

3.1.1.1 Capacitive Degeneration

Let us consider the equivalent half-circuit of a capacitive degenerated differential pair, represented in Fig. 3.1. Where G_m represents the effective transconductance, which is expected to be increased at higher frequencies due to the placing of a new zero, and therefore compensating the gain roll-off due to the dominant pole, as mentioned in Section 2.1.4.2. The goal is to cancel out the dominant pole by placing the zero at the exact same frequency (extending the bandwidth up to the transconductance's pole) which would give the maximum bandwidth extension without any frequency peaking - which could potentially degrade the time response of the amplifier.

Analysing the small signals' equivalent of the circuit in Fig. 3.1 it is possible to write the following relations:

$$\begin{cases} i_{out} = g_m \cdot v_{gs} \\ v_{gs} = V_{in} - \left(\frac{R_s}{2} // \frac{1}{2 \cdot s \cdot C_S}\right) \cdot i_{out} \end{cases} \tag{3.1}$$

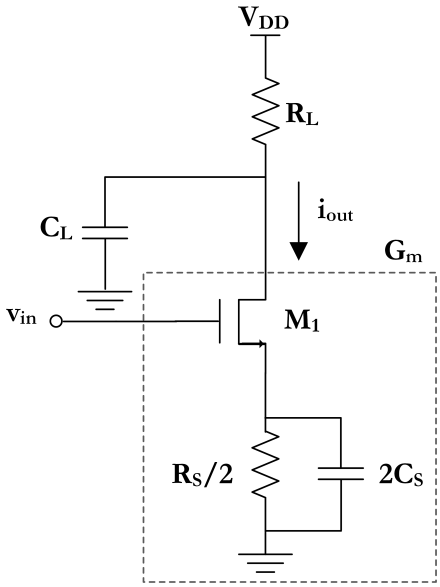


Figure 3.1: Equivalent half-circuit of a capacitive degenerated differential pair.

Where i_{out} is the drain current, v_{gs} is the gate to source voltage and g_m is the transconductance of transistor M_1. Solving the system equation in 3.1, it is possible to derive the expression of the equivalent transconductance, as well as the correspondent zero and pole.

$$G_m = \frac{i_{out}}{v_{in}} = \frac{g_m(R_S C_S s + 1)}{R_S C_S s + 1 + g_m \frac{R_S}{2}} \tag{3.2}$$

$$w_z = \frac{1}{R_S C_S} \tag{3.3}$$

$$w_p = \frac{1 + g_m \frac{R_S}{2}}{R_S C_S} \tag{3.4}$$

It also can be useful to look at the overall transfer function of the circuit and not just the equivalent transconductance. Using the previous equations, by inspection, the transfer function of the capacitive degenerated differential pair is given by 3.5.

$$\frac{v_{out}}{v_{in}} = \frac{g_m R_L \cdot (R_S C_S s + 1)}{(R_L C_L s + 1)\left(R_S C_S s + 1 + g_m \frac{R_S}{2}\right)} \tag{3.5}$$

If the zero of the transconductance matches the dominant pole, given by $\frac{1}{R_L C_L}$ the $-3dB$ bandwidth of the circuit will be extended up to the transconductance pole. In order to satisfy this condition, the following relation must be obeyed: $R_L C_L = R_S C_S$. Thus, the bandwidth is extended by a factor of $m = 1 + g_m \frac{R_S}{2}$, which corresponds to the numerator of the expression of the transconductance pole. Obviously, this extension in the bandwidth comes with a proportional decrease in the DC gain, which is given by $\frac{g_m R_L}{1 + g_m \frac{R_S}{2}}$.

With the so far performed analysis, it seems that there is no advantage in using capacitive degeneration, since the same results can be accomplished by reducing the load resistance by the bandwidth enhancement factor, m. This is not exactly true, because the input impedance of a capacitive degenerated amplifier is smaller when compared to a simply resistive loaded differential pair, thus, reducing the load effect seen by the preceding stage, in a cascade of gain stages. To explain this subject, let us consider the circuit of Fig. 3.1 using a Thevenin's equivalent to represent the previous stage and including the C_{gs} capacitance (the gate-source parasitic capacitance), as represented in Fig. 3.2.

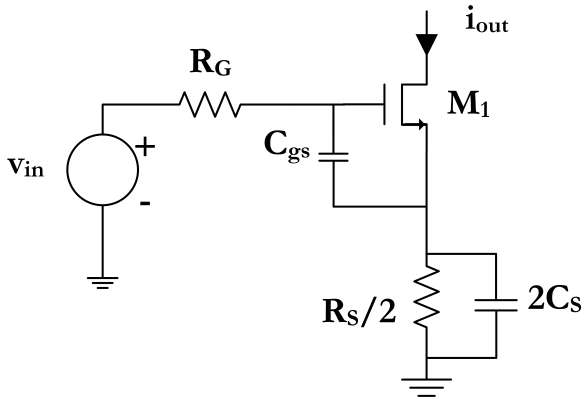


Figure 3.2: Equivalent half-circuit of the load effect created by a capacitive degenerated differential pair.

Considering the small signals' model of the circuit, one can see that $i_{out} = g_m v_{gs}$, thus, the current that flows through C_{gs} is given by $\frac{i_{out}}{g_m} C_{gs} s$ and the current through the parallel of the degeneration's capacitor and the degeneration's resistor is $\frac{i_{out}}{g_m} C_{gs} s + i_{out}$. Applying Kirchhoff's Voltage Law (KVL) from v_{in} to ground, is it possible to obtain the following equation in 3.6.

$$\frac{i_{out}}{g_m} C_{gs} s R_G + \frac{i_{out}}{g_m} C_{gs} s + \left(\frac{i_{out}}{g_m} C_{gs} s + i_{out} \right) \frac{\frac{R_S}{2}}{R_S C_S s + 1} = v_{in} \tag{3.6}$$

Solving 3.6 for I_{out} and dividing by v_{in} the following transfer function is obtained:

$$\frac{i_{out}}{v_{in}} = \frac{g_m (R_S C_S s + 1)}{R_G C_{gs} R_S C_S s^2 + \left(R_G C_{gs} + R_S C_S + \frac{R_S C_{gs}}{2} \right) s + 1 + g_m R_S / 2} \tag{3.7}$$

In order to estimate the dominant pole at the input node, it is useful to write the following equation:

$$\left(\frac{s}{w_{p1}} + 1 \right) \left(\frac{s}{w_{p2}} + 1 \right) = \frac{s^2}{w_{p1} w_{p2}} + \left(\frac{1}{w_{p1}} + \frac{1}{w_{p2}} \right) s + 1 \tag{3.8}$$

Assuming that $w_{p1} \ll w_{p2}$, which is a reasonable assumption since $g_m R_S$ is usually below 5 (otherwise the gain per stage would be very small), the previous expression simplifies to:

$$\left(\frac{s}{w_{p1}}+1\right)\left(\frac{s}{w_{p2}}+1\right)=\frac{s^2}{w_{p1}w_{p2}}+\left(\frac{1}{w_{p1}}\right)s+1 \tag{3.9}$$

Combining Eq. 3.7 and Eq. 3.9 an aproximmate expression for the dominant input pole is derived:

$$w_{p1}\approx\frac{1+g_mR_S/2}{R_GC_{gs}+R_SC_S+R_SC_{gs}/2} \tag{3.10}$$

Considering that R_GC_{gs} is much larger than $R_S\left(C_S+C_{gs}/2\right)$ then the expression of the input pole can be further simplied to $w_{p1}\approx\frac{1+g_mR_S/2}{R_GC_{gs}}$. This means that the input pole was also increased by a factor of m, proving that using capacitive degeneration offers a greater advantage in the extension of the bandwidth when compared to a proporcional reduction of the load resistance.

The ideal situation would be to match the transconductance zero to the dominant pole, otherwise, the step response would exhibit overshoot or undershoot, which is not desirable. This situation is represented in Fig. 3.3. Furthermore, there is a limit to which the bandwidth can be extended without adding any peaking[1] (which is the cause for the overshoot in the step response) to the frequency response. This behaviour is illustrated in Fig. 3.4. Up to a bandwidth enhancement factor of 2.5 the percentage of frequency peaking remains constant and equal to zero. These are the the situations where the zero is after the pole, still moving towards the pole or matching the pole. The percentage of peaking starts to increase abruptly for bandwidth enhancement values superior to 2.5, which means that the zero appears much before the pole.

Observing Fig. 3.3 one can see that, when the transconductance's zero matches the dominant pole, the step response presents zero overshoot and when the frequency of the zero is smaller than the frequency of the pole, the step response exhibits overshoot. The bandwidth enhancement factor, m, is 2.2 in the first case and 2.8 in the second case. Although it seems that the second case would be better, since it is the one with more bandwidth, the overshoot in the step response can be dangerous.

Let us now look at this situation more closely. Placing the zero before the pole means that the frequency response would exhibit some peaking. This translates into a difference in the voltage gain according to the frequency of the signal. This effect would not be harmful when working with deterministic single-toned signals. But, in the case of a Pseudo-Random Binary Sequence (PRBS), where the signal frequency varies with time, this is no longer true. The different amplification at different frequencies means that the signal will rise or fall from different voltage levels (according to the gain) which causes different rise and fall times for different signal frequencies, causing a possible variation of the zero crossings.

[1] Frequency peaking can be defined as the maximum magnitude value over frequency minus the DC gain or the relative error in relation to the DC gain in percentage.

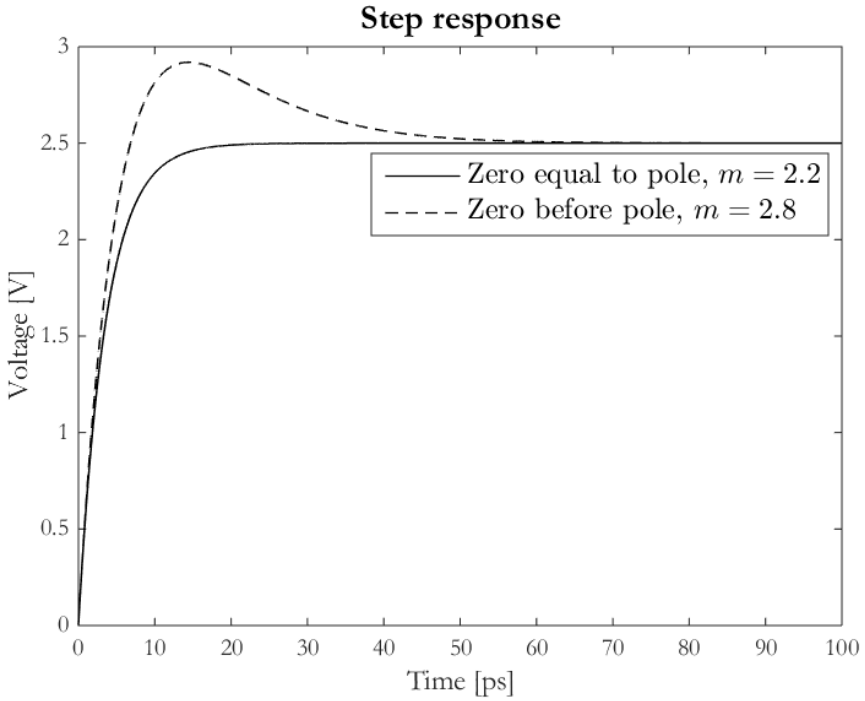


Figure 3.3: Step responses of a capacitive degenerated differential pair as a function of the transconductance's zero position - obtained using the mathematical model of Eq. 3.5

In order to better understand this effect, let us analyse the frequency response and the eye diagrams of the output signal for the first two cases for a PRBS at 5 Gb/s. When the zero is matched with the dominant pole, the frequency response presents zero peaking. When the zero is placed before the pole, meaning, larger C_S, the frequency response of the system presents about 1.5 dB (20%) of peaking, as presented in Fig. 3.5.

In order to have a better understading of this effect, let us analyse the correspondent eye diagrams, represented in Fig. 3.6 a) and b). One can see that in the second case, where the zero is placed before the dominant pole, although the -3 dB bandwidth is greater, the eye diagram looks worst. There is a deviation in the zero crossings, which is due to the existent the frequency peaking, resulting in deterministic jitter.
This effect translates into another major constrain in the design of the Limiting Amplifier, which is the need to minimise the frequency peaking to avoid these effects since the jitter requirement of the overall Optical Receiver needs to be below 0.3 UI (this value refers to the 6σ deviation). Also, this effect would be even more pronounced in a cascade of gain stages, which is the case of the Limiting Amplifier.

The previous analyses were done without much concern with the parasitic capacitances and the gate resistance (which has to be considered when designing high speed amplifiers). Let us now draw a more complete small signals' model for the equivalent half-circuit of capacitive degenerated differential. The small signals' equivalent is illustrated in Fig. 3.7.

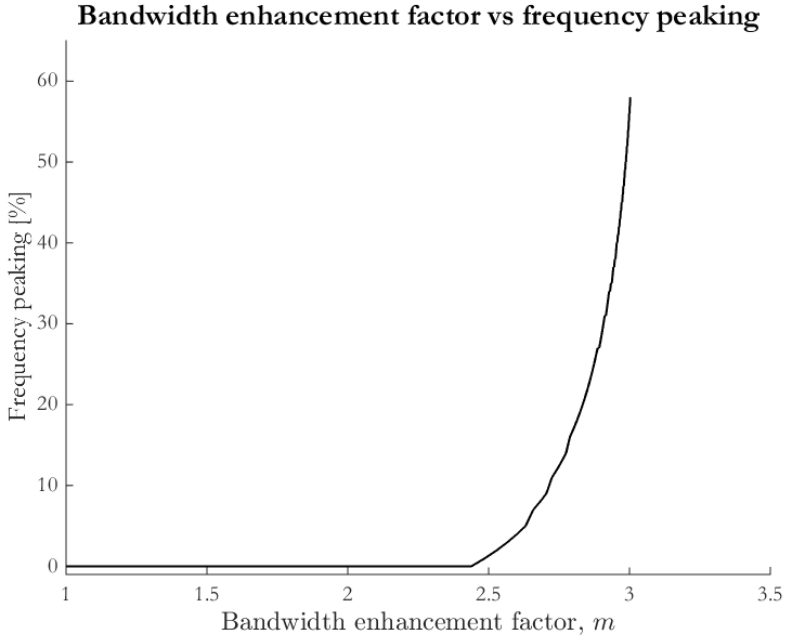


Figure 3.4: Tradeoff between the bandwidth enhancement factor, m, and frequency peaking - obtained using the mathematical model of Eq. 3.5.

Where C_{gd} is the gate-drain parasitic capacitance, C_{gs} is the gate-source parasitic capacitance, C_{ds} is the drain-source parasitic capacitance and C_{sb} is the source-bulk parasitic capacitance. R_g is the gate resistance and r_{ds} is the drain-source resistor of the transistor. V_{sb} is the source-bulk voltage and g_{mb} is the bulk's transconductance.

It is possible to define three nodes in the circuit, V_G, V_S and V_{out}. Aplying KCL to these nodes, the following equations are derived:

.

$$\begin{cases} \frac{(v_G - v_{in})}{R_g} + (v_G - v_S)\cdot s\cdot C_{gs} + (v_G - v_{out})\cdot s\cdot C_{gd} = 0 \\ (v_{out} - v_G)\cdot s\cdot C_{gd} + g_m\cdot(v_G - v_S) - g_{mb}\cdot v_S + \frac{(v_{out} - v_S)}{r_{ds}} + (v_{out} - v_S)\cdot s\cdot C_{ds} + \frac{v_{out}}{R_L} + v_{out}\cdot s\cdot C_L = 0 \\ -g_m\cdot(v_G - v_S) - (v_G - v_S)\cdot s\cdot C_{gs} - \frac{(v_{out} - v_S)}{r_{ds}} - (v_{out} - v_S)\cdot s\cdot C_{ds} + g_{mb}\cdot v_S + v_S\cdot s\cdot C_{bs} + \frac{v_S}{0.5R_S} + v_S\cdot s\cdot 2\cdot C_S = 0 \end{cases} \tag{3.11}$$

Due to the complexity of the model, it is difficult to solve the previous equations' system symbolically. It also does not provide a better insight of the circuit's behaviour. For these reasons, the complete expressions of the poles and zeros considering the parasitic capacitances and the gate resistance will not be presented in this work, only a comparison between the theoretical and simulated results using the model presented in Fig. 3.7. The complete model was also used to emulate a more realistic behaviour of the circuit and was essential in the early stages of the design process. Fig. 3.8 presents the comparison between the model in Fig. 3.7 and the simulated results for a capacitive degenerated differential pair.

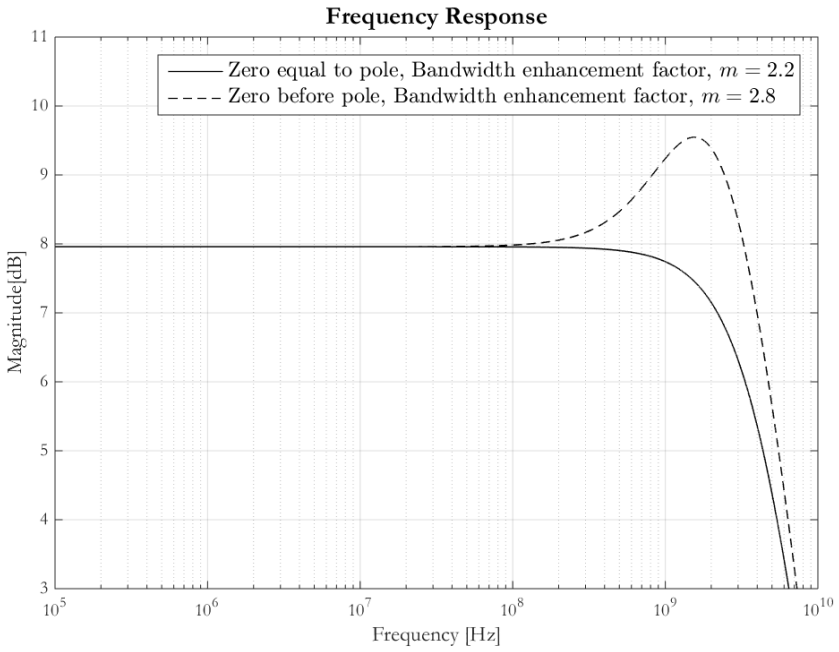


Figure 3.5: Frequency response of a capacitive degenerated differential for two different positions of the transconductance's zero - obtained using the mathematical model of Eq. 3.5.

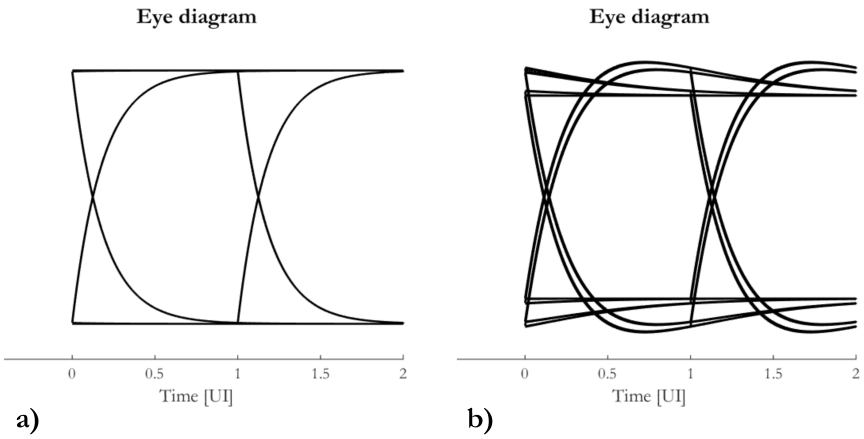


Figure 3.6: Eye diagrams of the output signals of a capacitive degenerated differential pair as a function of the transconductance's zero position, with the zero: a) matching the dominant pole b) before the dominant pole - obtained using the mathematical model of Eq. 3.5.

Table 3.1 presents the results of bandwidth, gain and frequency peaking (which is defined as $A_{vmax} - A_{vDC}$) obtained by the model versus the ones obtained by simulation. The results obtained show that the electrical model provides for a fairly good aproximmation of the real behaviour of the circuit.

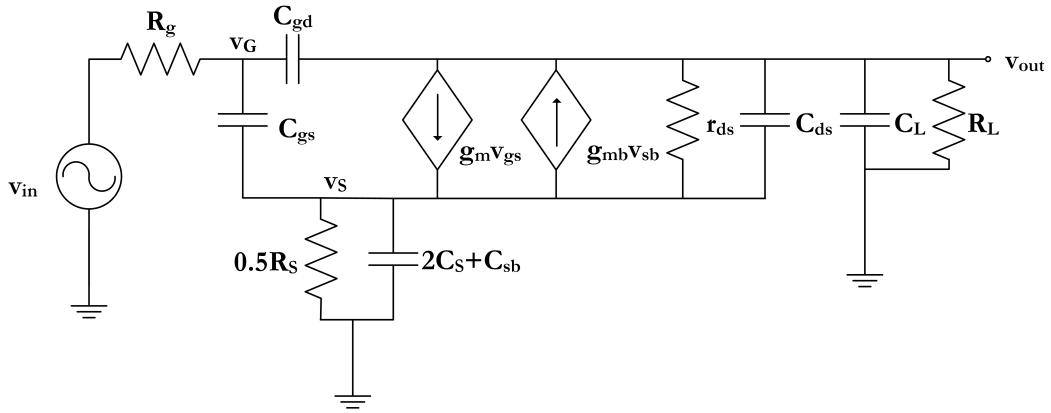


Figure 3.7: Small signals' model for the equivalent half-circuit of capacitive degenerated differential pair.

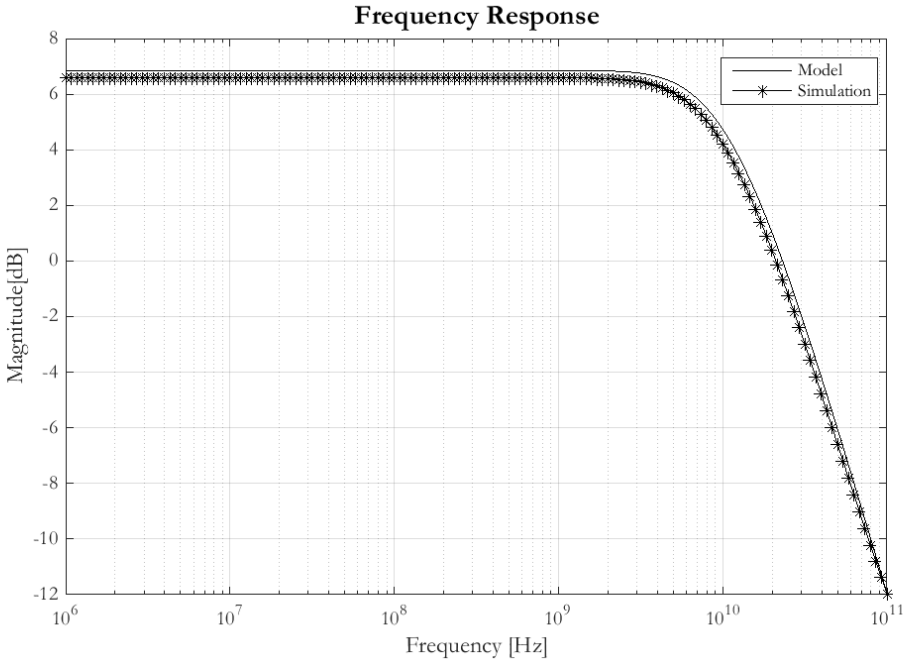


Figure 3.8: Modeled and simulated frequency response of a capacitive degenerated differential pair.

Table 3.1: Comparison of results obtained by the mathematical model vs simulation results for a capacitive degenerated differential pair.

	Bandwidth [GHz]	DC gain [dB]	Peaking [mdB]
Model	12.27	6.8488	0
Simulation	11.52	6.5920	0

3.1.1.2 NMC

As mentioned in Section 2.1.4.3 the Miller effect is quite limitative in terms of bandwidth in a cascade of gain stages. For this reason, the architecture of each Limiting Amplifier's gain cell will not only employ capacitive degeneration for bandwidth improvement. Negative Miller Capacitance was used in order to supress the Miller effect and therefore, increase the bandwidth of the overall cascade. Typically, canceling the C_{gd} capacitance in deep submicron technologies working at high speed, can be a very challenging task. It is difficult to implement capacitors small enough to accurately match the C_{gd} value because the matching between the capacitors (in a differential configuration) is relatively poor. Let us now analise the benefits of canceling the gate-drain overlap capacitance in a cascade of identical gain stages.

The idea behind this technique is placing a negative capacitor in parallel with C_{gd}, reducing the load of the previous stage, hence, improving the system's bandwidth. Although the idea of a negative capacitance may seem strange, since it means that its voltage drops when we try to charge it up, there are some active circuits that can provide this. One way to create a negative capacitance is to exploit the Miller effect, if we connect a regular capacitor C_M across a non-inverting amplifier the Miller capacitance will become negative $(1-A)C_M$, if the amplifier's gain, A, is larger than one. Thus, as explained in Section 2.1.4.3, the effective capacitance seen at the input would be equal to $C_{effec} = C_P + (1-A)C_M$. One should note that C_M capacitors are employing positive feedback. Meaning, if the amplifier's voltage gain is equal to 1, the feedback capacitor C_M would have no effect. This is because the output voltage exactly follows the input voltage, behaving as an ideal voltage buffer and thus there is no voltage drop across C_M and also no current flowing through it. If the amplifier's voltage gain is larger than 1, which is the normal case, the Negative Miller Capacitance shows and the input impedance is reduced, easing the load effect. One of the problems regarding this technique is that it extends the bandwidth using positive feedback, which means that, if the feedback capacitors are made too large, the effective capacitance at the input may become negative, and the system will become unstable.

Let us analyse in more detail the impedance seen at the input of a differential pair using crossed-coupled capacitors to cancel the gate-drain overlap capacitance. In order to calculate the input impedance let us consider the circuit illustrated in Fig. 3.9. Aplying KCL in nodes v_{in} and v_{out} it is possible to obtain the equation's system in 3.12 (ignoring the channel's resistance, r_{ds}).

$$\begin{cases} i_{in} = ({v_{in}}^{+} - {v_{out}}^{-})sC_{gd} + ({v_{in}}^{+} - {v_{out}}^{+})sC_M + {v_{in}}^{+}sC_{gs} \\ ({v_{out}}^{-} - {v_{in}}^{+})sC_{gd} + ({v_{out}}^{-} - {v_{in}}^{-})sC_M + \frac{{v_{out}}^{-}}{R_L} + g_m{v_{in}}^{+} = 0 \end{cases} \tag{3.12}$$

Where ${v_{in}}^{+} = -{v_{in}}^{-}$ and ${v_{out}}^{+} = -{v_{out}}^{-}$ considering differential operation.

Solving the previous equations' system is possible to obtain an expression for the single-ended impedance seen at the input of one side of the differential pair, given by 3.13.

.

$$z_{in}(s) = \frac{{v_{in}}^{+}}{i_{in}} = \frac{1+C_{gd}R_Ls+C_MR_Ls}{s(C_{gs}+C_M-C_Mg_mR_L+C_{gs}C_MR_Ls+C_{gd}(1+g_mR_L+C_{gs}R_Ls+4C_MR_Ls))} \tag{3.13}$$

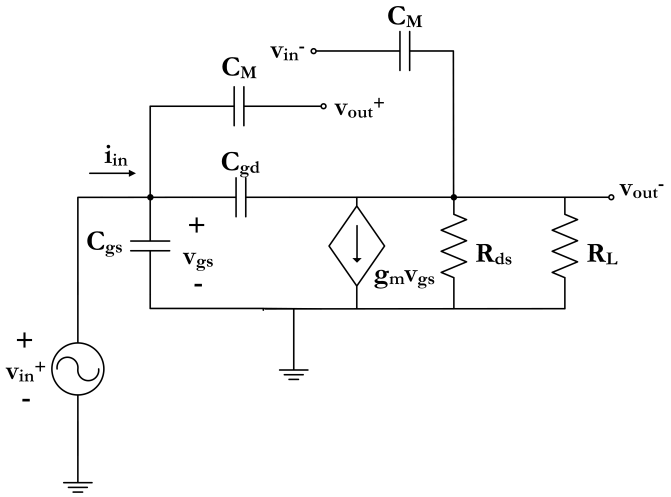


Figure 3.9: Small signals' model of the equivalent half-circuit of a differential pair employing NMC technique.

Now that there is an expression for the input impedance, let us analyse the case where we have a standard differential pair loaded by another differential pair employing NMC, which the correspondent small signals' equivalent half-circuit is depicted in Fig. 3.10. Once again, aplying KCL to node v_{out}, the following transfer function is obtained (ignoring the channel's resistance, r_{ds}):

$$H(s) = \frac{v_{out}}{v_{in}} = \frac{R_L(g_m - C_{gd}s)z_{in}(s)}{R_L + z_{in}(s) + C_{gd}R_Lsz_{in}(s)} \tag{3.14}$$

Replacing 3.13 in 3.14, a model for a standard differential pair loaded by an identical differential pair using NMC is obtained. It is possible to study the benefits of total or partially canceling the C_{gd} capacitances in bandwidth extension. More specifically, let us analyse the bandwidth extension factor, m (calculated at the output of the first stage), as a function of the ratio C_M/C_{gd}. It is also interesting to compare the results obtained by the mathematical model with real simulation results. Fig. 3.11 provides this analysis. The bandwidth extension factor is calculated dividing the bandwidth obtained by a certain C_M/C_{gd} ratio by the bandwidth resultant of C_M being zero.

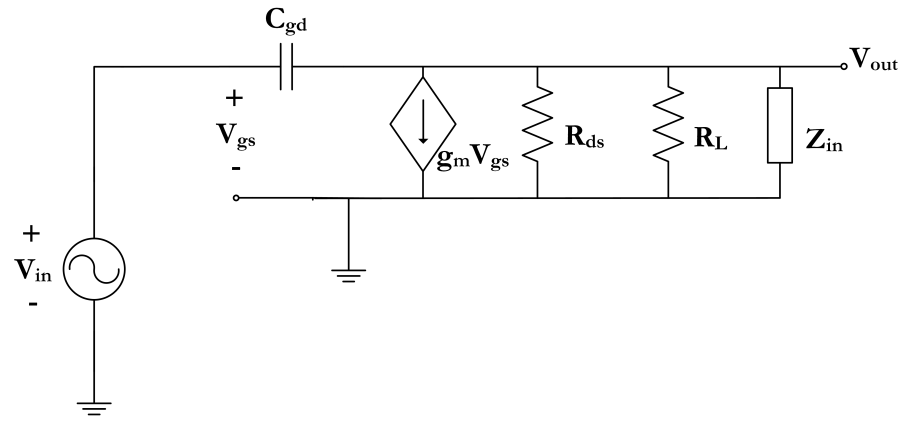


Figure 3.10: Small signals' model of the equivalent half-circuit of a simple differential pair loaded by a differential pair employing NMC.

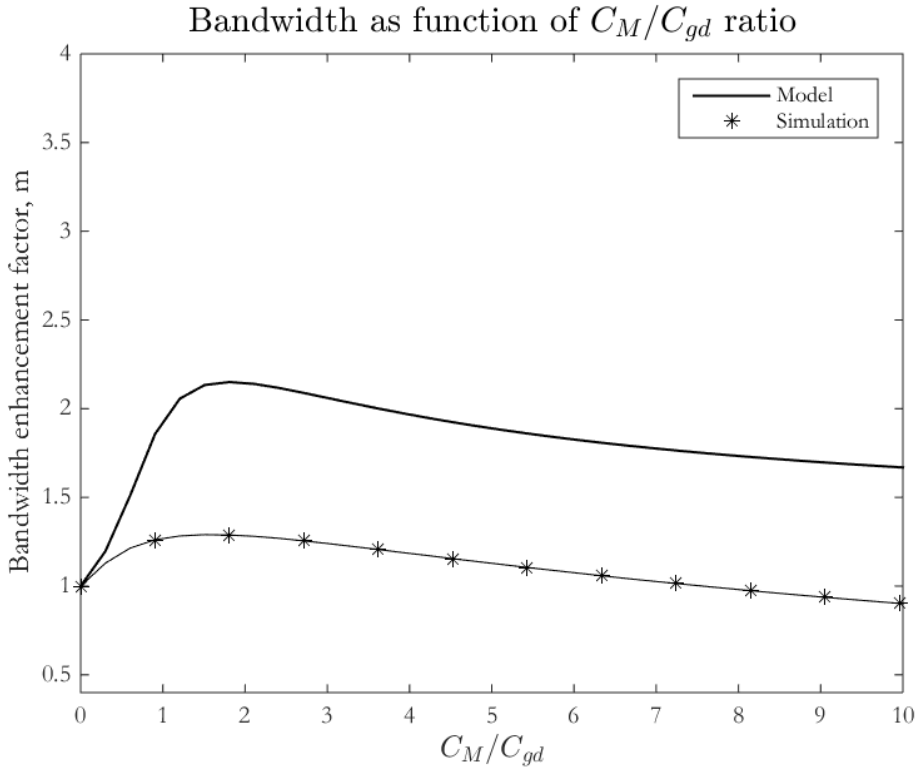


Figure 3.11: Variation of a bandwidth enhancement factor, m, as a function of the ratio C_M/C_{gd} - model results obtained using the mathematical model of Eq. 3.14.

It is possible to observe that, even though the curve obtained by the mathematical model does not perfectly fit the simulated one (mostly due to its simplicity), they both suggest that there is an optimum design point for the value of the crossed-coupled capacitors. The bandwidth extension factor achieves its maximum (in simulation), for a ratio C_M/C_{gd} of approximately 1.3, slightly after capacitor C_M matches the value of the gate-drain overlap capacitance.

This suggests the optimum ratio to be between 1 and 2 (the optimum ratio will depend on the DC gain of the differential pairs, this analysis was done for a gain of 2.15). The fact that the bandwidth starts to decrease as the effective input capacitance decreases may seem odd, but if we look at the frequency responses for two different situations - $C_M/C_{gd} = 1$ and$C_M/C_{gd} = 4$ - it is easy to understand this effect. The simulated frequency response for the two distinct situations is presented in Fig. 3.12.

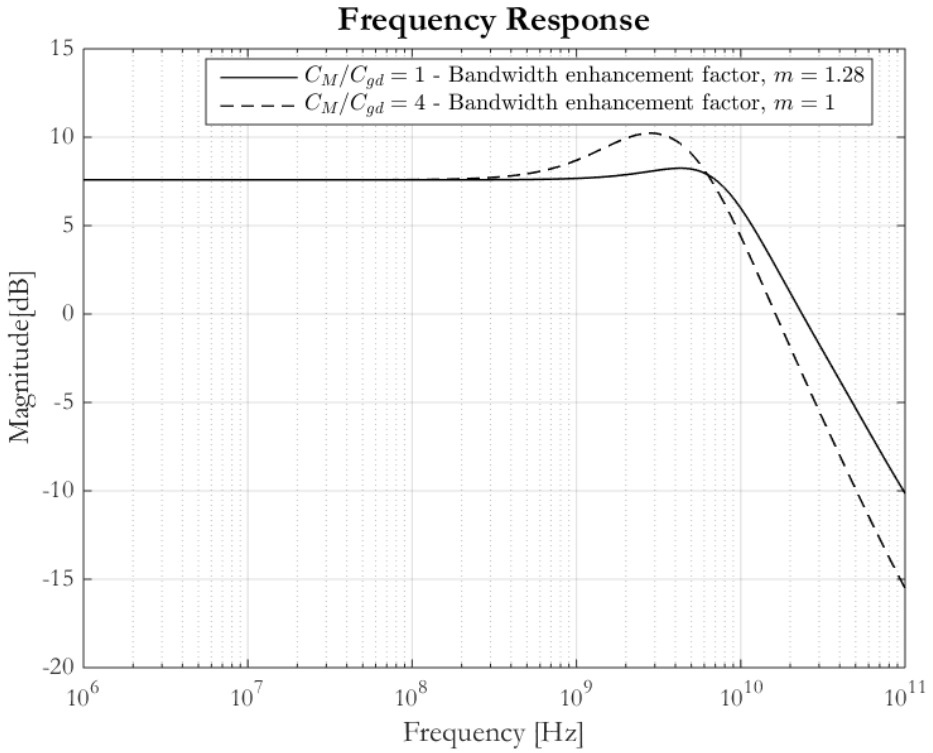


Figure 3.12: Different frequency responses for different C_M/C_{gd} ratios - simulated.

For larger values of C_M/C_{gd} the frequency response of the circuit starts to exhibit too much frequency peaking, causing the bandwidth to decrease. This translates into overshoot in the transient response. As mentioned before, this situation can be harmful in terms of jitter when working with PRBS as input signals. In light of these results and due to the stringent bandwidth and jitter requirements, it is clear to understand that it is fundamental to accurately match the C_{gd} value in order to take advantage of the maximum bandwidth extension possible and also to guarantee an acceptable step response.

3.1.2 Gain Cell

The selected architecture for each Limiting Amplifier's gain cell is represented in Fig. 3.13 in a simplified scheme. It is basically a differential pair with resistive load employing capacitive degeneration and crossed-coupled capacitors to improve the broadband response.

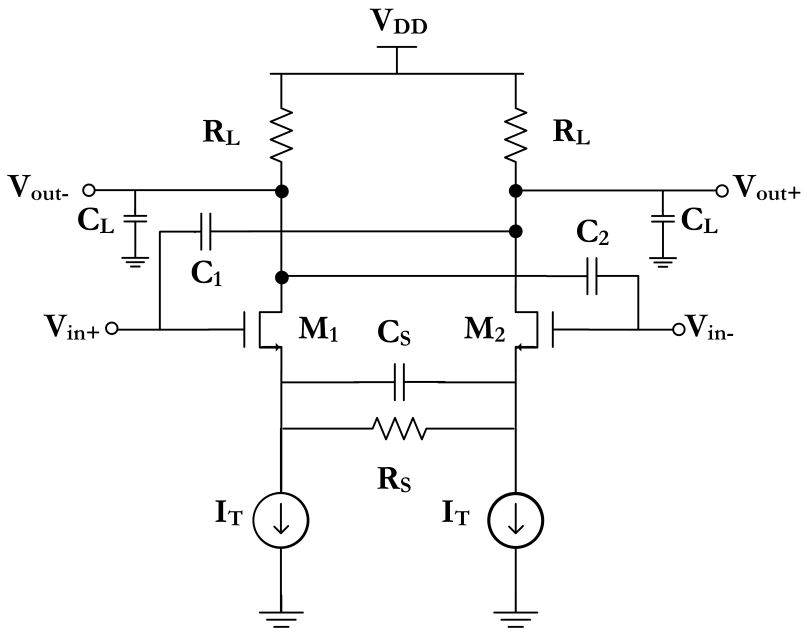


Figure 3.13: Simplified schematic of each Limiting Amplifier's gain cell.

The Limiting Amplifier needs to be capable of saturating the signal coming from the TIA with a minimum amplitude of 5 mV (peak-to-peak) which means it has to present a minimum voltage gain of 44 dB. In theory, and as discussed Section in 2.1.2, the optimal number of stages, in order to achieve a gain of 44 dB, would be given by $N_{opt} = 2ln(10^{\frac{44}{20}}) \approx 10$ with each stage achieving a voltage gain of 4.4 dB. In practice, the Process Voltage and Temperature (PVT) variations have to be taken into account and, unfortunately, the voltage gain of each gain cell will vary with process, temperature and supply voltage, specially in an open-loop configuration with passive loads. Also, with the increase in the number of stages, the variations in the gain become more accentuated. Therefore, the Limiting Amplifier was designed in order to achieve at least 44 dB and a minimum bandwidth 3.5 GHz (70% of the data rate) across all the PVT corners. Also, minimising the frequency peaking was also a major concern in order to fulfil the JTOL specifications. This is considering a ±10% variation in the supply voltage and the temperature ranging from -40 to 100°C.

Since the major design constrains regarding the Limiting Amplifier have already been presented let us continue to a more detailed analysis of each gain cell and of the complete limiting chain. The simplified architecture of each LA's cell was already presented in Fig. 3.13. Since the zero created by the capacitive degeneration is dependent on the value

of C_S and it is of the greatest importance to reduce the frequency peaking across PVT, the degeneration's capacitor was implemented using transistors.

This way, the capacitor C_S will vary with process in the same way that the parasitic capacitances of differential pair's transistors. Meaning, the position of the zero will track the position of the dominant pole, minimising the variability in the value of the peaking, keeping it at an acceptable value.

This way, capacitor C_S was implemented using a PMOS transistor due to their larger parasitic capacitances using a smaller area - compared to NMOS. The configuration used for the transistor is depicted in Fig. 3.14. All the device terminals are shorted, except for the gate, so, the effective capacitance seen from both sides is C_{gg} (C_{gg} is the sum of all the parasitic capacitances connected to the transistor's gate). To improve the differential pair's simetry in the layout, the PMOS transistor is divided in two, and they are placed in parallel between the sources of the differential pair transistor in opposite positions. Such an arrangement is illustrated in Fig. 3.15. The value of C_S will be equal to the sum of the C_{gg} capacitances of transistor M_3 and M_4.

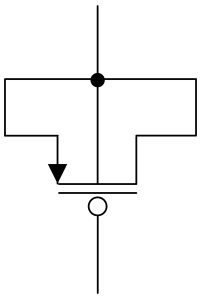


Figure 3.14: Degeneration's capacitor implemented with a PMOS transistor.

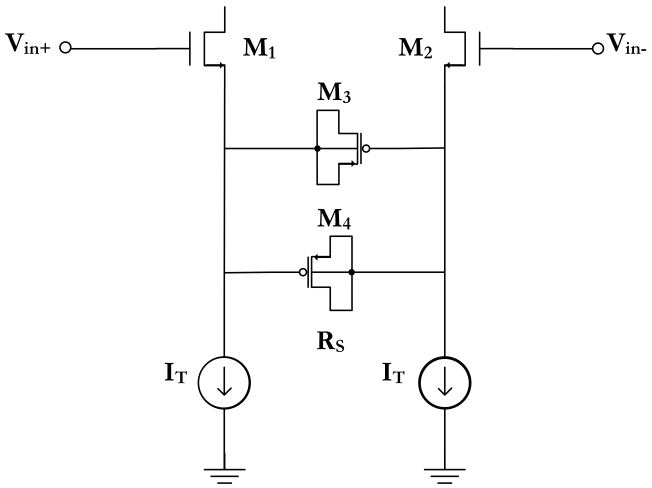


Figure 3.15: Degeneration's capacitors implemented with PMOS transistors.

Table 3.2 shows the variation of the frequency peaking for different processes implementing the degeneration's capacitor with PMOS transistors or using Metal Oxide Metal (MOM) capacitors. Analysing the results of Table 3.2 it is clear to see that the variations

in the value of the frequency peaking are smaller when implementing the capacitor with transistors.

One should note that these variations were measured considering the overall Limiting Amplifier, and they do not correspond to the variation of a single stage, but to the complete chain of gain stages. Although the variations using the PMOS transistors may still seem large, all of them correspond to less than 1 dB of peaking at the overall Limiting Amplifier, which is considered aceptable.

Table 3.2: Variation of the frequency peaking against the TT process for two different implementations of the degeneration's capacitor, C_S.

		FF	FS	SF	SS
Variation of frequency peaking with process against the TT process	PMOS Transistor	66 %	2%	0%	119%
	MOM capacitor	100%	20%	18%	758%

The crossed-coupled capacitors, C_1 and C_2, that provide for the cancelation of the parasitic capacitance C_{gd} of the differential pair's transistors were also implemented using transistors, although not for the same motives. As mentioned before, in deep submicron technologies working at high speed the gate-drain overlap capacitance tends to be smaller than 50 fF, and it is relatively hard to create a capacitor that accurately matches its value. Furthermore, in a differential configuration, the matching between the two capacitors would not be good which would degrade the symmetry of the differential pair. For these reasons, the crossed-coupled capacitors were also implemented using transistors, in this case, PMOS ones, since the required area is smaller. The configuration is presented in Fig. 3.16. The crossed-coupled capacitors C_1 and C_2 were implemented by the C_{gg} capacitance of transistors M_5 and M_6. The value of the gate-drain overlap capacitance of transistors M_1 and M_2 was previously measured and afterwards, the dimensions of M_5 and M_6 were tuned, taking into consideration the V_{gs} voltage across its terminals, in order to match their C_{gg} capacitance with the C_{gd} capacitance of M_1 and M_2.

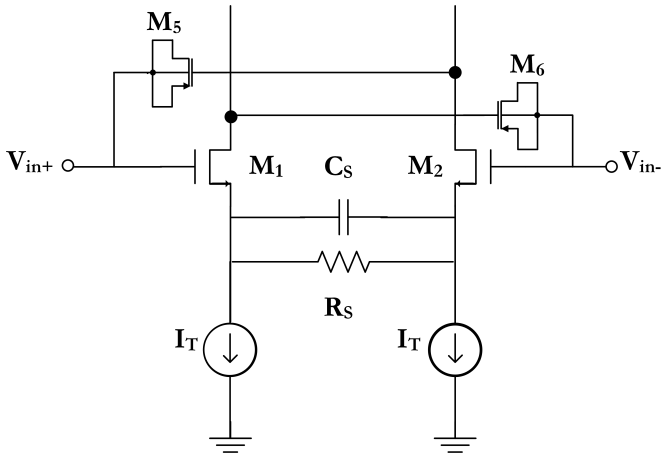


Figure 3.16: Crossed-coupled capacitors, C_1 and C_2, implemented with PMOS transistors.

The complete final architecture of the gain cell is presented in Fig. 3.17. Where M_7 and M_8 are the current sources' transistors and are biased through the control voltage, V_{biasN}.

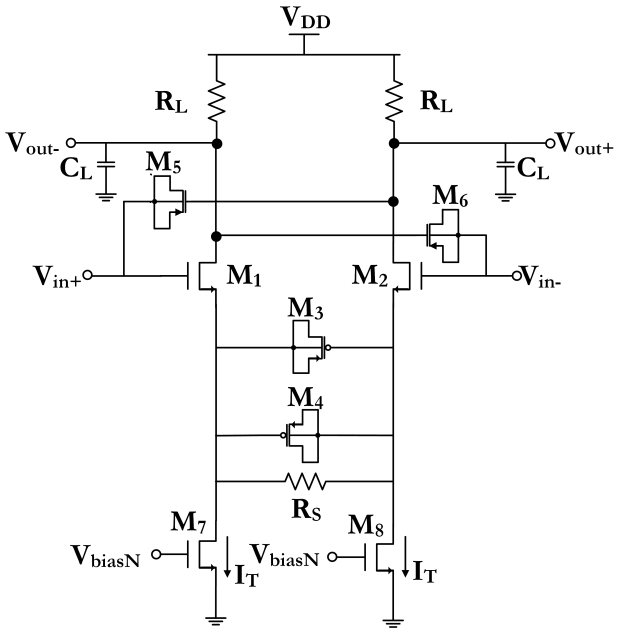


Figure 3.17: Complete architecture of each Limiting Amplifier's gain cell.

Table 3.3 presents the components' dimensions of the LA's gain cell. Since bandwidth is a major concern the transistors of the differential pair, M_1 and M_2, use minimum channel length.

Table 3.3: Components' dimensions of the Limiting Amplifier's gain cell.

	W[um]	L[um]	Resistance value [Ω]	Capacitance value [fF]
$M_{1,2}$	10	0.06	-	-
$M_{3,4}$	120	1	-	278.6
$M_{5,6}$	3.4	0.06	-	2.3
$M_{7,8}$	42	0.5	-	-
R_L	-	-	820	-
R_S	-	-	70	-

Now the LA's gain cell was fully exposed, let us discuss how the biasing of the current sources' transistors is implemented and the pratical issues related to it.

3.1.3 Replica Bias

The amplitude of the output voltage, V_{SWING}, of the differential pair depends on the value of the load resistor, R_L, and the bias current, I_T. The value of the load resistor can vary up to 30% from its nominal value due to process and temperature.

These changes in the effective resistor value will change the common mode voltage of the LA's stages. In the last stages of amplification, or if the input signal is large enough, some gain cells will saturate and work in large-signal operation. This means that the total current of each saturated gain cell, $2I_T$, will be steered by one side of the differential pair only. So, the common mode voltage, V_{CM}, will be given by $V_{DD} - R_L 2I_T$. If this value is too low, it will not be enough to keep transistors $M_{1,2}$ and $M_{7,8}$ in saturation. Therefore, it is of the utmost importance to control the variations of the common mode voltage across corners in order to guarantee that the transistors stay in saturation even in large-signal operation. Such an arrangement is possible using negative feedback to adjust the bias current, I_T, in order to maintain a constant common mode voltage and output voltage swing. It would be inefficient to use this feedback circuit inside each limiting cell since it would dissipate a lot of power and it would be necessary to eliminate the differential signal from the feedback path. A more efficient solution is to have a replica of the original circuit (only half of the circuit is necessary) and adjust the common mode voltage of the replica to be equal to the desired one [30]. This is possible because the replica "feels" the temperature and process variations in the same way the original circuit does, so the variations will be the same. Basically, the bias current of the replica circuit is adjusted through a feedback loop in order to keep the common mode voltage constant and that current is mirrored to all the gain cells. This principle is shown in Fig. 3.18.

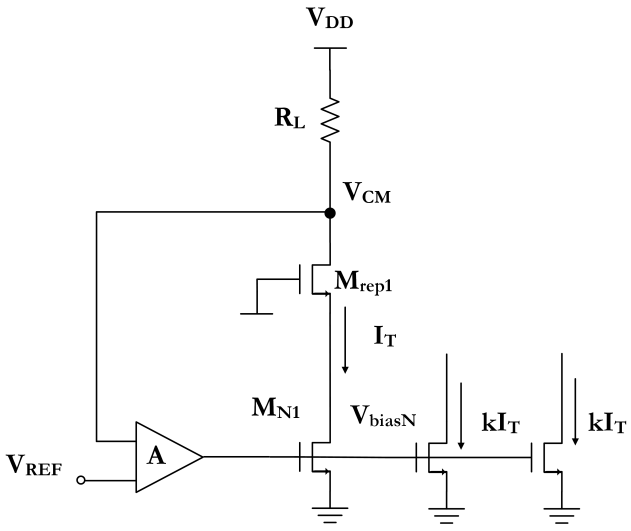


Figure 3.18: Replica bias' architecture.

In other words, the replica bias circuit compares the common-mode voltage V_{CM} with a reference voltage V_{REF} using an amplifier. The amplifier's output voltage V_{biasN} controls the current through transistor M_{N1}. The amplifier will work until the common mode voltage equals the reference voltage, V_{REF} (this reference voltage is generated using a bandgap circuit). The biasing voltage, V_{biasN}, of the replica bias circuit is then applied to the current sources' transistors of all the limiting stages, generating a tail current equal to the biasing current of the replica circuit.

Thus, all the gain cells will have the same common mode voltage which is equal to the replica bias circuit's common mode voltage[2], V_{CM}. This is based on the assumption that the components' dimensions of the gain cells are adjusted accordingly to the mirror relation of the current sources. If the transistors of one gain cell are scaled to have a larger multiplicity, k, than the transistors of the replica circuit, the bias current of that gain cell will be k times higher than the bias current of replica. In this case, the load resistance value of the gain cell is scaled to R_L/k to maintain the common-mode voltage and the output swing (this technique is going to be further explored in Section 3.1.4). The replica circuit does not necessarily have to be half of the original circuit (first LA gain cell). In order to reduce the power dissipation is to possible to have the replica scaled by a $1/k$ factor (the transistors are k times smaller and the resistor is k times larger) reducing the current consumption of the overall bias circuit. If the replica is half-circuit of the first gain cell its power consumption will be half of the first gain cell, which is a lot for a biasing circuit. In this fashion, the current consumption of the replica is reduced by $1/k$, since the first gain cell will have a bias current of kI_T. Obviously, there will be an error between V_{REF} and V_{CM} and it will depend on the loop gain of the overall replica bias circuit. The relative error is given by the following expression [30]:

$$\frac{1}{1 + A g_{mM_{N1}} R_L} \tag{3.15}$$

Where A is the amplifier's gain and $g_{mM_{N1}}$ is the transconductance of the current source's transistor. Since the product $g_{mM_{N1}} R_L$ is defined *a priori* in the design of the gain cell, the only way to reduce the error between V_{CM} and V_{REF} is to increase the gain of the amplifier. The feedback loop, as expected, must be designed to be unconditionally stable. Since the control voltage, V_{biasN} is, in essence, a DC signal, and its value its determined by process corner (which does not change after manufacture) and temperature (which is assumed to vary slowly) the bandwidth requirements for the feedback loop are only a few kHz. Therefore, the stability compensation of the loop is relatively easy to perform with a simple Miller compensation. The architecture choosen for the amplifier is illustrated in Fig. 3.19. It is composed by a differential pair implemented with NMOS transistors (the reason for choosing NMOS transistor is the fact that the desired common-mode voltage, V_{REF}, is much above $V_{DD}/2$) with PMOS active loads and single-ended output. The differential pair is followed by a second gain stage which output drives the gate of the current source's transistor, M_{N1}. The gain of the loop, by inspection, is given by Eq. 3.16. Where g_{ds} is the drain-to-source transconductance of the respective transistor.

$$G_{loop} = \frac{g_{m2} g_{m8}}{(g_{ds4} + g_{ds2})(g_{ds7} + g_{ds8})} g_{m_{MN1} R_L} \tag{3.16}$$

[2]The output voltage of the gains cells will have a difference to the V_{CM} voltage of the replica circuit due to matching errors between the load resistances and transistors of both circuits. For matched devices in close proximity, matching errors can be as small as 0.1%, but for distant devices the matching errors are larger and can be up to 5% [30].

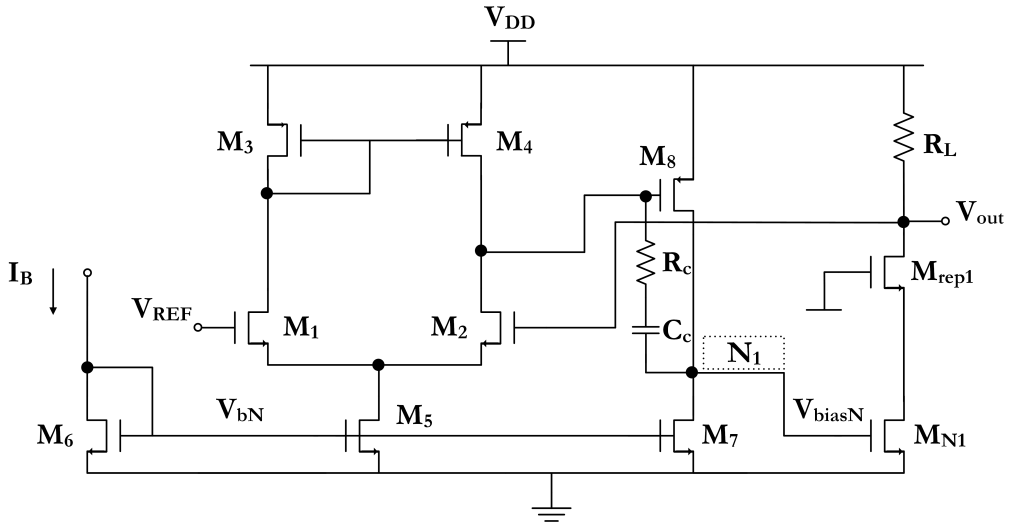


Figure 3.19: Schematic of the replica bias' amplifier.

Table 3.4: Components' dimensions of the replica bias' amplifier

Transistor	Size [µm]
$M_{1,2}$	9/1
$M_{3,4}$	4/1
M_5	10/1
M_6	5/1
M_7	5/1
M_8	16/1
M_{N1}	6/0.5
M_{rep1}	1.42/0.06
Resistor	**Size [kΩ]**
R_c	10.00
R_L	5.74
Capacitor	**Size [pF]**
C_c	9.5

The dominant pole, by design, is located at node N_1. Its location can be calculated using the Miller theorem, and is given by expression 3.16. The -3dB bandwidth (in Hz) of the replica loop is given by $BW_{replica} = \frac{\omega_p}{2\pi}$.

$$\omega_p = -\frac{g_{ds7} + g_{ds8}}{C_c(1 + \frac{gm_8}{g_{ds7}+g_{ds8}})} \tag{3.17}$$

Table 3.4 presents the components' dimensions of the replica bias' amplifier. As mentioned before, the third amplifier stage is a scaled replica of one arm of the LA's first gain cell and its dimensions have a scaling factor of 1/7 in relation to the original one.

3.1.3.1 Simulation Results

Table 3.5: Estimated and simulated results of the replica bias' amplifier.

	DC gain [dB]	Bandwidth [kHz]	GBW [MHz]	Phase Margin [°]	Power [μW]
Estimated	72.5725	1.8724	7.9624	-	-
Simulated	72.1669	2.0892	8.4786	77.81	146

Table 3.5 presents the most relevant parameters regarding the replica bias' amplifier. The loop gain is of approximately 72 dB which corresponds to a voltage error (between the common mode voltage and the reference voltage) smaller than 1%. In this case, the voltage error is not that crucial since changes of a few mV in the common mode voltage are negligible. The phase margin of the loop is larger than 60°. A phase margin of 60° would be more than acceptable for this application (since step response is not really a concern) but the variations of compensation's capacitor C_c with process, require a larger phase margin in the typical corner in order to match the specifications across all the process corners. The power consumption was reduced to 146 µW is which is reasonable for a biasing circuit.

3.1.3.2 Layout

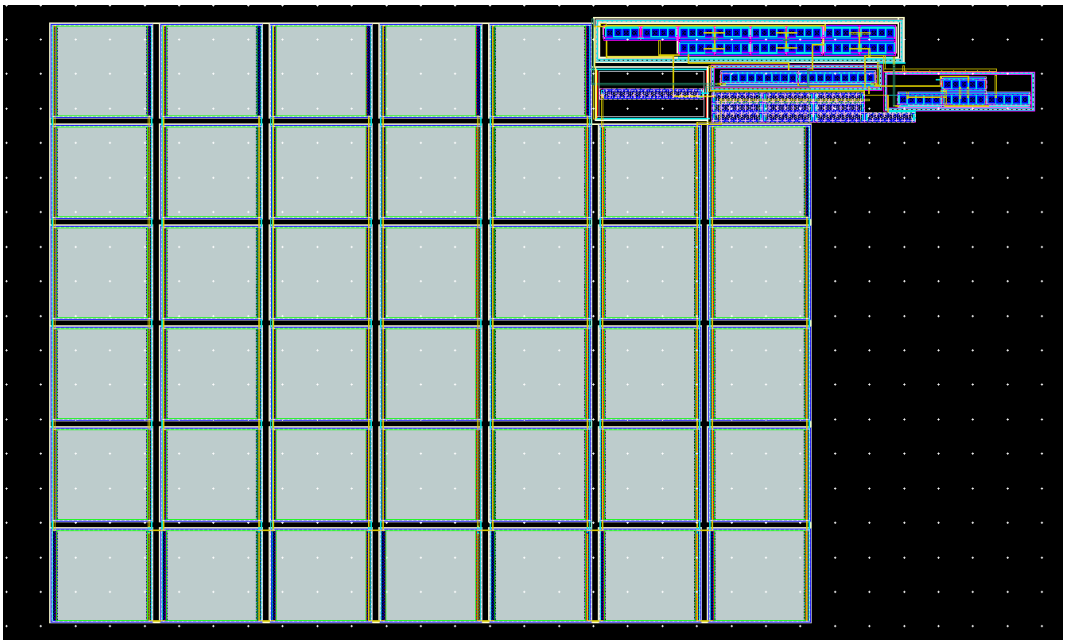


Figure 3.20: Layout of the replica bias' amplifier.

Table 3.6: Schematic vs layout simulation results of the replica bias' amplifier.

	DC gain [dB]	Bandwidth [kHz]	GBW [MHz]	Phase Margin [°]	Power [μW]
Schematic	72.1669	2.0892	8.4786	77.81	146
Layout	72.1656	1.0234	4.1526	91.23	145

Fig. 3.20 shows the layout of the replica bias's amplifier. The total layout area is approximately 10 203 µm^2 (1.4576%) on the IC. Table 3.6 presents a comparison of the most relevant parameters regarding the replica bias' amplifier between the schematic and the layout. The DC gain remained almost unchanged although the bandwidth suffered a "2x" reduction, due to the increase on the compensation capacitor value due to the layout. The phase margin also increased since the GBW was pushed in. A post-layout tuning in the compensation capacitor value would lead to the original phase margin and significantly improve the overall area of the amplifier.

3.1.4 Limiting Chain

The chosen number of stages was 9 (since it allowed to fulfil the gain and bandwidth specifications across PVT) with the device's dimensions and bias currents scalled accordingly in such a fashion that every stage is "strong" enough to drive the previous one and the last one can drive the Output Buffer, minimising the power dissipation at the same time. The cascade of gain cells and respective scaling is represented in Fig. 3.21.

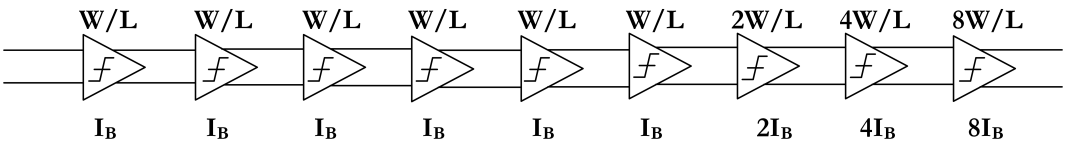


Figure 3.21: Cascade of limiting stages and scaling factors.

In order to keep the voltage gain of all the cells equal and to keep the common mode voltage constant, the scaling of the currents implies a change in the components' dimensions. Let us consider a simple resistive loaded differential pair, where the gain is just given by $g_m R_L$ and the total bias current is given by $2I_D$. The transconductance of a MOSFET in the active region is given by the following expression ([16], Chapter 1):

$$g_m = \sqrt{2\mu C_{ox}\frac{W}{L}I_D} \tag{3.18}$$

Where μ is the electronic mobility of the carriers (electrons or holes, depending on the channel type), C_{ox} is the gate capacitance per unit area, W is gate width, L is the gate length and I_D is the drain current of the transistor.

Also, for a simple differential pair, the common mode voltage will be given by $V_{DD} - R_L I_D$ (assuming that it is not working in large-signal operation). Now let us assume that the bias current is increased by a factor of k, meaning $I_B = k2I_D$. The common mode voltage would now be equal to $V_{DD} - kR_L I_D$. Thusly, the only way to keep the common mode voltage constant is to decrease the resistor by the same factor, k. Visibly, this also means that the voltage gain of the amplifier would be reduced by the same factor unless the transconductance's value changes. The transconductance would also have to be increased by the same factor to make up for the decrease in the load resistor. The new value of the transconductance, g'_m would have to be k times bigger than g_m. So far, considering all the assumptions, so far the new transconductance's value is given by:

$$g'_m = \sqrt{2\mu C_{ox}\frac{W}{L}kI_D} = \sqrt{k}\sqrt{2\mu C_{ox}\frac{W}{L}I_D} \tag{3.19}$$

Looking at expression 3.19 it is possible to see that the actual value of the new transconductance is only $\sqrt{k}$ times larger than the original one. To solve this problem, and therefore keep the new voltage gain equal to the original one, the transistor's $\frac{W}{L}$ relation can also be increased by a factor of k. This results in the following expression:

$$g'_m = \sqrt{k}\sqrt{2\mu C_{ox}k\frac{W}{L}I_D} = k\sqrt{2\mu C_{ox}\frac{W}{L}I_D} = kg_m \tag{3.20}$$

This means that the voltage gain of the scaled differential pair would be given by $kg_m\frac{R_L}{k} = g_m R_L$. Using this scaling technique it is possible to increase the bias current keeping the DC operating point of the circuit constant. In the case of a capacitive degenerated differential pair, which is the case of each LA's gain cell, the voltage gain also includes the degeneration's resistor, R_S. The voltage gain of a LA's gain cell is given by:

$$Gain = \frac{g_m R_L}{1 + \frac{g_m R_S}{2}} \tag{3.21}$$

Expression 3.21 tells us that in order to keep the gain constant, the value of the degeneration's resistor has to be decreased by k as well. The Limiting Amplifier's gain stages were scaled according to the methodology described above.

The first stage has a bias current $I_B = 2I_T = 780$ µA which means that the last limiting stage, which has a scaling factor of 8 compared to the first one, possesses a bias current of 6.24 mA, large enough to drive the large transistors of the Output Buffer without significantly degrading the rise and fall times of the signal. The first six stages are identical, and the following ones are scaled by a factor of two in relation to the previous one. The

components' dimensions of the 7th, 8th and 9th limiting stages are the ones presented in Table 3.3 with the transistor's widths multiplied by the respective scaling factors, and the resistors divided by the scaling factors as depicted in Fig. 3.21. The layout of the first six gain cells is presented in Appendix A - Fig. A.1-, the extraction simulation results are not presented in this work since the layout of the last gain cells was not finished.

3.1.5 Simulation Results

The frequency response of the overall cascade of gain cells, is presented in 3.22.

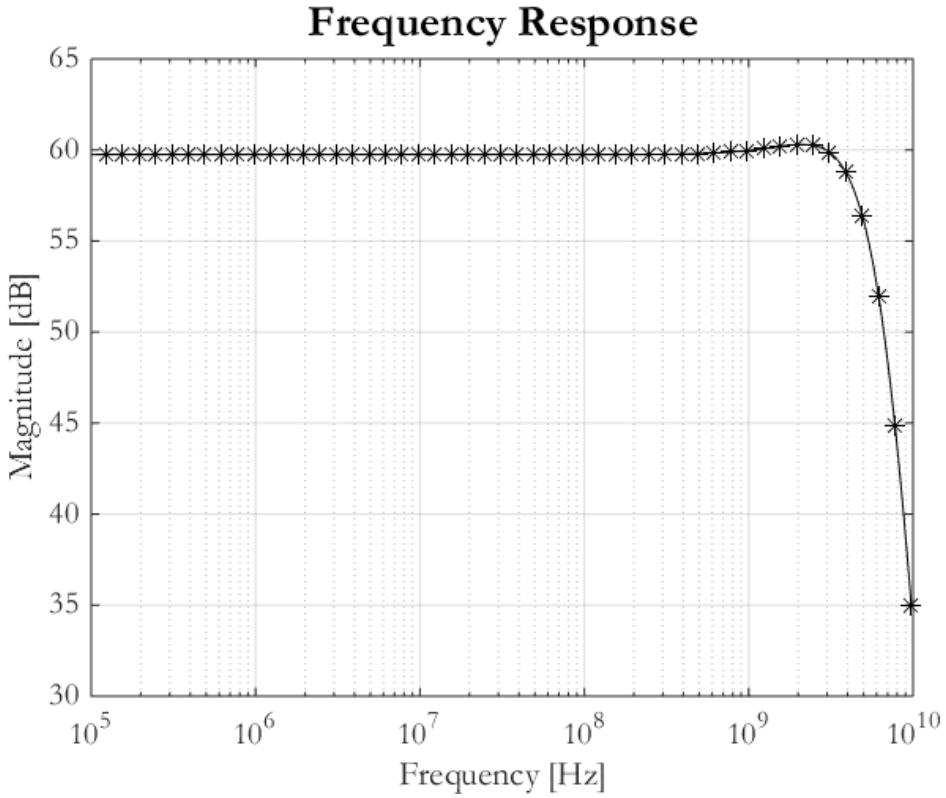


Figure 3.22: Frequency response of the overall Limiting Amplifier.

Table 3.7: Simulation results of the overall Limiting Amplifier.

DC gain [dB]	Bandwidth [GHz]	Frequency Peaking [dB]	Input Integrated Noise (differential) [µV]	Power [mW]
59.8	4.8	0.6	435	18.94

The most relevant parameters considering the Limiting Amplifier are presented in Table 3.7. The bandwidth of the LA (this value was measured with the Output Buffer connected to the last stage and the the RSSI's cells connected to all the gain stages) is almost equal to the maximum data rate (5 Gb/s) and the frequency peaking is below 1 dB, in the typical corner. The total power consumption of the circuit (including the biasing

circuit) is 18.94 mW. In addition to these results, Table 3.8 provides the Limititing Amplifier's bandwidth, gain, noise, frequency peaking and power consumption results across some PVT corners (the corners presented are the ones with more variability in gain and bandwidth in relation to the typical corner).

Table 3.8: Limiting Amplifier's simulation results across the most relevant PVT corners.

	SS 1.08V 100°C	FF 1.32V -40°C	FF 1.08V 100°C	SS 1.32V -40°C
DC gain [dB]	61.3	57.8	43.2	74.9
Bandwidth [GHz]	4	6.0	4.7	5
Frequency Peaking [dB]	0.391	0.960	0.094	1.8
Integrated Noise [μV]	556	332	573	343
Power [mW]	16.3	20.8	22.0	16.5

The first corner (SS 1.08V 100°C) is the slowest one, achieving a bandwidth equal to 80% of the data rate. The second corner is the fastest one, and yields a bandwidth larger than the data rate. Typically, this is not desirable due to the large integrated noise that comes with it. Since this is not the case, this corner is consider acceptable. The third corner (FF 1.08V 100°C) is, as expected, the lowest gain and highest noise corner (since the noise in input referred is normal that the lowest gain corner exhibits the larger noise). The last corner is the highest gain corner and also the one that exhibits more frequency peaking, 1.8 dB. Still, transient simulations showed that this amount of peaking was not enough to cause excessive jitter noise.

It also may be interesting to analyse the bandwidth enhancement factor using only capacitive degeneration technique or only NMC technique, and comparing these results to when both techniques are combined, which is the case of this project. Table 3.9 provides this analysis. Employing only capacitive degeneration a bandwidth enhancement factor of 1.61 is achieved along with a penalty of about 13% in the voltage gain of the amplifier. NMC technique provides for a bandwidth enhancement factor of 1.62 without degrading the voltage gain of the LA. Both techniques joined yield a bandwidth enhancement factor of 2.6.

Table 3.9: Bandwidth enhancement factor for different broadband techniques.

	Capacitive Degeneration	NMC	Both
Bandwidth enhancement factor, m	1.61	1.62	2.6
DC gain loss [%]	13	0	13

Fig. 3.23 presents the eye diagram of the differential output of the LA for a PRBS sequence at 5Gb/s with 5 mV_{pp} at the input (which is expected to be the minimum signal's amplitude provided by the TIA). Table 3.10 presents important metrics regarding the time response of the LA at 5Gb/s.

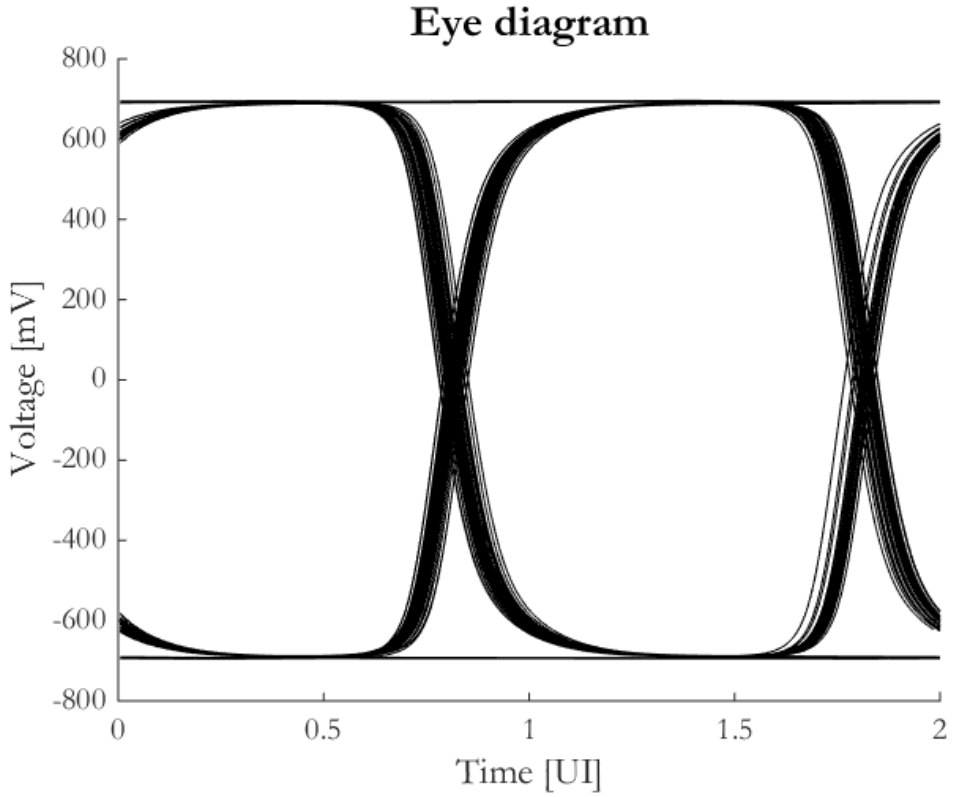


Figure 3.23: Eye diagram of the last Limiting stage for an input PRBS at 5Gb/s for the minimum input signal's amplitude.

Table 3.10: Simulation results concerning the time response of the LA at 5Gb/s.

Rise/fall time [ps]	Slew rate [GV/s]	Total jitter [UI]
62	20	0.06

The rise and fall times of the output signal are about 60 ps with the total jitter at 0.06 UI, well below the specified value of 0.3 UI (this value is obviously larger when the input signal is generated by the TIA which is the main source of noise in the Optical Receiver chain).

It also important to analyse the eye diagram at the first stage of the Limiting Amplifier, to check if the SNR specifications are met. From the eye diagram, the SNR can be measured as [6]:

$$\frac{V_{AVG_1} - V_{AVG_0}}{1\sigma_1 + 1\sigma_0} \tag{3.22}$$

Where V_{AVG_1} is the average value of the logic level 1 and V_{AVG_0} is the average value of the logic level 0. $1\sigma_1$ and $1\sigma_0$ are the standard deviations from the average value of the logic levels, 1 and 0, respectivelly. Fig. 3.24 presents the eye diagram of the differential output of the first LA's gain cell for a PRBS sequence at 5Gb/s with 5 mV_{pp} at the input. Aplying expression 3.22 the previous eye diagram yields a SNR of 10, which is above the specified value of 7.

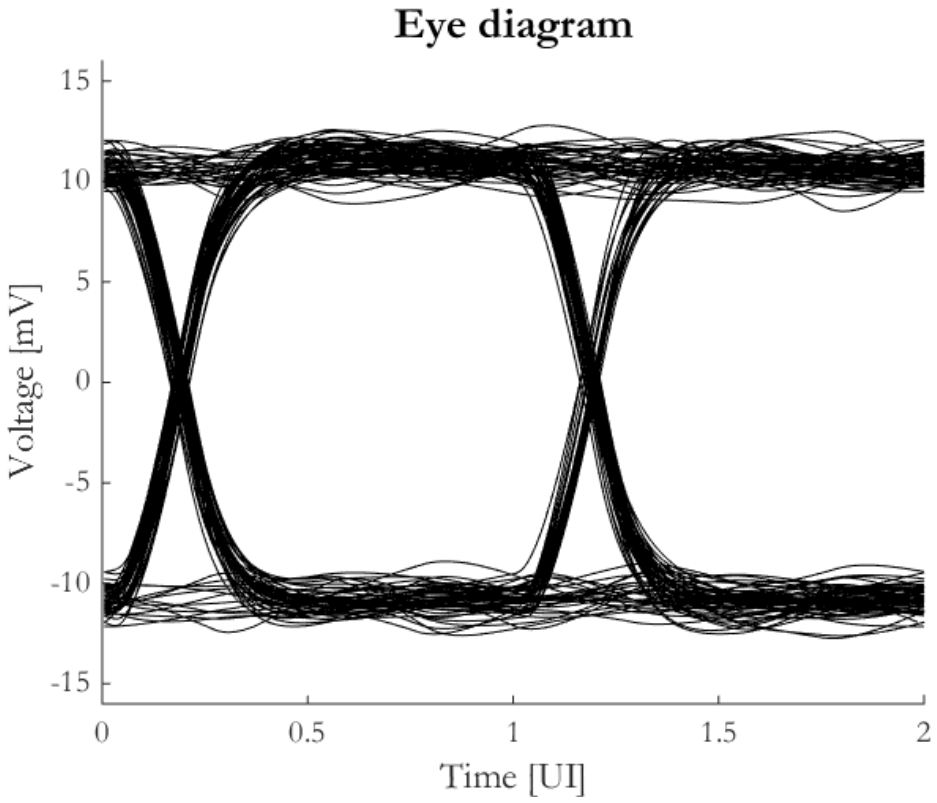


Figure 3.24: Eye diagram of the first Limiting stage for an input PRBS at 5Gb/s for the minimum input signal's amplitude.

Lastly, let us look at the eye diagram of the last Limiting stage for an input PRBS at 5Gb/s with maximum input voltage, which is expected to be 600 mV_{pp}, as represented in Fig. 3.25. The total jitter is now only 0.03 UI (almost nonexistent) whereas the rise and fall times are the same as in the minimim amplitude case. It is possible to observe a more "squared" eye shape.

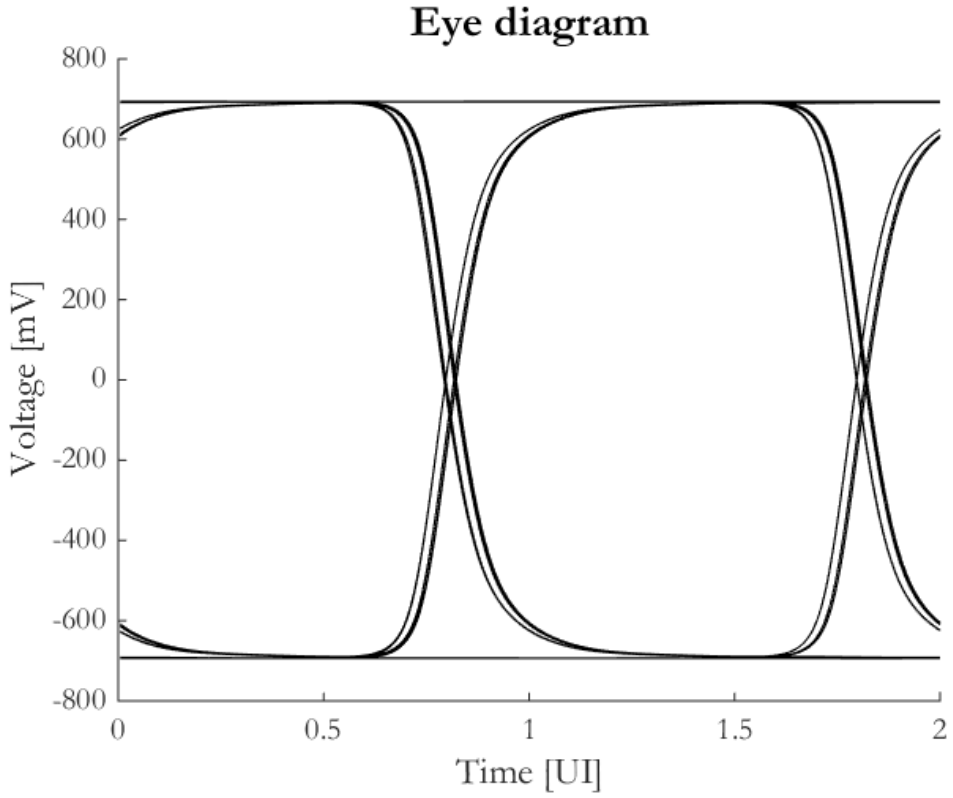


Figure 3.25: Eye diagram of the last Limiting stage for an input PRBS at 5Gb/s for the maximum input signal's amplitude.

Although the Limiting Amplifier is still capable of saturate with signals with smaller amplitudes (up to 1 mV_{pp}) it is not useful since the SNR of the first stage would be too low. For signals with a peak-to-peak amplitude below a certain value the SNR would not grant the BER specifications. The SNR can be calculated (in case of differential operation) as $2V_{pp_{in}}/\sigma_N$, where σ_N is the input integrated noise across the entire bandwidth (single-ended). For the first gain cell, the input integrated noise is about 688 µV which means that, for input signals with amplitudes below 2.4 mV_{pp} the circuit is not of use for this particular application since the BER[3] specification is 10^{-12} and that demans a SNR equal or larger than 7.

[3] $BER = \frac{1}{SNR\sqrt{2\pi}} \exp \frac{-SNR^2}{2}$ [7]

3.2 Received Signal Strength Indicator

A logarithmic amplifier is normally used for the RSSI since it allows for a wide Dynamic Range, in terms of input power, to be represented within a limited voltage range. This is accomplished by feeding each one of the Limiting Amplifier outputs to rectifiers which convert the voltage signal at each node into current. Then, all the currents originating from the Full-Wave Rectifier (FWR)s are summed up and low-pass filtered (the low pass filter function is performed by resistor R_{LOAD} and capacitor C_{LOAD}), creating an almost DC indicating voltage of the input signal's strength, $V_{STRENGTH}$. Successive detection architecture is used to implement a piece-wise linear logarithmic function resulting in a power detection transfer function ($V_{STRENGTH}$ vs input power) that is linear-in-dB. This scheme is represented in Fig. 3.26. Note: All the figures with NMOS and PMOS with undefined bulk have their bulk connected to ground and V_{DD}, respectively.

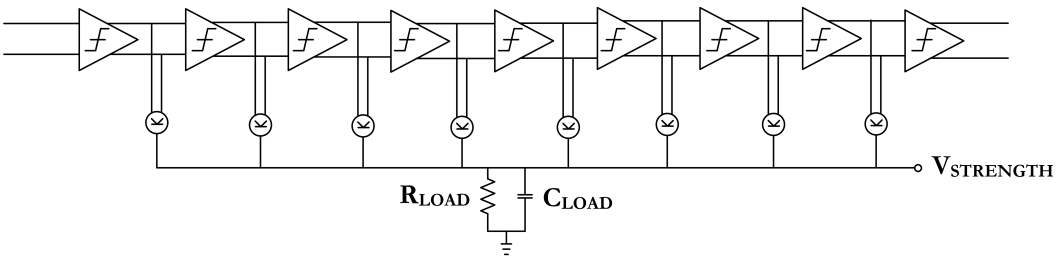


Figure 3.26: RSSI's architecture.

The two most important performance parameters of a RSSI are the Dynamic Range (DR) and detection sensitivity. The Dynamic Range is defined by the limits in the input power given by the points exactly before the RSSI saturates, Fig. 3.27 a). Basically it defines the input power up to which the RSSI can measure the signal's strength. Below and up to a certain power level the output of the RSSI will remain unchanged and equal to DC_{max} and DC_{min}, respectively. Detection sensitivity is defined as the slope of the curve and it is measured in mV/dB. In other words, it is the gain of the RSSI and it is given by $Gain = \frac{DC_{max} - DC_{min}}{DR}$ [31]. If we consider that the maximum and minimum indicating values remain constant then there is a plain tradeoff between DR and detection sensitivity, since both metrics are inversely proportional.

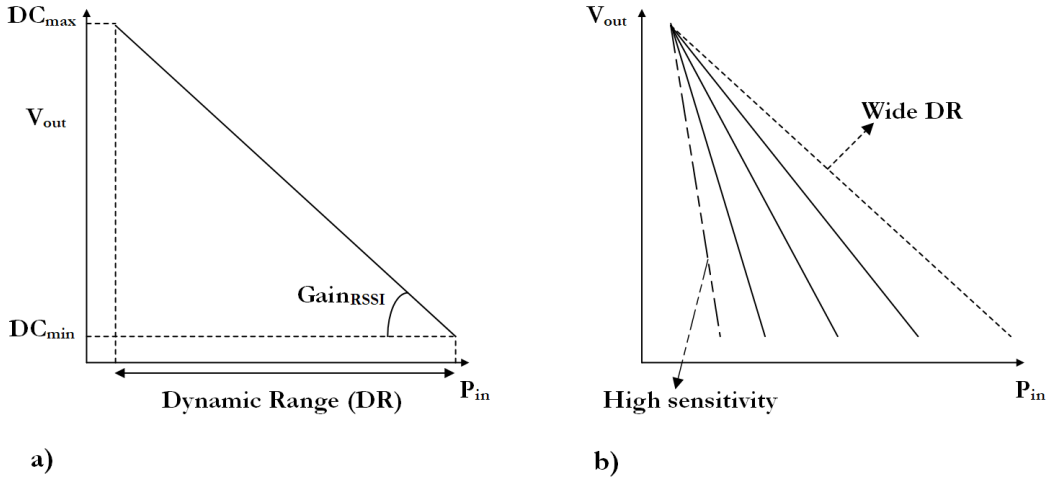


Figure 3.27: Tradeoff between Dynamic Range and detection sensitivity.

This relation is exemplified in Fig. 3.27 b). With limited supply voltage, widening the Dynamic Range mandatorily limits the detection sensitivity. This is particularly problematic for low supply voltages, which is the case for this project.

Another important figure of merit for the RSSI is the logarithmic linearity error. It is defined as the error between the output and a linear-in-dB best fit curve and is measured in dB. It provides a measure of how linear (in dB) the transfer function of the RSSI is. The logarithmic linearity error is given by Eq. 3.23 [32].

$$Error_{max}[dB] = \frac{10\left[(-1+\sqrt{A}+A)\log A-(A-1)\log A^{(3A-1)/(2A-2)}\right]}{A-1} \tag{3.23}$$

Where A is the gain per stage of the Limiting Amplifier in dB. Although the error is directly dependent on the gain of each Limiting Amplifier's gain cell, it is more useful to analyse it in terms of number of limiting gain stages. In other words, for a given overall Limiting Amplifier gain, A_t, the gain per cell is equal to $A = A_t/N$, where N is the number of limiting stages. So, the variation of the maximum logarithmic error is measured as a function of the number of cascaded stages. Such relation is represented in Fig. 3.28 for an overall Limiting Amplifier gain of 60 dB.

The graphic in Fig. 3.28 tells that when $A \geq 5$ the maximum RSSI's error is always less than unit. 1 dB of error is more than acceptable for the current application. This means that more than 5 cascaded stages are enough to fulfil the error specification. Still, since the number of limiting stages was already defined by other design constrains, and is equal to 9, the maximum error is expected to be less than 0.4 dB.

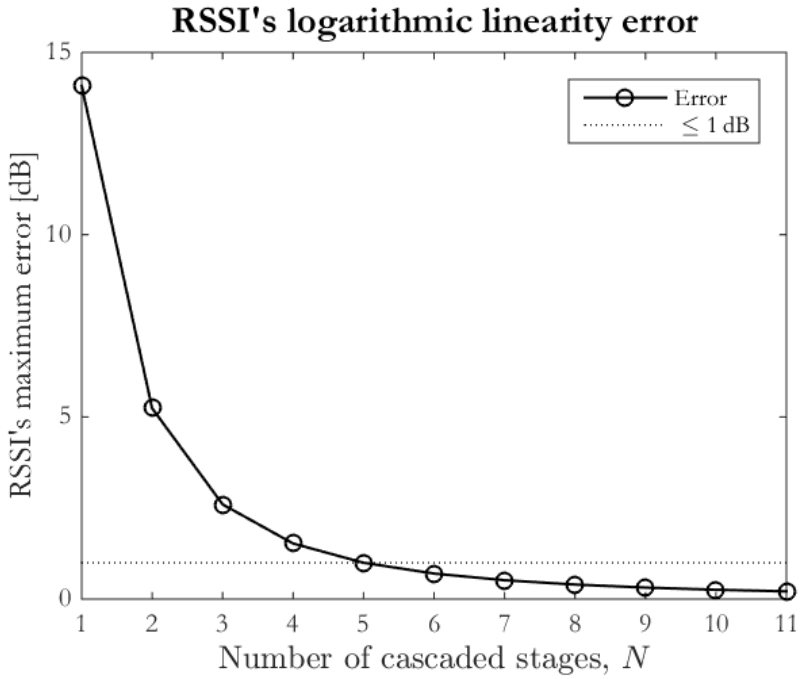


Figure 3.28: RSSI's logarithmic linearity error as a function of the LA's number of cascaded stages.

3.2.1 Full-Wave Rectifier

The proposed architecture for the FWR consists of two identical unbalanced source-coupled differential pairs, whose gates are connected cross-coupled and the outputs (drains) are connected in parallel [33]. Such an arrangement is depicted in Fig. 3.29. The first unbalanced differential pair is composed by transistors M_1 and M_2 and the second one by transistors M_3 and M_4. The transistors' dimensions of M_1 and M_4 are k times larger than the ones of M_2 and M_3.

The working principle is the following: when no signal is present at the input, the current that flows at the output, I_{out}, will be at its maximum value, which depends on the unbalancing factor, k. When the input voltage is relatively small, the wider transistors, M_1 and M_4, will consume most of the current available from the current sources, I_o. Since their drains are connected together, the current that flows through M_5 will be larger that the one at M_6. Assuming that mirroring errors are negligible, the current at the output is given by $I_{D_5} - I_{D_6}$. As the input voltage starts to increase, the narrower transistors will experience a greater relative increase in the current than the wider ones, and they will start to steal more current from the current sources. Therefore, the current flowing through M_6 starts to increase, and the output current I_{out} decreases. I_{out} will be almost zero when the differential input is large enough to the make current flowing through M_6 equal to current flowing in M_5.

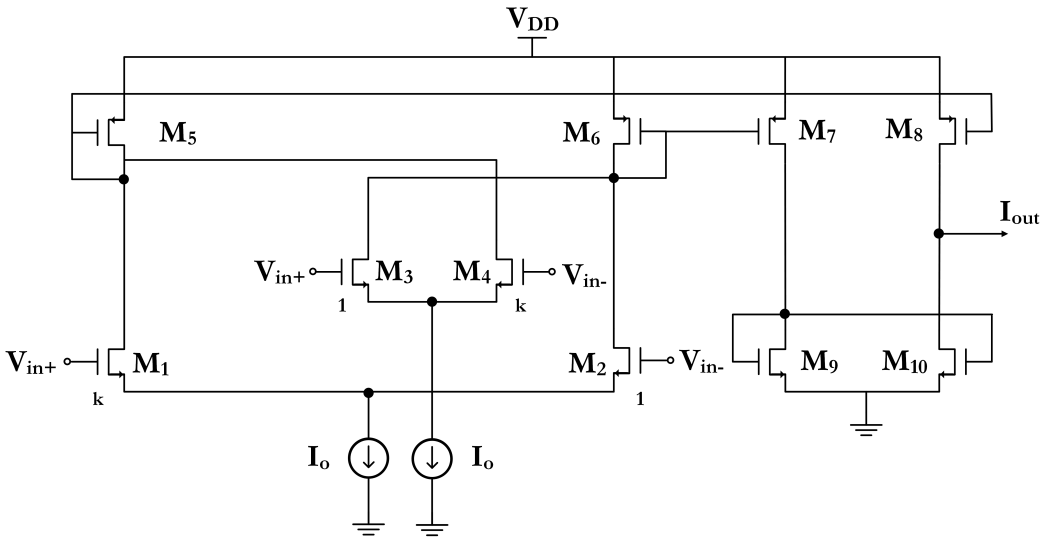


Figure 3.29: FWR's architecture.

The advantage of this topology is that it is differential, thus loading both sides of the Limiting Amplifier's gain cells in the same manner. Furthermore, since the rectifier configuration has only three stacked transistors, it can operate at low supply voltages. In pratice, the current that flows through M_6 is mirrored to M_7 and sinked by M_9 which mirrors it to M_{10}. The current through M_5 is directly mirrored to M_8. Hence, the output current I_{out} is the difference between M_8 and M_{10}'s currents. In the following analysis the mirroring errors are ignored therefore the output current is just given by the difference between M_5 and M_6's currents.

Let us now analyse in more detail how the rectification is performed in the current domain. First of all, assuming that all the devices are operating in saturation and are perfectly matched, the output differential currents (ΔI_{D_1} and ΔI_{D_2}) for both unbalanced differential pairs can be calculated under the assumption that $\left|\Delta I_{D_{1,2}}\right| \leqslant I_o$. Where β is the transconductance parameter, given by $\mu(C_{ox}/2)(W/L)$ with effective surface mobility μ, the gate capacitance per unit area C_{ox}, the gate width W and the gate length L. Also, k is the unbalancing factor and is assumed to be bigger than unit. The current flowing to the drain of a MOSFET in saturation is generally given by $I_D = \beta(V_{gs} - V_T)^2\,[1 + \lambda_D(V_{ds} - V_{dsat})]$. Neglecting channel length modulation effects, the former expression simplifies to $I_D = \beta(V_{gs} - V_T)^2$. So, it is possible to write the expressions for the drain currents of the differential pairs' transistors, Eq. 3.24 and Eq. 3.25.

$$\begin{cases} I_{D_1} = k\beta(V_{gs1} - V_{T1})^2 \\ I_{D_2} = \beta(V_{gs2} - V_{T2})^2 \end{cases} \Leftrightarrow \begin{cases} V_{gs1} = \sqrt{I_{D_1}/k\beta} + V_{T1} \\ V_{gs2} = \sqrt{I_{D_2}/\beta} + V_{T2} \end{cases} \tag{3.24}$$

$$\begin{cases} I_{D_3} = \beta(V_{gs3} - V_{T3})^2 \\ I_{D_4} = k\beta(V_{gs4} - V_{T4})^2 \end{cases} \Leftrightarrow \begin{cases} V_{gs3} = \sqrt{I_{D_3}/\beta} + V_{T3} \\ V_{gs4} = \sqrt{I_{D_4}/k\beta} + V_{T4} \end{cases} \tag{3.25}$$

It is also possible to define the differential input voltages, V_1 and V_2 as a function of the transistors' drain currents. Adding the obvious relation that states that the sum of the currents in each differential pair is equal to bias current, a two equation two inconigta system is obtained (one for each differential pair), Eq. 3.26 and Eq. 3.27.

$$\begin{cases} V_1 = V_{gs1} - V_{gs2} = \sqrt{I_{D_1}/k\beta} + V_{T1} - \left(\sqrt{I_{D_2}/\beta} + V_{T2}\right) = \sqrt{I_{D_1}/k\beta} - \sqrt{I_{D_2}/\beta}, V_{T1} = V_{T2} \\ I_{D_1} + I_{D_2} = I_o \end{cases} \tag{3.26}$$

$$\begin{cases} V_2 = V_{gs3} - V_{gs4} = V_{gs1} - V_{gs2} = V_1 = \sqrt{I_{D_3}/\beta} + V_{T3} - \left(\sqrt{I_{D_4}/k\beta} + V_{T4}\right) = \sqrt{I_{D_3}/\beta} - \sqrt{I_{D_4}/k\beta}, V_{T3} = V_{T4} \\ I_{D_3} + I_{D_4} = I_o \end{cases} \tag{3.27}$$

Solving 3.26 for I_{D_1} and I_{D_2}, it is possible to calculate the output differential current $\Delta I_{D_1} = I_{D_1} - I_{D_2}$. The same logic aplies to ΔI_{D_2}. Therefore, the following expressions are obtained:

$$\Delta I_{D_1} = I_{D_1} - I_{D_2} = \begin{cases} \frac{I_o(k^2-1) - 2\beta k V_1^2 (k-1) + 4V_1\sqrt{\beta k^2\left(I_o + I_o k - \beta k V_1^2\right)}}{(k+1)^2}, -\sqrt{I_o/\beta} < V_1 < \sqrt{I_o/k\beta} \\ I_o sgn(V_1), V_1 \leq -\sqrt{I_o/\beta}, V_1 \geq \sqrt{I_o/k\beta} \end{cases} \tag{3.28}$$

$$\Delta I_{D_2} = I_{D_3} - I_{D_4} = \begin{cases} \frac{I_o(k^2-1) + 2\beta k V_1^2 (k-1) + 4V_1\sqrt{\beta k^2\left(I_o + I_o k - \beta k V_1^2\right)}}{(k+1)^2}, -\sqrt{I_o/k\beta} < V_1 < \sqrt{I_o/\beta} \\ I_o sgn(V_1), V_1 \leq -\sqrt{I_o/k\beta}, V_1 \geq \sqrt{I_o/\beta} \end{cases} \tag{3.29}$$

As mentioned before, the output current, I_{out}, neglecting the mirroring errors, is given by Eq. 3.30.

$$\begin{gathered} I_{out} = I_{D_5} - I_{D_6} = (I_{D_1} + I_{D_4}) - (I_{D_2} + I_{D_3}) = \Delta I_{D_1} - \Delta I_{D_2} = \\ \begin{cases} 2\frac{k-1}{k+1} I_o - 4\frac{k(k-1)\beta V_1^2}{(k+1)^2}, |V_1| \leq \sqrt{I_o/k\beta} \\ -2(k-1)k\beta V_1^2 - 4k\beta|V_1|\sqrt{(k+1)\frac{I_o}{\beta} - kV_1^2} + \frac{2kI_o}{k+1}, \sqrt{I_o/k\beta} < |V_1| < \sqrt{I_o/\beta} \\ 0, |V_1| \geq \sqrt{I_o/\beta} \end{cases} \end{gathered} \tag{3.30}$$

The FWR transfer function, normalised output current, I_{out}/I_o as a function of input normalised differential voltage, $\frac{V_1}{\sqrt{I_o/\beta}}$, is represented in Fig. 3.30, for different values of the unbalancing factor, k (for a bias current, I_o, of 10 µA). It is possible to confirm that for smaller values of input voltage the output current will be at its maximum value, approaching zero as the input voltage increases.

As mentioned before, the maximum value for I_{out} depends on the unbalancing factor, k. The maximum value for the normalised current is 2, since it corresponds to the case where k is so large that no current is steered by the narrower transistors and thus, the output current is given by the double of the bias current, I_o. So, the maximum value for the current increases as the unbalancing factor does. Furthermore, it shows that the value of k has to be carefully optimised since the relationship between the input voltage and the output current features a parabolic characteristic and is proportional to $1/\sqrt{k}$. At the same time, the unbalancing factor also plays a determinant role in the detection sensitivity of the RSSI.

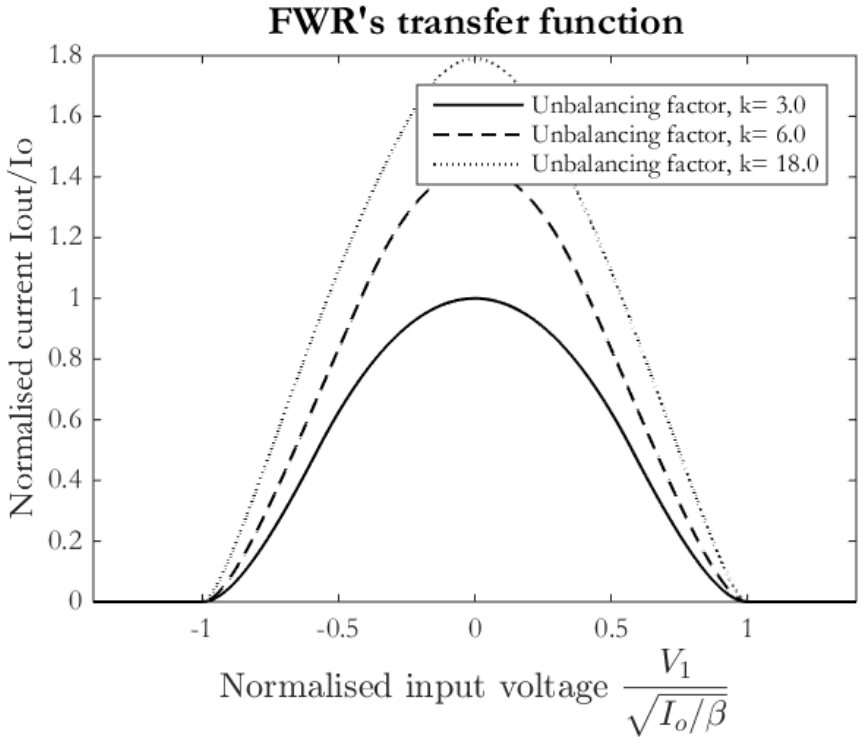


Figure 3.30: FWR's transfer function for different values of the unbalancing factor, k.

In order to study this matter in more detail let us consider the modeled transfer function of the overall RSSI and of the correspondent FWRs, meaning the nine FWRs fed by the LA's gain cells, for $k = 3$. Obviously, each FWR receives a different input differential voltage, meaning the first one receives a smaller amplitude signal than the last one, where for sure the Limiting Amplifier has already saturated. For this reason, the last FWRs are responsible for processing larger amplitude signals and the first FWRs less powerful ones. This situation is illustrated in Fig. 3.31. The overall transfer function, which is the sum of the currents originating from the nine FWRs, presents a maximum current of $9I_o$ and a Dynamic Range between -35 dBm to 20 dBm (for a bias current I_o of 10µA). When one FWR saturates the other ones "replaces" it, resulting in an almost continues transfer function. These transfer functions were obtained using the mathematical models presented before (expression 3.30).

The RSSI transfer function is calculated as the sum of each FWR transfer function. The input of each FWR is calculated assuming a gain of 2.15 for the LA's gain cells and saturation for the FWR's input differential signals with peak-to-peak amplitudes larger than 1.4 V (which models the behaviour of the real Limiting Amplifier).

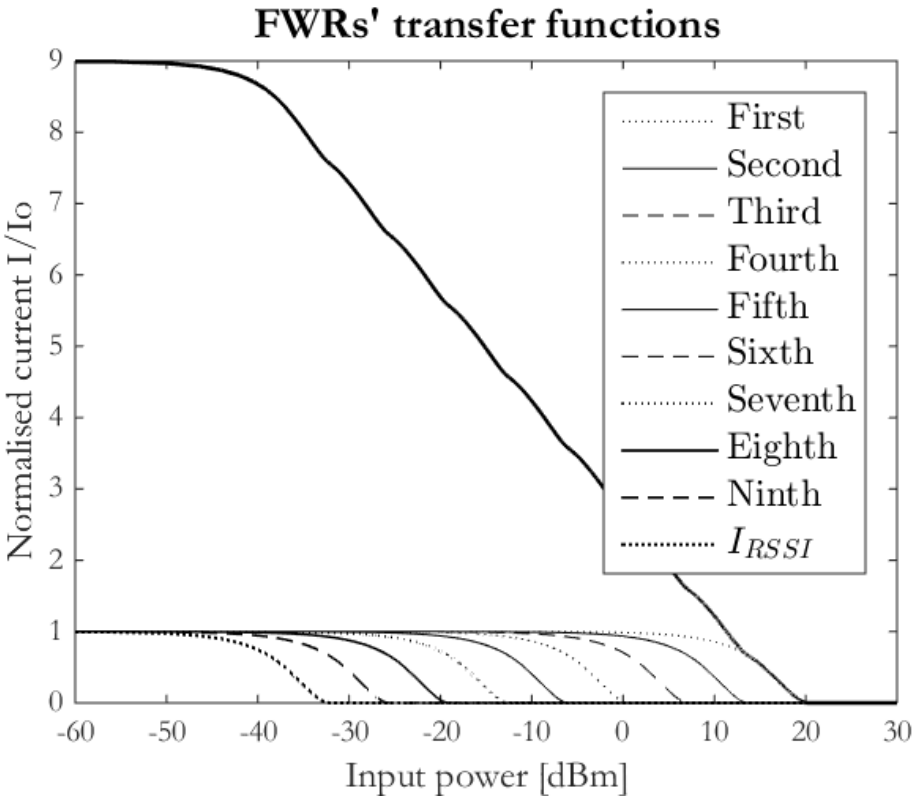


Figure 3.31: Modeled RSSI's and FWRs' transfer functions.

It was already mentioned that the detection sensitivity is one of the most important metrics for the RSSI. Its value is mainly related to the value of the bias current, I_o, the filter resistor R_{LOAD} and the value of the unbalancing factor, k. Increasing the bias current of each FWR would certainly improve the detection sensitivity, but the power consumption of the overall block would exceed the allowed value, which is about 600 µW. So, let us study the variation of the sensitivity with the unbalancing factor k, for a bias current I_o =10 µA (which meets the overall block power specifications) and a filter resistor of 11 kΩ. Such analysis is illustrated in Fig. 3.32 a) and b).

Thoroughly analysing Fig. 3.32 a) one can see that although the slope - detection sensitivity - of the curves is increasing with k the Dynamic Range is kept constant. The explanation for this is that the current's maximum value is also increasing with k, as previously observed (Fig. 3.30). This makes possible the increase of the detection sensitivity without deteriorating the RSSI's Dynamic Range. Fig. 3.32 b) shows the variation of the slope as the unbalancing factor increases. For values of k smaller than 10 the improvement in the sensitivity is much more evident, which indicates that this is the best working range.

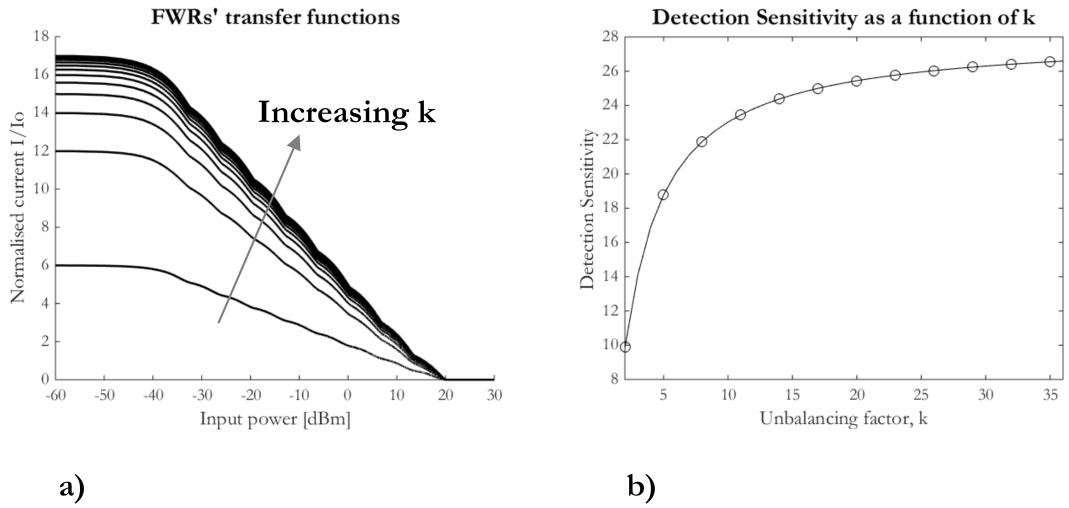


Figure 3.32: a) FWR's transfer functions for different values of the unbalancing factor, k. b) Detection sensitivity as a function of the unbalancing factor, k.

Ideally, it would be better to work with k values between 5 and 10, where the sensitivity presents much more satisfactory values. Unfortunately, the increase of the unbalancing factor goes hand in hand with a decrease of the Limiting Amplifier's bandwidth due to the load effect presented at the output of each gain cell. For this reason, the chosen value for the unbalancing factor was 3, which is the one that minimises the LA's bandwidth run-out providing an acceptable detection sensitivity value, approximately 17 mV/dB, according to the developed models.

Table 3.11 presents the components' dimesions for each FWR and for the RSSI's output RC-filter. The cut-off frequency of the filter is approximately 2.7 MHz. The channel length of transistors $M_{5,6,7,8,9,10}$ was chosen to be large in order to minimise the mirroring errors, which is essencial since the bias current is relatively small and the output current of each FWR is the subtraction of M_8 and M_{10} (which are mirrored by M_5 and M_9, respectively).

Table 3.11: Components' dimensions of the RSSI.

Transistor	Size [µm]
$M_{1,4}$	3/0.06
$M_{2,3}$	1/0.06
$M_{5,6,7,8}$	72/3
$M_{9,10}$	12/9
Resistor	**Size [kΩ]**
R_{LOAD}	10
Capacitor	**Size [pF]**
C_{LOAD}	6

3.2.2 PVT Independent Bias

In order to supress the PVT variations, and therefore, maintain the RSSI's transfer function constant, it is of the greatest importance to have a dynamic bias architecture that can help overcome these variations. First of all, the output of the RSSI, $V_{STRENGTH}$, is obtained by summing the rectified currents of all the FWRs at an on-chip resistor. The effective value of the resistor, R_{LOAD} can vary up to 30% from its nominal value due to process and temperature. The solution is to have the bias circuit adapting the bias currents in such a form that can track the on-chip resistor value. Also, it is necessary to find a way for the bias current to be independent from the supply voltage, which is excepted to vary 10% from its nominal value.

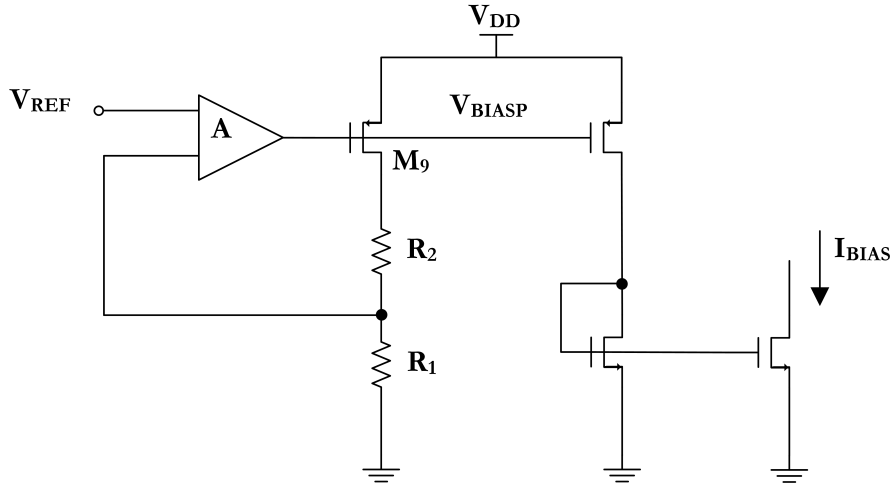


Figure 3.33: RSSI's PVT independent bias circuit.

The proposed architecture is illustrated in Fig. 3.33 [32].

The circuit will be used to bias all the FWRs cells. Amplifier A forces its input differential voltage to be zero using the negative feedback loop, so that the voltage across resistor R_1 equals the reference voltage, V_{REF}. To maintain the output voltage V_{REF} constant, the current has to be adjusted to even the changes in the resistor value. The amplifier adjusts the current of the resistors by tuning the bias voltage of the PMOS transistor M_9, V_{BIASP}. Voltage V_{REF} is generated by a bandgap reference circuit with low temperature dependence (the bandgap circuit is not the focus of this work so it will not be discussed in more detail). Let us now study in more detail the behaviour of the presented bias generator and how it helps solve the PVT variations of the output voltage. Neglecting the mirroring errors, the current I_{BIAS} can be defined as:

$$I_{BIAS} = \frac{V_{REF} \pm \frac{V_{REF}}{1+G_{loop}}}{R_1} \tag{3.31}$$

From Eq. 3.31, if the bandgap reference V_{REF} is fixed, the bias current will only depend on the value of resistor R_1 and the gain of the loop. The dependence on the loop gain is not much of a concern because, for a loop gain larger than 40 dB, the voltage error is smaller than 1% (therefore it will be ignored in further analysis). The bias current, at this moment, does not show any direct dependence on the supply voltage. The output current of the RSSI - I_{RSSI} - (the sum of all the FWR's currents) can be aproximate to (considering a mirror relation of 1:1 between I_{BIAS} and I_o):

$$I_{RSSI} = \gamma I_{BIAS} log V_1 \tag{3.32}$$

Where γ is a coefficient that determines the relation between the logarithm of the input voltage and the output current of the overall RSSI. Therefore, the output voltage is given by Eq. 3.33.

$$V_{STRENGTH} = R_{LOAD} I_{RSSI} = \frac{R_{LOAD}}{R_1} \gamma V_{REF} \log V_1 \tag{3.33}$$

If R_{LOAD} and R_1 are built with the same type of on-chip resistors and placed very closely to each other, their matching would be satisfactory and the output voltage would be nearly independent of process, temperature and supply variations. The only problem are the changes on the γ since its value would depend on the mirroring errors between the transistors of the FWRs and in the bias circuit itself. Obviously, the mirroring errors strongly depend on supply voltage and lightly on temperature. Also, the Dynamic Range of the RSSI is strongly depedent on the gain of the Limiting Amplifier and, since this value is quite variable across corners, so will the Dynamic Range of the RSSI.

In order to implement the PVT independent bias circuit it is necessary to design an amplifier that keeps the voltage drop across resistor R_1 equal to the reference voltage V_{REF}. Voltage V_{REF} is generated by a bandgap circuit, as mentioned before, and its value is lower than 300 mV. This implies that the first stage of the amplifier (which is differential) needs to the composed by a PMOS differential pair. Its architecture is portrayed in Fig. 3.34. The first gain stage is a PMOS differential pair with NMOS active loads and single-ended output. The second stage is a NMOS common-source configuration with a PMOS active load. The second stage attacks the gate of transistor M_9 which produces the bias current for the RSSI. The current of transistor M_9 is then mirrored to another PMOS transistor through V_{BIASP} and sinked by an NMOS one and further mirrored to all the FWRs, as schematised in Fig. 3.33.

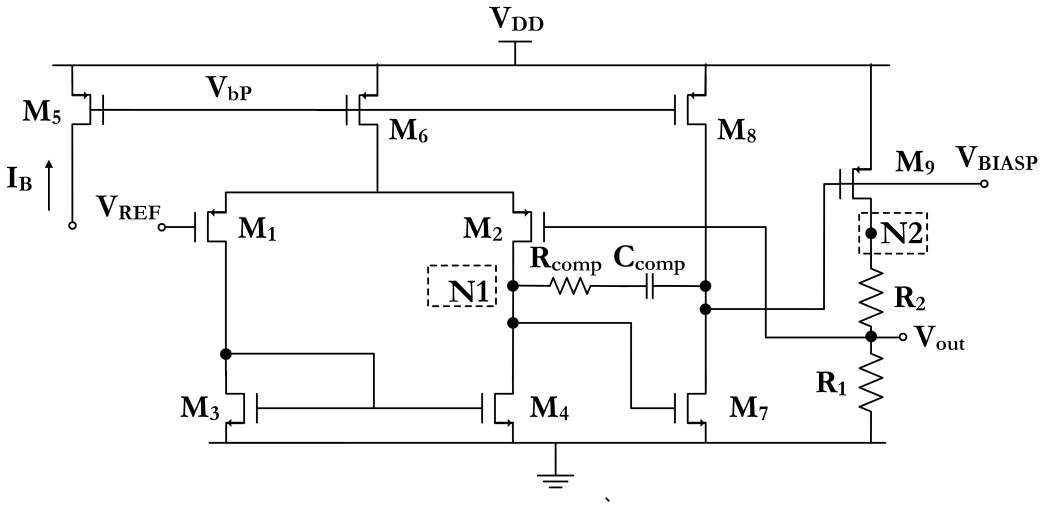


Figure 3.34: RSSI's bias circuit amplifier.

As any loop, it has to be designed to be unconditionally stable but seeing that this is almost a DC operation the bandwidth requirements of the loop are relatively low, which makes the stability compensation really straightforward (not forgetting that the feedback has to be capable of compensating for temperature changes and for that the necessary bandwidth is of a few kHz). Resistor R_{comp} and capacitor C_{comp} provide for stability compensation.

$$G_{loop} = \frac{g_{m2}g_{m7}}{(g_{ds4}+g_{ds2})(g_{ds7}+g_{ds8})} g_{m_9 R_1} \tag{3.34}$$

By inspection, the DC gain of the loop is given by Eq. 3.34. The dominant pole is located, by design, in node $N1$ and its expression is easily determined using Miller's Theorem:

$$\omega_p = \frac{g_{ds2}+g_{ds4}}{C_{comp}(1+\frac{g_{m7}}{g_{ds8}+g_{gds7}})} \tag{3.35}$$

Table 3.12 presents the components' dimensions for this circuit.

3.2.2.1 Simulation Results

Now that the PVT independent bias circuit and its sub-circuits have been presented, let us analyse the simulation results for this circuit and its improvements in the variations of the RSSI's transfer function.

Table 3.12: Components' dimensions of the RSSI's bias circuit amplifier.

Transistor	Size [µm]
$M_{1,2}$	80/1
$M_{3,4}$	4/0.24
M_5	2/1
$M_{6,8}$	4/1
M_7	4/0.24
M_9	20/1
Resistor	**Size [kΩ]**
R_1	14
R_2	14
R_{comp}	12
Capacitor	**Size [pF]**
C_{comp}	11.89

Table 3.13: Estimated and simulated results of the RSSI bias circuit's amplifier.

	DC gain [dB]	Bandwidth [kHz]	GBW [MHz]	Phase Margin [°]	Power [μW]
Estimated	71.8416	2.7661	10.8130	-	-
Simulated	71.0042	2.6433	9.3833	65.43	98

Table 3.13 presents some estimated and simulated metrics regarding the RSSI bias circuit's amplifier. One can see that the DC gain is about 71 dB which results in a voltage error much smaller than 1%. In this case it is very important to minimise the voltage error of the amplifier, since the reference voltage is supplied by the bandgap and its value will change across corners. So, all the variations in the voltage across resistor R_1 have to be minimised in order to supress the transfer function's variations across the PVT corners. The phase margin of the loop is about 65° which is more than enough to grant unconditional stability. Again, the variations across process corners of capacitor C_{comp} force that the phase margin in the typical corner is larger than 60°.

In order to analyse the performance of this bias circuit in supressing the RSSI's transfer function variability across corners, let us compare the performance to a regular bias circuit. Three opposing corners are presented and the transfer functions of the RSSI with a normal biasing circuit are illustrated in Fig. 3.35.

Looking at Fig. 3.35 it is possible to see a clear variation with the supply voltage since the maximum value for $V_{STRENGTH}$ increases or decreases its value according to the change in the supply voltage. The process and temperature variations are also visible with the changes on the detection sensitivity (slope) of the curves.

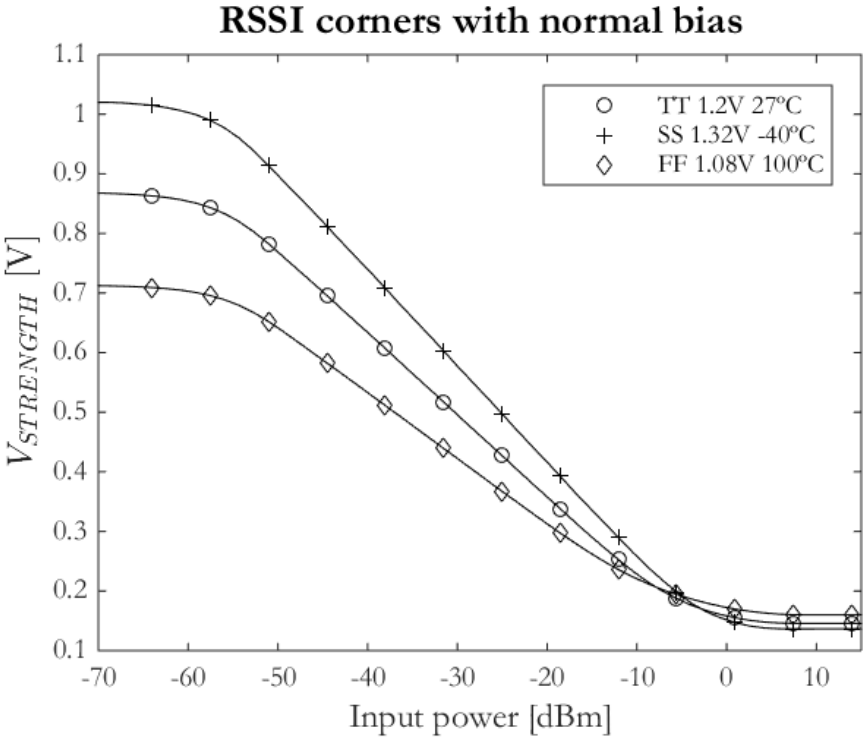


Figure 3.35: Variation of the RSSI's transfer function across corners using a normal bias circuit.

Fig. 3.36 provides the exact same analysis albeit the PVT independent bias is used instead of a regular one. By looking at Fig 3.36 it is clear to see the improvement in the variation across corners for the RSSI curve. Although the dependence on V_{DD} is still visible (majorly due to the mirroring errors which increase as the supply decreases) the detection sensitivity is kept almost constant for the different corners.

A detailed comparison between the two bias architectures is presented in Table 3.14. With the regular bias circuit, the variations in the detection sensitivity against the typical corner can go up to 26%. With the bias architecture used in this work the maximum variation is about 9%. In the SS corner, the variation is only of 2% whereas with the regular bias circuit is 18%. These measurements are only considering the changes in the detection sensitivity while the variations in the maximum and minimum levels of $V_{STRENGTH}$ were not considered.

These simulations were done with an "ideal" LA since their purpose is to study the variations caused by the RSSI and its bias circuit, and not the ones caused by the LA. As mentioned before, the gain changes in the LA have a large impact in the DR of the RSSI and consequently in the detection sensitivity.

Fig. 3.37 shows the simulations of the RSSI with the PVT independent bias circuit using the real LA. One can see that the variations, for the exact same corners, are much more pronounced. This can be explained by the DC gain variations of the LA that have a direct impact in the RSSI's Dynamic Range.

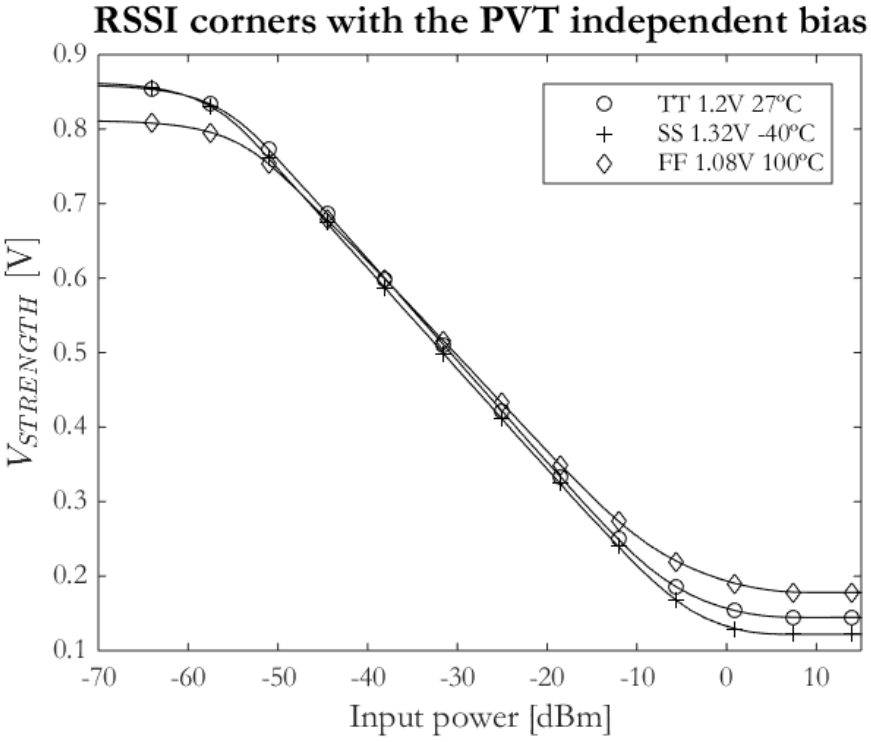


Figure 3.36: Variation of the RSSI's transfer function across corners using the proposed PVT independent bias circuit.

Table 3.14: Variations on the detection sensitivity across corners using the proposed PVT independent bias vs a normal bias circuit.

Detection Sensitivity [mV/dB] Relative error in relation with typical corner [%]	SS 1.32V -40ºC	TT 1.2 V 27º	FF 1.08V 100ºC
PVT independent bias	12.7 2	12.4 -	11.3 9
Normal bias	15.2 18	12.9 -	9.6 26

Although the gain of the Limiting Amplifier does not directly impact the detection sensitivity, it ends up changing it. This is because the DR changes whereas the DC maximum and minimum levels of $V_{STRENGTH}$ remain almost constant. Meaning, if the DR increases and the levels of $V_{STRENGTH}$ are the same, the detection sensitivity will mandatorily decrease, which is the case of the SS 1.32 V −40 °C corner, where the gain of the LA is at its maximum. In the FF corner where the LA's gain drops to 43.2 dB, the Dynamic Range decreases and the detection sensitivity increases.

Although these variations are undesirable, there is no simple solution for them since the LA's gain will inevitably change. In pratice, after manufacture, the RSSI's transfer function can be measured and the system is calibrated to read and correctly interpret the output for different values of temperature and supply.

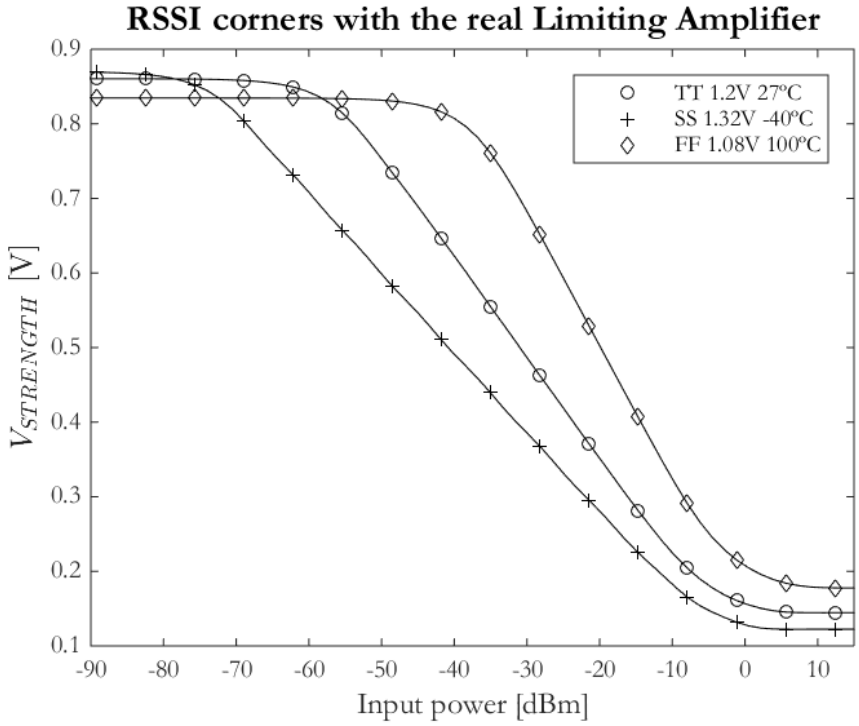


Figure 3.37: Variation of the RSSI's transfer function across corners using the proposed PVT independent bias circuit with the real LA.

3.2.3 Simulation Results

Now that the RSSI's architecture and its biasing circuit were already presented let us analyse the final simulation results concerning this block. A PRBS sequence at 5 and 2.5Gb/s within a range of amplitudes was fed at the input of the Limiting Amplifier. Each stage of the LA was connected to a FWR as schematized in Fig. 3.26. The RSSI's output voltage, $V_{STRENGTH}$, was plotted as a function of the power of the signals at the input of the LA. The respective transfer functions, at 5Gb/s and 2.5Gb/s are presented in Fig. 3.38. One can see that curve for a PRBS sequence at 5Gb/s is not exactly equal to the one at 2.5Gb/s which is mainly related to the bandwidth of the FWRs. The values of the detection sensitivity and the Dynamic Range for both situations are presented in Table 3.15 as well as the power consumption of the overall circuit (including the bias circuit).

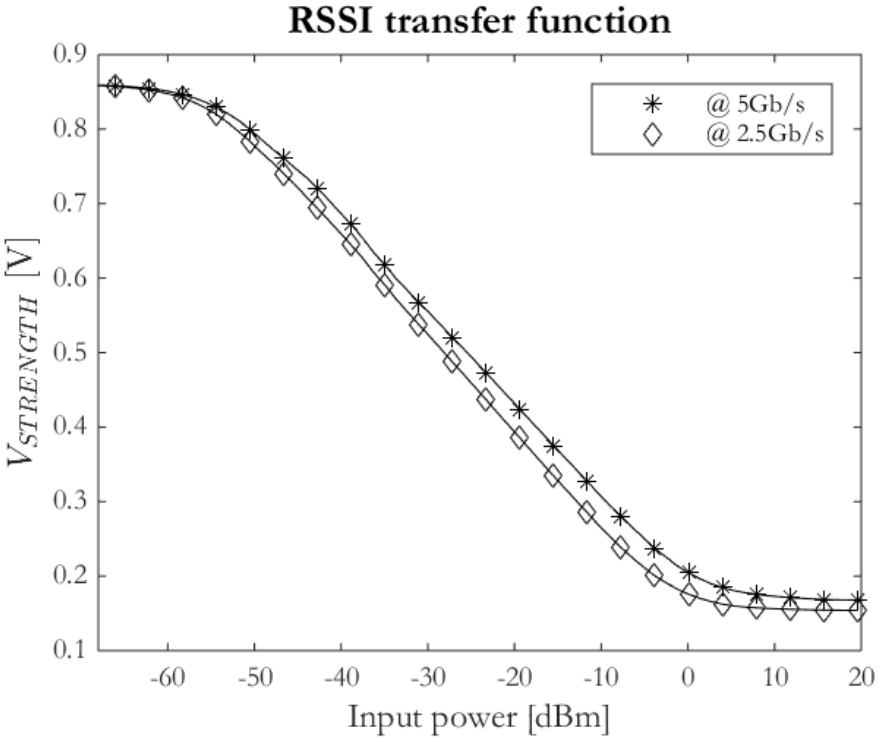


Figure 3.38: RSSI's transfer function at 5 and 2.5Gb/s.

Table 3.15: RSSI's simulation results for two different working frequencies.

	Detection Sensitivity [mV/dB]	Dynamic Range [dB]	Power [μW]
@2.5 Gb/s	12.3	50.1	533
@5 Gb/s	11.6	52.7	

The power dissipation of the circuit is below the targeted value of 600 µW (including bias). The Dynamic Range of the RSSI is slightly larger at 5Gb/s whereas the detection sensitivity is larger for 2.5 Gb/s. The Dynamic Range is about 50 dB at 2.5 Gb/s and nearly 53 dB at 5Gb/s. Both values are below the gain of the LA which is expected since, at the limit, the Dynamic Range is bounded by the gain of the Limiting Amplifier.

Lastly, it is also interesting to analyse the measured logarithmic error for both situations and see if it is below 0.4 dB which is theoretically expected. Fig. 3.39 shows the logarithmic error as a function of the input power at the LA.

One can see that, within the Dynamic Range of both curves, this value is always below 0.4 dB. The logarithmic error was calculated by finding the best linear-in-dB fit curve to each curve, and then calculating the error to the best fit curve for every point. This metric gives an idea of how linear (in dB) the transfer function of the circuit is. The lower the error the linear the curve, improving the reliability of the circuit and of the information provided by it.

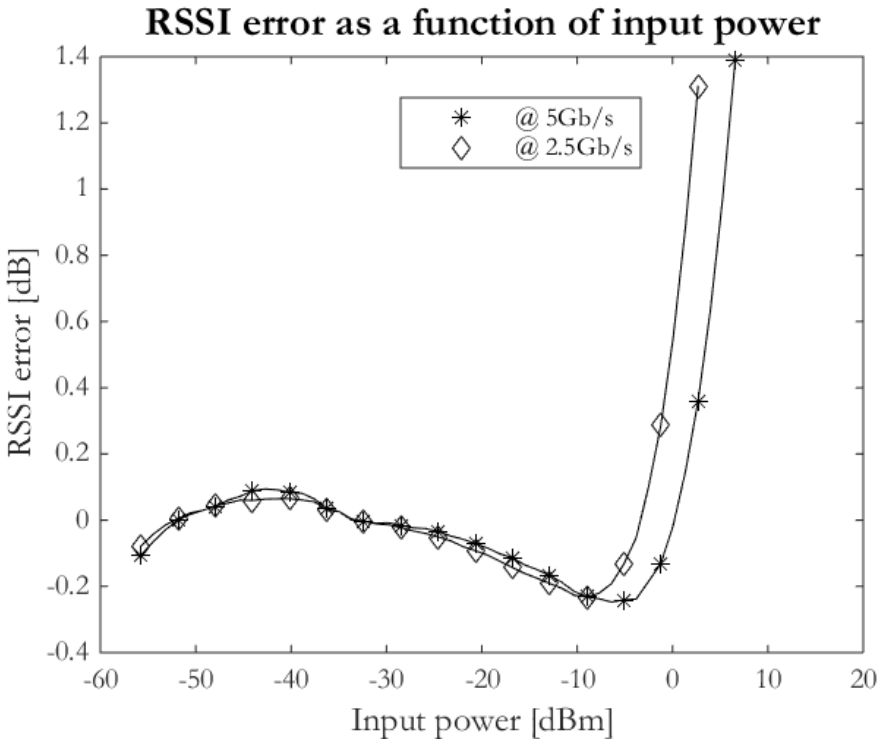


Figure 3.39: RSSI's logarithmic error at 5 and 2.5Gb/s.

3.2.4 Layout

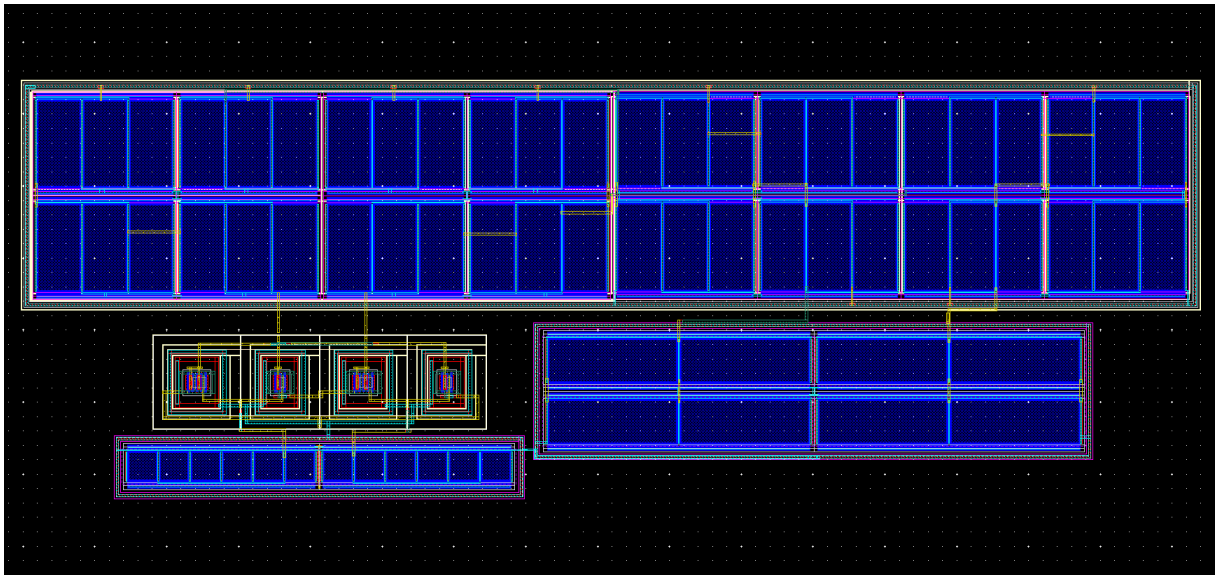
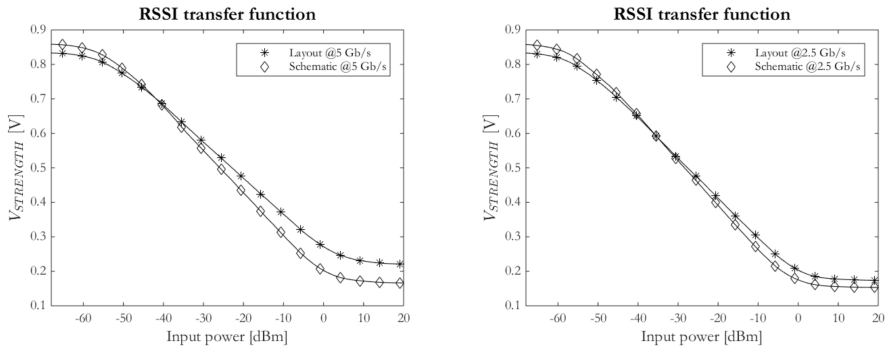


Figure 3.40: Layout of the RSSI's FWR.

Fig. 3.40 is the layout of each RSSI's FWR. The total layout area for the FWR cell is approximately 2151 μm^2 (0.3073%) on the IC. The layout vs schematic simulations of the RSSI's transfer function before and after the layout are presented in Fig. 3.41 a) at 5Gb/s and in Fig. 3.41 b) for 2.5Gb/s. It is possible to observe that, in both cases, the detection sensitivity is slightly small but the Dynamic Range remains almost unchanged. For 2.5Gb/s the layout transfer function is almost equal to the schematic one. This would suggest that the bandwidth of the FWR was slightly reduced during the layout.



a) **b)**

Figure 3.41: RSSI's transfer function at a) 5Gb/s and b) 2.5Gb/s - layout vs schematic.

3.3 Squelch

The Squelch block is an addition to the RSSI and it allows to "mute" the output when the input power is not strong enough. Meaning, when the Photodiode current, at the input of the TIA, is below the sensitivity limit of the Optical Receiver the resulting waveform, at the output of the buffer, will not meet the BER specifications. This is because, the BER is a direct function of the SNR at the output of TIA (considering that the LA does not degrade the noise figure). The SNR of the signal at the output of the transimpedance amplifier depends on two parameters: the output signal's amplitude and the integrated noise across the TIA's bandwidth. The first one is related to the input signal's amplitude and to the gain of the TIA (which is fixed by design - ignoring temperature and supply variations). The integrated noise also remains constant through time after manufacture, except for voltage and temperature variations. These three parameters give the SNR and therefore the expected BER of the overall Optical Receiver. Ignoring the temperarature and supply variations, there will be a minimum SNR to which the BER still falls within the specified value (10^{-12} in this case). Assuming that the gain and the integrated noise, σ_N, do not change, the only thing that changes the SNR at the TIA is the input signal's amplitude. Meaning, there is a minimum value for the input signal's amplitude in order to achieve a given BER - sensitivity limit. Note: All the figures with NMOS and PMOS with undefined bulk have their bulk connected to ground and V_{DD}, respectively.

This means that, below a certain input signal's amplitude value the output signal will no longer have interest since its BER is above the application limit. When this happens, there is no advantage in having the Output Buffer working. Furthermore, there is also the case when, for some unknown reason, the input signal ceases and the resulting signal is no more than amplified noise. Muting the Output Buffer, supresses the output toggling due to noise and also reduces the overall Optical Receiver power consumption.

In order to do this, it is necessary to have a measure of the input signal's power, in order to compare that measure to a predefined threshold value - Squelch threshold. The circuit that provides a measure of the signal's strength is the RSSI. If the RSSI's transfer function is known, one can find the RSSI's output that corresponds to a certain input power. Once the Squelch threshold is defined (meaning, the value for the input signal's amplitude where there is no interest in the output), it is possible to find what is the value of the output voltage produced by the RSSI for that specific value of input power. The RSSI output is then constantly compared to the Squelch's threshold. If the output signal of the RSSI, $V_{STRENGTH}$, is larger than the Squelch's threshold, a control signal is activated and the Output Buffer is disconnected, forcing the output to be constant. In addition, there is an external control signal that enables or disables the Squelch function - Enable.

The Squelch is only activated if the RSSI's output is larger than the threshold voltage, simultaneously with the Enable signal being logic high. The key idea is represented in Fig. 3.42. The Squelch's threshold value does not have to match the sensitivity limit. Although the input signal's power may be below the sensitivity limit, it is good to have a safety margin and ensure that the Squelch is not actived for useful input power levels. Hence, the Squelch's threshold is usually below the Optical Receiver's sensitivity limit.

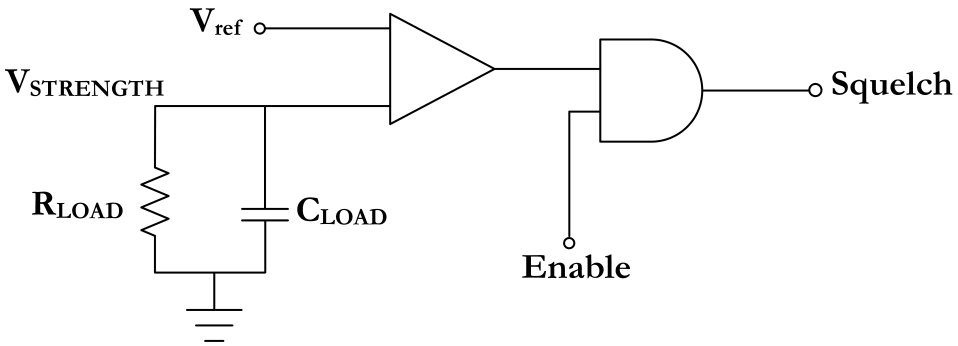


Figure 3.42: Squelch's working principle.

The major difficulty while designing this block is making sure that the control signal responsible for the Squelch decision is not active for incorrect values of input power. In other words, ensuring that no useful signal is lost due to incorrect activation of the Squelch control signal.

The faulty activation of the Squelch signal can happen due to two different reasons. The first is the corners variations of the RSSI's transfer function and of the Squelch threshold voltage, V_{ref}. The second one is the possibilty of a high-energy particle striking the comparator responsible for comparing voltages $V_{STREGTH}$ and V_{ref}. If that situation were to happen, the comparator could swap states and wrongly indicate that the voltage $V_{STRENGTH}$ is bigger than V_{ref}. If the Enable is ON, then the Squelch command would be activated and the data would be lost. Both situations result in a loss of the input data even though the second situation is more unpredictable, and cannot be tested during the design process.

The first problem is easily solved, instead of creating the reference voltage V_{ref} with a bandgap circuit, it is generated using the same current that it used to bias the RSSI. This way, it "feels" the same PVT variations as the RSSI. So, the shifts in the $V_{STRENGTH}$ value for a given input power will be tracked by the Squelch's threshold voltage, V_{REF}. The reference V_{REF} is taken from the voltage node N_2 at the amplifier responsible for the biasing of the RSSI, Fig. 3.34. In pratice, this is not exactly true, since the RSSI's transfer function not only has the changes relative to the bias circuit and the FWRs themselves, it also feels the gain changes of the LA.

For these reasons, the Squelch's threshold has to be carefully chosen, in order to accomodate the changes in the RSSI transfer function and ensure no incorrect Squelch detections.

The second, and more delicate situation, is when a high-energy particle collides with the comparator and alters its state causing an incorrect Squelch situation. The solution for this situation is to use redundancy design techniques. The principle behind redundancy techniques is to multiply critical components or blocks of a system increasing its reliability. In this particular situation, the critical component that needs to be replicated is the comparator. The idea is to have two replicas of the comparator that receive the same input signals and which outputs are fed into a 4-input AND gate along with the Enable signal. If the Enable is ON, the only way for the Squelch signal to be active is if all the comparators indicate the state ($V_{STRENGTH} > V_{ref}$). The simplified schematic of this circuit is presented in Fig. 3.43.

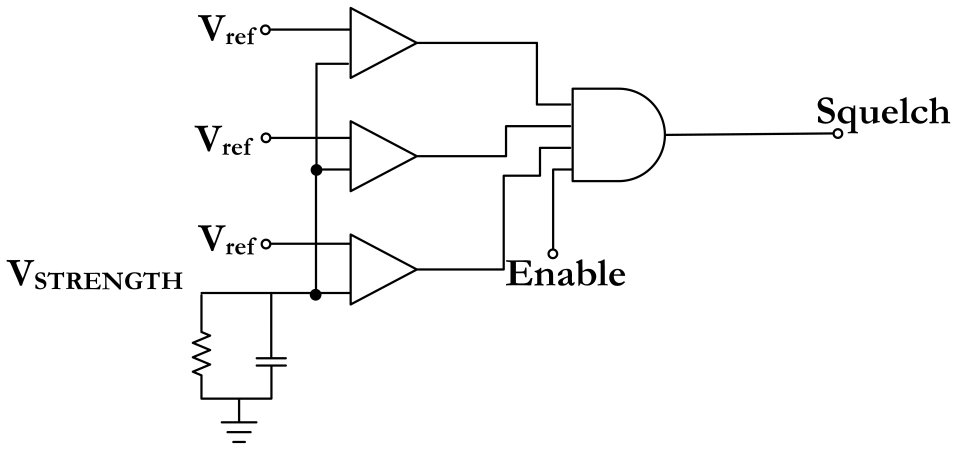


Figure 3.43: Simplified Squelch's architecture using redundancy techniques.

3.3.1 Comparator

The chosen architecture for the Squelch's comparator is depicted in Fig. 3.44. It basically a differential pair of NMOS transistors with diode connected PMOS loads. There is a second gain stage where the transconductance element is a PMOS with a NMOS current source load. Capacitor C_1 is used to reduce the GBW of the comparator, in order to increase the response time to a few μs. The goal is to make the circuit as slow as possible so no data is lost if the system glitches (the input power suddenly drops and rises again).

The DC gain of this assembly is given by expression 3.36.

$$Gain = \frac{g_{m2}}{g_{m4} + g_{ds4} + g_{ds2}} \cdot \frac{g_{m8}}{g_{ds6} + g_{ds8}} \tag{3.36}$$

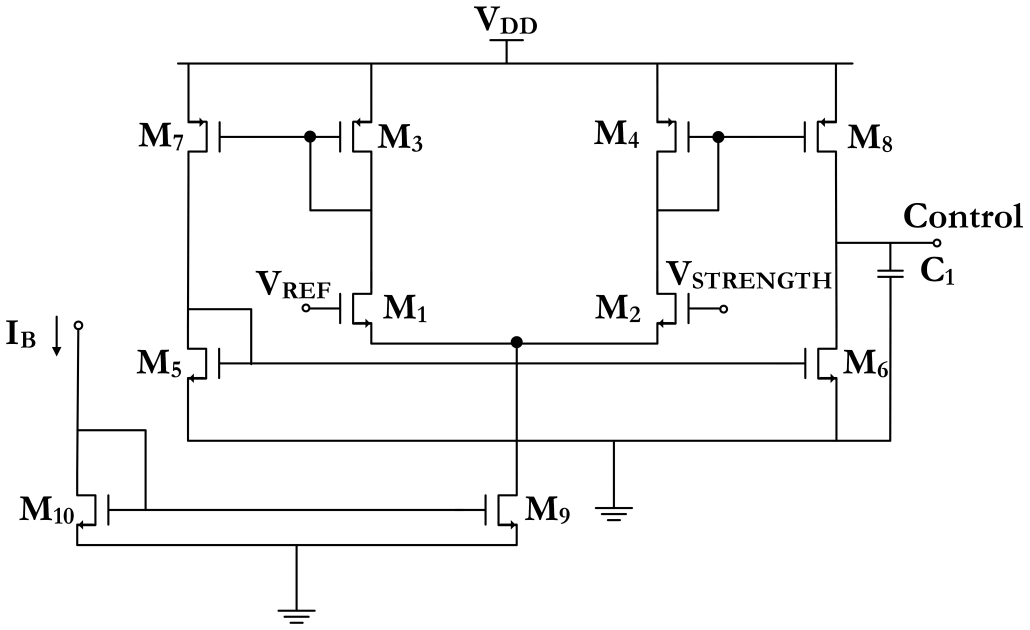


Figure 3.44: Squelch's comparator.

Table 3.16: Components' dimensions of the Squelch's comparator.

Transistor	Size [µm]
$M_{1,2}$	75/5
$M_{3,4}$	1/1
$M_{5,6}$	4/3
$M_{7,8}$	4/1
$M_{9,10}$	1/1
Capacitor	**Size [pF]**
C_1	4.3

The dominant pole, by design, is located at the output node. Its location can be calculated by inspection and is equal to:

$$\omega_p = \frac{g_{ds6} + g_{ds8}}{C_1} \tag{3.37}$$

Table 3.16 presents the components' dimensions for the Squelch's comparator. The circuit was designed to have the lowest possible bandwidth while at the same time minimising the area associated with capacitor C_1 (since the circuit is going to be replicated 3 times and C_1 has to be around a few pF). The goal is to increase the parasitic capacitances of the transistors as much as possible, which results in transistors with larger channel lengths.

3.3.1.1 Simulation Results

The comparator's architecture as well as the components' dimensions have already been presented. Table 3.17 presents some estimated and simulated metrics for the Squelch's comparator. The voltage gain of the comparator is close to 40 dB which is not that high since the comparator's GBW cannot be too high due to the necessity of a large response time. The simulated bandwidth is about 2.8 kHz which is adequate for the application. The power consumption of the buffer is extremely low due to the small bias currents (in order to reduce its bandwidth even further without increasing the area of capacitor C_1 too much). The response time of the comparator to an instantaneous change of the input signal is approximately 10µs. In pratice, the RSSI's output signal, $V_{STRENGTH}$, will not experience instantaneous changes due to the time constant associated with the output filter.

Table 3.17: Estimated and simulated results of the Squelch's comparator.

	DC gain [dB]	Bandwidth [kHz]	GBW [kHz]	Response time [µs]	Power [µW]
Estimated	39.3793	2.80	260.9	-	-
Simulated	39.1989	2.795	109.6	9.93	5.6412

3.3.1.2 Layout

Fig. 3.45 shows the layout of the Squelch's comparator. The total layout area for the Squelch's comparator is 60 377 μm^2 (8.62%) on the IC.

The frequency response of the Squelch's comparator before and after the layout is presented in Fig. 3.46. The DC gain is the same, but the bandwidth suffered a significant reduction (around 60%). This is due to the increase of capacitor C_1 in the layout. The decrease in the bandwidth of the comparator is beneficial to the application since the goal is to make that comparator as slow as possible without significantly increasing its area. Fig. 3.47 shows the time response of the comparator to an almost immediate change in one of its input signals, before and after layout. The layout vs schematic simulation shows an increase in the time response of more of about 60% (the increase in the time response is equal to the bandwidth reduction, since the gain remains constant).

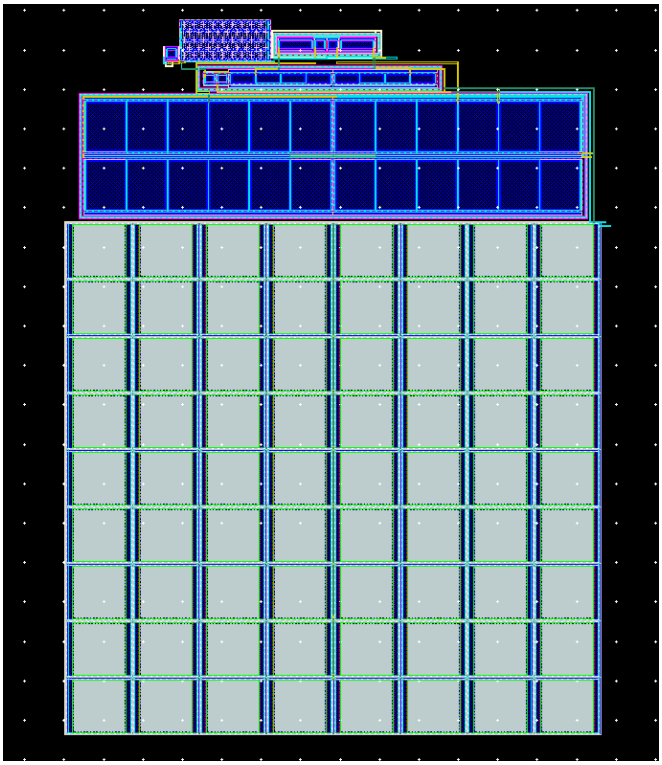


Figure 3.45: Layout of the Squelch's comparator.

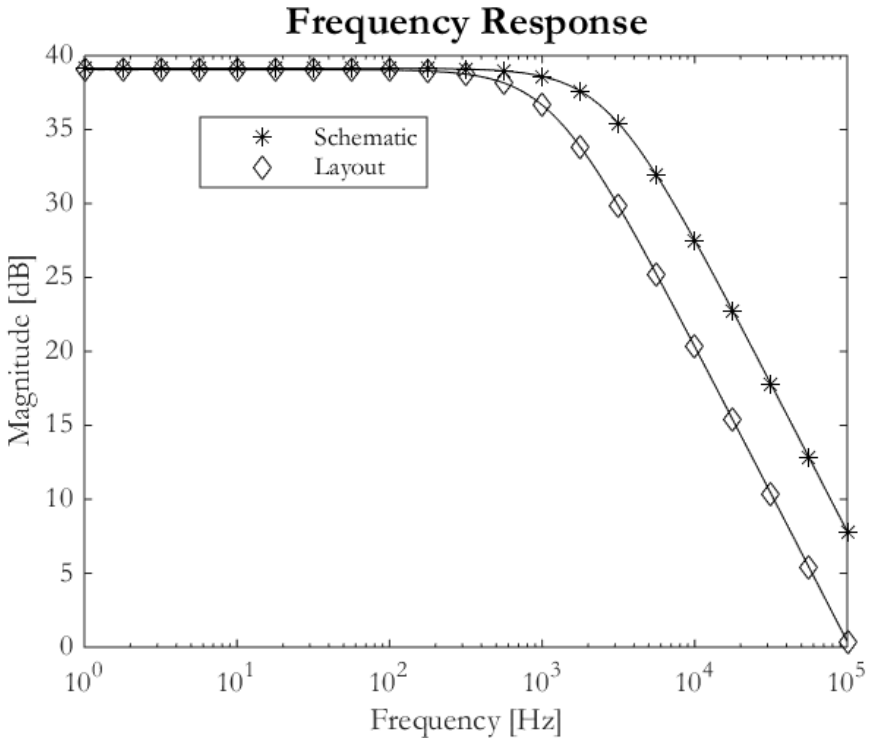


Figure 3.46: Frequency response of the Squelch's comparator - layout vs schematic.

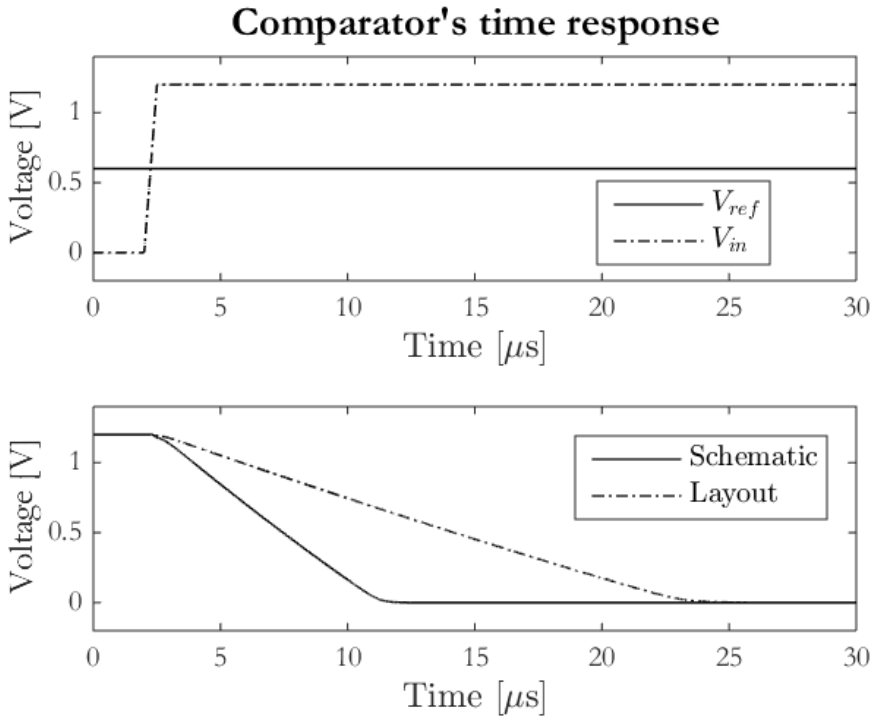


Figure 3.47: Time response of the Squelch's comparator - layout vs schematic.

3.3.2 Squelch's Logic

The output's of the three identical comparators serve as input to a 4-input AND gate, and the fourth input is the external control signal, Enable. If the four signals are logic high (meaning, equal to V_{DD}) the Squelch control signal is activated, and the Output Buffer's current sources are gated. Let us say that the input power is above the Squelch's threshold, which means that it is not desirable to activate the Squelch function, and one high-energy particle reaches one of the comparators and switches is state to 1.2 V. The Squelch is not going to be iniciated since it is necessary for all the comparators to be in agreement. This is the principle behind redundancy and helps to ensure the correct behaviour of this block.

Yet, the opposite situation is not quite solved with this technique. Let us imagine that the circuit is currently "squelched" (all the comparators present the same output) and that a high-energy particle strikes one of the comparators switching it to 0 V. In this case, the Squelch function ceases and the output will be toggling due to noise, since the input signal does not exist or does not have a useful power level. Although this event is undesirable and it cannot be solved using this architecture, the first situation would be much more dangerous in terms of data that could potentially be lost.

Ideally, the Squelch's architecture should work in such a fashion that when is activated, the Output Buffer produces a differential output correspondent to a logic 1 or 0. In order for this to happen, the Output Buffer has to be totally unbalanced. Meaning, one side must have V_{DD} at the transistor's gate, thusly driving all the bias current, while the other

side needs to have 0 V at the transistor's gate, hence, no current will flow through. This way, the differential output of the buffer would be frozen in a logic 1 or 0, depending on the order of the subtraction of the single-ended signals. Forcing the inputs of the Output Buffer to 0/1.2 V necessarily means gating the last stage of the Limiting Amplifier. Such an arrangement is presented in Fig. 3.48.

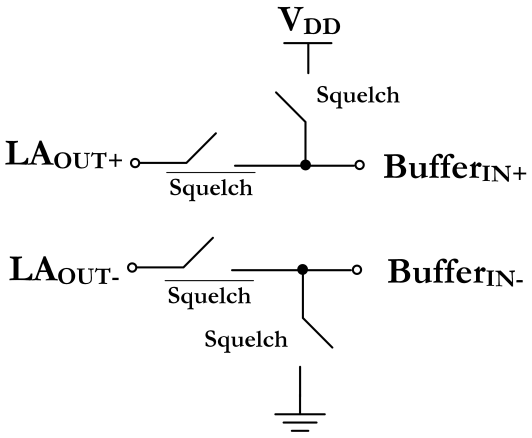


Figure 3.48: Unbalancing of the Output Buffer.

When the Squelch is high the switches on the right side will close and connect the inputs of the Output Buffer to V_{DD} and ground while the LA is isolated from the Ouput Buffer (switches on the left will be open). When the Squelch control signal is low, the switches on the right side will open and the left switches will close, connecting the LA to the Output Buffer and allowing for normal operation. The issue with this technique is that the switches are implemented by MOSFETs which will have linear conduction resistance and parasitic capacitances. Minimising the conduction resistance implies bigger transistors. On the other hand, minimising the parasitic capacitances means smaller transistors. Either way, the switches would add a large RC constant at the output of the LA, significantly degrading the rise and fall times of the output signals (which is not tolerable) when the Squelch is OFF.

This is because the last stage (where the switches are connected) of the LA is already working in large-signal operation and therefore the speed will be limited by the RC constant added by the switches (although the bandwidth reduction is not that significant). This approach was tried and tested out, and the results showed that it could not be used due to the high deterioration of the signal's transition times and the consequent diminished eye opening. For this reason, the Output Buffer is disconnected by forcing its bias current to be zero. This results in the differential output of the buffer to always be equal to 0 V. The problem is that zero does not correspond to a logic value. Furthermore, the output differential signal will have some minor fluctuations around zero, due to the high amplitude signals that are fed to the buffer. This architecture is depicted in Fig. 3.49. The ideal current source, I_T, represented in Fig. 3.49 is actually implemented by a NMOS transistor whose bias voltage depend on the value of the Squelch signal.

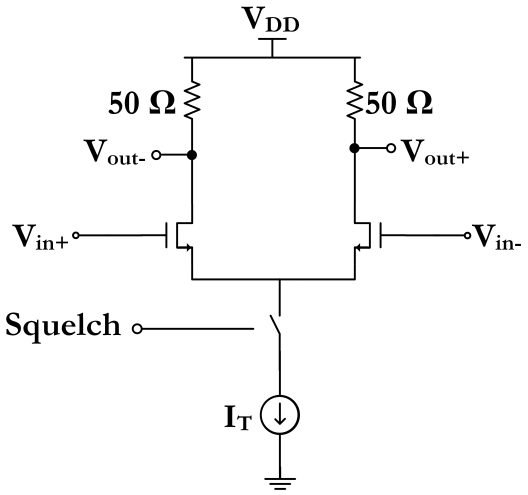


Figure 3.49: Disconnection of the Output Buffer's current source.

In order to better understand the operation performed to disconnect the Output Buffer's bias current let us consider schematic of Fig. 3.50 and that the Squelch signal is represented by C. Meaning, the control signal, C, and its denied version, $\overline{C}$, control two switches that allow for the current source transistor's gate to receive its biasing voltage or to be shorted to ground, depending on the value of the control signal. If the control signal is high (1.2 V) then switch S_1 will close and switch S_2 will open. Then, gate voltage of the current source transistor will be equal to V_{BIAS} (considering ideal switches). When the control signal is 0 V switch S_1 will open and S_2 will close, shorting the gate of the current source's transistor to ground.

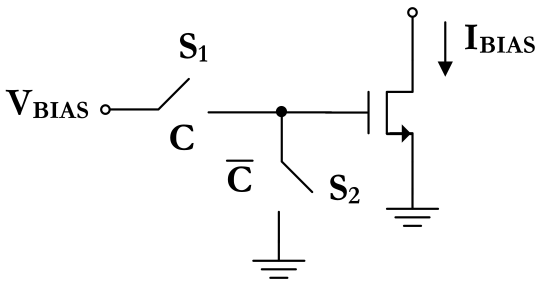


Figure 3.50: Switches for the Output Buffer's bias current's control.

As mentioned before, a non-ideal switch (implemented by a MOSFET) presents a linear conduction resistance, R_{ON}, between its channels (drain and source) when it is ON. This resistance generates a voltage drop between its terminals which would change the value of the bias voltage applied to the gate of the current source transistors. Obvisouly, it is important to minimise this voltage drop, and this is accomplished by minimising the conduction resistance. Without much details, R_{ON}[4], is as small as the V_{GS} voltage increases. This means that we want the V_{GS} voltage of the transistors to be close to

[4]The expression for the linear conduction resistance is $\frac{L}{uC_{ox}W(V_{GS}-V_{TH})}$ [16], Chapter 1.

Table 3.18: Component's dimensions of the switches for the Output Buffer's bias current's control.

Transistor	Size [µm]
M_{P1}	20/0.13
M_{N1}	20/0.13
M_{N2}	20/0.13

V_{DD}. Let us analyse in more detail the case of switch S_1. If an NMOS transistor is used to implement this switch its V_{GS} voltage would range from 600 to 700mV (since V_{BIAS} ranges from 500 to 600mV) which is far from V_{DD}. If a PMOS is chosen, its V_{GS} voltage would be 600mV maximum (value of V_{BIAS}). It is possible to understand that in both cases the V_{GS} voltage is far from the supply voltage, which results in a not so small linear conduction resistance. To minimise this effect, it is possible to connect a NMOS in parallel with a PMOS transistor whose gates are controled by opposite signals, a configuration commonly known as a transmission gate. This way, the effective resistance will be the parallel of the R_{ON} of the NMOS transistor with the R_{ON} of the PMOS transistor, which can be considered to be approximately half - this is not exactly true since the PMOS transistor's carriers (holes) exhibit a lower electronic mobility than the NMOS's carriers (electrons), therefore its R_{ON} is larger. Switch S_2 is easily implemented using an NMOS transistor.

The complete schematic for this configuration is presented in Fig. 3.51, where V_N is the voltage applied to the current source transistor's gate after going through the switches. The dimensions of the components used for the implementation of switches S_1 and S_2 are presented in Table 3.18.

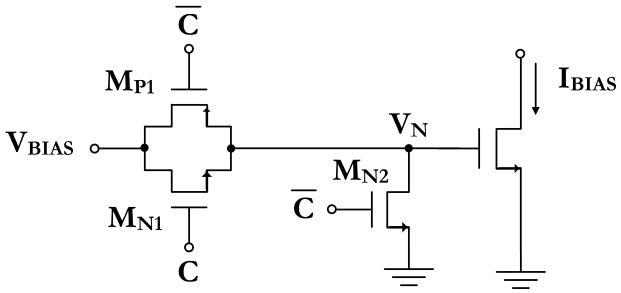


Figure 3.51: Implementation of the switches for the Output Buffer's bias current's control.

3.3.3 Simulation Results

In order to confirm the Squelch's performance, the input signal at the LA is kept at a constant amplitude, greater than the Squelch's threshold. At t =2 µs the input power drops below the Squelch's threshold. The Limiting Amplifier input signal, the RSSI output voltage, $V_{STRENGTH}$, the Squelch's comparators reference voltage, V_{ref}, the Squelch control signal and the Output Buffer's differential output signal are presented in Fig. 3.52.

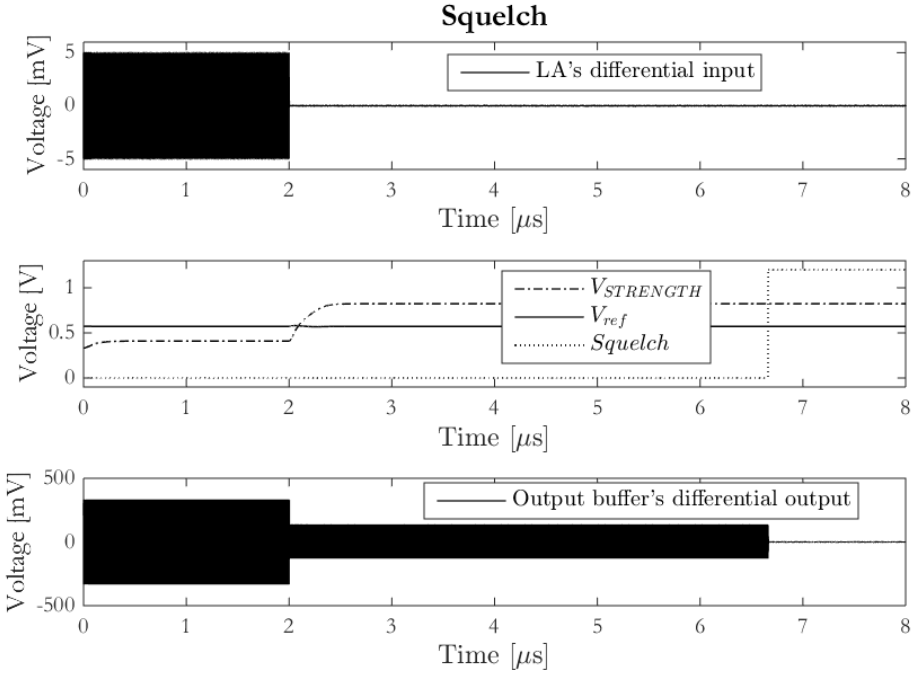


Figure 3.52: Squelch's transient simulations.

One can see that the Squelch takes more than 4.5 µs to react (as desired), in other words, switch its state. The buffer will be amplifying the input signal until the Squelch is activated, from that moment on the output of the buffer is forced to zero by disconnecting its bias current. The power consumption of the overall Squelch circuit, including the three comparators and the additional logic is 16.8 µW.

Due to the variability of the RSSI's transfer function across corners, and even though the reference voltage V_{ref} is supposed to track that variations, the input power to which the Squelch is activated changes. Again, this is due to the changes in the gain of the LA. Let us imagine an horizontal line with the value of V_{ref} (in the typical corner) as represented in Fig. 3.53. Let us also assume that the value of V_{ref} suffers minor changes across corners, since it is originated in the RSSI's PVT independent bias circuit. The interception of that line with the RSSI's transfer functions will be at different values of input power for different corners. This is why the input power to which the Squelch is activated is also much variant across corners. This example was given under the assumption that the reference voltage, V_{ref}, is kept constant across corners which is not true.

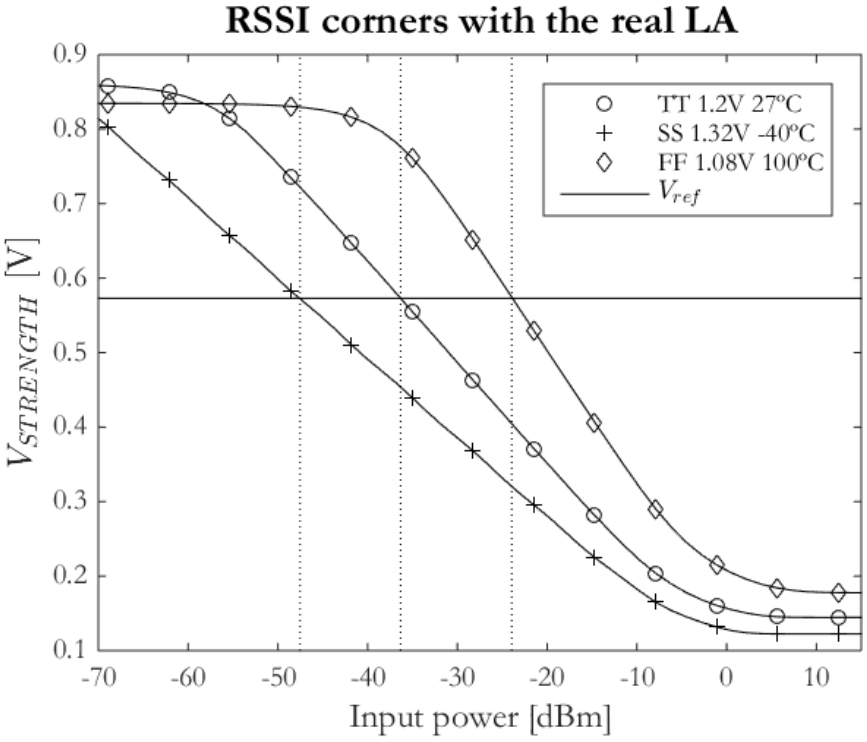


Figure 3.53: Variability of the Squelch's input referred threshold due to the variations of the RSSI's transfer function across corners.

Table 3.19: Variation of the Squelch's threshold across different corners.

Corner	V_{ref} [mV]	Input Voltage Limiting Amplifier [mVpp]	Input Current TIA [µA]
TT 1.2 V 27°C	573	0.99	1.98
FF 1.1 100°C	583	2.62	5.23
SS 1.32 -40°C	575	0.73	1.46
FS 1.2 27°C	559	1.2	2.39
SF 1.2 27°C	585	0.93	1.85

Table 3.19 presents the Squelch's thresholds in terms of input power - at the LA and referred to the TIA (considering a transimpedance gain of 500 Ω) - and the correspondent threshold voltage V_{ref}. Altough the variations of the Squelch's threshold are quite noticeable, the Squelch is never active close to the minimum input current at the TIA - 10 µA - keeping a satisfactory safety margin.

3.4 Output Buffer with Pre-emphasis Capability

The Output Buffer has to drive the external loads at high speed and, at the same time, provide for impedance matching. The typical impedance values for the off-chip loads are normally 50 Ω which results in the necessity to use very large currents in order to produce satisfactory output swings for the CDR. Note: All the figures with NMOS and PMOS with undefined bulk have their bulk connected to ground and V_{DD}, respectively.

The buffer's slew rate is also an issue since it cannot be too low, because it would limit the data rate nor excessively fast, since it can excite resonant circuits, resulting in ISI due to ringing [5] and causing excessive crosstalk. In order to yield relatively high slew rates, a Current-Mode Logic (CML) configuration is normally used. CML is adequate for high-speed drive of off-chip loads producing relatively small output swings (400 mV in this case). For larger output swings the current consumption would be too high. The logic behind CML circuits is to steer the bias current to only one arm of the differential pair, using the differential pair transistors as switches. Such an arrangement is illustrated in Fig. 3.54. If the input differential signal is large enough, the totality of the bias current - I_{SS} - is bypassed through only one side of the differential pair. If we assume that the far-end circuit is perfectly matched, then R_L would be equal to Z_0 and the output swing would be equal to $Z_0 I_{SS}$. CML logic is based on the assumption that the current source transistor remains in saturation region in order to maintain the bias current I_{SS} constant.

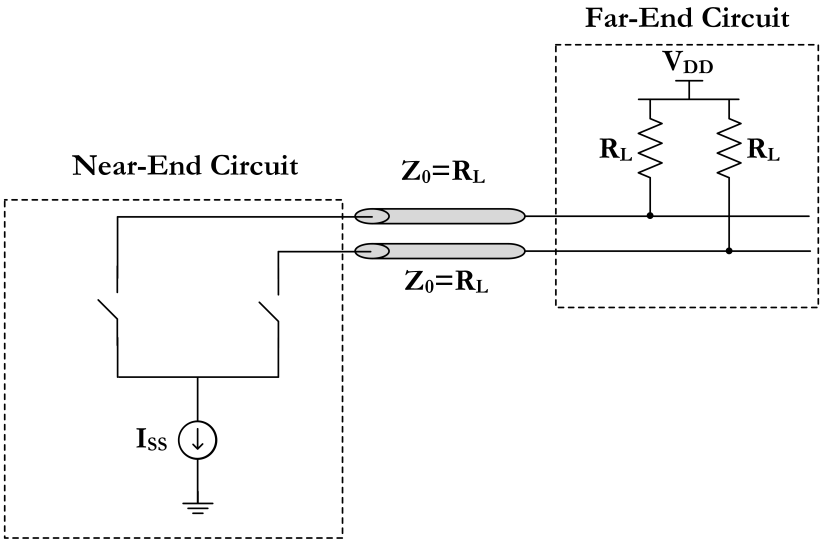


Figure 3.54: CML "open-drain" Output Buffer.

[5] In electrical circuits, ringing is an unwanted oscillation of a voltage or current. It happens when an electrical pulse causes the parasitic capacitances and inductances in the circuit (i.e. those that are not part of the design, but just by-products of the materials used to construct the circuit) to resonate at their characteristic frequency, [34].

The output differential signal must travel a transmission line, which in this case is a Printed-Circuit Board (PCB) line, before it reaches the CDR, Fig. 3.55. Impedance matching is of the utmost importance at the Output Buffer, since it minimises the reflections (which would introduce ISI in random data) in the transmission line, improving the signal's integrity thus minimising the ISI and improving the BER.

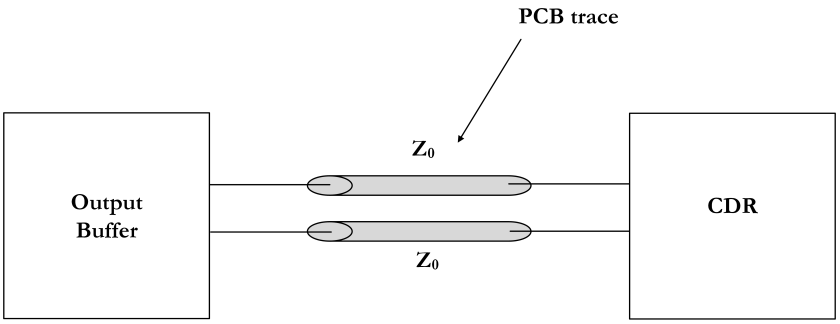


Figure 3.55: PCB transmission line connecting the Output Buffer and the CDR.

In order to have a better understanding of the importance of impedance matching at the Output Buffer, let us analyse in more detail the concept of a transmission line and characteristic impedance.

3.4.1 Transmission Lines

A transmission line (T line) is a physical connection whose length is a significant fraction of the wavelength of interest, meaning, the end-to-end delay is not negligible when compared with the signal transition times. In a PCB line we have to start considering the propagation effects when propagation time is bigger than 10% of the period (or when the circuit length is bigger that 10% of the wavelength) for a sinusoidal wave and when the propagation time is bigger than the square wave transition time for digital signals [35]. When considering the signal propagation effects, the concept of a transmission line arises and matching networks are required in order to overcome these effects.

Every transmission line, irrespective of the type, presents a characteristic impedance which is function of its inductance and capacitance. Let us consider a simple coaxial cable as illustrated in Fig. 3.56.

In this geometry, there is a direction where the geometry does not change. Let us consider that direction for the zz' axis. For relatively slow phenomena, the electric and magnetic field are kept at a perpendicular plane in relation with the zz' axis (electric and magnetic transversal fields – TEM mode). For sufficiently high frequencies the wavelength is so large that it is comparable to the distance between the two conductors.

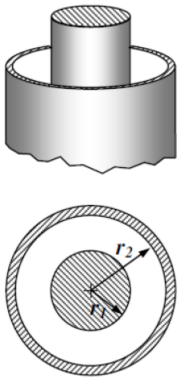


Figure 3.56: Coaxial Cable. Adapted from [36].

In this situation, one of the conductors can find its complementary current, not at the other conductor but in a further area of itself. Thusly the field can close not between two conductors, but between to areas of the same conductor distanced of $\lambda/2$ from each other. In this situation, either only the magnetic field (TM mode) or the electric field (TE mode) can be laid in the perpendicular plane.

By using the differential equations of the line (considering the TE mode), as demonstrated in [36], it is possible to arrive to the following expressions that describe the voltage and current space and temporal evolution:

$$\frac{di}{dz} = -G \cdot u - C \cdot \frac{du}{dt}, \frac{du}{dz} = -R \cdot i - L \cdot \frac{di}{dt} \tag{3.38}$$

Where G ($\Omega^{-1} \cdot m^{-1}$) is the transversal conductance between conductors, by unit of length; C ($F \cdot m^{-1}$) is the capacitance between conductors, by unit of length; R ($\Omega \cdot m^{-1}$) is the total longitudinal resistance of both conductors, by unit of length; L ($H \cdot m^{-1}$) is the total self-inductance coefficient of the line, by unit of length. Solving the system of differential equations, as demonstrated in [36], we arrive to an expression that relates the voltage and current at any point of the line:

$$\frac{u}{i} = Z_0 = \pm\sqrt{\frac{L}{C}} \tag{3.39}$$

This relation states that at any point of the line, the relation between the voltage and the current is constant and given by Z_0, which is known by the characteristic impedance of the line as it is a function of its inductance and capacitance. The value of the characteristic impedance is defined by the electronic mobility and the dielectric constant of the constituent material plus a geometric factor. This value is typically designed to be equal to 50 Ω because it is a compromise between the value of impedance that allows for minimum losses (77 Ω), and the impedance value that maximizes the power that the cable can handle with breaking the dielectric (30 Ω) [35].

3.4.2 Impedance Matching

We have seen that every transmission line presents a characteristic impedance, which remains the same at any given point of the line. Let us consider that we have a wave propagating from the source (generator) to the load. At each point of the line that same wave will "see" the characteristic impedance of the line, and the relation between the voltage and the current will be defined by that. Now, let us suppose that the line is terminated in a short circuit, meaning that the load impedance R_L is equal to zero. At the load there will be a border condition that forces the voltage to be zero at that place. This means that something has to happen in order to satisfy that condition, since the incident wave presents a value different from zero. A reflected/outgoing wave appears at the load, symmetric to the incident/incoming wave that cancels it at the short circuit in order to obey the border condition, Fig. 3.57. The problem with this is that the load is "sending" power back to the generator, so, the power available from the source is not delivered to the load. Now, let us imagine that the impedance of the load equals the characteristic impedance of the line. The incident wave, at each point of the line, will "see" the characteristic impedance of the line, when the wave reaches the load it will "see" the exact same thing, so, the border condition is automatically obeyed, Fig. 3.58. There will be no reflections at the load, and the power transference is maximised. The waveform at the load will be composed by the incident wave V_1 only, with some delay. This is the concept behind impedance matching. When the load impedance equals the characteristic impedance of the line we say that the load is matched to the line. Summing up, at each point of the line (except in the matched case) there will be two waves, the incident wave and the reflected wave.

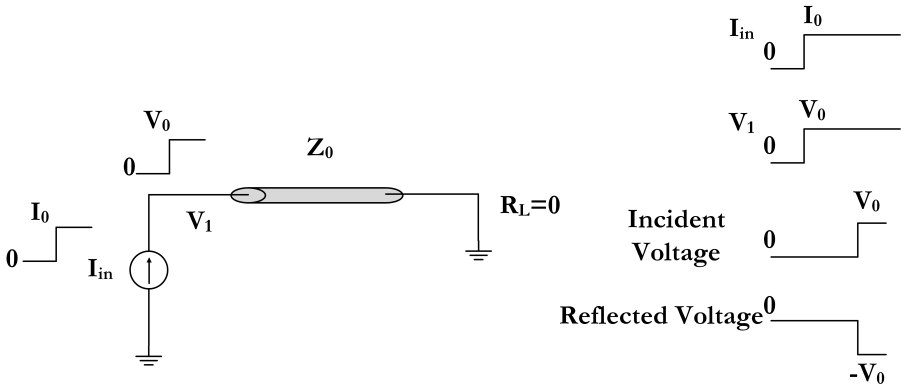


Figure 3.57: T line with short load.

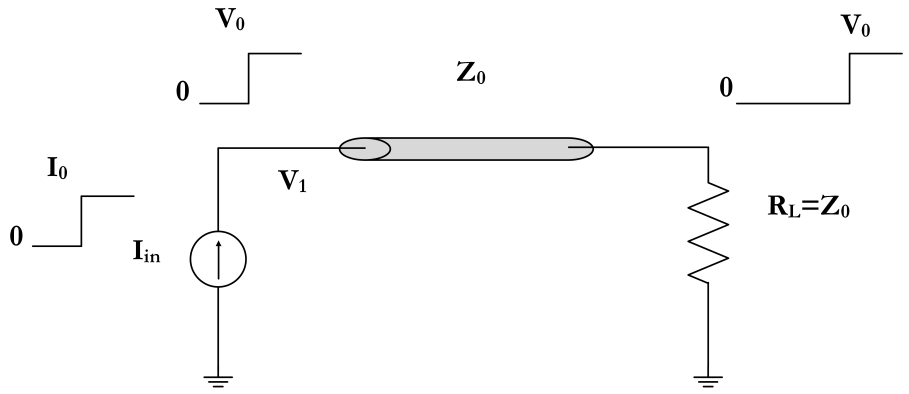


Figure 3.58: Matched T line.

3.4.3 Differential Signaling

As well as in the case of the Limiting Amplifier, differential operation offers many advantages when compared to single-ended operation for the transmission and reception of the Optical Receiver's output signal even though it requires an extra pad and package pin.

Two of the major advantages of differential signaling are related to the immunity to the supply noise and the packaging parasitic requirements. Let us analyse in more detail the benefits of differential signalling in the cases mentioned before.

3.4.3.1 Package Parasitics

In order to understand the harmful effects of the package parasitics and the advantage provided by the differential operation, let us consider the arrangement depicted in Fig. 3.59. Where two transmission lines carry the differential signals to a packaged circuit. The bond wire inductances are represented by L_1 and L_2 and the mutual inductance between the two inductors is given by M. The various capacitances are lumped into C_{in}. By inspection, the voltage drops in each inductor are given by:

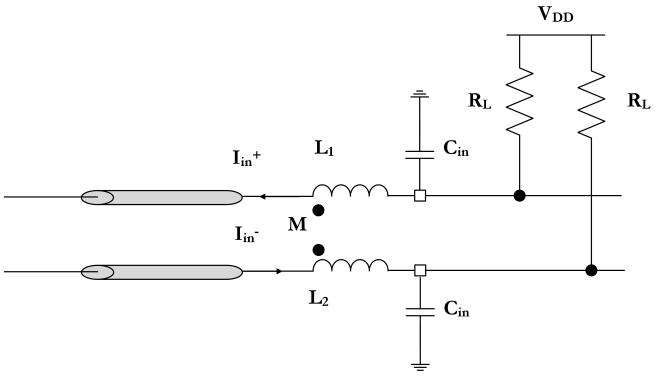


Figure 3.59: Effects of package parasitics. Adapted from [7], Chapter 5.

$$V_{L1} = I_{in}^{+} L_1 s - I_{in}^{-} M s \tag{3.40}$$

$$V_{L2} = -I_{in}^{-} L_2 s + I_{in}^{+} M s \tag{3.41}$$

Considering $L_1 = L_2 = L_P$ and $I_{in}^{=} I_{in}-$, Eq. 3.40 and Eq. 3.41 as simplified:

$$V_{L1} = I_{in}^{+}(L_P - M)s \tag{3.42}$$

$$V_{L2} = I_{in}^{-}(-L_P + M)s \tag{3.43}$$

Looking into Eqs. 3.42 and 3.43 it is possible to see that the mutual inductance between the bond wire inductors reduces the effective inductance in each signal line, therefore reducing the voltage drops across the package parasitics. Typically, if the chip pad frame and the package are carefully designed, then M is around $0.5L_P$ to $0.75L_P$, reducing the voltage drops up to 75% [7], Chapter 5. Obviously, this property cannot be exploited in single-ended configurations.

3.4.3.2 Supply Noise

Another beneficial characteristic in differential signalling is related to the transient currents drawn from the supply voltage. Let us consider the circuit represented in Fig. 3.54. As mentioned before, in a CML configuration, the current through the termination resistors is equal to the bias current, I_{SS}, at any point in time. If the V_{DD} node suffers from finite output impedance due to bond-wire and package inductance, the bias current would experience nearly zero transient changes [7], Chapter 5. Obviously, even in a differential configuration there will always be some transient current in the supply. This is due to the fact that the common-source node has a finite capacitance, which means that, during switching, the transitors will draw a current equal to I_{SS}, plus the current necessary to charge that capacitor. This would introduce some undesirable transient current in the supply node, which could be supressed by using on-chip bypass capacitors between V_{DD} and ground.

3.4.4 Double-termination Output Buffer

The main issue with the architecture presented in Fig. 3.54 - the "open-drain" buffer - is that the buffer exhibits high output impedance, which would be fine if the far-end circuit were well matched. That does not always happen, because the package parasitics and the input capacitance at the far-end introduce impedance mismatches. These mismatches would have created reflected waves at the far-end circuit. These reflected waves would travel back to the near-end circuit and be reflected again, if the Output Buffer were not matched. These doubly reflected waves would reach the far-end circuit with some delay in relation with the original signal. As a consequence, the output differential signal would experience substancial ISI. The solution to this problem is to have the buffer's

output impedance matched to the characteristic impedance of the transmission line. This architecture is outlined in Fig. 3.60.

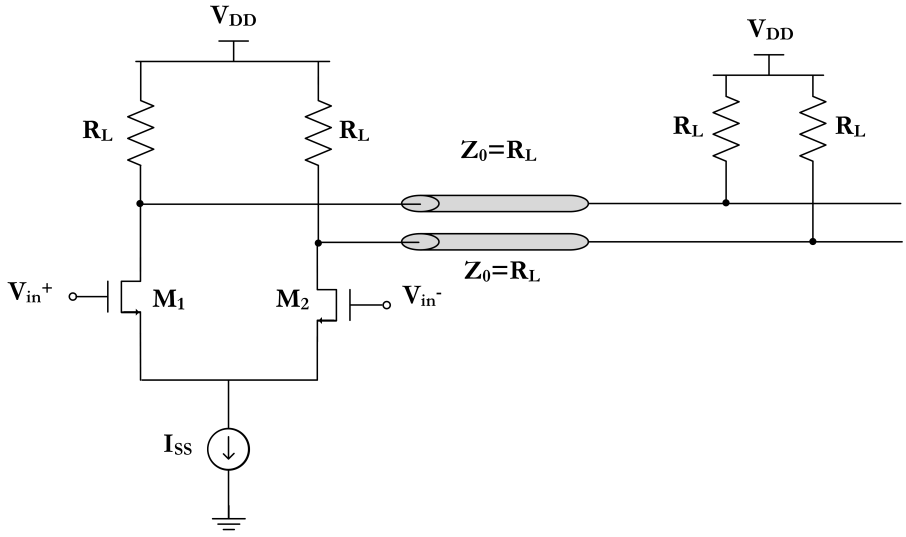


Figure 3.60: Double-termination Output Buffer.

The only issue with the proposed architecture is that for a given output swing, the current has to be doubled. Half of the current will flow through the termination resistors and the other half will flow through the differential pair loads. So, in this case, where a 400 mV_{pp} differential output swing is necessary, the load current I_{SS} has to be equal to 8 mA, whereas in the open-drain configuration 4 mA would be enough. In order to minimise the ISI (which would strongly degrade the BER) the chosen configuration was the double-termination Output Buffer.

3.4.5 Pre-emphasis Capability

In reality, transmission lines are not ideal, which means that experience losses and exhibit a low-pass behaviour, so it is desirable that the buffer has Pre-emphasis capability improving the eye opening at the far-end. Pre-emphasis is no more than equalisation, in other words, adjusting the balance between frequency components within an electric signal. In this case, the goal is to emphasize the high frequency components more than the low frequency ones so as to improve the signal's integrity at the end of the transmission line.

The proposed idea is to have a second, auxiliary, differential pair cross-connected to the main one. The input of the second differential pair would be delayed versions of the main buffer's input signals. The simplified schematic is represented in Fig. 3.61. Capacitors C_1 and C_2 are used for AC coupling.

The LA's output signals would flow through the main buffer and would be fed to a circuit that would produce a delay in relation to the original signal. The delayed signals would be fed to the secondary buffer which would also work in a CML configuration. Therefore, the currents produced by both buffers would have a delay, Δ_T, in relation

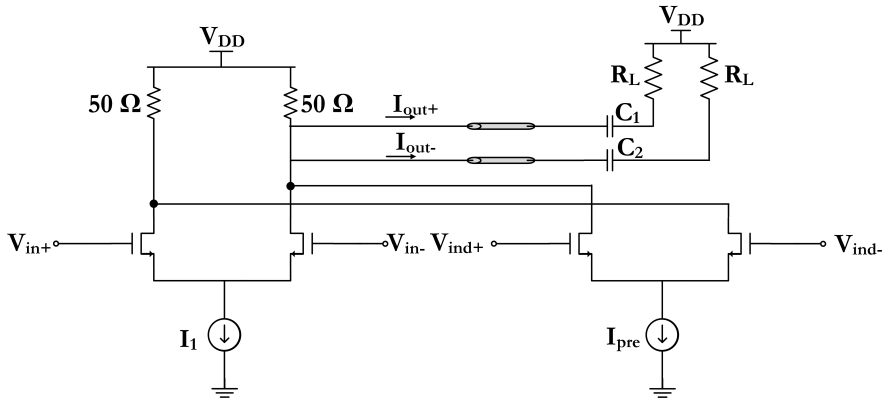


Figure 3.61: Simplified schematic of the Output Buffer with Pre-emphasis capability.

to each other. Since both buffers are crossed-connected (the positive output of the main buffer is shorted to the negative output of the secondary buffer, and vice-versa) the output differential current would be the sum of the main current I_1, and a phase-opposing delayed current I_{pre}. This idea is outlined in Fig. 3.62.

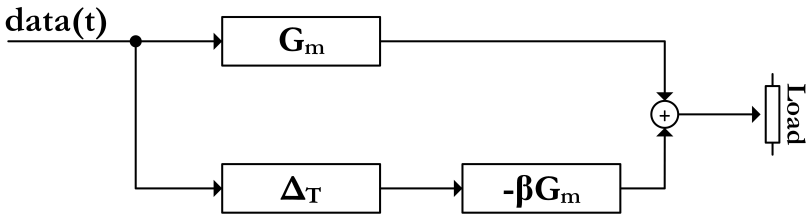


Figure 3.62: High level Pre-emphasis scheme.

Where data(t) is the incoming data originating from the LA, G_m is the effective transconductance of the buffers, Δ_T is the delay from the original signal and β is the ratio between the value of the Pre-emphasis current, I_{pre} and the main current I_1. Let us now analyse in more detail the waveforms of the currents involved in the Pre-emphasis process and the resulting output differential current. The correspondent waveforms are represented in Fig. 3.63.

Let us consider that $I_{out}(t)$ is the differential current flowing through the termination resistors. Then, $I_1(t)$ is the differential current that represents the contribution of the main buffer to the total current $I_{out}(t)$. In the same manner, $I_{pre}(t)$ is the differential current originating from the secondary buffer. Both $I_1(t)$ and $I_{pre}(t)$ are represented assuming negative values in time, since the termination is AC coupled. In the main buffer, the

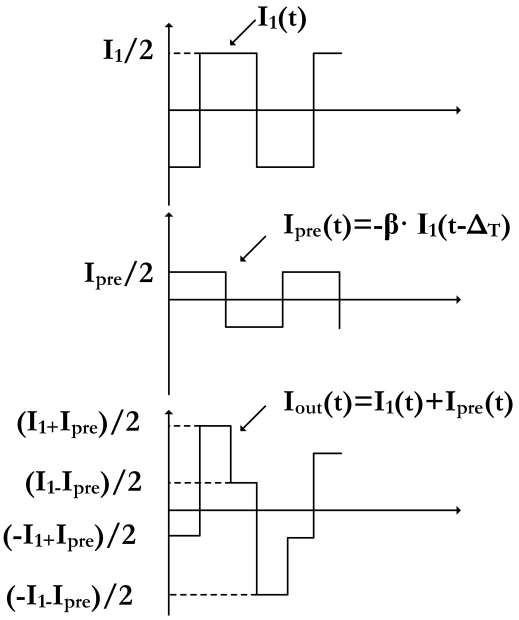


Figure 3.63: Waveforms of the currents involved in the Pre-emphasis function.

bias current I_1 will always be shifting from one arm of the differential pair to the other. Half of that current will flow through the correspondent termination resistor with its DC component removed. The effective current that will flow through the correspondent termination resistor will vary between $I_1/4$ and $-I_1/4$. Then, the differential current would range from $I_1/2$ and $-I_1/2$ as represented in Fig. 3.63. The same logic is valid for the secondary buffer, although the output differential current produced by it is phase-opposing and delayed in relation to current $I_1(t)$. Also, it is expected that its maximum and minimum values are smaller than the ones of $I_1(t)$. The output differential current would be the superimposition of the two currents. There will be periods when $I_1(t) = \pm I_1/2$ and $I_{pre}(t) = \pm I_{pre}/2$ producing a Pre-emphasis level of $\pm(I_1 + I_{pre})/2$. The static levels are given by $(I_1 - I_{pre})/2$ or $(-I_1 + I_{pre})/2$. The resulting current $I_{out}(t)$ would produce a differential swing of $V_{swing} = (I_1 - I_{pre})R_L$. This shows that the larger the desired Pre-emphasis level, the larger the buffer bias current needs to be, in order to keep a constant output swing.

3.4.5.1 Adjustable Delay

The overall Optical Receiver is designed to work at a maximum data rate of 5Gb/s, although operation at 2.5Gb/s is also possible. Hence, the operation of the Pre-emphasis circuit has to be adjusted according to the data rate. The delay, Δ_T, has to be different for a signal with a minimum pulse duration of 200 ps or 400 ps. Typically, the Pre-emphasis current must be active for half of the pulse time, meaning, 100 ps for 5Gb/s, and 200 ps for 2.5Gb/s. This means different delays are needed for different data rates, and therefore, a circuit that can produce different delays according to a control signal (which is

controlled externally). The control signal is Pre_{5G} and assumes two possible values: V_{DD} or 0 V. When the signal equals V_{DD}, it indicates that the Optical Receiver is working at 5Gb/s and a smaller delay is required. When the signal is 0V the Optical Receiver is working at 2.5Gb/s and the produced delay would have to be larger.

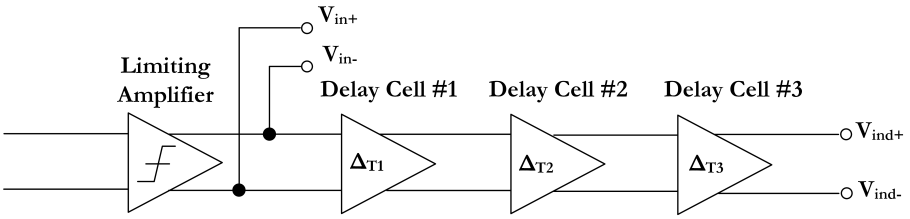


Figure 3.64: Chain of delays for the Pre-emphasis circuit.

The proposed architecture for the adjustable delay circuit is presented in Fig. 3.64. It composed by a series of three differential amplifiers. The first two delay cells receive the control signal Pre_{5G} and adjust the delay accordingly. The third delay cell is identical and has a larger current than the first ones in order to drive the secondary Output Buffer and recover the rise and fall times of the signals that were slowed down by the first and second delay cells.

The architecture for the first and second delay cell is depicted in Fig. 3.65. It is basically a resistively loaded differential pair. The bias current and the load value are adjusted to create a different delay according to the value of the control signal. In this case, there is no need to have a large bias current since the goal is to slow down the signal, and not having an excessively large slew rate is actually good. The simplest way to control the signal delay is to change the bandwidth of the differential pair which is a direct function of the load capacitance C_L and the load resistor R_L. If decreased the value of the load resistor, the bandwidth would increase by the same factor and delay of the output signal would be smaller. In the same way, if we were to increase the value of the resistor, the bandwidth would therefore decrease, and the produced delay would be larger. The problem is that we need one delay to be the double of the other one, which implicates decreasing or increasing the resistor by a factor of two. This would abruptaly change the common mode voltage of these amplifiers, which is not desirable. Therefore, and since the common mode voltage is given by $V_{DD} - R_L I_T$, the solution is changing the bias current in order to keep the common mode voltage constant.

When $Pre_{5G} = V_{DD}$, switch S_5 and S_6 close and the effective load resistor is $R_L/2$. Switch S_1 also closes and the bias current is equal $2I_T$ (switch S_2 is open). Thus, the common mode voltage is given by $V_{DD} - R_L I_T$. When $Pre_{5G} = 0$V all the switches, $S_{1,5,6}$ (switch S_2 closes) open and the effective load resistor is just R_L, and the bias current is

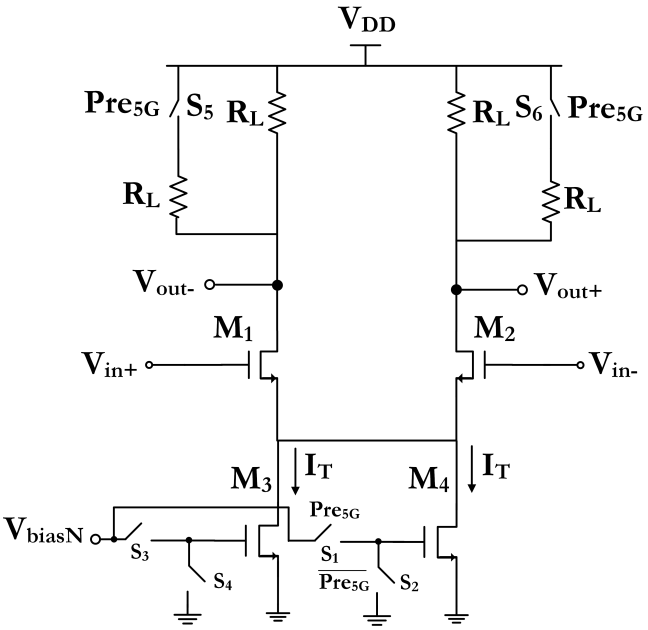


Figure 3.65: Schematic of first and second delay cell.

equal to I_T keeping the common mode voltage equal in both situations. Switches S_3 and S_4 control the current in transistor M_3. This current should always flow through this transistor except if the Pre-emphasis is OFF or if the Squelch is ON. Therefore, the control signals for switches S_3 and S_4 will be presented in Section 3.4.5.2.
As represented in Fig. 3.64, this circuit is responsible for producing the first delay Δ_{T1}. As mentioned before, there is no need in having a very large bias current in this differential pair, since we do not want a large slew rate. For this delay cell, the tail current I_T is 240 µA. Switch $S_{1,3}$ were implemented using a transmission gate and $S_{2,4}$ with a NMOS transistor, as explained in Section 3.3.2 (its dimensions are the same as the ones presented in Table 3.18).

Switches $S_{5,6}$ were implemented with PMOS transistors which control voltages are the denied version of the control signal, $\overline{Pre_{5G}}$ as in Fig. 3.66. The dimensions of the components are presented in Table 3.20.

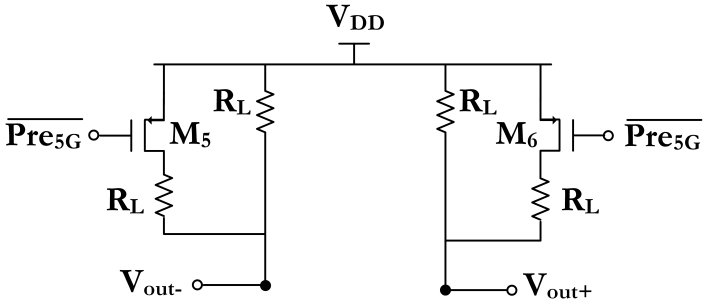


Figure 3.66: PMOS switches for the first delay cell.

Table 3.20: Components' dimensions of the first and second delay cell.

Transistor	Size [µm]
$M_{1,2}$	25/0.06
$M_{3,4}$	24/0.5
$M_{5,6}$	8/0.06
Resistor	Size [kΩ]
R_L	2

The third delay cell is a simple differential pair with a larger bias current, Fig. 3.67. The bias current has to be large enough that the differential pair is "strong" enough to drive the secondary differential pair in the Output Buffer (which receives the delayed version of the LA signals). In the case of the Limiting Amplifier, the last stage had to have a bias current larger than 6 mA in order to drive the main buffer. In this case, there is no need to have a bias current that big, since the Pre-emphasis currents are always smaller than the main ones, so, the transistors are also smaller. The tail current, I_T, for this differential pair is approximately 1.6 mA. As in the first and second delay cells the current flowing through the current source transistor, M_3, is subject to the value of the Squelch signal and if the Pre-emphasis is active. Switches S_1 and S_2 are implemented in the same way as the switches $S_{1,2}$ and $S_{3,4}$ of the first delay cell. The component dimensions are presented in Table 3.21. The W/L relation of the differential pair's transistors is smaller than in the first and second delay cells (although the bias current is larger) since it is desirable to have smaller parasitic capacitances in order to recover the rise and fall times of the signals.

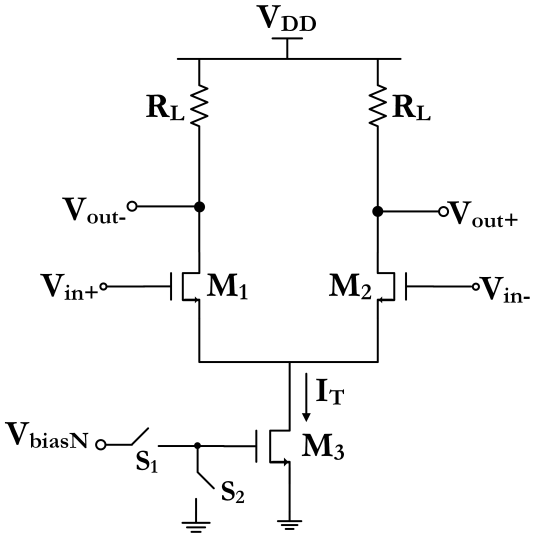


Figure 3.67: Schematic of the third delay cell.

Table 3.21: Components' dimensions of the third delay cell.

Transistor	Size [µm]
$M_{1,2}$	24/0.06
M_3	24/0.5
Resistor	Size [kΩ]
R_L	300

Table 3.22: Delays produced by the adjustable delay circuit as a function of the control signal Pre_{5G}.

Pre_{5G} [V]	Δ_T [ps]
1.2	105
0	190

Table 3.22 presents the overall delay, Δ_T, produced by the adjustable delay circuit (in the typical corner), according to the value of the external control signal, Pre_{5G}. For 2.5 Gb/s operation the produced delay is 190 ps and for 5 Gb/s is 105 ps. Although the produced delays are not exactly half of each other, this architecture can provide them without large power dissipation.

One should note that there is no point in having the delay cells working when the Squelch function is activated. Furthermore, it is possible that the Pre-emphasis capability is OFF (this is going to be discussed in more detail in Section 3.4.5.2). For these reasons, the control signal Pre_{5G} is only ON when the Squelch signal is OFF and if the Pre-emphasis is active. Meaning, Pre_{5G} is not just the external control signal that defines if the circuit is operating at 2.5 or 5 Gb/s, it has an extra logic that includes the Squelch signal and two other external control signals. This matter shall be discussed in more detail in the following Section.

3.4.5.2 Tunable Pre-emphasis

It is also useful to control the ammount of Pre-emphasis generated by the Output Buffer. Since the characteristic of the transmission line may change, the Pre-emphasis can be controlled in order to maximise the integrity of the signal or mininise the power consumption under different working environments. Ideally, to do this, it is only necessary to change the value of the Pre-emphasis current I_{pre}, keeping the main buffer current I_1 constant. In pratice, and since the output swing must be kept constant, the main buffer current has to track the increase/decrease in the Pre-emphasis current. The differential voltage swing (in the static levels) is given by $(I_1 - I_{pre})R_L$ which means that, if I_{pre} changes then I_1 has to change by the same ammount in order to keep the output swing constant and equal to 400 mV, in this case (since the value of R_L cannot change for impedance matching purposes). Since the Pre-emphasis levels are given by $\pm\frac{I_1+I_{pre}}{2}R_L$ increasing the Pre-emphasis current increases the voltage levels achieved by the Pre-emphasis. If the

main buffer's current were to be increased by the same factor, the differential output swing would remain unchanged in the static levels, and the Pre-emphasis levels would increase.

The control of the main buffer currents and the Pre-emphasis current is done by two external control bits, bit_0 and bit_1 whose outputs are equal to 1.2 or 0 V. This means that there are 4 different combinations for the two bits, and thus 4 different Pre-emphasis levels. Noting that the differential output swing has to be equal to 400 mV, which implies that $I_1 - I_{pre} = 8\text{mA}$ and that the common mode voltage of the buffer cannot be too low (since it has to be enough to keep the different pair transistors and the current source transistor in saturation). The values of both currents, $I_{1_{TOTAL}}$ and $I_{pre_{TOTAL}}$, and the theoretical Pre-emphasis levels[6] are presented in Table 3.23 according to the control bits.

Table 3.23: Main buffer and Pre-emphasis' currents according to the control bits.

Bit_1	Bit_0	$I_{1_{TOTAL}}$[mA]	$I_{pre_{TOTAL}}$[mA]	Pre-emphasis level [%]
0	0	8	0	0
0	1	9.5	1.5	37.5
1	0	11	3	75
1	1	14	6	150

All four combinations allow for 0%, 37.5%, 75% and 150% Pre-emphasis levels.

For these reasons, the Output Buffer circuit architecture has to change, in order to allow for the bias currents to change according to two control bits. Therefore, the current sources for the Output Buffer (main buffer and the secondary one) are not implemented by one transistor only, but by several transistors placed in parallel whose gates are biased (or not) according to the value of the different control signals. The simplified schematic for this circuit is represented in Fig. 3.68.

The different current sources $I_{1,2,3,4}$ and $I_{pre1,2,3}$ are controlled by five control signals: $C_{1,3,4,5,6}$. The logic values of the five control signals, plus an auxiliary control signal C_2, are presented in Table 3.24, according to the different combinations for the control bits. All control signals are only active if the Squelch is OFF. As a result of the logic value of the control bits, the control signals will assume different logic values for different combinations (the logic values 0 and 1 correspond to voltages of 0 and 1.2 V). Therefore, and as represented in Fig. 3.68, the various current sources will be activated or deactivaded generating a total current for each one of the buffers equal to the sum of the currents, whose control signals are logic high. For example, for $Bit_1 = 0$ and $Bit_0 = 1$, C_3 and C_5 are logic high, which means that the swiches corresponding to current I_2 and I_{pre1} will be closed. Then, the main buffer's total current would be given by the sum of I_1 and I_2, and the Pre-emphasis buffer current would be equal to I_{pre1}. Assigning $I_1 = 8\text{mA}$, $I_2 = 1.5\text{mA}$, $I_3 = 1.5\text{mA}$, $I_4 = 3\text{mA}$, $I_{pre1} = 1.5\text{mA}$, $I_{pre2} = 3\text{mA}$ and $I_{pre3} = 6\text{mA}$ the conditions previously announced in Table 3.23 are satisfied. In order to generate the control signals

[6]The Pre-emphasis level is typically calculated as $\frac{V_{pp}}{V_{static}} - 1$.

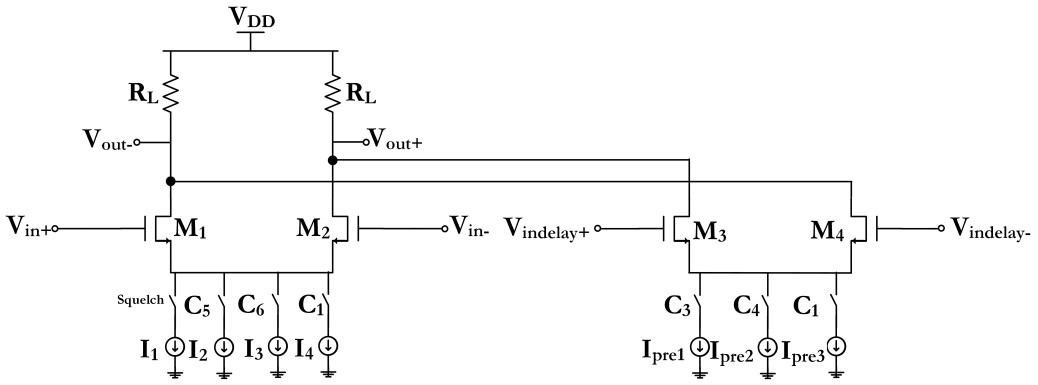


Figure 3.68: Output buffer with tunable Pre-emphasis capability.

responsible for controlling the current sources, the control bits are sent into a series of logic gates. The simplified schematic of the control logic for the Output Buffer's currents is depicted in Fig. 3.69.

Table 3.24: Truth table of the control signals and correspondent currents as a fuction of the control bits for Squelch=0 V.

Bit_1	Bit_0	C_1	C_2	C_3	C_4	C_5	C_6	$I_{1_{TOTAL}}$	$I_{pre_{TOTAL}}$
0	0	0	0	0	0	0	0	I_1	0
0	1	0	1	1	0	1	0	I_1+I_2	I_{pre1}
1	0	0	1	0	1	1	1	I_1+I_2+I_3	I_{pre2}
1	1	1	0	0	0	1	1	I_1+I_2+I_3+I_4	I_{pre3}

The ideal current sources represented in Fig. 3.68 are actually implemented by NMOS transistors whose bias voltages depend on the value of the correspondent control signal. The current souces' transistors are biased, or have their gates grounded, by the same mechanism presented in Section 3.3.2.

The complete architecture for the Output Buffer is finally presented in Fig. 3.70. One should note that the gates of the current source transistor are floating for design simplicity purposes.

Table 3.25 presents the components' dimensions of the Output Buffer correspondent to the circuit of Fig. 3.70. Again, bandwidth being a concern, all the transistors of the differential pair employ minimum channel length (except for the current source ones).

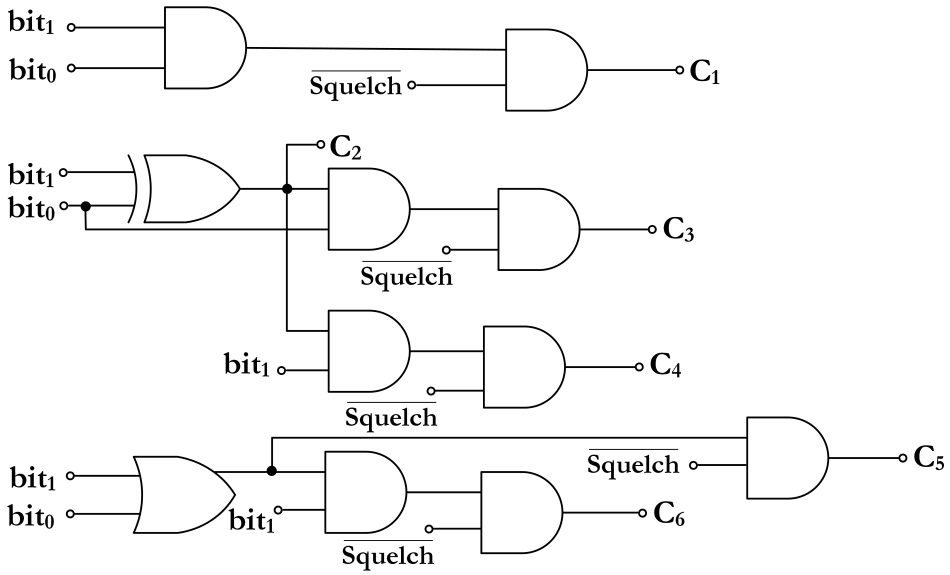


Figure 3.69: Control logic used to generate the control signals for the main buffer and Pre-emphasis' current sources.

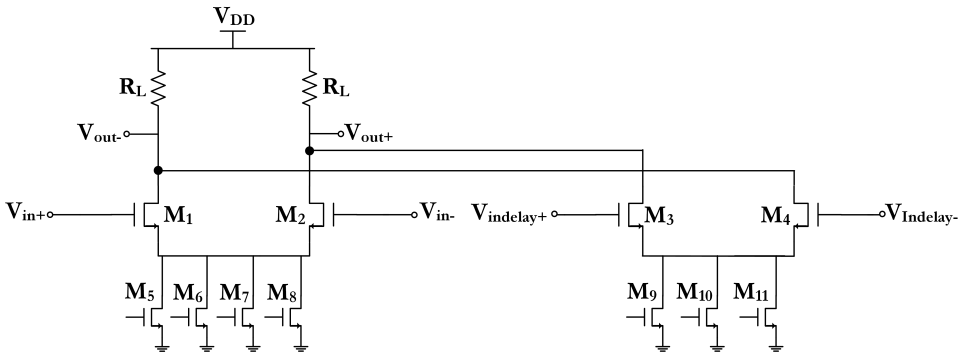


Figure 3.70: Complete schematic of the Output Buffer with tunable Pre-emphasis capability.

Now that the control bits for the Pre-emphasis amplitude and the resultant control signals for the main and secondary buffer current sources have been presented, let us finally understand how the signal Pre_{5G} is generated. Analysing Table 3.24 one can see that C_5 is the result of the OR operation between Bit_1 and Bit_0, followed by a AND operation with the denied version of the Squelch signal, meaning it will be logic high when one of the bits is 1 and Squelch is OFF, simultaneously. In practice, C_5 informs if the Pre-emphasis capability is active or not, independently of its magnitude. Pre_{5G} is the

Table 3.25: Components' dimensions of the Output Buffer with Pre-emphasis capability.

Transistor	Size [µm]
$M_{1,2}$	58/0.06
$M_{3,4}$	29/0.06
M_5	840/0.5
$M_{6,7}$	324/0.5
M_8	648/0.5
M_9	324/0.5
M_{10}	648/0.5
M_{11}	1648/0.5
Resistor	Size [Ω]
R_L	50

result of a AND between the external signal that indicates if the signal is at 5 Gb/s (V_{DD}) or 2.5 Gb/s (0 V), and the control signal C_5.

If C_5 is high (meaning the delay cells should be working) the value of Pre_{5G} is defined by the value of the external control signal. So the control signal discussed in Section 3.4.5.1, that controlled the switch S_3 (first and second delay cells) and S_1 (third delay cell) is C_5. $\overline{C_5}$ controls switches S_4 of the first/second dellay cells and switch S_2 of the third delay cell, respectively.

3.4.6 Simulation Results

Now that the Output Buffer architecture has been carefully explained let us analyse the simulation results for this circuit. Fig. 3.71 presents the differential output at the Output Buffer, for a PRBS sequence at 2.5 Gb/s with the minimum amplitude at the input of the LA, terminated by 50 Ω load resistors connected to V_{DD} and AC coupling capacitors as illustrated in Fig. 3.61. As mentioned before, the decoupling capacitors, $C_{1,2}$, remove the DC component of the output signals. Although they are external (and therefore its value is not decided during the design process) they have to be chosen correctly. The PRBS sequences will have signals with lower frequencies, closer to 100 kHz. This means that the capacitor can only filter the signals up to this value. This means that the cut-off frequency has to be below 100 kHz resulting in a capacitor value of approximately 32 nF with a safety margin (considering the 50 Ω impedance).

It is possible to observe the differential output for the four different combinations of the Pre-emphasis' control bits. Noticeably, each bits combination provides a different Pre-emphasis level, as theoretically expected. Also, the static differential peak-to-peak is about 400 mV which is the desired value. Ideally, when the Bit_1 and Bit_0 are zero, the waveform should present no Pre-emphasis. In pratice, the current sources' transistors parasitic capacitances create a current peak (an extra current is needed to charge those parasitic capacitances) during the transitions, resembling a Pre-emphasis effect.

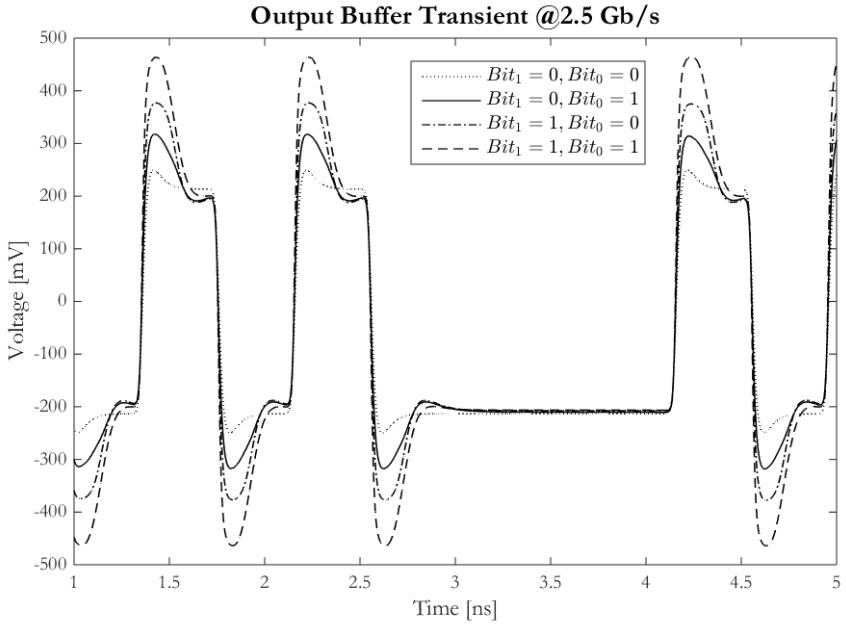


Figure 3.71: Output buffer's differential output for a 2.5 Gb/s PRBS sequence at the input of LA for different combination of the control bits ($Pre_{5G} = 0\,\text{V}$).

Table 3.26 presents a detailed analysis of the peak-to-peak voltages during the premphasis and the static ones, and a calculation of the Pre-emphasis percentages for the four situations. As expected, the maximum Pre-emphasis level - 133% - is achieved when both bits have a high logic value. The static peak-to-peak value never deviates more than 7% from the desired value, which is 400 mV.

Table 3.26: Simulated Pre-emphasis' levels according to the control bits at 2.5 Gb/s.

Bit_1	Bit_0	V_{pp} [mV]	V_{static} [mV]	Pre-emphasis level [%]
0	0	499.2	426.6	17
0	1	635.6	392.6	62
1	0	754	390.2	93
1	1	927	398.2	133

At 5 Gb/s the time response is similar except for the fact that the Pre-emphasis levels are not so defined. At this data rate the circuit is slower to respond, which means the "shape" of the Pre-emphasis is more rounded than in the previous case (when the pulse's width is 200 ps).

The simulated Pre-emphasis levels for 5Gb/s are presented in Table 3.27. As expected, the Pre-emphasis levels are equal or smaller than for 2.5Gb/s. This is due to the fact that the time that the Pre-emphasis circuit takes to settle is larger than the the delay created by the adjustable delay block. Therefore, the circuit is not able to fully reach the theoretical Pre-emphasis level.

The previous simulations did not include the package parasitics. In order to include

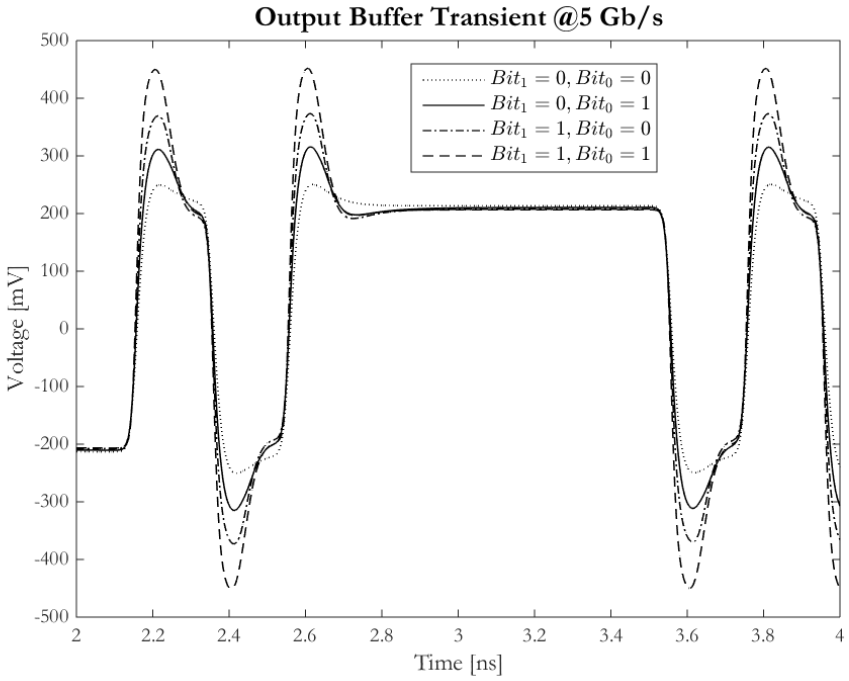


Figure 3.72: Output buffer's differential output for a 5 Gb/s PRBS sequence at the input of LA for different combinations of the control bits (Pre_{5G} = 1.2 V).

Table 3.27: Simulated Pre-emphasis' levels according to the control bits at 5 Gb/s.

Bit_1	Bit_0	V_{pp} [mV]	V_{static} [mV]	Pre-emphasis level [%]
0	0	497.8	427.2	17
0	1	622.2	399.4	56
1	0	738.6	383.4	93
1	1	899.6	390.8	130

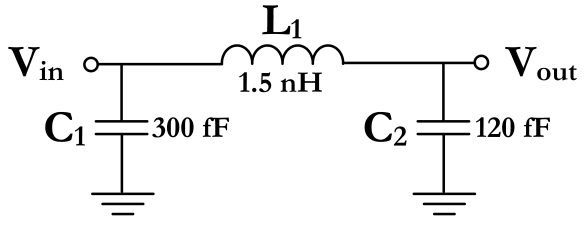


Figure 3.73: Electrical model of the package parasitics.

those, let us assume that they can be fairly modeled using the circuit in Fig. 3.73. Fig. 3.74 presents the eye diagram of the differential output of the buffer (for Bit_1 and Bit_0 equal to 0) for a 5GB/s PRBS with the minimum amplitude at the input of LA.

Analysing the Fig. 3.74, one can see that there is a little bit of ringing in the time response, as expected, which means that the paratisitic inductance L_1, and capacitance C_1 are resonating at their characteristic frequency. Obviously, and as mentioned before, this

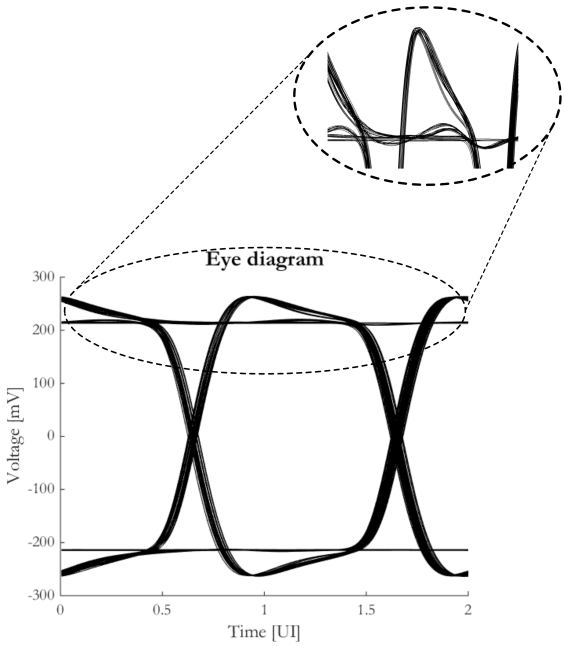


Figure 3.74: Eye diagram of the Output Buffer considering the package parasitics for a 5 Gb/s PRBS sequence at the input of LA.

is an undesarable effect since besides causing an extra current to flow (thereby wasting energy) it may also cause ISI. Table 3.28 presents some simulations' results regarding the time response of the Output Buffer.

Table 3.28: Simulation results concerning the time response of the Output Buffer at 5Gb/s.

Rise/fall time [ps]	Slew rate [GV/s]	Total jitter [UI]
64	6.8	0.06

The rise/fall times are larger than the ones of the LA but the total jitter remains the same (0.06 UI). The slew rate of the Output Buffer is also much smaller since the output swing was reduced in relation to the Limiting Amplifier.

Finally, let us analyse the power consumption of this block, as well as the output Return Loss, R_L, of the buffer. The Return Loss parameter measures the ratio of incident power by reflected power at the load (in other words, it measures the "quality" of the Output Buffer's impedance matching). It can be calculated as [37]:

$$-10\log\frac{P_R}{P_{IN}} \tag{3.44}$$

A higher Return Loss means that the matching is good and fewer power is being reflected at the load. Let us analyse these parameters with and without the package parasitics, for different combinations of the control bits and for the case of Pre-emphasis for 5 or 2.5Gb/s. Table 3.29 presents these results.

Table 3.29: Output Buffer's simulation results - power consumption and Return Loss.

Bit_1	Bit_0	Power [mW]		R_L @ 5GHz [dB]	
		Pre_{5G} [V]		With package parasitics	Without package parasitics
		1.2	0		
0	0	9.76	9.76	10.16	18.49
0	1	16.62	16.10	9.26	15.94
1	0	20.27	19.7	8.85	14.88
1	1	27.15	26.58	8.12	13.45

As expected, the power consumption of the block increases for higher Pre-emphasis levels (since the current of the main and secondary buffer are larger). The dissipation is also larger when Pre_{5G} =1.2 V, since the currents at the first and second delay cells of the tunable Pre-emphasis block are made larger to decrease the delay. Concerning Return Loss, it exhibits poor results when the packing parasitics are considered. This is due to the fact that the effective impedance seen by the transmission line is lowered by the package parasitics (if L_1 and C_1 resonate) [38]. Without considering the package parasitics circuit the output Return Loss results are fairly good.

Chapter 4

Conclusions and Future Work

4.1 Conclusions

In Chapter 2 the concept of a cascade of gain stages for the Limiting Amplifier and the implications of the number of cascaded stages on the overall system's bandwidth are addressed. The number of stages that maximises the GBW for a given power dissipation, is dependent on the voltage gain needed for the cascade. It is also concluded that the small signals' bandwidth is a conservative measure for the speed of the LA since it will work in large-signal operation on the last stages. Another issue regarding the LA is the AM-PM conversion that results in amplitude noise being converted into phase noise, resulting in jitter noise which is one of the most important metrics for the LA. If the Jitter exceeds the tolerance value the CDR can lost synchronisation and the data streams may be lost.

- It is tipically necessary to use bandwidth enhancement techniques for the Limiting Amplifier;
- The RSSI is useful to adjust the transceiver's gain and improve the SNR;
- Pre-emphasis allows for an improvement in the ISI when the transmission line exhibits losses or a low-pass characteristic;
- TID radiation effects on CMOS devices are mainly related to the charging in the oxides, which can result in the deterioration of some of the transistor performance parameters;
- An enclosed layout can be the solution to minimise the TID effects.

In Chapter 3 the implementation techniques of each block and its corresponding theoretical analysis were provided.

Regarding the Limiting Amplifier, two different bandwidth enhancement techniques were used for the gain cells. Namely, capacitive degeneration and negative Miller Capacitance. In order to use the first technique, one had to be careful regarding the peaking in the frequency response of the LA, since it could lead to undesirable deterministic jitter. This led to a the implementation of the degeneration capacitors with real PMOS transistors, in order to track variations of the dominant pole across corners and minimising peaking. This technique reduced the DC gain in about 13%, achieving a bandwidth enhancement factor of 1.61. NMC was also employed to cancel the gate-drain parasitic capacitance which, in high gain amplifiers, is a restrictive factor in terms of bandwidth, due to the Miller effect. This approach increased the bandwidth by about 1.62. The overall Limiting Amplifier was composed by a cascade of 9 gain stages, where the last one is scaled to have 8 times more current than the first one. With a current of 6.24 mA it is capable of driving the large transistors of the Ouput Buffer. The overall bandwidth extension factor is 2.6 for a bandwidth of 4.8 GHz, a gain of 59.8 dB and a power consumption below 19 mW. Furthermore, the LA presents a bandwidth of at least 80% of the data rate, and a minimum gain of 43.22 dB across all PVT corners. The LA's integrated noise results in a SNR of 10 for the minimum input amplitude. The transition times are about 60 ps for the minimum input amplitude, with a total jitter equal to 12 ps. Table 4.1 presents a comparison of this work with the referenced topologies presented in Chapter 2.

Table 4.1: Comparison of referenced LAs/VGAs with this work.

Reference	**Process** [µm]	**BW** [GHz]	**Gain** [dB]	**Input Sensitivity** [mV_{pp}]	**Supply Voltage** [V]	**Power** [mW]
[9]	0.18	4.5	32	20	1.62-1.98	12.15-14.85
[10]	0.18	1.8	44	2	1	3.7
[8]	0.6	1.25	40	5	5	130
[4] ■	0.13	5	40	N/A	2.5	47
[11]	0.25	2.5	32	2.2 ♦	2.5	53
[13]	0.13	0.8-3	35	N/A	1.2	32
[14]	0.18	3.125	45	5	1.8	95
[15]	0.9	34.7	32	N/A	1.2	97
[19]	0.35	2.1	39	N/A	1.8	79.2
[20]	0.18	6.8	26	25	3.3	45
This work ■	0.065	4.8	60	2.4♦	1.2	19

■ Radiation-tolerant;
♦ For a BER of 10^{-12}.

The RSSI was designed with successive detection architecture which implements a piece-wise linear logarithmic function. The FWRs (unbalanced source-coupled differential pairs) performed the rectification in the current domain. Theoretical analysis showed that there was a clear tradeoff between DR and detection sensitivity, and a clear dependence on the unbalancing factor. Increasing the unbalacing factor improves the characteristic of the RSSI, all the while having a negative impact on the LA's bandwidth (so it was settled to 3). This resulted on a dynamic range equal to 50.1 dB and detection

sensitivity of 11.6 mV/dB for 5 Gb/s and 12.3 mV/dB and 52.7 for 2.5 Gb/s, with a power consumption smaller than 600 µW. A special bias circuit was also developed in order to minimise the variations of the RSSI's transfer function across corners. Simulations showed that the proposed bias circuit supressed the variations on the RSSI transfer curve when compared to a regular bias circuit - variations of 26% were reduced to 9% - leading to the conclusion that the variations observed in the transfer curves are mostly resultant of the LA's gain variations. The LA impacts the RSSI's dynamic range which indirectly impacts the detection sensitivity.

A Squelch function was designed to mute the output when the input power is small. It employed redundancy techniques to ensure that no data was lost in the event of a high energy particle colliding with the Squelch's comparator. The Squelch function was also designed to be as slow as possible with a response time larger than 4.5 µs improving the system's reliability. The Output Buffer is squelched when the input current at the TIA is smaller than 1.98 µA, which is well below the sensitivity limit. This circuit has a power consumption smaller than 17 µW.

The designed Output Buffer provides for simultaneous impedance matching and Pre-emphasis function. Using a double termination CML configuration, the buffer is composed by two differential pairs. The second, auxiliary, differential pair is cross-connected with the main one. The input of the second differential pair would be delayed versions of the main buffer's input signals. The Pre-emphasis circuit was designed in such a fashion that two different data rates are possible, as well as four different Pre-emphasis amplitudes - according to external control signals. For 5 Gb/s the maximum Pre-emphasis is 130% whereas for 2.5 Gb/s it is 133%. With a differential swing of 427 mV (no Pre-emphasis), the rise and fall times of the input signal remain almost constant at the output of the buffer, and the jitter is kept constant, considering the package parasitics. The eye diagram of the Output Buffer reveals some ringing. Lastly, the buffer exhibits satisfactory results regarding the return loss, when the package parasitics are not considered - approximately 18.5 dB at 5GHz when Pre-emphasis is turned OFF.

4.2 Future Work

Firstly, the bias circuit of the Limiting Amplifier could be further investigated to minimise the gain variations of the LA across corners. If this were to be accomplished, the typical corner need not have a gain that large, and the power consumption of the block could be furtherly reduced. Not only would this improve the performance of the LA, it would also supress the variations of the Received Signal Strength Indicator transfer function. As mentioned, the RSSI's dynamic range is defined mainly by the LA, when its gain is lower it decreases and vice-versa. The consequences of all this on the RSSI's transfer function variability are huge, since it also indirectly affects the detection sensitivity. Consequently, it would also help the performance of the Squelch circuit, which would have a much more fixed threshold.

Another aspect that could be improved is the effective impedance seen at the output of the Buffer, when the package parasitics are considered (the Return Loss has poor results when the package is considered). If the bond wire inductance L_1 and parasitic capacitor C_1 of the package resonate, the effective impedance seen by the transmission line - which is supposed to be the load resistor of the Output Buffer - is lowered by the package parasitics [38]. This means that the load resistor can be chosen to be higher that the transmission line impedance, in order to accomodate for package parastics. This could minimise the ISI and save a substantial ammount of power, since it would improve the Return Loss.

Finally, finishing the layout of other blocks left undone as well as working on post-layout adjustments - on already finished layouts - would be desirable. Particularly on the MOM capacitors - it would allow to improve the area of the blocks while maintaining the performance achieved during the design process.

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Appendix A

Layouts

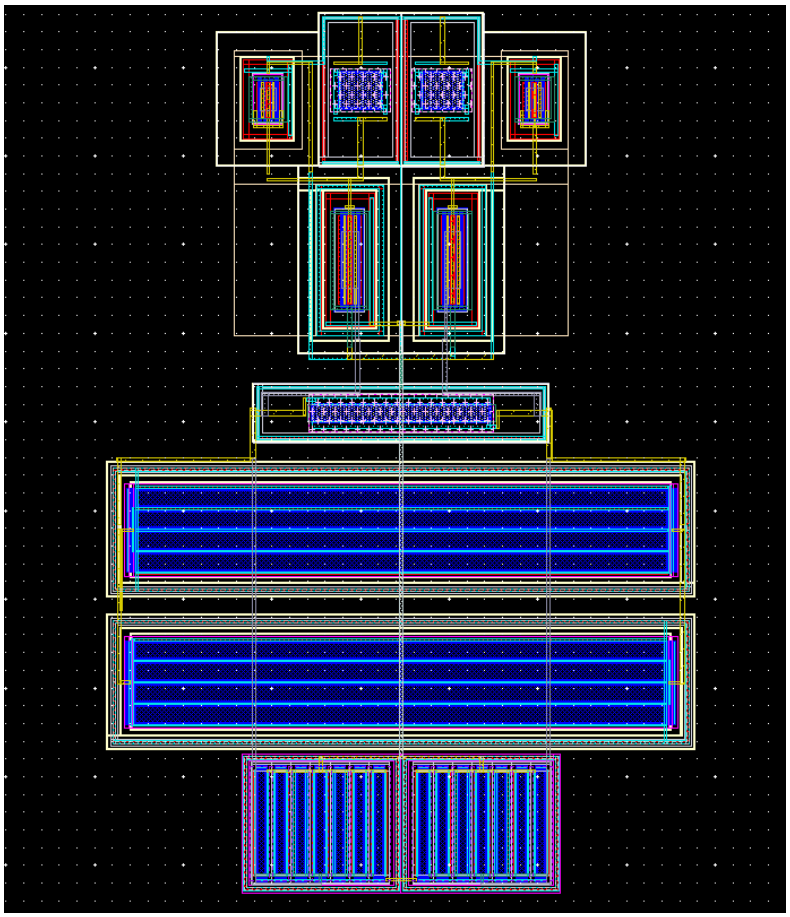

Figure A.1: Layout of the LA's first to sixth gain cell.

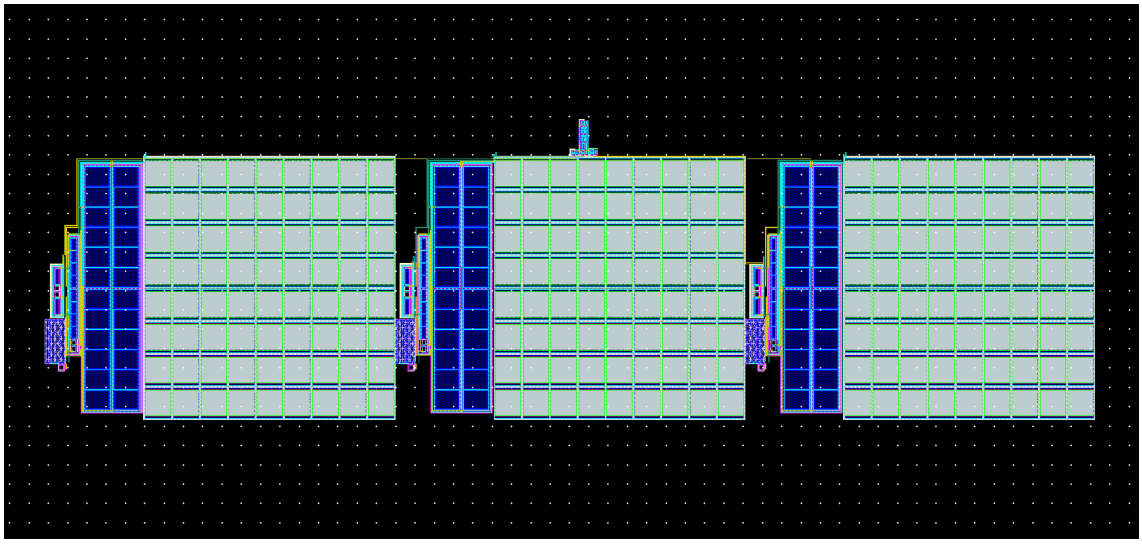

Figure A.2: Layout of the overall Squelch block.