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# Readout electronics for LGAD sensors

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Abstract: In this paper, an ASIC fabricated in 180 nm CMOS technology from AMS with the very front-end electronics used to readout LGAD sensors is presented as well as its experimental results. The front-end has the typical architecture for Si-strip readout, i.e., preamplification stage with a Charge Sensitive Amplifier (CSA) followed by a CR-RC shaper. Both amplifiers are based on a folded cascode structure with a PMOS input transistor and the shaper only uses passive elements for the feedback stage. The CSA has programmable gain and a configurable input stage in order to adapt to the different input capacitance of the LGAD sensors (pixelated, short and long strips) and to the different input signal (depending on the gain of the LGAD). The fabricated prototype has an area of 0.865 mm × 0.965 mm and includes the biasing circuit for the CSA and the shaper, 4 analog channels (CSA+shaper) and programmable charge injection circuits included for testing purposes.

Noise and power analysis performed during simulation fixed the size of the input transistor to W/L = 860 $\mu$m/0.2 $\mu$m. The shaping time is fixed by design at 1 us and, in this ASIC version, the feedback elements of the shaper are passive, which means that the area of the shaper can be reduced using active elements in future versions. Finally, the different gains of the CSA have been selected to maintain an ENC below 400 electrons for a detector capacitor of 20 pF, with a power consumption of 150 $\mu$W per channel.

Keywords: Analogue electronic circuits; VLSI circuits

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## Contents



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## 1 Introduction

Low Gain Avalanche Detectors (LGAD) represent a remarkable advance in high energy particle detection, since they provide a moderate increase (gain ~ 10) of the collected charge, thus leading to a notable improvement of the signal-to-noise ratio, which largely extends the possible application of Silicon detectors beyond their present working field. The optimum detection performance requires a careful implementation of the multiplication junction, in order to obtain the desired gain on the read out signal, but also a proper design of the edge termination and the peripheral region, which prevents the LGAD detectors from premature breakdown and large leakage current.

The Low Gain Avalanche Detector (LGAD) is based on the standard Avalanche Photo Diodes (APD) concept, commonly used in optical and X-ray detection applications, including an internal multiplication of the charge generated by radiation. The multiplication is inherent to the basic n++-p+-p structure, where the doping profile of the p+ layer is optimized to achieve high field and high impact ionization at the junction.

All avalanche diode detectors have a region with a high electrical field leading to multiplication of signal charges (electron and/or holes) flowing through this region. The gain mechanism is achieved within the semiconductor material by raising the electric field as high as necessary to enable the drifting electrons to create secondary ionization during the collection process. Normally, the junction consists of a thin and highly doped n-type layer on top of a moderately doped p-layer in which the multiplication (of electrons) takes place. A high resistivity p-type silicon substrate is typically used to produce detectors with a bulk that can be fully depleted.

Compared to standard APD detectors, LGAD (Low Gain Avalanche Detectors) structures exhibit moderate gain values. This is mandatory to obtain fine segmentation pitches in the fabrication of microstrip and pixel detectors, free from the limitations commonly found in avalanche detectors. In addition, a moderate multiplication allows the fabrication of thinner sensors, with an output signal amplitude that is as large as that from thicker sensors without internal gain. The design

of LGAD structure exploits the charge multiplication effect to obtain a silicon detector that can simultaneously measure precisely the position and time of arrival of incident particles.

The LGAD structures are optimized for applications such as tracking or timing detectors [1] for high energy physics experiments or medical applications where time resolution lower than 30 ps is required.

In this paper, an ASIC fabricated in 180 nm CMOS technology from Austria Micro Systems (AMS) with the very front-end electronics used to readout LGAD sensors is presented as well as its experimental results. The front-end is focused on tracking where noise and power constraints are more important than timing constraints. LGAD sensors, used in this paper, are produced by the Centro Nacional de Microelectrónica (CNM) which provides them in three different formats (shape of the sensor): pixelated sensors, short strip and long strips (not yet produced). The aim of this work is to provide a low power front-end designed to deal with different electronic characteristics of each LGAD version (i.e. input capacitances from 0.5 pF to 20 pF) and to use it in future colliders (e.g. ILD). Taking into account the different input capacitance and that the signal generated by the LGAD may vary depending on its gain, the front-end has to be programmable, in terms of gain, in order to adapt it to each set-up.

## 2 Front-end ASIC

The ASIC has been fabricated in a 180 nm technology from AMS. This technology has been selected basically because the price for prototyping is lower compared to technologies with a smaller channel length. Nevertheless, this technology also allows us to deal with the noise and power constraints imposed by the LGAD detector.

The front-end has the typical architecture for Si-strip readout [2], i.e., pre-amplification stage with a Charge Sensitive Amplifier (CSA) followed by a CR-RC shaper. Both amplifiers are based on a folded cascode structure with a PMOS input transistor and the shaper only uses passive elements for the feedback stage and the shaping time is fixed at 1 us. The CSA has programmable gain and a configurable input stage in order to adapt to the LGAD sensors. The fabricated prototype is 0.865 mm × 0.965 mm and includes the biasing circuits, 1 CSA, 1 channel (composed by a CSA and the shaper) and both structures are repeated with a programmable charge injection circuit at the input, included for testing purposes. The power consumption is 150 uW per channel. Figure 1 shows a scheme of the circuits included into the ASIC (a) and the layout of the whole ASIC (b).

### 2.1 Pre-amplifier (CSA)

Figure 2 shows the schematic of the pre-amplifier. This stage gives the main noise contribution to the circuit, particularly the PMOS input transistor. If the gain of the pre-amplifier is large enough to satisfy $A\,C_f \gg C_d$ and a simple CR-RC shaper is used after the pre-amplifier, the total equivalent noise charge (ENC) of the circuit [2] can be reduced to:

$$\mathrm{ENC} = \sqrt{\frac{2}{3}\mathrm{kT}\frac{1.57}{g_m}\frac{C_t^2 e^2}{\pi q^2 \tau} + \frac{K_f}{C_{ox}^2 \mathrm{WL}}\frac{C_t^2 e^2}{2q^2} + I_{leak}\frac{1.57}{2}\frac{\tau e^2}{\pi q} + \frac{\mathrm{kT}}{R}\frac{1.57\tau e^2}{\pi q^2}} \tag{2.1}$$

where kT is the product of the Boltzmann constant and the temperature, $\tau$ is the shaping time, $C_t$ is the total capacitance at the input, $C_{ox}$ is the gate oxide capacitance per unit area, $K_f$ is the flicker

noise constant, q is the electron charge, W, L and $g_m$ are the width, length and the transconductance of the input transistor. This expression can be simplified to:

$$\mathrm{ENC} = a + bC_\mathrm{d} \tag{2.2}$$

where $C_d$ is the detector capacitance. A first approach to find the proper dimensioning of the input transistor has been done using a Matlab script, where the transconductance value has been calculated with the EKV model [2]. The script permits to minimize the ENC while maintaining low power consumption. The proposed solution is then re-simulated and improved in Cadence, resulting in a transistor dimension of 860 $\mu$m/0.2 $\mu$m with a current consumption of 42 $\mu$A. Although flicker noise is increased when using small lengths, ENC is not, as can be seen in table 1. Table 1 summarizes ENC values in the worst case (where the $C_d$ is near to 20 pF) using a transistor width of 860 $\mu$m and different lengths.

**Table 1**. ENC for a 20 pF detector capacitance and an input transistor width of 860 $\mu$m.

| L ($\mu$m) | a (e) | b $C_d$ (e) | ENC (e) 20 pF |
|---|---|---|---|
| 0.20 | 148 | 242 | 390 |
| 0.50 | 148 | 236 | 384 |
| 0.75 | 153 | 240 | 393 |
| 1.00 | 159 | 245 | 404 |

As the detector capacitance may vary depending on the type of LGAD that we use and the generated signal may vary depending on the gain of the LGAD, the pre-amplifier can be configured to have 2 different gains (feedback capacitor of 100 fF or 500 fF).

The bias circuit for the CSA was designed to reduce the noise [5–7]. The bias voltages have been selected to have a power consumption as low as possible while having the maximum gain and bandwidth. Final values on the fabricated pre-amp are a gain of 67,5 dB, a gain bandwidth product (GBW) of 19,5 MHz and a power consumption below 80 $\mu$W.

### 2.2 Shaper

As commented, the shaper is also based on a folded cascode structure with a PMOS input transistor, however the noise constraints on the input transistor are relaxed and it can be sized with a lower width. Nevertheless, gain, GBW and power consumption values are similar to the CSA.

In this prototype, input capacitor and resistor as well as the feedback capacitor and resistor are passive and selected to have a shaping time of 1 us. Process variations during fabrication eventually result in a measured shaping time of 860 ns.

### 2.3 ASIC characterization

Tests on the fabricated ASIC have been done using programmable charge injection circuits [8] which are connected to the input of one CSA and to the input of one channel. These circuits inject a known charge, which can go from 4 fC to 208 fC. The results show that the CSA has a gain of 8,86 mV/fC



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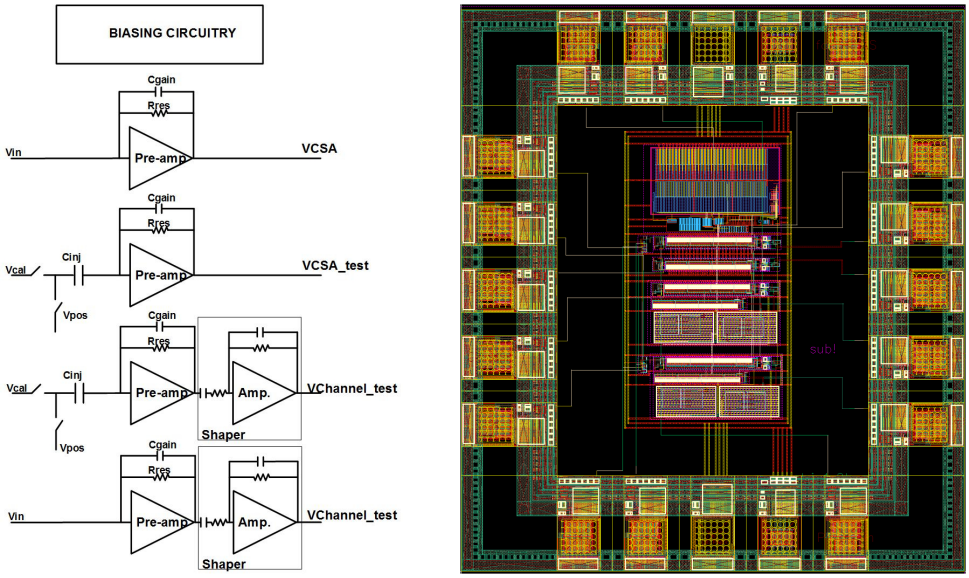


**Figure 1**. (a) Schematic of the circuits included in the ASIC. (b) Layout view of the fabricated ASIC.

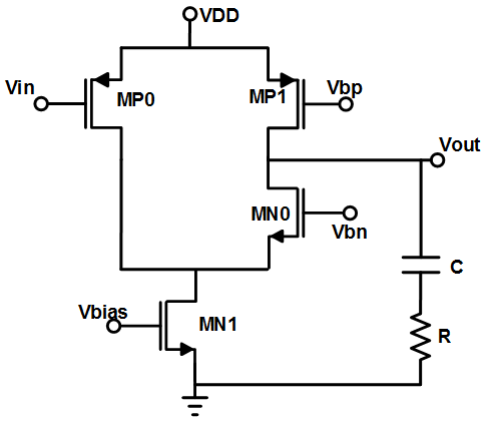


**Figure 2**. Schematic of the pre-amplifier.

when the feedback capacitor value is 100 fF and a gain of 1,82 mV/fC when the feedback capacitor value is 500 fF. For the whole channel (CSA followed by the shaper) the gains are 2,64 mV/fC and 0,74 mV/fC when the feedback capacitor value is 100 fF and 500 fF respectively.

The electronic noise at the laboratory has been acquired by measuring the variation of the maximum peak at the shaper's output when injecting a known charge. With the sensor connected (pixelated LGAD with a detector capacitance of 4 pF) and the ASIC supplied with batteries the noise root mean square voltage (Vrms) is 80 $\mu$V, which is equivalent to an ENC of 190 e and 675 e for the high and low gain configurations. The results agree with the simulations despite the process variations that changed the shaper peaking time.

## 3 Test with a 6 × 6 LGAD matrix

In order to demonstrate that the analog front-end circuits operate properly, the circuit was tested with a 6 × 6 LGAD matrix provided by CNM. The main goals of these tests are to measure the gain uniformity from pixel to pixel and to measure the crosstalk.



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As the LGADs provided by CNM are DC sensors, the charge injection circuit are reprogrammed to work as a decoupling capacitor. Figure 3 shows a schematic of the test circuit, where the ASIC is contains the decoupling capacitor, the CSA and the shaper. Two buffers are included in the printed circuit board (PCB) connected to the ASIC's output. With this configuration and the supply sources connected to the electrical network, the noise of the whole system at the output of the buffers is Vrms is 0,73 mV. Hereinafter, this value will be taken as the whole system voltage error of the measurements.

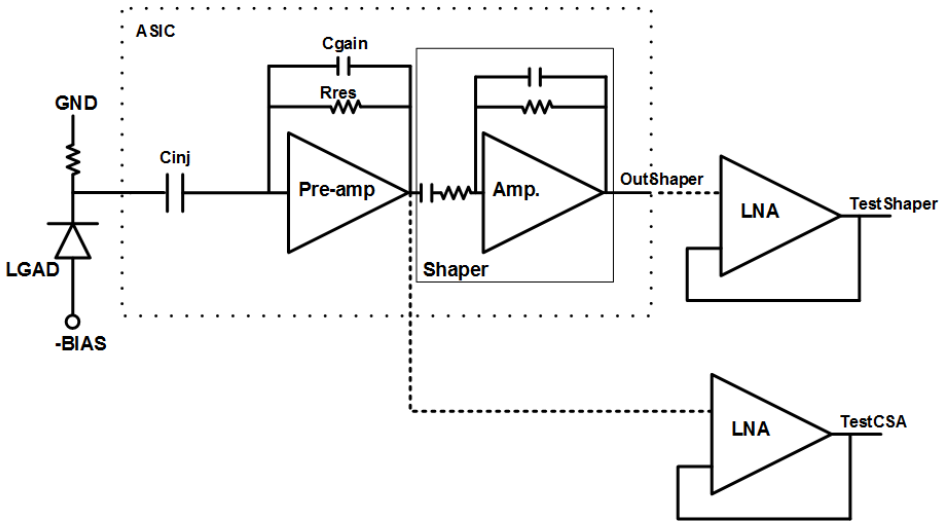


**Figure 3**. Schematic of the test circuit.

The first test consists in using the whole channel to measure the response of each pixel. To do this, the LGAD matrix is placed on a board which is moved using micro-positioners moved by micro-motors. Since the ASIC only has one entire channel to measure six different sensors, an adaptive board with an analogue switch controlled by an FPGA is used to select each pixel. A red laser is used to simulate the impact of an ionization particle. As the spot of the laser is quite large, a 100 um pin-hole is placed between the laser and the LGAD matrix. Figure 4 shows a picture of the LGAD matrix placed on the board with only one row bonded (a), and the setup of the test, with the laser, the pin-hole and the LGAD matrix (b).

Figure 5 shows the response of each pixel when they are illuminated by the laser. In this test, the LGAD matrix is back illuminated and biased at −420 V. The results show that the response of each pixel is quite similar. Furthermore, Pixel6, which is the ring used to bias, has the expected behaviour.

The next test is performed to measure the crosstalk. In order to appreciate more the crosstalk, only the CSA is used in this case because of its higher gain. For this test, every pixel is back illuminated again, however one pixel is covered in order to avoid illumination. The response of this pixel is measured together with the other pixels to see if there is any response when neighbour pixels are illuminated. Figure 6 shows the results of the crosstalk test. In this case the response of the illuminated pixels are still similar. The crosstalk, even taking into account that Vrms is 0,73 mV, is almost unappreciable.

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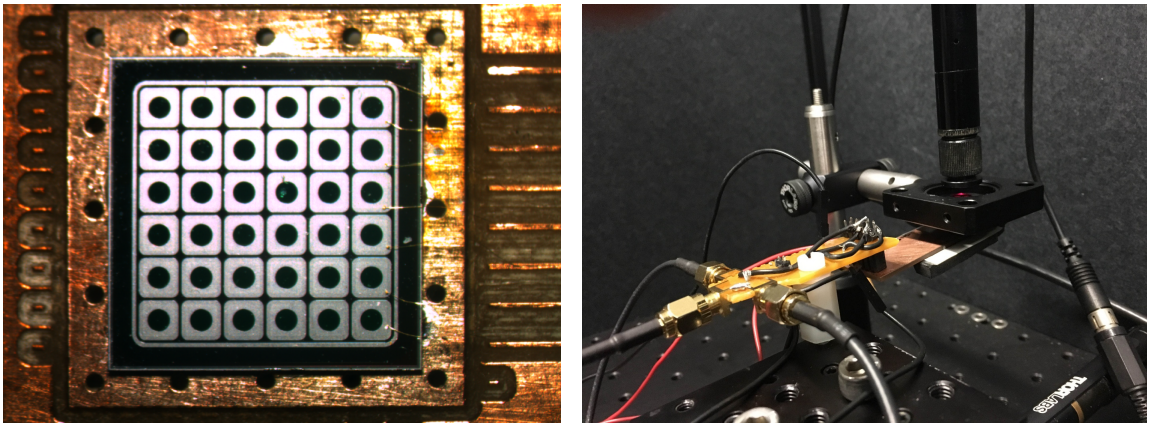

**Figure 4**. (a) LGAD matrix with one row bonded to the board. (b) Test setup with the laser, pin-hole and LGAD matrix. The LGAD matrix board is moved using micro-positioners.

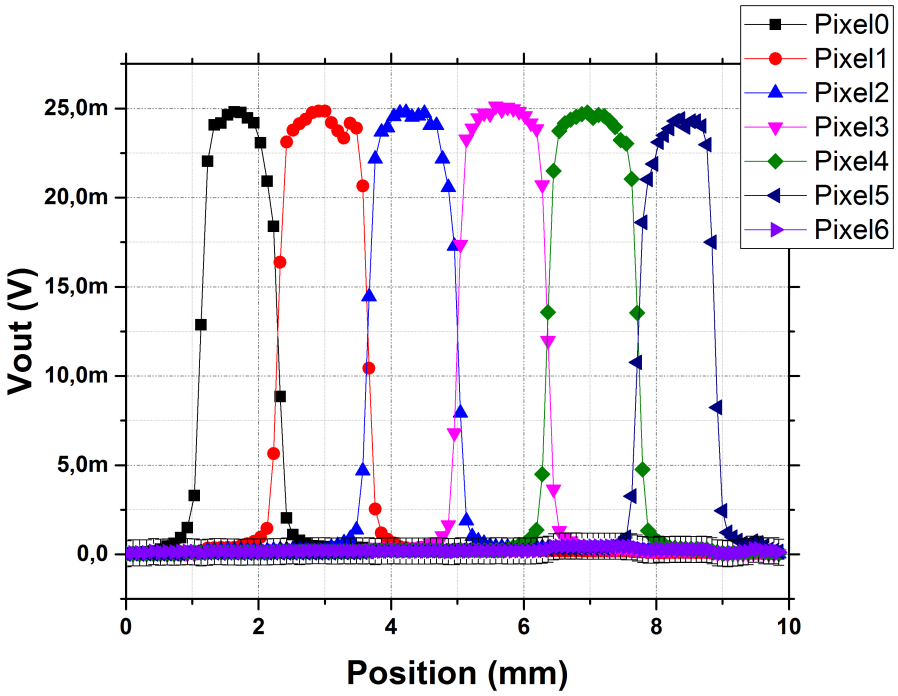


**Figure 5**. Response of each pixel when they are illuminated by the laser. In this test, the LGAD matrix is back illuminated and biased at −420 V and Vrms = 0,73 mV. The acquired signal is the average over 10000 measurements.

## 4 Conclusions

It is the first time that a pixelated LGAD matrix has been measured with a custom designed ASIC. The ASIC contains the very front-end electronics to readout the LGAD sensors. During the preliminary test, it has been demonstrated that the response of the LGADs, comparing pixel to pixel, is very similar. In addition, the crosstalk has been also measured and it is unappreciable compared to the signal generated by the LGAD.



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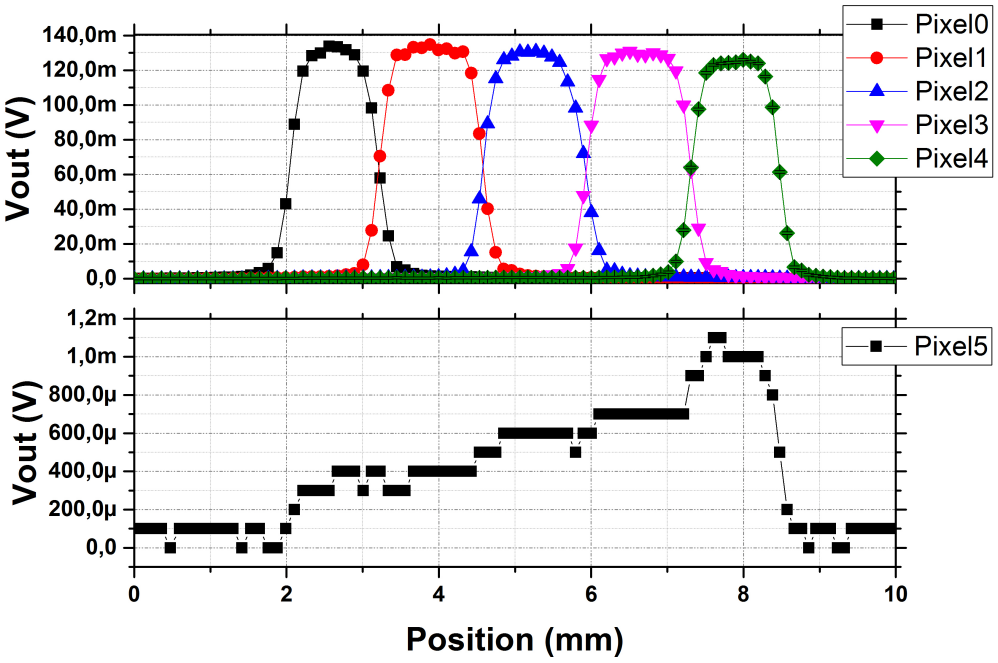


**Figure 6**. Response of Pixel 0 to Pixel4 when they are illuminated by the laser. Pixel5 is taped to measure crosstalk In this test, the LGAD matrix is back illuminated and biased at −420 V and Vrms = 0,73 mV. The acquired signal is the average over 10000 measurements.

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