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Voltage step stress: a technique for reducing test time of device ageing

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***Abstract*—Device ageing leads to circuit malfunction and must be controlled. During ageing, defects build up slowly and the test is time consuming and costly. The typical ageing tests are repeated ~5 times under different voltages. To reduce the test time, the voltage step stress (VSS) technique is proposed, which replaces the multiple tests under different voltage by a single test and saves time. This paper reviews the recent development of the VSS technique. After presenting its underlying principle, its applicability will be demonstrated for both the negative bias temperature instability and hot carrier ageing.**

Keywords-NBTI, Hot carriers, Ageing, Instabilities, Defects, Degradation, Lifetime.

I. INTRODUCTION

As device sizes are downscaled to sub-10 nm range, the operation voltage cannot be reduced proportionally. This is because the silicon bandgap will not reduce with device sizes. Consequently, the electrical field within devices increases for each generation of CMOS technologies. High electrical field accelerates device ageing and in turn reduces device lifetime. To avoid circuit malfunctioning, it is essential to control the ageing within its given specification and this requires proper testing.

Ageing occurs because of a gradual build-up of defects, such as interface states [1,2], electron traps [3,4], and positive charges [5,6] in gate dielectric. This is a slow process and the typical specified device lifetime is 10 years. To accelerate the ageing, it is common to apply voltages higher than the normal use voltage during the stress tests [7,8]. Typical procedure is to repeat the test 5~6 times under different voltages, as specified by the JEDEC standard [9]. One example is given in Fig. 1.

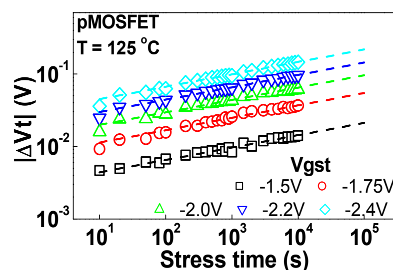

Figure 1. An example of the conventional multiple tests under different voltages for NBTI [10].

To reduce the test time and save cost, the voltage step stress (VSS) technique has been proposed, replacing the multiple tests under different voltages in Fig. 1 by a single test [10-12]. Its underlying principle will be reviewed in section II. Section III demonstrates its applicability to the negative bias temperature instability (NBTI) and Section IV shows that it also works for hot carrier ageing (HCA). Finally, conclusions are drawn in Section V.

II. PRINCIPLE OF VOLTAGE STEP STRESS TECHNIQUE

It used to be well accepted that ageing follows the power law in Eq.(1) against stress time and voltage [9-11]:

$$\Delta Vt = A \cdot Vg^m \cdot t^n \qquad (1)$$

where ΔVt is the threshold voltage shift, Vg the stress gate bias, t the stress time, A, m, and n are constants for a given temperature. This is challenged by the non-power law behavior of NBTI shown in Fig. 2, which is widely observed when measured by the fast (~µs) pulse technique that minimizes recovery [13,14]. Such non-power law behavior is successfully explained by the As-grown-Generation (AG) model [14], where defects are divided into two groups: As-grown hole traps (AHT) and Generated defects (GD). Their separation is based on their different energy profiles, charging and discharging properties, as detailed in early works [15,16].

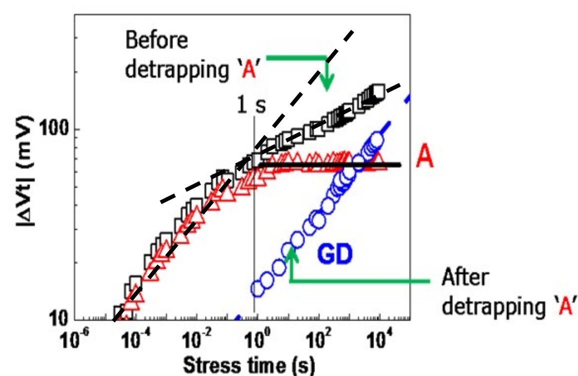

Figure 2. When measured by fast pulse technique (5 µs) NBTI (symbol '□') does not follow power law. As-grown hole traps ('Δ') saturates. The generated defects (GD, 'o')) follow a power law [14].

Charging AHTs can dominate the NBTI initially, leading to the deviation from the power law in Fig. 2 [14,16]. AHTs are pre-existing and not caused by stresses, so that it should not be included in the ageing process [14]. After removing AHTs, the power law is restored for the ageing kinetics. This work will focus on the component that follows the power law hereafter.

For the voltage acceleration in Eq.(1) to be valid, the underlying assumption is that the same types of defects are generated under different Vg and higher Vg only accelerates the generation rate. Once a defect precursor is converted into a defect under one Vg, it will not be available even if a higher Vg is applied later on the same device. Since a higher Vg will not introduce new type of defects, its induced ageing can be considered as equivalent to the ageing under a lower Vg for an effective longer time, as shown in Fig. 3.

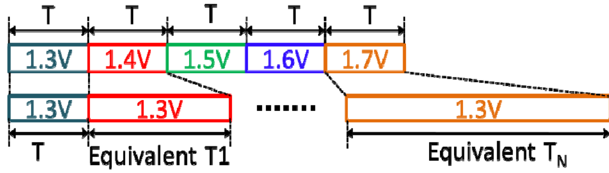

Figure 3. Principle of voltage step stress: a stress under a higher voltage is equivalent to a stress under a lower voltage for an effetive longer time. [11].

Based on Eq.(1), if a device is stressed under V2 for a time t, its effective time, teff, to reach the same ΔVt under a stress voltage V1 is

$$A \cdot {V_2}^m \cdot t^n = A \cdot {V_1}^m \cdot t_{eff}^n \quad (2)$$

Re-arranging Eq. (2), we have:

$$t_{eff} = t \cdot (\frac{V_2}{V_1})^{m/n} \quad (3)$$

teff>t for V2>V1, since a stress under higher bias is equivalent to a stress under lower bias for a longer time. If V2 is applied after V1, the total equivalent time will be t+teff. The time can be added together because the ageing kinetics can be transformed into a linear process in Eq.(4). For a linear process, the same time duration, (t_2—t_1), will give the same function difference, independent the starting point t_1. This lays the foundation for the voltage step stress (VSS) technique, as it allows different stress voltages being applied to the same device in series. The stress voltage can be stepped up either by a constant ratio, such as 10% each step [10], or by a constant value, such as 0.1 V shown in Fig. 3 [11].

$$\sqrt[n]{\Delta Vt} = \sqrt[n]{A} \cdot Vg^{m/n} \cdot t \quad (4)$$

III. VSS FOR NBTI

A typical result of NBTI under VSS stress is given in Fig. 4. The test starts with V1=-1.5 V for 1000 sec. The voltage is then increased by a factor of 1.1 in each step, i.e. V2=1.1×V1, and the stress time is kept at 1000 sec for each step.

The data at V1 in the first 1000 sec is fitted with a power law to extract the time exponent, n. Since ageing is faster under higher voltage, the threshold voltage shift, ΔVt, under V2 clearly moves above the power law in Fig. 4. Each higher voltage causes a further acceleration, as expected.

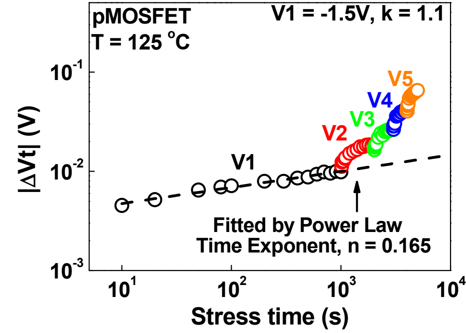

Figure 4. A typical result of NBTI under VSS stress. The stress voltage was increased by 10% in each step and the stress time is 1000 sec for each step. [10].

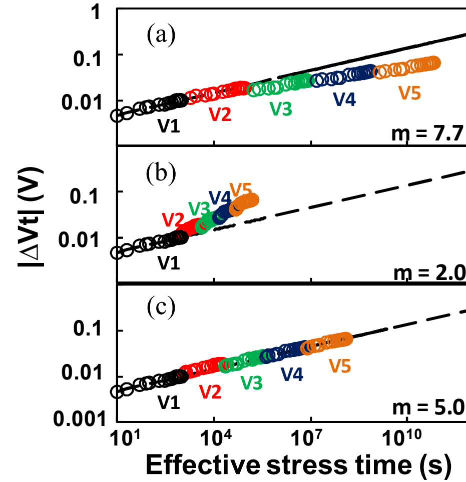

Figure 5. The impact of different voltage exponent, m, on converting the test time under higher voltages to the effective time at V1. (a) m=7.7, (b) m=2.0, and (c) m=5.0. [10].

The voltage exponent, m, can be extracted by fitting the test data at higher voltage with the power law obtained from the data at V1 (The line in Fig. 5). The effective time is calculated from Eq.(3). On one hand, Fig. 5a shows that if m is too high, the teff is too long and the test data under higher voltage will be extended below the power law line. On the other hand, Fig. 5b shows that if m is too low, the teff is too short and the test data under higher voltage will be

compressed to above the power law line. Fig. 5c shows that, when the correct m is used, the data under higher voltage will fall on the power law line. As a result, m can be extracted from the minimum error by fitting the data under higher voltage with the power law, as shown in Fig. 6. This allows the voltage exponent being extracted from a VSS test on a single device, rather than the multiple tests on different devices illustrated in Fig. 1.

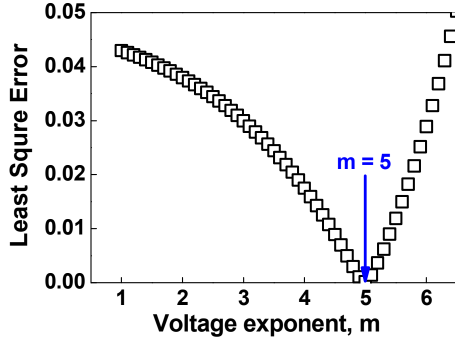

Figure 6. The voltage exponent, m, is extracted from the point of least square error when fitting the test data under higher voltages to the power law line in Fig. 5. [10].

To test the accuracy of the m and n extracted by the VSS technique, they are used to calculate the ΔVt under a constant voltage stress. Fig. 7 shows that the calculation agrees well with the test data.

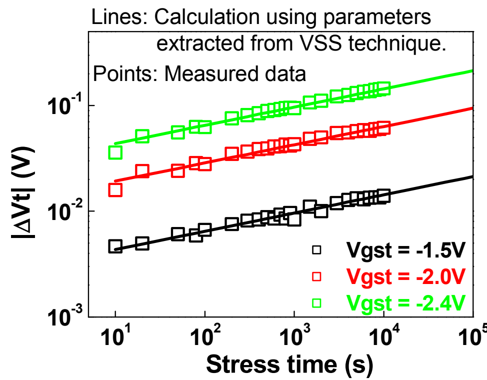

Figure 7. The voltage and time exponents, m and n, extracted by the VSS technique is used to calculate the ΔVt (lines) and compared with the test data under contant voltage stresses (symbols). Good agreement is obtained. [10].

IV. VSS FOR HOT CARRIER AGEING

Unlike the uniform degradation of NBTI, hot carrier ageing (HCA) occurs near the drain junction, where the space charges create a high field, as shown in Fig. 8. To test the applicability of VSS technique to HCA, a constant voltage step of 0.1 V is used in Fig. 9, starting from 1.3 V and ending at 1.7 V. The hot carriers are generated by applying Vd=Vg. The voltage acceleration of HCA can be clearly observed from Fig. 9.

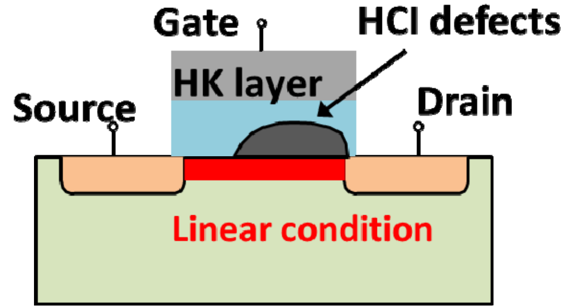

Figure 8. A schematic illustration of the non-uniform HCA. Defects are created near the drain junction.

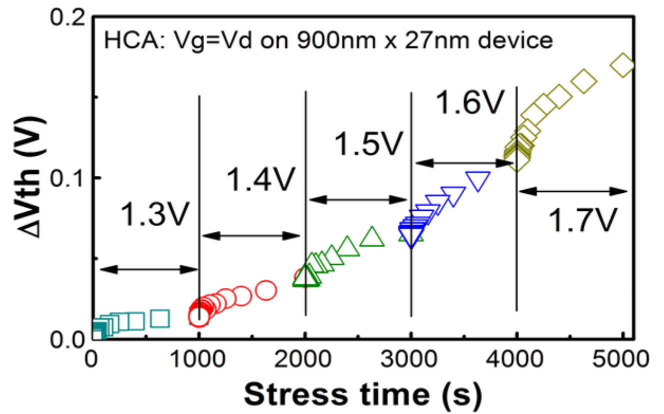

Figure 9. The hot carrier VSS stress. The stress was carried out under Vg=Vd and both Vg and Vd are increased by a constant step of 0.1 V. The stress time of each step is 1000 sec. [11].

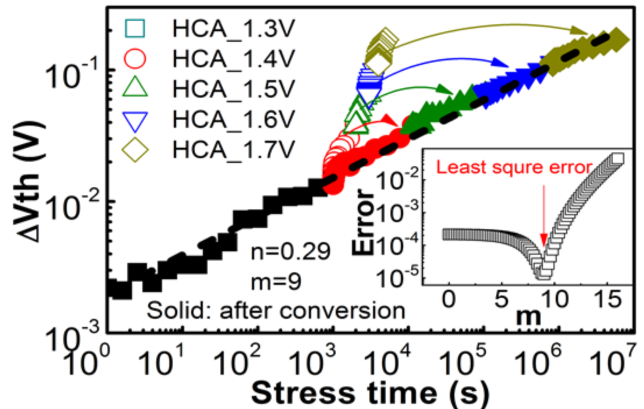

Figure 10. The extraction of voltage exponent, m, of HCA by fitting the test data of high stress voltages with the power law of the lowest voltages, Vg=Vd=1.3 V. The inset shows that the correct m gives the minimum error. [11].

Using Eq.(3), Fig. 10 shows that the test data under higher stress voltages can be converted to an equivalent longer stress time under lower voltage. The voltage

exponent, m, can be extracted from the minimum error point for fitting the test data with the power law.

To test the accuracy of m and n extracted by VSS with a stress voltage between 1.3 V and 1.7 V, they are used in Eq.(1) to predict the HCA under lower stress voltages. Fig. 11 shows that good agreement has been achieved.

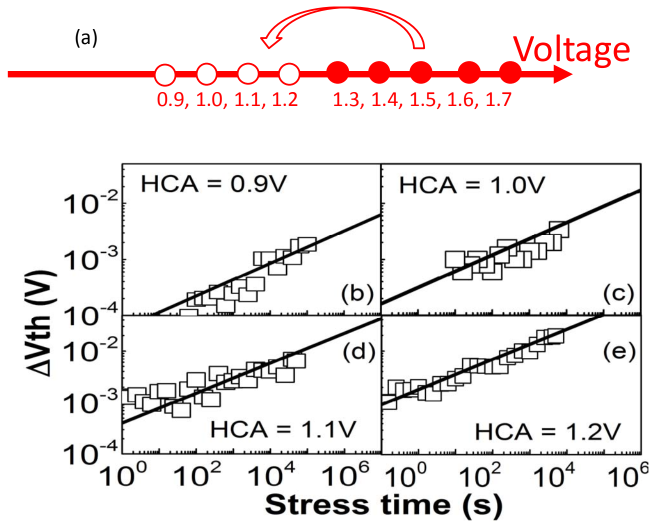

Figure 11. Verification of the voltage and time exponents, m and n in Eq.(1), extracted by VSS technique for HCA. (a) shows that the m and n were extracted in the voltage range between 1.3 V and 1.7 V. They were used to calculate the HCA under lower voltages: (b) 0.9 V; (c) 1.0 V; (d) 1.1 V; and (e) 1.2 V. [11].

V. CONCLUSIONS

Ageing can be a slow process and it is common to accelerate it by raising stress voltages. The multiple constant voltage stresses are time consuming. This work gives a review of the proposed voltage step stress (VSS) technique. Based on the assumption that the types of generated defects are independent of stress voltage and higher voltage only accelerate the generation rate, VSS applies different stress voltages to the same device. The test data under higher voltages are converted to an effective longer stress time under lower voltage. The voltage exponent is extracted by fitting the power law of lower voltage. The applicability of VSS to both NBTI and HCA is demonstrated and the accuracy of the extracted parameters is verified. This allows replacing the multiple tests by a single test and saving test time.

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