Jones, M, Levi, E and Darijevic, M

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A dc-link voltage stability analysis technique for hybrid five-phase open-end winding drives

Milan Darijevic[1], Martin Jones[2*], Emil Levi[2]

[1] Kinestas d.o.o, Belgrade, Serbia
[2] Faculty of Engineering and Technology, Department of Electronics and Electrical Engineering
Liverpool John Moores University, Liverpool, UK
[*]m.jones2@ljmu.ac.uk

Abstract: This paper studies the dc-link voltage stability for a hybrid five-phase open-end winding (OeW) drive operating under carrier based (CB) pulse-width modulation (PWM). The drive consists of a five-phase induction machine, supplied using one three-level and one two-level voltage source inverter (VSI). This configuration is analysed for the case of isolated dc-link rails, while dc-link voltage ratio is considered as an additional degree of freedom. It is demonstrated that different dc-link voltage ratios lead to the different overall number of voltage levels across stator windings. Modulation strategies are investigated and their performances are analysed from the dc-link voltages stability point of view. An analytical method for dc-link voltage stability analysis is presented. Results show that the four-level configuration always leads to stable dc-link voltages, regardless of the modulation strategy. On the other hand, if six-level configuration is combined with modulation strategies that lead to an optimal harmonic performance, not all dc-link capacitor voltages will be in balance depending on the operating conditions.

1 Introduction

The open-end winding (OeW) supply concept has been under intensive scrutiny for the last 25 years [1-2]. OeW drives are considered as an alternative to single-sided multilevel inverter feeding, which enables realisation of multilevel supply by using simpler inverter structures [1-2]. The main benefits of this concept are related to the distributed machine feeding structure, which allows easier inverter construction, offers several options for drive reconfiguration [3-4], and increases possibilities for post-fault control development [5-7]. OeW drives offer greater scope for increasing the operating speed range [3, 8-9]. A matrix converter based OeW drive has recently been investigated as a means of eliminating common mode voltages which lead to bearing damage and electrolytic capacitor degradation [10]. The OeW structure offers attractive features for EV applications including integrated fast charging systems [11]. When compared to the conventionally used two-level drives, multilevel structure enables utilisation of higher overall dc-link voltages, by eliminating the limitation that comes from voltage blocking characteristic of individual switches. Usage of multiphase machines instead of three-phase ones enables further increment of the drive power, by splitting the overall drive current on more than three phases [12]. Multiphase concept also offers an easier development of post-fault control strategies, based on either simpler solutions or solutions without any additional hardware, when compared to solutions for three-phase drives. For these reasons multiphase machines have attracted considerable interest over the past 20 years and have been investigated for use in more-electric aircraft, offshore wind and naval applications [13].

In general, dc-link capacitor voltage balancing is an important topic for all multilevel voltage source topologies [14-19], since development of modulation methods usually assumes nearly constant dc-link voltages. Besides, any unexpected voltage variation across capacitor terminals may lead to an overvoltage and ultimately breakdown. A solution to this problem is to use auxiliary circuits, similar to braking choppers in two-level VSIs, in order to limit capacitor voltage rise above a certain level. In that case, unbalanced capacitor discharge causes additional energy losses, due to surplus energy dumping. An alternative hardware based approach is given in [15, 16]. However, it also leads to a more complex structure with an increased component count, which is in contradiction with the primary motivation for the OeW drive development.

A software approach, i.e. modification of the modulation strategy, is a less costly and more elegant solution [17-20]. It is shown in [17] and [18] that so-called decoupled modulation techniques avoid the switching states that lead to overcharging for the case when the OeW drive comprises two two-level three-phase and five-phase inverters, respectively. There is however, a trade-off between harmonic quality of produced waveforms, switching losses and capacitor voltage balancing. The work presented in [19] proposes a three-phase modified coupled modulation method, which is able to balance the dc-link and maintain high harmonic performance, while [20] employs a discontinuous PWM to achieve dc-link voltage balancing in the OeW drive comprising two two-level VSIs.

This paper analyses a new OeW multiphase drive topology suitable for high power applications [21] and investigates the modulation strategies with particular emphasis on the dc-link stability building on the analysis method proposed in [18]. In Section 2, the topology is at first analysed using the equivalent drive modelling approach [21]. It is shown that this drive can be made equivalent to a four-, five- or six-level single-sided supply, depending on the ratio of dc-link voltages. Coupled and two decoupled CB PWM methods [22, 23] are briefly reviewed in Section 3. Section 4 is dedicated to the analysis of the dc-link voltage stability, with regard to the dc-link voltage ratio and modulation strategy. Experimental results are presented in Section 5, while Section 6 concludes the paper.

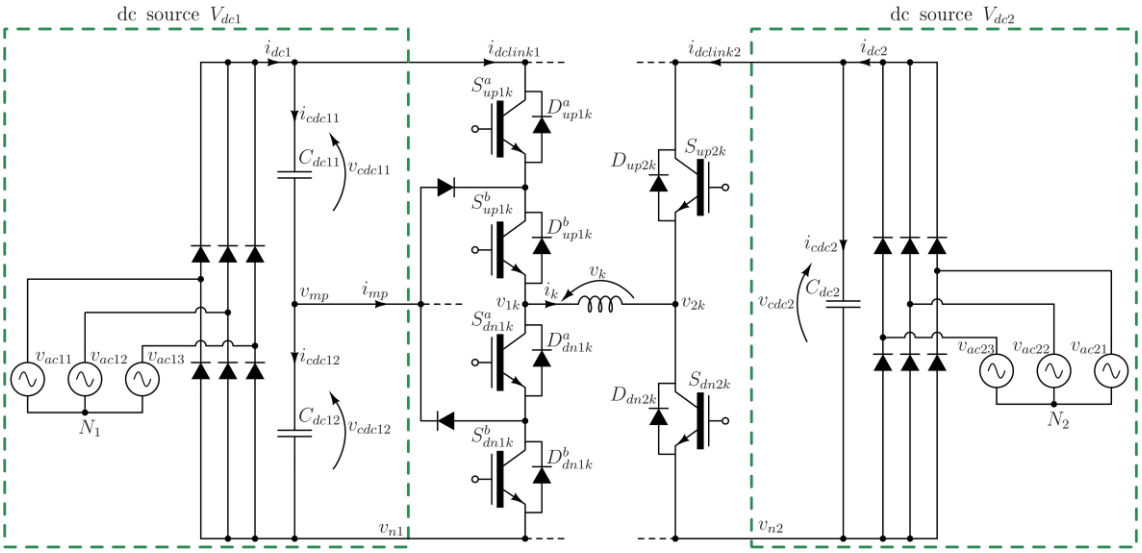

Fig.1. *One drive's phase that represents equivalent drive model [18, 24] for five-phase open-end winding topology with one three-level and one two-level VSI.*

2 Analysis of the hybrid five-phase open-end winding topology

One phase of the analysed drive topology is shown in Fig. 1. Each VSI is connected to one set of stator winding ends. Leg voltages of VSI_1 and VSI_2 are denoted with v_{1k} and v_{2k} for the k^{th} drive phase and measured with respect to the bottom dc-link rail potential of the corresponding inverter, v_{n1} and v_{n2}, respectively. Phase voltage and phase current in the k^{th} drive phase are labelled with v_k and i_k, respectively. In Fig. 1, two complementary pairs of power switches in VSI_1 are denoted with superscripts *a* and *b* (S^a_{up1k} and S^a_{dn1k}, S^b_{up1k} and S^b_{dn1k}) for the k^{th} drive phase. Complementary switches in VSI_2 are labelled as S_{up2k} and S_{dn2k}. In order to prevent dc-link short circuiting, switches with the indices "up" and "dn" should not be turned on at the same time. Having that in mind, analysis is simplified using switching states, defined as:

- $S^a_{1k} = 1$ if S^a_{up1k} or D^a_{up1k} is turned on; $S^a_{1k} = 0$ if S^a_{dn1k} or D^a_{dn1k} is turned on;
- $S^b_{1k} = 1$ if S^b_{up1k} or D^b_{up1k} is turned on; $S^b_{1k} = 0$ if S^b_{up1k} or D^b_{up1k} is turned on;
- $S_{2k} = 1$ if S_{up2k} or D_{up2k} is turned on; $S_{2k} = 0$ if S_{dn2k} or D_{dn2k} is turned on.

Regardless of the chosen modulation strategy and the rest of the drive, it is clear from Fig. 1 that the output voltage of VSI_1 (i.e. v_{1k} with respect to v_{n1}) is determined with S^a_{1k} and S^b_{1k}:

- $S^a_{1k} = 1$ and $S^b_{1k} = 1$ results in $v_{1k} = V_{dc1}$;
- $S^a_{1k} = 0$ and $S^b_{1k} = 1$ results in $v_{1k} = v_{mp} = V_{dc1}/2$;
- $S^a_{1k} = 1$ and $S^b_{1k} = 0$ results in $v_{1k} = Z$;
- $S^a_{1k} = 0$ and $S^b_{1k} = 0$ results in $v_{1k} = 0$;

The third switching combination listed above results in the off state of S^b_{up1k} and S^a_{dn1k}, meaning that the neutral point clamped (NPC) leg output voltage is in this case determined by conduction of antiparallel diodes and the phase current sign. This is referred to as a high impedance state (Z). Switching between 0 and $V_{dc1}/2$ is referred to as low-side PWM operation, while high-side PWM corresponds with switching between $V_{dc1}/2$ and V_{dc1}. The equivalent drive model [18, 24], depicted in Fig. 1, shows that there are $2^3 = 8$ possible switching combinations per one drive phase. The resulting leg and phase voltage levels are given in Table 1 using the dc-link voltage ratio as a system parameter:

$$r = \frac{V_{dc1}}{V_{dc2}} \tag{1}$$

Inspection of Table 1 shows that the topology is capable of producing up to six voltage levels. For some values of r however, certain switching combinations result in the same phase voltage level. For example, for $r = 1$ switching combinations 2 and 7 result in the same voltage level. For $r = 2$, voltage levels of $V_{dc}/(r + 1)$ and 0 can be obtained using two different switching combinations. This is a direct consequence of the dc-link voltage ratio, since $V_{dc1} = 2 \cdot V_{dc2}$ results in equivalence $v_{mp} = V_{dc1}/2 = V_{dc2}$.

Table 1. Relationship between switching states, leg and equivalent voltages.

N	S^a_{1k}	S^b_{1k}	S_{2k}	v_{1k}/V_{dc}	v_{2k}/V_{dc}	Equivalent v_k/V_{dc}
1	1	1	0	$r/(r+1)$	0	$r/(r+1)$
2	1	1	1	$r/(r+1)$	$1/(r+1)$	$(r-1)/(r+1)$
3	1	0	0	Z	0	Z
4	1	0	1	Z	$1/(r+1)$	Z
5	0	1	0	$r/(r+1)/2$	0	$r/(r+1)/2$
6	0	1	1	$r/(r+1)/2$	$1/(r+1)$	$(r/2-1)/(r+1)$
7	0	0	0	0	0	0
8	0	0	1	0	$1/(r+1)$	$-1/(r+1)$

The overall dc-link voltage supply is equal to $V_{dc} = V_{dc1} + V_{dc2}$. This is clear from the equivalent drive model, where in the case of $v_{n1} = v_{n2}$ one would find that maximal and minimal equivalent phase voltage are equal to V_{dc1} and $-V_{dc2}$, respectively. Maximal voltage amplitude across the load is equal to $(V_{dc1} + V_{dc2})/2$. The distance between the minimal and maximal voltage levels is always equal (normalisation with V_{dc} is used, while v_{n1} is considered as the zero potential). These two voltage levels define the co-domain for phase voltage reference in the case of CB PWM. In order to determine the actual phase voltage waveform, common-mode voltage (CMV) v_{n2n1} should be taken into account. Therefore, the phase voltage waveform can be obtained using:

$$v_k = v_{1k} - v_{2k} - v_{n2n1} \tag{2}$$

Assuming that the sum of all phase voltages is zero, the CMV is calculated as:

$$v_{n2n1} = v_{n2} - v_{n1} = \frac{1}{5}\sum_{k=1}^{5}(v_{1k} - v_{2k}) \tag{3}$$

Using the equivalent drive model in Fig. 1 and switching state combinations in Table 1 one is able to calculate equivalent voltage levels for different values of r.

$$\begin{aligned} &l_1 = 0 \\ &l_2 = \begin{cases} 1/2 \cdot r/(r+1), & \text{if } r < 2 \\ 1/(r+1), & \text{if } r \geq 2 \end{cases} \quad l_3 = \begin{cases} 1/(r+1), & \text{if } r < 2 \\ 1/2 \cdot r/(r+1), & \text{if } r \geq 2 \end{cases} \\ &l_4 = \begin{cases} 1 - 1/2 \cdot r/(r+1), & \text{if } r < 2 \\ 1 - 1/(r+1), & \text{if } r \geq 2 \end{cases} \quad l_5 = \begin{cases} 1 - 1/(r+1), & \text{if } r < 2 \\ 1 - 1/2 \cdot r/(r+1), & \text{if } r \geq 2 \end{cases} \\ &l_6 = 1 \end{aligned} \tag{4}$$

Fig. 2 shows that drive under analysis has four inner voltage levels, which are produced differently for $r < 2$ and $r \geq 2$. Clearly, for $r = 1$, l_3 and l_4 are equal, while $r = 2$ results in $l_2 = l_3$ and $l_4 = l_5$. Although carrier signals are time dependent variables, their amplitudes are determined with r. In order to visualise influence of dc-link voltage ratio on carriers' distribution, they are represented with triangular signals in the background. One may conclude that $r = 1$, 2 and 4 result in configurations that operate with equidistant voltage levels. With $r = 1$, the drive can be operated as a five-level single-sided VSI. Since VSI_1 has two and VSI_2 one complementary pair of IGBTs, transitions between certain phase voltage levels are clearly based on simultaneous switching of the inverters. This leads to the presence of so-called dead-time spikes, as shown in [24, 25]. With $r = 2$, the drive topology is capable of producing only four voltage levels, since four out of eight combinations in Table 1 are feasible. The overall dc-link voltage of $V_{dc} = 600$ V results in $V_{dc1} = 400$ V and $V_{dc2} = 200$ V and voltage levels of –200 V, 0 V, 200 V and 400 V. While both $1 < r < 2$ and $r > 2$ result in a six-level configuration, comparison of the two cases shows that two VSIs operate differently, due to differences in formation of the $l_{2..4}$ voltage levels. The voltage levels are not equidistant for any dc-link voltage ratio in $1 < r < 2$ range, which leads to a worse harmonic performance.

For $r > 2$, transitions between l_3 and l_4 involve only switching of one VSI, while transitions between l_2 and l_3 and l_4 and l_5 can be only performed using simultaneous switching of two inverters. This means that dead-time spikes will occur less frequently than in the case of $1 < r < 2$, while NPC converter never operates in rail-to-rail switching mode.

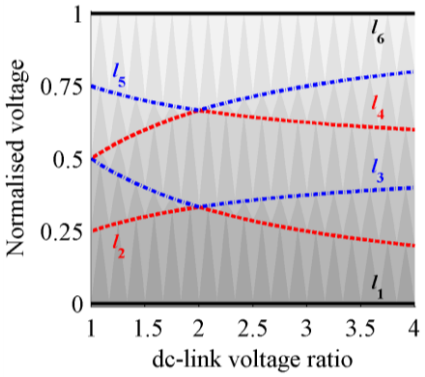

Fig. 2. *Equivalent phase voltage levels against dc-link voltage ratio.*

Only $r = 4$ results in equidistant voltage levels. As known from previous research [26], this ensures the lowest harmonic distortion, due to more uniform distribution of phase voltage space vectors in two planes. This short analysis of dc-link voltage ratio influence on available voltage levels, presence of dead-time spikes and expected drive behaviour narrows down the number of configurations, i.e. different values of r, for further consideration. Hence, only $r = 2$ and $r = 4$ are analysed in this paper.

3 Modulation methods

OeW drives can be modulated in such a way that inverters are controlled either as a single entity or individually. The former is referred to as coupled control and it relies on already known modulation strategies for single-sided multilevel inverters, applied to OeW drives after slight modifications [23-26]. The latter approach considers the inverters as separate entities that are modulated independently, using two phase voltage reference sets, formed by splitting the original sinusoidal phase voltage reference. This concept, referred to as decoupled inverter modulation [17, 18], leads to somewhat simpler inverter control, when compared to the coupled modulation methods, but also to reduced harmonic quality of produced waveforms.

As known from the literature, modulation strategies for dual inverter systems can be developed in several ways. Comparison of CB and SV PWM methods shows that CB PWM can achieve the same level of performance as the SV PWM methods, i.e. the maximum modulation index in the linear region of $1/\cos(\pi/10) = 1.051$ in the case of a five-phase machine [27]. This can be achieved by adding the zero-sequence injection to the sinusoidal phase voltage reference, calculated as:

$$v_{inj} = -1/2 \cdot (v_{min} + v_{max}) \tag{5}$$

where v_{max} and v_{min} stand for the maximum and minimum value, respectively, of the normalised phase voltage references. The final phase voltage references are generated using the following expression:

$$v_k^*(t) = \frac{1}{2} + \frac{M}{2} \cdot \sin(M \cdot 2 \cdot \pi \cdot f_n \cdot t - 2 \cdot \pi / 5 \cdot (k+1)) + v_{inj} \tag{6}$$

where modulation index M is defined as a ratio between the reference amplitude and $V_{dc}/2$. Equation (6) provides phase voltage references for $V/f = const.$ control, since sine wave amplitude is normalised with M, as is the angular frequency

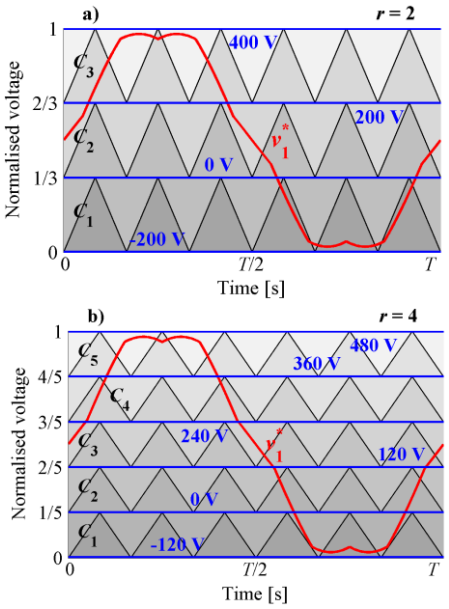

Fig. 3. *Phase voltage reference with min-max injection and carrier signals for PD PWM for: r = 2 (a), r = 4 (b).*

as well (f_n stands for the nominal machine frequency). Angular phase shift is $2\cdot\pi/5\cdot(k-1)$ for the k^{th} drive phase.

Using data from Table 1 one is able to obtain the exact values of available voltage levels for different values of r, which actually define reference zones as depicted in Fig. 3, for $r = 2$ and 4 for carriers with in-phase disposition (PD). Other carrier arrangements result in worse harmonic performance [27], and therefore are not in the focus of this paper. Phase voltage reference v_i^* is given in red, for modulation index $M = 1$, defined as a ratio between the v_i^* amplitude and $V_{dc}/2$.

Since each of the VSIs has lower number of levels than OeW drive when considered as a coupled entity, some additional calculations are required. Depending on r, a different set of equations has to be applied, in order to generate the final gating signals. This approach is explained in detail in [23, 26, 28].

Firstly, v_i^* is compared with carrier signals C_k, in order to obtain logical variables A_{ki} which are equal to 1 if $v_i^* > C_k$ and otherwise 0. Relations that connect A_{ki} with S_{jk} are obtained from the analysis of data given in Table 2 and expected drive behaviour when v_i^* is in between certain carriers (areas denoted with shades of grey in Fig. 2). Using state machine analysis methods and other rules explained in detail in [23, 26, 28], final expressions are given in Table 2. Clearly when $r = 2$ the inverters never operate in PWM mode at the same time, meaning the simultaneous switching and dead-time spikes do not exist in this drive configuration. Also, PWM operation between 0 and $-V_{dc1}/2$, and between $V_{dc1}/2$ and V_{dc2} is symmetrical, due to symmetry that comes from expressions for S^a_{1k} and S^b_{1k}. This ensures the natural balancing of dc-link voltages on VSI_1 side. When $r = 4$ Table 2 shows that A_{2k} and A_{4k} appear in more than one expression, which confirms that simultaneous switching of VSI_1 and VSI_2 exists. Hence, a modification proposed in [24, 26] should be applied in reference zones 2 and 4 in order to eliminate dead-time spikes from phase voltage waveforms.

Next, the decoupled modulating algorithms developed in [18] for a drive comprising two two-level VSIs are modified and applied to the analysed OeW topology. In this case, phase voltage reference is obtained using (6) with dc offset of 1/2. Modulation indices for two inverters are calculated as:

$$M_1 = \begin{cases} 0 & \text{if} \quad 0 \le M \le M_{max}/(r+1) \\ (r+1)\cdot\left(M - M_{max}/(r+1)\right) & \text{if} \quad M_{max}/(r+1) \le M \le M_{max} \end{cases}$$

$$M_2 = \begin{cases} (r+1)\cdot M & \text{if} \quad 0 \le M \le M_{max}/(r+1) \\ M_{max} & \text{if} \quad M_{max}/(r+1) \le M \le M_{max} \end{cases} \tag{7}$$

where $M_{max} = 1.05$ represents maximal modulation index value. Using M_1 and M_2, one is able to perform the unequal reference sharing as in [18] and to produce voltage references for VSI_1 and VSI_2:

$$v^*_{1k}(t) = \frac{1}{2} + (M_1/M)\frac{1}{2}v^*_k(t)$$
$$v^*_{2k}(t) = \frac{1}{2} - (M_2/M)\frac{1}{2}v^*_k(t) \tag{8}$$

Equations (7) and (8) can be applied for any r. From that point of view, these, so-called unequal reference sharing (URS) algorithms, are simpler than any coupled inverter control. In general, only VSI_2 operates in PWM mode for modulation indices up to $M_{max}/(r+1)$. Multilevel operation will take place over a wider range of M for higher values of r. Similarly to strategies presented in [18], two decoupled modulation strategies can be produced, based on phase disposition of VSI_1 and VSI_2 carrier signals. These are refered to in [18] and [21] as URS1 and URS2. However, this has no infuence on dc-link capacitor voltage stability, only on harmonic performance. Hence, only term URS will be furher used in this paper. Formation of the VSI references is depicted in Fig. 4, for all carriers with in-phase disposition. More details can be found in [18] and [21].

4 DC-link capacitor stability issues

Efforts to analyse dc-link capacitor voltage balancing in OeW drives are reported in [17, 29, 30]. All of them can be classified as a voltage-based dc-link capacitor voltage

Table 2. Expressions for switching state generation in the case of 3L-OeW-2L drive.

dc-link voltage ratio	number of levels	VSI_1	VSI_2
$r = 1$	5	$S^a_{1k} = A_{4k}, S^b_{1k} = A_{3k} + \overline{A}_{2k}\cdot A_{1k}$	$S_{2k} = \overline{A}_{2k}$
$1 < r < 2$	6	$S^a_{1k} = A_{5k}\cdot\overline{A}_{4k}\cdot A_{3k}, S^b_{1k} = A_{3k}\cdot\overline{A}_{2k}\cdot A_{1k}$	$S_{2k} = \overline{A}_{4k}\cdot A_{3k}\cdot\overline{A}_{2k}$
$r = 2$	4	$S^a_{1k} = A_{3k}, S^b_{1k} = A_{1k}$	$S_{2k} = \overline{A}_{2k}$
$r > 2$	6	$S^a_{1k} = A_{4k}, S^b_{1k} = A_{2k}$	$S_{2k} = \overline{A}_{5k}\cdot A_{4k}\cdot\overline{A}_{3k}\cdot A_{2k}\cdot A_{1k}$

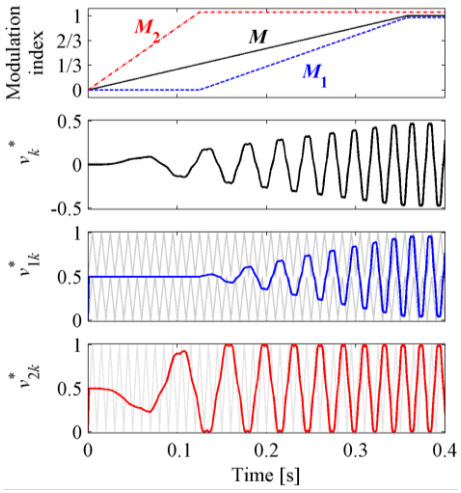

Fig. 4. *Formation of the VSI voltage references in the case of decoupled control: V/f acceleration, r = 2 and the final M value equal to 1.*

analysis, since they rely on the Kirchhoff's voltage law and investigation of the space vector application time impact on the dc-link capacitor voltage levels.

However, they can be applied only in special cases, for which proposed control algorithms are developed. Namely, some parameters, such as the number of voltage levels, number of drive phases and dc-link voltage ratio define the phase voltage space vector distribution, while their influence on the dc-link capacitor voltages is defined under the assumption that current flow in all drive phases is always the same when a specific vector is applied. This last condition drastically limits the number of cases in which voltage-based analysis can be used, since phase angle between stator phase voltage and stator phase current is a variable load-dependent parameter. Consequently, a novel approach using only Kirchhoff's current law, introduced in [18, 25], is used for the studied topology. Firstly, impact of drive and modulation strategy parameters on dc-link capacitor voltages is analysed using a simplified and then linearized drive model, which does not include pulse width modulation and relies on a sinusoidal approximation, i.e. the harmonic content of all ac signals in the circuitry is neglected. Using labels from Fig. 1, the dc-link model based on Kirchhoff's current law is formed:

$$\begin{aligned} i_{cdc11}(t) &= i_{dc1}(t) - i_{dclink1}(t) \\ i_{cdc12}(t) &= i_{dc1}(t) - i_{dclink1}(t) - i_{mp}(t) \\ i_{cdc2}(t) &= i_{dc2}(t) - i_{dclink2}(t) \end{aligned} \tag{9}$$

where i_{mp} stands for the current sourced from the mid-point of the NPC inverter dc side. This current, as well as $i_{dclink1}$, $i_{dclink2}$, can have both positive and negative mean value over one fundamental period, which affects dc-link capacitors' voltage balancing on the VSI_1 side. Expressions for dc-link capacitors voltages, based on Fig. 1 are:

$$\begin{aligned} v_{cdc11}(t_2) &= \frac{1}{C_{dc11}} \int_{t1}^{t2} \left(i_{dc1}(t) - i_{dclink1}(t)\right) \cdot \mathrm{d}t + v_{cdc11}(t_1) \\ v_{cdc12}(t_2) &= \frac{1}{C_{dc21}} \int_{t1}^{t2} \left(i_{dc1}(t) - i_{dclink1}(t) - i_{mp}(t)\right) \cdot \mathrm{d}t + v_{cdc11}(t_1) \\ v_{cdc2}(t_2) &= \frac{1}{C_{dc2}} \int_{t1}^{t2} \left(i_{dc2}(t) - i_{dclink2}(t)\right) \cdot \mathrm{d}t + v_{cdc2}(t_1) \end{aligned} \tag{10}$$

Analysis of Fig. 1 and (9) reveals the conditions under which all dc-link capacitor voltages are in balance. Due to current unidirectional nature of dc-link formation circuit, currents i_{dc1} and i_{dc2} are always positive or zero, which means that a constraint for power sourcing from the dc to ac side of application is that $i_{dclink1}$ and $i_{dclink2}$ have positive mean values over one fundamental period. This ensures stable dc-link capacitor voltage on VSI_2 side, determined by the rest of the dc source circuitry.

The situation is more complex on the VSI_1 side. This inverter is aimed to operate with three equidistant voltage levels (V_{dc1}, $v_{mp} = V_{dc1}/2$ and $v_{n1} = 0$), while switching is only allowed between adjacent levels, i.e. there should be no switching from V_{dc1} to v_{n1} and vice versa. The desired dc-link voltage levels on VSI_1 side mean that the expected capacitor voltages are $v_{cdc11} = v_{cdc12} = V_{dc1}/2$. In this case, it is not sufficient to have positive $i_{dclink1}$ and $i_{dclink2}$, in order to ensure stable dc-link voltages. In addition, the i_{mp} mean value has to be zero over one fundamental period in order for v_{cdc11} and v_{cdc12} to be equal. In other words, in order to understand the dc-link capacitor voltage balancing, it is sufficient to analyse $i_{dclink1}$, i_{mp} and $i_{dclink2}$.

Relations between switching states and phase currents, with dc-link currents, obtained using analysis of different modulation strategies and labels from Fig. 1, are:

$$\begin{aligned} i_{dclink1}(t) &= \sum_{k=1}^{5} \left(S_{1k}^{a}(t) \cdot S_{2k}^{b}(t) \cdot i_k(t)\right) \\ i_{mp}(t) &= \sum_{k=1}^{5} \left(\overline{S}_{1k}^{a}(t) \cdot S_{2k}^{b}(t) \cdot i_k(t)\right) \\ i_{dclink2}(t) &= \sum_{k=1}^{5} \left(S_{2k}(t) \cdot i_k(t)\right) \end{aligned} \tag{11}$$

where the bar over the logical variable represents logical negation operation. Analysis of switching patterns shows that S_{1k}^{q} and S_{1k}^{h} are never in PWM mode at the same time, at least in the case of modulation strategies presented in this paper.

Linearized drive model, based on the sinusoidal phase current approximation, is shown in Fig. 5a. An equivalent circuit, based on ideal transformers and (11) is shown in Fig. 5b. Expressions for dc-link current contributions from one drive phase are:

$$\begin{aligned} i_{dclink1k}(t) &= d_{1k}^{a}(t) \cdot i_k(t) \\ i_{mpk}(t) &= d_{mpk}(t) \cdot i_k(t) \\ i_{dclink2k}(t) &= -d_{2k}(t) \cdot i_k(t) \end{aligned} \tag{12}$$

where $d_{mpk}(t)$ stands for VSI_1 mid-point duty ratio, which is calculated as:

$$d_{mpk}(t) = \begin{cases} 1 - d_{1k}^{a}(t) & \text{if} \quad 1 - d_{1k}^{a}(t) < d_{1k}^{b}(t) \\ d_{1k}^{b}(t) & \text{if} \quad 1 - d_{1k}^{a}(t) \geq d_{1k}^{b}(t) \end{cases} \tag{13}$$

In (12) and (13) d_{1k}^{a} and d_{1k}^{b} duty ratios correspond to S_{1k}^{a} and S_{1k}^{b} switching states, respectively. These two expressions form the complete drive model, which can be applied to any configuration (i.e. r value) and any modulation strategy. The only difference comes from the fact that duty ratios are calculated in a different manner. Phase current is in all these cases calculated as:

$$i_k(t) = I_m \cdot \sin(\omega_m \cdot t - (k-1) \cdot 2 \cdot \pi/5 - \phi) \tag{14}$$

while (6) provides the overall phase voltage reference,

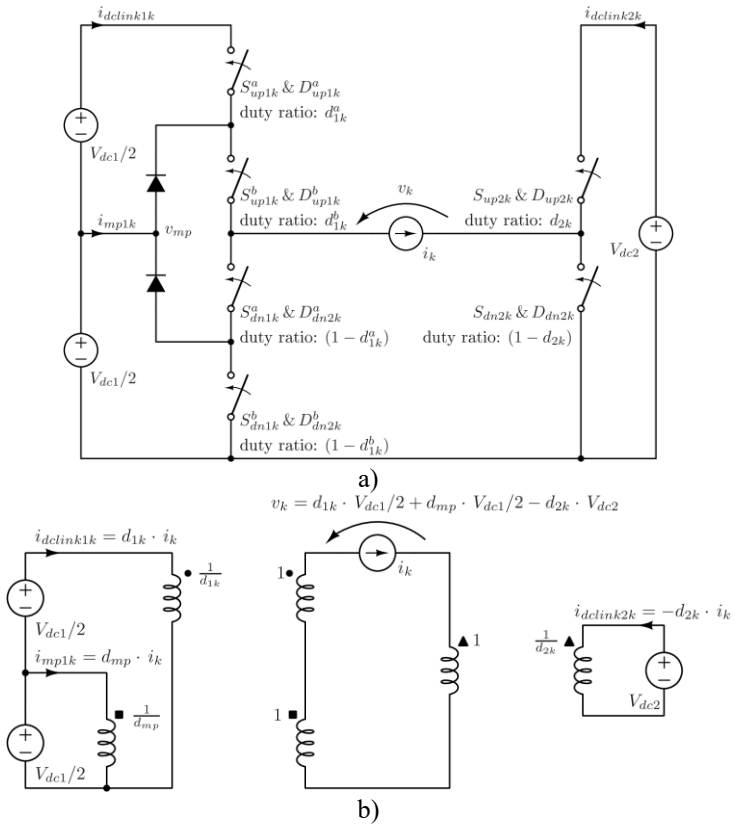

Fig. 5. *Equivalent model of topology under the sinusoidal approximation (a) (for simplicity, only the k[th] drive phase is shown). Linearized equivalent model of topology under the sinusoidal approximation (b).*

regardless of the drive configuration and modulation strategy. For simplicity reasons, analysis is performed for the phase voltage reference without min-max injection, i.e. $v_{inj} = 0$ in (6).

In the case of $r = 2$, duty ratios are calculated using simpler expressions. All three complementary pairs of switches (S^a_{1k}, S^b_{1k} and S_{2k}) are equally and symmetrically used during one fundamental period (in multilevel operation). Normalised voltage levels are $l_1 = 0$, $l_2 = 1/3$, $l_3 = 2/3$ and $l_4 = 1$. Duty ratio expressions, based on Table 2 under the assumption of infinite switching frequency, are summarised in Table 3. Duty ratio expressions for decoupled modulation are given in Table 4 [28]. Those can be used regardless of dc-link voltage ratio, which only has an influence on the border between two-level and multilevel PWM operation.

Based on the model in Fig. 5b, mean values of dc-link currents are calculated for the complete range of ϕ. Results are shown in Fig. 6, for three different modulation index values, for which multilevel PWM operation takes place. Line over the symbol in Fig. 6 represents the mean value in steady state conditions, over one fundamental period. Current i_{mp} has a mean value equal to zero with both modulation methods, while all other dc-link currents have always positive mean values. This means that all dc-link voltages are naturally balanced, which makes the four-level configuration ($r = 2$) suitable for variable speed drives.

With $r = 4$, the drive is able to produce six equidistant voltage levels, with normalised values $l_1 = 0$, $l_2 = 1/5$, $l_3 = 2/5$, $l_4 = 3/5$, $l_5 = 4/5$ and $l_6 = 1$. In this case, VSI_2 is employed in every reference zone (Fig. 3.). VSI_1 performs low-side PWM switching in the reference zone 2 and high-side PWM in reference zone 4. It can be seen in Table 1 that the transitions between $l_2 - l_3$ and $l_4 - l_5$ can only be performed with simultaneous switching on both OeW sides. Similarly to four-level OeW drive presented in [24, 26], this kind of modulation causes not only dead-time spikes, but also capacitor voltage balancing problem at the lower dc-link voltage side [20]. Duty ratios for coupled modulation methods with $r = 4$ are listed in Table 5. In the case of decoupled control, expressions for duty ratios are identical to those in Table 5. Using (12) and the model in Fig. 5b, contributions of each drive phase to the overall dc-link currents are obtained. Fig. 6(c-d) shows the dc-link current mean values for coupled and decoupled modulation when $r = 4$.

Due to symmetrical operation of the low- and high-sides of VSI_1, i_{mpk} negative and positive parts are symmetrical, regardless of M and ϕ. Operation of VSI_1 high-side also ensures that $i_{dclink1k}$ always has a positive mean value. Situation on the VSI_2 side is more complex, since this inverter operates in all reference zones in PWM mode. For some M values, this leads to an overcharging, which can be seen from the $i_{dclink21}$ waveform in Fig. 6c, for $M = 0.6$ and 0.8. In this case, the lower M value for which $i_{dclink2}$ becomes negative is not equal to the border between single-sided and multilevel operation (i.e. $M = 0.2$). Numerical analysis shows that this phenomenon takes place for $0.495 < M < 0.901$, regardless of the phase angle. This means that for the $r = 4$ configuration, when coupled PWM is used the dc-link voltage of VSI_2 will rise when $0.495 < M < 0.901$. The rate of the dc-link voltage rise will depend on the phase angle as shown in Fig. 6c and hence on the parameters and loading for the machine. This

Table 3. Duty ratio calculations for the four-level configuration and coupled PWM methods.

Condition	d_{1k}^{a}	d_{1k}^{b}	d_{2k}
$l_1 \le v_k^*(t) \le l_2$	0	$3\cdot(v_k^*(t) - l_1)$	1
$l_2 < v_k^*(t) \le l_3$	0	1	$3\cdot(l_2 - (v_k^*(t))$
$l_3 < v_k^*(t) \le l_4$	$3\cdot(v_k^*(t) - l_3)$	1	0

Table 4. Duty ratio calculations for the four-level configuration for decoupled PWM methods.

Condition	d_{1k}^{a}	d_{1k}^{b}	d_{2k}
$0 \le v_k^*(t) \le 1/2$	$2\cdot(v_{1k}^*(t) - 1/2)$	1	$v_{2k}^*(t)$
$1/2 < v_k^*(t) \le 1$	0	$2\cdot v_{1k}^*(t)$	$v_{2k}^*(t)$

Table 5. Duty ratio calculations for the six-level configuration and coupled and decoupled PWM methods.

Condition	d_{1k}^{a}	d_{1k}^{b}	d_{2k}
$l_1 \le v_k^*(t) \le l_2$	0	0	$5\cdot(1 - v_k^*(t))$
$l_2 < v_k^*(t) \le l_3$	0	$5\cdot(v_k^*(t) - l_2)$	$5\cdot(v_k^*(t) - l_2)$
$l_3 < v_k^*(t) \le l_4$	0	1	$5\cdot(l_4 - v_k^*(t))$
$l_4 < v_k^*(t) \le l_5$	$5\cdot(v_k^*(t) - l_4)$	1	$5\cdot(v_k^*(t) - l_4)$
$l_5 < v_k^*(t) \le l_6$	1	1	$5\cdot(l_6 - v_k^*(t))$

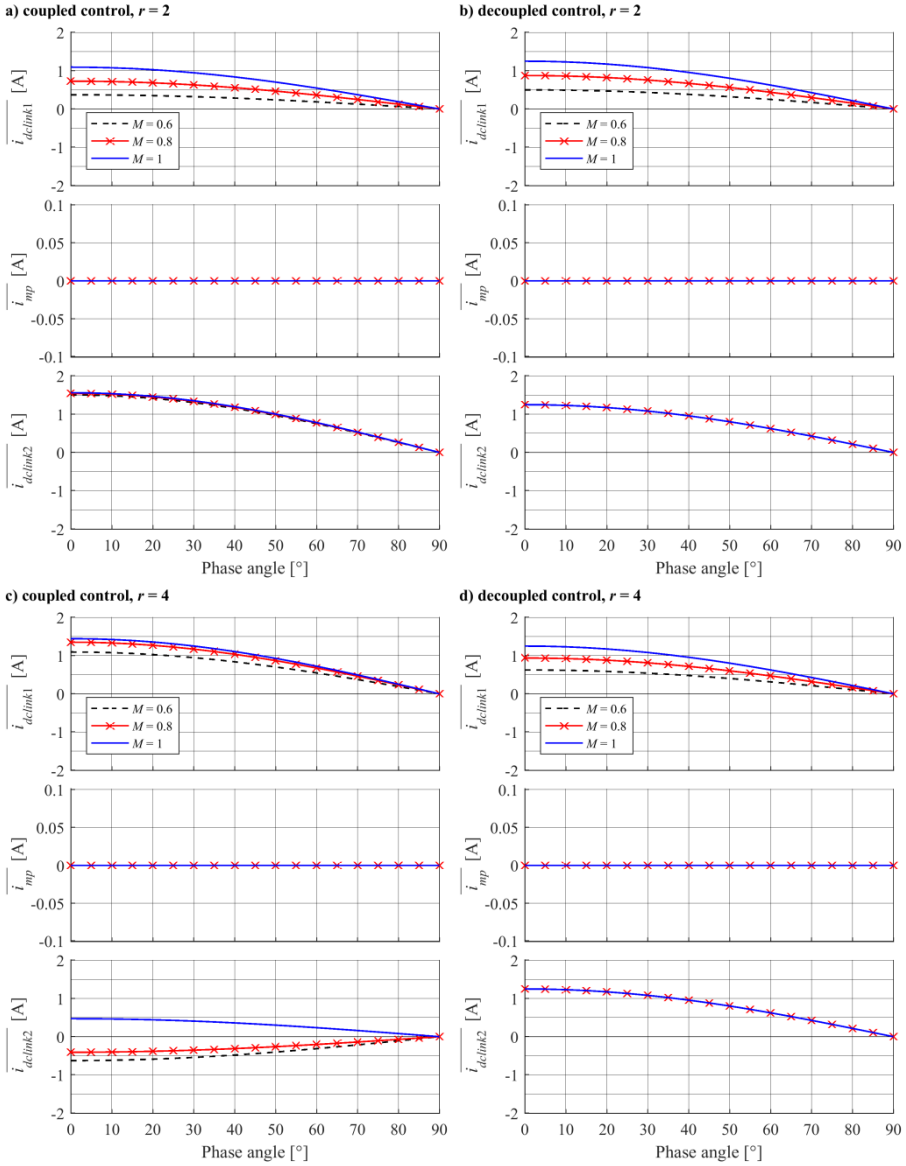

Fig. 6. *Phase angle influence on the dc-link current mean values in the case of four-level configuration (r = 2) with coupled (a) and decoupled (b) control and in the case of six-level configuration (r = 4) with coupled (c) and decoupled (d) control.*

can be avoided by switching to the decoupled PWM method during the operating region. This comes at the cost of slightly worse harmonic performance [21].

5 Experimental results

Experimental results are obtained using a custom built five-phase three-level NPC inverter (VSI_1), a custom made two-level inverter (VSI_2) and a four-pole five-phase induction motor. The inverters are supplied from controllable dc power supplies. The motor is controlled using the *V/f = const.* control law with the switching frequencies of both VSIs equal to 2 kHz, while dead-time interval is set to be 6 μs.

Steady-state waveforms, obtained with coupled and decoupled control with $r = 2$ and $r = 4$, are shown in Fig. 7 for nominal speed ($M = 1$). VSI_2 leg voltage v_{21} is shown on oscilloscope channel CH1, VSI_1 leg voltage v_{11} at CH2, machine phase voltage v_1 at CH3, while channel CH4 shows the stator current i_1. Clearly, six-level configuration results in more sinusoidal phase voltages and phase currents regardless of the modulation strategy. This is a direct consequence of finer division of the same overall dc-link voltage range.

In the second set of experiments (Fig. 8) the machine is accelerated from 0 to 1500 rpm in a linear ramped manner over 8 s. This takes the drive through the modulation index range 0 to 1 in order to investigate the performance of the modulation techniques with regard to the dc-link stability. Regarding coupled control, it is clear that $r = 2$ results in optimal energy consumption, while $r = 4$ leads to additional energy losses. In that case, VSI_1 naturally keeps its voltage levels balanced, due to symmetrical low- and high-side PWM operation, but coupled modulation leads to an overcharging on the VSI_2 side. As expected from derived model analysis, the modulation results in negative $i_{dclink2k}$ mean value over one fundamental period, for any phase angle lower than 90°. Experimental results for decoupled PWM methods show that drive operates with naturally balanced dc-link voltages for both values of *r*. Although the modulation index range in which the drive with $r = 4$ suffers from overcharging problem is somewhat smaller, as well as the overcharging rate, when compared to the results in [26], it is clear that this represents a significant drawback.

On the other hand, it is clear that this drive configuration with coupled control has the best harmonic performance, compared to decoupled PWM. From that point of view, it seems that configuration with $r = 4$ may have great practical significance for high-power applications in which the

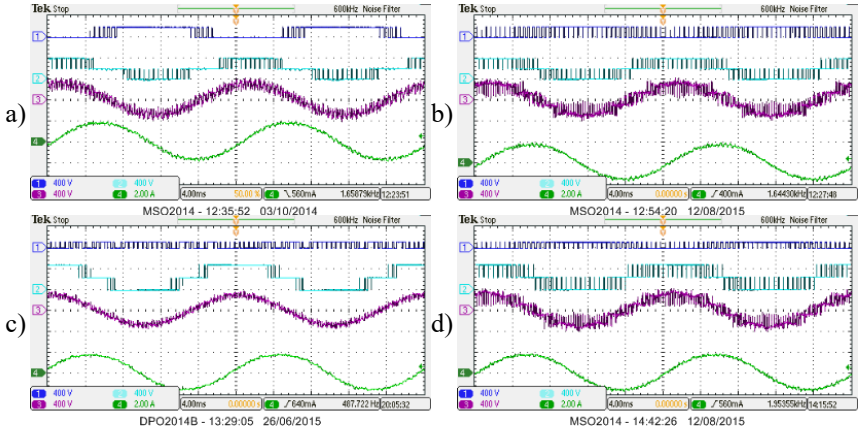

Fig. 7. *Experimental results: waveforms for r = 2 and M = 1, with PD PWM (a) and URS PWM (b); for r = 4 and M = 1, with PD PWM (c) and URS PWM (d).*

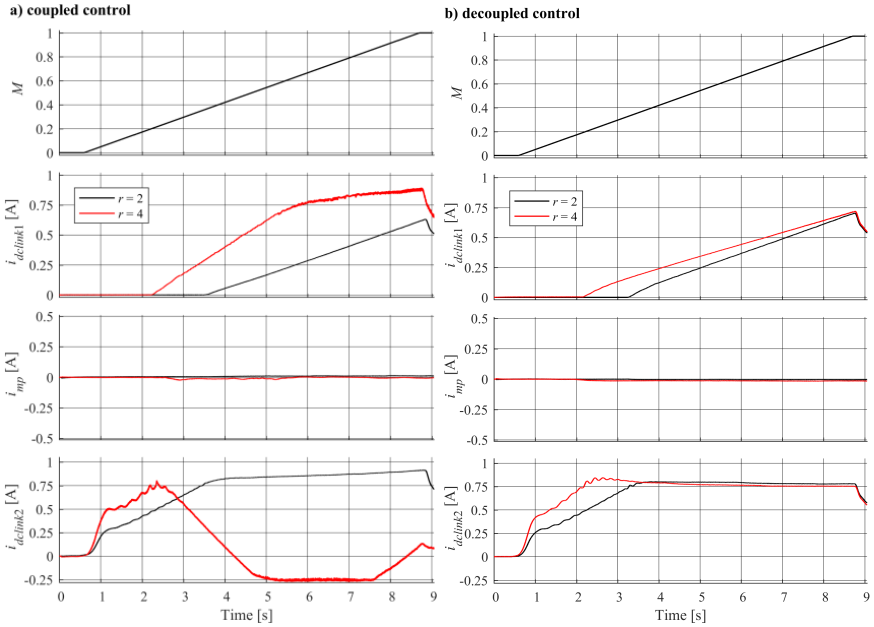

Fig. 8. *Experimental results: dc-link currents and total drive power during V/f=const. acceleration, for coupled (a) and decoupled (b) control, with r = 2 and r = 4.*

machine is aimed to operate with constant speed most of the time. Regarding variable speed drives, this configuration can be utilised only if application demands allow combination of modulation strategies during speed variation [21]. According to the harmonic performance, available in [21], it appears that PD PWM should be replaced with URS in the modulation index range in which overcharging phenomenon takes place.

6 Conclusion

A novel multilevel five-phase open-end winding drive is analysed in this paper. The drive consists of a five-phase induction machine with open-end windings, supplied from two voltage source inverters, with isolated dc-links. The inverter with the higher dc-link voltage is a three-level neutral-point clamped VSI. The other side of the machine windings is supplied from a two-level VSI. It is shown that this drive configuration can operate as a four-, five- or six-level single sided five-phase drive. The number of equivalent voltage levels depends on the ratio between dc-link voltages that are used to supply the two inverters. Four- and six-level drive configurations are chosen for further analysis. For these two cases, two different modulation strategies are discussed. It is shown that coupled modulation strategies offer better harmonic performance, when compared to decoupled counterparts, which are based on phase voltage reference sharing.

Modulation strategy influence on dc-link voltage stability is analysed as well. The results show that the lower dc-link voltage capacitor can be overcharged when optimal modulation strategy is applied to the six-level configuration. This conclusion is based on the novel approach of dc-link modelling and is later experimentally confirmed. It is also shown that, in all other cases, all dc-link voltage levels are stable for any commanded speed (modulation index value) and phase angle between phase voltage and phase current.

Since overcharging phenomenon is only present in small range of modulation index values, the benefits offered by high harmonic performance quality of this drive configuration can be exploited in applications where frequent speed variation is not expected. In those cases, low harmonic distortion of phase voltages and currents may lead to the higher efficiency and easier fulfilment of industrial standards for electromagnetic interference and acoustic noise. Other presented cases result in stable dc-link voltages, which makes them more suitable for variable speed drives and automotive applications.

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