Design and Scaling of Lateral Super-Junction Multi-Gate MOSFET by 3-D TCAD Simulations

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Abstract

A design, optimisation, and scaling of a complementary metal-oxide-semiconductor CMOS-compatible lateral super-junction (SJ) multi-gate (MG) MOSFET (SJ-MGFET) based on silicon-on-insulator (SOI) technology is examined as a preferred solution in mitigating the predominance of channel resistance during operation at a low voltage. In order to overcome the preponderance of the channel resistance, the SJ-MGFET uses a non-planar 3-D embedded trench gate and a folded alternating U-shaped n/p– SJ drift region pillar. The trench gate will redistribute electron current crowding near the top surface of the $n-$ pillar reducing the channel resistance. The folded U-shaped n/p– pillar uniformly distributes the electric field in the SJ drift region.

The variations in the device architecture of a 1 μm gate length lateral super-junction (SJ) multi-gate MOSFET (SJ-MGFET) are explored using the physically based commercial 3-D TCAD device simulations by Silvaco. Investigation and analysis of different carrier transport models are carried out with different doping profiles by calibrating the drift-diffusion simulations to experimental I-V characteristics and breakdown voltage of the SJ-MGFET. The study, then aimed to improve drive current, breakdown voltage (BV), and specific on-resistance ($R_{on,sp}$). The effect of charge imbalance in the SJ pillar unit on the device breakdown voltage is studied with variations in the drift region length. It is observed that the charge imbalance in the SJ unit barely changes due to the fixed ratio between the pillar width and the pillar height.

It has been reported that the simulated and optimised SJ-MGFET device achieves 41% increase in the drive current with an on-off ratio of 5×10^6 at a drain voltage of 10 V and a gate voltage of 20 V, thereby demonstrating a big advantage of the multi-gate device design to reduce the leakage current. The results have shown that the optimised 1 μm gate length SJ-MGFET device offers a specific on-resistance of 0.21 $m\Omega.\text{cm}^2$ and a breakdown voltage of 65 V with a trench-gate depth of 2.7 μm, a pillar height of 3.6 μm and a drift region length of 3.5 μm. In addition, it achieves 68%, 52% and 15% reduction in the specific on-resistance compared to the reported fabricated SJ-LDMOSFET, fabricated SJ-FinFET and simulated SJ-FinFET at the same BV rating, thereby capable of offering a better performance in terms of a high drive current, a maximum breakdown voltage, a minimum specific on-resistance, and excellent FoM for sub - 100 V rating applications.

Furthermore, the potentiality of scaling the device architecture of the optimised SJ-MGFET is examined from the 1 μm gate length to 0.5 μm, and 0.25 μm, respectively. Different scaling approaches is carefully explored in all dimensions of the 3-D device structure in the simulations. The scaling down of the 1.0 μm gate length SJ-MGFET structure laterally (along the y-axis) by scaling the channel length, the gate length, the gate oxide thickness, and the SJ drift unit length by a factor S to shrink the gate length of 1.0 μm to 0.5 μm and 0.25 μm is examined in the simulations in this thesis. In order to prevent a weak electrostatic integrity in the scaled 0.5 μm and 0.25 μm gate lengths (L_{gate}) SJ-MGFETs, the doping profile is optimised aiming at achieving a maximum drive current, a minimum leakage current, a high switching capability, a low specific on-resistance, and an improve avalanche capabilities of the devices. The scaled and optimised SJ-MGFETs with a gate length of 0.5 μm and 0.25 μm achieve 30% and 63% increase in the drive current in comparison with the 1.0 μm gate length SJ-MGFET at a drain voltage of 0.1 V and a gate voltage of 15 V. Additionally, the

scaled SJ-MGFETs offer a transconductance (g_m) of 20 mS/mm and 56 mS/mm at a drain voltage of 0.1 V with a gate length of 0.5 μm and 0.25 μm, respectively. The SJ-MGFETs with a gate length of 0.5 μm and 0.25 μm having a pillar of a width of 0.3 μm and a trench depth of 2.7 μm, achieve a low specific on-resistance ($R_{on,sp}$) of 7.68 $m\Omega.mm^2$ and 2.24 $m\Omega.mm^2$ ($V_{\mathrm{GS}} = 10\ V$) and breakdown voltage (BV) of 48 V and 26 V, respectively.
Finally, the lateral scaling and optimisation of the 1 μm gate length SJ-MGFET to gate lengths of 0.5 μm and 0.25 μm using Silvaco Technology Computer Aided Design (TCAD) simulations has shown that the FoM of the non-planar transistor can be greatly improved in terms of switching speed, drive current, breakdown voltage, specific on-resistance, and physical density for a higher integration in a CMOS architecture.

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List of contributions

Journal publications

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Conference proceedings

O. A. Adenekan, P. Holland, and K. Kalna, "Optimisation of the Breakdown Voltage of a Lateral Super-Junction Multi-Gate Power MOSFET (SJ-MGFET) for Sub - 200 V Applications," *UK Semiconductors,* 12th-13th July, 2017 (Talk) 1 page paper in the Conference proceeding.

O. A. Adenekan, P. Holland, and K. Kalna, "Scaling and Optimisation of a 3-D Lateral Super-Junction Multi-Gate Power MOSFET (SJ-MGFET) for sub - 100 V Applications," *UK Semiconductors,* 4th-5th July, 2018 (Talk) 1 page paper in the Conference proceeding.

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O. A. Adenekan, P. Holland, and K. Kalna, "Optimisation of Breakdown Voltage of a Lateral Super-Junction Multi-Gate Power MOSFET (SJ-MGFET) for Sub - 200 V Applications," *Zienkeiwicz Centre for Computational Engineering,* 24th-25th January 2018 (Poster).

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Chapter 1

Introduction

1.1 Background

The super-junction (SJ) power MOSFET as one of the most ubiquitous semiconductor devices has been able to overcome the limit set by a bulk unipolar silicon technology. The SJ device overcomes this limit by using alternating heavily doped $n-$ and $p-$ pillars in the drift region thereby achieving a low specific on-resistance [1] with a reduction in gate and output charge for effective switching at any range of frequencies [2]. Additionally, the manufacturing of SJ MOSFETs is less costly compared to wide-band-gap switching devices (SiC or GaN) [3]. The first commercial power MOSFET based on the SJ concept were the CoolMOS [4, 5], and the MDmesh [6] announced by Infineon and STMicroelectronics, respectively. Currently, various architectures with different novelty in design have been proposed in great numbers of publications, and literatures on the SJ devices [7–18]. The SJ power MOSFET market has shown tremendous progress in the last decade due to wide popularity of the MOSFET in various applications such as a power supply, display devices and in renewable energy systems. The SJ global market has reached a benchmark of about U.S. $1 billion value in 2018, with annual growth rate of 10.3 percent per year as shown in the Fig. 1.1 [19]. The high-rise in the market forecast is a result of the technological innovations in fabrication and packaging techniques. Different approaches have been used in a fabrication of the SJ MOSFET: (i) Infineon technology employs multi-epitaxy doping process to creates an island of ions in the epi-layer which diffuses into n-doped pillar layer; (ii) Toshiba and IceMOS Technologies use, and Fairchild Semiconductor used, a deep-trench process that utilises

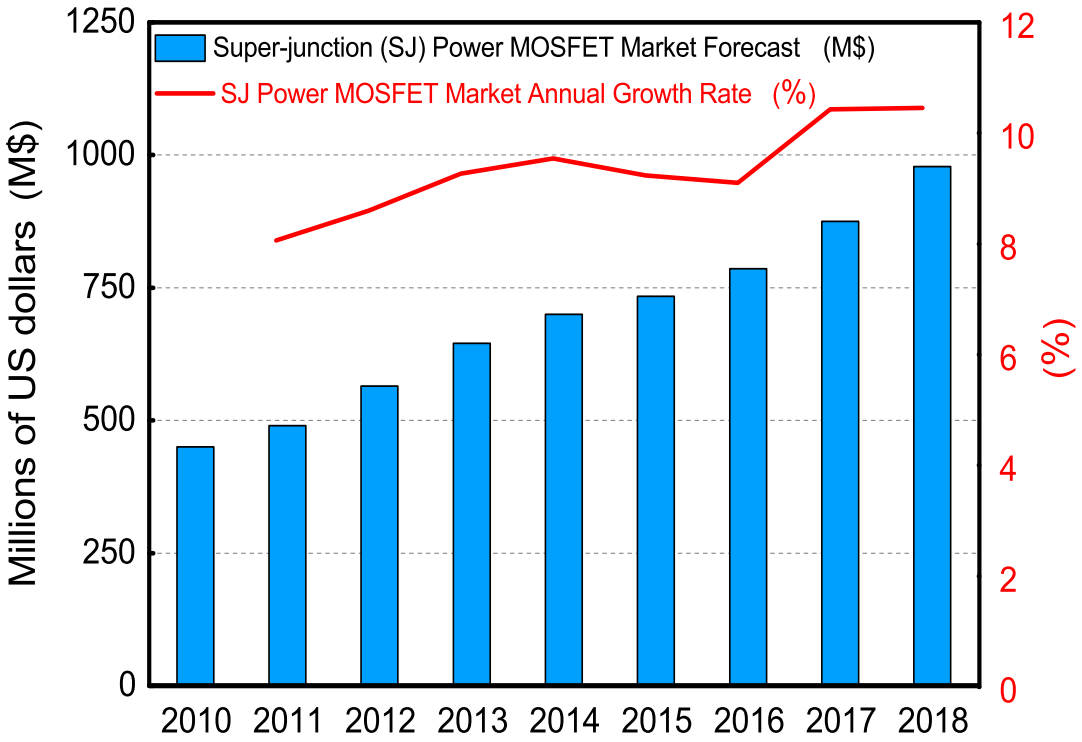

Figure 1.1: Super-junction power MOSFET market forecast (M$) and the annual growth rate from 2010 to 2018.

reactive ion etching of a semiconductor layer, such that the trenches are filled with the n-type doping. The pursuit of achieving a lower specific on-resistance and an improved avalanche capability in a SJ device has led to a great technological competition between multi-epitaxy and deep trench processes. The multi-epitaxy process requires repetitive masking, epitaxy growth, and implantation procedures to realise the p/n columns particularly when the column is long leading to a higher cost and fabrication complexity [20]. In addition, the shifting of the p/n columns during thermal diffusion causes dopant inter-diffusion between the columns to become a non-abrupt transition junction, and thereby lowering the effective impurity concentration, which inevitably affects the trade-off between the breakdown voltage and the specific on-resistance of the structure [21]. The improvement in the SJ MOSFET packaging technologies like power flat and power module is achieving a smaller form factor with a better electrical and thermal performances [22]. This has further increased the demands for the SJ devices in many applications such as renewable energy sources, electric vehicles, and hybrid electric vehicles where space-factor is an hindrance.

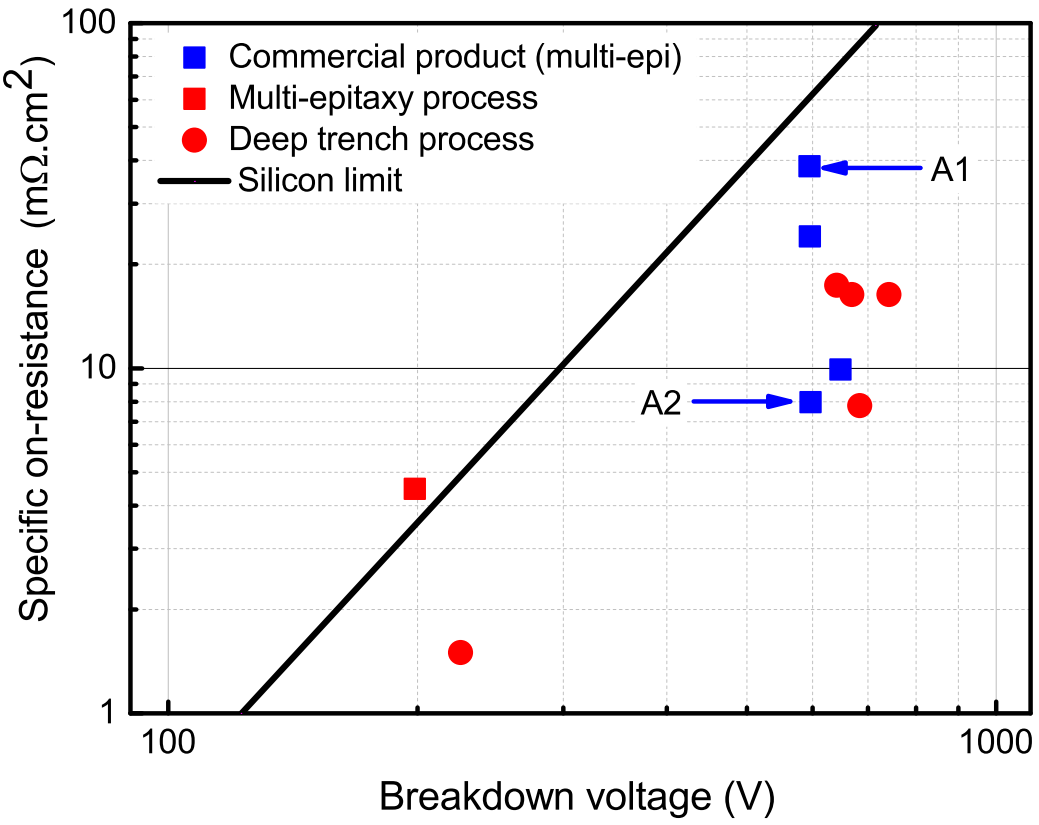

Figure 1.2: The ideal silicon limit against the specific on-resistance of super-junction devices using the multi-epitaxy method, the deep-trench process, and some commercial (CoolMOS) products using multi-epitaxy method including the first generation (CoolMOS) $A1$ and the latest generation (CoolMOS) $A2$.

The ideal silicon limit against the specific on-resistance ($R_{on,sp}$) of SJ devices using the multi-epitaxy process [23], the deep-trench process [12, 24–27] and some commercial multi-epitaxy devices (CoolMOS) manufactured by the Infineon is shown in Fig. 1.2 [28]. Fig. 1.2 also shows that the specific on-resistance has been reduced by approximately 80% from the first generation of CoolMOS ($A1$ with $R_{on,sp}$ of 38.5 $m\Omega.cm^2$) [4] to the latest generation of CoolMOS ($A2$ with $R_{on,sp}$ of 8 $m\Omega.cm^2$) [29]. The SJ device offers a linear relationship between the breakdown voltage and the specific on-resistance [1], thereby enhancing a low on-resistance, an increase in current density and a high breakdown voltage compared to a conventional MOSFET with the same silicon area. The SJ device has also a lower junction capacitances due to the non-linearity of the output and reverse capacitances. As a result of the n/p pillars deplete each other at a given voltage, thereby leading to expansion of the space charge depletion region in the structure.

Therefore, with the capacity of having smaller junction capacitances, the SJ device is more desirable for high switching applications compared to conventional transistors [30]. In addition, the SJ MOSFET is more reliable and more prone to stress in term of the dynamic analysis of the temperature distribution over the metal source surface compared to conventional MOSFETs [31].

1.2 Aim and Objectives

The aim of this work is to design, optimise and scale a lateral SJ multi-gate (MG) MOSFET (SJ-MGFET) for low voltage applications. The work is divided into three main tasks: The first task involves the calibration of the 1 μm gate length SJ-MGFET to experimental characteristics of non-planar lateral SJ multi-gate MOSFET (SJ-MGFET) fabricated within a silicon-on-insulator (SOI) technology [32] by reproducing its transfer (I_{D}-V_{GS}) characteristics and the breakdown voltage (BV) using a drift-diffusion (DD) transport approach in the simulations. The objectives of this study include:

(a) to analyse iteratively different carrier transport models along with different doping profiles using the 3-D Atlas simulations [33, 34];

(b) to demonstrate the dependence of breakdown voltage on charge imbalance in SJ drift region in the device during off-state;

The second task examines the optimisation of the device structure under charge imbalance. Therefore, the objectives of this task include:

(a) to predict improvement in the device performance such as drive current, gate capacitance and conductance;

(b) to study the effects of self-heating and bias dependence in the device structure;

(c) to improve the trade-off between the breakdown voltage (BV) and the specific on-resistance ($R_{on,sp}$) in the device;

The third task involves scaling of the device laterally by a factor of 0.5 and 0.25 aiming to improve the levels of integration in a CMOS architecture. The objectives are as follows:

(a) to scale the optimised SJ-MGFET architecture laterally from 1 μm gate length to 0.5 μm, and 0.25 μm, respectively;

(b) to optimise the scaled devices aiming at improving the physical density, switching speed and drive current;

(c) to explore the possible ways of improving voltage-sustaining capability of the scaled devices;

(c) to improve the trade-off between the breakdown voltage (BV) and the specific on-resistance ($R_{on,sp}$) in the scaled and optimised devices;

1.3 Original Contributions

This work has helped to progress the understanding of the design and the scaling of the lateral SJ multi-gate MOSFET (SJ-MGFET) for low voltage applications. The key contributions are listed below:

(i) 3-D Atlas simulations to investigate variations in the device architecture and improve device performance by optimising doping profile in order to achieve a large on-current density and a low off-current in the device.

(ii) An improvement in figures-of-merit (FoM) between the breakdown voltage (BV) and the specific on-resistance ($R_{on,sp}$) in the optimised SJ-MGFET.

(iii) Scaling of the device design aiming at achieving a high drive current and an increase in the switching capability in the device for a higher level of integration in a CMOS architecture.

(iv) An improvement in figures-of-merit (FoM) between the breakdown voltage and the specific on-resistance in the scaled and optimised SJ-MGFETs.

1.4 Outline

This thesis is organised as follows:
Chapter 2 describes the theory, basic operation of a MOSFET device, and its equivalent circuit. This will be followed by theory of breakdown phenomenon in power devices. A discussion of the state of the art of power semiconductor devices, the

device physics and a review of the current developments in vertical and lateral power semiconductor technologies. In addition, it also discusses the SJ concepts, reported literatures and structures using SJ concepts and their challenges. Finally, it describes the trade-off between the breakdown voltage (BV) and the specific on-resistance ($R_{on,sp}$) in a power device, and the theory of a trench gate power MOSFET.

In Chapter 3, the simulation methodology is presented. This chapter will introduce the physically based commercial TCAD device simulator by Silvaco and related physical models used in this study. A brief review of the numerical techniques for 3-D device simulations will be also presented.

Chapter 4 describes the optimisation of the lateral SJ multi-gate MOSFET (SJ-MGFET) for a high drive current and a low specific on-resistance in sub-100 V applications. The effect of breakdown voltage (BV) on the charge imbalance in the SJ drift region using the 3-D Atlas simulations is investigated here. The chapter also discusses the optimisation of the device performance, study the effect of self-heating and electric field distribution in the device. Finally, it describes the comparison of the specific on-resistance as a function of the breakdown voltage of the optimised SJ-MGFET with reported conventional power devices.

Chapter 5 presents scaling and optimisation of the lateral SJ multi-gate MOSFET for a high drive current and a low specific on-resistance in sub – 50 V applications. It describes the scaling approach and optimisation of the scaled down SJ-MGFETs, on-state and off-state simulations of the scaled devices. It also discusses the gate capacitance extraction, transconductance and gate turn-on transient simulations in the three scaled structures. Conclusively, it presents the trade-off between the specific on-resistance and the breakdown voltage for the simulated SJ-MGFETs scaled down to 0.5 μm and 0.25 μm gate lengths compared with the ideal silicon limit and with various reported conventional LD-MOSFETs.

Finally, in Chapter 6, conclusions are discussed.

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Chapter 2

Fundamentals of Power MOSFETs

2.1 Introduction

The Metal-Oxide-Semiconductor (MOS) field effect transistor plays a dominant factor as the main building block in the development of Integrated-Circuit (IC) Technologies. The MOS field effect transistor (MOSFET) is a basic element in a CMOS technology for digital and analogue circuits which make components of every mobile phone, tablet, and computer and are used in various other digital, power, communication and microwave applications [1]. CMOS technology offers many advantages in a transistor operation which allow a reduction in size, whereby millions of the devices can be fabricated in a single integrated circuit (IC) for higher levels of integration, and smaller resistive effects of a crossover with no need for an isolation in the structure, all thanks to the most advanced fabrication process with cost reduction [2]. A typical MOSFET is a field-effect transistor (FET) with a metal gate electrode placed on the top of a silicon dioxide ($Si0_2$) or dielectric layer, which in turn is on the top of a semiconductor substrate. MOSFET can be fabricated in two configurations namely; the n-channel MOSFET and the p-channel MOSFET, a combination of these two configurations creates a so-called complementary MOS (CMOS) circuit. The CMOS technology offers a high input impedance with dual active outputs, and a low power consumption with a high noise immunity [2]. The applications of CMOS circuits are prefered solutions in modern IC technology, offering a better performance in terms of high packing density, cost effectiveness and low static power consumption to other technology with the same functionality.

2.2 Principles of MOSFET

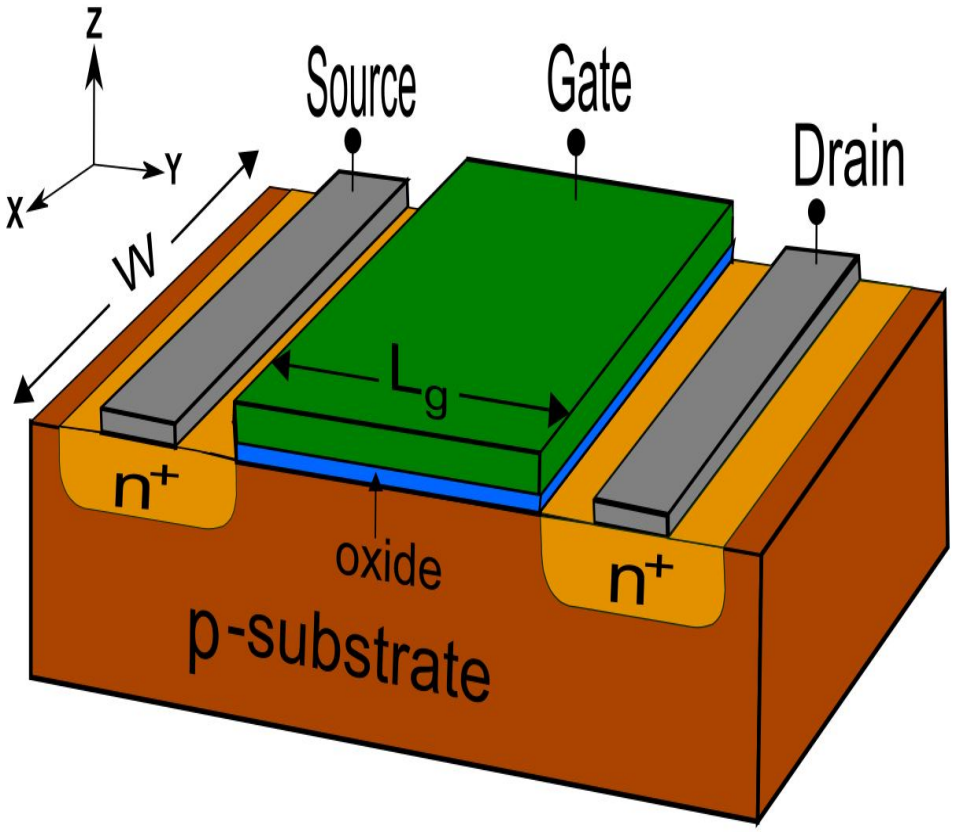

Figure 2.1: Schematic cross section of n-channel MOSFET.

MOSFET is derived from a MOS capacitor in which a gate voltage (V_G) controls the state of a semiconductor surface underneath it, by the creation of either an accumulation or an inversion layer [1–3]. The structure shown in Figure 2.1 [1] is an n-channel MOSFET with a gate length of L_g and a width of W. It also consists of a p-type semiconductor substrate, having two n-type contacts at the ends with a low potential region referred to as the source (n^+) and a high potential region referred to as the drain (n^+), respectively (n^+ and p^+ layers denote heavily doped regions). A thin silicon dioxide ($Si0_2$) layer is deposited on the top surface, followed by a polysilicon material gate formed on a top of $Si0_2$. An electron-rich path can be created referred to as a channel by inverting the semiconductor surface under the gate from p-type to n-type when a positive V_G is applied [4]. In an n-channel MOSFET, a positive V_G larger than the threshold voltage (V_{TH}) is required for the creation of an inversion layer of an electrons in the channel.

For a p-channel MOSFET, a negative V_G greater than the threshold voltage (V_{TH}) is needed for inducing an inversion layer of holes to make a channel. The threshold voltage in a MOSFET is defined as the minimum applied gate voltage needed to make the surface of a substrate under the gate electrode to be strongly inverted. For a power MOSFET, the threshold voltage is normally measured at a drain-source current of 250 μA [5]. The circuit design requirements of safety are much easily fulfilled when a power MOSFET is off when the gate voltage is zero (a device normally-off) because the source and the drain resistances are not negligible and may results in a power dissipation in the device [2]. The V_{TH} can be expressed as [2]:

$$V_{TH} = \Delta V_{ox} + \Delta\phi_s = V_{ox} + \phi_s + \phi_{ms} \tag{2.1}$$

where ϕ_s is the surface potential, ϕ_{ms} is the metal-semiconductor work function difference, and V_{ox} is the potential drop across the oxide.
At a threshold voltage, the surface potential $\phi_s = 2\phi_{fp}$. This expression can be substituted into Equation (2.1) as

$$V_{TH} = V_{oxT} + \phi_{ms} + 2\phi_{fp} \tag{2.2}$$

where V_{oxT} is the voltage across the oxide at the threshold inversion point and ϕ_{fp} is the potential difference between E_{Fi} and E_F (in V) given by:

$$\phi_{fp} = \frac{kT}{q} \ln \frac{N_a}{n_i} \tag{2.3}$$

where k is the Boltzmann's constant, T is the absolute temperature, q is the electronic charge, N_a is the acceptor doping concentration of the substrate, and n_i is the intrinsic carrier concentration of the silicon. The voltage across the oxide at the threshold inversion point can be written as:

$$V_{oxT} = \frac{Q'_{mT}}{C_{ox}} \tag{2.4}$$

where Q'_{mT} is the charge density on the metal gate at threshold and C_{ox} is the gate

oxide capacitance.

$$Q'_{mT} = |Q'_{SD}(max)| - Q'_{ss} \tag{2.5}$$

where Q'_{mT} is the charge density on the metal gate at threshold, $Q'_{SD(max)}$ is the conservation of charge density between the metal and the oxide-semiconductor interface and Q'_{ss} is the charge density adjacent to the oxide-semiconductor interface. The gate oxide capacitance can be expressed as:

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{2.6}$$

ε_{ox} is the dielectric constant of oxide and t_{ox} is the oxide thickness of a gate dielectric layer. Substituting Equations (2.5) and (2.6) into Equation (2.2), the equation can be rewritten as:

$$V_{TH} = \frac{|Q'_{SD}(max)|}{C_{ox}} - \frac{Q'_{ss}}{C_{ox}} + \phi_{ms} + 2\phi_{fp} \tag{2.7}$$

Using Equation (2.7) and assuming a flat-band voltage (V_{FB}), V_{TH} can expressed as

$$V_{TH} = \frac{|Q'_{SD}(max)|}{C_{ox}} + V_{FB} + 2\phi_{fp} \tag{2.8}$$

where

$$V_{FB} = \phi_{ms} - \frac{Q'_{ss}}{C_{ox}} \tag{2.9}$$

$$|Q'_{SD}(max)| = \sqrt{4q\varepsilon_{si}\phi_{fp}N_a} \tag{2.10}$$

In a linear region of a MOSFET operation, the channel resistance (R_{ch}) can be expressed as [1]:

$$R_{ch} = \frac{L_{ch}t_{ox}}{W\mu_n\varepsilon_{ox}(V_{GS} - V_{TH})} \tag{2.11}$$

where L_{ch} is the channel length, t_{ox} is the gate oxide thickness, V_{GS} is the gate voltage, V_{TH} is the threshold voltage, ε_{ox} is the dielectric constant of oxide, μ_n is the average electron mobility in the channel, and W is the channel width.

2.2.1 Equivalent Circuit of an n-channel MOSFET

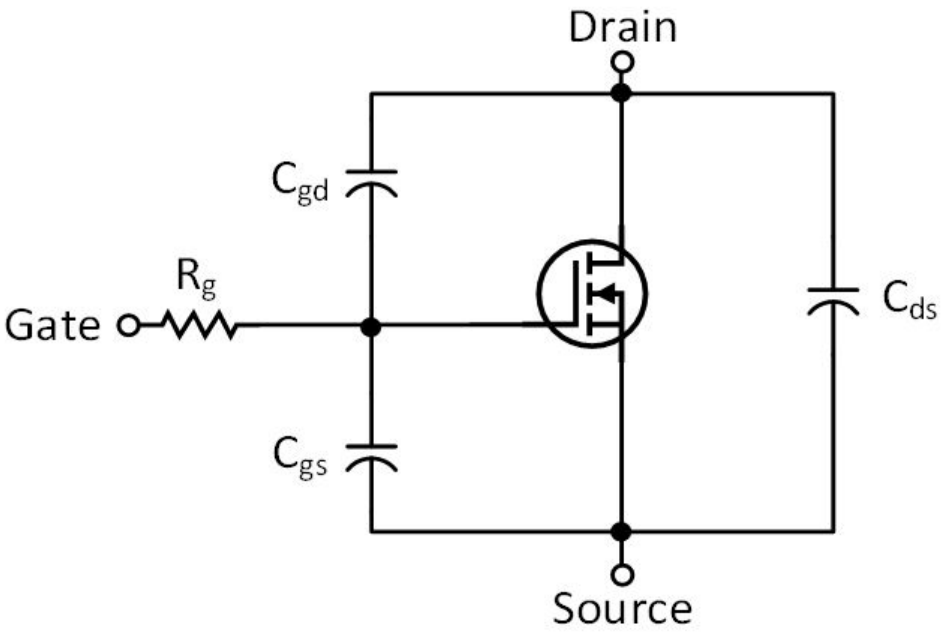

Figure 2.2: Equivalent circuit of n-channel MOSFET and its parasitic capacitances.

A typical MOSFET is a modified MOS capacitor structure with the drain and source insulated from the gate as shown in the Figure 2.2. The gate-source capacitance (C_{gs}), and the gate-drain capacitance (C_{gd}) are determined by the capacitance of the gate oxide thickness, whereas the drain-source capacitance (C_{ds}) is a junction capacitance of the parasitic diode [6]. These capacitances were modified into three parameters that defined MOSFET parasitic capacitances in terms of the input capacitance (C_{iss}), the output capacitance (C_{oss}) and the reverse transfer capacitance (C_{rss}). C_{iss} is the total capacitance of a MOSFET that can be expressed as the sum of C_{gs} and C_{gd}, i.e., (C_{gs} + C_{gd}). This capacitance is charged by a gate charge (Q_g) in order to drive the MOSFET into operation. C_{oss} is expressed as a sum of the C_{ds} and C_{gd}, i.e., C_{ds} + C_{gd}. This output capacitance accounts for the total capacitance on the output side. A small C_{oss} is desirable for timely turn off of the device output. C_{rss} is approximately equal to C_{gd}. This reverse transfer capacitance is also referred to as Miller capacitance because it permits the total dynamic input capacitance to become larger than the sum of static capacitances. In addition, this capacitance is the most important parasitic parameter because it provides a feedback loop between the output and the input of a device [1, 7].

The internal gate resistance (R_g) is a critical parameter that account for the device switching performance, thermal management, and power conversion efficiency. A higher R_g implies a larger device switching and increase in the gate drive losses which leads to increase in the device temperature [8]. A non-linearity of C_{gd} and its dependence on the drain bias limits its choice as a parameter for defining power in MOSFETs. For effective description of a power MOSFET, the standard practice is to extract the gate charge (Q_g) at a constant current source while turning the device from blocking state. This gate charge is specified in data sheets of a particular transistor. Q_g offers advantages of being not dependent on the drain current, the supply voltage, and the device temperature [9]. Additionally, it can be use to estimates the device switching time, the total charge, the energy stored, and the current required to switch the device on for a period of time.

2.3 Theory of Device Breakdown

Improvements in performance of a power device tend to achieve a negligible current flow during the off-state at a high voltage. Capability of a power device to withstand a maximum voltage without a significant rise in the current is limited by the avalanche breakdown of the device, which is strongly dependent on the electric field distribution [7]. In a power device, during the off-state, electron-hole pairs injected into the depletion region will acquire sufficient kinetic energy from longitudinal electric field to create electron-hole pairs by colliding with a lattice atom within the space charge region. The generation of electron-hole pairs, which result from carriers acquiring a high kinetic energy, is referred to as impact ionisation. Generation of the electron-hole pairs by impact ionisation in the depletion region can lead to the creation of more electron-hole pairs. The impact ionisation is a multiplicative process in which device is unable to sustain the application of an elevated voltage due to uncontrolled increase in the current. Thus, the device undergoes avalanche breakdown which limits its maximum operating voltage. In the next sub-sections, the avalanche breakdown as well as the so-called punch-through breakdown are briefly reviewed.

2.3.1 Avalanche Breakdown

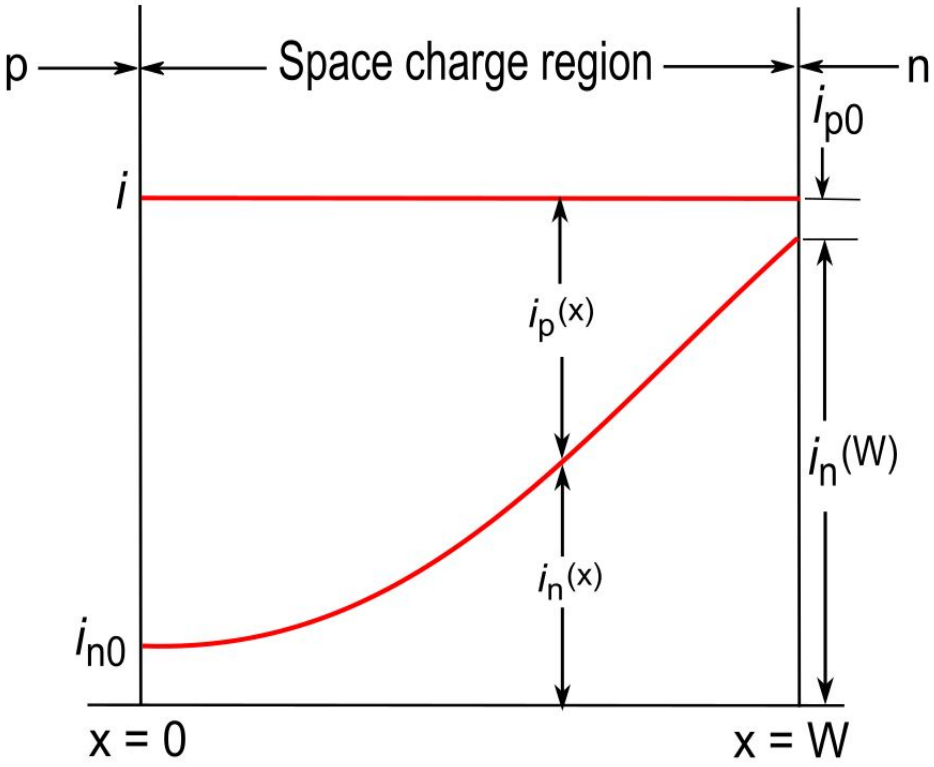

Figure 2.3: Current and hole components through the space charge region during avalanche multiplication.

Avalanche breakdown is a process that occurs when electron-hole pairs moving in the space charge region gains sufficient kinetic energy in the presence of a high longitudinal electric field to generate electron-hole pairs by the impact ionisation of the covalent bond in silicon atom within the depletion region [1, 2].

Let us assume that a reverse-biased current i_{n0} enters the depletion region at $x = 0$ as shown in Figure 2.3, the current i_n will increase with the distance through the depletion region due to the avalanche process. The current at the point where $x = W$ can be written as [2]:

$$i_n(W) = M_n i_{n0} \tag{2.12}$$

where M_n is a multiplication factor. The hole (i_p) will increases through the depletion region from the n-type to the p-type region and reaches a maximum value at $x = 0$. Thus, the total charge through the pn junction is constant in steady state.

The elementary increment of the current at some point x can be expressed as [2]:

$$di_n(x) = i_n(x)\alpha_n dx + i_p(x)\alpha_p dx \tag{2.13}$$

where α_n and α_p are the electron and the hole ionisation rates, respectively. Equation (2.13) can be rewritten as:

$$\frac{di_n(x)}{dx} = i_n(x)\alpha_n + i_p(x)\alpha_p \tag{2.14}$$

The total current i is given by:

$$i = i_n(x) + i_p(x) \tag{2.15}$$

solving for $i_p(x)$ in Equation (2.15) and substituting into Equation (2.14), which gives:

$$\frac{di_n(x)}{dx} + (\alpha_p - \alpha_n)i_n(x) = i\alpha_p \tag{2.16}$$

assuming that α_n and α_p are equal. Equation (2.16) may be simplified and integrated within the space charge region. Thus, leading to the expression given by:

$$i_n(W) - i_n(0) = i\int_0^W \alpha\ dx. \tag{2.17}$$

Using Equation (2.12), Equation (2.17) can be rewritten as [2]:

$$\frac{M_n i_{n0} - i_n(0)}{i} = \int_0^W \alpha\ dx. \tag{2.18}$$

Since $M_n\ i_{n0} \approx i$, and $i_n 0 = i_{n0}$, Equation (2.18) becomes

$$1 - \frac{1}{M_n} = \int_0^W \alpha\ dx \tag{2.19}$$

The avalanche breakdown voltage can be expressed as the voltage at which M_n approaches infinity. Therefore, the avalanche breakdown condition is given by

$$\int_0^W \alpha\ dx = 1 \tag{2.20}$$

2.3.2 Punch-Through Breakdown

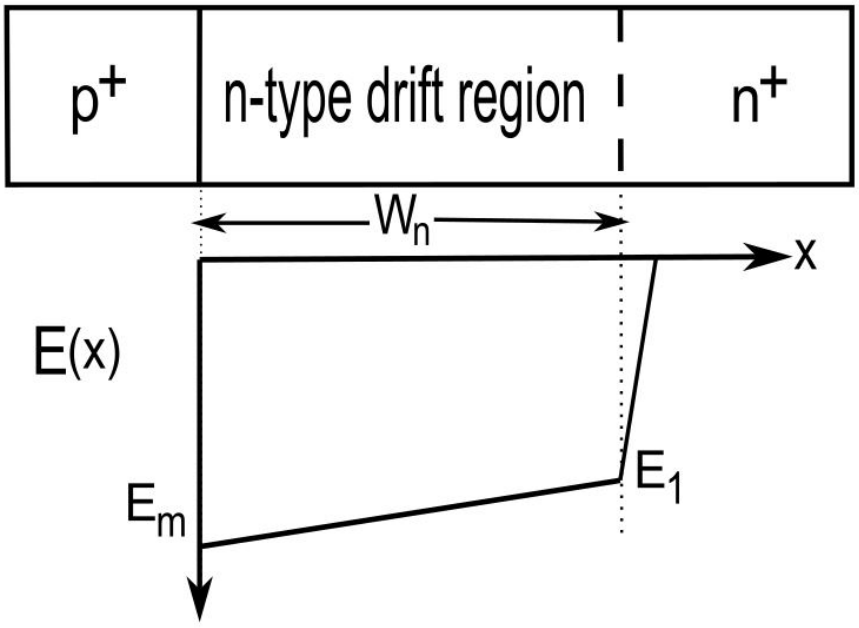

Figure 2.4: The punch-through design for a $p-i-n$ rectifier. The $p^+$and n^+ stands for highly doped p-type and n-type regions, respectively.

Punch-through breakdown in a semiconductor device occurs at a condition in which the depletion region at the p-body/drain contact extends across the channel region and merges with the source/p-body depletion region. This extension of the depletion region eliminates a channel which leads to the field beneath the gate becoming strongly dependent on the drain-source voltage subsequently resulting in a very high drain current in the device [2]. During this condition, the gate loses all its control over the channel and a large drain current flows in the device irrespective of the applied gate voltage.

A power device which is using a $p-i-n$ rectifier to support an applied voltage as show in Figure 2.4, a lightly doped n-type drift region is needed in the middle of highly doped p-type and n-type regions because the injection of a high concentration of minority carriers during the on-state limits the drift region resistance such that current flow is independent of the doping concentration in the drift region [7]. The electric field distribution in a punch-through design will vary moderately in the lightly doped n-type drift region and swiftly move towards the heavily doped n^+ end region, thereby forming a trapezoidal-shape field distribution.

The electric field distribution at the junction between the n-type drift region and the n^+ end region can be expressed as [7]:

$$E_1 = E_{max} - \frac{q\ n_n}{\varepsilon_{si}} W_n \tag{2.21}$$

where E_{max} is the maximum electric field at the interface between the p^+ and the n-type drift region, q is the electronic charge, ε_{si} is the dielectric constant of silicon, n_n is the doping concentration of the n-type drift region, and W_n is the width of the n-type drift region.

2.4 Classification of Power MOSFETs

Power semiconductor devices are two or three terminal devices as shown in Figure 2.5, having the capability of controlling the energy flow in electronic systems. They offers operating conditions from an off-state, in which a negligible current flows in the device when the supply voltage is sustained, to an on-state, when a substantial current flows through the device. Cells in a power MOSFET can be designed in a paralleled architecture to compensate for a low current of a single transistor and to allow a low on-resistance. Being a majority carrier device, the power MOSFET offers a better performance in terms of a low gate drive power, a fast switching speed and a superior paralleling architecture, thereby enhancing its utilisation for power application such as a DC-DC converter, a low voltage motor control, a linear power and switching supplies.

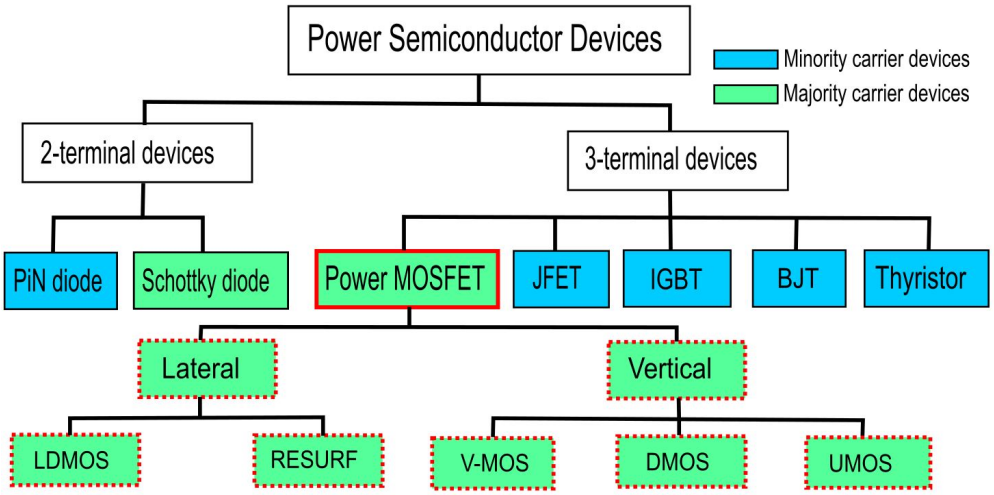

Figure 2.5: Types of power semiconductor transistors.

The transistor is used in power switches for low voltage (less than 200 V) applications, because its on-state resistance (R_{on}) increases swiftly with increase in the BV, resulting in a huge conduction losses and degradation of the system performances. In order to achieve a low resistive channel in a MOSFET, a shorter channel length (L_{ch}) is required with respective reduction in a gate oxide thickness (t_{ox}) since these two parameters are related to the breakdown voltage. Consequently, a variation in these two parameter limits the implementation of a power MOSFET for medium and high voltage applications. However, the cascade design of power MOSFETs can overcome this limitation but requires multiple transistors connected to operate as multi-level hybrid configuration [10–12]. The power MOSFET can be classified into lateral and vertical devices based on device design techniques. The structure and basic operating principle of both lateral and vertical power MOSFETs will be briefly discussed in the subsequent sections.

2.4.1 Vertical Power MOSFETs

2.4.1.1 V-MOSFET

A V-groove MOSFET (V-MOSFET) is a non-planar structure that consists of a V-groove gate design with the source and the drain regions separated by a p-body substrate, leading to a formation of two p-n junctions referred as J_A and J_B as shown in Figure 2.6 [7]. The gate electrode penetrates into trench etched in the device body and will be fabricated after thermal oxidation of the gate oxide on its surface [7, 13, 14]. Historically, the device was the first fabricated and commercialised power MOSFET structure. However, the stringent conditions of compliance with the orientation of anisotropic etching of the grooves in the structure limits the design variation of this architecture [2]. Thus, the V-MOSFET became less popular because of these manufacturing complexities and replaced by a planar architecture called a double-diffusion MOSFET (D-MOSFET). Additionally, the V-MOSFET suffered from a degradation of the breakdown voltage due to the high electric field crowding at the tip of the V-groove.

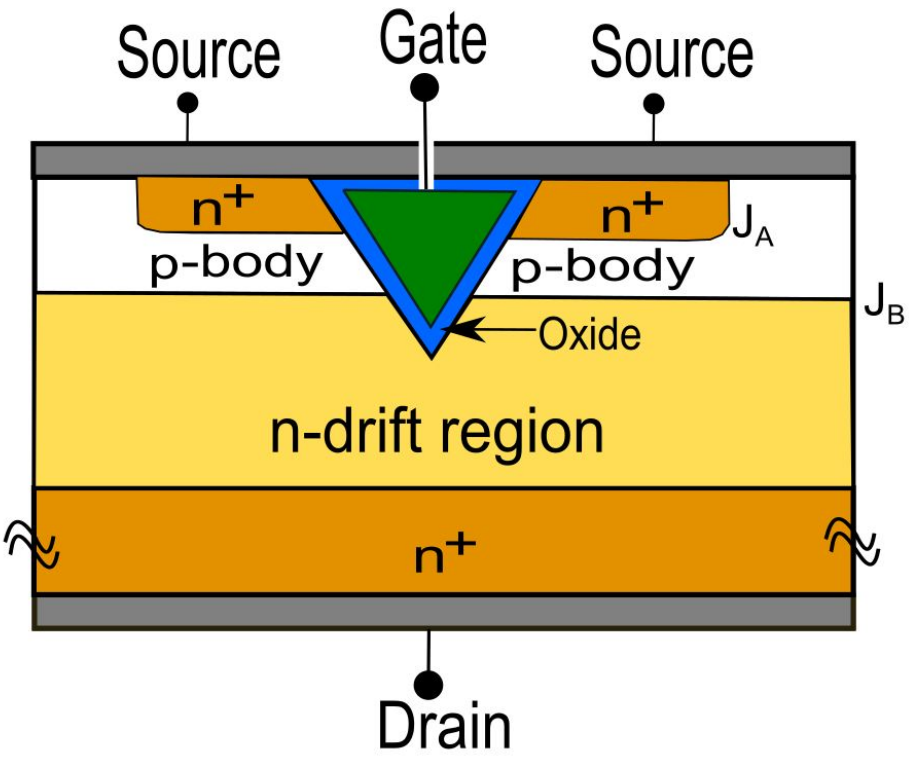

Figure 2.6: Cross-section of a V-groove MOSFET structure.

2.4.1.2 D-MOSFET

The D-MOSFET is a planar structure that uses a double diffusion process in which the p-body region and the source (n^+) contact are diffused via a common opening defined by the edge of the gate [2, 7]. A channel length is defined by the difference between the lateral diffusion distance of the p-body region and the source (n^+) as shown in Figure 2.7 [2]. The electron flows laterally through the inversion layer to the thick and lightly doped n-drift region and vertically to the drain, thereby establishing a conventional current flow from the drain to the source. The structure suffers from a non-uniform distribution of the current in the drift region, resulting in a large internal resistance that is higher than the ideal specific on-resistance of the drift region.

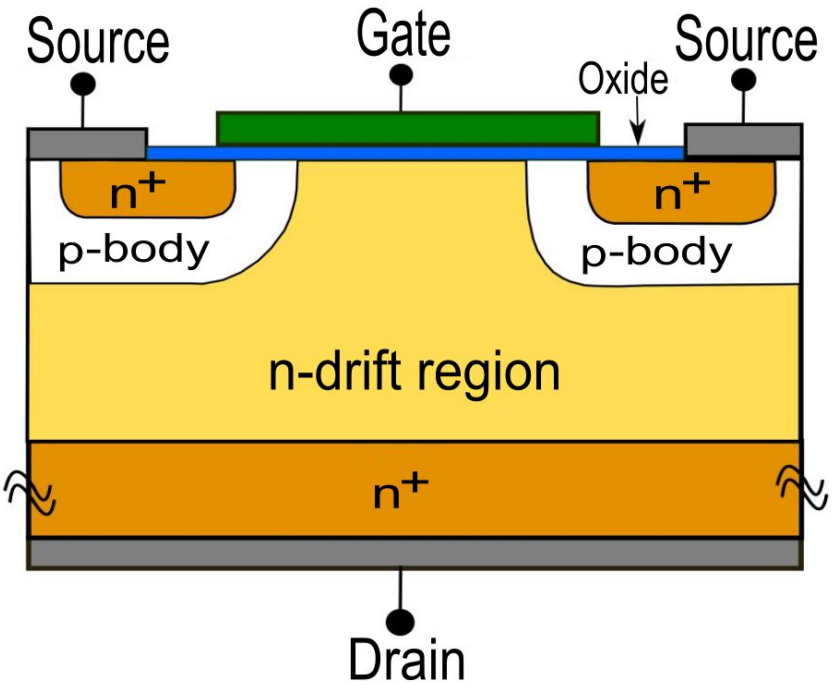

Figure 2.7: Cross-section of a D-MOSFET structure.

2.4.1.3 U-MOSFET

A U-MOSFET is also non-planar structure like the V-MOSFET but with a U-shaped groove or a trench at the gate region as shown in Figure 2.8 [15]. The implanted

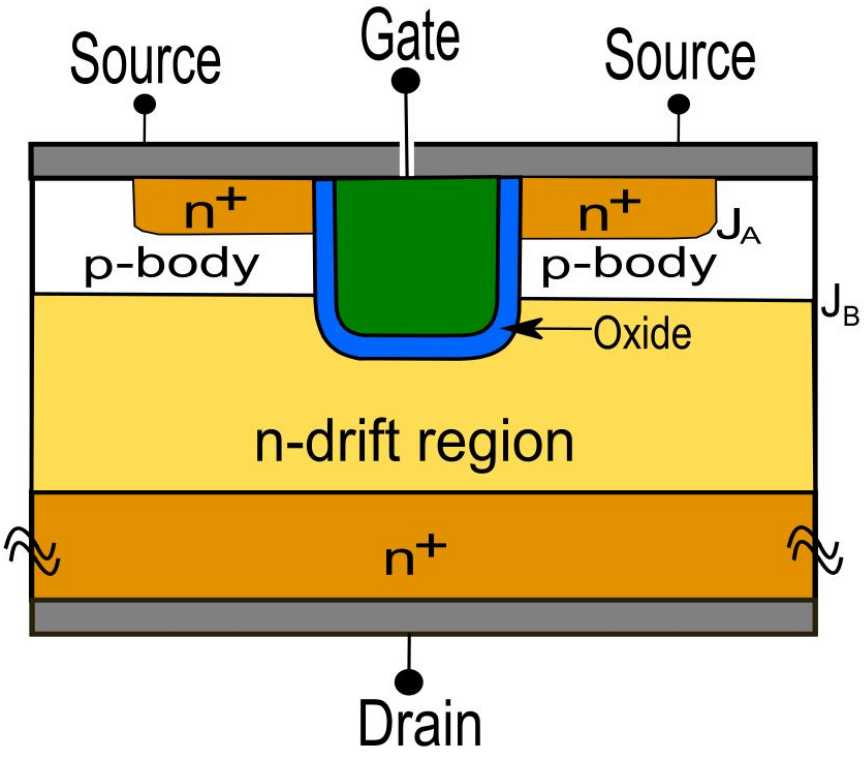

Figure 2.8: Cross-section of a U-MOSFET structure.

trench gate extends from the top surface of the device through the p-body and the source (n^+) regions into the n-drift. In contrast to the D-MOSFET, this device architecture does not suffer from a high input impedance resulting in the reduction of on-resistance [15]. In addition, the bottom of the trench gate is rounded by the isotropic etching in order to protect the gate oxide and to redistribute electron current crowding at the edge of the gate [16]. Likewise, a deeper and higher doping concentration of the p-body, will ensure that the avalanche breakdown occurs at a junction between the p-body and the n-drift region. In comparison with the D-MOSFET, the U-MOSFET offers a higher transconductance because of its larger channel density.

2.4.2 Lateral Power MOSFETs

2.4.2.1 Lateral Double Diffused MOSFETs (LDMOSFETs)

The lateral double diffused MOSFET (LDMOSFET) has become a popular device choice for power integrated circuit technologies (PICT) [17], with the capability of offering a low resistance, a high input impedance, a high breakdown voltage, and a fast switching speed. The device is desirable for integration as a high-power transistor with a low-voltage digital circuit in the BiCMOS technology [18, 19]. A LDMOSFET with a gate length of L_g and a width of W_g shown in Figure 2.9 [20] is a lateral surface effect device in which a vertical field induced by the gate controls the channel. During on-state, biasing with a positive gate voltage higher than a threshold voltage will induces a formation of an inversion layer at the surface of the p-body, resulting in a flow of electrons from the source (n^+) electrode through the conductive channel to the drain (n^+) electrode via the n-drift region. During off-state, a reverse-bias applied voltage at the drain results in a large depletion region with a high blocking voltage which extends through the n-drift region. During the diffusion process of the device, the same mask can be used for the channel and the source regions resulting in a short channel. In addition, the deeper diffused p-body has a large radius in doping distribution that reduces the edge effects in the structure [20].

The drift region is necessary to support the electric field during the blocking voltage on the drain. It must be thick enough to provide a sufficient space for the both lateral and vertical electric fields and lightly doped for a slowly changing electric

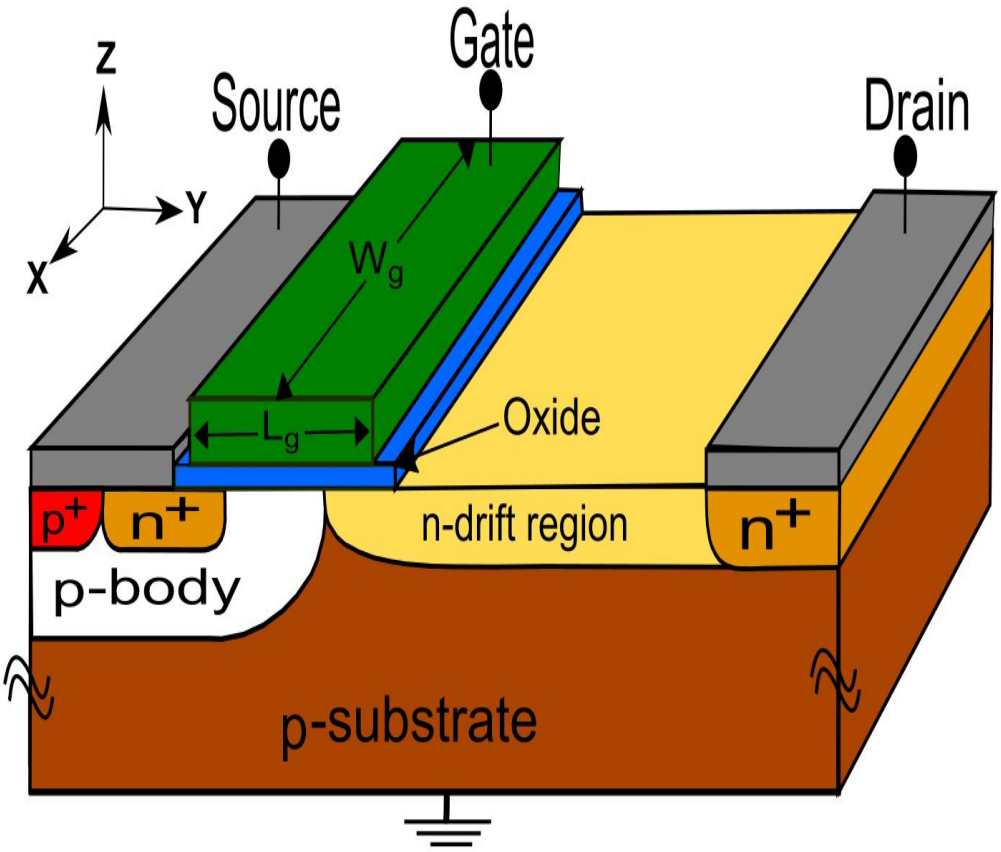

Figure 2.9: Cross-section of a LDMOSFET structure having a gate length of L_g with a width of W_g.

field ideal for a flat band profile. The avalanche breakdown capability of the device is determined by the doping concentration of a drift region (n_{drift}), the drift length (L_{drift}) and its thickness t_{drift} [21]. Adversely, a thick and lightly doped drift region will aggravate the specific on-resistance ($R_{on,sp}$) of the device, because of its relationship with a breakdown voltage (BV) (Note that the breakdown voltage is abbreviated by the word BV and a symbol for the breakdown voltage is also BV). The specific on-resistance ($R_{on,sp}$) can be expressed by [7]:

$$R_{on,sp} = \frac{L_d}{q\ \mu_n\ n_n} \tag{2.22}$$

where n_n is the doping concentration of the n-type drift region, q is the electronic charge, μ_n is the average electron mobility and L_d is the length of the drift region.

Given that L_d can be expressed by [7]:

$$L_d = \frac{2BV}{E_c}, \tag{2.23}$$

the breakdown voltage (BV) can be written as:

$$BV = \frac{\varepsilon_0 \varepsilon_{si} E_c^2}{2qn_n}, \tag{2.24}$$

Substituting Equations (2.23) and (2.24) into Equation (2.22) gives

$$R_{on,sp} = \frac{4BV^2}{\mu_n \varepsilon_{si} E_c^3}, \tag{2.25}$$

A solution from Equations (2.25) will lead to an expression given by:

$$R_{on,sp} = 5.93 \times 10^{-9}\ BV^{2.5}. \tag{2.26}$$

This quadratic expression implies that doubling of the BV leads to increase in the specific on-resistance by a factor of five. Therefore, p-body and the n-drift regions has to be optimised, aiming at achieving a high voltage blocking capability and minimising the drain-to-source resistance, the transistor pitch, and the transistor width.

2.4.2.2 RESURF (Reduced Surface Field) LDMOSFET

The REduced SURface Field (RESURF) as proposed by Appels and Vaes [22] is a concepts that provides an improvement in the trade-off between the breakdown voltage and the specific on-resistance of a lateral device. It involves reducing the surface electric field of the device, which will allow a higher reverse voltage to be applied before a critical value of the avalanche breakdown is reached. This is achieved by extending the space charge region in the blocking state in the entire drift zone, resulting in a voltage drop over the charge distribution along the drift region and not across the junctions [22, 23]. Figure 2.10 shows a cross-section of a single RESURF LDMOS having two diodes (D_1 and D_2), with D_1 located at the lateral junction between the n-epi and the p-body region; and D_2 positioned at the vertical junction between the n-epi and the p-substrate region. With a careful choice of the thickness

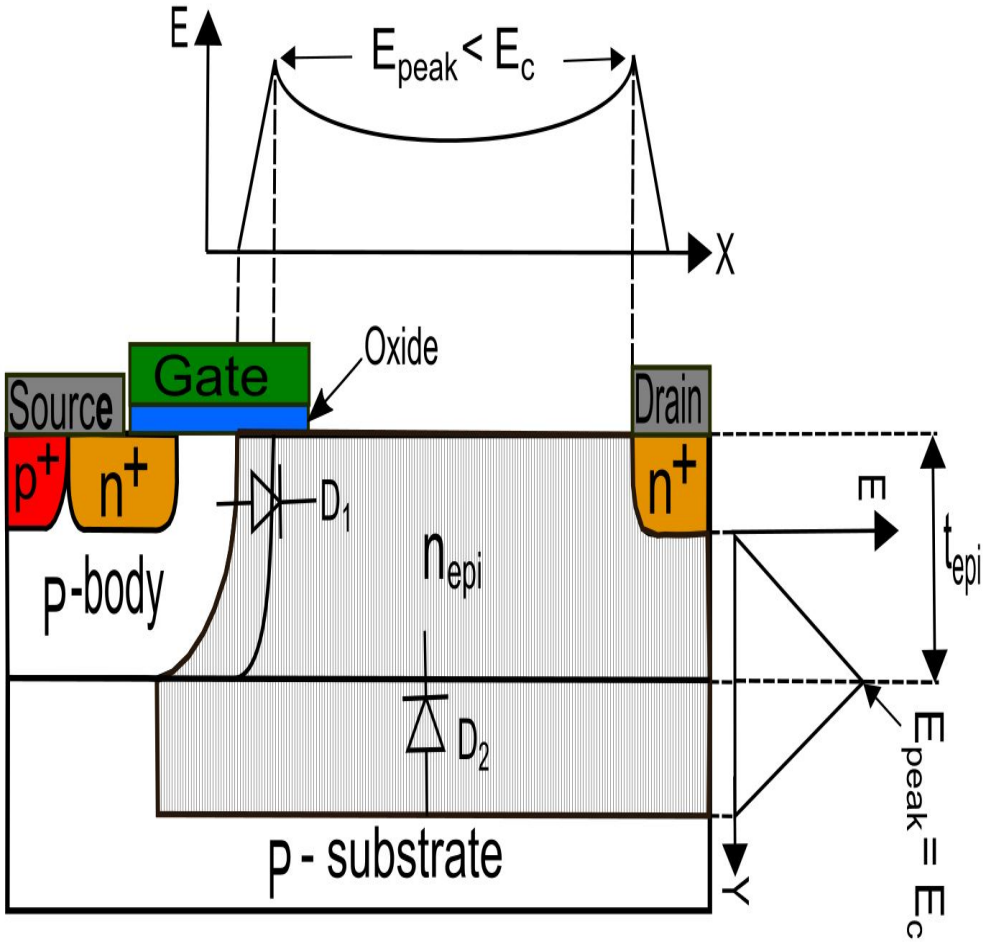

Figure 2.10: A single RESURF LDMOSFET architecture having a drift region of n_{epi} layer with a thickness of t_{epi}, at a full depletion with the field distributions in the shaded regions.

of the drift region chosen in a blocking state, the space charge regions from both lateral and vertical junctions extend up to a surface of the device thereby reducing the electric field below the critical electric field E_C. This will ensures a higher blocking voltage at the junction between the n-epi and the p-substrate when the electric field reaches a critical value. At a full depletion, the depletion width (W_d) must be equal to the thickness of the epitaxial layer (t_{epi}) as expressed by [22]:

$$W_d = t_{epi} = \sqrt{\frac{2\varepsilon_s(BV)}{q(n_{epi} + n_{sub})}} \tag{2.27}$$

where ε_{si} is the dielectric constant of silicon, q is the electronic charge and n_{epi} and n_{sub} are the doping concentration of the epitaxial layer and the p-substrate, respectively.

The ideal BV of a planar junction is given by [22]:

$$BV = \varepsilon_{si} \frac{E_c^2}{2q(n_{epi} + n_{sub})} \tag{2.28}$$

where E_c is the critical electric field in silicon with an optimal epitaxial charge density $Q_{epi} = n_{epi} \times t_{epi}$ given by [22]:

$$Q_{epi} = n_{epi}\ t_{epi} = \varepsilon_{si} \frac{E_c}{q} \sqrt{\frac{n_{sub}}{(n_{epi} + n_{sub})}} \tag{2.29}$$

If $n_{epi} >> n_{sub}$, where t_{epi} is the thickness of the epitaxial layer, then n_{sub}, equal to n_{epi} at an upper theoretical bound of Q_{epi}, is given by:

$$Q_{epi,max} = \varepsilon_s \frac{E_c}{q\sqrt{2}} \tag{2.30}$$

$$n_{epi}\ t_{epi} \cong 1 - 2 \times 10^{12} \quad cm^{-2} \tag{2.31}$$

Considering the fact that maximum fields are limited by the RESURF architectures, the doping concentration of the drift region can be increased and the drift region length can be decreased simultaneously, resulting in a reduction of the on-resistance of the structure. The single RESURF architecture has been in use in high-voltage LDMOSFETs [24–28] for about 45 years.

A double RESURF architecture using a shallow-trench isolation (STI) is shown in Figure 2.11 [29]. The n-drift region is fully depleted by two junctions, the P_{top} layer and the n-drift junction at the top and the p-substrate layer and the n-drift junction at the bottom. In order to achieve a high breakdown in the structure, both the P_{top} layer and the n-drift region must be fully depleted before the lateral breakdown voltage between the P_{top} layer to the drain (n^+) is reached. Since $n_{P_{top}} > n_D > n_{p-sub}$, the breakdown voltage can be expressed as [21]:

$$BV \ = \ \frac{\varepsilon_0 \varepsilon_{si} E_c^2}{2\ q\ n_D} \quad [V] \tag{2.32}$$

where

$$n_{P_{top}} \times t_{top} \ = \ \frac{2 \times 10^{12}}{\sqrt{1 + \frac{n_{P_{top}}}{n_D}}} \quad cm^{-2} \tag{2.33}$$

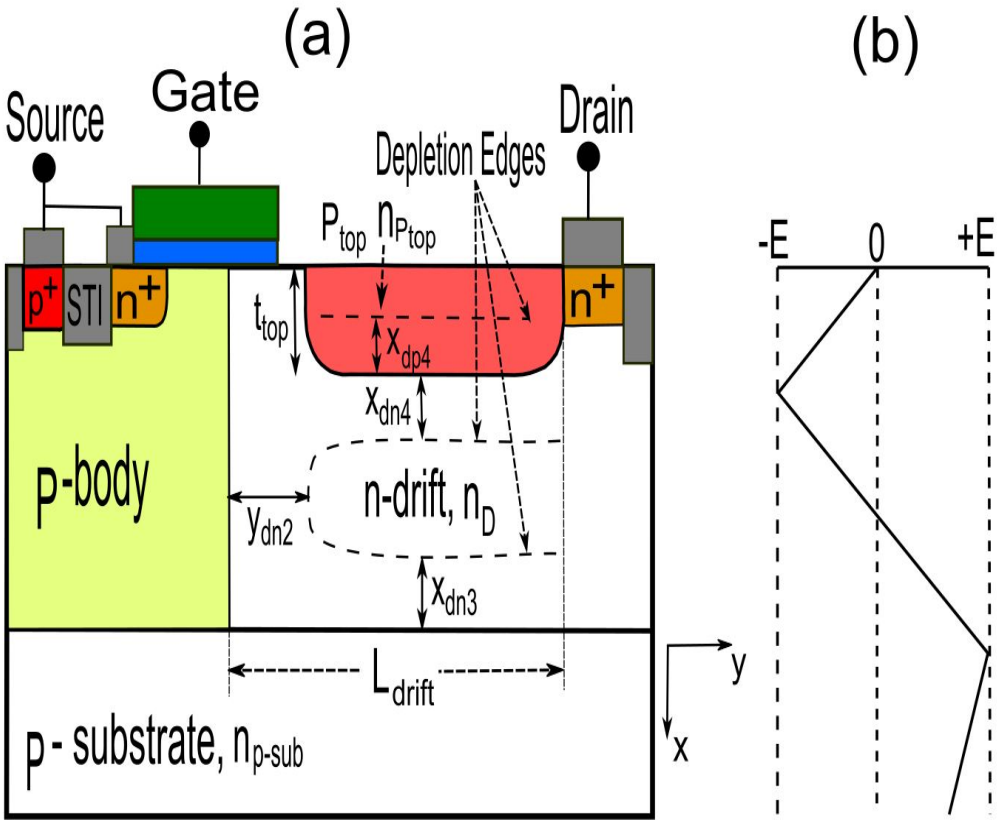

Figure 2.11: (a) Schematic cross-section of a double RESURF structure consisting of a P_{top} layer of t_{top} thickness having a doping concentration of $n_{P_{top}}$ implanted at the top of the n-drift region with a distance of x_{dn4} between the P_{top}/n-drift junction, (b) field distribution in a double RESURF structure assuming a full depletion in the n-drift region with a distance of y_{dn2} between the p-body/n-drift junction and a distance of x_{dn3} between the n-drift/p-substrate junction.

where $n_{P_{top}}$, n_D and n_{p-sub} are the doping concentration of P_{top} layer, n-drift region and p-substrate, respectively, while ε_0 and ε_{si} are the dielectric constants of oxide and silicon and t_{top} is the thickness of the P_{top} layer. In a double-RESURF structure, since the drift region is simultaneously depleted from both the top and the bottom junctions, the integrated concentration between these two junctions in the drift region can be increased by approximately a factor of 2 to about 2.8×10^{12} cm^{-2} in comparison to a single RESURF structure of the same drift thickness. This will ensure a lower drift resistance in the structure. Various device designs of double RESURF architecture for a high-voltage LDMOSFET structure have been reported [29–33]. In a triple RESURF structure using a shallow-trench isolation (STI), as shown in Figure 2.12 [34], a buried p-layer is implanted into the n-drift region, thereby splitting the n-drift into two conducting paths, one at the bottom and the other on top of the buried layer.

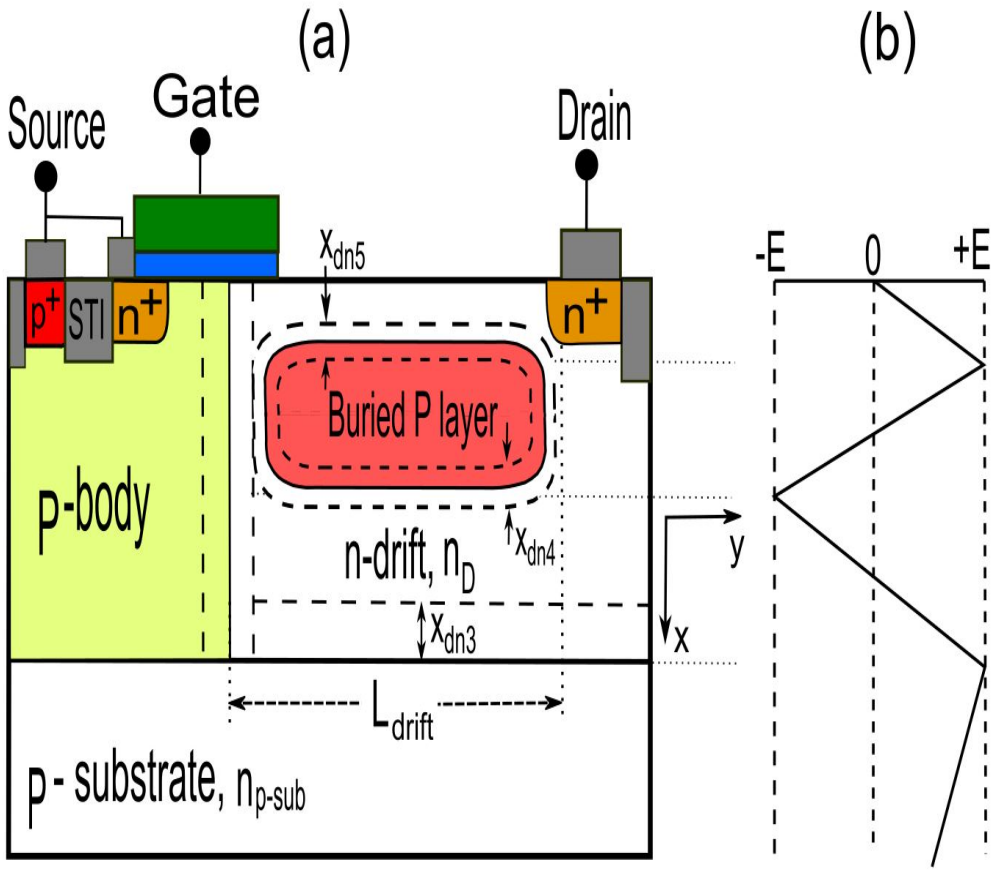

Figure 2.12: (a) Schematic cross-section of a triple RESURF structure having a buried p-layer implanted inside the n-drift region, with an expanded depletion regions of x_{dn4} at the bottom and x_{dn5} at the top, (b) vertical field distribution at midpoint of L_{drift} at a full depletion in the n-drift region with a distance of x_{dn3} between the n-drift/p-substrate junction.

The depletion region within the buried layer expands to x_{dn4} at the bottom and x_{dn5} at the top of the layer. Therefore, these three junction boundaries continuously deplete the drift region, the n-drift/p-substrate junction (x_{dn3}), the bottom (x_{dn4}) and the top (x_{dn5}) junction of the buried layer [34–36].

2.5 Fundamentals of Super-Junction (SJ) Power MOSFETs

The realisation of super-junction (SJ) [37] concept has offered a great improvement in the trade-off between the BV and the specific on-resistance ($R_{on,sp}$) of a power device for medium and high voltage applications [37–42]. In order to explain a concept of the SJ MOSFET, one can start from a simplified SJ diode layer shown in Figure 2.13 where T is the thickness of the device, n_n and n_p are the doping concentration of the $n-$ and $p-$ pillars with their corresponding width of W_n and W_p, respectively, while ε_{si} is the dielectric constant of silicon and q is the electronic charge. The 2-D electric field distribution in the SJ diode layer can be expressed

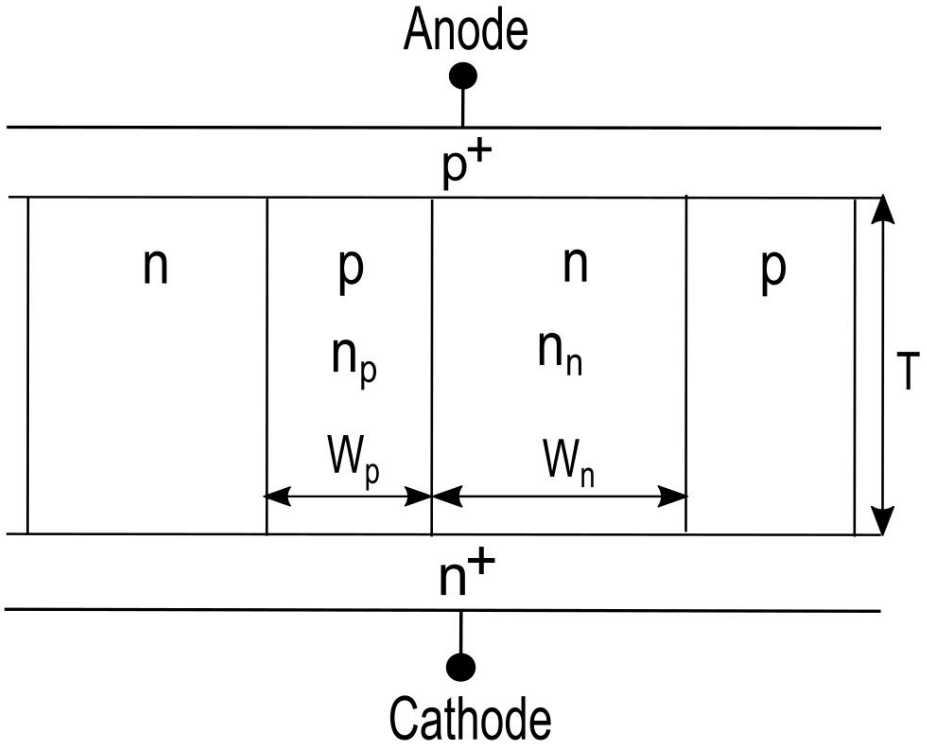

Figure 2.13: Cross-section of a super-junction diode layer.

as [37]:

$$\nabla \cdot E = \frac{dE(x)}{dx} + \frac{dE(y)}{dy} = \frac{q(n_n)}{\epsilon_{si}} \tag{2.34}$$

In a doped $n-$ pillar, $n_n > 0$, this Equation (2.34) can be rewritten as:

$$\frac{dE(x)}{dx} = \frac{q(n_n)}{\epsilon_{si}} - \frac{dE(y)}{dy} \tag{2.35}$$

which implies that the dE/dx is no more dependent on the n_n but can be reduced by the presence of the electric field that varies in the y-direction. A BV is given by:

$$BV = \int_0^T E_x dx \tag{2.36}$$

The presence of a 2-D electric field in Equation (2.35) implies that the electric field distribution in the structure can be lowered without reducing the doping concentration of the $n-$ pillar. Therefore, the SJ concept demonstrates that a 2-D design of the sustaining layer can produce an electric field in y-direction that results in the generation of a similar electric field in x-direction even with increase in the doping concentration of the pillar. The point in which the electric field in the $n-$ and $p-$ pillars mutually deplete each other is referred as a charge-balanced condition in a SJ layer.

A power device requires a thick and lightly doped drift region to achieve a higher breakdown voltage. However, the quadratic relationship of Equation (2.26) between the BV and the $R_{on,sp}$ [43] implies that the on-resistance increases with increase in the BV. A SJ-LDMOS transistor uses a set of alternating heavily doped n-type and p-type pillars in the drift region, resulting in minimising the on-resistance of the transistor area [38–42, 44–46]. In addition, the SJ-LDMOS has been able to overcome the ideal theoretical limit of silicon [37, 47]. A basic operation of the SJ power MOSFETs is reviewed in the next sub-sections.

2.5.1 Vertical Super-Junction (SJ) Power MOSFETs

The vertical SJ power MOSFET (SJ-VDMOSFET) structures were the first commercialised device design [40–42, 44] that have achieved a tremendous improvement in the relationship between the BV and the $R_{on,sp}$. Figure 2.14 shows the vertical SJ-MOSFET [47] in which the n^+ layer is connected to the drain while the $p-$ pillars is connected to the source via the p-body of the device. In off-state, the reverse biased $p-n$ junctions are mutually depleted by optimising the width and the doping concentration of the n_{epi} layer and the $p-$ pillars, thereby ensuring that the two opposite pillars are fully depleted before the critical electric field is reached. Upon reaching a full depletion, an equal but opposite charges are needed to compensate each other, thereby achieving a horizontal electric field without upsetting the ver-

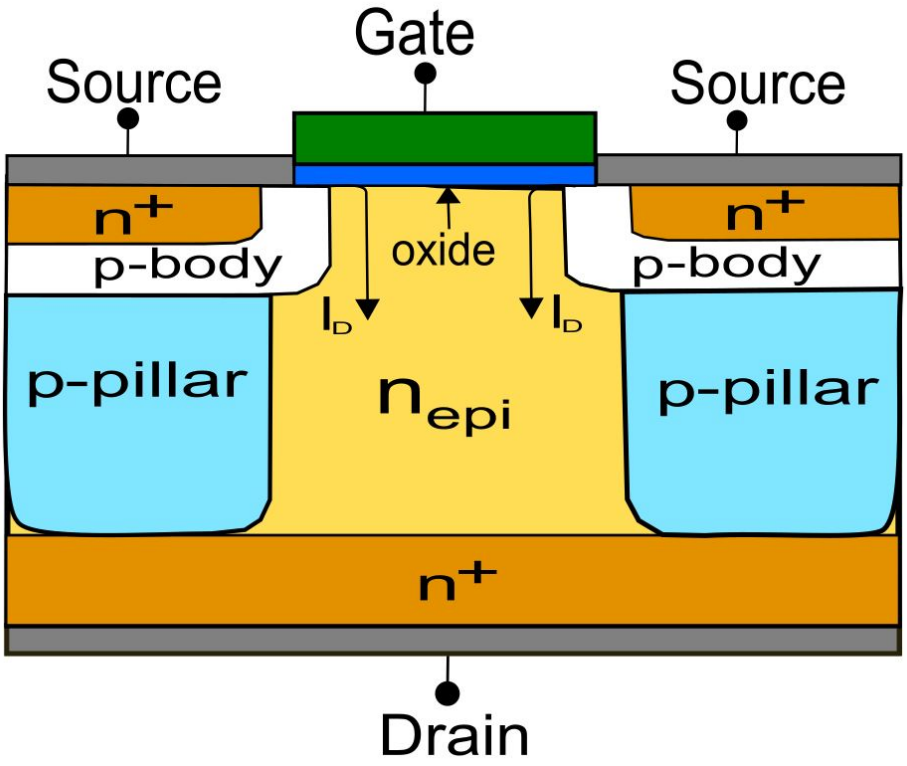

Figure 2.14: Cross section of a vertical SJ-MOSFET structure.

tical electric field distribution in the SJ structure. This SJ design benefits from a charge compensation between opposite pillars when the n_{epi} layer are fully depleted. The vertical electric field in the drain-to-source region depends on the depth of the drift region. Consequently, a higher breakdown voltage can be achieved by increasing only the depth of the drift region with no need of changing the pillars doping concentration.

Given that the structure has a drift region length of L_d, the doping concentration of n_{epi} layer and p–pillar are n_n and n_p, with W_n and W_p their corresponding widths, respectively, and assuming a fully depleted drift region under charge balanced condition, with $W_n = W_p = W_{np}$, a relationship between the BV and the charge Q of a pillar can be expressed as [48]:

$$BV = E_c \, L_d \tag{2.37}$$

$$Q = \frac{n_n \, W_{np}}{2} = \frac{\varepsilon_{si} E_c}{q} \tag{2.38}$$

where the critical electric field (E_c) increases with the increase in the doping concentration of the pillar. Since the electron current flows through the n_{epi} layer only,

the specific on-resistance can be written as [48]:

$$R_{on,sp} = \frac{L_d}{q\ \mu_n\ n_n} = \frac{W_{np}\ BV}{2\ \mu_n \varepsilon_{si} E_c^2} \tag{2.39}$$

Since the optimal integrated doping concentration is fixed for a given BV, the doping concentration of n_{epi} layer can be increased to be inversely proportional to the drift width resulting in a reduction of the specific on-resistance. This leads to linear relation between the BV and the $R_{on,sp}$ [37, 49]. A more comprehensive analysis carried out for some of vertical designs has shown that dependence of $R_{on,sp}$ on the BV can be expressed as $BV^{\frac{7}{6}}$ [42, 45, 46, 50]. Optimal performance of the vertical SJ structure can be realised by optimising the pillar width, the doping concentration, and the drift region depth, respectively, aiming at achieving a high BV by a fully depleted charge compensating SJ drift region, and a low $R_{on,sp}$ by a heavily doped n_{epi} layer in the drift region.

2.5.2 Lateral Super-Junction (SJ) Power MOSFETs

The lateral SJ power MOSFETs (SJ-LDMOSFETs) uses the principle of a charge compensation between the alternating $n-$ and $p-$ pillars [51–57]. However, the imperfect inter-diffusion in the SJ pillars might cause the BV to become sensitive to charge imbalance in a drift region [53]. In an ideal SJ operation, the charge induces by the SJ $n-$ and $p-$ pillars should provide a mirror symmetry of each other in order to ensure a charge compensation during off-state.

A fully depleted SJ unit will be accomplished if ion charge of each pillar is cancel out by its two adjacent opposite conductivity pillars, thereby resulting in uniform electric field distribution in the drift region. This phenomenon is inherent to the SJ-VDMOSFETs because of its 2-D structure but, the SJ-LDMOSFETs being a 3-D device, requires a well designed p-type substrate or dielectric beneath the SJ drift region design to eliminate a leakage current. A junction isolated (JI) SJ-LDMOSFET having a drift region length of L_{drift} with the $n-$ and $p-$ pillars widths of W_n and W_p and a pillar height of h [54, 55] is shown in Figure 2.15.

The structure is implemented on a p-type substrate, such that $p-n$ junctions will be formed between the $n-$ pillars and both the $p-$ pillars and the p-substrate, resulting in a vertical electric field that strongly depends on the lateral position in

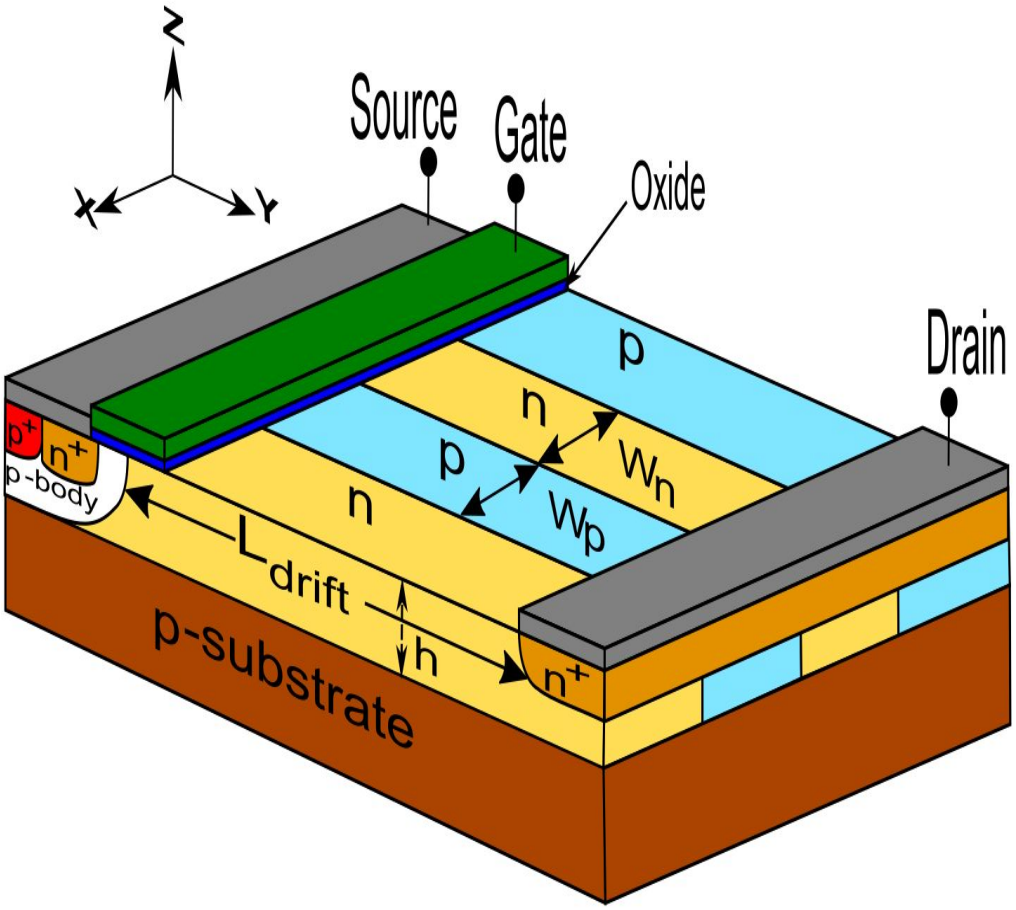

Figure 2.15: 3-D geometry of a Junction Isolated (JI) SJ-LDMOSFET structure.

the drift region. In off-state, the $n-$ pillars are depleted by both the $p-$ pillars and the p-type substrate, whereas the $p-$ pillars are only depleted by the opposite $n-$ pillars. This gives rise to excess charge in the pillars which increases monotonically towards the drain region due a voltage gradient across the SJ drift unit resulting in a charge imbalance and degradation of the BV [56]. In order to mitigate the effect of substrate-assisted depletion (SAD) in the JI SJ-LDMOSFET and improve the trade-off between BV and the specific on-resistance, various device designs have been reported in the last few decade to overcome these problem. In the following sections, a brief summary of the various evolutions of the SJ-LDMOSFETs technologies and their challenges in achieving an optimal device performances.

2.5.2.1 Buffered SJ-LDMOSFET

Super-junction (SJ) LDMOSFET structure having a drift region length of L_{drift} with the $n-$ and $p-$ pillars widths of W_n and W_p and a pillar height of h is shown in Figure 2.16 [57]. The device has an n-type buffer layer sandwiched between the SJ

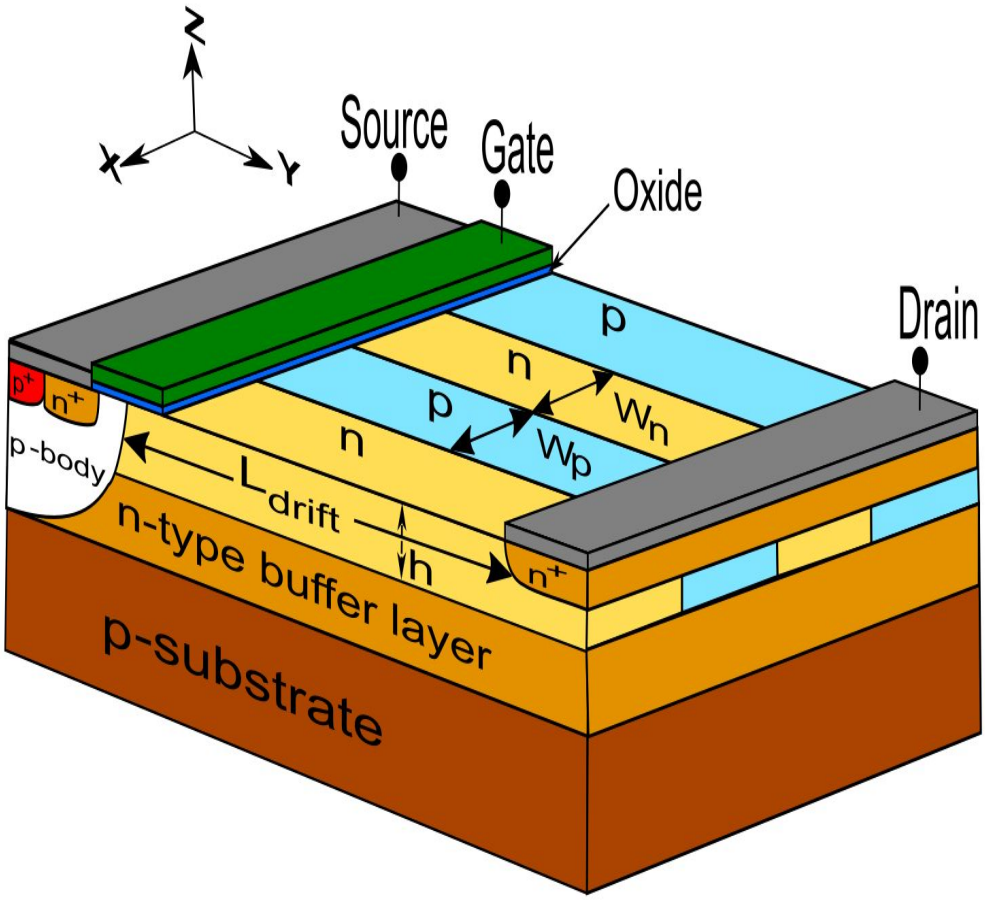

Figure 2.16: 3-D geometry of a buffered SJ-LDMOSFET structure.

layer and the p-type substrate. During off-state, the $p-$ pillars are depleted by both the $n-$ pillars and the n-type buffer layer, unlike the JI SJ-LDMOSFETs where the $p-$ pillars are depleted by $n-$ pillars only. After the n-type buffer layer have been fully depleted, the p-type substrate will begins to deplete the $n-$ pillars, to the extent that the resultant effect of both the vertical and the lateral electric field in the SJ drift region will reduces the charge imbalance of the structure compared to the JI SJ-LDMOSFETs. In this structure, the n-type buffer layer compensates for the extra charge needed to deplete the $p-$ pillars completely, thereby eliminating the SAD in the SJ region. Various architecture designs of this structure have been reported to eliminate the effect of SAD in the SJ layer, like the REBULF SJ-MOSFET with n^+

buried layer [58], which consists of a n-type buffer layer sandwiched between two p-type substrate layers such that the pillars are depleted by the vertical depletion effect due to electric field in the horizontal direction resulting in the complete charge balance in the SJ drift region. Duan et al. [59, 60] has reported a new SJ-LDMOS with a step n-type buffered layer implemented beneath the SJ layer, in which the step doped n-type layer uses an electric field modulation to generate a new lateral electric field resulting in a more uniform lateral electric distribution in the device. Cao et al. [61] has also proposed a SJ-LDMOS with multi-floating buried layers, which utilises the combination of the surface and bulk electric field optimisation at the same time.

2.5.2.2 Silicon on Insulator (SOI) SJ-LDMOSFET

A silicon on insulator (SOI) SJ-LDMOSFET structure shown in Figure 2.17 [62] is based on dielectrically isolated (DI) region that consists of a drift region with a length of L_{drift} and $n-$ and $p-$ pillars with widths of W_n and W_p, respectively, and a height of h. The structure has also a buried oxide layer implanted between the SJ

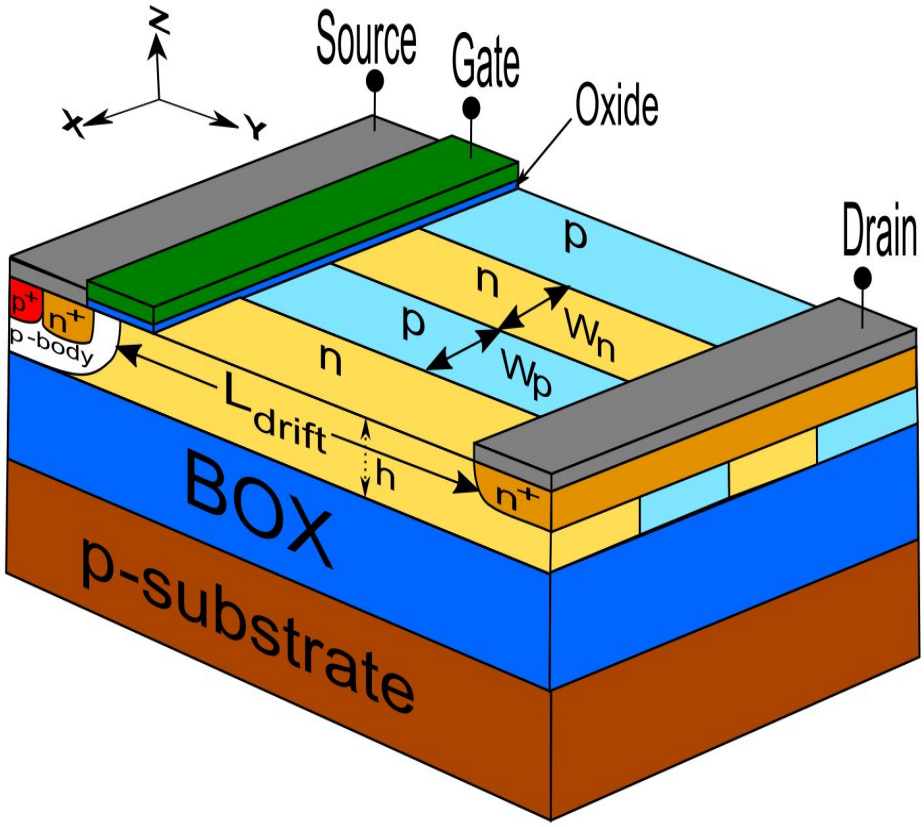

Figure 2.17: 3-D geometry of a silicon-on-insulator (SOI) SJ-LDMOSFET.

layer and the p-substrate resulting in the uniform distribution of the electric field, thereby alleviating the effect of the SAD. Various modifications of a design structure of the SOI SJ-LDMOSFETs have been reported [63–68].

The advantage of the SOI design includes, amongst others, an improve device isolation, a high packing density, a low leakage current at high temperature operation, and a latch-up-free operation [68]. However, the structure suffers from a similar effect of the SAD as a result of the vertical electric field that is emanating from the capacitive coupling of inserting an insulator or a silicon dioxide ($Si0_2$) between two silicon layers [69]. In addition, the SOI SJ-LDMOSFETs suffer from enhanced self-heating effects [70, 71], due to the poor thermal conductivity of the silicon dioxide ($Si0_2$) (1.4 W/m-K) in comparison to silicon (140 W/m-K)) [72, 73]. The buried oxide layer hinders heat transfer from the SOI layer to the p-substrate resulting in the degradation of the device performance such as a reduction of current mobility and the stressing of wire bonds or metal contacts.

Duan et al. [74] has proposed a SJ-LDMOSFET with a double step oxide layer beneath the SJ structure that formed a step SOI layer, creating a thin SOI layer close the source and the gate, and with a thick SOI layer situated in the proximity of the drain. In this structure, a uniform lateral electric field is produced due to the linearly increment in the thickness of the SOI layer from the source to the drain.

2.5.2.3 Partial Silicon on Insulator (PSOI) SJ-LDMOSFET

The partial SOI (PSOI) SJ-LDMOSFET, shown in Figure 2.18 [75, 76], consists of a drift region with a length of L_{drift} and $n-$ and $p-$ pillars with widths of W_n and W_p, respectively, and with a height of h. The structure has also a small window opening in the buried oxide layer underneath the p-body and source.

The PSOI SJ-LDMOSFET was reported as a preferred solution to conventional SOI (C-SOI) SJ-LDMOSFETs [75–80]. The silicon opening in this device architecture serves as a thermal window for heat transfer from the active SOI layer to the p-substrate thereby reducing the self-heating effect [81, 82], but also enhancing uniform distribution of electric field in the drift region [83, 84]. However, the fabrication of PSOI structure is a major hindrance resulting in a asymmetry window size that leads to degradation of the insulating properties.

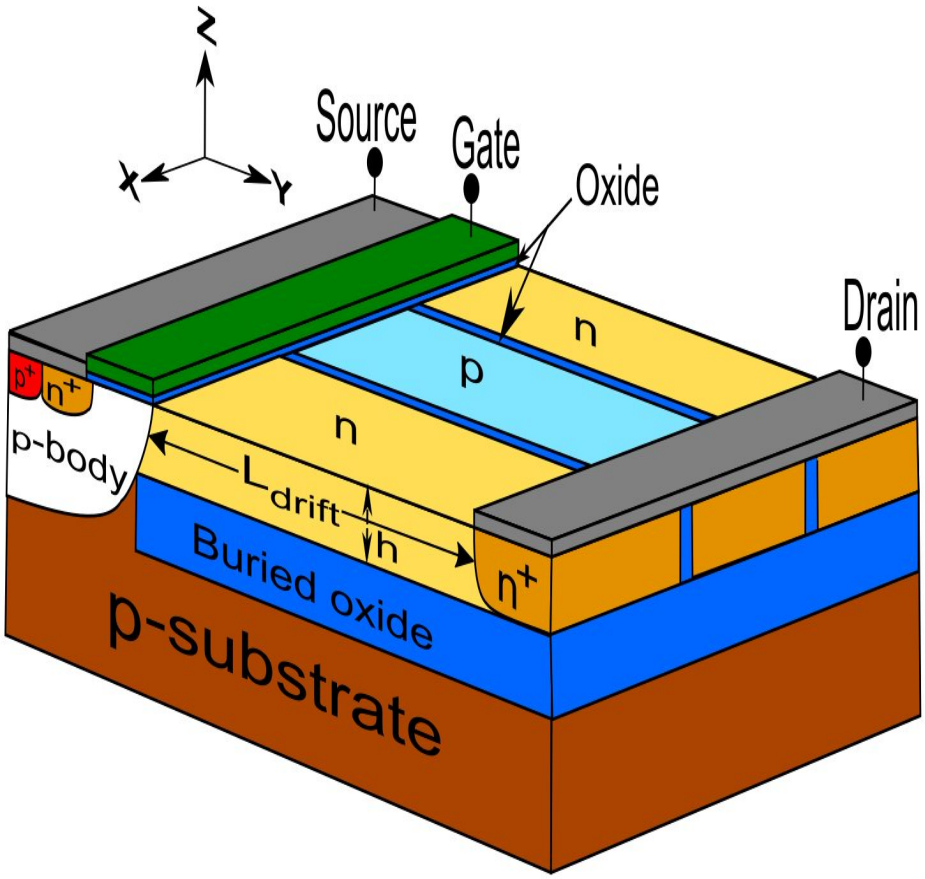

Figure 2.18: 3-D geometry of a partial silicon-on-insulator (PSOI) SJ-LDMOSFET.

2.5.2.4 Silicon on Sapphire (SOS) SJ-LDMOSFET

A SJ-LDMOSFET having a drift region length of L_{drift} with the $n-$ and $p-$ pillars with widths of W_n and W_p, respectively, and a height of h can be fabricated on a sapphire substrate [85] as shown in Figure 2.19. The device design is reported as a preferred solution of alleviating the self-heating effects in the DI SJ-LDMOSFET. The structure consists of a SJ layer that is fabricated on a crystal sapphire substrate. The sapphire (αAl_2O_3) substrate offers a better thermal conducting path than a silicon dioxide ($Si0_2$) because of its thermal conductivity of 0.42 W/cm-K is higher than that of the silicon dioxide ($Si0_2$) by a factor of 30 but less than the silicon by a factor of 3.7 at room temperature [86]. The silicon-on-sapphire (SOS) structure offers a better thermal and RF characteristics with a higher breakdown capability than the SOI and the PSOI devices. However, in comparison with the SOI structures, the SOS devices are costly, susceptible to a lower carrier mobility and a higher trap density at the Si/Al_2O_3 interface [87].

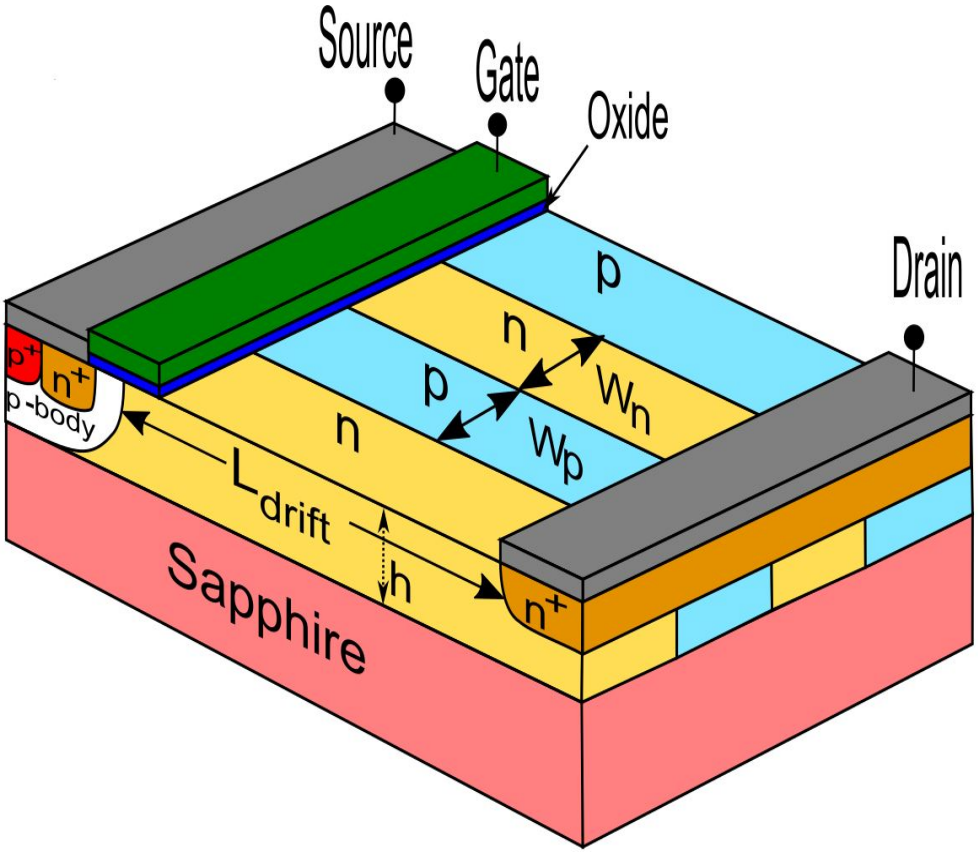

Figure 2.19: 3-D geometry of a silicon-on-sapphire (SOS) SJ-LDMOSFET.

2.5.2.5 SJ/RESURF LDMOSFET

The superjunction (SJ) RESURF LDMOSFET [88] splits the drift region into two distinct portions with an equal pillar height of h as shown in Figure 2.20. The first part consists of a SJ structure with a set of alternating and heavily doped $n-$ and $p-$ pillars having equal doping concentrations of $n_n = n_p$ with W_n and W_p as their corresponding widths and a drift length of L_{d1}, respectively. The second part is a RESURF region having a doping concentration of n_R and a drift length of L_{d2} that terminates at the drain contact. The two regions are fabricated on the p-substrate such that n_R is less than $n_n = n_p$, and L_{d1} is greater than L_{d2}. Interaction between the SJ region and a substrate can be alleviated by using a lightly doped p-substrate. Metal field plates that extends over the oxide layer from the gate to the drain are incorporated to mitigate electric field crowding under the gate and the drain. The RESURF drift region length plays a major factor in achieving a low specific on-resistance in the device. The drift region should be minimised for optimum performance, since a higher L_{d2} will increase the substrate-assisted depletion and degrade the breakdown voltage of the structure.

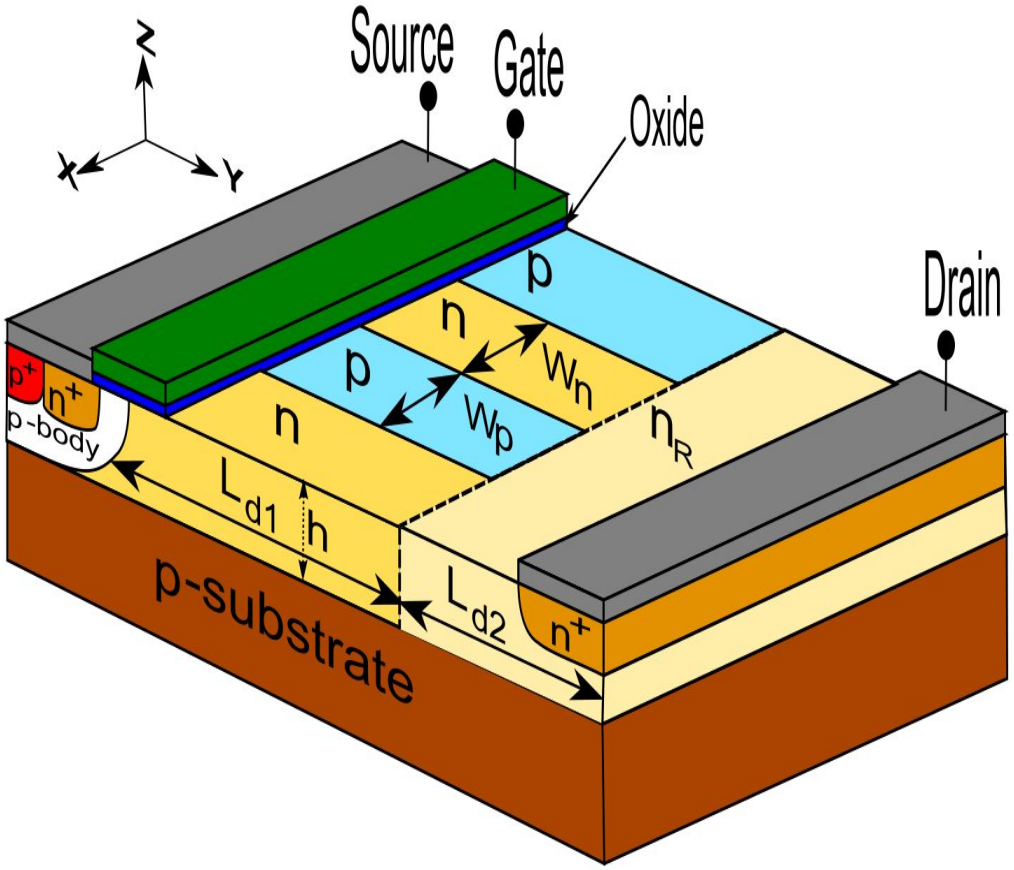

Figure 2.20: 3-D geometry of a super-junction (SJ) RESURF LDMOSFET.

In order to satisfy the RESURF condition as expressed by [88]:

$$n_n \cdot W_n = n_p \cdot W_p = n_R \cdot h = 2 \times 10^{12} \quad cm^{-2} \tag{2.40}$$

the doping concentrations and the drift length of the SJ layer and the RESURF should be optimised so that the whole drift region is full depleted. The fully depleted drift region will enhance a uniform electric field distribution in the device that will achieve a high breakdown voltage and a low specific on-resistance.

2.6 Trade-Off Between Breakdown Voltage and Specific On-Resistance

One of the main objective of SJ transistor architecture is to achieve the lowest specific on-resistance and the highest breakdown voltage. Since the breakdown voltage (BV) decreases with the increase in the doping concentration of the drift region, any reduction in the doping concentration of a drift region will result in an increase in the on-resistance. Therefore, there is a need to find an acceptable trade-off between the BV and the specific on-resistance ($R_{on,sp}$) of the device. Several transistor architecture designs have been proposed to improve the relationship between BV and $R_{on,sp}$. Figure 2.21 shows a relationship between the BV and the specific on-resistance of various conventional power MOSFETs in comparison with the latest SJ-LDMOS transistor. The theoretical limit given by a bulk silicon is also shown for comparison.

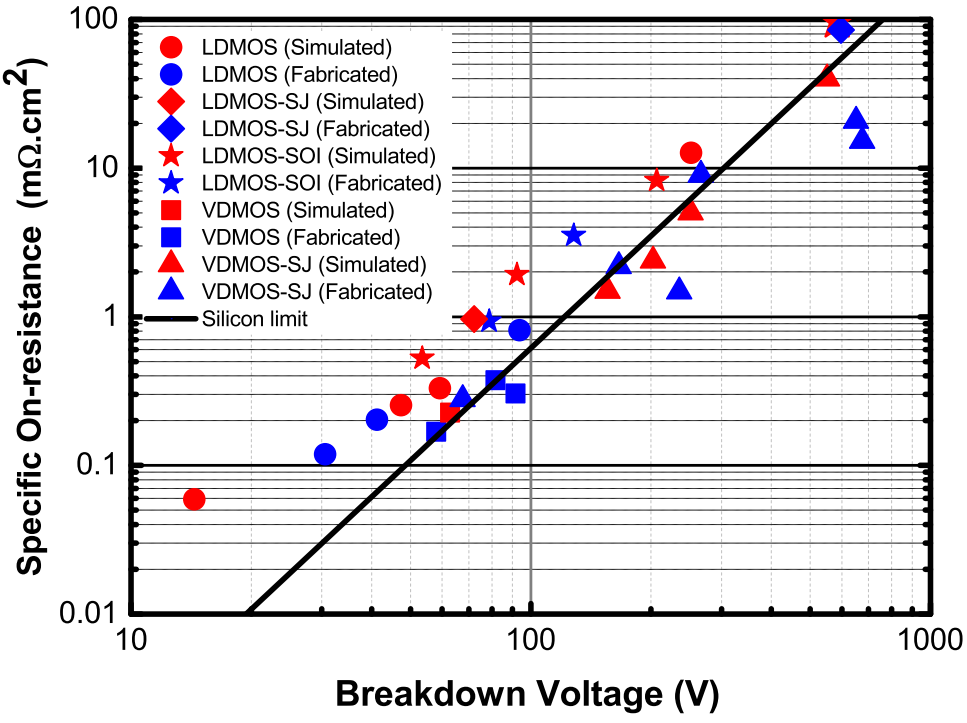

Figure 2.21: Specific on-resistance as a function of the breakdown voltage for different power MOSFETs technologies (simulated and fabricated) [89–98]. The theoretical limit given by a bulk silicon is also shown for comparison.

2.7 Trench Gate Power MOSFET

The trench gate power MOSFET has become known as one of the universal semiconductor devices, having be able to defied all logics that a MOSFET could only be fabricated effectively on the surface of a silicon wafer, and certainly not along the vertically etched trench side-wall [99]. Trench fabrication technology has grown over the years from a small scale venture to a large scale commercial enterprise with huge investments running into billion of dollars [99]. The trench gate MOSFET has been utilised for a wide-range of applications in the semiconductor technology such as the lateral trench MOSFETs and power integrated circuits [100], the trench IGBTs [101, 102], and the trench SJ MOSFETs [103–106].

2.7.1 Trench Gate Lateral Super-Junction (SJ) Power MOSFETs

The SJ concept has been employed to achieve a high BV and a low specific on-resistance. However, the implementation of the lateral SJ transistor technology for low voltage ($<$ 200 V) applications has not been attractive due to the fact that the channel resistance becomes comparable to the drift resistance at a low voltage ratings. Because a conventional planar gate SJ-LDMOSFET consists of a heavily doped alternating $n-$ and $p-$ pillars with the pillar widths of W_n and W_p in a SJ drift region length of L_d, a specific on-resistance ($R_{on,sp}$) (neglecting the built-in depletion region and assuming the on-resistance is dominated by the drift region) can be expressed as [37]:

$$R_{on,sp} = K \cdot L_d^2 \cdot \frac{W_n}{n_n \cdot h_{n-pillar}} \tag{2.41}$$

where

$$K = \frac{2}{q \cdot \mu_{ns}} \tag{2.42}$$

where n_n is the doping concentration of the $n-$ pillar, $h_{n-pillar}$ is the height of $n-$ pillar, μ_{ns} is the electron mobility, and q is the electronic charge. $R_{on,sp}$ in Equation (2.41) can be minimised by increasing the doping concentration of the $n-$pillar (n_n), reducing the $n-$pillar widths (W_n), or increasing the height ($h_{n-pillar}$).

Further, a narrowing of $n-$pillar width will lead to the space charge region within the SJ drift unit becoming similar to the built-in depletion region. Therefore, the only effective way of minimising the $R_{on,sp}$ is to increase the pillar height. However, it has been reported [104] that the specific on-resistance of a conventional SJ-LDMOS transistor barely decreases with increases in the pillar height because of a large concentration of electron current crowding at the top surface of the $n-$ pillar. This large current crowding at the top surface increases a channel resistance in the planar gate structure of the SJ-LDMOS transistor. Consequently, the $R_{on,sp}$ for a low voltage SJ device is strongly dependent on the channel resistance and not only on the doping concentration of the $n-$ pillar.

In order to overcome the dominance of the channel resistance in a low voltage SJ-LDMOS transistor, a non-planar gate structure has been suggested [104–106]. The non-planar gate SJ-LDMOS transistor uses an embedded trench gate to redistribute electron current crowding near the top surface of the $n-$ pillar and, subsequently, reduces the channel resistance in the device.

In Chapters 4 and 5, the design, optimisation and scaling of a complementary metal-oxide-semiconductor CMOS-compatible lateral super-junction multi-gate MOSFET (SJ-MGFET) based on a SOI technology will be examined as a preferred solution in alleviating the predominance of channel resistance during the application of a low voltage. Concomitantly, the relationship between the breakdown voltage and the specific on-resistance in the device is improved.

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Chapter 3

Simulation Methodology

3.1 Introduction

The device simulation has played a crucial role in the development of semiconductor technology in terms of design, optimisation, characterisation and, most importantly, providing an insights into the carrier transport mechanisms by studying phenomena that cannot be directly analysed on real devices. The simulation process involves the implementation of numerical procedures in solving equations related to the physical model chosen to describe transport process in a device. The complexity of the selected physical model and the related time consumption to solve the model are two-fold issues to be seriously considered when selecting the physically based simulation approach. However, the continuous improvement offering fast and powerful computational resources makes these limitations greatly reduced resulting in a more accurate, reliable and high-speed non-linear and linear solution techniques.

Silvaco Atlas is a commercial physically based simulator that allows analysis and modelling of 1-D, 2-D, and 3-D semiconductor devices based on approximation models of carrier transport derived from Schrödinger or Boltzmann equation, and self-consistently coupled to Poisson's equation [1]. The Atlas simulation tool is integrated with Virtual Wafer Fab (VWF) interactive tools for effective interactive run-time environment and scientific visualisation capabilities. This chapter provides insights into a drift-diffusion transport model used in this thesis; with the procedural hierarchy of 3-D simulation techniques applied in modelling of a non-planar lateral SJ multi-gate MOSFET (SJ-MGFET) [2].

3.2 Basic Semiconductor Equations

3.2.1 Gauss's Law

The Gauss's law states the relationship between charge density and the electric field within a closed surface. Assuming no time-dependent magnetic fields, the 1-D equation is given by [3–5]:

$$\frac{dE(x)}{dx} = \frac{\rho(x)}{\epsilon} \tag{3.1}$$

where $E(x)$ is the electric field, $\rho(x)$ is the charge density and ϵ is the permittivity. Applying integral form on the above equation, the $E(x)$ for 1-D charge distribution can be expressed as

$$E(x_2) - E(x_1) = \int_{x_1}^{x_2} \frac{\rho(x)}{\epsilon} dx \tag{3.2}$$

In a 3-D closed surface, the application of Gauss's law states the divergence of the electric field as [5]:

$$E(x, y, z) = \frac{\rho(x, y, z)}{\epsilon} \tag{3.3}$$

3.2.2 Poisson's Equation

The Poisson's equation gives the relationship between the electric potential and the charge density in any single point of the device. In a 1-D equation, the electric field can be defined as a negative gradient of the electric potential expressed as [5]:

$$-E(x) = \frac{d\phi(x)}{dx} \tag{3.4}$$

where $E(x)$ is the electric field and ϕ is the electric potential since the $E(x)$ flows from a higher potential point to a lower potential point. Applying integral form on Equation (3.4) gives the expression of electric potential as [5]:

$$\phi(x_2) - \phi(x_1) = -\int_{x_1}^{x_2} E(x) dx \tag{3.5}$$

Substituting the expression for $E(x)$ from Equation (3.4) into Equation (3.1), results in Poisson's equation given by:

$$\frac{d^2\phi(x)}{dx^2} = -\frac{\rho(x)}{\epsilon} \tag{3.6}$$

In a 3-D closed surface, the potential gradient can be expressed as:

$$\nabla \cdot \phi(x, y, z) = -E(x, y, z) \tag{3.7}$$

Expression (3.3) is substituted in to Equation (3.7) to acquire a general expression for Poisson's equation given by:

$$\nabla \cdot \phi(x, y, z) = -\frac{\rho(x, y, z)}{\epsilon} \tag{3.8}$$

3.2.3 Continuity Equation

The continuity equations can be derived from Maxwell's first equation by applying "div" and splitting the conduction current density into holes and electrons components, respectively. Neglecting the influence of charged defects, and assuming that all charges in the semiconductor, except the mobile carriers (electrons and holes), are not a function of time therefore [6]:

$$div(J_p + J_n) + q.\frac{\delta}{\delta t}(p - n) = 0 \tag{3.9}$$

where J_n and J_p are the electron and hole current densities, n and p are the electron and hole concentrations and q is the electronic charge. This result implies that sources and sinks of the total conduction current are completely compensated by the time variation of the mobile charge [6]. Obtaining two continuity equations will involve definition of any another quantity R in Equation (3.9). Thus:

$$div(J_n) - q.\frac{\delta n}{\delta t} = q.R \tag{3.10}$$

$$div(J_p) + q.\frac{\delta p}{\delta t} = -q.R \tag{3.11}$$

where R is the net generation or recombination of electrons and holes, which could be

positive (recombination) or negative (generation), respectively. The 3-D continuity equations for electrons and holes are expressed as [7]

$$\frac{\delta n}{\delta t} = \frac{1}{q}\left(\frac{\delta Jn}{\delta x}x + \frac{\delta Jn}{\delta y}y + \frac{\delta Jn}{\delta z}z\right) - R \tag{3.12}$$

$$\frac{\delta p}{\delta t} = -\frac{1}{q}\left(\frac{\delta Jp}{\delta x}x + \frac{\delta Jp}{\delta y}y + \frac{\delta Jp}{\delta z}z\right) - R \tag{3.13}$$

3.3 Drift-Diffusion Transport Model for Device 3-D

The Drift-Diffusion (DD) transport model was applied in most of the simulation works in this thesis. The DD transport model provides an excellent convergence with little or no computational cost. It is applicable for all technologically feasible devices, although, with the limitations of device structures well below micrometer range even the validity of DD can be substantially extended by various corrections (for example, quantum-mechanical confinement corrections). The solution of the DD model is based on the following set of equations: the current equations for electrons and holes [8–10], the continuity equation, and the Poisson's equation all given by [11]:

(1) Current equations

$$\begin{aligned} J_n &= qn\mu_n E + qD_n \nabla n, \\ J_p &= qp\mu_p E - qD_p \nabla p. \end{aligned} \tag{3.14}$$

where μ_n and μ_p are the electron and hole mobility, E is the electric field, and D_n and D_p are the diffusion coefficients of electrons and holes, respectively.

(2) Continuity equations

$$\begin{aligned} \frac{\delta n}{\delta t} &= \frac{1}{q}\nabla \cdot J_n + U_n, \\ \frac{\delta p}{\delta t} &= -\frac{1}{q}\nabla \cdot J_p + U_p. \end{aligned} \tag{3.15}$$

where U_n and U_p are the net generation-recombination rate.

(3) Poisson's equation

$$\nabla \cdot \epsilon \nabla V = -(p - n + N_D^+ - N_A^-) \tag{3.16}$$

where V is the electric potential, E is the applied electric field, and N_D^+ and N_A^- are the ionised donor and acceptor impurity densities.

The choice of using the DD transport model in the approach of modelling the 1 μm gate length SJ-MGFET is based on the following: (i) the dimensions of active region of the physical device on a micrometer scale, which permits an assumption of electron transport close to equilibrium (considering that the phenomena governing carrier transport depend on the characteristics as De Broglie wave-length, mean free path (MFP), and phase relaxation length (PRL) which are all related to dimensions of the physical device [12–15]); (ii) obtaining a solution for a 3-D device geometry with a simple, fast and robust transport model decribing studied properties of the physical device with no further increase in the computational costs.

3.4 Silvaco Technology Computer Aided Design

The advent of computer-aided simulations in the design of modern semiconductor technology has offered several advantages to implement complex mathematical models in physical device simulations. The computer-aided simulations can complement the experimental investigations of physical devices because the experiments can be very expensive and time consuming. Additionally, some specific variations in the design of devices can be technologically limited [6]. The technology computer aided design (TCAD) is the electronic design automation that models integrated circuit (IC) fabrication and device operation [5]. It follows a standard sequence that involves process, device and circuit simulation tools, respectively [11], in implementing an appropriate methods for device exploration, design, scaling, and optimisation.
The process simulation is an interface tool that involves modelling the mathematical operations of the physical effects of IC fabrication steps to a feasible technologically design, whereas, the device simulation accounts for numerical analysis and operation of the device using physical models. Device simulation can also provide parameters that are needed to generate compact behavioural models when coupled with process and circuit simulations. The circuit simulation refers to simulation that includes elements simulated with device simulation and compact circuit models. It obtains solution by combining different levels of abstraction to model circuits in which compact models for such devices are unavailable or sufficiently defined.

The Silvaco software is an interface tool to handle process, device and circuit simulations data using Athena, Atlas, and MixedMode simulators, respectively [1]. In this thesis, Silvaco Atlas is used in the modelling, scaling and optimisation of a non-planar lateral Super-Junction Multi-Gate MOSFET (SJ-MGFET). The Atlas device simulator is capable of performing 1-D, 2-D and 3-D device simulations of semiconductor devices. It is also embedded with Virtual Wafer Fab (VWF) Interactive Tools such as DeckBuild, TonyPlot, TonyPlot3D, DevEdit, DevEdit3D, MaskViews, and Optimizer for effective capability as a one comprehensive device simulation package. The basic operational features of the Atlas device simulator are described in the following sections.

3.4.1 Meshing

The concept of having a good mesh specification poses a greater challenges in a modelling of semiconductor device structure. For accurate description of the device geometry, a mesh definition plays a crucial role in specifying nodes in a device structure for numerical simulations. The computational time required to derive a solution of a linear system resulting from a discretisation of partial differential equations on a mesh with N nodes is proportional to N^{β}, where β has a range from $2-3$ [1]. A mesh size should be smaller than Debye length in order to resolve charge variations in space [11]. A poor mesh will leads to convergence failure, inaccurate simulation results and increase in computational time. A refined mesh should be specifying at the channel junctions, electrodes, and any region where there is high electric fields, abrupt doping or concentration profile. Mesh configuration should be fully optimised for numerical efficiency. The software employs finites element method by subdividing the simulation domain into smaller regions usually of triangular (or tetrahedral) shape and estimates the dependent variable in the subregion using polynomial approximation [6]. The Silvaco Atlas simulator allows mesh specification in 2-D and 3-D rectangular and cylindrical geometries. However, it cannot combine the two mesh specifications together as a single file structure. Mesh 2-D and 3-D editors, DevEdit and DevEdit3D, can be interfaced with a simulator to mesh rectangular and cylindrical structures. Specifying structure in rectangular 2-D geometry involves using the X and Y mesh spacings, while for cylindrical 2-D, the radial and angular mesh spacings should be defined.

3.4.1.1 Defining a 3-D Structure in Rectangular and Cylindrical Parameters

The software allows mesh definition in 3-D geometry for both rectangular and cylindrical structures. To activate a 3-D mesh generation, "MESH THREE.D" and "MESH THREE.D CYLINDRICAL" command has to be defined at the beginning of the input file for rectangular and cylindrical geometries. The command syntax for a 3-D geometry is an extension of 2-D syntax; for 3-D rectangular parameter, X, Y and Z coordinates should be specified while radius, angle and Z directions are defined for 3-D cylindrical parameter [1]. Figure 3.1 shows the 3-D geometry of the investigated 1 μm gate length non-planar lateral SJ-MGFET [2].

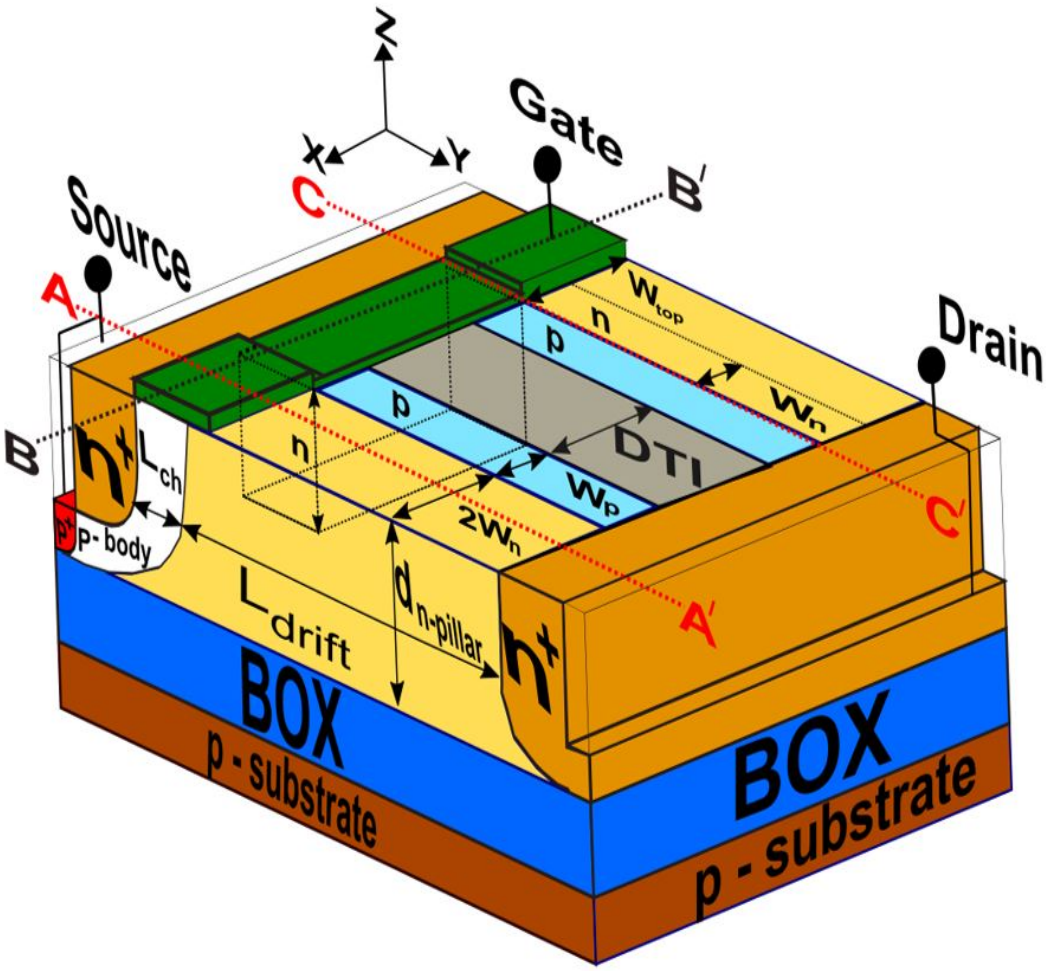


Figure 3.1: 3-D geometry of the investigated 1μm gate length SJ-MGFET having a width of 200 μm and a drift length of 3.5 μm.

3.4.2 Material and Model Specifications for 3-D Structure

Solid materials in Atlas are classified into three basic group namely: semiconductors, insulators and conductors. The command syntax "MATERIAL" allows user to specify classes and composition of the component into region in the device structure. Material basic properties such as band gap, electron affinity, density of states, permittivity and saturation velocities are specified in the code. Compound material can be defined in addition to a single material by specifying the composition dependent material parameters like dielectric constants, and saturation velocities. Boundary conditions such as Ohmic contacts, Schottky contacts, insulated contacts, and Neumann (reflective) boundary condition can be specified using syntax "CONTACT" in the code. Also, X, Y and Z coordinates (rectangular geometry), and radius, angle and Z directions (cylindrical) should be specified in each command syntax statement for 3-D structure. Validating a model for effective device simulation in a certain domain is costly, time consuming [16]. The inclusion of experimental data is essential for a valid model verification in the simulation. The user needs to verified the appropriate model by calibrating the simulation with experimental data. The command syntax "MODEL" enables definition of transport models such as dependence of mobility on electric field (low or high), carrier statistics, carrier generation-recombination, carrier temperature, tunnelling and carrier injection for each material statement. To define impact ionization model in the simulation, the command syntax "IMPACT" should be specified in the code. The software allows combination of two or more models for effective device simulation depending on the model compatibility chart as stated by [1]. All the physical models available for 3-D device are extension of 2-D command syntax.

3.4.3 Numerical Methods for Device 3-D Simulation

Several numerical solution techniques are provided in Atlas in computing the solutions of de-coupled, fully coupled linear and non-linear partial differential equations arising from a chosen transport model. The numerical iteration techniques are Gummel, Newton and Block iterations. The Gummel's method solves for each unknown variable in the equation while keeping the other variables constant, repeating the sequence until convergence is achieved. This method converges relatively slowly, but tolerate poor initial guesses. The Gummel method is failing when using lumped

elements or user defined current boundary conditions [1]. The Newton's method is a coupled process that solves the equations simultaneously through application of the Newton-Raphson method for determining the roots of a general non-linear equation [11]. This method is fast because it can start a very close to a true solution, and decreases quadratically from one iteration to the other. Newton's method is the default solver for DD simulations in Atlas. In practice, the Gummel and Newton methods can be combined, by taking advantage of the fast initial error reduction in Gummel's method, coupled with faster and better convergence capability in Newton's method. Block's method computes subgroups of equations in various sequences and typically used to solve a lattice heating model or energy balance equation transport model. However, there is a lot of discrepancy between the default numerical methods applied in 2-D and 3-D Atlas. The 3-D Atlas does not support the "BLOCK" iteration with respect to non-linear iteration techniques [1]. The "GUMMEL" and "NEWTON" iterations are supported for 3-D device simulations, while "GUMMEL", "NEWTON" and "BLOCK" are available for 2-D device simulations. The command syntax "METHOD" statement should be specified in the code to activate any numerical iteration techniques.

3.4.3.1 DC and Transient Solutions

Atlas provides two methods for solving DC linear sub-problems; namely direct and iterative methods [1]. The direct method is the default solver for 2-D simulations, whereas the iterative method is the default for 3-D simulations. The 3-D iterative solver consists of two linear iterative solutions. They are "ILUCGS" (incomplete lower-upper decomposition conjugate gradient system) and "BICGST" (bi-conjugate gradient stabilized). Experimental tests have shown that "ILUCGS" provides more stable current implementation than "BICGST", thus it is defined as the default iterative solver in 3-D [1]. Iterative solver can be define in the code using command syntax "METHOD" statement. Transient solutions can be computed for piecewise-linear, exponential, and sinusoidal bias functions in Atlas. These solutions are specified when a time dependent test or response is required in the device simulation. The command syntax "TSTOP", "TSTEP" and "RAMPTIME" statements should be specified to obtain transient solutions for a linear ramp.

3.4.3.2 Small-Signal AC Solution

The software also provides solution for obtaining a small signal AC analysis. Atlas computes two types of AC simulation methods; namely single and ramped frequencies. In single frequency, the solution is obtained during a DC ramp with a predetermined AC signal whereas, for ramped frequency, a linear ramp of range of frequency is applied at a DC bias point to obtain the AC signal [1].

3.4.3.3 Numerical Methods for SOI

Device simulations of SOI structure require a different choice of numerical methods due its complexity. Since the potential in the *p*-body (channel) region of SOI body has no direct contact with any electrode; a numerical convergence problem occurs when the device is biased during impact ionisation. The problem is more pronounced in isothermal DD simulations. The "GUMMEL" and "NEWTON" methods should be combined in the input file to overcome this convergence problem of poor initial guess in the command syntax "METHOD" statement.

3.4.4 Reading Results from 3-D Device Simulation

The TonyPlot and TonyPlot3D are graphical tools that enable scientific visualisation in 2-D and 3-D Atlas simulations. They can operate as stand-alone or incorporated with other VWF Interactive Tools, such as DeckBuild, or Subsystem Power Distribution Box (SPDB) [17, 18]. In 3-D Atlas, the solution log files can be plotted using the same TonyPlot as for 2-D Atlas since the are essentially also 2-D data. However, there is a disparity in units of current obtained in the two geometries. The currents are solved in Amper unit for 3-D, whereas, they are stored as Amper/micrometer unit in 2-D [1]. Structure files obtained in 3-D Atlas simulations require TonyPlot3D to be viewed [18]. Atlas also provides an option in TonyPlot3D, that allow files to be extracted, exported and save in TonyPlot's structure file. This will permits a 1-D cut-line through the simulate device structure, in order to visualise some quantities such as meshing, acceptor/donor concentration, current density, electron/hole concentration, electric field, net-doping, absolute net-doping, etc.

3.5 Breakdown Simulation in 3-D Device

A breakdown voltage in Atlas device simulations is determined when the current slightly increases above the flat shaped pre-breakdown value by a small voltage increment. To obtain a solution in a breakdown simulation can be quite challenging because a high increase in current by orders of magnitude for a small voltage bias may lead to convergence problems. The software provides some techniques that make it easy to trace the avalanche breakdown curve to the highest current values. These techniques are current boundary conditions (CDC) and compliance parameter. In the CDC, the voltages are forced while the currents are being measured by the command syntax "SOLVE" statement, whereas the compliance parameter involves limiting the current or voltage on the electrode during a device simulation. The physical models available for 3-D device breakdown simulations are compatible with 2-D simulations. In 3-D SOI MOSFET breakdown simulation, experience plays a crucial role in overcoming convergence problem during simulation. In the simulations, a denser vertical mesh is applied in the p-body under the gate and a tight lateral mesh spacing at the n-drift/drain junction in order obtain a high peak of electric field during impact ionisation as well as improving the avalanche capability during charge balanced condition. The command syntax "IMPACT" statement should be specified for impact ionisation simulation.

3.6 Electro-Thermal Modelling in 3-D Device

The effect of lattice temperature in the SJ-MGFET is investigated in this thesis aiming at providing an additional thermal conductive path in the device and to improve uniform distribution of electric field during avalanche breakdown. In the electro-thermal simulations, the effect of lattice self-heating on the mobility degradation in the device is examined due to poor thermal conductivity of silicon dioxide of the SOI technology. Atlas uses Wachutka's thermodynamic model [19] to implement lattice heat flow and general thermal environments in a simulation. This model computes the four equations consisting of the Joule heating, heating, and cooling due to carrier generation and recombination, and the Peltier and Thomson effects in the simulated device as given by [19]. In 3-D Atlas, the "thermal3D" simulation model is specified to account for the modelling of lattice temperature in time and space

invariant in the structure. This model iterative solver considers transport model equations and self-consistently coupled with a lattice heat flow equation. The Atlas simulation provides a solution to the equations of lattice heat flow as expressed by [1]:

$$\rho C_p \frac{\delta T_L}{\delta t} = \nabla(k\ \nabla T_L) + H \tag{3.17}$$

where C_p is the specific heat, ρ is the density of the material, k is the thermal conductivity, H is the heat generation and T_L is the local lattice temperature.

3.7 Calibrating SJ-MGFET Models

The calibration of the SJ-MGFET requires a simplified procedures from a 2-D silicon-on-insulator (SOI) MOSFET structure to a 3-D SOI SJ-MGFET geometry. The procedural steps of modelling a device with the Silvaco Atlas simulator [1] is shown in Figure 3.2.

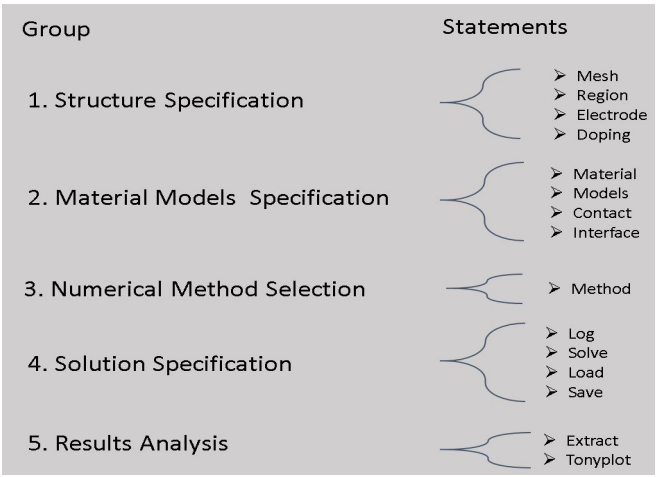


Figure 3.2: Atlas command groups with the primary statements.

3.7.1 Modelling a 2-D Silicon-on-Insulator (SOI) LDMOS

The following steps can be followed in modelling a LDMOS (Lateral Double Diffused MOSFETs) fabricated on a silicon-on-insulator (SOI) as shown in Figure 3.3. In addition, Figure 3.3 depicts the net doping concentration, simulations of the transfer (I_D-V_{GS}) and the output (I_{D}-V_{DS}) characteristics with the electric field distribution

during the off-state in the device. When using a commercial simulator Atlas by Silvaco, one would perform the following steps:

- Run Atlas in the DeckBuild by starting with the command: go atlas

- The structure can be defined using mesh specification as follow:
  Mesh space.mult = (value)
  x.mesh location = (0.0) spacing = (0.0)
  y.mesh location = (0.0) spacing = (0.0)
  (The value of x.mesh and y.mesh should be defined from (0.0, 0.0) to (6.5, 6.1) with appropriate spacing, denser mesh can be specified for region with abrupt junction, under gate electrode and interface between metal/oxide/semiconductor contact. For easy referencing the structure can be subdivided into regions such as source, p-body, n-drift and drain regions.)

- The structure can be specified into region with the appropriate material type and position parameters in the geometry:
  region num=1 x.min=0.25 x.max=6.25 y.min=0 y.max=3.6 silicon
  region num=2 x.min=0.0 x.max=6.5 y.min=3.6 y.max=5.6 oxide
  region num=3 x.min=0.0 x.max=6.5 y.min=5.6 y.max=6.1 silicon
  region num=4 x.min=1.0 x.max=2.0 y.min=-0.03 y.max=0 oxide
  region num=5 x.min=0.0 x.max=0.25 y.min=3.0 y.max=3.6 silicon
  region num=6 x.min=6.25 x.max=6.5 y.min=3.0 y.max=3.6 silicon

- The electrodes specification can be defined as electrode name = (name) position parameters:
  electrode name=gate x.min=1.0 x.max=2.0 y.min=-0.2 y.max=-0.03
  electrode name=source x.min=0.25 x.max=1.0 y.min=0.0 y.max=0.0
  electrode name=drain x.min=5.0 x.max=6.25 y.min=0.0 y.max=0.0

- The doping of the structure is specified with referencing to region number, analytical doping profiles such as uniform, Gaussian, or complementary error function can defined with the dopant type, dose and position parameters:
  doping uniform conc=1e15 p.type reg=3
  doping gauss n.type conc=1e20 char=0.1 lat.char=0.1 reg=1 x.r=0.75 y.min=0 y.max=2.80
  doping gauss n.type conc=1e20 char=0.1 lat.char=0.1 reg=1 x.l=5.05 y.min=0

y.max=3.275
doping gauss n.type conc=1e15 char=0.1 lat.char=0.2 reg=1 x.r=4.98 x.l=1.5 y.min=0 y.max=3.4
doping gauss p.type conc=2.5e17 char=0.15 lat.char=0.1 reg=1 x.r=1.39 x.l=1.05 y.min=0 y.max=3.35
doping gauss p.type conc=2.5e17 char=0.15 lat.char=0.1 reg=1 x.min=0.25 x.max=1.0 y.min=2.85 y.max=3.35
doping uniform conc=1e19 p.type reg=5
doping gauss n.type conc=1e20 char=0.1 lat.char=0.1 reg=6 y.min=3.0 y.max=3.275
doping gauss n.type conc=1e15 char=0.2 lat.char=0.1 reg=1 x.r=5.8 x.l=0.2 y.min=2.5 y.max=3.6

- Save and import file as structure outfile = (output filename.str);
  save outf=SOI-LDMOS.str

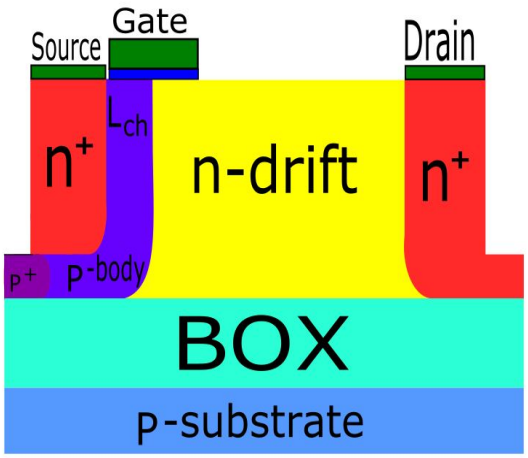
- The next step is to specified the model(s), contact electrode, and interface charge between the metal-oxide-semiconductor contact:
  models fldmob, srh print (DD model)
  impact selb (impact ionisation model)
  contact name=gate n.poly
  interface qf=3e10
  (The choice of model depends on the material, structure size and type of simulation.)

- Numerical solver is selection for the simulation using solve statement:
  solve init
  method gummel newton trap maxtraps=10 climit=1e-4 ir.tol=1e-35 ix.tol=1.e-35

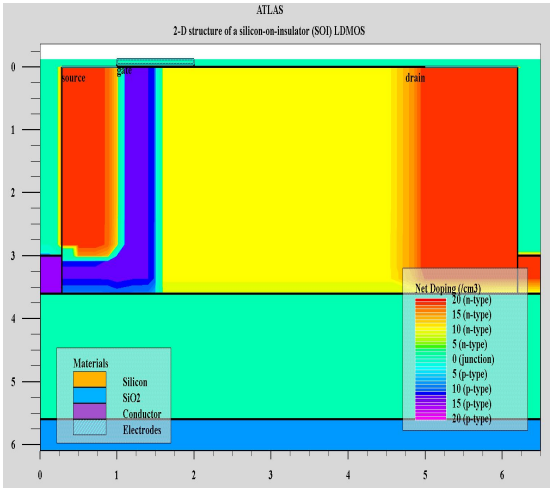
- The solve, load, and save statements should be specified after numerical solver:

- The results analysis is using extract, tonyplot log and structure files:
  tonyplot SOI-LDMOS.log
  tonyplot SOI-LDMOS.str

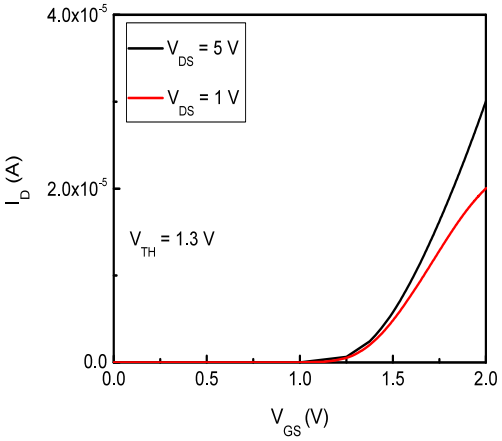
- To quit/end the simulation type the command: quit.



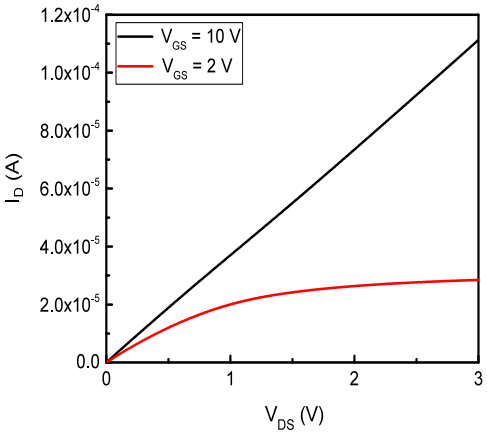
(a) 2-D structure of a SOI-LDMOS.



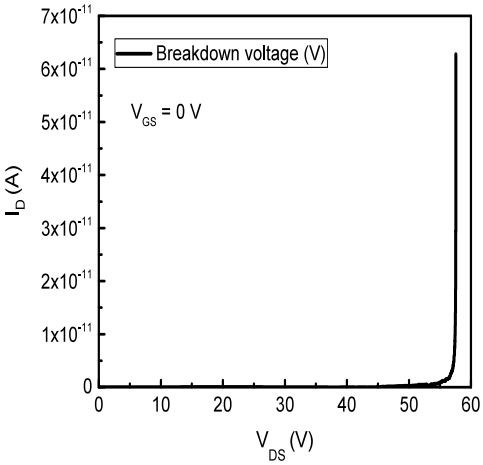
(b) Net doping concentration in the device.



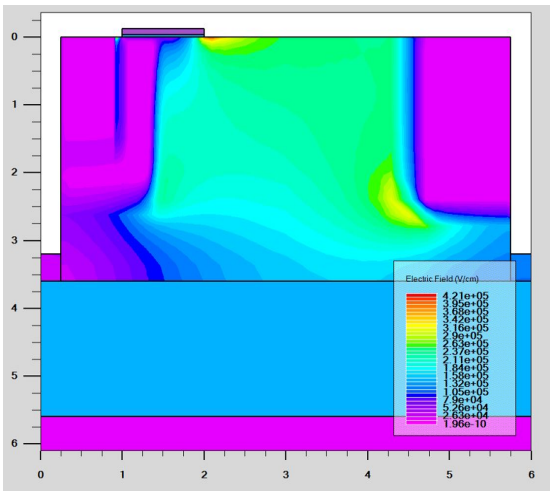
(c) I_D-V_{GS} at low and high drain biases.



(d) I_D-V_{DS} with a drift length of 3.5 μm.



(e) I_D-V_{DS} at the breakdown voltage during the device off-state.



(f) Electric field distribution at BV.

Figure 3.3: A 2-D structure of a SOI LDMOS with the transfer and output characteristics having a breakdown voltage of 58 V during the device off-state.

3.7.2 3-D Device Simulations of the SJ-MGFET

A model of the 1 μm gate length SJ-MGFET is calibrated to experimental characteristics of a non-planar lateral SJ multi-gate MOSFET (SJ-MGFET) fabricated within a silicon-on-insulator (SOI) technology [20] by reproducing its transfer (I_{D}-V_{GS}) characteristics. The micrometer scale of the device dimensions implies that a drift-diffusion (DD) transport approach will be sufficient to describe carrier transport process in the device. The DD carrier transport model is carried out with different doping profiles in the SJ drift region of the device. The initial doping concentration of the n-pillar (n_n) is calculated from the expression given by [21]:

$$n_n = 1.41 \times 10^{12} \cdot \lambda^{7/6} \cdot \omega^{(-7/6)} \quad (cm^{-3}) \tag{3.18}$$

where ω is the width of the n/p pillar of SJ device ($\omega = W_n = W_p$) and λ is the optimal doping coefficient ($0 < \lambda < 1$) for vertical or lateral SJ device which is $\frac{1}{2}$ or $\frac{1}{3}$, respectively. Equation (3.18) provides a value of $n_n = 7.4{\times}10^{16}$ cm^{-3}. A charge balanced simulation is carried out by varying the doping concentration of the p-pillar (n_p) while keeping the n_n constant until a maximum breakdown voltage is achieved. The Silvaco 3-D Atlas simulator is used to design the device geometry and doping profile in order to achieve optimal device performance in sub-100 V power applications. The carrier mobility is simulated using analytic low-field model (ANALYTIC), and parallel electric field dependence model (FLDMOB). Shockley-Read-Hall (SRH) model is used for carrier generation-recombination process in the simulated device, while Selberherr model is specified for the impact ionization process during off-state simulation. The device doping profile is assume to be a gaussian doping profile specified between the source/p-body and the p-body/drain to minimise and prevents short-channel effects (SCEs). A heavily doped n^+ polysilicon gate electrode is specified with a work function of 4.12 eV defined.

Figure 3.4 shows the comparison of the I_{D}-V_{GS} of the experimental and the simulated SJ-MGFET at a drain bias (V_{DS}) of 0.1 V. The simulation in Figure 3.4 is carried out using the analytic low-field (ANALYTIC), and parallel electric field dependence (FLDMOB) mobility model depicting a good agreement with the experimental characteristics. The data validation is carried out at a $V_{\mathrm{DS}} = 0.1\ V$ in order to have a fair comparison with the experimental behaviour. The device simulations at elevated drain bias is investigated and analysed in Chapter 4.

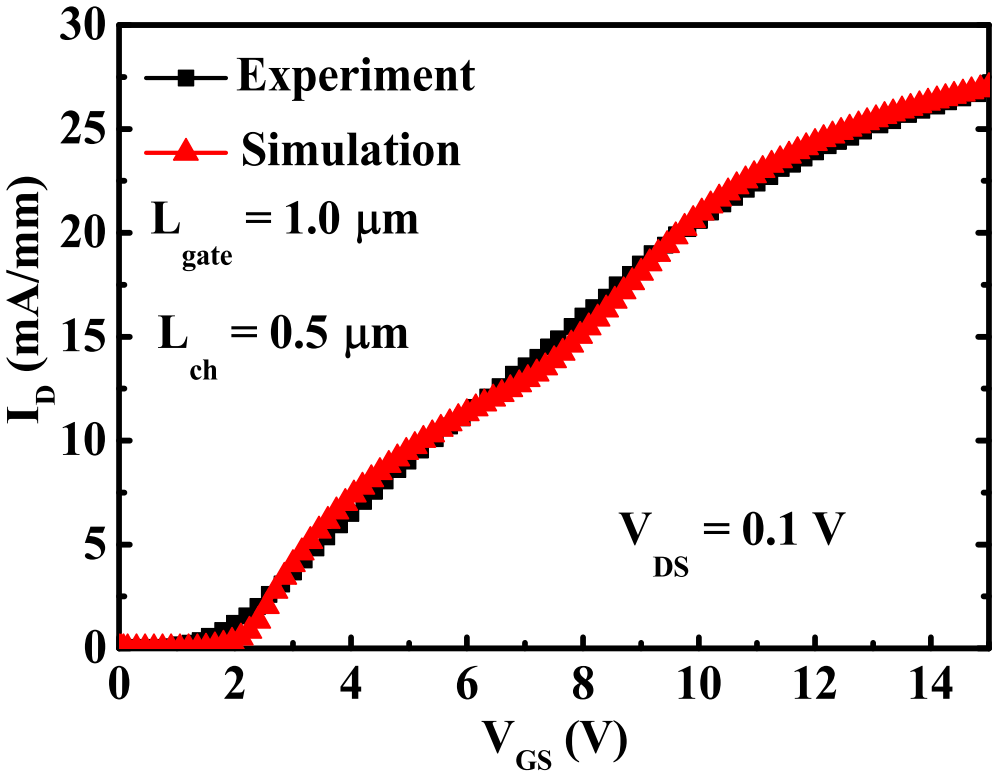


Figure 3.4: Calibrated transfer (I_{D}-V_{GS}) characteristics of the SJ-MGFET with the experimental data at $V_{\mathrm{DS}} = 0.1\ V$ with $L_{\mathrm{drift}} = 3.5\ \mu m$, $W_{\mathrm{side}} = 2.7\ \mu m$, and $W = 200\ \mu m$.

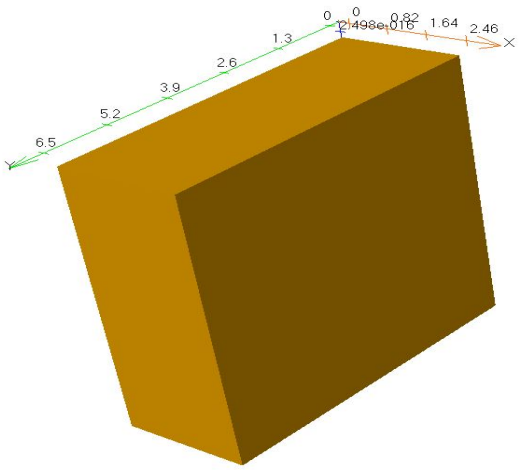
3.7.3 Simulation Flowchart for Modelling of the SJ-MGFET

The simulation is carried out with procedural steps ranging from a specification of the device mesh structure to a grid refinement. In order to avoids convergence problem and reduces computational time, a denser mesh is applied at channel, material boundaries, and $p-n$ junctions in the device geometry. The 3-D SJ-MGFET structure is split into various regions with the electrodes, materials and doping profile specified in each region.

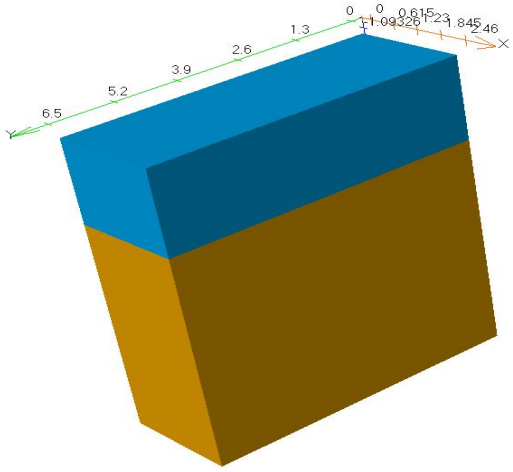
Table 3.1 shows the physical parameters of the SJ-MGFET geometry used for the device simulations. Figure 3.5 shows a simplified simulation flowchart of the SJ-MGFET while Figure 3.6 depicts the net doping concentration (cm^{-3}) profile of the device structure.

Table 3.1: The Physical Parameters for Device Simulations of the SJ-MGFET.

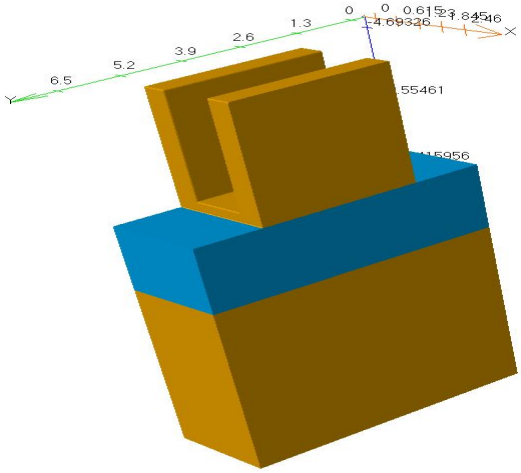
Parameter	Value
Gate length, L_{gate} (μm)	1.0, 0.5, 0.25
Gate oxide thickness (nm)	35, 18, 9
Channel length, L_{ch} (μm)	0.5, 0.25, 0.125
SOI layer thickness (μm)	3.6
SJ drift region length, L_{drift} (μm)	2.5, 3.5, 4.75, 6.0 and 7.5
n-pillar width, $2.W_n$ (μm)	0.6
n-pillar doping concentration, n_n (cm^{-3})	7.4×10^{16}
p-pillar width, W_p (μm)	0.3
p-pillar doping concentration (cm^{-3})	1.55×10^{17}
p-substrate thickness (μm)	5.0
p-substrate doping concentration (cm^{-3})	1.0×10^{15}
p-body doping concentration (cm^{-3})	2.5×10^{17}, 1.0×10^{18}, 1.0×10^{19}
p^+ sinker doping concentration (cm^{-3})	1.0×10^{19}
Buried oxide thickness (μm)	2.0
Top channel surface width, W_{top} (μm)	0.6
Side channel width, W_{side} (μm)	2.7
n^+ source/drain doping concentration (cm^{-3})	1.0×10^{20}



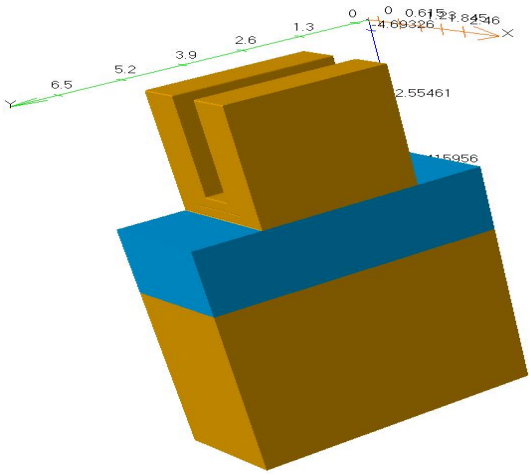
(a) Formation of the active p-substrate layer underlay in a 3-D device domain.



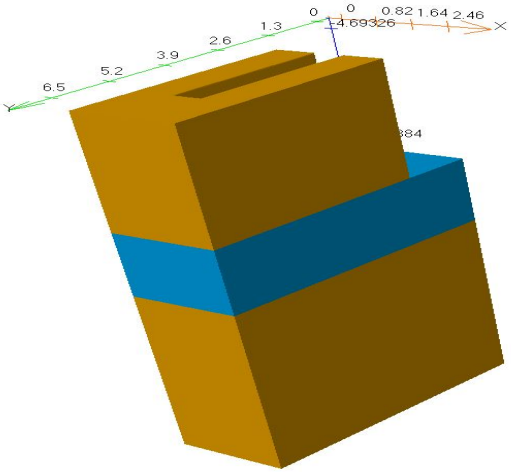
(b) Buried oxide (BOX) deposited on the p-substrate layer.



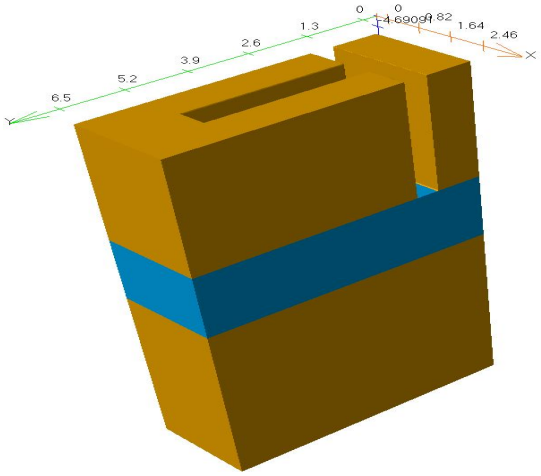
(c) U-shaped n-pillar formed on the BOX in a 3-D device domain.



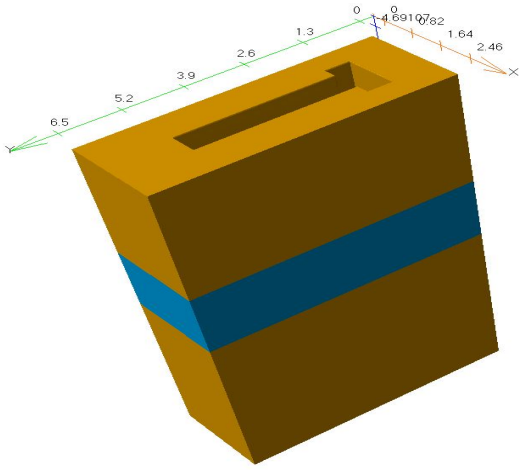
(d) SJ drift region of n/p-pillars formed on the buried oxide layer.



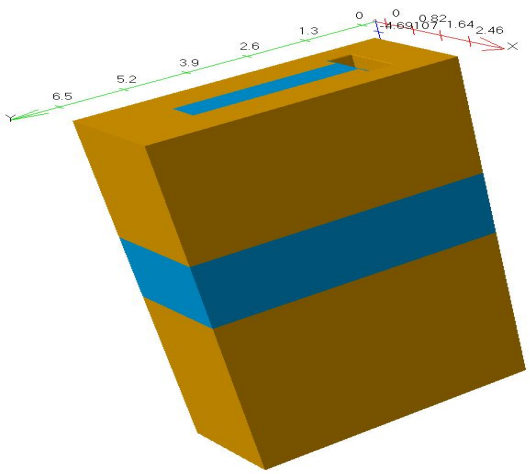
(e) Modelling of the drain contact on the BOX in a 3-D device domain.



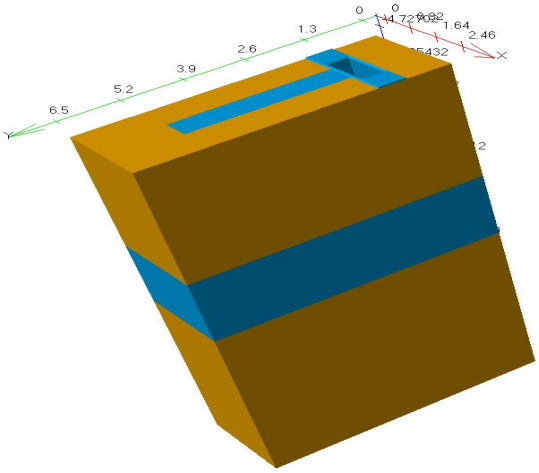
(f) Formation of the source contact on the BOX in a 3-D device domain.



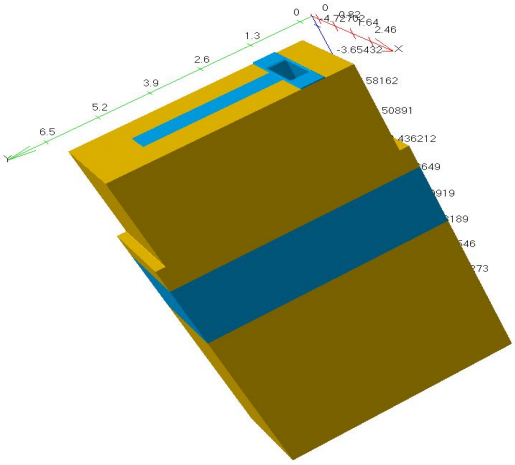
(g) *p*-body contact formation in a 3-D device domain.



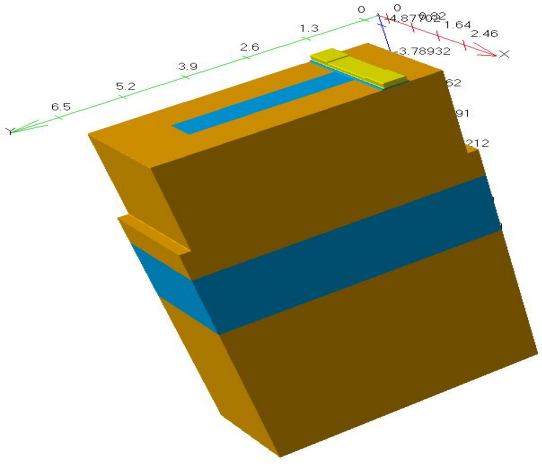
(h) Filling the deep trench isolation (DTI) with a silicon dioxide.



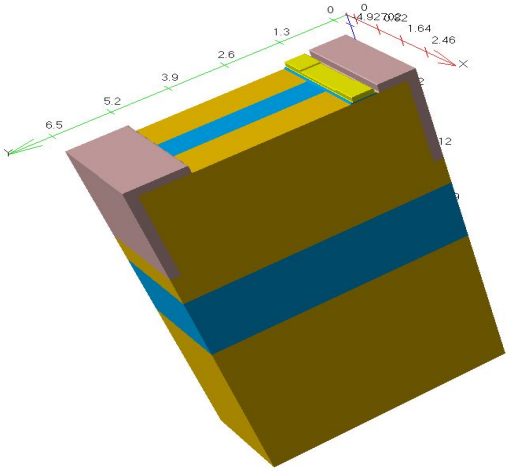
(i) Gate oxide layer in the embedded trench-gate structure.



(j) Deep trench etching at the source and drain side contacts in a 3-D device domain.



(k) Formation of the polysilicon embedded trench-gate in a 3-D device domain.



(l) Metallisation of the source and drain contacts.

Figure 3.5: A Flowchart for the Device Simulation of the SJ-MGFET

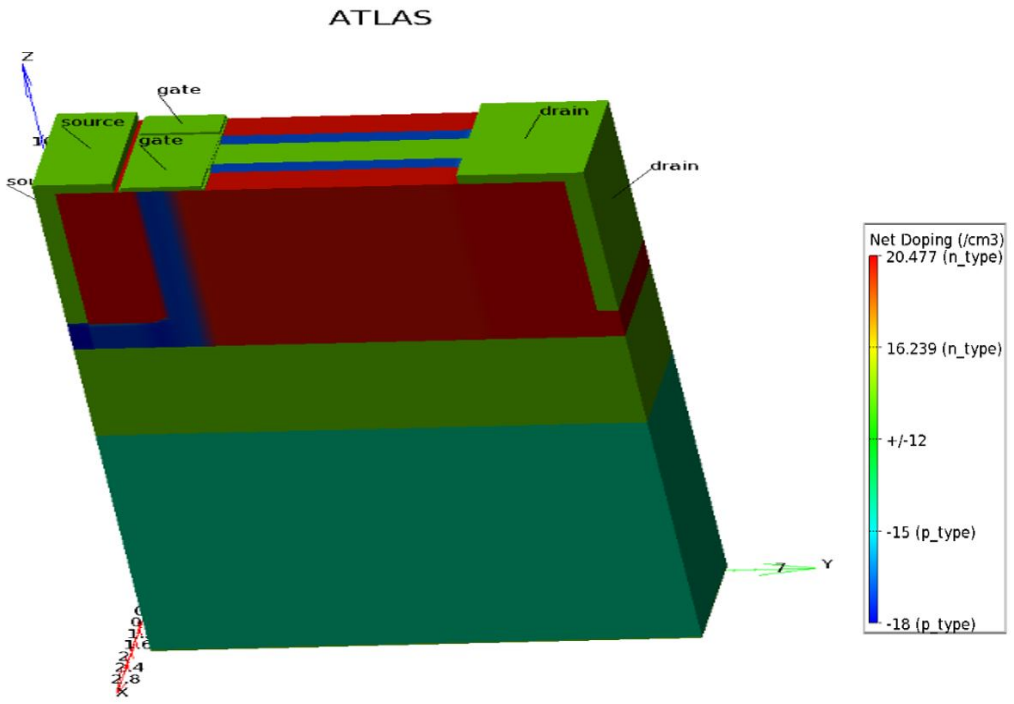


Figure 3.6: Net doping concentration (cm^{-3}) profile of the device structure.

3.8 Conclusion

In this chapter, detail description of how the Silvaco Atlas commercial device simulator can perform predictive analysis of electrical characteristics of a physical device with selected carrier transport models and obtain a numerical solution in a 2-D or 3-D structure is explained. The choice of the drift-diffusion transport model in modelling of semiconductor devices have been argued by the dimensions of the investigated device and by a need to have full 3-D device domain considered. In addition, the choice of the drift-diffusion transport model is driven by a need to simulate the 3-D device under a very large applied bias with an electro-thermal model which accounts for lattice self-heating effects by considering carrier transport of electrons and holes self-consistently coupled with thermal model. Emphasise has been made on the importance of obtaining a solution during impact ionisation modelling aiming at improving device avalanche capability and the need for effective calibration technique in achieving the best match between the experimental I_{D}-V_{GS} characteristics and the simulated characteristics of a device. Conclusively, the procedures and techniques in Silvaco Atlas (2-D and 3-D) device simulation software with its predictive and insightful capabilities as an effective tool for semiconductor technology development is presented.

3.9 References

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Chapter 4

Optimisation of Lateral Super-Junction Multi-Gate MOSFET (SJ-MGFET) for High Drive Current and Low Specific On-Resistance in Sub - 100 V Applications

4.1 Chapter Summary and Original Contributions

The LDMOS (Lateral Double Diffused MOSFETs) technology based on super-junction (SJ) design has been widely employed for various voltage applications such as domestic and office electronics appliances, automotive, military, and industrial control [1]. The super-junction (SJ) power MOSFET has shown a significant improvement in the trade-off relationship between the breakdown voltage (BV) and the specific on-resistance ($R_{on,sp}$). This is improvement is achieved with a heavily doped alternating n– and p– pillars in the drift region because the SJ design benefits from charge-compensation between these alternating n–type and p–type regions. During the off-state when the n-pillars are fully depleted, the vertical electric field component is a function of the lateral position in the drift region. In order to achieve a high breakdown voltage, the depth of the columns is increased without decreasing the doping concentration [1, 2]. Considering that an optimal doping concentration is set for a specific breakdown voltage, the n-pillar doping concentration can be increased to be inversely proportional to the pillar width resulting in a reduction of the on-resistance. This n-pillar doping concentration increase will subsequently lead

to a linear relationship between the BV and $R_{on,sp}$ [2]. However, the adaptation of lateral SJ transistor technology for low voltage (<200 V) applications has not been successful due to the fact that the channel resistance in a lateral SJ design becomes comparable to the drift region resistance at low voltage ratings. This is as a result of the minimum pillar width in the SJ drift region becoming similar to the built-in depletion region. On-resistance of the minimum pillar width cannot be further reduced and design variations of the SJ transistor are thus very limited [3, 4].
In this work, the potential of a non-planar SJ silicon MOSFET technology to be used as integrated power transistor with applications in power switching and amplifiers using physically based 3-D TCAD simulations [5] is explored. The experimental characteristics of the non-planar SJ multi-gate MOSFET (SJ-MGFET) fabricated within a silicon-on-insulator (SOI) technology [6] is analysed by reproducing its I-V characteristics and the breakdown voltage . The original contributions are as follows:

- The application of 3-D Atlas simulations to investigate variation in the device architecture and improve device performance by optimising doping profile under charge imbalance principle in the SJ unit.

- An investigation of the avalanche capability of the simulated SJ-MGFET during off-state aiming at achieving a uniform electric field in the drift region by a redistribution of electron current crowding near the top of n-pillar SJ unit.

- Using drift-diffusion (DD) transport models self-consistently coupled with electro-thermal model to simulate and optimise device design in order to mitigate the effect of lattice self-heating during the device on-state operations.

- C-V analysis of the optimised SJ-MGFET with a small AC signal model thereby quantifying the capacitance (C) and the conductance (G) effects, respectively, to allow further optimisation of the structure to meet different applications.

- An improvement in the figures-of-merit (FoM) between the BV and the specific on-resistance ($R_{on,sp}$) of the optimised SJ-MGFET device.

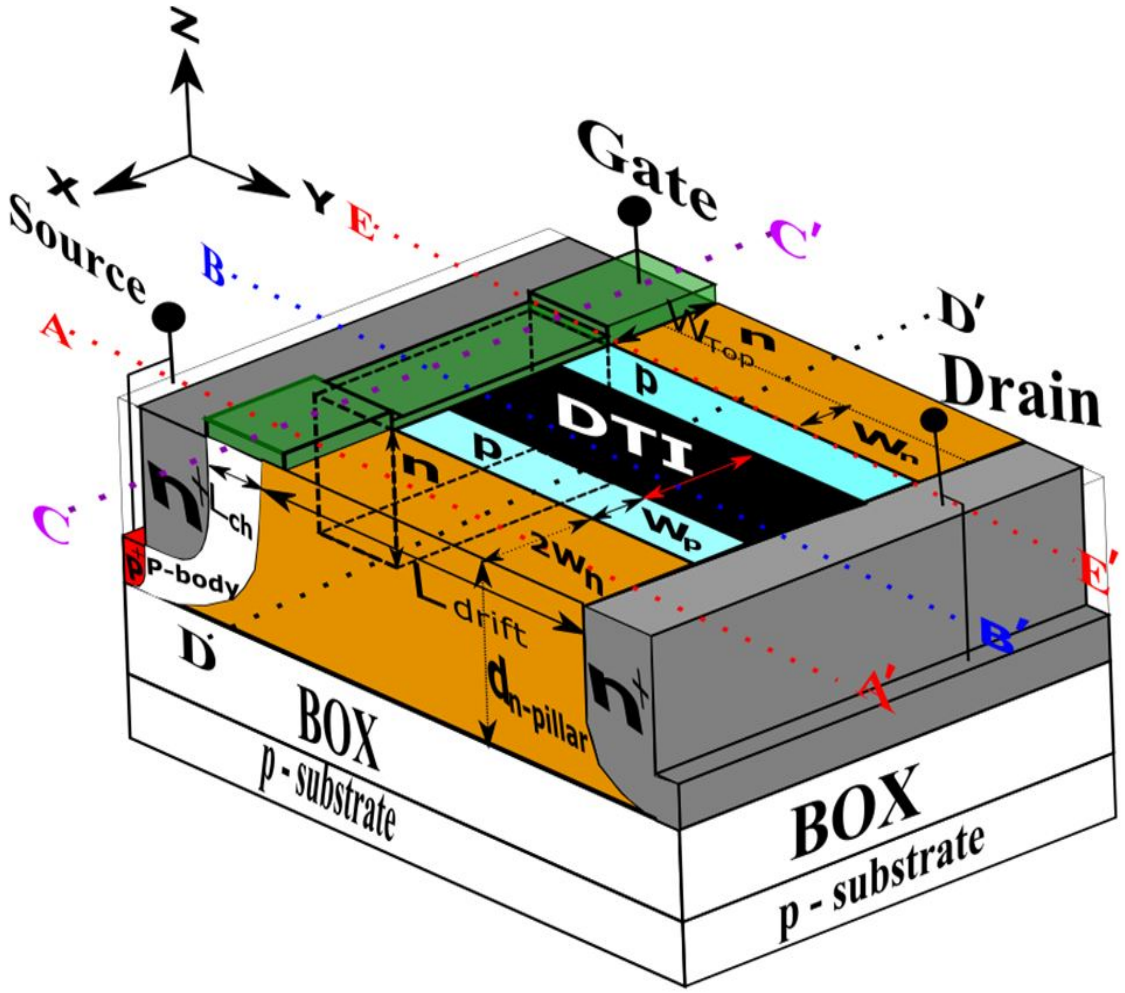
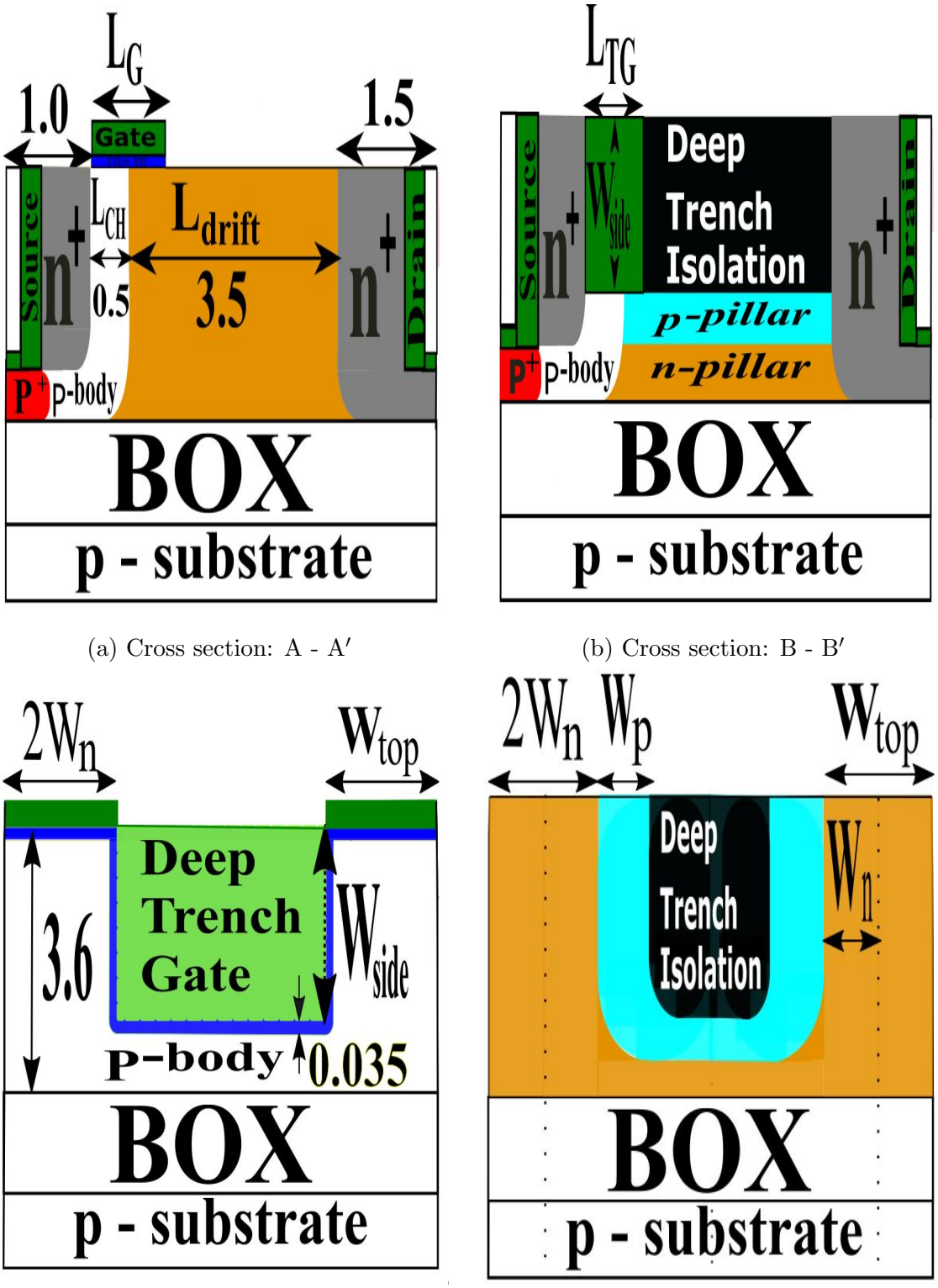


Figure 4.1: 3-D geometry of the investigated 1 μm gate length SJ-MGFET having a width of 200 μm and a drift length of 3.5 μm.

4.2 Device Structure of the 3-D SJ-MGFET

The SJ-MGFET investigated in the thesis has a relatively complex 3-D design permitted by the application of non-planar SOI technology [6]. The transistor consists of a deep trench gate with a heavily doped alternating U-shaped n-type and p-type doping pillars forming a drift region. The schematic of the device simulation domain with the cross-sectional views is illustrated in Figure 4.1 and Figure 4.2 (all dimensions are in μm). This transistor design follows closely the architecture of SJ-MGFETs reported in [6, 7]. The whole transistor structure is grown on a buried oxide layer to mitigate the effect of substrate-assisted depletion (SAD) [8–10]. The SJ-MGFET has a 1 μm gate length trenched in the channel of 0.5 μm length, creating a top surface (W_{top}) and a side wall (W_{side}) enclosure in the channel (a non-planar technology). This forms a multi-gate structure in the channel aiming at reducing the channel resistance and redistributing electron current crowding



(a) Cross section: A - A′

(b) Cross section: B - B′

(c) Cross section: C - C′

(d) Cross section: D - D′

Figure 4.2: A 2-D cross-sectional views at the locations indicated by X - X′ (X=A, B, C and D) in the investigated 1 μm gate length SJ-MGFET.

near the peak of the n-pillar in a SJ unit. The trench gate depths ranging from 1.5 μm - 3.0 μm in a step of 0.3 μm is carefully examined . It is observed that the difference in the doping concentration of the SJ n– and p–pillars becomes smaller

as the trench gate depth is increased, also reported by [7]. A trench gate depth of 2.7 μm (W_{side}) is chosen to create an effective pathway to the SJ drift region. The deep trench source and drain contacts provide an effective 3-D current density distribution in the structure that ensures uniform conducting flow with the deep trench isolation (DTI) separating each SJ unit. A different dimension of buried silicon dioxide ($Si0_2$) ranging from 0.5 μm to 5.0 μm has been studied in order to minimise the effect of substrate-assisted depletion (SAD) [8, 11] and mitigate the degradation of current during self-heating. The self-heating management should ensure a good thermal conductive path for the dissipated heat in the active device region to the substrate (due to a poor thermal conductivity of $Si0_2$ (1.4 W/m-K) compared to silicon (140 W/m-K)) [12, 13]. Thus, 2 μm is chosen as the depth of the buried oxide. The doping concentration of n– and p–pillars are n_n and n_p with W_n and W_p their widths of 0.3 μm, respectively. The peak doping concentrations in the p-type substrate and the n-type source/drain contact are $1{\times}10^{15}$ cm^{-3} and $1{\times}10^{20}$ cm^{-3}, respectively. Note that a design of this doping profile has to prevent a current leakage and a punch-through in the device.

4.3 3-D TCAD Simulations of the SJ-MGFET

The study is carried out with a 3-D commercial device simulator Atlas by Silvaco [5] using a drift-diffusion (DD) transport approach. In the DD transport approach, the carrier mobility model plays a central role. Since electrons are the major carriers in the SJ-MGFET, the Caughey-Thomas electron mobility model [14] is employed which can be expressed as:

$$\mu_e = \mu_1(\frac{T_L}{300K})^{\alpha_e} + \frac{\mu_2(\frac{T_L}{300K})^{\beta_e} - \mu_1(\frac{T_L}{300K})^{\alpha_e}}{1 + (\frac{T_L}{300K})^{\gamma_e}(\frac{N}{N_{\text{crit}}})^{\delta_e}} \tag{4.1}$$

where μ_e is the doping and temperature dependent low field electron mobility, while μ_1 and μ_2 are the first and second term mobility components, N_{crit} is the electron concentration between μ_1 and μ_2. N is the total impurity concentration, T_L is the lattice temperature, and α_e, β_e, γ_e, and δ_e are the doping and temperature coefficients for electrons. The following electron mobility parameters are used: μ_1= 55.24 cm^2/V.s, μ_2= 1429.23 cm^2/V.s, $N_{\text{crit}} = 1.072 \times 10^{17}$ cm^{-3}, $\alpha_e = 0.0$, $\beta_e = -2.3$, $\gamma_e = -3.8$, $\delta_e = 0.73$. All these parameters are default for the Caughey-Thomas

mobility model in Atlas [14]. Transfer (I_{D}-V_{GS}) and output (I_{D}-V_{DS}) characteristics of the SJ-MGFET at different voltage ratings will be compared with the reported experimental data [6] including the breakdown voltage (BV). In addition, the degradation of the current induced by self-heating (as a result of power dissipation and a low thermal conductivity of the buried oxide layer) is also investigated. Finally, a doping profile and 3-D geometry of the SJ-MGFET are optimised to increase the BV and to minimise device specific on-resistance ($R_{on,sp}$). In 3-D electro-thermal simulations, a heat transport equation is solved, which can be written as:

$$C\frac{\delta T_L}{\delta t} = \nabla(k\ \nabla T_L) + H \tag{4.2}$$

where C is the temperature-dependent heat capacitance per unit volume in real space, k is the temperature-dependent thermal conductivity in real space, H is the heat generation and T_L is the local lattice temperature. Placement of the thermal contacts in the device along the x, y, and z axes has been carefully examined because the choice of thermal boundary conditions determines the degree and distribution of temperature within the structure [15]. Thermal contacts are positioned at a bottom, and at the electrodes (source and drain), with all contacts set to 300 K in order to achieve a real time self-heating effect that has occurred in measurements [16, 17]. The switching performance of the SJ-MGFET is investigated with the aim of quantifying its capacitance (C) and conductance (G) effects, respectively, to allow further optimisation of the structure to meet different applications. The capacitive behaviour of the device is a function of the inversion, depletion and accumulation states [18, 19]. The C-V characteristics in the simulations at a frequency of 1 MHz in order to quantify the junction capacitances and the doping concentration of the substrate is studied. In addition, the resultant effect of the gate-drain capacitance (C_{gd}) and the gate-source capacitance (C_{gs}) on the gate capacitance C_{g} is investigated.

4.3.1 On-State Simulations

The transfer (I_{D} - V_{GS}) characteristics of the simulated SJ-MGFET with L_{drift} = 3.5 μm, and W = 200 μm are obtained in the on-state while maintaining the optimum charge balanced conditions of $n_n = 6.4{\times}10^{16}\ cm^{-3}$ and $n_p = 9.85{\times}10^{16}\ cm^{-3}$,

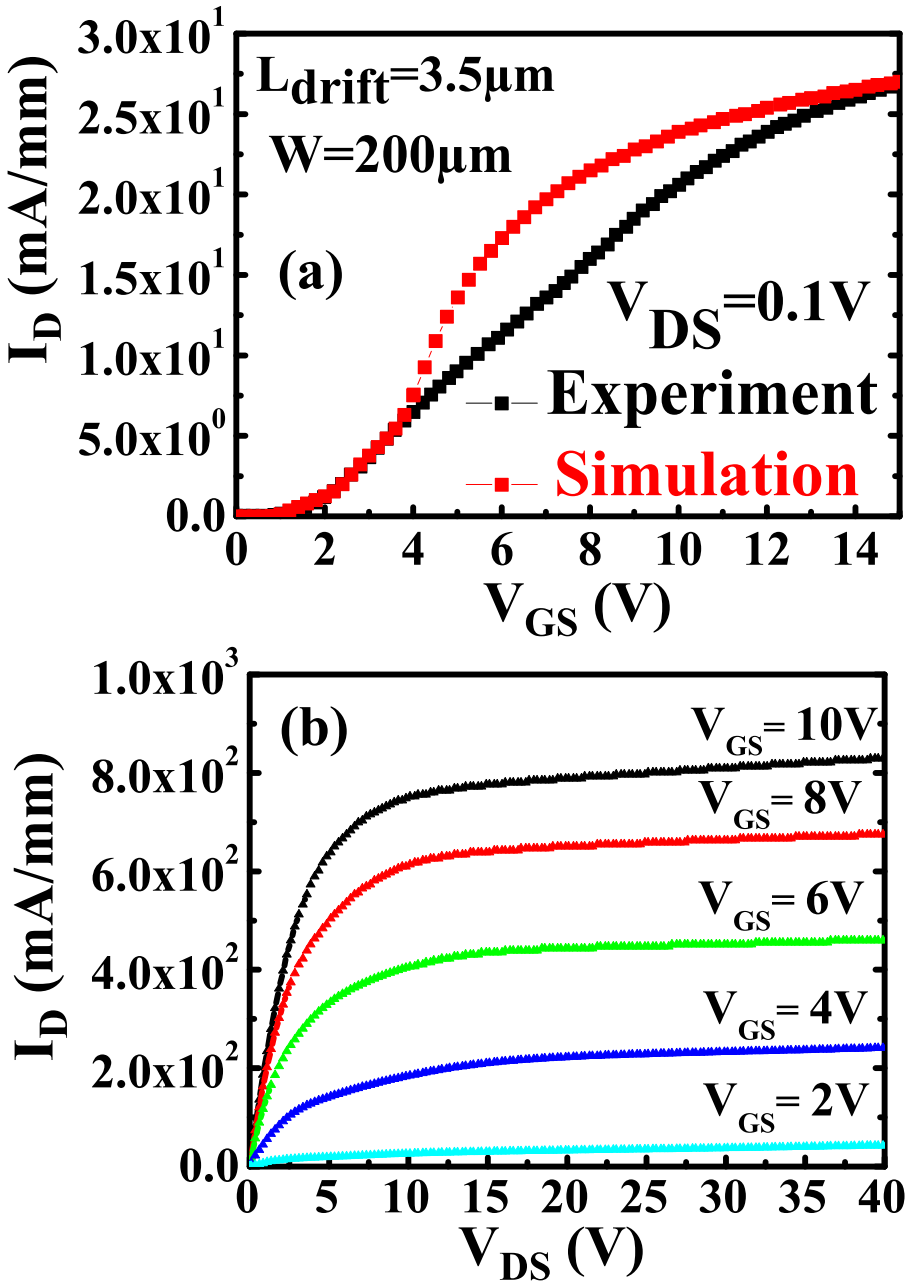


Figure 4.3: (a) Transfer (I_{D}-V_{GS}) characteristics of the simulated SJ-MGFET with a trench depth (W_{side}) of 2.7 μm and a gate oxide thickness (t_{ox}) of 35 nm in comparison with experiment data at $V_{\mathrm{DS}} = 0.1\ V$. (b) Output (I_{D}-V_{DS}) characteristics of the SJ-MGFET with $L_{\mathrm{drift}} = 3.5\ \mu$m, $W_{\mathrm{side}} = 2.7\ \mu$m, and $W = 200\ \mu$m at indicated gate voltages in a step of 2.0 V.

respectively. Figure 4.3 (a) compares the transfer characteristics (I_{D}-V_{GS}) of a simulated transistor with experimental measurements at a drain bias (V_{DS}) of 0.1 V. The simulations in Figure 4.3 (a) is carried out using the analytic low-field (ANALYTIC) mobility model only as opposed to the simulation results shown in Figure 3.4. The experimental transistor shows a linear dependence above a gate bias (V_{GS}) of 4 V till a saturation on-set at about 12 V exhibiting a more resistive behaviour in the device

body than observed in simulations. This increase in the resistivity of the channel occurring in experimental [6] I_{D}-V_{DS} characteristics is caused by the loss of a gate control because the deep trench gate fabrication is technologically limited and does not fully encompass the p-body of the device (see Figure 4.1). The simulations are in excellent agreement with experimental observations up to an elevated V_{GS} of 4 V. Above $V_{\mathrm{GS}} = 4$ V, the simulations show typical transistor switching characteristics when the drain current increases before reaching a saturation point ($V_{\mathrm{GS}} \sim 14$ V). Note here that the drain current is normalised per width of the non-planar transistor in order to be able to make a fair comparison with planar SJ-MOSFET technology. A threshold voltage of approximately 1.8 V has been obtained by interpolating a linear region of the I_{D}-V_{GS} characteristics at a low drain bias of 0.1 V. Figure 4.3 (b) shows the output characteristics (I_{D}-V_{DS}) with a maximum saturation drain current over 650 mA/mm at a V_{GS} of 10 V at $V_{\mathrm{DS}} = 5$ V. The I_{D}-V_{GS} characteristics of the simulated SJ-MGFET at drain bias of 1 V and 10 V are investigated as shown in Figure 4.4, aiming at achieving a high drive current at an elevated gate voltage. Since the electron current density distribution is limited by the channel-carrier mobility, this leads to saturation in the drain current as the gate voltage increases due to carrier-scattering mechanisms in the simulated device channel.

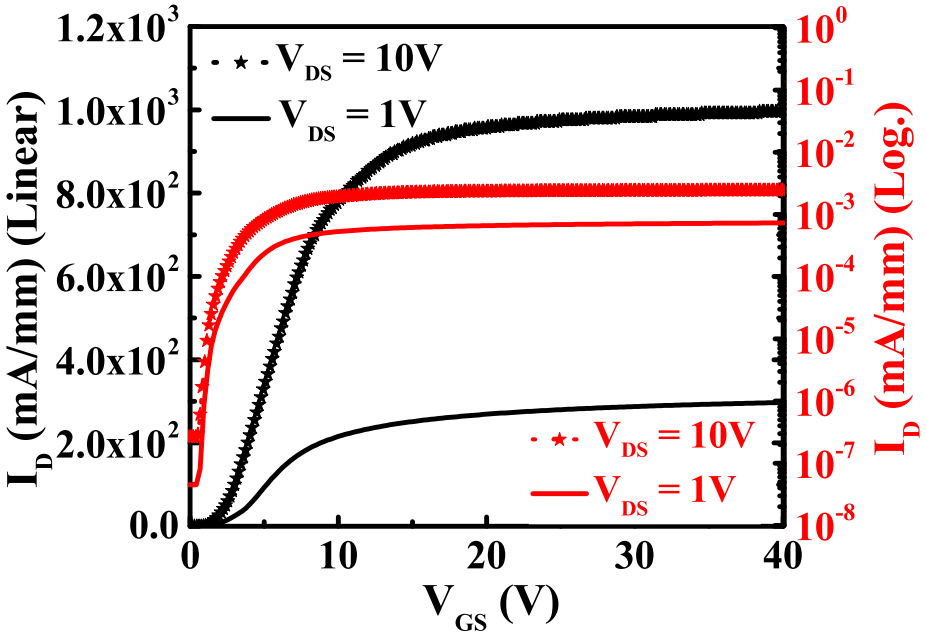


Figure 4.4: Transfer (I_{D}-V_{GS}) characteristics at low and high drain biases of 1 V and 10 V in both linear and log. scales of the simulated SJ-MGFET with a trench depth (W_{side}) of 2.7 μm and a gate oxide thickness (t_{ox}) of 35 nm.

4.3.2 Electro-Thermal Modelling

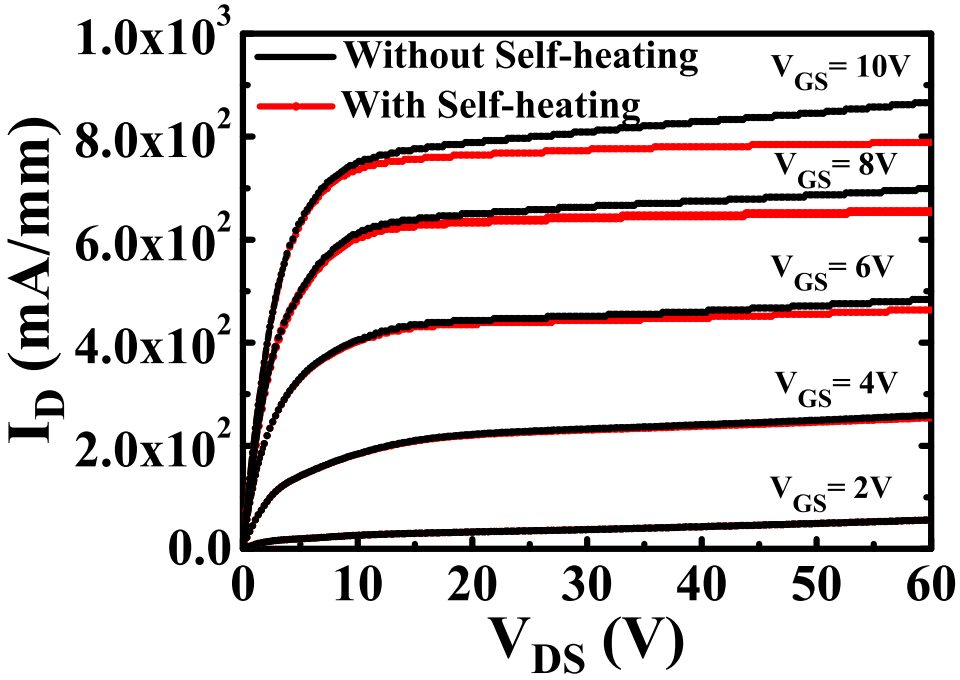


Figure 4.5: Output characteristics of the SJ-MGFET with $L_{\text{drift}} = 3.5$ μm and $W = 200$ μm obtained from the electro-thermal simulations at indicated gate voltages in a step of 2.0 V comparing simulations when the self-heating is excluded and included.

In this thesis, the effect of lattice temperature on the SJ-MGFET is investigated, and examined ways of dissipating the distributed heat in the drift region into the p-substrate aiming at reducing mobility degradation in the device. Figure 4.5 compares the previous on-state simulations with the electro-thermal simulations which account for the effect of lattice temperature on I_{D}-V_{DS} characteristics. The heat-per-Joule effect exhibits itself by the reduction of conductance in the saturation region of the drain current which is more pronounced at high drain biases. The SOI transistor architecture suffers from enhanced self-heating issues because of the low thermal conductivity of silicon dioxide. Therefore, a variation of the SOI based design when a fully deployed buried oxide (BOX) substrate in the partially depleted SOI SJ-MGFET is replaced by a partial BOX with opening under the drain is studied as illustrated in Figure 4.6(a). The partially buried oxide transistor architecture aims to provide an additional thermal conductive path for the dissipated heat to a substrate and enhance uniform distribution of electric field at breakdown. This is because the thermal window alleviates the low thermal conductivity of BOX and limits the total temperature rise in the device by allowing the heat to dissipate through the opening in the device SOI structure.

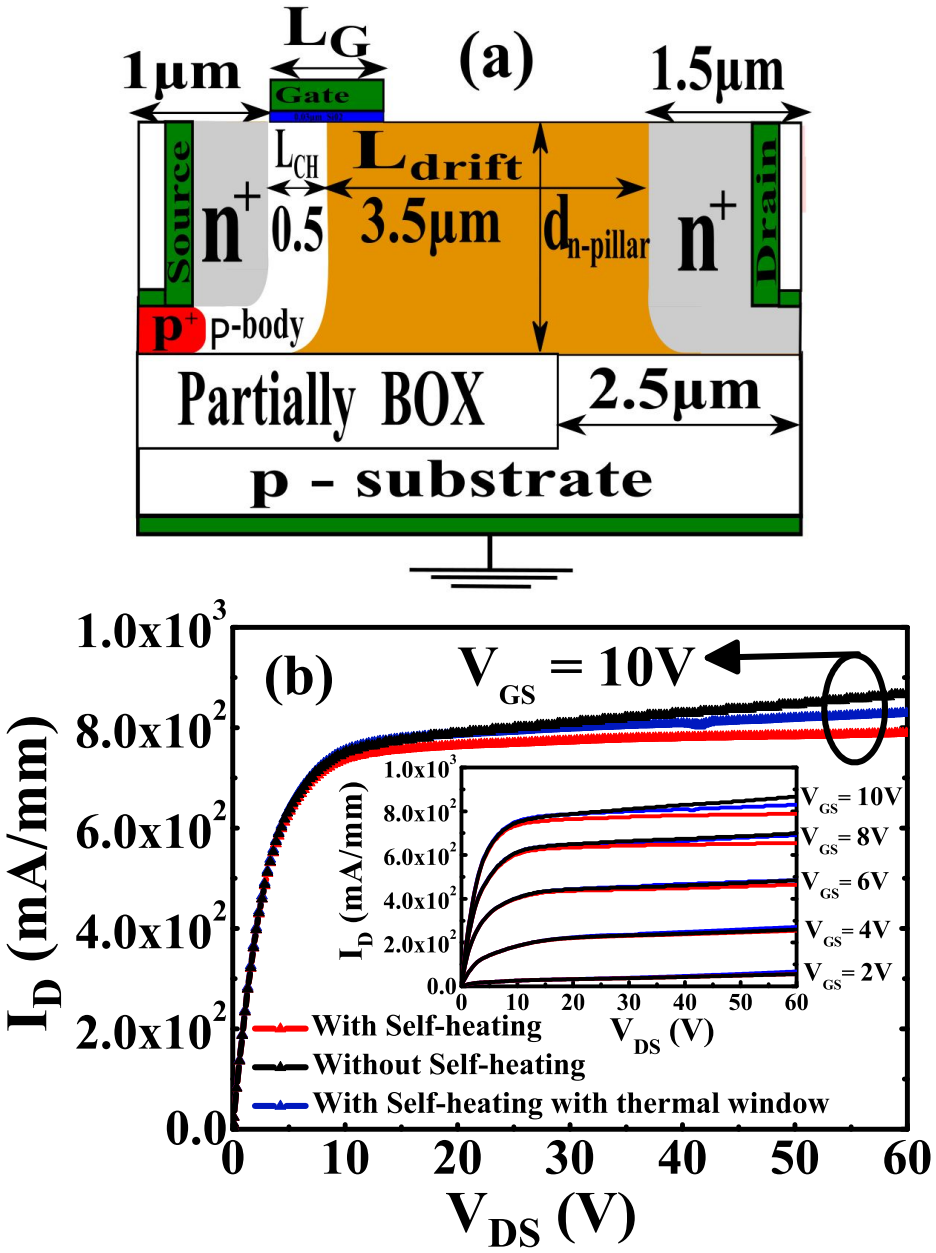


Figure 4.6: (a) 2-D schematic of the partially buried oxide with opening at the drain for L_{drift}= 3.5 μm, and W_{side} = 2.7 μm. (b) I_{D}-V_{DS} characteristics of the electro-thermal simulations comparing a transistor design with and without the thermal window for L_{drift}= 3.5 μm, W_{side} = 2.7 μm, and W= 200 μm at V_{GS} = 10 V and V_{DS} = 50 V.

Figure 4.6 (b) shows the I_{D}-V_{DS} characteristics of the SJ-MGFET with fully buried oxide (SOI technology) compared to the I_{D}-V_{DS} characteristics of the SJ-MGFET which uses only a partially buried oxide (thermal window) architecture. Both I-V characteristics are obtained from the electro-thermal simulations. At a gate bias of 10 V and a drain voltage of 50 V, the current decreases about 7.5% due to the self-heating when compared to the device with an ideal heat dissipation (the ideal heat

dissipation means that a lattice temperature in the whole device would be at kept at room temperature of 300 K). When the SJ-MGFET is designed using a thermal window as shown in Figure 4.6 (a); the current decrease seen in Figure 4.6 (a) is less than 3% as a result of redistribution of temperature in the substrate through the additional heat conductive path. This current decrease is relatively very small suggesting a quite limited effect of the thermal window in the transistor architecture.

4.3.3 Off-State Simulations

The effect of varying the drift region lengths on the BV is carefully examined. The SJ-MGFET architecture is redesigned and simulated with two different L_{drift} of 3.5 μm and 6.0 μm, respectively, during the off-state while maintaining the same trench gate depth (W_{side}) of 2.7 μm with alternating U-shaped n/p– SJ drift region pillar width of 0.3 μm since the charge induced by the SJ n-and p-pillars should provide a mirror symmetry of each other in order to ensure charge compensation during the off-state. However, a cross-sectional area of the n-pillar (A_n) is larger than that of the p-pillar (A_p) as shown in Figure 4.1. This leads to asymmetry in a SJ unit and results in a charge imbalance in the drift region. In order for the SJ unit to sustain a maximum voltage and achieve a fully depleted drift region before a breakdown, the total charge Q has to satisfy the relation [2]:

$$Q < \varepsilon_s(\frac{E_C}{q}) \tag{4.3}$$

where E_C is the critical electric field of silicon, ε_s is the permittivity of silicon and q is the elementary charge. In other words, the doping concentration of the p-pillar (n_p) should be greater than the n-pillar (n_n). This will ensure that the average charge in the depleted SJ unit tends toward zero. Figure 4.7 depicts the effect of charge imbalance in the SJ unit on the BV. The variation along the drift region has no effect on the charge imbalance. This is due to the fixed ratio between cross-sectional areas of the two SJ pillars. The charge balance condition tends to shift toward the highly doped acceptor side for each dose variation in the p-pillar region. This is a result of substrate-assisted depletion effect and a volume difference between the p-pillar and the n-pillar in the SJ region.

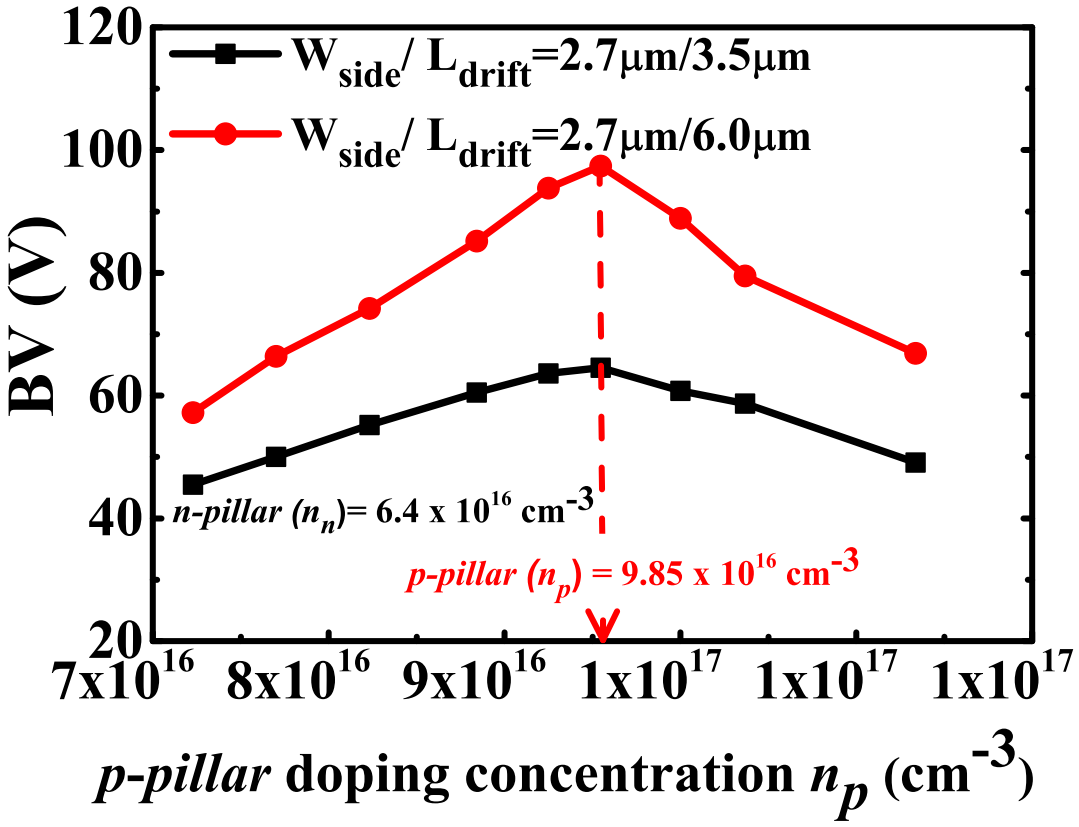
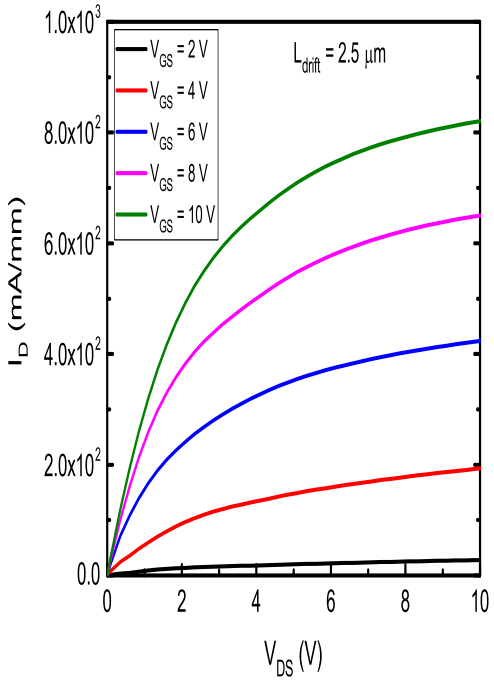


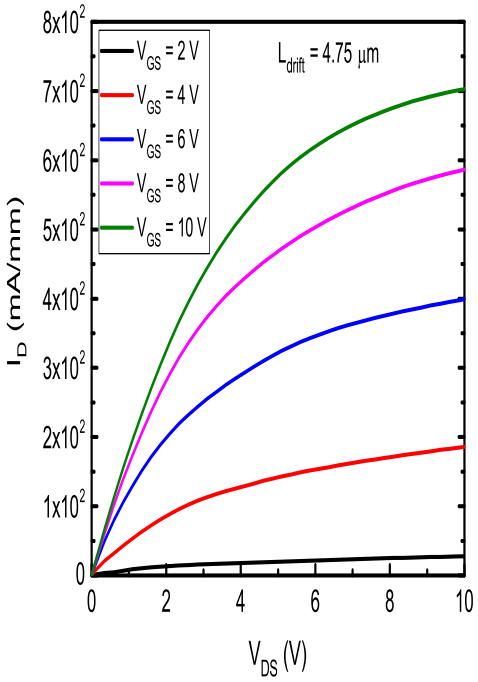
Figure 4.7: The effect of charge imbalance on the BV in SJ-MGFET with $W_{\text{side}} = 2.7\ \mu$m and $W_n = W_p = 0.3\ \mu$m, comparing two device widths of $L_{\text{drift}} = 3.5\ \mu$m and $6.0\ \mu$m during off-state.

4.4 On-State Simulations For Different SJ Drift Region Lengths

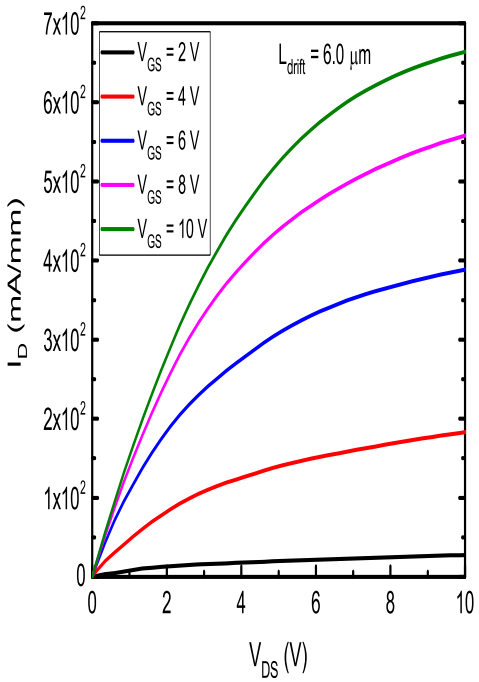
The on-state simulations are carried out for various the SJ drift region lengths by varying the drift region length from 1.5 μm to 7.5 μm in a step of 1.25 μm under a charge balanced condition while maintaining the same the gate length of 1.0 μm, channel length of 0.5 μm, and source/drain contact of 1.0 μm/1.5 μm, respectively. Figure 4.8 shows output (I_{D}-V_{DS}) characteristics of the SJ-MGFET during on-state for different SJ drift region lengths of 2.5 μm, 4.75 μm, 6.0 μm and 7.5 μm. It is observed that the SJ-MGFETs offer saturation drain current of 825 mA/mm, 715 mA/mm, 668 mA/mm and 615 mA/mm at a V_{DS} of 10 V with $V_{\text{GS}} = 10\ V$ for a SJ drift region length of 2.5 μm, 4.75 μm, 6.0 μm and 7.5 μm, respectively. The drain current reduces as the drift region length increases due to the increase in the on-resistance between the source and the drain contacts.



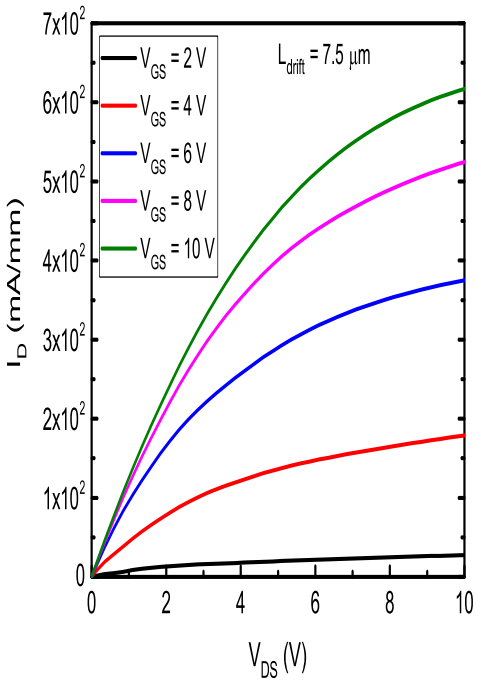
(a) I_D-V_{DS} of a SJ-MGFET with a drift region length of 2.5 μm.



(b) I_D-V_{DS} of a SJ-MGFET having a drift region length of 4.75 μm.



(c) I_D-V_{DS} of a SJ-MGFET having a drift region length of 6.0 μm.



(d) I_D-V_{DS} of a SJ-MGFET having a drift region length of 7.5 μm.

Figure 4.8: Output (I_D-V_{DS}) characteristics of the SJ-MGFET at different gate voltages for various SJ drift region lengths of 2.5 μm, 4.75 μm, 6.0 μm and 7.5 μm.

4.5 Electric Field Distribution

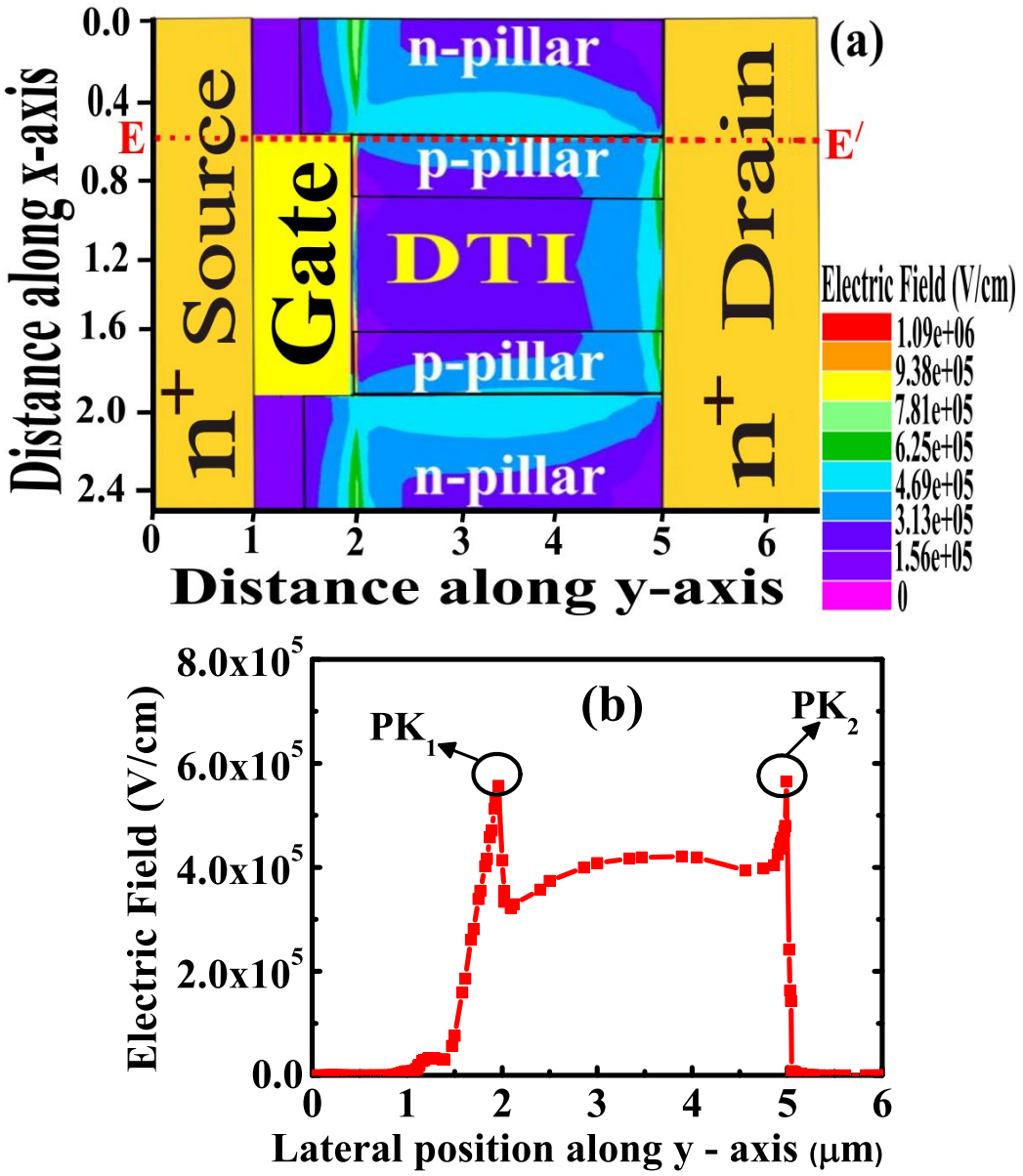


Figure 4.9: (a) Contour plot of the electric field distribution at the surface of the SJ-MGFET during the off-state with L_{drift}= 3.5 μm, and W_{side} = 2.7 μm under a charge balance condition. (b) Lateral electric field distribution at the surface of a drift region along the E-E′ cutline between the interface of the n– and the p–pillars during the off-state under a charge balance condition with W_{side} = 2.7 μm, L_{drift}= 3.5 μm, and $d_{\text{n-pillar}}$ = 3.6 μm.

Figure 4.9 (a) shows the contour plot of the electric field at the surface of the SJ-MGFET during off-state under a charge balance with $W_n = W_p$ = 0.3 μm and L_{drift} = 3.5 μm. High electric field can be observed at the gate edge under W_{top}, with n– and p– pillars mutually depleted resulting in uniform distribution of electric field in the drift region. The SJ-MGFET will undergo avalanche breakdown at the junction

between the p-body and the n-pillar when the electric field reaches a critical value, E_C, of approximately 5.5×10^5 V/cm .

Figure 4.9 (b) shows the lateral electric field distribution at a surface during off-state under charge balance condition. The fully depleted SJ drift region shows two peak electric fields (PK_1 and PK_2) at the gate (W_{top} and W_{side}) edge and the p-pillar/n^+ drain junction, respectively. The surface peak electric field at the edge of the gate electrode can be relaxed by using a metal field plate aiming at redistributing electron current crowding near the junction between the p-body and the n-pillar.

4.5.1 Potential Distribution

Figure 4.10 shows the potential distribution in the device along the A-A′ cut-line during the off-state under a charge balance condition. The slope of the potential determines electric field distribution at a breakdown voltage in the SJ structure.

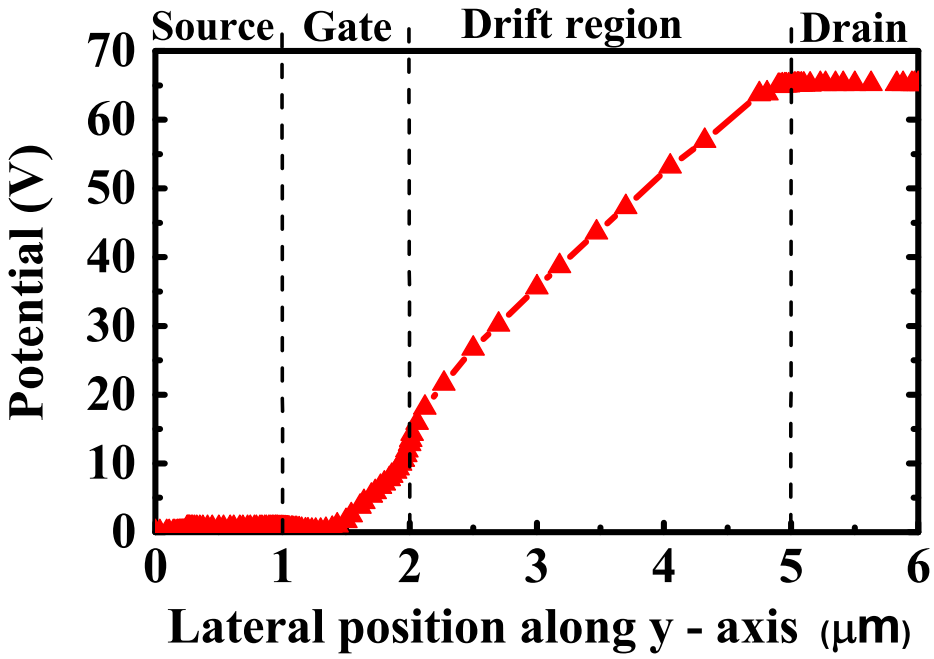


Figure 4.10: Potential distribution profile along the A-A′ cut-line in the off-state under a charge balance for the SJ-MGFET with L_{drift} of 3.5 μm, $W_n = W_p =$ 0.3 μm, and $W_{\text{side}} = 2.7$ μm.

A breakdown of 65 V is obtained for $W_{\text{side}} = 2.7$ μm, and L_{drift}= 3.5 μm which corresponds to an average lateral electric field of 18.6 V/μm.

4.6 Gate Capacitance and Conductance Extractions Using AC Analysis

In the simulations, the C-V analysis is carried out with a small signal $A.C$ response by performing a two carrier solution, thereby extracting the gate overlap capacitance and conductance in the SJ-MGFET structure. Figure 4.11 (a) shows the C_{g} and G_{g} of the device in the C-V simulation. In the on-state when the gate is reverse biased, the p-body area situated in the proximity of the gate is switched on to an accumulation state and the n-pillar is maintained in an inversion state; when the gate is forward biased, the p-body area changes to an inversion state and the n-pillar switches to an accumulation state. An overall C_{g} of approximately 0.01 pF is achieved, which is the summation of C_{gs} and C_{gd}.

Figure 4.11 (b) depicts the dependence of the output capacitance ($C_{\mathrm{oss}} = (C_{\mathrm{ds}} + C_{\mathrm{gd}})$) on the drain source voltage (V_{ds}) during small-signal AC analysis at 1 Mhz. Drain-source capacitance (C_{ds}) is the dominant factor at drain biases of $V_{\mathrm{ds}} < 22\ V$ in which the C_{oss} is directly proportional to it. However, as the drain voltage increases beyond $V_{\mathrm{ds}} > 30\ V$; the gate-drain capacitance (C_{gd}) plays an active role in the total resultant effect of C_{oss} of the device. The SJ-MGFET exhibits $R_{on,sp}.C_{\mathrm{oss}} = 445$ mΩ.pF in the C_{oss} - V_{ds} characteristics at $V_{\mathrm{ds}} = 50\ V$ which is approximately one-tenth and one-fifth of the D-MOSFET and FP-MOSFET, respectively [20].

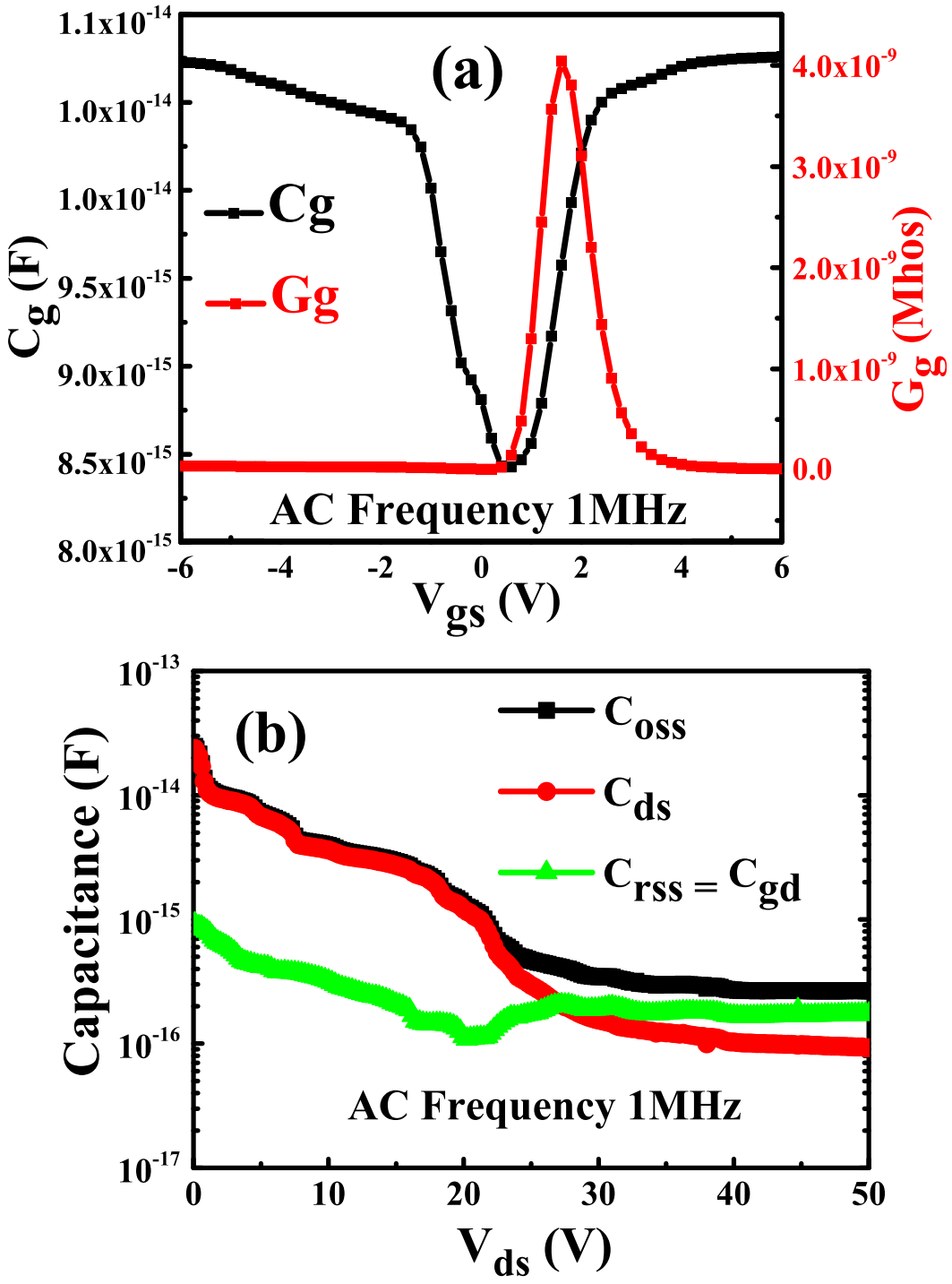


Figure 4.11: (a) Gate capacitance and conductance plotted as function of the gate-source voltage $V_{\rm gs}$ at $A.C$ signal of 1 MHz with $L_{\rm drift}$ = 3.5 μm, $W_{\rm side}$ = 2.7 μm. (b) The dependence of the $C_{\rm oss}$, $C_{\rm rss}$ and $C_{\rm ds}$ on the $V_{\rm ds}$ at small signal $A.C$ analysis of 1 MHz.

4.7 Transient Simulation of SJ-MGFET as a Switch

Figure 4.12 shows a simple circuit which utilises SJ-MGFET as a switch with its drain terminal D connected to the supply voltage drive V_{DD} via the external resistor of R_L acting as a load resistance. The device is biased between the cut-off region and the saturation region with its source terminal S grounded.

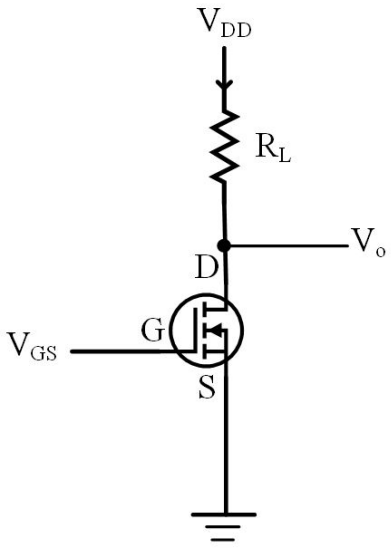


Figure 4.12: SJ-MGFET functioning as a switch.

Figure 4.13 (a) and Figure 4.13 (b) show the SJ-MGFET turn-on simulation as a switch when the device is ramped to $V_{\mathrm{GS}} = 10\ V$ and $V_{\mathrm{DD}} = 50\ V$ neglecting the circuit resistance R_c and the stray inductance L_s. An external resistor of 1 $k\Omega$ is used to simulate a low load resistance path between the drain and the drive. Hence, the SJ-MGFET offers a better switching turn-off time (t_{off}) of approximately 1.0 ns compared with the planar gate double diffused MOSFETs (D-MOSFETs) ($t_{off} = 18.5$ ns) and the field-plate trench MOSFETs (FP-MOSFETs) ($t_{off} = 1.1$ ns) at the same voltage rating [20].

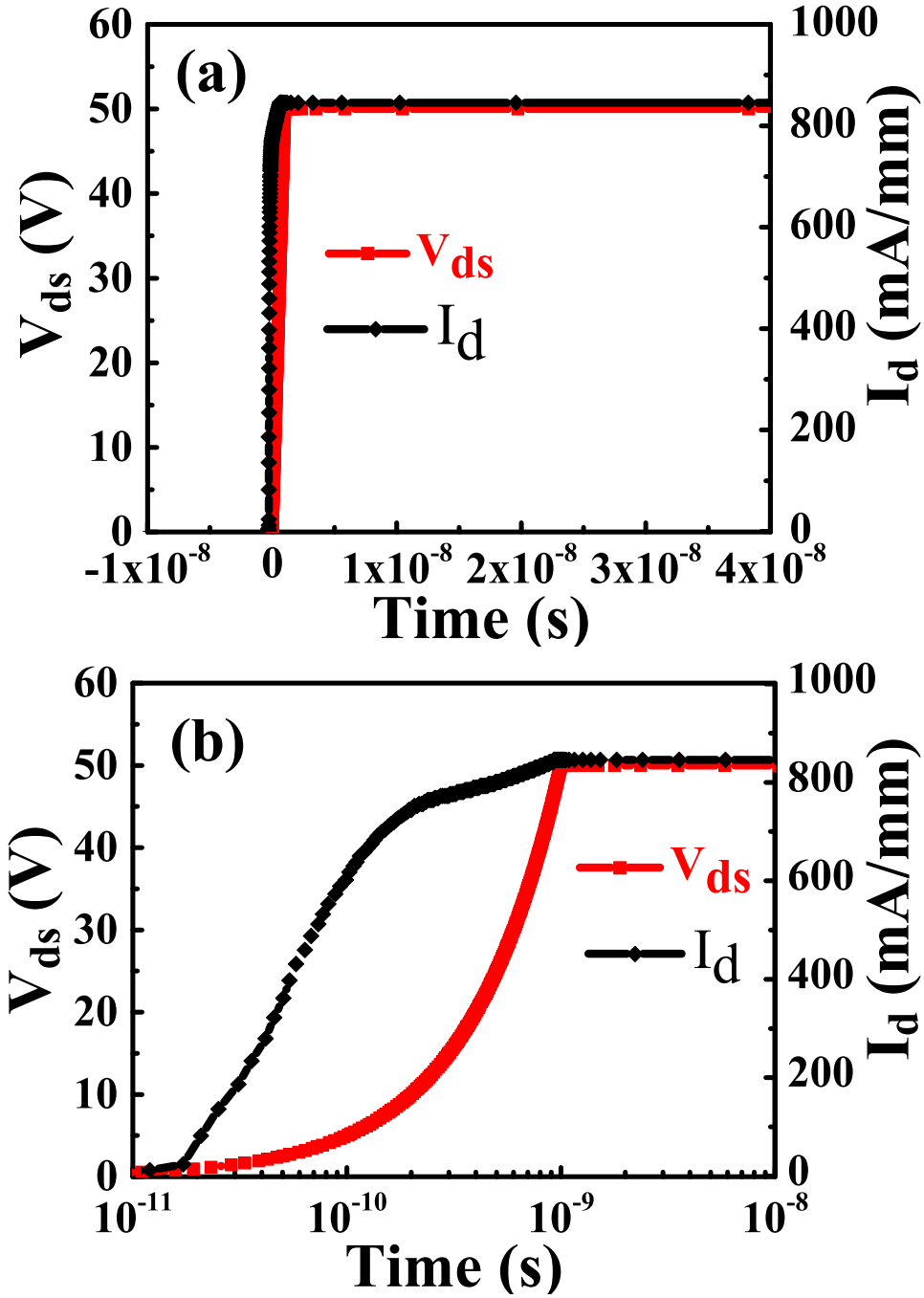


Figure 4.13: Switching waveforms of the SJ-MGFET turn-on simulation as a switch when the device is ramped from the cut-off region into saturation region against time (s) in a (a) linear scale (b) log. scale.

4.8 Specific On-Resistance of the Optimised SJ-MGFET

Figure 4.14 illustrates the specific on-resistance profile along the A-A′ cut-line of the SJ-MGFET under a charge balance condition with $W_{\text{side}} = 2.7$ μm, and L_{drift}= 3.5 μm. In comparison with conventional SJ-LDMOSFET technology at the same voltage rating and channel length, the SJ-MGFET offers $R_{on,sp}$ of 8.9 $\mu\Omega.\text{cm}^2$ and 0.204 $m\Omega.\text{cm}^2$ at both the channel and the drift regions, respectively, corresponding to 88% and 56% reduction [7]. It is also observed that the simulated and optimised SJ-MGFET, unlike the conventional planar gate SJ structure, can make of use of the deep trench gate to redistribute electric field crowding near the peak of the n-pillar thereby reducing the channel and the drift resistances.

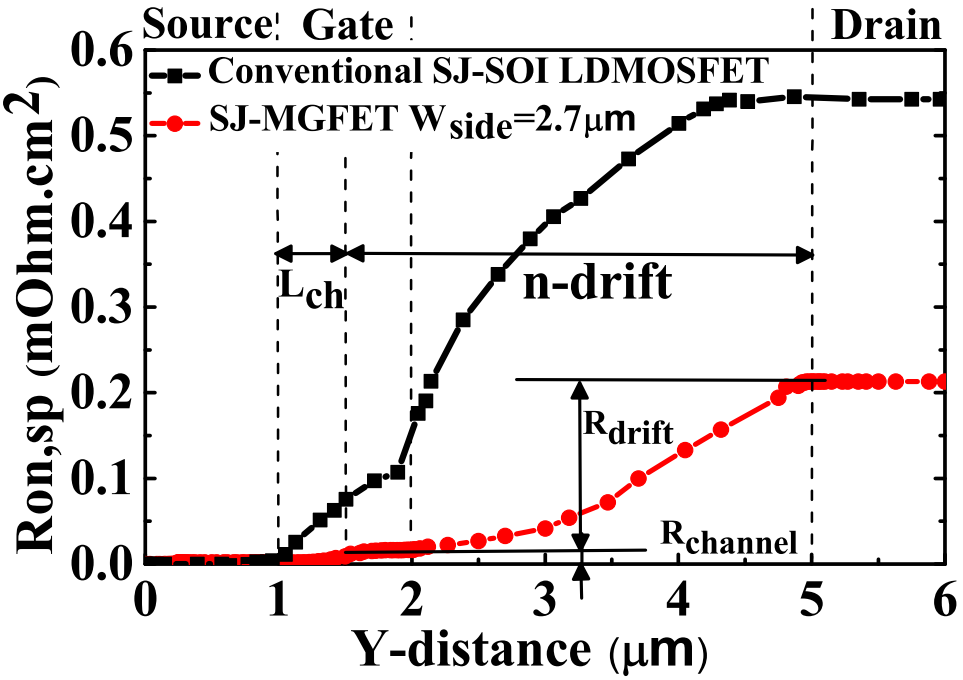


Figure 4.14: $R_{on,sp}$ profiles along the A-A′ cut-line in the on-state for the SJ-MGFET with L_{drift} of 3.5 μm, $W_n = W_p = 0.3$ μm, and $W_{\text{side}} = 2.7$ μm.

4.9 Trade-Off Between the Specific On-Resistance and the Breakdown Voltage

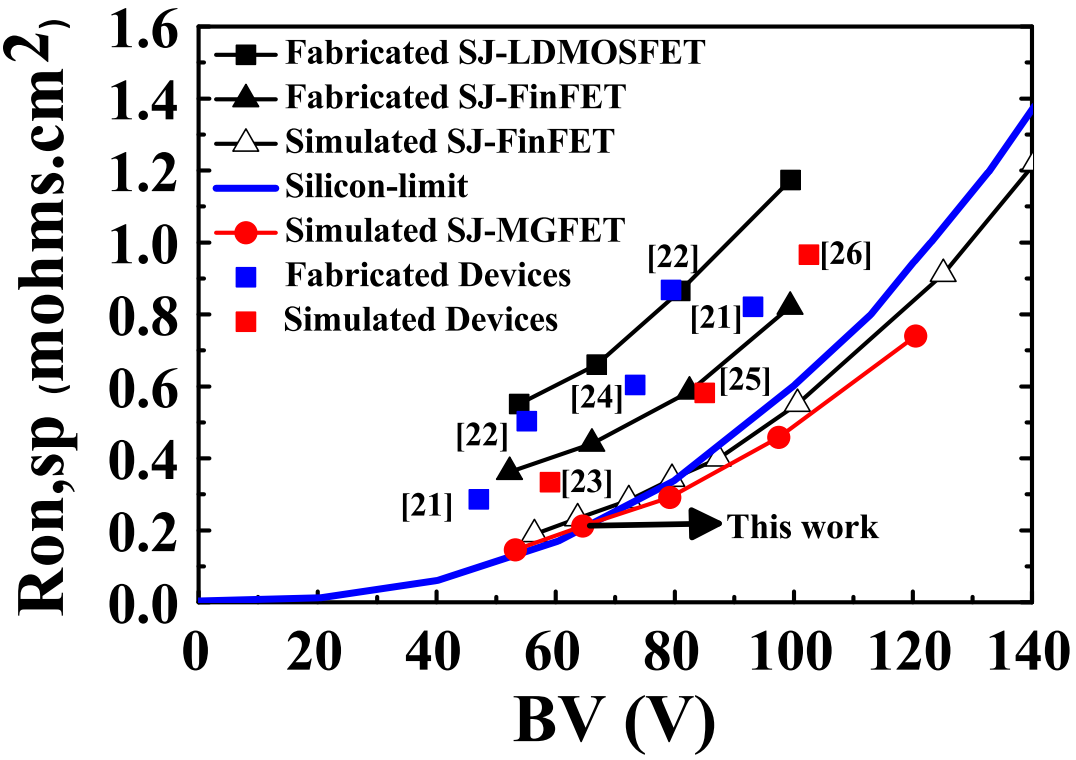


Figure 4.15: Specific on-resistance as a function of the breakdown voltage of the optimised SJ-MGFET at drift lenghts of 2.5 μm, 3.5 μm, 4.75 μm, 6.0 μm and 7.5 μm are compared with the reported conventional LDMOSFETs [21, 22] and conventional SJ-LDMOSFETs [23–26].

The trade-off between the BV and the $R_{on,sp}$ for the simulated SJ-MGFET, fabricated SJ-LDMOSFET and SJ-FinFET are compared with the ideal silicon limit and with several conventional LD-MOSFETs in Figure 4.15. The simulations of the SJ-MGFET show a low $R_{on,sp}$ of 0.21 mΩ.cm^2 and a BV of 65 V with $d_{\mathrm{n-pillar}}$ = 3.6 μm and L_{drift} = 3.5 μm. This leads to 68%, 52% and 15% reduction in $R_{on,sp}$ compared to the fabricated SJ-LDMOSFET, fabricated SJ-FinFET and simulated SJ-FinFET at the same BV rating, respectively. In addition, the SJ-MGFET offer the following specific on-resistances and breakdown voltages at various drift region lengths as follows: a $R_{on,sp}$ of 0.15 mΩ.cm^2 and a BV of 53 V with L_{drift} = 2.5 μm; a $R_{on,sp}$ of 0.29 mΩ.cm^2 and a BV of 79 V with L_{drift} = 4.75 μm, a $R_{on,sp}$ of 0.46 mΩ.cm^2 and a BV of 98 V with L_{drift} = 6.0 μm, and a $R_{on,sp}$ of 0.74 mΩ.cm^2 and a BV of 121 V wit L_{drift} = 7.5 μm.

4.10 Conclusion

The optimisation of doping profile of the 1 μm gate length SJ-MGFET using Silvaco TCAD simulations has shown that the FoM of this non-planar transistor can be substantially improved. The drive current has increased by 41% from 380 mA/mm to over 650 mA/mm, while the off-current decreased from 4×10^{-2} mA/mm to 2×10^{-4} mA/mm, respectively [6], demonstrating a big advantage of the multi-gate device architecture to reduce leakage current. The optimisation of the SJ-MGFET doping profile gives an on-off ratio of 5×10^{6} with a saturation drain current of approximately 1000 mA/mm obtained at a drain voltage of 10 V and a gate voltage of 20 V. The application of 3-D TCAD simulations of the SJ-MGFET has been able to optimise the overall device design for a better trade-off between the BV and the $R_{on,sp}$ for sub-100 V rating applications. The optimised SJ-MGFET has achieved 15% reduction in $R_{on,sp}$ from 0.25 mΩ.cm^2 to 0.21 mΩ.cm^2 when compared with a simulated SJ-FinFET at a BV of 65 V [6]. With the trench gate and optimised fully-depleted SJ multi-gate architecture, the structure can offer a superior performance in achieving a maximum breakdown voltage, a minimum specific on-resistance, and excellent FoM.

4.11 References

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Chapter 5

Scaling and Optimisation of Lateral Super-Junction Multi-Gate MOSFET for High Drive Current and Low Specific On-Resistance in Sub – 50 V Applications

5.1 Chapter Summary and Original Contributions

A scaling aimed at increasing physical density of transistors per chip area, increasing switching speed, and improving power capability delivers to smaller Power Integrated Circuits (PICs) with improved efficiency thanks to technological improvements in CMOS design. The complementary advantage of device dimension reduction is a linear increase in the drive current as the channel length decreases, and the switching losses decrease as the gate capacitance decreases. In order to sustain these two benefits simultaneously and not compromising other parameters, the overall device dimensions have to be scaled down rather than the physical channel length only [1]. Scaling of LDMOS (Lateral Double Diffused MOSFETs) based on a super-junction (SJ) concept ensures a high transconductance with improved frequency response and a low specific on-resistance ($R_{on,sp}$) for applications such as power management, domestic and office electronics appliances, automotive, military, and industrial control [2]. The two dimensional (2-D) effects of scaling of the gate oxide thickness (t_{ox}), the buried oxide (BOX), and the silicon thickness in a short-channel (SC) ultrathin SOI MOSFETs have been reported for a better suppression of the junction leakage current and power [3, 4]. However, the scaling

theory applicable to a bulk MOSFET and a single-gate MOSFET cannot be fully implemented in a SJ multi-gate MOSFET, because of the disparity in distributions of electric field as a result of the asymmetric SJ device doping profile [5–7].
In this work, the three dimensional (3-D) effects of scaling of a non-planar SJ silicon MOSFET transistor by a factor S is examined, which can be used as an integrated power transistor with applications in power amplifiers and switching. It is observed that the scaling requires a subsequent optimisation of the SJ unit. The non-planar lateral SJ multi-gate MOSFET (SJ-MGFET) has been fabricated within a silicon-on-insulator (SOI) technology [8]. The scaling and the optimisation of the non-planar SJ SOI MOSFET [9] is performed by physically based 3-D TCAD simulations using a drift-diffusion (DD) transport model [10]. This SJ multi-gate (MG) FET (SJ-MGFET) is optimised using a calibration of the simulations against experimental characteristics by reproducing its I-V characteristics and the breakdown voltage (BV). Later, a better calibration with a different DD transport approach in the simulations is carried out to analyse scaling of the device dimensions in order to improve major device figures-of-merit (FoM) including a drive current, a switching capability, a breakdown voltage (BV), and a specific on-resistance ($R_{on,sp}$).
The original contributions of this works are:

- The application of 3-D Atlas simulations to scale the optimised SJ-MGFET architecture from 1 μm gate length to 0.5 μm, and 0.25 μm, respectively; and to optimise a doping profile under a charge imbalance principle in the SJ unit.

- The simulation and optimisation of the scaled devices design to have a larger number of transistors per chip and a higher integration by using 3-D Atlas simulations with drift-diffusion (DD) transport models.

- C-V analysis of the scaled and optimised SJ-MGFETs with a small AC signal model thereby quantifying the gate capacitance, the output and the reverse transfer capacitances effects, respectively, to quantify improvements in the transconductance, frequency response and switching speed.

- An investigation of the device voltage-sustaining capacity of the scaled and optimised SJ-MGFET during off-state aiming at achieving a fully depleted drift region and improving the device avalanche capability during the charge balanced condition.

- An improvement in a figures-of-merit (FoM) between the BV and the specific on-resistance ($R_{on,sp}$) of the scaled and optimised SJ-MGFETs.

5.2 Device Structure of the 3-D SJ-MGFET

The investigated SJ-MGFET in this work has a complex 3-D design permitted by a non-planar technology [11] with an embedded deep trench gate and heavily doped alternating U-shaped n-type and p-type doping pillars forming a SJ drift region length of L_{drift} with a pillar height of $d_{n-pillar}$ [8]. The whole transistor structure is grown on a buried oxide layer to mitigate the effect of substrate-assisted depletion (SAD) [12–14]. This SOI SJ-MGFET has a 1 μm gate length (L_{gate}) with a 0.5 μm channel (L_{ch}) length underneath. The gate is deep trenched to create a top surface with a width of W_{top} and a trench side wall of W_{side} width to enclose the channel (a non-planar technology). This embedded trench gate structure ensures reduction in the channel resistance and redistribution of electron current crowding under the gate, near the peak of the n-pillar in a SJ unit. The trench gate depths in the structure, ranging from 1.5 μm - 3.0 μm in a step of 0.3 μm is carefully investigated, and observed that the difference in the doping concentration of the SJ n– and p–pillars becomes smaller as the trench depth is increased [15]. To have an effective conducting pathway to the SJ drift region, W_{top} and W_{side} of 0.6 μm and 2.7 μm are chosen in the simulations. Deep trenched source and drain contacts provide an effective 3-D uniform current density distribution in the n–pillar region with a deep trench isolation (DTI) separating each SJ unit. The doping concentrations of n– and p–pillars are expressed as n_n and n_p, respectively, with their corresponding widths referred to as W_n and W_p.

The schematic of the device simulation domain is illustrated in Figure 5.1 showing the 3-D geometry of the investigated 1 μm gate length SJ-MGFET having a width of 200 μm and a drift length of 3.5 μm, respectively. Figure 5.2 shows cross-sectional views defined in Figure 5.1 as follows: (a) a 2-D structure of the 1 μm gate length SJ-MGFET having $L_{\text{ch}} = 0.5$ μm and $L_{\text{drift}} = 3.5$ μm with source and drain contact lengths of 1.0 μm and 1.5 μm, respectively, along a A - A$'$ cutline at the middle of the n-pillar in the SJ unit; (b) a 2-D structure at a B - B$'$ cutline, a midpoint of the gate length in Figure 5.1 showing the formation of the W_{top} and the W_{side} enclosure (with the $W_{\text{top}} = 2W_n$), by the embedded deep trench gate structure in the p-body

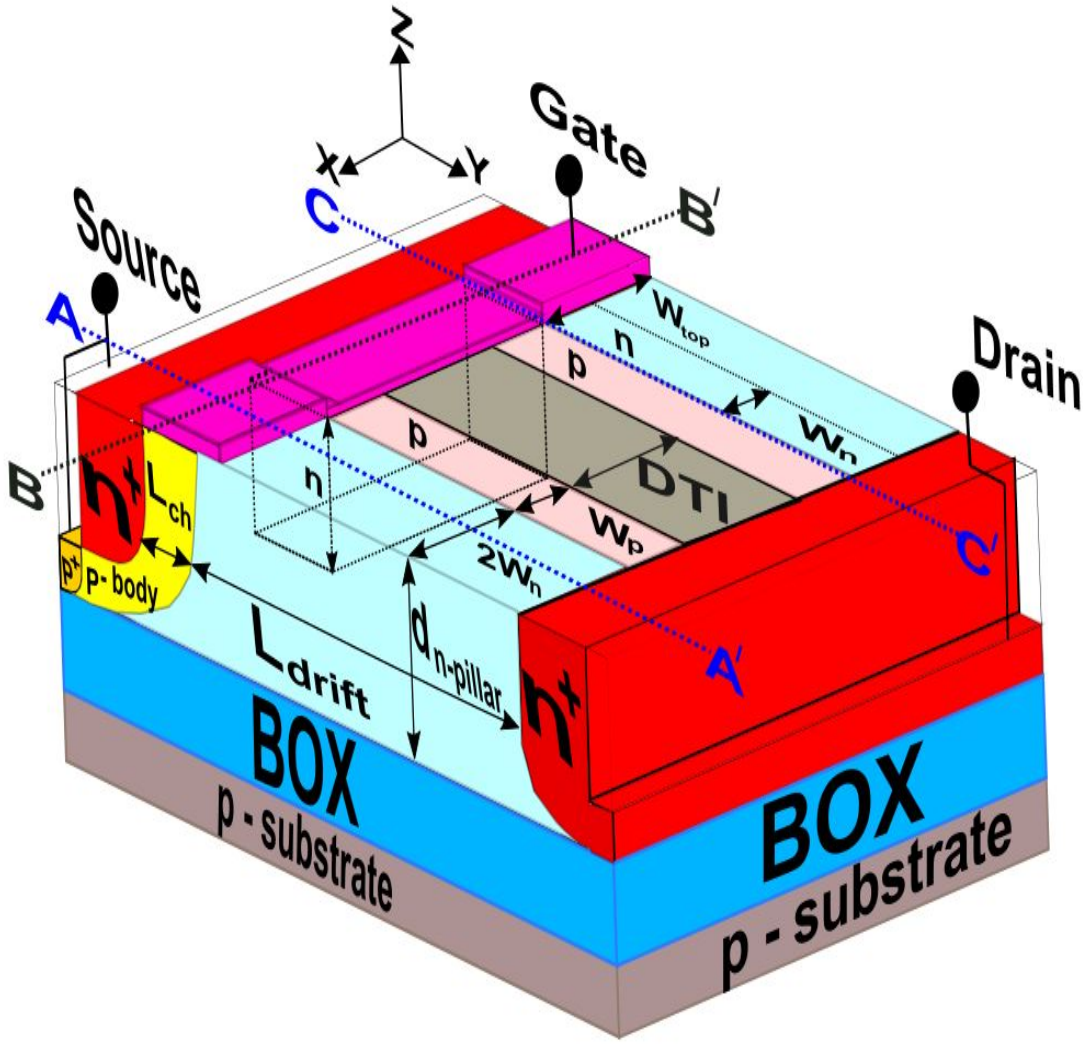
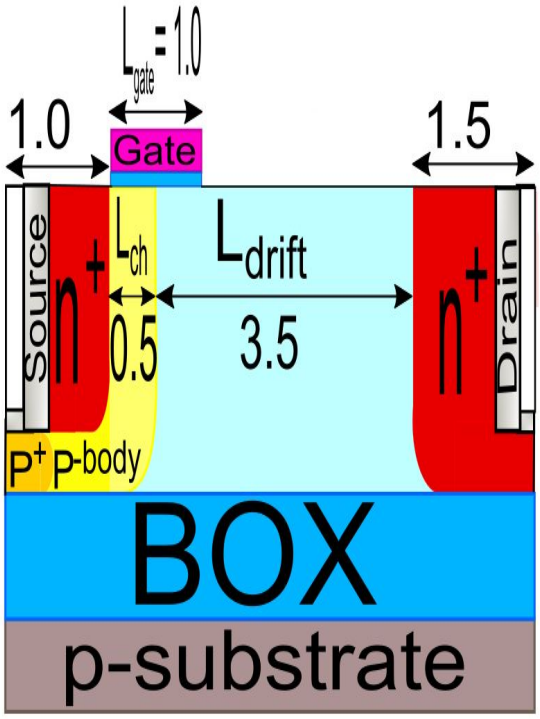


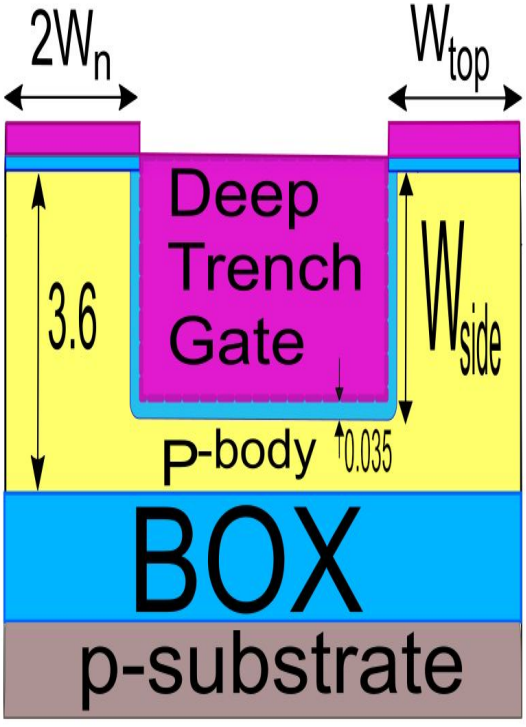
Figure 5.1: 3-D geometry of the investigated 1 μm gate length SJ-MGFET.

region of the device; (c) a 2-D structure of the scaled 0.5 μm gate length SJ-MGFET having $L_{\text{ch}} = 0.25$ μm, and $L_{\text{drift}} = 1.75$ μm with source and drain contact lengths of 0.5 μm and 0.75 μm, respectively, along a cutline at the middle of the n-pillar in the SJ unit; (d) a 2-D structure of the scaled 0.25 μm gate length SJ-MGFET having $L_{\text{ch}} = 0.125$ μm, and $L_{\text{drift}} = 0.875$ μm with source and drain contact lengths of 0.25 μm and 0.375 μm, respectively, along a cutline at the centre of the n-pillar in the SJ unit.

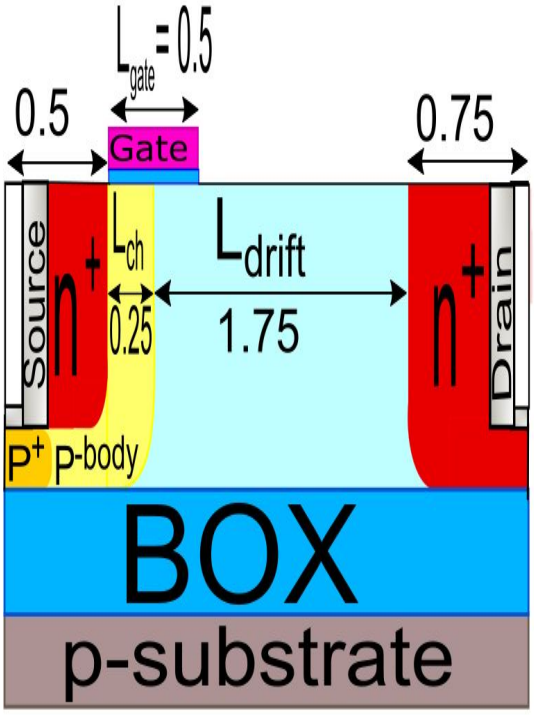
The different scaling approaches in all dimensions of the 3-D device structure in the simulations is carefully examined. It is observed that a scaling of the device vertically (along the z-axis) will degrade its trench-gate design because W_{side} of the trench gate structure accounts for about 75% of the SOI body [15, 16]. A narrowing



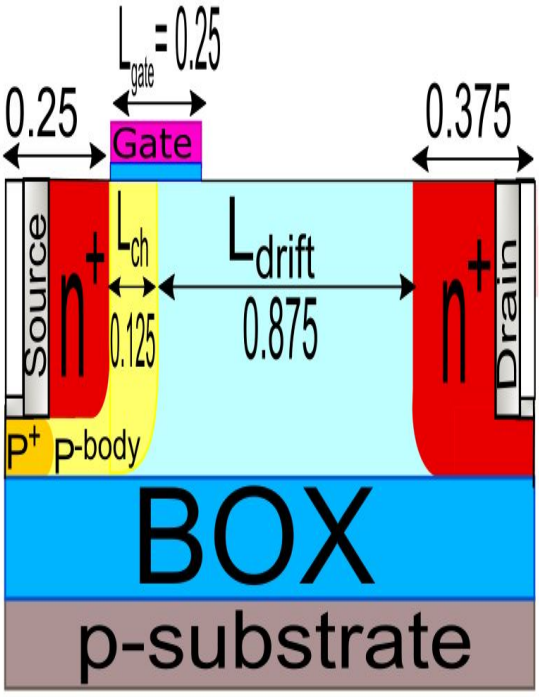
(a) Cross section: A - A′



(b) Cross section: B - B′



(c) 2-D lateral view of the 0.5 μm gate length SJ-MGFET.



(d) 2-D lateral view of the 0.25 μm gate length SJ-MGFET.

Figure 5.2: Cross-sectional views at the indicated locations in the investigated 1 μm gate length SJ-MGFET and a pictorial view of the proposed 0.5 μm and 0.25 μm gate length SJ-MGFETs.

down the buried oxide (BOX) and the p-substrate thickness will induce a junction leakage current, degrades the current during self-heating, and increase the effect of substrate-assisted depletion (SAD) [12, 17]. Scaling the structure along the x-axis will minimise the widths (W_n and W_p) of the SJ n– and p– pillars. However, the channel resistance, which play a crucial role in low voltage applications, becomes comparable to the drift resistance as a result of the minimum pillar width in the SJ drift region becoming similar to the built-in depletion region. This limits the reduction of the on-resistance due to a minimum pillar width/height ratio in the SJ unit [18]. Consequently, design variations of the SJ transistor n– and p– pillar widths are technologically limited [15, 19].

The scaling down of the 1.0 μm gate length SJ-MGFET structure laterally (along the y-axis) by scaling the channel length, the gate length, the gate oxide thickness, and the SJ drift unit length by a factor S to shrink the gate length of 1.0 μm to 0.5 μm and 0.25 μm is examined by the simulations in the thesis. Here, aiming at improving a major device figures-of-merit (FoM) including drive current, switching capability, BV and specific on-resistance ($R_{on,sp}$). In the simulations, a large channel doping is employed in the scaled down structures in order to minimise the maximum depletion-layer width (W_{dm}) and suppress short-channel effects (SCEs) [20–22]. However, this has an adverse effect on the input capacitance due to an increase in threshold voltage (V_{th}) associated with a high channel doping. To maintain electrostatic integrity of the channel potential by the gate, its oxide thickness is reduced by the same factor S of 0.5 and 0.25 to compensate for a loss of gate capacitance. The peak doping concentrations in the p-type substrate and the n-type source/drain contact are 1.0×10^{15} cm^{-3}, and 1.0×10^{20} cm^{-3}, while W_n and W_p are of equal widths of 0.3 μm, respectively.

5.3 3-D TCAD Simulations of SJ-MGFET

The study is carried out with a 3-D commercial device simulator Atlas by Silvaco [10] using a drift-diffusion (DD) transport model. The classical DD transport model is employed with analytic low-field mobility model based on Caughey-Thomas mobility model (ANALYTIC), and parallel electric field dependence mobility model (FLDMOB) along with Shockley-Read-Hall (SRH) recombination.

The analytic low-field mobility model, which is the doping and temperature dependent [23] is given by:

$$\mu_e = \left[\mu_1 \left(\frac{T_L}{300K} \right)^{\alpha_e} + \frac{\mu_2 \left(\frac{T_L}{300K} \right)^{\beta_e} - \mu_1 \left(\frac{T_L}{300K} \right)^{\alpha_e}}{1 + \left(\frac{T_L}{300K} \right)^{\gamma_e} \left(\frac{N}{N_{\text{crit}}} \right)^{\delta_e}} \right] \tag{5.1}$$

where μ_1 and μ_2 are the first and second term mobility parameters, N_{crit} is the electron concentration parameter at which the first term mobility parameter μ_1 changes to the second term mobility parameter μ_2. N is the total impurity concentration, T_L is the lattice temperature, and α_e, β_e, γ_e, and δ_e are doping and temperature coefficients. The following electron mobility parameters are used: $\mu_1 = 55.24\ cm^2/V.s$, $\mu_2 = 1429.23\ cm^2/V.s$, $N_{\text{crit}} = 1.072 \times 10^{17}\ cm^{-3}$, $\alpha_e = 0.0$, $\beta_e = -2.3$, $\gamma_e = -3.8$, $\delta_e = 0.73$. All these are default parameters for the analytic low-field mobility model in Atlas [23]. The parallel electric field dependence model [23] can be expressed:

$$\mu_e(E) = \mu_1 \left[\frac{1}{1 + \left(\frac{\mu_1 E}{v_{\text{SAT}n}} \right)^{\beta_{ex}}} \right]^{\frac{1}{\beta_{ex}}} \tag{5.2}$$

$$v_{\text{SAT}n} = \left[\frac{\alpha_{ex}}{1 + \theta_{ex}^{\left(\frac{T_L}{T_{\text{NOM}n}} \right)}} \right] \tag{5.3}$$

where $v_{\text{SAT}n}$ is the saturation velocity for electron, μ_1 is the first term low-field electron mobility, E is the parallel electric field, T_L is the lattice temperature, while β_{ex}, α_{ex}, θ_{ex}, and $T_{\text{NOM}n}$ are doping and temperature coefficient parameters specified as $\beta_{ex} = 2.0$, $\alpha_{ex} = 2.4 \times 10^7$, $\theta_{ex} = 0.8$, and $T_{\text{NOM}n} = 600$ [10]. Selberherr impact ionization model [24] used in the simulations examines the effect of charge imbalance of a doping concentration in n– and p– pillars of the SJ unit on BV when the device is in off-state. The model is based on the expression given by:

$$\alpha_n = A_n \exp \left[- \left(\frac{B_n}{E} \right)^{\beta_n} \right] \tag{5.4}$$

where E is the electric field in the direction of the current flow at a particular position in the device. A_n, B_n, and β_n are material parameters defined as $7.03 \times 10^5\ cm^{-1}$, $1.231 \times 10^6\ V/cm$ and 1.0 [10]. The transfer (I_{D}-V_{GS}) and the output (I_{D}-V_{DS})

characteristics of the SJ-MGFETs scaled down to 0.5 μm and 0.25 μm gate length are analysed. Finally, the doping profile and the 3-D geometry of the SJ-MGFET is optimised to improve the frequency response, drive current, breakdown voltage (BV), and specific on-resistance ($R_{on,sp}$).

5.3.1 Device Simulations of the 1 μm gate length SJ-MGFET

The transfer (I_{D}-V_{GS}) characteristics of the simulated 1.0 μm gate length SJ-MGFET with L_{drift} = 3.5 μm, and Width (W) = 200 μm are obtained in the on-state while maintaining the optimum charge balanced conditions of $n_n = 7.4{\times}10^{16}\ cm^{-3}$ and $n_p = 1.55{\times}10^{17}\ cm^{-3}$, respectively.

Figure 5.3 (a) compares transfer characteristics (I_{D}-V_{GS}) of the experimental [8] with the calibrated drift-diffusion simulations at a drain bias (V_{DS}) of 0.1 V. The simulation is in excellent agreement with experimental behaviour having a maximum error of approximately 0.5%. The transfer characteristics exhibit a typical transistor switching characteristics before reaching a saturation point. A threshold voltage of approximately 2.0 V is obtained at a drain bias of 0.1 V by interpolating the linear region of the I_{D}-V_{GS} characteristics with a drain current normalised per width of the non-planar transistor in order to be able to make a fair comparison with the planar SJ-MOSFETs.

Figure 5.3 (b) shows the effect of charge imbalance in the SJ unit on the BV during off-state in the simulated 1.0 μm gate length SJ-MGFET. The charge balance condition tends to shift toward the highly doped acceptor side for each dose variation in the p-pillar region [9]. This is a result of the volumetric difference between the p-pillar and the n-pillar in the SJ region and the substrate-assisted depletion (SAD) effect. A breakdown of 65 V is obtained for W_{side} = 2.7 μm, and L_{drift}= 3.5 μm which corresponds to an average lateral electric field of 18.6 V/μm.

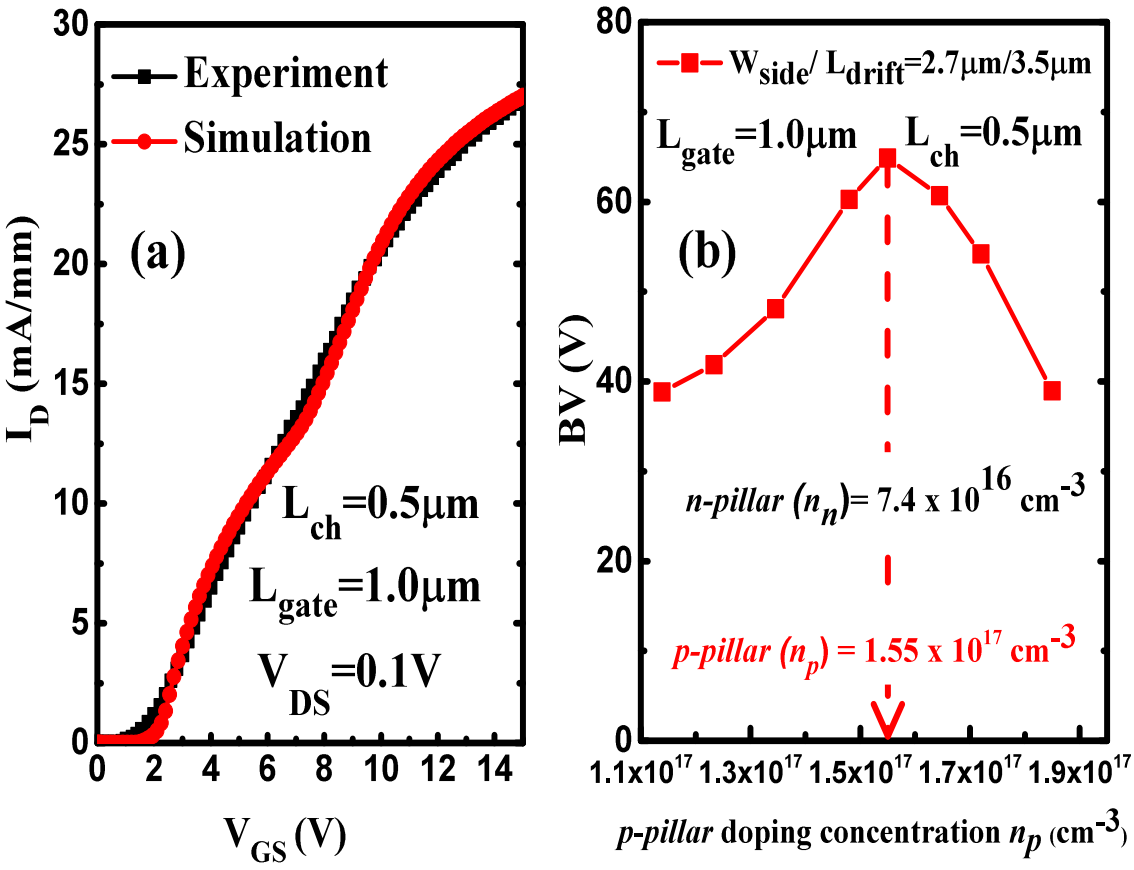


Figure 5.3: (a) Transfer (I_D-V_{GS}) characteristics of the 1.0 μm gate length SJ-MGFET showing a comparison between the experiment [8] and the simulations at V_{DS} = 0.1 V with L_{gate} = 1.0 μm, L_{drift} = 3.5 μm, W_{side} = 2.7 μm , and W = 200 μm. (b) The effect of charge imbalance on the BV in the SJ-MGFET with W_{side} = 2.7 μm, L_{drift} = 3.5 μm and $W_n = W_p$ = 0.3 μm during the off-state.

5.4 Scaling Approach and Optimisation of the Scaled down SJ-MGFETs

In order to prevent a weak electrostatic integrity in the 0.5 μm and 0.25 μm gate length (L_{gate}) SJ-MGFETs, optimisation of the doping profile is carried out aiming at achieving a maximum drive current, a lower specific on-resistance and improve the breakdown voltage of the scaled devices. Ideally, in a transistor technology, the threshold voltage decreases with decreasing channel length. However, in order to offset this threshold voltage decrease and control the SCEs, the channel doping is increased from 2.5×10^{17} cm^{-3} to 1.0×10^{18} cm^{-3} in the 0.5 μm gate length SJ-MGFET. This doping increase will also improve avalanche capability of the depleted SJ drift region during off-state. The thickness of the gate oxide (t_{ox}) is also reduced from 35 nm to 18 nm to increase the input capacitance.

5.4.1 On-State Simulations of the 0.5 μm gate length SJ-MGFET

The transfer (I_{D}- V_{GS}) characteristics and output characteristics (I_{D}-V_{DS}) of the simulated 0.5 μm gate length SJ-MGFET with $L_{\mathrm{drift}} = 3.5$ μm, and W = 200 μm are obtained in the on-state while maintaining the optimum charge balanced conditions of $n_n = 5.5{\times}10^{16}$ cm^{-3} and $n_p = 1.16{\times}10^{17}$ cm^{-3}, respectively.

Figure 5.4 (a) shows transfer characteristics (I_{D}-V_{GS}) of the optimised 0.5 μm gate length SJ-MGFET at V_{DS} of 0.1 V with a threshold voltage of 2.0 V. At a V_{GS} of 15.0 V with a $V_{\mathrm{DS}} = 0.1$ V, a saturation drain current of 38 mA/mm is obtained, resulting in 30% increase when compared with the current reported in an experimental device [8].

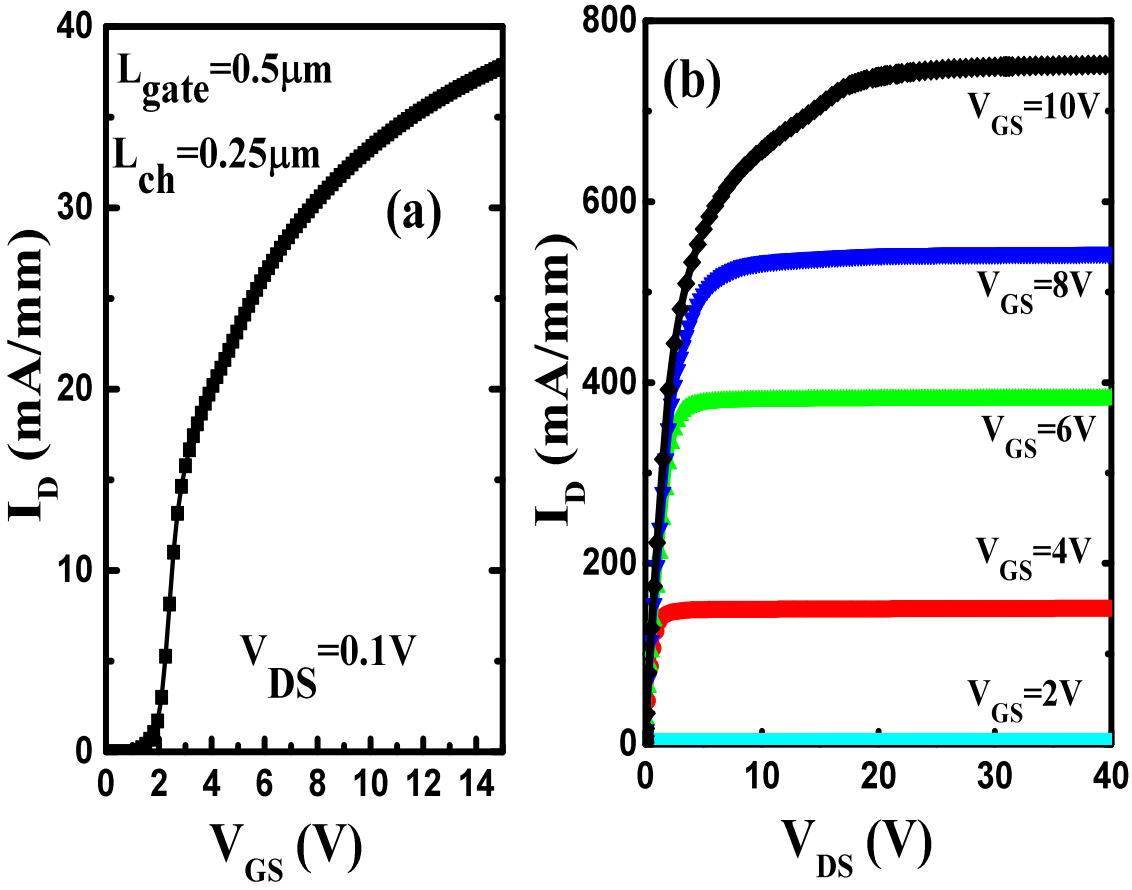


Figure 5.4: (a) Transfer (I_{D}-V_{GS}) characteristics of the optimised 0.5 μm gate length SJ-MGFET at $V_{\mathrm{DS}} = 0.1$ V with $L_{\mathrm{drift}} = 1.75$ μm and trench depth (W_{side}) of 2.7 μm. (b) Output (I_{D}-V_{DS}) characteristics of the 0.5 μm L_{gate} SJ-MGFET with $L_{\mathrm{drift}} = 1.75$ μm, $W_{\mathrm{side}} = 2.7$ μm, and $W = 2.46$ μm at indicated gate voltages in a step of 2.0 V.

Figure 5.4 (b) shows the output characteristics (I_{D}-V_{DS}) of the 0.5 μm gate length SJ-MGFET. The device exhibits a good current saturation with a flat output response at a large range of operational gate voltages. A saturation drain current over 740 mA/mm is extracted at a V_{GS} of 10 V with a $V_{\mathrm{DS}} = 20\ V$.

5.4.2 Off-State Simulations of the 0.5 μm gate length SJ-MGFET

Figure 5.5 (a) illustrates the relationship between the BV and the p-pillar doping concentration during a charge imbalance condition in the SJ unit of the 0.5 μm gate length SJ-MGFET when the device is in off-state. The asymmetrical geometry of the SJ unit as illustrated in Figure 5.1 causes a charge imbalance to occur in the device irrespective of the scaling factor. It has been stated in Section 4.3.3 that for a fully deleted SJ drift region the total charge (Q) must satisfy the relation [18]:

$$Q < \varepsilon_s \left(\frac{E_C}{q} \right) \tag{5.5}$$

where E_C is the critical electric field of silicon, ε_s is the permittivity of silicon, and q is the elementary charge. The SJ-MGFET scaled down to 0.5 μm L_{gate} will undergo avalanche breakdown at the junction between the p-body and the n-pillar with a breakdown of 48 V, which corresponds to an average lateral electric field of 27.5 V/μm for $L_{\mathrm{ch}} = 0.25\ \mu$m, and $L_{drift} = 1.75\ \mu$m.

Figure 5.5 (b) shows I_{D}-V_{DS} characteristics used to determine a BV when the optimised SJ-MGFET scaled down to $L_{\mathrm{gate}} = 0.5\ \mu$m, and $L_{\mathrm{ch}} = 0.25\ \mu$m is off during impact ionisation.

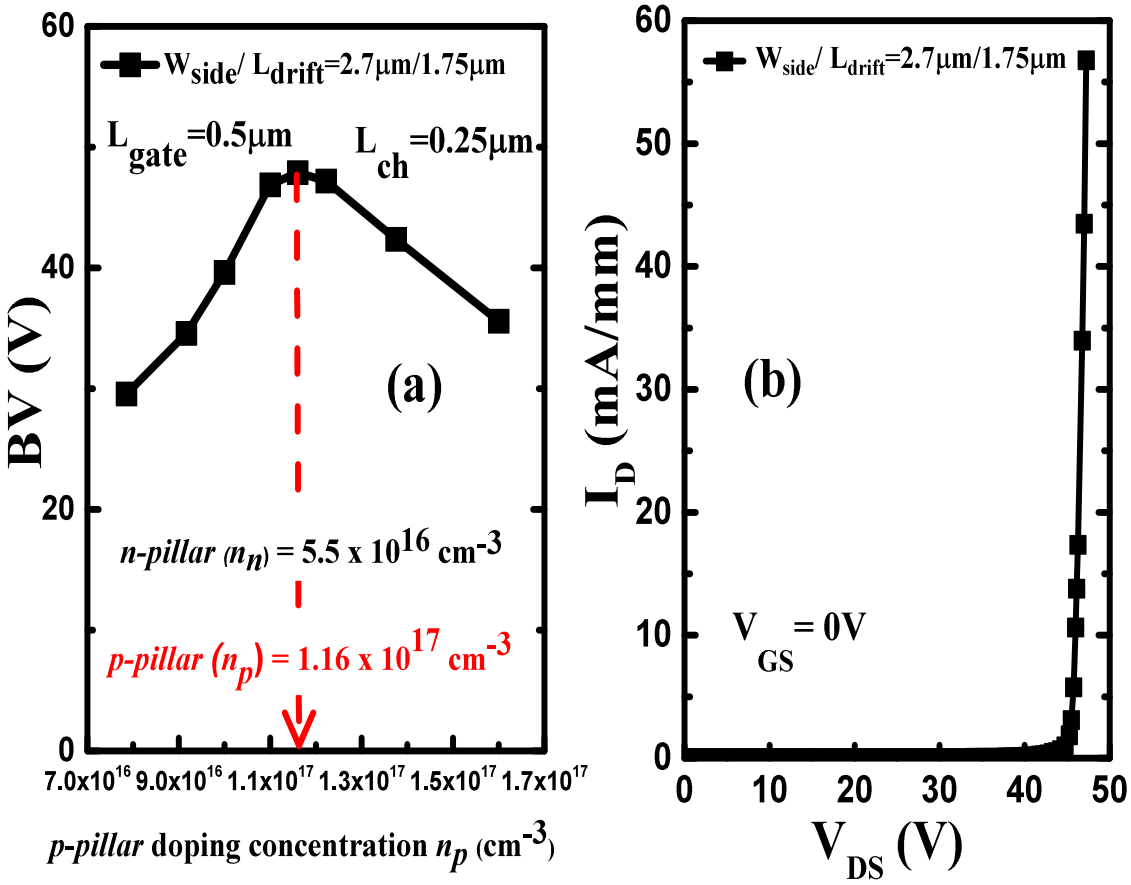


Figure 5.5: (a) The effect of charge imbalance on BV in the SJ-MGFET scaled down to 0.5 μm L_{gate} with $W_{\text{side}} = 2.7$ μm, $L_{\text{drift}} = 1.75$ μm and $W_n = W_p = 0.3$ μm during the off-state. (b) The BV during off-state under a charge balance condition for the SJ-MGFET scaled down to $L_{\text{gate}} = 0.5$ μm, and $L_{\text{ch}} = 0.25$ μm.

5.4.3 On-State Simulations of the 0.25 μm gate length SJ-MGFET

The SJ-MGFET scaled by a factor S of 0.25 has a gate length of $L_{\text{gate}} = 0.25$ μm, a channel length of $L_{\text{ch}} = 0.125$ μm, and a drift region length of $L_{\text{drift}} = 0.875$ μm, respectively. An oxide thickness (t_{ox}) of 35 nm reduced by a factor $S = 0.25$ scales to 9 nm in order to maintain gate electrostatic integrity. This will also compensate for the effect of lowering V_{th} due to the narrowing of channel length and suppress the SCEs. In addition, the channel doping is increased from 2.5×10^{17} cm^{-3} to 1.0×10^{19} cm^{-3} to prevent a punch-through in the structure.

Figure 5.6 (a) shows transfer characteristics (I_{D}-V_{GS}) of the optimised SJ-MGFET scaled down to 0.25 μm L_{gate} with an extracted threshold voltage of 3.9 V at V_{DS} of 0.1 V. A saturation drain current of 72 mA/mm is achieved at V_{GS} of 15.0 V and

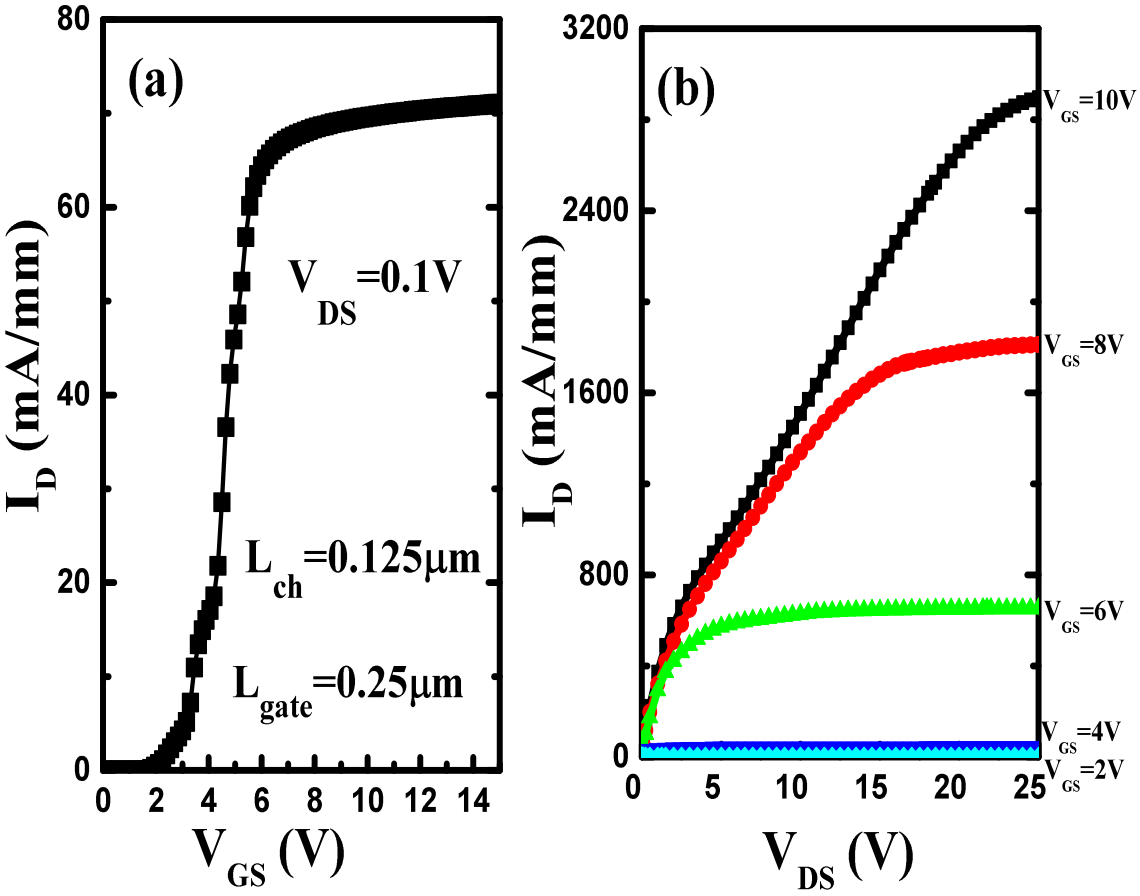


Figure 5.6: (a) Transfer (I_{D}-V_{GS}) characteristics of the optimised SJ-MGFET scaled down to 0.25 μm L_{gate} at $V_{\mathrm{DS}} = 0.1\ V$ with $L_{\mathrm{drift}} = 0.875\ \mu$m and a trench depth ($W_{\mathrm{side}}$) of 2.7 μm. (b) Output (I_{D}-V_{DS}) characteristics of the SJ-MGFET scaled down to 0.25 μm L_{gate} with $L_{\mathrm{drift}} = 0.875\ \mu$m, $W_{\mathrm{side}} = 2.7\ \mu$m, and $W = 2.46\ \mu$m at indicated gate voltages in a step of 2.0 V.

$V_{\mathrm{DS}} = 0.1\ V$, which corresponds to 63% increase when compared with the current reported in experimental device [8]. Figure 5.6 (b) shows output characteristics (I_{D}-V_{DS}) of the 0.25 μm gate length SJ-MGFET at various gate voltages in a step of 2.0 V. The I_{D}-V_{DS} characteristics show a current saturation up to an elevated V_{GS} of 6.0 V. Above $V_{\mathrm{GS}} = 6.0\ V$, the vertical electric field from the gate bias increases with the drain bias increase causing a channel resistance and a drain current to be strongly dependent on the drain voltage. This strong dependence is specific to a SJ structure because current flows only through the n-pillar. An elevated drain voltage will cause a voltage drop across a narrow depletion region between the channel end and the n-pillar resulting in a shortening of the channel length. This generates a high electric field in the shortened channel leading to the increase in the drain current with a higher drain voltage.

It is observed that the drain current increases in the I_D-V_{DS} characteristics with increasing of V_{GS} compared to the 1 μm gate length device structure with a thicker oxide. However, despite a strengthening of a gate control by the oxide thickness reduction and aggressive doping in the channel, the SCEs occur in the scaled 0.25 μm gate length device, especially at higher V_{GS}s. This is partially a result of increasing effect of the drain induced barrier lowering (DIBL) at very large applied drain voltages [25–27].

5.4.4 Off-State Simulations of the 0.25 μm gate length SJ-MGFET

The dependence of the BV on the p-pillar doping concentration during charge imbalance is plotted in Figure 5.7 (a) for the SJ-MGFET scaled down to the 0.25 μm gate length, when the device is in off-state.

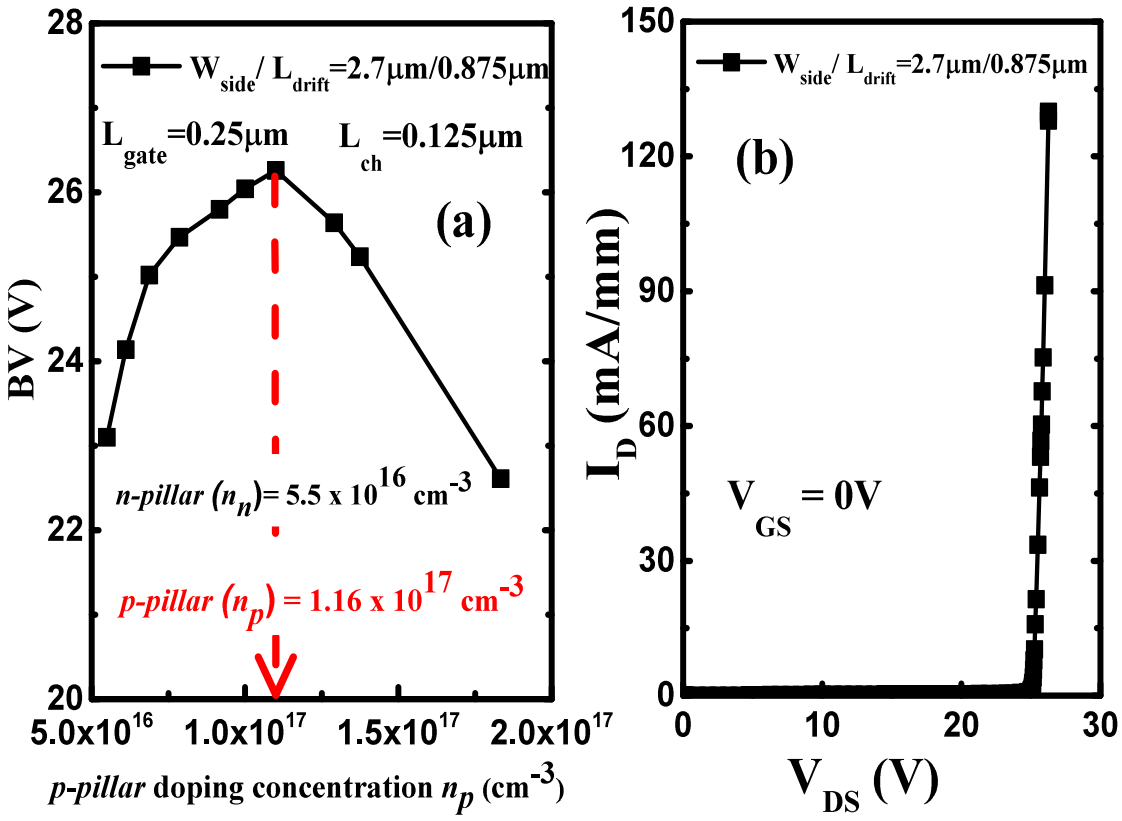


Figure 5.7: (a) A relationship between the BV and the p-pillar doping concentration during charge imbalance in the SJ unit when the device is scaled down to 0.25 μm L_{gate} with W_{side} = 2.7 μm, L_{drift} = 0.875 μm and $W_n = W_p$ = 0.3 μm during the off-state. (b) The BV during the off-state under a charge balance for the optimised SJ-MGFET scaled down to L_{gate} = 0.25 μm, and L_{ch} = 0.125 μm.

Figure 5.7 (b) illustrates determination of a BV of 26 V from I_{D}-V_{DS} characteristics for the 0.25 μm gate length SJ-MGFET during the off-state. An average lateral electric field in a drift region (see Figure 5.1) of the 0.25 μm gate length SJ-MGFET defined by L_{drift} = 0.875 μm is approximately 30 V/μm at a BV of 26 V. It is observed that varying the doping concentration in the SJ unit has a less effect on the BV because there is an optimal doping concentration limit per unit volume upon which the device can be optimised.

5.5 Electric Field Distribution

Figure 5.8 shows the lateral electric field distributions at the surfaces of the devices with L_{gate} of 1.0 μm, 0.5 μm, and 0.25 μm, respectively, during the off-state under charge balance condition along the C - C$'$ cutline. The electric field distribution along the C - C$'$ cutline (the line defined along the junction between n– and p–pillars as defined in Figure 5.1) is the field at 10 nm below the surface, from the source to the drain, during the off-state under the charge balance condition. The figure exhibits two peak electric fields at the gate edge and the $p - pillar/n^{+}$ drain junction in SJ-MGFETs with (a) L_{ch} = 0.125 μm, L_{gate} = 0.25 μm, and L_{drift} = 0.875 μm, (b) L_{ch} = 0.25 μm, L_{gate} = 0.5 μm, and L_{drift} = 1.75 μm, and (c) L_{ch} = 0.5 μm, L_{gate} = 1.0 μm, and L_{drift} = 3.5 μm.

The device avalanche breakdown occurred at the junction between the p-body and the n-pillar when electric field in all the three structures reaches a critical value, E_C, of approximately 5.5×10^5 V/cm. It is observed that surface electric field in the drift region (defined by the end of the channel and the beginning of the n-type drain doping) in each structure is relatively uniform and increases as the length of the drift region decreases. This implies that for an higher BV, more space is required for the electric field to be deployed.

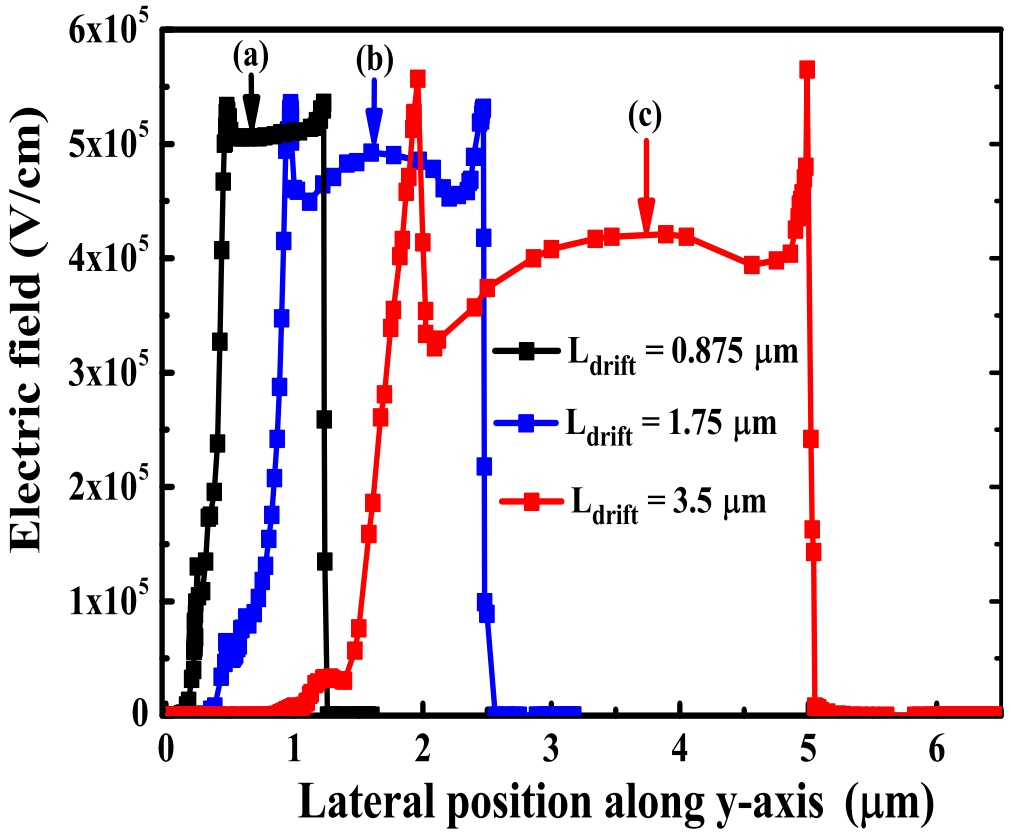


Figure 5.8: Lateral electric field distribution at the surface of the drift region along the $C - C'$ cutline defined along the junction between the n– and the p–pillars in Figure 5.1 during the off-state under the charge balance condition (a) in the SJ-MGFET with $L_{\text{ch}} = 0.125\ \mu$m, $L_{\text{gate}} = 0.25\ \mu$m, and $L_{\text{drift}} = 0.875\ \mu$m at $V_{\text{GS}} = 0\ V$ and $V_{\text{DS}} = 26\ V$, (b) in the SJ-MGFET with $L_{\text{ch}} = 0.25\ \mu$m, $L_{\text{gate}} = 0.5\ \mu$m and $L_{\text{drift}} = 1.75\ \mu$m at $V_{\text{GS}} = 0\ V$ and $V_{\text{DS}} = 48\ V$, and (c) in the SJ-MGFET with $L_{\text{ch}} = 0.5\ \mu$m, $L_{\text{gate}} = 1.0\ \mu$m, and $L_{\text{drift}} = 3.5\ \mu$m at $V_{\text{GS}} = 0\ V$ and $V_{\text{DS}} = 65\ V$.

5.6 Gate Capacitance Extractions Using AC Analysis

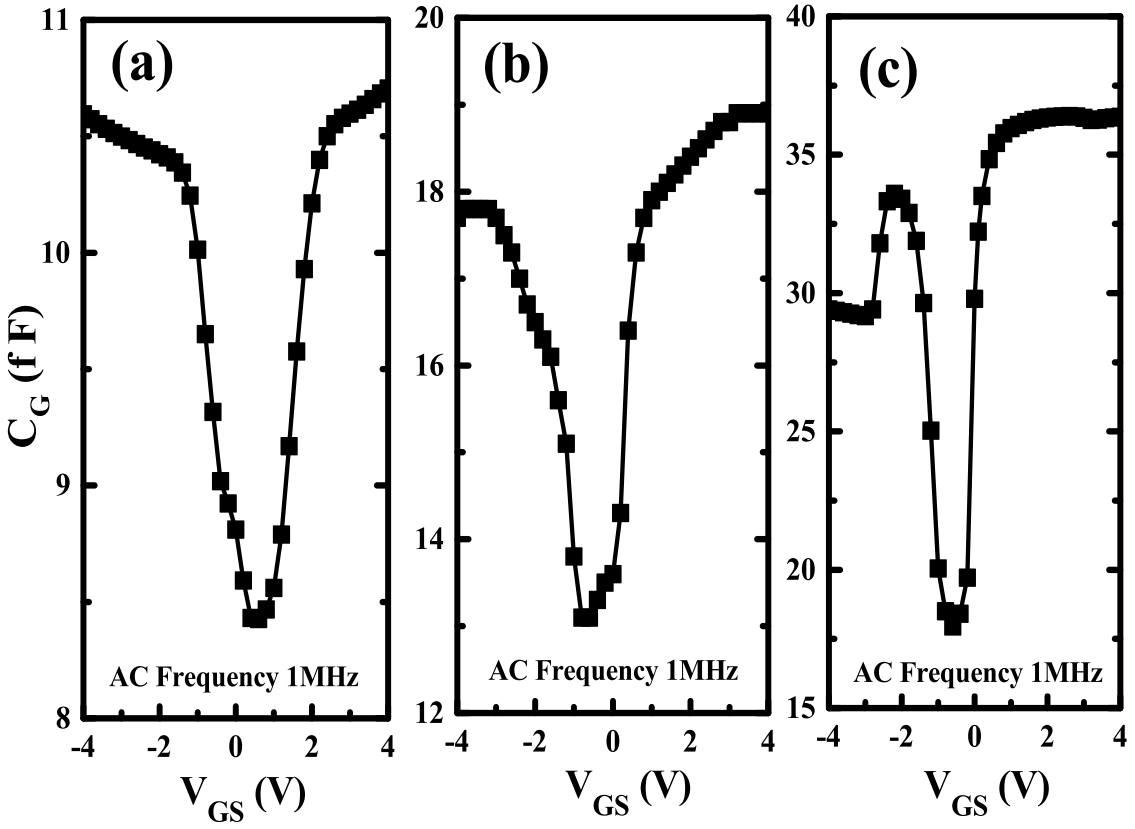


Figure 5.9: Gate capacitance plotted as a function of gate-source voltage V_{GS} at a small signal $A.C$ analysis of 1 MHz for (a) the 1.0 μm gate length SJ-MGFET having a channel length of 0.5 μm and a drift region length of 3.5 μm, (b) the 0.5 μm gate length SJ-MGFET having a channel length of 0.25 μm and a drift region length of 1.75 μm, and (c) the 0.25 μm gate length SJ-MGFET having a channel length of 0.125 μm and a drift region length of 0.875 μm.

In the simulations, the C-V analysis is carried out with a small signal $A.C$ response by performing a two carrier solution, thereby extracting the gate overlap capacitances in the SJ-MGFETs devices with L_{gate} of 1.0 μm, 0.5 μm, and 0.25 μm, respectively. A gate capacitance (C_{G}) as a function of the gate bias for the three scaled device structures is shown in Figure 5.9. During the on-state, with the gate reverse biased, the p-body situated closer to the gate is switched on to accumulation mode which is the most pronounced in a structure with the thinnest gate oxide while at the same time maintains the n-pillar in inversion mode. When the gate is forward biased, the p-body area changes to inversion mode and the n-pillar switches to accumulation mode. It is observed that the 0.25 μm gate length SJ-MGFET has the

most elongated penetration of the drain-to-channel depletion layer under the gate because of the shortest L_{ch} and the thinnest t_{ox}. An overall C_{G} of approximately 0.01 pF, 0.02 pF, and 0.04 pF is achieved in conformity with the scaling ratio of 1 : 0.5 : 0.25, respectively.

5.7 Bias Dependence of the Capacitance

A 3-D numerical simulation using an $A.C$ signal at 1 MHz is investigated to shows the dependence of the output (C_{oss}) and reverse transfer (C_{rs}) capacitances on the drain voltage (V_{DS}) in the SJ-MGFETs devices with L_{gate} of 1.0 μm, 0.5 μm, and 0.25 μm, respectively. Figure 5.10 depicts the dependence of output (C_{oss}) and reverse transfer (C_{rs}) capacitances on the drain voltage (V_{DS}).

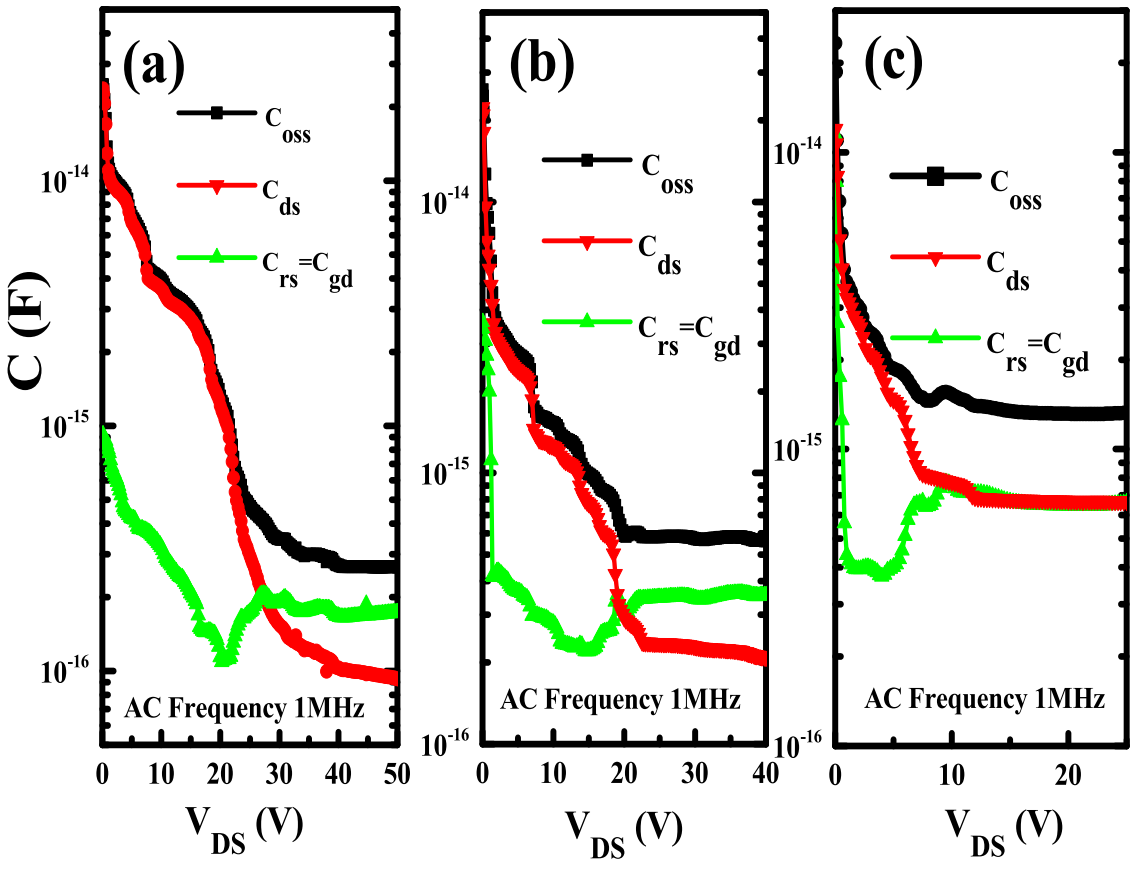


Figure 5.10: The dependence of C_{oss}, C_{rss} and C_{ds} on V_{DS} at a small $A.C$ signal analysis of 1 MHz for (a) the 1.0 μm gate length SJ-MGFET having a channel length of 0.5 μm and a drift region length of 3.5 μm, (b) the 0.5 μm gate length SJ-MGFET having a channel length of 0.25 μm and a drift region length of 1.75 μm, and (c) the 0.25 μm gate length SJ-MGFET having a channel length of 0.125 μm and a drift region length of 0.875 μm.

A non-linearity of the output and the reverse transfer capacitances (C_{oss} and C_{rs}) can be seen as a result of their strong dependence on the depletion width, in which the drain voltage plays a dominant factor. It is observed that, as the drain voltage increases in the three device structures, the gate-drain capacitance (C_{gd}) plays a major role in a total effect of C_{oss} in the devices.

5.8 Dependence of the Transconductance on the Gate Voltage

The transconductance (g_m) is extracted from the transfer (I_{D} - V_{GS}) characteristics during on-state simulations in the SJ-MGFETs devices with L_{gate} of 1.0 μm, 0.5 μm, and 0.25 μm, respectively. Figure 5.11 shows the dependence of transconductance (g_m) on the gate voltage in the three scaled device structures at $V_{\text{DS}} = 0.1\ V$.

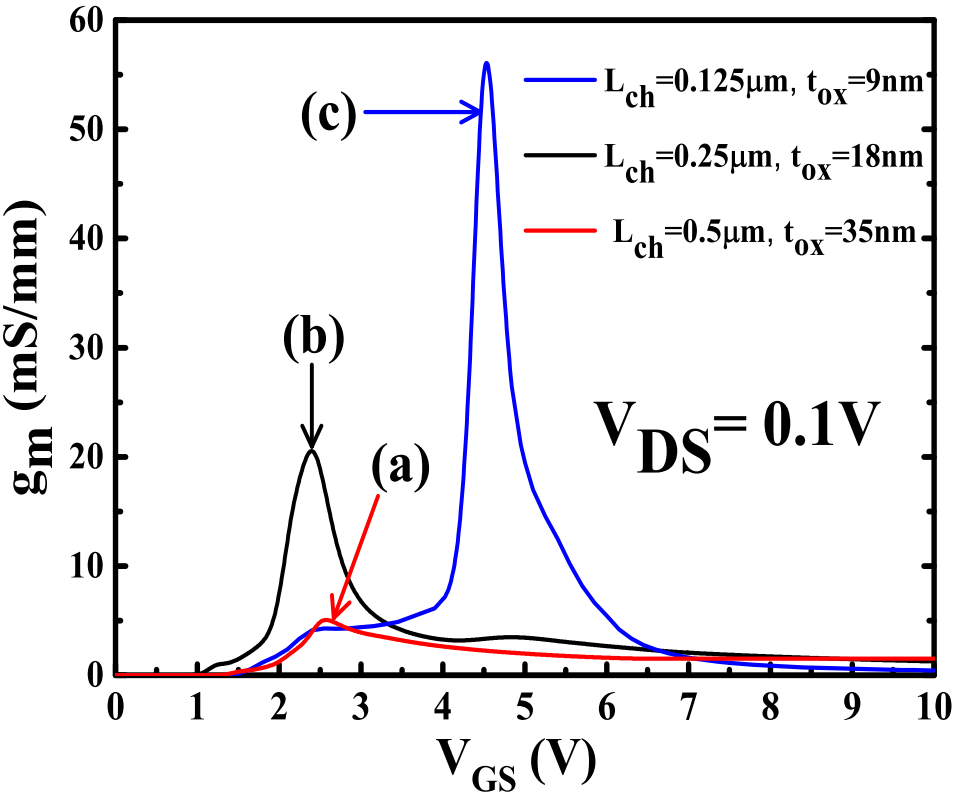


Figure 5.11: Transconductance of the three device structures for (a) the 1.0 μm gate length SJ-MGFET having a channel length of 0.5 μm and a drift region length of 3.5 μm, (b) the 0.5 μm gate length SJ-MGFET having a channel length of 0.25 μm and a drift region length of 1.75 μm, and (c) the 0.25 μm gate length SJ-MGFET having a channel length of 0.125 μm and a drift region length of 0.875 μm.

The transconductance (g_m) per device width increases with shorter L_{ch} and thinner t_{ox}. The following maximum transconductance for three scales SJ-MGFETs has been extracted at $V_{\text{DS}} = 0.1\ V$: (a) g_m of 5 mS/mm for the device with $L_{\text{ch}} = 0.5\ \mu$m, $L_{\text{gate}} = 1.0\ \mu$m and $t_{ox} = 35\ nm$, (b) g_m of 20 mS/mm for the device with $L_{\text{ch}} = 0.25\ \mu$m, $L_{\text{gate}} = 0.5\ \mu$m and $t_{ox} = 18\ nm$; and (c) g_m of 56 mS/mm for the device with $L_{\text{ch}} = 0.125\ \mu$m, $L_{\text{gate}} = 0.25\ \mu$m and $t_{ox} = 9\ nm$. The SJ-MGFET scaled down to $L_{\text{gate}} = 0.25\ \mu$m with the thinnest t_{ox} shows the highest transconductance resulting in a larger RF gain having an intrinsic voltage gain (A_v) of 0.16 extracted at $V_{\text{GS}} = 4.5\ V$ and $V_{\text{DS}} = 0.1\ V$ [28, 29]. The cut-off frequency (f_T) [30, 31] can be obtained as:

$$f_T = \frac{g_m}{2 \cdot \pi \cdot (C_{\text{gs}} + C_{\text{gd}})} \tag{5.6}$$

The maximum operating frequency achieved at $V_{\text{DS}} = 0.1\ V$ are 0.2 GHz for the device with $L_{\text{gate}} = 1.0\ \mu$m, 0.6 GHz for the device with $L_{\text{gate}} = 0.5\ \mu$m, and 0.9 GHz for the device with $L_{\text{gate}} = 0.25\ \mu$m, respectively.

5.9 Transient Simulation of the Scaled SJ-MGFETs functioning as a Switch

The transient switching turn-on simulation is investigated by performing a two carrier solution when SJ-MGFETs with L_{gate} of 1.0 μm, 0.5 μm, and 0.25 μm act as a switch in a circuit when biases between cut-off and saturation regions as shown in Figure 4.12. Figure 5.12 shows a comparison of performance of the three scaled transistors during switching turn-on simulations when the devices are operated ramped to $V_{\text{DD}} = 10.0\ V$ and $V_{\text{GS}} = 10.0\ V$, neglecting a circuit resistance R_c and a stray inductance L_s. Thus, the SJ-MGFETs with L_{gate} of 0.5 μm and 0.25 μm offer a switching turn-off time (t_{off}) of approximately 0.2 ns and 0.05 ns, respectively, compared with the 1 ns (t_{off}) in the SJ-MGFET with 1 μm gate length.

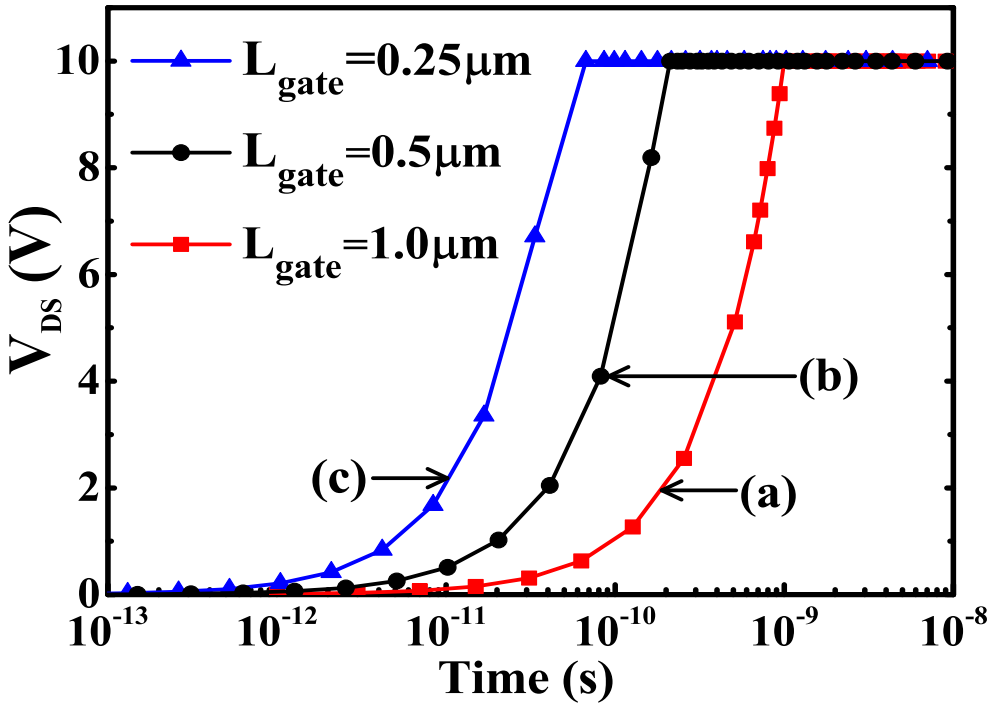


Figure 5.12: Switching waveforms of the SJ-MGFET turn-on simulations with a device ramped to $V_{\text{DS}} = 10\ V$ and $V_{\text{DS}} = 10\ V$ for (a) the device with $L_{\text{ch}} = 0.5\ \mu$m, and $L_{\text{gate}} = 1.0\ \mu$m; (b) the device with $L_{\text{ch}} = 0.25\ \mu$m, and $L_{\text{gate}} = 0.5\ \mu$m; and (c) the device with $L_{\text{ch}} = 0.125\ \mu$m, and $L_{\text{gate}} = 0.25\ \mu$m.

5.10 Trade-Off Between the Specific On-Resistance and the Breakdown Voltage

The trade-off between BV and $R_{on,sp}$ for the simulated SJ-MGFETs scaled down to 0.5 μm and 0.25 μm gate lengths are compared with the ideal silicon limit and with various conventional LD-MOSFETs in Figure 5.13. The simulations show that the SJ-MGFET with 0.25 μm gate length achieves a low $R_{on,sp}$ ($V_{\mathrm{GS}} = 10\ V$) of 2.24 $m\Omega.mm^2$ and $BV = 26\ V$ with $L_{\mathrm{drift}} = 0.875$ μm and the SJ-MGFET with 0.5 μm gate length offers a $R_{on,sp}$ ($V_{\mathrm{GS}} = 10\ V$) of 7.68 $m\Omega.mm^2$ and $BV = 48\ V$ with $L_{\mathrm{drift}} = 1.75$ μm, respectively. The SJ-MGFET scaled to the 0.5 μm gate length leads to 16% reduction in $R_{on,sp}$ compared to super-junction UMOSFET (SJ-UMOSFET) at the same BV rating [32], 73% reduction compared to Floating RESURF (FRESURF) at the same BV rating [33], 78% reduction compared to dual RESURF LDMOS at the same BV rating [34], and 85% reduction compared to isolated low nLDMOS at the same BV rating [35]. The SJ-MGFET scaled to the 0.25 μm gate length has $R_{on,sp}$ lower by 90% compared to isolated low nLDMOS [35] at the same breakdown voltage rating.

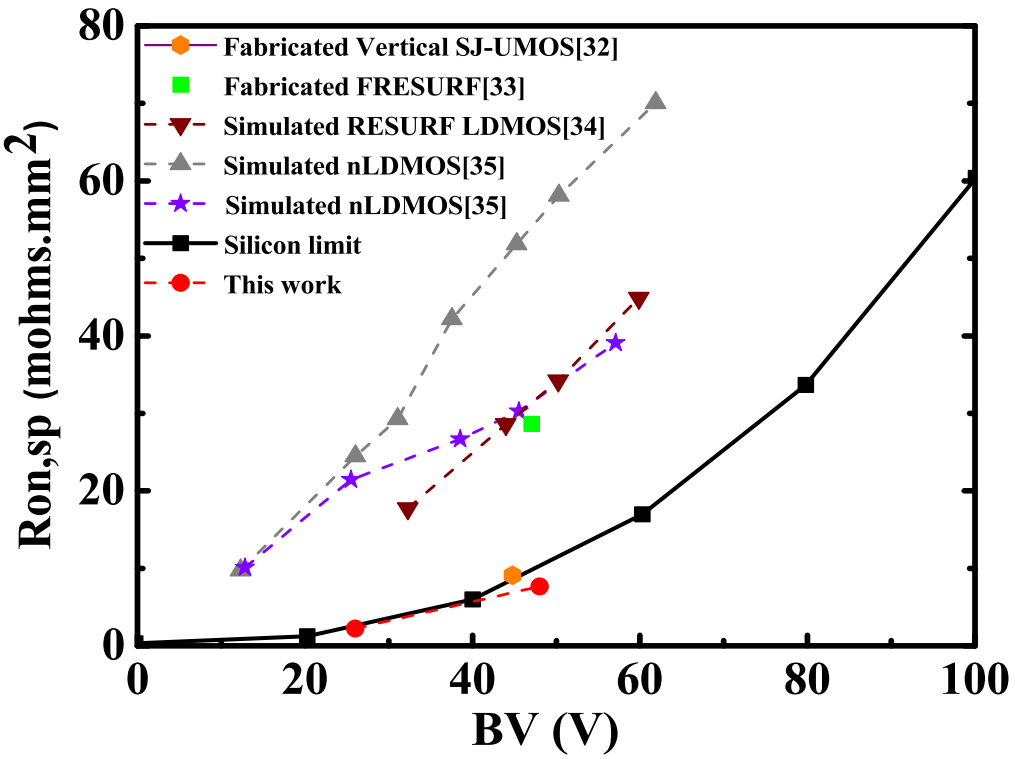


Figure 5.13: Specific on-resistance as a function of the breakdown voltage of the scaled down SJ-MGFET compared with reported conventional LDMOSFETs and SJ-LDMOSFETs [32–35].

The SJ-MGFET scaled to 0.5 μm gate length offers superior performance in term of high drive current, switching speed, breakdown voltage (BV) and specific on-resistance ($R_{on,sp}$) compared with the 1 μm gate length SJ-MGFET. The combination of these fourfold benefits with the reduction in device dimensions suggests a better architecture design in achieving a larger number of transistors per chip and a higher integration. Although, the SJ-MGFET scaled to the 0.25 μm gate length achieves the largest device dimension reduction with a vastly superior drive current and improved transconductance. However, the extreme scaling of the gate oxide thickness and decrease in the channel length limits the device voltage-sustaining capability. In addition, a fabrication of the aligned deep trenched gate structure with a small channel length within the non-planar SOI power technology is challenging, costly and technologically limited.

5.11 Conclusion

The scaling of non-planar SJ-MGFETs following conventional scaling rules [36, 37] requires a subsequent optimisation of their SJ unit. The lateral scaling and optimisation of the 1 μm gate length SJ-MGFET to gate lengths of 0.5 μm and 0.25 μm using Silvaco TCAD simulations has shown that the FoM of this non-planar transistor can be substantially improved including physical density, switching speed, drive current, breakdown voltage and specific on-resistance ($R_{on,sp}$). The scaling and optimisation of the overall device design have achieved a low specific on-resistance of 7.68 $m\Omega.mm^2$ and 2.24 $m\Omega.mm^2$ ($V_{\mathrm{GS}} = 10\ V$), and breakdown voltages of 48 V and 26 V for the 0.5 μm and 0.25 μm gate length SJ-MGFETs, respectively. The investigations have also shown that excessive channel doping in the scaled SJ-MGFETs offers no significant improvement in the device avalanche capability during charge balanced condition. With the twofold benefits of device dimension reduction and optimised fully-depleted SJ multi-gate architecture, the transistor can offer a superior performance in achieving a higher levels of integration, a maximum breakdown voltage, a minimum specific on-resistance, and excellent FoM in sub - 50 V applications.

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Chapter 6

Conclusions

The variations in the device architecture of a 1 μm gate length lateral super-junction (SJ) Multi-Gate MOSFET (SJ-MGFET) is explored using Silvaco 3-D TCAD simulations. In an effort to optimised the SJ-MGFET, the effect of charge imbalance on the breakdown voltage of the device during off-state using two different SJ drift regions length is examined. The results show that variations along the drift region has no effect on the charge imbalance due to the fixed ratio between the cross-sectional area of the two SJ pillars. The optimised SJ-MGFET delivers a 41% increase in the drive current with an on-off ratio of 5×10^6 at a drain voltage voltage of 10 V and a gate voltage of 20 V, thereby exhibiting a big advantage of the multi-gate device design to reduce leakage current.

In order to mitigate the effect of self-heating in the structure, a variation in the silicon-on-insulator (SOI) based design by replacing the fully deplored buried oxide (BOX) layer with a partial BOX with opening under the drain creating a thermal window is investigtaed. It has been reported that the current decrease in partially buried oxide (thermal window) architecture at a gate bias of 10 V and a drain voltage of 50 V is less than 3%, compared to about 7.5% seen in a fully deplored buried oxide design. The C-V analysis with a small signal AC response is performed with a two carrier solution. The C-V analysis has given a gate capacitance of approximately 0.01 pF with a turn-off time of approximately 1.0ns. In addition, the dependence and the non-linearity of the output and reverse capacitances on the drain bias is highlighted.

It has been reported that the simulated SJ-MGFET has a specific on-resistance of 0.21 $m\Omega.\text{cm}^2$ and a breakdown voltage of 65 V with a pillar height of 3.6 μm and a drift region length of 3.5 μm. Additionally, it has been reported that the

optimised SJ-MGFET has achieved 68%, 52%, and 15% reduction in the specific on-resistance compared to reported fabricated SJ-LDMOSFET, fabricated SJ-FinFET, and simulated SJ-FinFET at the same breakdown voltage rating. In conclusion, the 1 μm gate length SJ-MGFET is capable of offering a better performance in terms of a high drive current, a maximum breakdown voltage, a minimum specific on-resistance, and excellent FoM for sub - 100 V rating applications.

In the second part of the thesis, the scaling of the device architecture of the optimised 1 μm gate length super-junction (SJ) multi-gate MOSFET (SJ-MGFET) is investigated. The 3-D effects of transistor scaling by a factor S is carefully examined. The SJ-MGFET structure with 1.0 μm gate length is scaled down laterally (along the y-axis) by scaling the channel length, the gate length, the gate oxide thickness, and the SJ drift unit length shrinking the gate length of 1.0 μm to 0.5 μm, and 0.25 μm. The effect of charge imbalance on the breakdown voltage in the scaled devices during off-state is investigated, and reported that the avalanche capability of the scaled devices improves with a fully depleted SJ drift region.

The drive current in the scaled SJ-MGFET gate lengths of 0.5 μm and 0.25 μm increases by 30% and 63%, respectively, in comparison with the reported 1.0 μm gate length SJ-FinFET at a drain voltage of 0.1 V and a gate voltage of 15 V. The effect of electric field distribution in the scaled and optimised devices is examined. The 0.5 μm gate length device has a breakdown voltage of 48 V, which corresponds to an average lateral electric field of 27.5 $V/\mu m$ with a drift region length of 1.75 μm and the 0.25 μm gate length device exhibits a breakdown voltage of 26 V, which corresponds to an average lateral electric field of 30 $V/\mu m$ with a drift region length of 0.875 μm. The investigations have also shown that excessive channel doping in the scaled SJ-MGFETs offers no significant improvement in the device avalanche capability during charge balanced condition.

Analysis of the simulated C-V shows that the non-linearity of the output and reverse capacitances on the drain bias in the scaled and optimised devices. Gate capacitances of approximately 0.02 pF and 0.04 pF are extracted in the scaled SJ-MGFETs with a gate length of 0.5 μm, and 0.25 μm, respectively, in conformity with the scaling ratio of 0.5 : 0.25. In addition, the dependence of transconductance on the gate voltage in the three device structure is highlighted, and a maximum transconductance of 5 mS/mm, 20 mS/mm, and 56 mS/mm is extracted at a drain bias of 0.1 V in the SJ-MGFETs with a gate length of 1 μm, 0.5 μm and

0.25 μm, respectively. The performance of the three scaled devices during transient switching turn-on transient is examined at a drain bias of 10 V and a gate voltage of 10 V. The transient switching turn-on time of approximately 1.0ns, 0.2ns, 0.05ns in the SJ-MGFETs is obtained with a gate length of 1 μm, 0.5 μm, and 0.25 μm, respectively.

The simulation shows that the SJ-MGFET with the 0.5 μm gate length achieves a specific on-resistance of 7.68 $m\Omega.mm^2$ and a breakdown voltage of 48 V, and that the 0.25 μm gate length offers a low specific on-resistance of 2.24 $m\Omega.mm^2$ and a breakdown voltage of 26 V. The twofold benefits of device dimension reduction and optimised fully-depleted SJ multi-gate design are highlighted, the scaled and optimised SJ-MGFET can offer a superior performance in achieving higher levels of integration, a maximum breakdown voltage, a minimum specific on-resistance, and excellent FoM in sub - 50 V applications.