CORE
Metadata, citation and similar papers at core.ac.uk
Provided by University of Liverpool Repository

A Framework for TSV based 3D-IC to Analyze Aging and TSV Thermo-mechanical stress on Soft Errors

Raviteja P Reddy*, Amit Acharyya* and Saqib Khursheed+
* Department of Electrical Engineering, Indian Institute of Technology, Hyderabad, India.
{ee15resch11006, amit_acharryya}@iith.ac.in
+Department of Electrical Engineering and Electronics, University of Liverpool, U.K.
S.Khursheed@liverpool.ac.uk

***Abstract*— The CMOS aging, transient effects, and TSV thermomechanical stress degrade the resilience of 3D-ICs. The transients effects lead to soft errors and aggravated with the CMOS Bias temperature instability (BTI). In this paper, we analyze detrimental transient and BTI effect on soft error rate (SER) in 3D-ICs. However, TSV thermomechanical stress presents a considerable benefit by enhancing the critical charge (Q_c) and reduce the SER due to decrease in the threshold voltage and increase in mobility of carriers in transistor present out of keep-out-zone and useful range. Therefore we propose a framework to evaluate the effect of transient, BTI, and TSV thermomechanical stress on critical charge and SER in 3D-ICs. Subsequently, through HSPICE simulation we show that for a lifetime of ten years and on the topmost layer of stacked 3D-IC, the reduction in SER of NAND gate by 5.12% – 9.05% and in 6T SRAM 2.51% – 4.76% and 3.77% – 5.64% decrease for storing 0 and 1 respectively.**

***Index Terms*—3D-IC, Through-silicon via (TSV), Resilience, BTI, and SER.**

I. INTRODUCTION

The Through-Silicon-Via [1] based stacked 3D integrated circuits facilitate heterogeneous computing systems. However, the decrease in the foot-area and increase in power density leads to thermal and resilience issues, which are hindrances in the bulk production of 3D-ICs. Designing resilient systems in accordance with intended functionality with aging and radiation effects is a daunting task for the system designers. In 3D-ICs TSV thermo-mechanical stress and CMOS temporal unreliability effects the resilience of 3D-IC. The temporal unreliability of CMOS transistors present in 3D-ICs is due to aging and transient effects, as shown in Fig. 1. The bias temperature instability (BTI) is caused by charge trapping and interface–state generation [3]. The threshold voltage of PMOS transistor increases by 50mV over ten years due to NBTI and resulting in deprivation of the circuit performance by 20% [4]. The other temporal unreliability factor is single event transients. It affects the data-paths of high-performance computing system by changing the values stored in the flip-flops. This leads to an improper sampled value and gives rise to soft errors (SE). The integrated circuit susceptibility to single events transients is aggravated further by BTI [5]. BTI effect results in the increase in the threshold voltage of the transistor and which in turn decreases the critical charge (Q_c) at the nodes [5]. The decrease in the Q_c at the sensitive nodes results in increases of SE and a decrease in the noise margin, thus giving rise to more SE [6, 7]. On the other hand, TSV undergoes thermo-mechanical stress during its fabrication process,

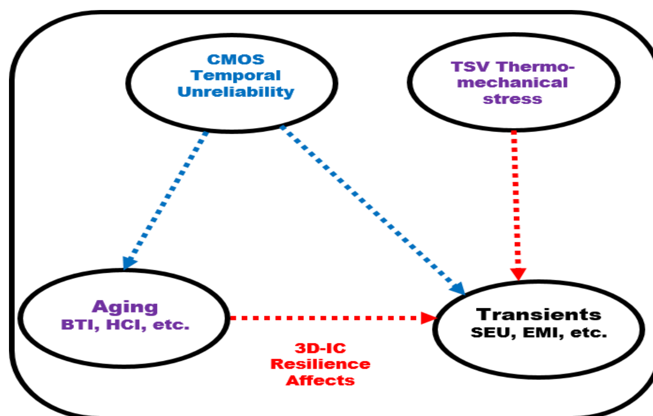

Fig. 1. Various factors affecting stacked 3D-IC Resilience

as well as in the post-fabrication due to the discrepancy in coefficients of thermal expansion (CTE) between copper and silicon dioxide. The fabrication process of TSV is done with copper filling, and thereafter TSV passes through layers of silicon after thermal cycling and final annealing process. Subsequently, after annealing and cooling the TSV undergoes thermal variation from 250ºC to the room temperature, leading to residual stress surrounding the TSV. This residual thermal stress in silicon leads to the variation in the threshold voltage and affects the mobility of carriers in the transistors [2]. This, in turn, affects the Q_c critical charge and subsequently leads to soft error in 3D-ICs. The only work that addresses resilience in 3D-IC due to the soft error at the micro-architecture level of 3D-IC is presented in [8], however it did not consider the effect of circuit level technology vulnerable factors in terms of aging and TSV thermo-mechanical effect. Therefore this necessitates a comprehensive analysis of CMOS temporal unreliability and TSV thermo-mechanical stress effect on SER in stacked 3D-IC for designing resilient 3D-IC systems.

To the best of our knowledge, this is the first study to evaluate the CMOS aging and TSV thermo-mechanical stress effect on soft error susceptibility of 3D-IC. Initially, CMOS aging effect in stacked 3D-IC is analyzed for the critical charge at various lifetime. It is observed that critical charge decreases with aging due to an increase in the threshold voltage. SER evaluated for the respective critical charge on different stacked 3D-IC layers increases SER and thus affected the resilience of 3D-IC. Subsequently, the combined effect of CMOS aging and TSV thermo-mechanical stress is analyzed for the critical charge at various lifetime, which leads to enhanced critical charge compared to only aging effect into consideration. The increase of the threshold voltage of the transistor due to the BTI

effect is compensated by an increase in mobility and a decrease in threshold voltage due to TSV thermo-mechanical stress. Hence, the increased critical charge leads to the reduction in the SER of 3D-IC on various stacked layers of 3D-ICs in contrast to only aging effect into consideration. For a lifetime of 10 years, we evaluated the critical charge and SER for two input NAND gate and 6T SRAM nodes for storing 1 and 0. It is observed that for two input NAND gate 5.12% – 9.05% decrease in SER with aging and TSV stress effect consideration in comparison to aging alone. Similarly, for 6T SRAM for storing 1 resulted in 3.77% – 5.64% decrease in SER, and for storing 0 resulted in 2.51% – 4.76% decrease in SER is observed. Therefore, the proposed framework and analysis can be applied to any node to evaluate the soft error susceptibilities and design heterogeneous resilient 3D-ICs.

The rest of the paper is organized as follows. Section II discusses the motivational background and provides the details of the bias temperature instability. In Section III, we present the proposed framework, the effect of TSV thermo-mechanical stress on the threshold voltage and mobility variation of carriers in transistors, critical charge, and soft error rate evaluation. In Section III, simulation results are presented for soft error rate of NAND and 6T SRAM. Finally, Section IV concludes the paper.

II. Motivational Background

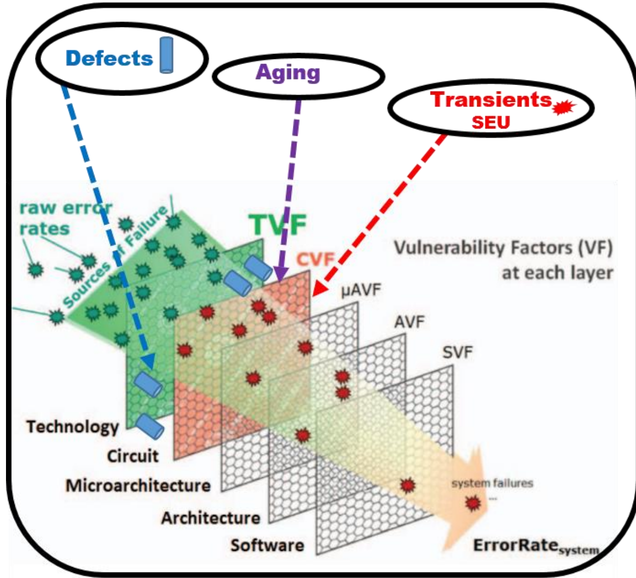

Fig. 2. Resilience effects at different abstraction levels [25]

Fig. 2 shows different abstraction levels in system design. The resilience of a system at various levels can be effected due to aging, hard errors, and soft error. The error at any one of the abstraction level results in system error and adversely affect the complete resilience of the system. The only work that addresses resilience in 3D-IC due to the soft error susceptibility at the micro-architecture level of 3D-IC is presented in [8] but did not consider the effect of circuit level technology vulnerable factors in terms of aging and TSV thermomechanical effect. Whereas at the micro-architecture level the overall soft error rate depends on the architecture vulnerability factor (AVF) and circuit soft error rate (SER_{RAW}) as presented in [11] and shown in equation (1). Hence, this motivates us to develop a proper framework to evaluate the aging and TSV thermo-mechanical effect on circuit SER_{RAW} of 3D-ICs, such that it gives proper insights to the resilient 3D-IC micro-architecture design.

$$SER = SER_{RAW} \text{ x AVF} \quad (1)$$

At the technology level (Fig. 2) of 3D-IC, the defects in the TSV are the source of hard errors. The defects in TSV arises during the copper filling or in the dielectric layer around the TSV during the fabrication, and these defects are permanent once manifested. For example, short circuit and open circuit in the TSVs due to improper metallization during fabrication. The state-of-the-art solution for hard errors is fault-tolerant architectures [9, 10], which can tolerate the defects in TSVs by re-routing through defect-free regular or redundant TSV.

The circuit level abstraction (Fig. 2) is effected by the transient effects and which gets aggravated with the aging of transistors. The aging effect in CMOS is due to bias temperature instability (BTI). BTI increases the threshold voltage of transistors during the stress phase (On state). In the recovery phase, the BTI induced degradation is recovered when the MOS transistor is partially polarized. In accordance with the reaction-diffusion model [3], the origination of BTI due to the creation of charges trapped at the dielectric and silicon interface during the On state. The traps present at the dielectric and silicon interface shield the gate voltage applied and increases the threshold voltage of the transistors. The traps generated are partially annealed [3] during the recovery phase. In pMOS transistors, negative BTI (NBTI) is observed, and it dominates over nMOS transistor positive BTI (PBTI) [11, 3]. To find the threshold voltage shift, an analytical model is presented in [11, 12] and shown in (2). Where C_{ox} is oxide capacitance parameter, t is operating time, α is the fraction of the operating time during the stress phase of the MOS transistor, Boltzmann constant k, device temperature is T and fitting parameter $E_a \approx 0.08$ [5]. The environment parameter and technology-specific $K \approx 2.7\ V^{1/2} F^{-1/2} S^{-1/6}$ [13]. The NBTI ($\chi = 1$) dominates over PBTI ($\chi = 0.5$) [11] based on the coefficient χ.

$$\Delta V_{th} = \chi\, K\, (C_{ox}\, (V_{dd} - V_{th}))^{1/2}\, e^{(-Ea_{EM}/kT)}\, (\alpha t)^{1/6} \quad (2)$$

In the view of above, it can be concluded that error at any one of the abstraction levels propagates and result in system error as shown in Fig. 2. However, there is no work to address the circuit level SER. Hence, in this paper, we study the impact of aging and TSV thermo-mechanical effect on SER of 3D-IC.

III. Proposed Framework

Fig. 3 shows the overall flow of the proposed framework. Initially a spice circuit is designed with all the configuration parameters like for voltage, temperature and the input stored at the sensitive nodes. The alpha particle strike is modeled as a pulse cell input. The transistor aging effect due to BTI degradation is based on the analytical model [3] and CMOS predictive technology model [24]. Whereas, the TSV thermomechanical effect on the threshold voltage and mobility variation is based on the analytical model [2] and stored in the lookup table. The circuit configuration parameters, aging effects and TSV thermomechanical effects are given as input to the SPICE simulator. Subsequently, critical charge at the sensitive nodes is obtained from the simulator. Finally, we evaluate the soft error rate (SER) at the various sensitive nodes in the circuit and on the different layers of stacked 3D-IC.

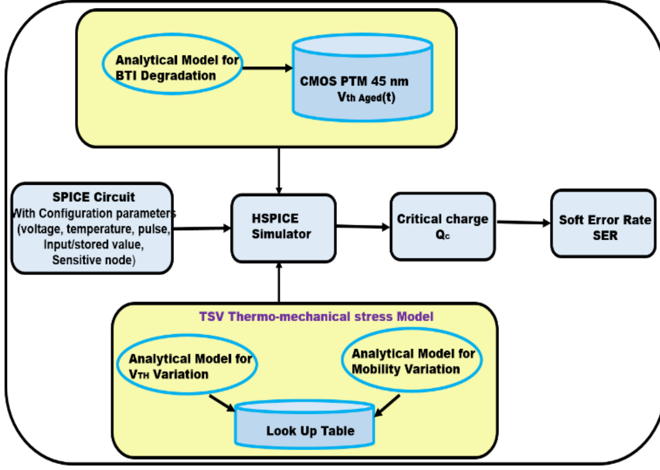

Fig. 3. Simulation flow of the proposed framework

A. Threshold Voltage and Mobility variation due to TSV Thermomechanical stress

The mechanical strain generated from the TSV changes the structures of the band in the semiconductors [14] and leads to the changes in the electrical parameters like threshold voltage and mobility of the carriers in the transistor. In this section, we present the state-of-the-art analytical models for threshold voltage and mobility variations due to TSV induced stress.

According to the many valley theory in the unstrained silicon, there exists six degenerate conduction band valley, and the valence band contains two degenerate electronic bands. Thus, the TSV induced strain lift the degeneracies of valance and conduction bands valleys and leads to the shift in the band potentials. Thus, mobility change is attributed to intervalley scattering, and strain induced effective carrier change [14]. The threshold change is related to the strain induced shifts in valence and conduction band potentials [14, 15]. In silicon, band potentials are defined along the direction of <100> miller notation [14]. The orientation of the transistor channel with the crystallographic axes determine the properties of carrier transportation in transistors and thus the magnitude of mobility variations. The mobility variations depend on the effective mass of the carriers and the scattering mechanism as per the Drude's model [14] and shown in equation (3).

$$\mu = e\, \tau / m^* \quad (3)$$

The above equation gives the mobility in terms of mean free time between relaxation or scattering τ, a charge of the carrier e and effective mass of the charge carrier m*. In the PMOS and NMOS transistor, the charge carriers are holes and the electrons respectively. The band splitting leads to the scattering mechanism and results in the increase of τ and consequently the mobility. The decrease in the effective mass also increases mobility. In our analysis, we use the analytical model presented in [2] with mobility variations in the PMOS and NMOS transistor at room temperature (25°C), transistor oriented along the [110] axis and shown in the equation (4). The piezoresistivity coefficients (Π') [2] and the stress components (σ) [2] change with the channel orientation, this indicates that transistor channel orientation is directly related to mobility variation, as well as directly related to temperature, as the stress directly related to temperature.

$$\Delta\mu / \mu = \Pi'_{11}\, \sigma_{x'x'} + \Pi'_{12}\, \sigma_{y'y'} = \Pi'_{44}\, \sigma_{x'x'} \quad (4)$$

Similarly, TSV thermomechanical strain affects the transistor channel by splitting and lifting the degeneracy in the conduction band and the valence band potentials in accordance with the deformation potential theory [14-16]. This results in the corresponding shift in the transistor threshold voltage. The variation in the threshold voltage can be expressed as the function of bandgap potentials. Thus, presented as the function of conduction and valence band for PMOS and NMOS transistors in the following equations:

$$\Delta V_{Th\,p} = (m\Delta E_C - (m\text{-}1)\Delta E_V) / q \quad (5)$$

$$\Delta V_{Th\,n} = (m\Delta E_V - (m\text{-}1)\Delta E_C) / q \quad (6)$$

Where $\Delta V_{Th\,p}$ and $\Delta V_{Th\,n}$ are the threshold voltage of PMOS and NMOS transistor, respectively. The electron charge $q=1.6\times10^{-19}$ coulomb and the body effect coefficient m in the range of 1.1-1.4. ΔE_C is the change in the conduction band potential and it is lowered under the TSV induced stress and it results in the negative value. ΔE_V is the maximum change in the valance band potential and positive valued. Thus, TSV related-thermo-mechanical stress is leading to a decrease in band potentials in accordance with [17, 18], and it affects threshold voltage. The state-of-the-art analytical model, the variation in the threshold voltage of PMOS and NMOS transistor at room temperature (25oC), decreases [2]. The positive shift in the PMOS and negative shift in NMOS mobility is observed in [2].

B. Aging and TSV Thermomechanical stress effect on Q_c

We jointly find the CMOS aging effects and TSV thermomechanical stress effects on the critical charge at the sensitive nodes. The threshold voltage shift ΔV_{th} of pMOS/nMOS transistor is caused by NBTI/PBTI degradation is shown in equation (2) and presented in section II. The alternating stress (ON) and the recovery phase(OFF) are considered in the simulation phase with an input switching activity of 50% and a lifetime of 2, 5, and 10 years. The voltage shift estimated ΔV_{th} for various lifetimes has been included in the SPICE simulation by 45nm predictive technology model (PTM) [24]. In the analysis, we assume that transistor always work in the velocity saturation condition [19] at time t=0 is

$$I^o_{Dn} = I^o_{Dp} => W_{eq\,n}\, C_{ox} [\, V_{GS\,n} - V^o_{Th\,n}]\, v_{sat\,n} = W_{eq\,p}\, C_{ox} [\, V_{GS\,p} - |V^o_{Th\,p}|\,]\, v_{sat\,p} \quad (7)$$

Where $V_{GS\,p}$ and $v_{sat\,p}$ ($V_{GS\,n}$, $v_{sat\,n}$) is the voltage difference between gate-source and velocity saturation of the pMOS (nMOS) transistor respectively. $V^o_{Th\,p}$ ($V^o_{Th\,n}$) is the threshold voltage of the pMOS (nMOS) transistor at time t = 0. C_{ox} is the oxide capacitance per unit area. W_{eq} is the equivalent channel width of the transistor. Specifying $K_{eq} = W_{eq\,n}\, C_{ox}\, v_{sat}$, the above equation can be written as follows:

$$K_{eq\,n} [V_{GS\,n} - V^o_{Th\,n}] = K_{eq\,p} [\, V_{GS\,p} - |V^o_{Th\,p}|\,] = I^o_D \quad (8)$$

The drain current of the pMOS and nMOS transistor with the aging of transistor caused by BTI degradation at time instant t are shown in equation (9, 10). The variation in the transistor threshold voltage is obtained from equation (2).

$$I_{D\,p}(t) = K_{eq\,p}[V_{GS\,p} - (|V^o_{Th\,p} - V_{Th\,p}(t)|] = I^o_D - K_{eq\,p}\, V_{Th\,p}(t) \quad (9)$$

$$I_{D\,n}(t) = K_{eq\,n}[V_{GS\,n} - (V^{o}_{Th\,n} - V_{Th\,n}(t))] = I^{o}_{D} - K_{eq\,n} V_{Th\,n}(t) \quad (10)$$

Finally, we evaluate critical charge by considering BTI degradation and TSV thermo-mechanical stress as shown in the below equation.

$$Q_{crtical} = \int_0^T I'_D(t)\,dt = \int_0^T I_D(t)\,[1 + (\Delta u/u)_h]\,dt \quad (11)$$

Where $I_D(t)$ and change in mobility in equation (11) are obtained from equation (12) and (4) respectively.

$$I_D(t) = K_{eq\,p}[V_{GS} - (|V_{Th} - \Delta V_{Th\,BTI} + \Delta V_{Th\,Stress}|)] = I^{o}_{D} - K_{eq}[|V_{Th} - \Delta V_{Th\,BTI} + \Delta V_{Th\,Stress}|] \quad (12)$$

In the above equation, change in threshold voltage due to BTI is obtained from (2) and change in threshold voltage due to stress is obtained from equations (6 and 5).

C. Soft Error Rate Evaluation

Radiation-induced failures result in soft errors and thus affect the resilience of the system. The source of radiation-induced failures are alpha particles from the atmosphere. The strike of the alpha particles leads to soft errors that have a high impact on the reliability of the circuit and thus effecting the resilience of the 3D-ICs.

The alpha particle strike of an electronic system produce an electrical charge of a certain amount. The minimum charge required to produce the glitch in the output or switch On or Off transistor or losing the stored data leads to the malfunction of the system is called the critical charge Q_{crit}. The alpha particle strike is modeled by injecting the current pulse at the sensitive nodes of an element to malfunction the circuit and subsequently Q_{crit} is estimated. In [20], a model is proposed to evaluate the soft error rate of a circuit as follows:

$$SER_{RAW} = Constant \times Flux \times Area \times e^{(-Q_{crit}/Q_{coll})} \quad (13)$$

Constant is a process technology dependent parameter; *Flux* is an alpha particles flux at a given location, *Area* is the area of the sensitive nodes, Q_{coll} is the efficiency of charge collection and depend on the doping and operating voltages and obtained empirically from device physics models or accelerated alpha particles test. Q_{crit} is obtained from the circuit simulators.

The alpha particle strike losses energy while passing through different layers of the stacked 3D-IC. The distance traveled by the particle depends on the initial kinetic energy and the number of layers. Hence, in the stacked 3D-IC particle flux decreases in the inner layers, and flux is the major factor in the evaluation of SER. Hence, leading to the heterogeneous soft error rate in stacked 3D-ICs. The aggregate flux and SER for various layers of 3D-IC are given in equation (14 and 15) [11].

$$F_{layer\text{-}1} = 62.6\,\%\,F \quad \text{---->} \quad SER_{layer\text{-}1} = SER_{RAW} \quad (14)$$

$$F_{layer\text{-}2} = 6.27\,\%\,F \quad \text{---->} \quad SER_{layer\text{-}2} = 0.1SER_{RAW} \quad (15)$$

IV. Simulation Results

The SPICE simulations are performed using HSPICE for the proposed framework. Alpha particles strike is modeled by double exponential pulse as it is the most commonly used method in SER evaluation. The drain area of the transistor is defined as the sensitive region to the alpha particle strikes and specified in the netlist of the spice circuit. The 3D-IC package dimensions and angle of strike of the particle are taken according to section-III [8]. The constant parameter used in equation (13) is a technology dependent parameter has a value of 2.2×10^{-5} [20]. The exponential part of the equation is a technology vulnerability factor [20]. The presence of various sensitive nodes in circuit or element results in the sum of SER at all the nodes [23].

The alpha particle causes a malfunction and minimal charge required for each element is called the critical charge Q_{crit}. The Q_{crit} strongly depends on the shape of the current pulse. We take the pulse width as start of the pulse and decrease up to 80% of its maximum value, which indicates the spike of the pulse. The parameter typically taken are 1V, 50°C and 2psec pulse. Subsequently, Q_{crit} is computed by integral of the current pulse in that range. After obtaining the Q_{crit}, SER is evaluated and expressed in terms of FITS (Failure in time), that is number of failure in one billion device hours of operation. The raw SER is obtained using the model in [20] for each Q_{crit}.

The variations in the mobility and threshold voltage are observed in the useful range and out of keep-out-zone of TSV. We define the KoZ of 1µm from the edge of TSV or 3.5µm with respect to center of the TSV. The useful range considered as transistor present in range of 3.5µm – 6.5µm from center of TSV. In our analysis we consider 15% mobility variation and 10 mV threshold voltage variation in the useful range [2]. The TSV height and diameter are 30µm and 5µm respectively.

The NAND gate SER analysis is done by incorporating the current pulses in the sensitive nodes, which in turn depend on the input combinations. The overall SER is the average of the different SER input combinations. The alpha particle strike triggers an OFF transistor, from this we can analyze which nodes are sensitive and incorporate current pulses in these nodes. For a two input NAND gate shown in Fig. 4 and Table II shows nodes sensitive for each input combination. The SER of two input NAND gate is evaluated for each input combination by adding the SER of all sensitive nodes.

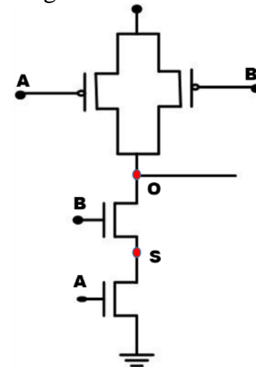

Fig. 4. Two input NAND Gate

TABLE II
SENSITIVITY ANALYSIS OF NANG GATE

Input (AB)	Output (O)	Two input NAND nodes sensitivity to strikes	
		‘O’ Node	‘S’ Node
00	1	No	No
01	1	Yes	No
10	1	No	Yes
11	0	Yes	No

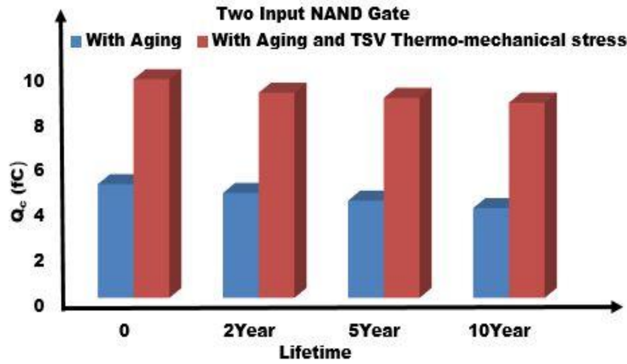

Fig. 5. Critical charge analysis of two input NAND gate

TABLE III
SOFT ERROR RATE ANALYSIS OF NAND GATE

Time Period	Aging effect without TSV Thermo-mechanical stress		Aging effect with TSV Thermo-mechanical stress		Percentage decrease after TSV Thermo-mechanical stress and Aging	
	SER_{3D-1} (%)	SER_{3D-2} (%)	SER_{3D-1} (%)	SER_{3D-2} (%)	SER_{3D-1} (%)	SER_{3D-2} (%)
0Yrs	22.09	2.20	16.97	1.69	5.12	0.51
2Yrs	23.86	2.38	17.78	1.77	6.08	0.60
5Yrs	25.98	2.59	18.12	1.81	7.42	0.74
10Yrs	27.17	2.71	18.56	1.85	9.05	0.90

Fig. 5 presents the critical charge evaluation of two input NAND gate for various lifetimes. It is observed that critical charge decreases with aging. In the case of aging and TSV thermo-mechanical stress, the critical charge is more compared to the aging alone factor, but even in the presence of TSV stress, the critical charge decreases with aging. For the above obtained critical charge we evaluate the SER on layer1 and layer2 with several lifetimes. Table III shows with aging the SER increases irrespective of the layer. As well as 5.12 – 9.05 % and 0.51 – 0.90% decrease in SER observed on layer 1 and 2 respectively, due to the TSV thermo-mechanical stress and aging in comparison to aging alone.

We evaluate the SER of 6T SRAM by including the current pulse at the sensitive node. The current pulses are inserted in the storage node Q and other symmetric node QB. The SRAM cell is evaluated for stored values of 0 and 1 as shown in Fig. 6 and Fig. 7 respectively.

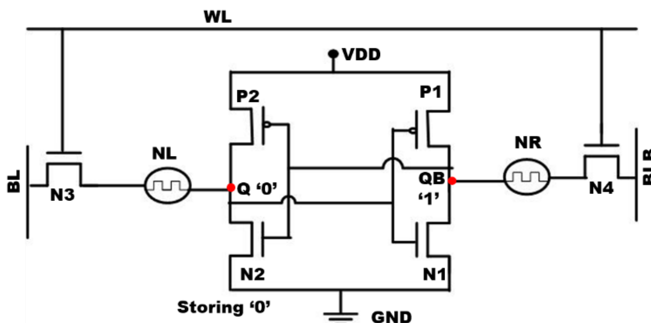

Fig. 6. 6T SRAM storing 0 effected by alpha strike at Q and QB

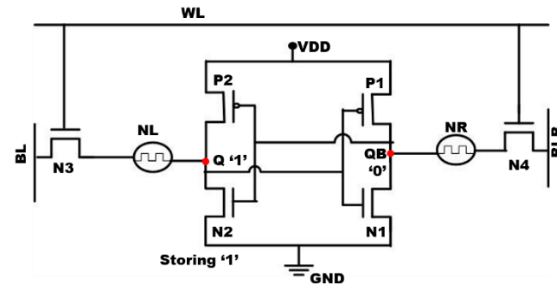

Fig. 7. 6T SRAM storing 1 effected by alpha strike at Q and QB

Fig. 8 shows the critical charge evaluation of 6T SRAM storing 0. It is observed that critical charge decreases with aging. In the case of aging and TSV thermo-mechanical stress, the critical charge is more compared to the aging alone, but even in the presence of TSV stress, the critical charge decreases with aging. For the critical charge we evaluate the SER on layer1 and layer2 with various lifetime. From Table IV it observed that with aging the SER increases irrespective of the layer. As well as 4.75 – 2.51% and 0.47–0.26% decrease in SER observed on layer 1 and 2 respectively, due to the TSV thermo-mechanical stress and aging in comparison to aging alone.

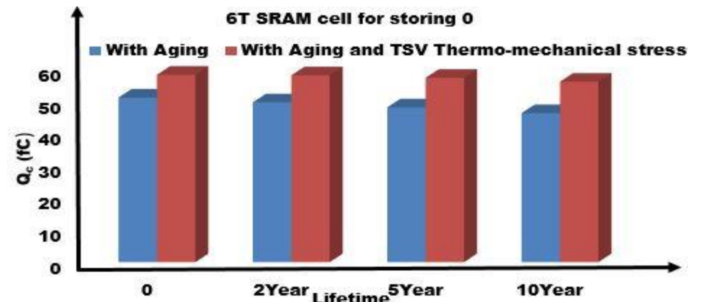

Fig. 8. Critical charge analysis of 6T SRAM storing 0

Fig. 9 shows the critical charge evaluation 6T SRAM storing 1. It is observed that critical charge decreases with aging. In the case of aging and TSV thermo-mechanical stress, the critical charge is more compared to the aging alone, but even in the presence of TSV stress, the critical charge decreases with aging. For the above obtained critical charge we evaluate the SER on layer1 and layer2 with various lifetime. From Table IV it observed that with aging the SER increases irrespective of the layer. As well as 3.77 – 5.64 % and 0.38 – 0.56% decrease in SER observed on layer 1 and 2 respectively, due to the TSV thermo-mechanical stress and aging in comparison to aging alone.

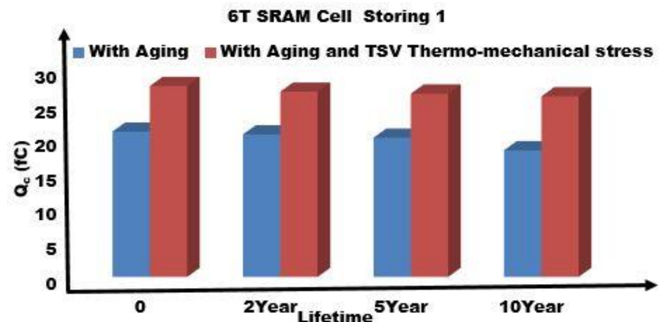

Fig. 9. Critical charge analysis of 6T SRAM storing 1

TABLE IV
SOFT ERROR RATE ANALYSIS OF 6T SRAM

Time Period	Aging effect on 6T SRAM without TSV Thermo-mechanical stress				Aging effect on 6T SRAM with TSV Thermo-mechanical stress				Percentage change after TSV Thermo-mechanical stress and Aging			
	Storing 0		Storing 1		Storing 0		Storing 1		Storing 0		Storing 1	
	SER 3D-1 (%)	SER 3D-2 (%)	SER 3D-1 (%)	SER 3D-2 (%)	SER 3D-1 (%)	SER 3D-2 (%)	SER 3D-1 (%)	SER 3D-2 (%)	SER 3D-1 (%)	SER 3D-2 (%)	SER 3D-1 (%)	SER 3D-2 (%)
0Yrs	26.98	2.69	13.26	1.32	24.47	2.24	9.49	0.94	2.51	0.45	3.77	0.38
2Yrs	28.56	2.85	14.53	1.45	25.91	2.59	10.12	1.01	2.65	0.26	4.41	0.44
5Yrs	29.68	2.96	15.09	1.50	26.18	2.61	10.86	1.08	3.50	0.35	4.23	0.42
10Yrs	32.98	3.29	17.56	1.75	28.23	2.82	11.92	1.19	4.75	0.47	5.64	0.56

IV. CONCLUSION

In this paper, we contributed to the effect of aging and TSV thermo-mechanical stress effect on the resilience of 3D-ICs. It was observed that the soft error rate increased with aging on different layers of 3D-IC. Whereas, the combined effect of aging and TSV thermo-mechanical stress resulted in a decrease of soft error rate in contrast to aging only and the different soft error rate is produced on the various stacked layers of 3D-IC. Hence, the proposed framework and analysis can be used as a baseline for 3D-IC micro-architecture design, as this is the only work that considers aging and TSV thermo-mechanical stress in the analysis of soft error rate.

REFERENCES

[1] Banerjee, K., Souri, S. J., Kapur, P., & Saraswat, K. C. (2001). 3-D ICs: A novel chip design for improving deep-submicrometer interconnect performance and systems-on-chip integration. *Proceedings of the IEEE*,*89*(5), 602-633.

[2] Marella, S. K., & Sapatnekar, S. S., (2015). A holistic analysis of circuit performance variations in 3-D ICs with thermal and TSV-induced stress considerations. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, *23*(7), 1308-1321.

[3] Alam, M. A., Kufluoglu, H., Varghese, D., & Mahapatra, S. (2007). A comprehensive model for PMOS NBTI degradation: Recent progress. *Microelectronics Reliability*, *47*(6), 853-862.

[4] Omana, M., Rossi, D., & Metra, C. (2010). High-performance, robust latches. *IEEE Transactions on Computers*, *59*(11), 1455-1465.

[5] Rossi, D., Omaña, M., Metra, C., & Paccagnella, A. (2015). Impact of bias temperature instability on soft error susceptibility. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, *23*(4), 743-751.

[6] Baumann, R. C., (2005). Radiation-induced soft errors in advanced semiconductor technologies. *IEEE Transactions on Device and materials reliability*, *5*(3), 305-316.

[7] Rossi, D., Omana, M., & Metra, C. (2010, October). Transient fault and soft error on-die monitoring scheme. In *Defect and Fault Tolerance in VLSI Systems (DFT), 2010 IEEE 25th International Symposium on* (pp. 391-398). IEEE.

[8] Zhang, W., & Li, T. (2008, November). Microarchitecture soft error vulnerability characterization and mitigation under 3D integration technology. In *Proceedings of the 41st annual IEEE/ACM International Symposium on Microarchitecture* (pp. 435-446). IEEE Computer Society.

[9] Zhao, Y., Khursheed, S., & Al-Hashimi, B. M. (2015). Online fault tolerance technique for TSV-based 3-D-IC. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, *23*(8), 1567-1571.

[10] Reddy, Raviteja P., Amit Acharyya, and Saqib Khursheed. "A Cost-Effective Fault Tolerance Technique for Functional TSV in 3-D ICs." *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* (2017).

[11] Joshi, K., Mukhopadhyay, S., Goel, N., & Mahapatra, S. (2012, April). A consistent physical framework for N and P BTI in HKMG MOSFETs. In *Reliability Physics Symposium (IRPS), 2012 IEEE International* (pp. 5A-3). IEEE.

[12] Fukui, M., Nakai, S., Miki, H., & Tsukiyama, S. (2011, June). A dependable power grid optimization algorithm considering NBTI timing degradation. In *New Circuits and Systems Conference (NEWCAS), 2011 IEEE 9th International* (pp. 370-373). IEEE.

[13] Yang, H. I., Hwang, W., & Chuang, C. T. (2011). Impacts of NBTI/PBTI and Contact Resistance on Power-Gated SRAM With High-$\kappa $ Metal-Gate Devices. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, *19*(7), 1192-1204.

[14] Sun, Y., Thompson, S. E., & Nishida, T. (2007). Physics of strain effects in semiconductors and metal-oxide-semiconductor field-effect transistors. *Journal of Applied Physics*, *101*(10), 104503.

[15] Van de Walle, C. G. (1989). Band lineups and deformation potentials in the model-solid theory. *Physical review B*, *39*(3), 1871.

[16] Herring, C., & Vogt, E. (1956). Transport and deformation-potential theory for many-valley semiconductors with anisotropic scattering. *Physical Review*, *101*(3), 944.

[17] Uchida, K., Krishnamohan, T., Saraswat, K. C., & Nishi, Y. (2005, December). Physical mechanisms of electron mobility enhancement in uniaxial stressed MOSFETs and impact of uniaxial stress engineering in ballistic regime. In *Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International* (pp. 129-132). IEEE.

[18] Yang, P., Lau, W. S., Lai, S. W., Lo, V. L., Toh, L. F., Wang, J., ... & Chan, L. (2010). Mechanism for improvement of n-channel metal-oxide-semiconductor transistors by tensile stress. *Journal of Applied Physics*, *108*(3), 034506.

[19] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, Digital Integrated Circuits, 2nd ed. Englewood Cliffs, NJ, USA: Prentice-Hall, 2003.

[20] Hazucha, P., & Svensson, C. (2000). Impact of CMOS technology scaling on the atmospheric neutron soft error rate. *IEEE Transactions on Nuclear science*, *47*(6), 2586-2594.

[21] Heijmen, T. (2005, July). Analytical semi-empirical model for SER sensitivity estimation of deep-submicron CMOS circuits. In *On-Line Testing Symposium, 2005. IOLTS 2005. 11th IEEE International* (pp. 3-8). IEEE.

[22] "Predictive Technology Model (PTM)," http://www.ptm.asu.edu.

[23] Riera, Marc, et al. "A detailed methodology to compute soft error rates in advanced technologies." *Proceedings of the 2016 Conference on Design, Automation & Test in Europe*. EDA Consortium, 2016.