Analysis and Assessment of Modular Multilevel Converter Internal Control Schemes

Shuren Wang, *Student Member, IEEE*, Grain P. Adam, *Member, IEEE*, Ahmed M. Massoud, *Senior Member, IEEE*, Derrick Holliday, and Barry W. Williams

***Abstract*—Adoption of distributed submodule (SM) capacitors in a modular multilevel converter (MMC) necessitates complex controllers to ensure the stability of its internal dynamics. This paper presents comprehensive analysis and assessment of different proportional resonant (PR)-based control schemes proposed to stabilize the internal dynamics and ensure ac and dc sides power quality of the MMC within a dc transmission system. With the consideration of passive component tolerances, different energy and voltage based control schemes under various conditions are analyzed. It has been established that without vertical voltage balance control, unequal passive component values in the upper and lower arms of the same phase-leg may cause: unbalanced fundamental currents in the arms, unequal dc voltage across the arms, and fundamental oscillations in the common-mode currents that lead to fundamental frequency ripple in the dc link current. The theoretical analysis that explains this mechanism is presented, and is used to show that vertical voltage balancing is necessary for the nullification of arm voltage difference and suppression of odd oscillations caused by capacitive/inductive asymmetry between arms of the same phase-leg. Simulations support the theoretical analysis and the effectiveness of voltage balancing in ensuring correct operation, independent of tolerances of the MMC passive elements and operating conditions. A new direct method for elimination of fundamental oscillations in the common-mode and dc link current is proposed. Experimental results from a single-phase MMC prototype validate the presented theoretical discussions and simulations.**

***Index Terms*—dc link oscillations, internal control, internal dynamics, modular multilevel converter.**

I. Introduction

WITHIN point-to-point and multi-terminal high-voltage direct current (HVDC) transmission systems, the voltage source converter (VSC) is the preferred technology as it offers dc power reversal with change of current polarity rather than change of voltage polarity (as with line commutated converters), independent control of active and reactive power with the ability to generate leading and lagging reactive power, no minimum dc power flow; and resilience to ac network disturbances and faults. Among many VSC topologies, the MMC is the preferable choice because of its modularity, low switching frequency and high quality ac/dc waveforms [1]–[3].

The MMC requires a number of high and low-level controllers to regulate its output ac and dc voltages, as well as the active and reactive power exchanged with the ac grid. With the high modularity of the MMC circuit topology, however, there are many distributed passive voltage sources or energy tanks facilitating the use of low-voltage rated switching devices, for suppression of electromagnetic interference (EMI) and for providing fault-tolerant operation. The use of distributed floating capacitors in the MMC results in a converter with complex internal dynamics (dynamics between SMs of the same arm, upper and lower arms of the same leg, and different legs), so the converter is difficult to stabilize over the full operating range. Also, MMC capacitor voltages affect the synthesis of common and differential mode arm voltages that create common and differential mode currents respectively. Normally, the common-mode current within the MMC leg consists of dc and even harmonic currents, and its dc component helps transfer power between the dc side and the MMC arms, while the ac component (usually referred to as circulating current) increases capacitor voltage ripple and semiconductor losses [4]–[7]. Many control strategies have been developed to suppress the circulating current and capacitor voltage ripple, and these strategies broadly exploit injection of appropriate harmonics into the common-mode voltage or arm currents [8]–[12]. The comparatively decoupled nature of the inner and outer MMC circuits facilitates the control of the inner variables without influencing the output performance, neither dc side nor ac side. Once the MMC internal dynamics are controlled, its overall performance under normal and abnormal ac grid conditions, particularly its dynamic response due to the decoupling of SM capacitor voltage from the dc link voltage, are improved [13]–[19].

Still, fundamental plus higher-order harmonics which appear as capacitor voltage ripple are unavoidable due to the unique operation of the MMC where both inner and outer circuits contribute to arm currents which flow through the SM capacitors with finite combined inertia, causing voltage ripple which is out of phase in the upper and lower arms of each leg. The main variables that influence the internal dynamics are SM, arm and leg voltages, which represent three coupled control hierarchies within the MMC that could be exploited to enhance

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Shuren Wang, Grain P. Adam, Derrick Holliday and Barry W. Williams are with the University of Strathclyde, Glasgow, G1 1RD, U.K. (e-mail: shuren.wang@strath.ac.uk; grain.adam@strath.ac.uk; derrick.holliday@strath.ac.uk; barry.williams@strath.ac.uk).

Ahmed M. Massoud is with Qatar University, Doha, Qatar. (e-mail: ahmed.massoud@qu.edu.qa).

its performance independent of operating conditions. Voltage control of each SM capacitor is essential for ensuring switching device safety and good performance of higher hierarchies. Different methods for managing voltage differences amongst SMs of the same arm caused by different charging/discharging times and non-ideal parameters are widely discussed in the literature, including SM voltage control algorithms based on either centralized or individual schemes [20]–[25]. Many have focused on control of higher hierarchies such as arm and leg capacitor voltages, and arm and leg energy (power integral), considering both normal and abnormal cases [26]–[49]. The importance of controlling MMC arm voltage was first recognized in [26] where internal voltage regulation was implemented based on an individual SM voltage balancing method with Phase-Shifted Carrier Pulse Width Modulation (PSC-PWM). The individual SM balancing method was improved in [27]–[34] by direct control of the MMC arm voltages, which is realized through manipulation of the active powers of the upper and lower arms of each phase-leg in order to estimate the appropriate fundamental current to be injected into the common-mode current of each leg. Early studies identified the importance of controlling the MMC internal stored capacitive energy for safe and proper operation [35], [36]. Subsequently, a comprehensive study of MMC capacitive energy variation during asymmetric ac faults was presented, considering three control objectives (suppression of negative currents to zero, balanced active power or balanced reactive power) [37]. The study concluded that the control objective which eliminates reactive power oscillations offers clear advantage over maintaining balanced output phase current or oscillation free active power, particularly, in terms of capacitor energy and voltage ripple for reactive power loadings, ranging from unity to zero power factor [37]. In [38]–[44], methods of balancing the arm voltage (or energy) using the concept of equivalent arm capacitance was proposed, and was assessed considering a single-phase to ground fault with a number of control objectives. However, some of the claims in [38] may be misinterpretation of the findings, particularly with regard to the relationship between the ability to suppress circulating currents and injection of negative sequence current into the ac grid. But generally, the methods discussed in [38]–[44] show satisfactory MMC operation during normal and abnormal conditions.

In general, most research neglects passive element tolerances such as for SM capacitance and arm inductance [50]–[52]. A steady-state comparison of voltage and energy MMC balancing approaches that employ three-level flying capacitor SMs, is presented in [53], and its main finding indicates that unequal capacitances affect the quality of the ac side waveforms when an energy-based control approach is employed. The impact of unequal arm inductances on MMC performance is investigated in [54], and this study recommends the use of additional controllers (proportional resonant, PR-based) to prevent the development of a dc component in the ac side waveforms and to suppress fundamental oscillation in the dc link. A general modeling framework and design methodology that considers parameter uncertainty in order to decide the required design margins and predict the operation range has been introduced in [55], but does not reveal any potential implications of SM capacitance or arm inductance tolerances on wider MMC performance. Although the negative effects of SM capacitor voltage difference can be eliminated by voltage balancing algorithms at the SM level, the differences in SM capacitances due to tolerances could not be handled adequately by the inner-arm balancing within each arm. That is, as the ac output controller selects different SMs during operation with a fixed number of inserted and bypassed SMs, capacitance asymmetry may appear as variable capacitance in each phase-leg (upper plus lower arms), rather than fixed capacitance C_{SM}/N.

Considering MMC passive component tolerances, this paper presents comprehensive analytical assessments of different control methods proposed in the literature to control MMC internal dynamics, namely, the voltage and energy based controllers and their variants. This assessment considers two SM-level voltage balancing approaches. The presented mathematical analysis and simulations show that unequal SM capacitance in the upper and lower arms of the same phase-leg (vertical asymmetry) introduces negative sequence currents into the MMC arms and appears as fundamental current in the common-mode currents; thus, causing excessive voltage ripple in the common-mode voltage, with negative sequence fundamental current tending to leak into the dc link current. Ditto for arm inductance tolerance. Detailed investigation reveals that the vertical voltage-based balancing controller helps suppress fundamental oscillation in the common-mode currents and dc link current in the case of vertical asymmetry of SM capacitances and arm inductances. A direct method for eliminating the fundamental circulating current is proposed. The proposed method is effective in ensuring MMC dc link current quality with worst-case passive component asymmetry at the expense of a marginal reduction in the modulation index control range.

The remainder of this paper is organized as follows: Section II presents a brief review of the fundamentals of the modular multilevel converter, including basic definitions which will be used in subsequent sections. Section III describes a number of control architectures that can be used to manipulate the common-mode current in order to regulate MMC internal dynamics. The mechanism that generates dc side oscillation as a result of different capacitance tolerances between the upper and lower arms of the same phase-leg, is presented in Section IV. Section V presents simulation evaluation of the different control schemes being studied and Section VI gives experimental results. Finally, Section VII concludes this paper.

II. System Structure and Parameters

Fig. 1 shows a three-phase half-bridge MMC connected to an ac grid (v_{ac2}) via a Δ-Y interfacing transformer. The output phase voltage measured relative to ground at the ac pole of each phase is v_{io}, and V_{dc} and I_{dc} are the dc link voltage and current respectively. Each MMC arm incorporates an arm inductor L and N series-connected SMs.

With the positive direction arm currents i_{ij} (where, i: a, b, c, are for three phase-legs and j: u, l, indicate the upper and lower arms respectively) and ac output current i_i as indicated in Fig.

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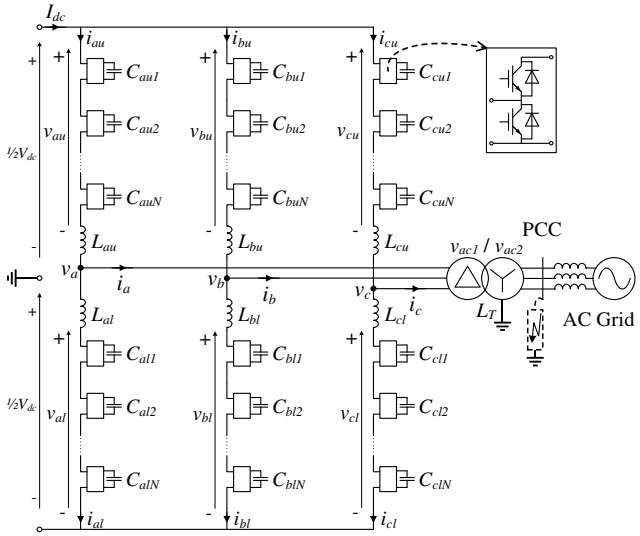

Fig. 1. MMC circuit configuration.

1, the common and differential mode currents i_{icm} and i_{idiff} of an arbitrary phase-leg i are defined as $i_{icm} = ½(i_{iu}+i_{il})$ and $i_{idiff} = i_{io} = i_{iu}-i_{il}$ respectively. This means that the common-mode current refers to the arm current component which is shared between the upper and lower arms of the leg, and consists of a dc component due to dc power transfer and an ac component which is predominantly 2nd order harmonics. For the i^{th} leg, V_{cijk} represents the capacitor voltage of the k^{th} SM in the j^{th} arm and V_{cij} is the sum of the SM capacitor voltages of the j^{th} arm of the i^{th} phase-leg, where $k = 1$-N. The voltage developed across an MMC arm v_{ij} can therefore be approximated by the product of modulation or insertion function m_{ij} (normally $0 \le m_{ij} \le 1$) and its respective SM capacitor voltage sum V_{cij}: $v_{ij}(t) = m_{ij}(t)\times V_{cij}(t)$ [52]. With these assumptions, the differential-mode voltage and current of each phase resemble the output phase voltage v_i and current, that is, $v_{io}(t) = v_{idiff}(t) = v_{iu}(t)$-$v_{il}(t)$. Also, the common and differential modes of the upper and lower arm capacitor voltage sums are defined as:

$$\Sigma V_{ci} = V_{ciu} + V_{cil} \quad (1)$$

$$\Delta V_{ci} = V_{ciu} - V_{cil} \quad (2)$$

Then, the common-mode capacitor voltage sum ($\sum V_{ci}$) is mostly comprised of a dc component and a small ac component that drives the circulating current in each arm, when counter harmonics are not injected into the common-mode voltage of each leg. The differential-mode capacitor voltage sum (ΔV_{ci}) of each leg is mainly comprised of the fundamental ac voltage, provided the upper and lower arm capacitor voltage sums have the same dc components.

Practically, it is essential to account for the passive component tolerances [53], [54], [56] for the following reasons:

1) Each MMC SM must be regulated correctly to ensure that the voltage stresses on each SM capacitor and switching device do not exceed their rated voltage;
2) Although the majority of publications assume identical SM capacitance, the inherent SM capacitance tolerances have noticeable adverse impact in terms of stored energy variation;
3) Provided the SM capacitors and arm inductors play fundamental roles in the synthesis of the ac and dc output voltages and power transfer between ac and dc sides, substantial differences in their magnitudes lead to unbalanced fundamental arm currents, which could affect the common-mode and dc link currents; and
4) The assumption of identical SM capacitance leads to performance deterioration of some control methods in hardware implementation, which appears as voltage imbalance between the arms of the same or different legs, etc.

Accurate theoretical quantification of the impact of SM capacitance tolerance on MMC performance is difficult as it involves a large number of components with highly complex dynamics that operate as part of a variable structure system, with variability of the structure influenced by several controllers. The study of the potential impact of SM capacitance tolerance is divided into three parts:

1) Capacitance tolerance impacts on the pattern and rate of the capacitor voltage variation at the SM level within each arm (this effect is expected to be mitigated by SM level capacitor voltage balancing);
2) Vertical asymmetry (the upper and lower arms of the same phase-legs present different total capacitances) may lead to unequal voltage or energy distribution between the upper and lower arms; and
3) Horizontal asymmetry (the phase-legs reflect different equivalent capacitances) may cause unequal energy distribution and excessive circulating currents between legs.

Generally, there are two SM capacitor voltage balancing approaches, depending on the employed modulation method. The first approach calculates the number of SMs to be inserted into the conduction path and bypassed from each arm using nearest voltage level modulation [57]–[59] or pulse width modulation with various carrier arrangements such as Phase-Shifted Carrier PWM (PSC-PWM) [60], [61] or phase disposition PWM (PD-PWM) [62], [63]. The SM number to be inserted and bypassed, and the sorted order of SM capacitor voltages for each arm, are fed to the SM selection algorithm. The second approach assigns the PSC-PWM and a dedicated modulating signal to each SM, with SM capacitor voltage being controlled individually by additional components injected into the main modulation signal of the arms [64]–[68]. As both balancing algorithms usually operate at high frequency [25], [69], the analysis in this paper assumes that the impact of SM capacitance differences at the SM-level is mitigated by the capacitor voltage balancing method.

III. Assessment of Internal Control Schemes

In this section, different control schemes for ensuring MMC internal stability are analyzed. From the modulation and SM voltage balancing point of view, these methods are divided into two broad categories. Methods that use dedicated SM controllers to regulate individual SM capacitor voltage without employing capacitor voltage sorting, are classified as Method-I

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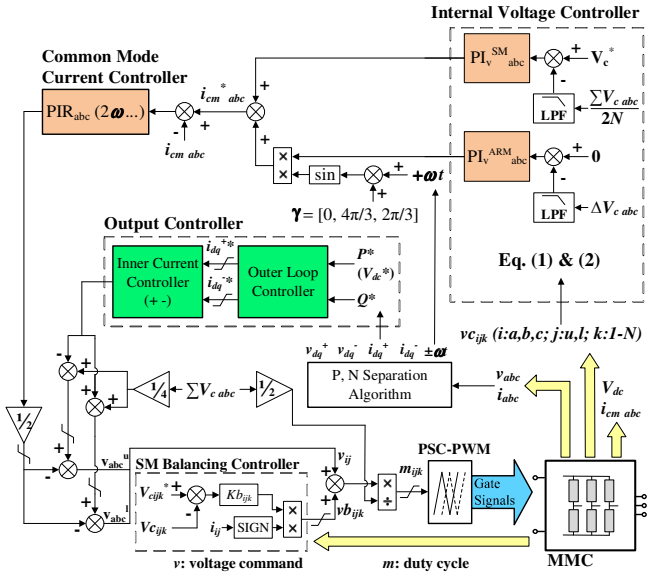

Fig. 2. Schematic diagram of Method-I.

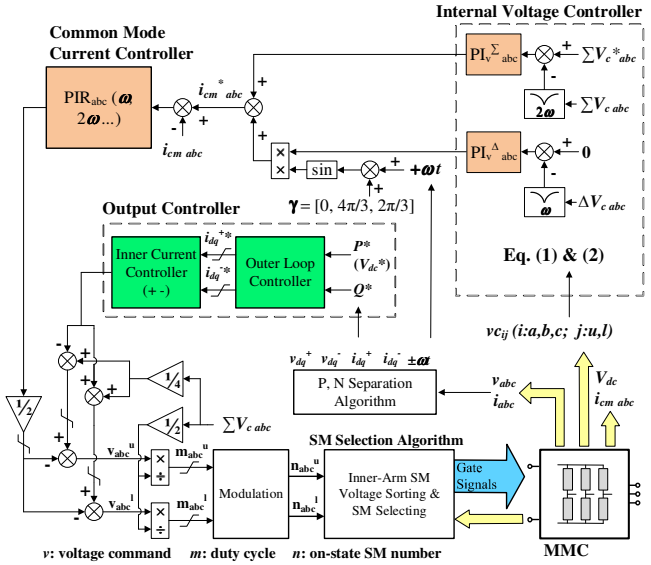

Fig. 3. Schematic diagram of Method-II.

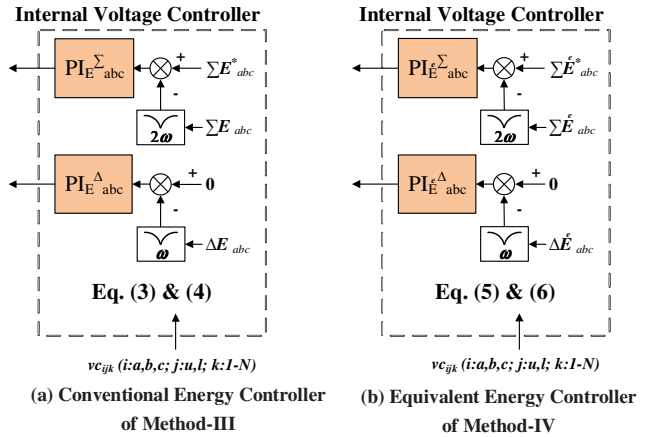

Fig. 4. Arm controller schematic diagrams of Methods III and IV.

(with such methods, capacitor voltage balancing and modulation represent two successive stages or layers). Whereas methods that insert or bypass SMs based on the combined outcomes of modulation and a capacitor voltage sorting algorithm, are classified as Methods II to IV (in these cases, capacitor voltage balancing and the modulation process are inseparable).

Fig. 2 and Fig. 3 depict generic control structures for the Methods I and II respectively, with both employing the same controller for regulating the output ac currents and active and reactive power. Both methods employ a positive and negative separation stage that decomposes the three-phase voltages and currents into positive and negative sequence components to be used by the inner current controller to compute the modulating signals [13]–[19].

Because the common-mode arm voltage or common-mode capacitor voltage sum only influences the common-mode current in each leg, its exploitation to regulate arm or leg voltage or energy will not affect the differential ac output current or voltage of the MMC, provided any modification is applied to both the upper and lower arm voltage commands and the modulation functions remain within the linear range (no saturation). All the methods investigated include a dedicated controller for MMC internal dynamics regulation, and a proportional-resonant controller tuned at 2ω for circulating current suppression in each leg [9], [37], [70]. To minimize the adverse impact of cross-modulation due to undesirable SM capacitor voltage dynamics on the output voltage and current waveforms, a dedicated PI controller is used in each leg to regulate the common-mode capacitor voltage sum independent of the dc link voltage. Thus SM capacitor voltage dynamics and regulation are decoupled from the dc link voltage. From observation of the active power of the upper and lower arms and literature review, injection of a small fundamental current into the common-mode current of each leg improves the vertical balance, specifically, equalizing SM capacitor voltages or energy sum of the upper and lower arms of the same leg [33], [38], [42]–[44].

A. Method-I: Internal Voltage Control Scheme Based on Individual SM Voltage Balancing

This method does not employ a sorting-based SM capacitor voltage balancing algorithm in the inner layer as originally envisioned by Marquardt. Rather it uses a simple proportional controller at each SM level to regulate the capacitor voltage in an isolated manner. The SM capacitor voltage controller estimates the adjustment to be introduced to the main modulation signal of each arm in order to synthesize the modulating signal to be compared with the dedicated PSC of each SM [26], [71]. A depiction of Method-I in Fig. 2 shows that the main modulation signal of the arm or leg is modified by an amount that represents the output of the capacitor voltage controller multiplied by the polarity of the arm current ($Kb_{ijk}\times(V_{cijk}^{*}-V_{cijk})\times\text{sign}(i_{ij})$, where Kb_{ijk} represents the proportional gain of the SM capacitor voltage controller). The main attribute of this method over a sorting-based method is that the average switching frequency of the switches is constant

in all SMs and equal to the assigned carrier frequency, independent of modulation depth. Therefore, this method ensures even thermal distribution and simpler design of the heat management system [72].

Two ways to implement Method-I have emerged, *viz*. [73]–[76] and [20], [27]–[31]. The main difference is the choice of the reference V_{cijk}* used by each SM capacitor voltage controller that ensures capacitor voltage balancing. The first implementation sets the reference voltage for each SM capacitor constant (dc) or equal to the average of the common-mode capacitor voltage sum per leg, excluding the ripple (V_{cijk}* = ½$\sum V_{ci}/N$). The initial premise of this implementation is that, if the common-mode capacitor voltage sum is tightly controlled and the individual SM capacitor voltages in the entire leg are also controlled to balance, the upper and lower arm capacitor voltage sums of the same leg will be the same, which means vertical balancing is eventually achieved. Low pass filters are needed to prevent introducing SM voltage ripple into the control loops. A common implementation uses the SM arithmetical average voltage of each arm as a reference, balancing SM voltage within one arm. This shows good dynamic response and has low parameter sensitivity [20].

For management of internal arm-level dynamics, Method-I in Fig. 2 uses both average SM capacitor voltage control and arm voltage balancing control [30], [77]. The average SM voltage controller ensures the SM average capacitor voltage of each leg is controlled and independent of the dc link voltage. This is achieved through manipulation of the common-mode current of each leg, whilst the arm voltage balancing controller aims to eliminate any error between the dc components of the capacitor voltage sum of the upper and lower arms of the same leg. This is facilitated by manipulation of the active-power difference between the upper and lower arms of the same leg, through injection of a small fundamental current into the common-mode current which is predominantly dc with a remnant of the circulating current [27]–[34], [76], [78]. As shown in Fig. 2, SM voltage and arm balancing controllers PI_v^{SM} and PI_v^{ARM} control the common and differential mode capacitor voltage sums respectively, with the ac components of the measured capacitor voltages low-pass filtered (LPFs in Fig. 2). In previous studies [34], [77], both common and differential mode controllers use only proportional terms, benefiting from the natural ability of the MMC to balance its arm capacitor voltages. Hence the integral terms only accelerate convergence toward the desired settling points with zero steady-state error.

Accordingly, common and differential mode mean capacitor voltage sum control are achieved, therefore, horizontal and vertical balance are ensured with decoupled capacitor voltages. As a well-designed SM balancing scheme can isolate SM-level manipulation and higher-level control, the direct higher level voltage control scheme can naturally be applied to the sorting algorithm, as to be discussed [37].

B. Method-II: Internal Voltage Control Scheme Based on Sorting Algorithm

The conventional MMC control system has a similar structure to that of the two-level converter with minor controller modifications to account for circulating currents. This approach is known for its simplicity and stability, but its main drawback is that the SM capacitor voltages are directly coupled to (or track) the MMC dc link voltage. This means any change in active power set-point necessitates dc link voltage change of the power controlling converter. The SM capacitor voltages and their corresponding energy levels are also changed. As a result, such a controlled MMC tends to suffer from slow dynamic response and is subject to strict and slow power ramp rates. Therefore, Method-II with an additional control stage to manage the MMC internal dynamics and decouple the common-mode SM capacitor voltage sum from the dc link voltage in order to improve dynamic response, was proposed. In this paper, Method-II adopts similar common and differential mode capacitor voltage sum controllers, PI_v^{Σ} and PI_v^{Δ}, respectively, as proposed by Akagi *et al*. [26], [77], implemented with Method-I to regulate MMC internal dynamics.

The MMC leg common and differential mode capacitor voltage sums contain ac components, predominantly 2nd and 1st harmonics respectively [51], [79]; therefore, a number of notch filters tuned at 2ω and ω suppress these ac components in Fig. 3.

C. Method-III: Conventional Energy Control Scheme

MMC internal dynamics regulation using energy-based controllers, as shown in Fig. 4(a), is referred to as Method-III in this paper. The control structure is similar to Method-II, but it regulates the dc components of the common and differential mode energy of the upper and lower arms of each leg to be constant and zero respectively [38], [42], [44]. The common and differential mode capacitor energy sums of each leg are:

$$\Sigma E_i = \frac{1}{2}\left(\sum_{k=1}^{N} C_{iuk} \times V_{ciuk}^{\ 2} + \sum_{k=1}^{N} C_{ilk} \times V_{cilk}^{\ 2}\right) \tag{3}$$

$$\Delta E_i = \frac{1}{2}\left(\sum_{k=1}^{N} C_{iuk} \times V_{ciuk}^{\ 2} - \sum_{k=1}^{N} C_{ilk} \times V_{cilk}^{\ 2}\right) \tag{4}$$

where the capacitance and voltage of each SM are incorporated into the calculation. Studies have shown that the common and differential mode capacitor energy sums of each leg oscillate or contain the same dominant frequencies as in the common and differential mode capacitor voltage sums respectively, i.e. 2ω and ω, where ω represents fundamental angular frequency [42], [44]. Therefore, notch filters tuned at 2ω and ω are adopted respectively to obtain the corresponding dc components. Most (if not all) previous research that has studied the conventional energy-based controller ignores SM capacitance tolerance. Assuming that all SM capacitances are equal results in the dc components of the common and differential mode energy sums being constant and zero respectively, representing sufficient and necessary conditions for balanced arm capacitor voltage sums. Mathematically, forcing the dc component of the total energy of the upper and lower arms to be equal does not ensure that the upper and lower arms have the same dc components of voltage. The adverse implication of such a fallacy remains unobserved in previous studies as the MMC operates away from its maximum modulation index range, whence all SM capacitors of each arm are inserted or bypassed in order to

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synthesize the output ac voltage, as will be shown. With unequal capacitance in the upper and lower arms, uncontrolled and unequal fundamental currents are induced into the leg common-mode currents, which can potentially result in a dc output voltage bias.

D. Method-IV: Equivalent Energy Control Scheme

The energy calculation in Method-IV neglects the SM capacitance tolerances and assumes each arm has an equivalent capacitance [38], [42], and is thus termed "Equivalent Energy Control". The method can be viewed as an alternative implementation of the conventional energy-based controller, but the equal SM capacitance assumption means it can be viewed as another implementation of Method-II using the difference and sum of two arm voltages squared instead of direct control of common and differential mode capacitor voltage sums. Assuming the ideal case of equal SM capacitance, the common and differential mode capacitor voltage sums of the legs are:

$$\Sigma \overset{e}{E}_i = \tfrac{1}{2} C_{arm} \times (V_{ciu}{}^2 + V_{cil}{}^2) \tag{5}$$

$$\Delta \overset{e}{E}_i = \tfrac{1}{2} C_{arm} \times (V_{ciu}{}^2 - V_{cil}{}^2) \tag{6}$$

where C_{arm} represents the equivalent capacitance of the arm and superscript "e" refers to the equivalent energy (or energy calculated based on the equal equivalent capacitance). The reference of common-mode capacitor energy sum for a generic leg is:

$$\Sigma \overset{e}{E}_i{}^* = 2 \times \tfrac{1}{2} C_{arm} (N \times V_c^*)^2 = 2N \times \tfrac{1}{2} C_{SM} (V_c^*)^2 \tag{7}$$

where C_{SM} represents the capacitance of each SM and V_c* refers to the SM voltage reference as in Fig. 2. Similarly, the controllers are shown in Fig. 4(b) and the control objectives of the internal arm controller using Method-IV are to achieve energy balance both among legs and between upper and lower arms within each leg. When these objectives are satisfied, the following equations hold:

$$\tfrac{1}{2} C_{arm} \times (V_{ciu}{}^2 + V_{cil}{}^2) = \tfrac{1}{2} C_{arm} \times 2 (N \times V_c^*)^2 \tag{8}$$

$$\tfrac{1}{2} C_{arm} \times (V_{ciu}{}^2 - V_{cil}{}^2) = 0 \tag{9}$$

Solving (8) and (9), yields

$$V_{ciu}{}^2 = V_{cil}{}^2 = (N \times V_c^*)^2 \Rightarrow V_{ciu} = V_{cil} = N \times V_c^* \tag{10}$$

Practically, in the equivalent energy method, the controllers manipulate the sum and difference of squares of the arm voltage sum, where the term ½C_{arm} can be treated as a coefficient lumped into the PI controller gains.

IV. Comprehensive Analysis of Internal Arm-Level Characteristics

As described, and mentioned in [42], [64], management of the MMC inner dynamics requires horizontal balancing (leg *a*, *b* and *c*) and vertical balancing (upper and lower arms of the same leg, *iu* and *il*). Some publications have adopted the use of a dedicated controller to ensure horizontal balancing by forcing the dc link current to be equally split among the three legs of the three-phase MMC. Such enforced equalization of the common-mode dc current of the three legs can lead to unnecessary curtailment of the dc or active power exchanged between the dc and ac sides during unbalanced and asymmetric ac faults [4], [32], [38]. Although this approach performs well during normal operation, it exhibits unsatisfactory performance during operation with unbalanced ac voltages and asymmetric ac faults (as equalization of dc current per leg could be an unachievable control objective in some situations). Therefore, a relaxed MMC horizontal balancing approach is preferred, in which the common-mode capacitor voltage sum of the three legs is controlled to be the same and constant. Such control of the common-mode capacitor voltage sum ensures satisfactory operation over the full range and with fast dynamic response at both the ac and dc sides. This is because of the reduced coupling between the principal ac and dc variables involved in the power transfer and synthesis of the output voltages and currents.

Concerning vertical balancing, unbalanced voltage between the upper and lower arms of the same leg appears not to cause dc offset or even harmonics in the ac output voltage [2], [80], [81]. But this observation is true only when the MMC operates at relatively low modulation indices (where it does not need to insert or bypass all the SMs in its arms to satisfy output voltage requirements). Failure to nullify the errors between the mean value of upper and lower arm capacitor voltage sums (basically differential capacitor voltage sum) may introduce dc offsets into ac output voltages and currents when MMC operation requires all SMs. However, the potential problems of dc offsets and even harmonics in the output waveforms can be avoided by using redundant SMs in each MMC arm or by regulating the capacitor voltage sum of each arm to be higher than the actual dc link voltage (thus, appearing to have redundant SMs). As stated, when the upper and lower arms of the same phase-leg have different capacitances, uncontrolled fundamental current appears in the common-mode current of each phase-leg, and also in the dc link current. This problem could be typically avoided, however, if the dc components of the differential-mode capacitor voltage sums of the upper and lower arms of all three phase-legs are nullified (or forced to zero).

To substantiate this discussion mathematically, approximate analysis is used to explain the influence of asymmetric arm capacitance, assuming [51], [82]:

1) Modulation signals are continuous and harmonic free;
2) Switching frequency is sufficiently high, so the output and arm currents and voltages can be assumed constant within each switching period;
3) The capacitance tolerances between the SMs of each arm are taken into account, but for simplicity these tolerances are reflected to the mean or equivalent capacitance of each arm;
4) The SM capacitor voltages within one arm are balanced; and
5) Common-mode capacitor voltage sum (SM average) controllers are effective among three legs.

For simplicity, the MMC inherent second and higher even order harmonic circulating currents are suppressed. Thus, taking phase-leg *i* as an example, the upper and lower arm currents are:

$$i_{iu}(t) = \tfrac{1}{2} i_i(t) + i_{icm}(t) = \tfrac{\sqrt{2}}{2} I_i \sin(\omega t + \varphi_i) + I_{icm} \tag{11}$$

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$$i_{il}(t) = -\tfrac{1}{2} i_i(t) + i_{icm}(t) = -\tfrac{\sqrt{2}}{2} I_i \sin(\omega t + \varphi_i) + I_{icm} \quad (12)$$

where I_i and φ_i are the rms and phase angle of fundamental output current respectively, and i_{icm} only consists of dc component I_{icm}.

Independent of the modulation method, the switching functions that describe or define the number of SMs to be inserted from the arms of each leg can be approximated by the followings average and normalized insertion functions:

$$S_{iu}(t) = \tfrac{1}{2} - \tfrac{1}{2} M_i \sin(\omega t + \varphi_s) + M_{icm} \quad (13)$$

$$S_{il}(t) = \tfrac{1}{2} + \tfrac{1}{2} M_i \sin(\omega t + \varphi_s) + M_{icm} \quad (14)$$

where M_i and φ_s are the amplitude and phase angle of the modulation index respectively, M_{icm} is the output of common-mode controller, $0 \le M_i \le 1$ and $0 \le M_{icm} \le 1$.

The upper and lower SM average capacitor currents can be approximated as [51], [79]:

$$\begin{aligned} i_{cu}(t) &= I_{icm}(\tfrac{1}{2} + M_{icm}) - \tfrac{\sqrt{2}}{8} I_i M_i \cos(\varphi_s - \varphi_i) \\ &\quad - \tfrac{1}{2} I_{icm} M_i \sin(\omega t + \varphi_s) + \tfrac{\sqrt{2}}{2} I_i (\tfrac{1}{2} + M_{icm}) \sin(\omega t + \varphi_i) \\ &\quad + \tfrac{\sqrt{2}}{8} I_i M_i \cos(2\omega t + \varphi_s + \varphi_i) \end{aligned} \quad (15)$$

$$\begin{aligned} i_{cl}(t) &= I_{icm}(\tfrac{1}{2} + M_{icm}) - \tfrac{\sqrt{2}}{8} I_i M_i \cos(\varphi_s - \varphi_i) \\ &\quad + \tfrac{1}{2} I_{icm} M_i \sin(\omega t + \varphi_s) - \tfrac{\sqrt{2}}{2} I_i (\tfrac{1}{2} + M_{icm}) \sin(\omega t + \varphi_i) \\ &\quad + \tfrac{\sqrt{2}}{8} I_i M_i \cos(2\omega t + \varphi_s + \varphi_i) \end{aligned} \quad (16)$$

where dc components control the mean SM voltages and fundamental and second-order harmonics constitute SM voltage ripple. By integrating the average capacitor currents in (15) and (16), the upper and lower arm capacitor voltage sums are

$$\begin{aligned} v_{cu}(t) &= v_{cu}{}^0 + \frac{1}{C_u} \int i_{cu}{}^{\omega, 2\omega} dt \\ &= V_{cu} + A_u \cos(\omega t + \varphi_s) - B_u \cos(\omega t + \varphi_i) + D_u \sin(2\omega t + \varphi_s + \varphi_i) \end{aligned} \quad (17)$$

$$\begin{aligned} v_{cl}(t) &= v_{cl}{}^0 + \frac{1}{C_l} \int i_{cl}{}^{\omega, 2\omega} dt \\ &= V_{cl} - A_l \cos(\omega t + \varphi_s) + B_l \cos(\omega t + \varphi_i) + D_l \sin(2\omega t + \varphi_s + \varphi_i) \end{aligned} \quad (18)$$

where $A_u = \frac{I_{icm} M_i}{2\omega C_u}$, $B_u = \frac{\sqrt{2} I_i}{2\omega C_u}(\frac{1}{2} + M_{icm})$, $D_u = \frac{\sqrt{2} I_i M_i}{16\omega C_u}$, $A_l = \frac{I_{icm} M_i}{2\omega C_l}$, $B_l = \frac{\sqrt{2} I_i}{2\omega C_l}(\frac{1}{2} + M_{icm})$, $D_l = \frac{\sqrt{2} I_i M_i}{16\omega C_l}$, and C_u and C_l represent the equivalent capacitances of the upper and lower arms respectively. DC components of capacitor voltages $v_{cu}{}^0$ and $v_{cl}{}^0$ represent the settling points for the upper and lower arm capacitor voltage sums [50], [51]. Switching action then reflects SM voltage back to the ac terminals and the common-mode voltage of each phase-leg is described by:

$$v_{icm}(t) = v_{iu}(t) + v_{il}(t) = N S_{iu}(t) v_{cu}(t) + N S_{il}(t) v_{cl}(t) \quad (19)$$

where S_{iu} and S_{il} remain unchanged as (13) and (14) because no new component is added into the switching functions. Similarly, as the dc component of the mean common-mode capacitor voltage sum is controlled to $2N \times V_c{}^*$, only ac components are considered.

Based on (13), (14), (17), (18) and (19), the ac components (frequency at ω, 2ω and 3ω) of the leg common-mode voltages are:

$$\begin{aligned} v_{icm}(t)^{(\omega)} &= v_{iu}(t)^{(\omega)} + v_{il}(t)^{(\omega)} = N(\tfrac{1}{2} + M_{icm})(A_u - A_l)\cos(\omega t + \varphi_s) \\ &\quad - N\left[(\tfrac{1}{2} + M_{icm})(B_u - B_l) + \tfrac{1}{4} M_i (D_u - D_l)\right]\cos(\omega t + \varphi_i) \\ &\quad - \tfrac{1}{2} M_i (V_{cu} - V_{cl}) \sin(\omega t + \varphi_s) \end{aligned} \quad (20)$$

$$\begin{aligned} v_{icm}(t)^{(2\omega)} &= v_{iu}(t)^{(2\omega)} + v_{il}(t)^{(2\omega)} = -N \tfrac{1}{4} M_i (A_u + A_l) \sin(2\omega t + 2\varphi_s) \\ &\quad + N\left[\tfrac{1}{4} M_i (B_u + B_l) + (\tfrac{1}{2} + M_{icm})(D_u + D_l)\right] \sin(2\omega t + \varphi_s + \varphi_i) \end{aligned} \quad (21)$$

$$v_{icm}(t)^{(3\omega)} = v_{iu}(t)^{(3\omega)} + v_{il}(t)^{(3\omega)} = \tfrac{1}{4} N M_i (D_u - D_l) \cos(3\omega t + 2\varphi_s + \varphi_i) \quad (22)$$

where the voltage ripple at ω, 2ω, and 3ω generates corresponding common-mode ac currents. Equation (20) indicates that unequal capacitances of the upper and lower arms of the same leg can lead to the appearance of fundamental voltage in the common-mode capacitor voltage sum which would drive fundamental current in the common-mode loop of each phase-leg. Equation (21) represents the component of the common-mode voltage that would drive 2nd order harmonic current in each phase-leg, which will be eliminated. Any resistance in the common-mode circuit loop is neglected for simplicity, thus only total inductance of the common-mode loop is considered [51]. The amplitude of the 3ω components is small compared to that at ω, so the common-mode current (due to the fundamental voltage ripple) is:

$$\begin{aligned} i_{icm}(t)^{(\omega)} &= \frac{1}{L_u + L_l} \int v_{icm}(t)^{(\omega)} dt \\ &= K_1 \sin(\omega t + \varphi_s) - K_2 \sin(\omega t + \varphi_i) + K_3 \cos(\omega t + \varphi_s) \\ &= \sqrt{K_1{}^2 + K_2{}^2 + K_3{}^2 - 2K_2 \sqrt{K_1{}^2 + K_3{}^2} \cos(2\varphi_s - \varphi_k)} \\ &\quad \times \sin\left[\omega t + \arctan\left(\frac{\sqrt{K_1{}^2 + K_3{}^2}\sin(\varphi_s + \varphi_k) - K_2 \sin\varphi_s}{\sqrt{K_1{}^2 + K_3{}^2}\cos(\varphi_s + \varphi_k) - K_2 \cos\varphi_s}\right)\right] \end{aligned} \quad (23)$$

where L_u and L_l are the upper and lower arm inductances respectively, $\varphi_k = \arctan(\frac{K_3}{K_1})$, $K_1 = N\frac{(\frac{1}{2} + M_{icm})(A_u - A_l)}{\omega(L_u + L_l)}$, $K_2 = N\frac{(\frac{1}{2} + M_{icm})(B_u - B_l) + \frac{1}{4} M_i (D_u - D_l)}{\omega(L_u + L_l)}$, and $K_3 = \frac{M_i (V_{cu} - V_{cl})}{2\omega(L_u + L_l)}$.

The amplitude range of the fundamental common-mode current is

$$\begin{aligned} &\sqrt{K_1{}^2 + K_2{}^2 + K_3{}^2 - 2K_2\sqrt{K_1{}^2 + K_3{}^2}} \\ &\le \sqrt{K_1{}^2 + K_2{}^2 + K_3{}^2 - 2K_2\sqrt{K_1{}^2 + K_3{}^2}\cos(2\varphi_s - \varphi_k)} \le \\ &\sqrt{K_1{}^2 + K_2{}^2 + K_3{}^2 + 2K_2\sqrt{K_1{}^2 + K_3{}^2}} \end{aligned} \quad (24)$$

Considering the range of M_i and M_{icm}, and the definitions of K_1, K_2 and K_3, it can be concluded that when $C_u \ne C_l$ the fundamental frequency current in (23) must exist in the common-mode current.

Accordingly, for one MMC leg, capacitance asymmetry leads to odd harmonics in the common-mode current (mainly a fundamental frequency component), and its amplitude, depending on various variables, increases proportionally with capacitance difference. Generally, asymmetric capacitance in one leg results in two major effects:

1) As asymmetry is random among the legs, the amplitude and phase angle of the fundamental common-mode currents of the three legs will be unbalanced, causing unbalanced fundamental current to feed into the dc link current; and

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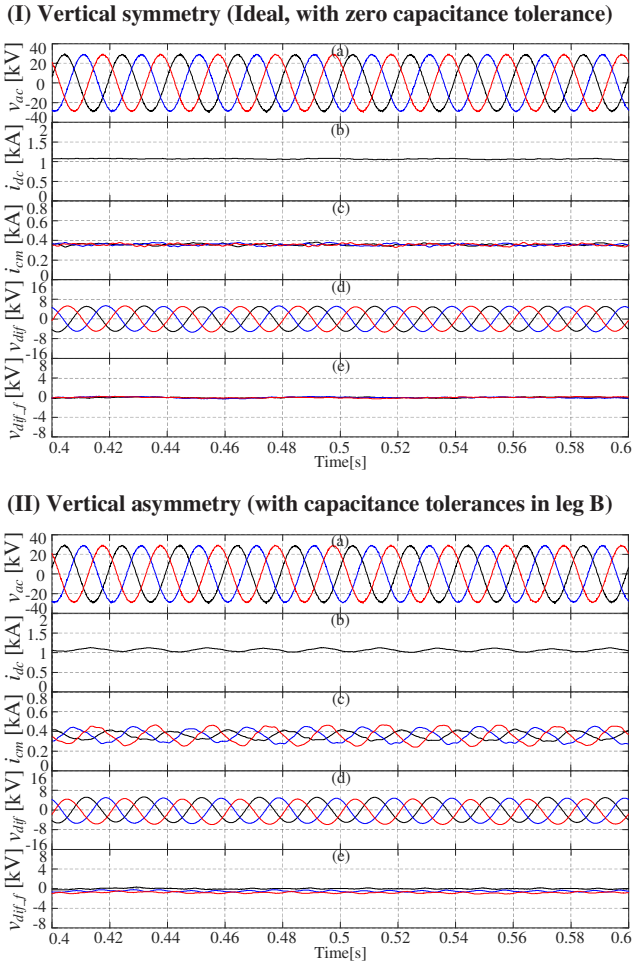

Fig. 5. Waveforms of 40kV-MMC in vertically symmetric and asymmetric cases: (a) ac output voltage v_{ac}, (b) dc link current i_{dc}, (c) common-mode current i_{cm}, (d) differential-mode capacitor voltage sum v_{diff}, (e) 50Hz-notch filtered differential-mode capacitor voltage sum v_{diff_f}.

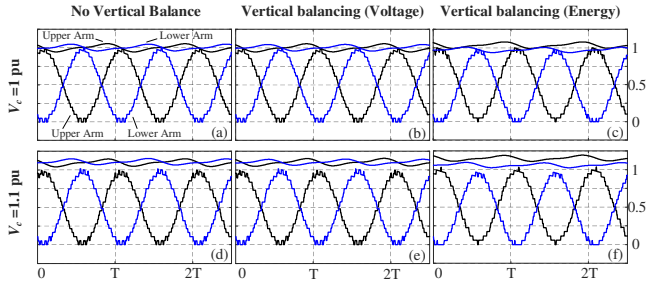

Fig. 6. Normalized arm terminal voltages and common-mode capacitor voltages of methods in asymmetric case.

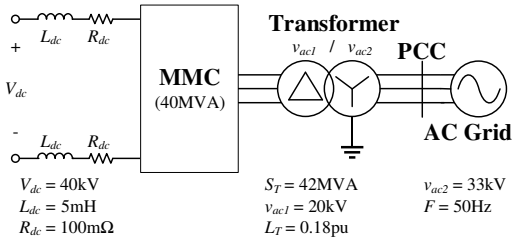

Fig. 7. Illustrative 40MW MMC for HVDC transmission system.

2) Such additional fundamental arm currents interact with switching functions, resulting in dc and 2ω voltage deviation of the upper and lower arms.

The following mathematical derivation establishes the generation of such dc and 2ω deviation. For simplicity, additional fundamental current is added into the ideal arm currents in (11) and (12):

$$\begin{aligned} i_{iu}'(t) &= \tfrac{1}{2} i_i(t) + i_{icm}(t) \\ &= \tfrac{\sqrt{2}}{2} I_i \sin(\omega t + \varphi_i) + I_{icm} + \sqrt{2} I_{icm\omega} \sin(\omega t + \varphi_{icm\omega}) \end{aligned} \tag{25}$$

$$\begin{aligned} i_{il}'(t) &= -\tfrac{1}{2} i_i(t) + i_{icm}(t) \\ &= -\tfrac{\sqrt{2}}{2} I_i \sin(\omega t + \varphi_i) + I_{icm} + \sqrt{2} I_{icm\omega} \sin(\omega t + \varphi_{icm\omega}) \end{aligned} \tag{26}$$

where $I_{icm\omega}$ and $\varphi_{icm\omega}$ are the rms and phase angle of the fundamental common-mode current respectively. If no active controller is designed for the fundamental oscillation, the switching functions remain as (13) and (14). The SM mean capacitor currents are:

$$\begin{aligned} i_{cu}'(t) = {} & I_{icm}(\tfrac{1}{2} + M_{icm}) - \tfrac{\sqrt{2}}{8} I_i M_i \cos(\varphi_s - \varphi_i) - \tfrac{\sqrt{2}}{4} I_{icm\omega} M_i \cos(\varphi_s - \varphi_{icm\omega}) \\ & - \tfrac{1}{2} I_{icm} M_i \sin(\omega t + \varphi_s) + \tfrac{\sqrt{2}}{2} I_i (\tfrac{1}{2} + M_{icm}) \sin(\omega t + \varphi_i) \\ & + \sqrt{2} I_{icm\omega} (\tfrac{1}{2} + M_{icm}) \sin(\omega t + \varphi_{icm\omega}) \\ & + \tfrac{\sqrt{2}}{8} I_i M_i \cos(2\omega t + \varphi_s + \varphi_i) + \tfrac{\sqrt{2}}{4} I_{icm\omega} M_i \cos(2\omega t + \varphi_s + \varphi_{icm\omega}) \end{aligned} \tag{27}$$

$$\begin{aligned} i_{cl}'(t) = {} & I_{icm}(\tfrac{1}{2} + M_{icm}) - \tfrac{\sqrt{2}}{8} I_i M_i \cos(\varphi_s - \varphi_i) + \tfrac{\sqrt{2}}{4} I_{icm\omega} M_i \cos(\varphi_s - \varphi_{icm\omega}) \\ & + \tfrac{1}{2} I_{icm} M_i \sin(\omega t + \varphi_s) - \tfrac{\sqrt{2}}{2} I_i (\tfrac{1}{2} + M_{icm}) \sin(\omega t + \varphi_i) \\ & + \sqrt{2} I_{icm\omega} (\tfrac{1}{2} + M_{icm}) \sin(\omega t + \varphi_{icm\omega}) \\ & + \tfrac{\sqrt{2}}{8} I_i M_i \cos(2\omega t + \varphi_s + \varphi_i) - \tfrac{\sqrt{2}}{4} I_{icm\omega} M_i \cos(2\omega t + \varphi_s + \varphi_{icm\omega}) \end{aligned} \tag{28}$$

where the dc and 2ω ac components in (27) each contain a term related to the amplitude of fundamental frequency common-mode current $\sqrt{2}\, I_{icm\omega}$ which has the opposite sign to the corresponding term in (28). Charging and discharging SMs with the currents in (27) and (28) causes dc, ω and 2ω differences between the upper and lower arms. Also, both dc and 2ω frequency voltage differences are introduced by the non-zero fundamental frequency common-mode current. Furthermore, the voltage differences contribute to the common-mode loop current ripple through the coefficient K_3 in (24), leading to MMC inner-leg interactions. Also, this analysis initially assumed the output of the common-mode capacitor voltage sum controller to be a pure dc component to maintain the constant SM average dc voltage. However, the fundamental fluctuations will induce small corresponding components into the PI controllers, depending on bandwidth and phase-shift characteristics. Therefore, both dc and ω frequency voltage deviation continues until reaching equilibrium in terms of phase angle and magnitude change. Moreover, the mathematically analysis assumed an ideal MMC dc power supply. However, long distance cables introduce parasitic parameters and as a result, the fundamental oscillation in one leg influences other legs through the weak dc terminal voltage, actuating fundamental oscillations and arm voltage differences as well. This phenomenon could be considered as power circulating among three legs to compensate for the stored energy of

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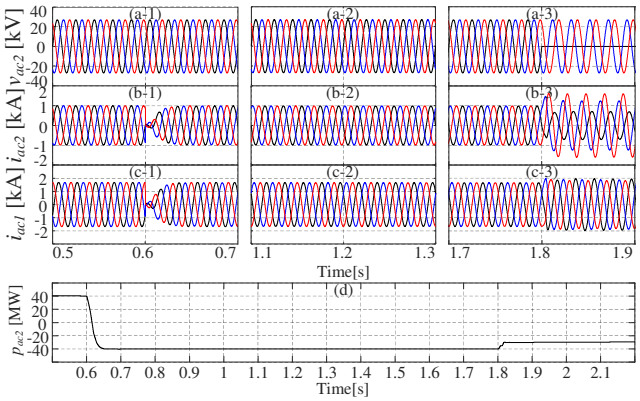

Fig. 8. AC output performance: (a) grid phase voltage v_{ac2}, (b) grid current i_{ac2}, (c) MMC side current i_{ac1}, (d) mean active power p_{ac2}.

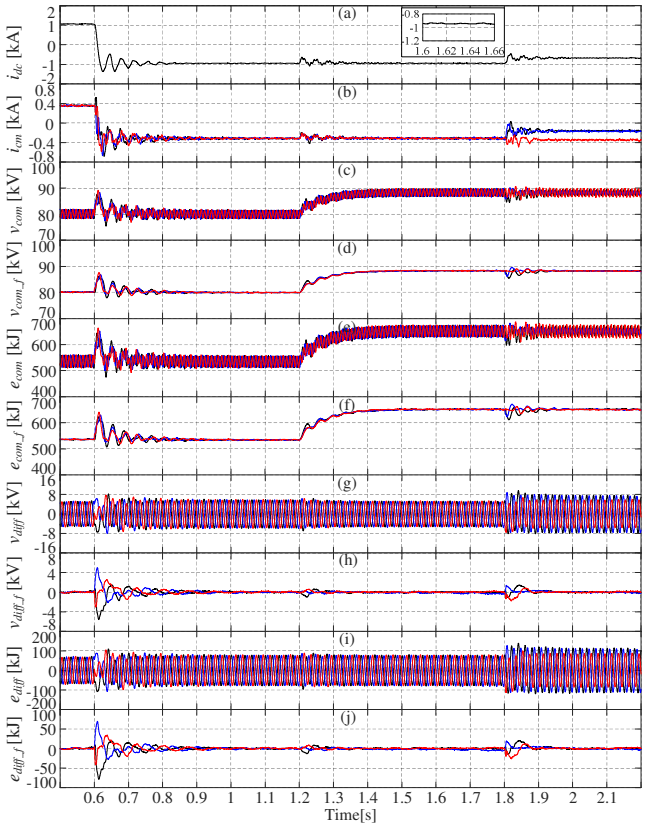

Fig. 9. Waveforms of only average voltage controller in symmetric case: (a) dc link current i_{dc}, (b) common-mode current i_{cm}, (c) common-mode capacitor voltage sum v_{com}, (d) filtered common-mode capacitor voltage sum v_{com_f}, (e) common-mode capacitor energy sum e_{com}, (f) filtered common-mode capacitor energy sum e_{com_f}, (g) differential-mode capacitor voltage sum v_{diff}, (h) filtered differential-mode capacitor voltage sum v_{diff_f}, (i) differential-mode capacitor energy sum e_{diff}, (j) filtered differential-mode capacitor energy sum e_{diff_f}.

different arms, which is an inter-leg interaction. Based on the previous discussions on such a complicated system, an accurate calculation of the amplitude of the fundamental frequency dc link current ripple caused by passive component tolerances is extremely tedious, with much uncertainty that cannot be accounted for readily, such as collective action of various internal controllers. Therefore, the presented analysis is an attempt to explain the mechanism of the inducement of fundamental current ripple and its potential causes, rather than a precise quantification of its magnitude. Fortunately, there are various internal control schemes that are able to (or intend to) suppress such ripple, facilitating MMC internal and external decoupling.

For unbalanced grid analysis, most approaches in the literature focus on eliminating the 2ω power component, which causes the dc voltage and/or dc current oscillation [14]. However, unlike the 2ω components only occurring during output unbalanced conditions, oscillation at ω always exists due to MMC charging and discharging with unequal arm capacitances in the same leg. Similarly, the tolerances of arm inductance within one leg can cause the same current oscillation as the energy stored in the arm inductors and the ac voltage drops they present are no longer balanced. Therefore, additional controllers are needed to regulate the inherent fundamental current difference between arms and energy differences caused by passive component tolerances. This discussion shows that a vertical balancing controller that minimizes the differential-mode capacitor voltage sum is effective for correct MMC operation when passive components tolerances are significant. Also, in the asymmetry case, the incorporation of a dedicated controller to directly eliminate the fundamental current from the common-mode current of each leg, may aid suppression of fundamental frequency oscillation of the dc link current, but cannot eliminate the differential-mode capacitor voltage sum.

V. Simulation Evaluation

The MATLAB/SIMULINK MMC model described in section II is used to clarify some of the issues due to the potential mismatch of MMC capacitance and arm inductance.

TABLE I
Simulation Parameters of The 40MVA MMC

Rated power	40MVA
DC voltage	40kV
AC grid line voltage	33kV
AC grid frequency	50Hz
Transformer leakage inductance	0.18pu
Transformer ratio	20/33kV
Arm inductance	6.1mH(0.2pu)
Numbers of SMs per arm	20
SM capacitance	6.7mF(40kJ/MVA)
Modulation carrier frequency	1.0kHz

The differences between individual SM capacitance of arms are simulated by making the values of arm equivalent capacitances different, and it is assumed that the asymmetry only exists in leg B for ease of illustration. For horizontal capacitance asymmetry, it is assumed that the equivalent capacitance of leg B SMs is $0.9C_{SM}$. Whilst for vertical capacitance asymmetry, the equivalent capacitances of the SMs of the upper and lower arms of leg B are $0.9C_{SM}$ and $1.1C_{SM}$ respectively. It is assumed that the SMs of legs A and C have nominal capacitance C_{SM}. Similar considerations are applied for the arm inductance asymmetry study.

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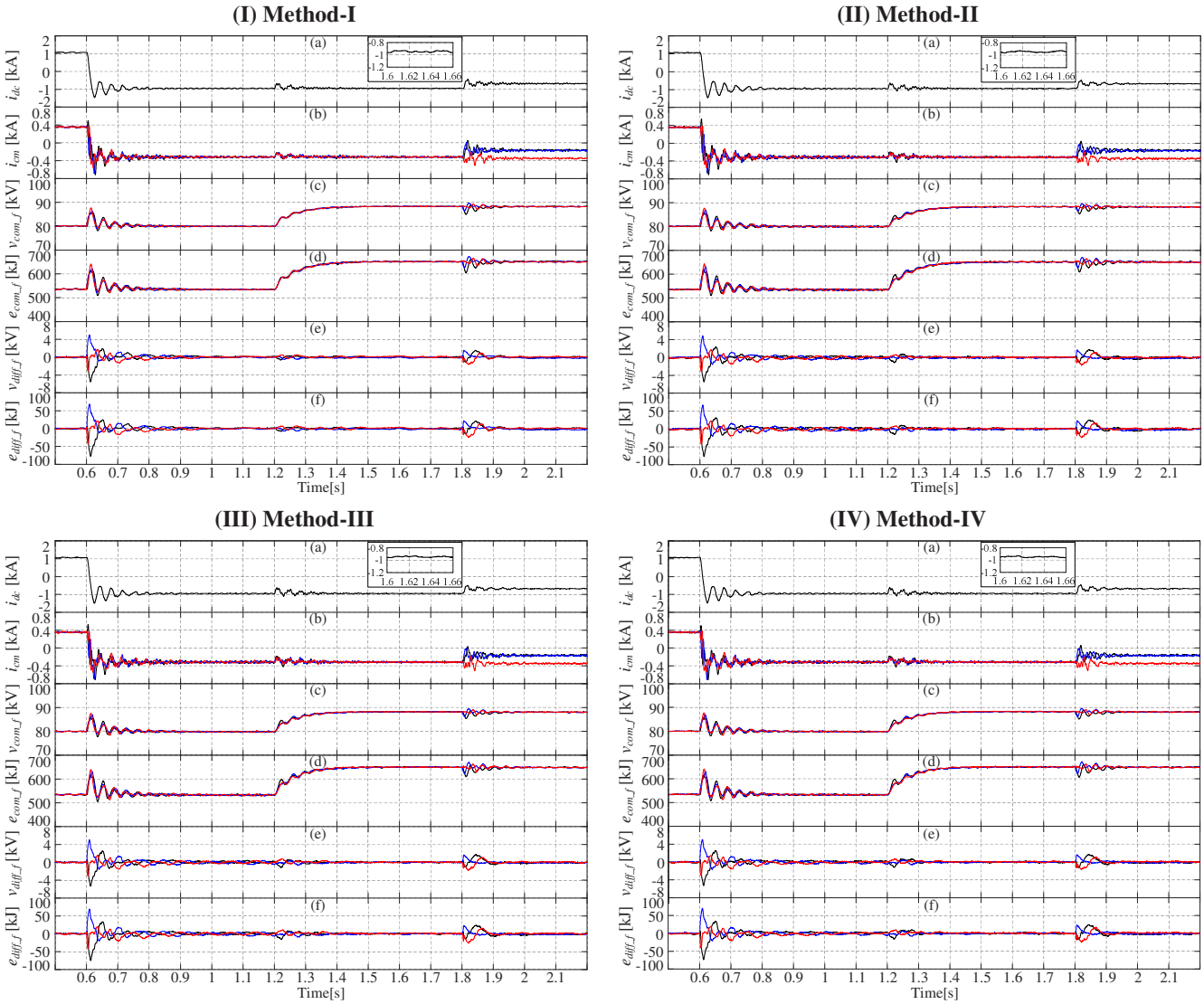

Fig. 10. Waveforms of Methods I to IV in the symmetrical case: (a) dc link current i_{dc}, (b) common-mode current i_{cm}, (c) filtered common-mode capacitor voltage sum v_{com_f}, (d) filtered common-mode capacitor energy sum e_{com_f}, (e) filtered differential-mode capacitor voltage sum v_{diff_f}, (f) filtered differential-mode capacitor energy sum e_{diff_f}.

A. Vertical Balance Study of MMC in an Open-Loop Condition

This subsection illustrates basic MMC behavior with and without SM capacitance tolerances in leg B, assuming inverter mode operation, with parameters in Table I but feeding a passive load. Fig. 5 show simulation waveforms of the output ac voltages, dc link current, common-mode currents, and differential-mode capacitor voltage sums, where 0 and ±10% tolerances are applied to SM capacitances of the arms in leg B, and without active vertical balance control. The plots in Fig. 5-I show that the mean differential-mode capacitor voltage sums of the three legs are near zero with zero SM capacitance tolerance. The dc link current and common-mode currents do not exhibit any low frequency oscillation. However, when ±10% SM capacitance tolerance is incorporated, Fig. 5-II shows the common-mode currents contain noticeable unbalanced ac components, with significant 50Hz components in both the common-mode and dc link currents [see Fig. 5-II(b) and (c)]. Also, the pre-filtered and post-filtered differential-mode capacitor voltage sums become unbalanced and deviate from zero, respectively [see Fig. 5-II(d) and (e)].

To further substantiate the discussion in section III, particularly, the effectiveness of different implementations of the vertical balancing controllers previously described, are assessed when SM capacitance tolerance is considered. Three sets of simulation cases are presented, namely, without vertical balancing, and with voltage and energy based vertical balancing methods, where the dc link voltage remains 40kV, modulation index is fixed at 95%, and two set points common-mode capacitor voltage sums, namely, 80kV (V_c=1pu) and 88kV (V_c=1.1pu).

Fig. 6 summarizes the normalized arm voltages of leg B and their corresponding upper and lower arm capacitor voltage sums, with vertical SM capacitance asymmetry of ±10%. Fig.

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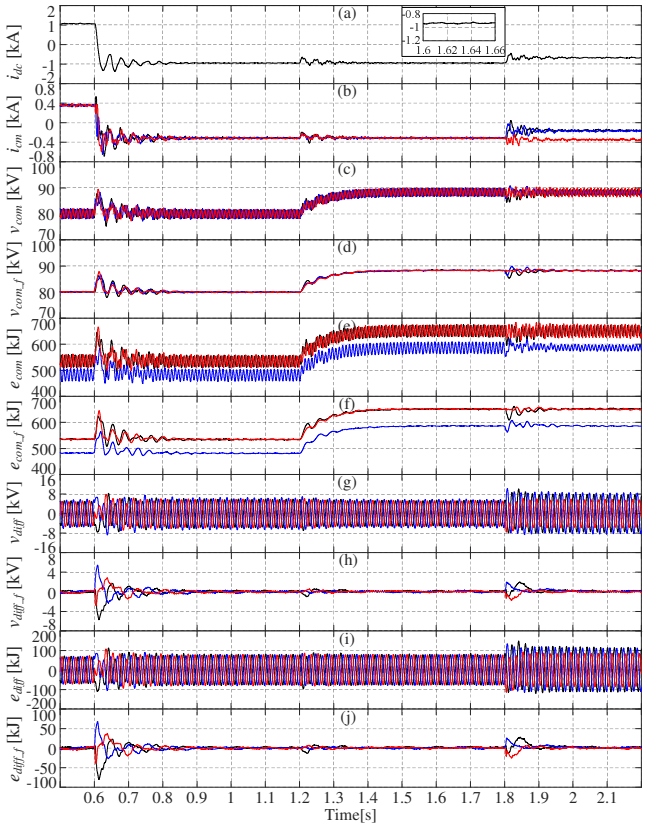

Fig. 11. Waveforms of average voltage controller in horizontal asymmetry case: (a) dc link current i_{dc}, (b) common-mode current i_{cm}, (c) common-mode capacitor voltage sum v_{com}, (d) filtered common-mode capacitor voltage sum v_{com_f}, (e) common-mode capacitor energy sum e_{com}, (f) filtered common-mode capacitor energy sum e_{com_f}, (g) differential-mode capacitor voltage sum v_{diff}, (h) filtered differential-mode capacitor voltage sum v_{diff_f}, (i) differential-mode capacitor energy sum e_{diff}, (j) filtered differential-mode capacitor energy sum e_{diff_f}.

6(a) and (d), and (b) and (e) show that without vertical balancing and with voltage-based vertical balancing the drift of the differential-mode capacitor voltage sums from zero remain small for both set points of the common-mode capacitor voltage sums of 1pu and 1.1pu; thus both arms are able to synthesize the correct arm voltages. In contrast, Fig. 6(c) and (f) show that with the energy-based vertical balancing the drift of the differential-mode capacitor voltage sums from zero becomes large as the set point of the common-mode capacitor voltage sums increases from 1pu to 1.1pu; thus making the arm with lower voltage unable to synthesize the correct arm voltages. This problem would be exacerbated if the MMC operates at higher modulation indices that approach unity for SPWM and 1.155 with SPWM plus 3rd harmonics. Fig. 6(f) shows even though the modulation index or upper and lower voltages do not hit the limits, the dc components of capacitor voltage sums of the upper and lower arms become unequal, and this may cause dc-offset in the output ac voltages if not mitigated.

B. Waveform Study of Internal Control Schemes

This section assesses the performance of different internal control methods described above when the MMC is connected to an ac grid as shown in Fig. 7, with its simulation parameters in Table I, and with and without considering SM capacitance tolerances.

Initially, the MMC is controlled to inject 40MW into an ac grid and regulates its average SM capacitor voltage at 2kV (common-mode capacitor voltage sum is 80kV). At 0.6 s, a step change is applied to the active power output references to reverse the power flow from 40MW to -40MW. At 1.2s, a step change is applied to the common-mode capacitor voltage sums to increase the average common-mode capacitor voltage sums (SM average capacitor voltage) by 0.1pu. At 1.8s, a single-line-to-ground (SLG) fault is applied at the point of common coupling of phase A. The reactive power output is controlled to be zero. During the SLG fault, the positive-sequence over-current limit is set to 1.1pu and the negative-sequence current is suppressed to zero.

Since the steady-state and dynamics of the output quantities with different inner control schemes are the same, only three-phase phase voltages and currents at the PCC, MMC ac current at the low-voltage side of the interfacing transformer, and average active power are given in Fig. 8. Fig. 8(a-1), (b-1) and (c-1), and (a-2), (b-2) and (c-2), and (a-3), (b-3) and (c-3) show the voltages and currents at the PCC and currents at the converter side, zoomed around t=0.6s (instant of active power reversal), t=1.2s (application of step change to reference of common-mode capacitor voltage sums) and t=1.8s (initiation of single-phase ac fault) respectively. These simulation waveforms show the MMC exhibits quick dynamic response during power reversal, presents high quality ac side waveforms to the ac grid, and the magnitude increases of the common-mode capacitor voltage sums do not lead to any noticeable changes in ac current waveforms (which indicates good decoupling of the external dynamics). Also, during the solid single-phase ac fault, the converter ac side currents remain balanced as expected (because of negative sequence current suppression). Fig. 8(d) shows active power the MMC injects into PCC over the entire simulation period. The plots shown in Fig. 8 confirm the simulated MMC operates correctly, and are similar for all methods being compared in this paper.

1) Performance of Control Schemes in the Symmetrical Case

Fig. 9 shows waveforms when only the common-mode capacitor voltage sum (SM average voltage) controller is used with symmetric capacitance. The power reversal at 0.6s triggers a brief damped oscillation period in the arm currents, voltages and energies. When the step change is applied to the reference common-mode capacitor voltage sum (to vary its mean from 80kV to 88kV) at 1.2s, the differential-mode capacitor voltage and energy sums exhibit clear fluctuations. Fig. 9(c) and (d) show that the common-mode capacitor voltage sums follow the reference commands, hence horizontal capacitor voltage balance is maintained. As expected, the common-mode capacitor energy sum increases with the common-mode capacitor voltage sum [see Fig. 9(e) and (f)]. In the pre-fault condition, the dc link current is equally distributed between the three legs, which results in balanced common-mode currents, but during the SLG fault, the dc component of the common-mode currents are not equal as expected [see Fig. 9(b)].

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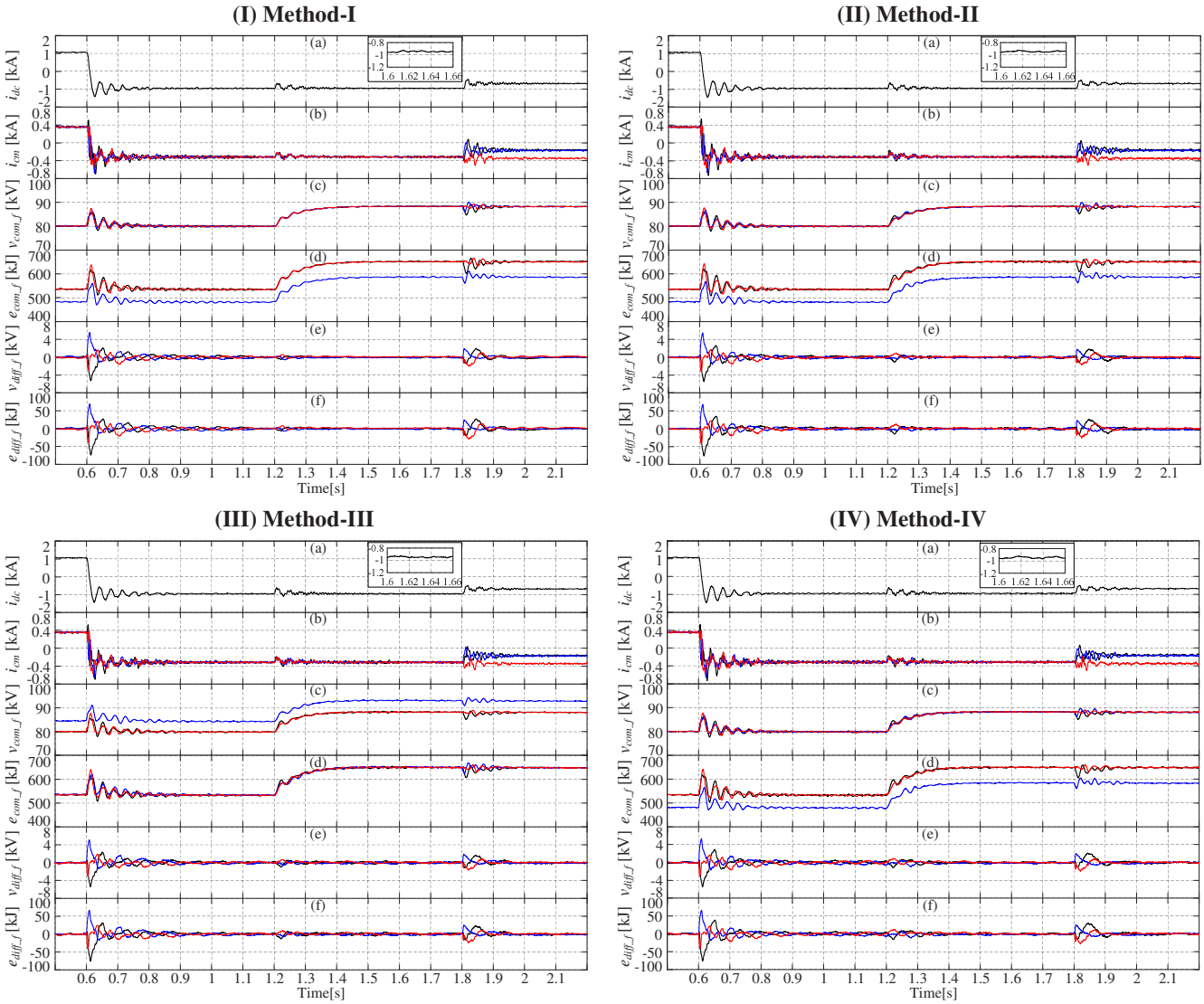

Fig. 12. Waveforms of Method-I to IV in horizontal asymmetry case: (a) dc link current i_{dc}, (b) common-mode current i_{cm}, (c) filtered common-mode capacitor voltage sum v_{com_f}, (d) filtered common-mode capacitor energy sum e_{com_f}, (e) filtered differential-mode capacitor voltage sum v_{diff_f}, (f) filtered differential-mode capacitor energy sum e_{diff_f}.

The performance of Methods I to IV with zero capacitance tolerance is examined (only the filtered waveforms of the capacitor voltage and energy sums are presented) and system operating conditions remain the same as previously outlined. Parts (a) and (b) in Fig. 10-I to IV show that all the control methods maintain the same quality dc link current and common-mode currents in the symmetrical case. Horizontal leg energy and voltage balance are achieved, with dc link current equally distributed among the three legs. During the SLG fault, the common-mode mean currents become unequal, with the average SM voltage unchanged, thus, the three common-mode capacitor energy sums (leg power integral) are unchanged [see (c)-(f) in Fig. 10-I to IV]. For vertical balance of the symmetric legs, the mean voltage (energy) difference of the arms remains zero [see (e) and (f) in Fig. 10-I to IV]. It is concluded that the analyzed control methods basically show the same performance, with both horizontal and vertical voltage/energy balance with symmetrical capacitance.

2) Performance of Control Schemes With Horizontal Capacitance Asymmetry

Each leg B SM capacitance is assumed to be $0.9C_{SM}$, while that of legs A and C are C_{SM}. Fig. 11 shows the waveforms when only a common-mode capacitor voltage sum controller is used. Because the common-mode capacitor voltage sums are horizontally balanced, the average common-mode capacitor energy sum of leg B is lower than those in legs A and C [see Fig. 11(c)-(f)]. In the horizontal asymmetry case, without vertical balancing (differential-mode capacitor voltage/energy sum) control, the dc link current and common-mode currents show no difference from those of the symmetric case [see (a) and (b) in Fig. 9 and Fig. 11].

The effectiveness of control Methods I to IV with horizontal asymmetry can be assessed from the simulation waveforms in

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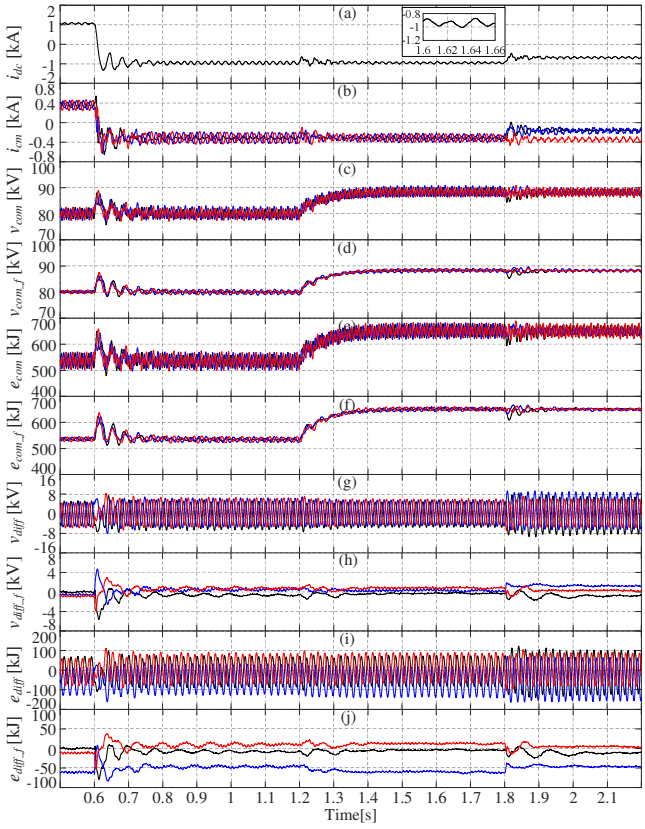

Fig. 13. Waveforms of average voltage controller in vertical asymmetry case: (a) dc link current i_{dc}, (b) common-mode current i_{cm}, (c) common-mode capacitor voltage sum v_{com}, (d) filtered common-mode capacitor voltage sum v_{com_f}, (e) common-mode capacitor energy sum e_{com}, (f) filtered common-mode capacitor energy sum e_{com_f}, (g) differential-mode capacitor voltage sum v_{diff}, (h) filtered differential-mode capacitor voltage sum v_{diff_f}, (i) differential-mode capacitor energy sum e_{diff}, (j) filtered differential-mode capacitor energy sum e_{diff_f}.

Fig. 12 (only the filtered waveforms of the capacitor voltage and energy sums are presented). The system operating conditions remain unchanged. When horizontal voltage balance is accomplished by Methods I and II, the common-mode capacitor energy sum stored in leg B is lower than symmetrical legs A and C because of lower capacitance during steady-state and remain unchanged during dynamic conditions. This indicates the three legs exchange zero energy (active power integral) with the ac grid [see (c) and (d) in Fig. 12-I and II]. Without vertical capacitance asymmetry, dc link current, common-mode current and differential-mode characteristics show no obvious difference from those of the symmetric case [see (a), (b), (e) and (f) in Fig. 12-I and II]. The same performance is seen in Fig. 12-IV for Method-IV that purports to control energy through equal equivalent capacitance and square of voltage sum, as discussed in section III. Fig. 12-III(c) and (d) show that with balanced common and differential mode capacitor energy sums, the capacitor voltage sum of leg B is higher than the other legs with horizontal asymmetrical capacitance (when capacitances of both arms of leg B are deliberately set different from those of legs A and C). There is no noticeable difference in the dc link current, common-mode currents and differential-mode characteristics from those of the symmetry case [see Fig. 12-III(a), (b), (e) and (f)].

3) Performance of Control Schemes With Vertical Capacitance Asymmetry

For the vertical asymmetry case of leg B, each SM capacitance of the upper arm is assumed to be $0.9C_{SM}$, while those of the lower arm are $1.1C_{SM}$. Fig. 13 shows the waveforms when only common-mode capacitor voltage sum control is used. The mean values of common-mode capacitor voltage and energy sums of the three legs are basically the same [see Fig. 13(c)-(f)]. However, without vertical symmetry, the deviations observed in the differential-mode capacitor voltage and energy sums indicate that neither vertical voltage balance nor vertical energy balance is achieved, especially in leg B [see Fig. 13(g)-(j)]. Also, the dc link and common-mode currents exhibit 50Hz oscillation [see Fig. 13(a) and (b)]. This 50Hz oscillation in the common-mode currents of the legs with symmetrical capacitances (legs A and C) is caused by coupling interaction through the shared dc bus terminal. Fundamental components of the common-mode currents further actuate small dc voltage deviations in the differential-mode capacitor voltage sum of legs A and C. Provided the dc voltage deviation between the upper and lower arms remains small, and the output ac voltages being synthesized do not require the modulation index to reach its maximum limit [see Fig. 13(g) and (h)], the MMC output ac voltage is not affected.

MMC internal dynamic regulation performance results for Methods I to IV during vertical asymmetry are given in Fig. 14. For the voltage-based control schemes in Fig. 14-I and II (c) and (d), horizontal voltage balance is maintained, with the mean values of the common-mode capacitor energy sums controlled to be equal and constant. Also, the vertical voltage balance controllers have reduced the deviation of the mean differential-mode capacitor voltage sum to zero, achieving equalization of the total dc capacitor voltage sum across both arms of each leg under normal and fault conditions [see (e) in Fig. 14-I and II]. However, the capacitor energy sums of each arm remain unequal as predicted [see (f) in Fig. 14-I and II]. With these voltage-based methods that include both horizontal and vertical controllers, the positive and negative sequence fundamental currents which appear as unbalanced ac components in the common-mode currents, are significantly reduced, with the 50Hz negative sequence current that appears as oscillation in the dc link current being suppressed [see (a) and (b) in Fig. 14-I and II]. Also, the results of Method-IV (capacitor voltage sum squared as the control variable instead of the actual energy), indicate that its performance under normal and abnormal conditions is similar to that of the Methods I and II [see Fig. 14-IV]. In contrast, the results of Method-III that exploits the actual energy as control variables, show that the horizontal balancing indicators such as the common-mode capacitor energy and voltage sums remain balanced during vertical asymmetry [see Fig. 14-III(c) and (d)]. The differential-mode capacitor energy sums of all three legs are, however, nullified after an extended oscillation period (which indicates vertical arm energy balance is ensured), under both normal and fault conditions [see Fig. 14-III(f)]. However, ensuring vertical energy balance in Method-

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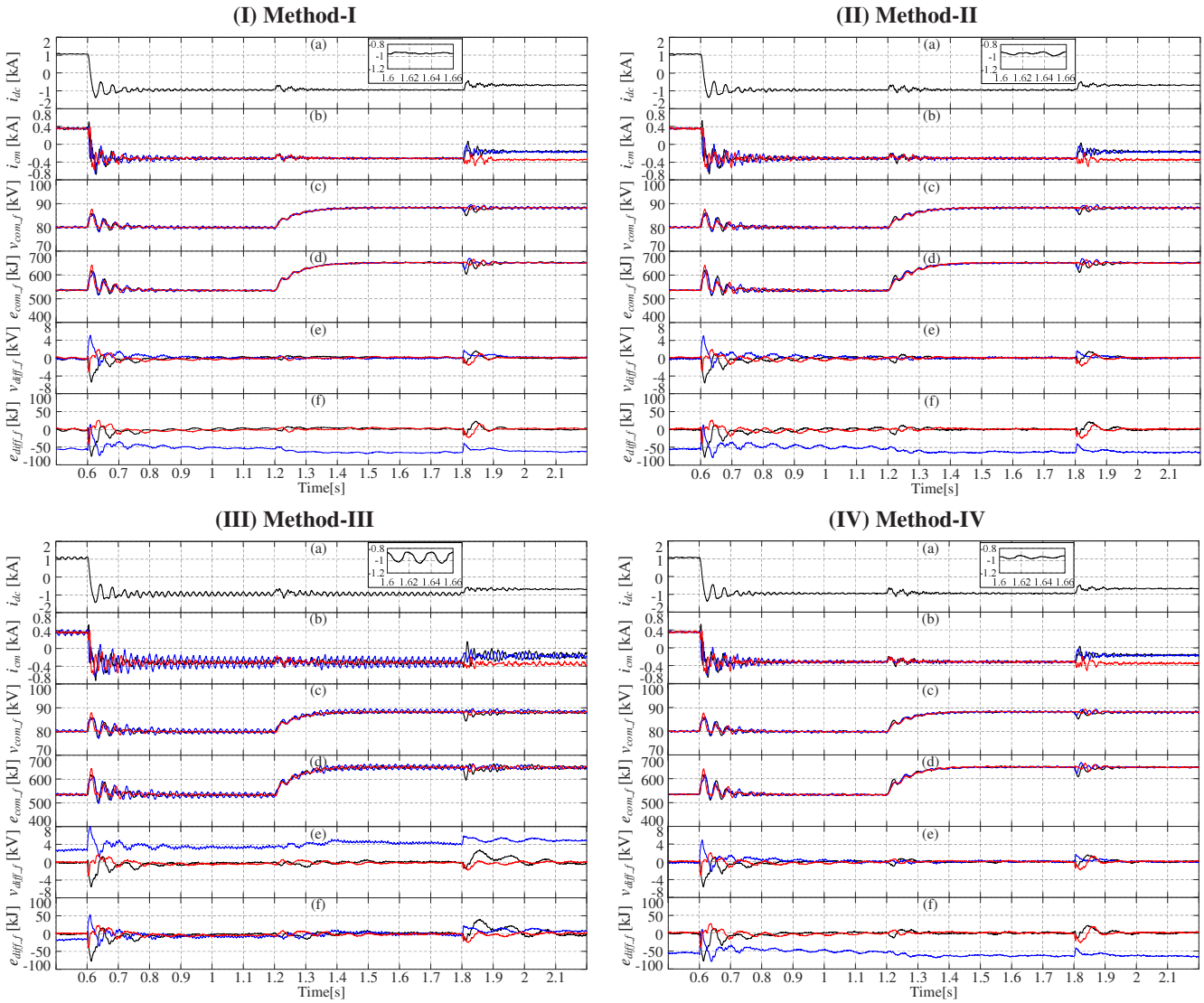

Fig. 14. Waveforms of Methods I to IV in vertical asymmetry case: (a) dc link current i_{dc}, (b) common-mode current i_{cm}, (c) filtered common-mode capacitor voltage sum v_{com_f}, (d) filtered common-mode capacitor energy sum e_{com_f}, (e) filtered differential-mode capacitor voltage sum v_{diff_f}, (f) filtered differential-mode capacitor energy sum e_{diff_f}.

III increases the deviation of the mean differential-mode capacitor voltage sums from zero, which leads to failure of arm vertical voltage balance in the case of vertical asymmetry [see Fig. 14-III(e)]. This phenomenon increases the magnitudes of unbalanced 50Hz components in the common-mode currents and common-mode capacitor voltage, which reflect into the dc link current [see Fig. 14-III(a)-(d)]. As Method-III fails to ensure arm voltage balance, the mean capacitor voltage sum of leg B lower arm is approximately 38kV and 42kV, respectively, before and after the application of the step change to the common-mode capacitor voltage sum at 1.2s. This indicates that the dc voltage across the lower arm remains below 40kV and 44kV, respectively, before and after 1.2s, but high enough and sufficient to synthesize the required MMC output ac voltage amplitude. Thus, no distortion is observed in the output ac voltage [see Fig. 8(c) and Fig. 14-III(e)].

4) Performance of Direct Fundamental Current Ripple Suppression

This paper proposes an alternative method to directly eliminate the fundamental components from the MMC common-mode currents, where significant vertical capacitance asymmetry is expected. Instead of dedicated voltage or energy-based differential-mode controllers, a PR controller tuned at 50Hz is used to suppress the ωcomponent in the common-mode currents. This means, a zero-magnitude fundamental component is adopted as the reference for the 50Hz band, rather than the differential-mode capacitor voltage sum controllers PI_V^{Δ} in Fig. 3. Its effectiveness has been assessed in this subsection and experimental results in the section VI. Simulation waveforms with zero and ±10% vertical capacitance tolerances are presented in Fig. 15-I and II respectively. These results show that with the common-mode capacitor voltage sum being controlled, horizontal capacitor voltage balance is

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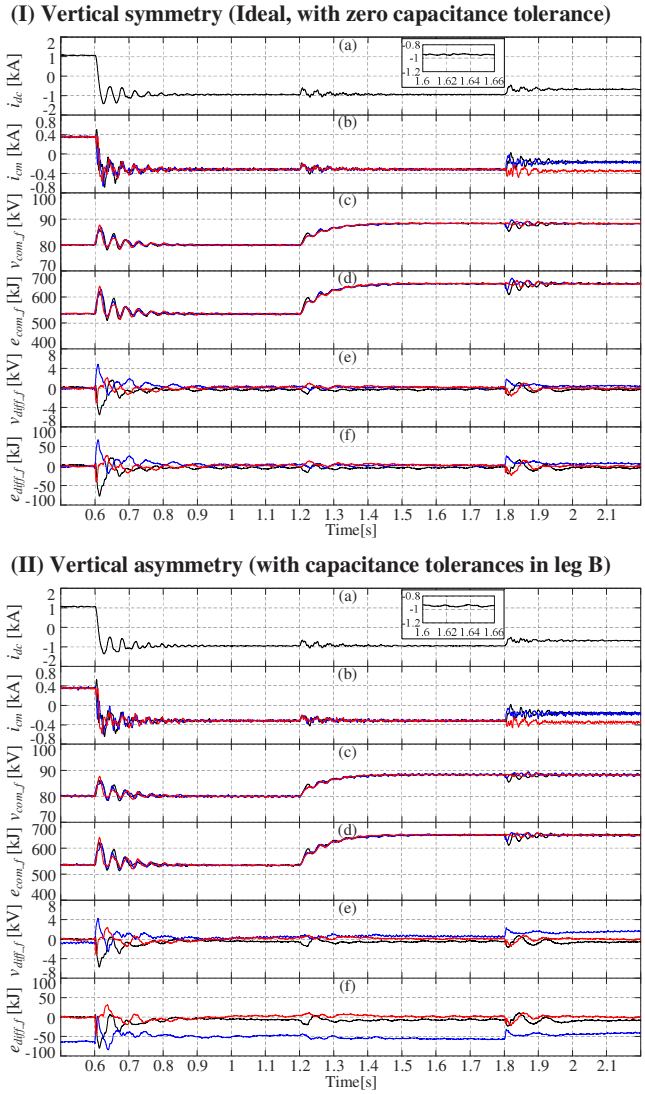

Fig. 15. Waveforms of the direct fundamental oscillation elimination method in symmetry and vertical asymmetry cases: (a) dc link current i_{dc}, (b) common-mode current i_{cm}, (c) filtered common-mode capacitor voltage sum v_{com_f}, (d) filtered common-mode capacitor energy sum e_{com_f}, (e) filtered differential-mode capacitor voltage sum v_{diff_f}, (f) filtered differential-mode capacitor energy sum e_{diff_f}.

achieved [see (c) in Fig. 15-I and II]. When vertical capacitance tolerance asymmetry is considered, the 50Hz oscillation in the common-mode currents of the three legs and dc link current are suppressed [see Fig. 15-II(a) and (b)]. The 50Hz fundamental oscillation of the common-mode capacitor voltage is cancelled by injecting the appropriate fundamental frequency voltage into the modulating signals in order to produce the needed fundamental current to neutralize the 50Hz component [see Fig. 15-II(c)]. However, the proposed fundamental current elimination is unable to nullify the mean differential capacitor voltage sums with vertical capacitance asymmetry (both arm capacitor voltages remain unbalanced) [see Fig. 15-II(d) and (e)]. This may limit the maximum attainable modulation index as the arms with the lower dc voltages would be unable to synthesize the needed arm voltages at high modulation indices.

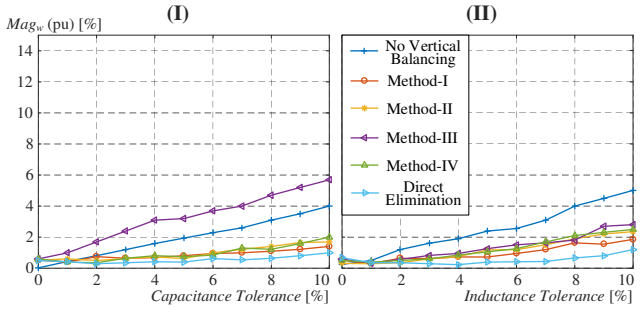

Fig. 16. The relationship between normalized dc link current ripple magnitude and passive component tolerances, with different control methods (Table I).

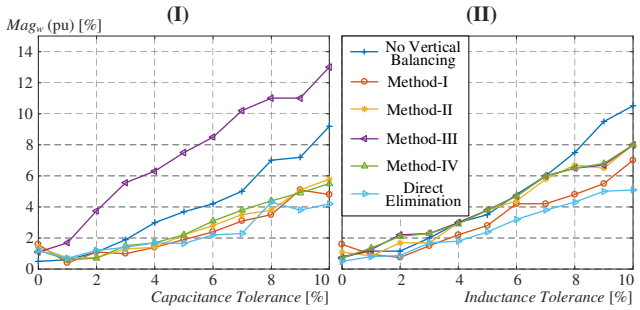

Fig. 17. The relationship between normalized dc link current ripple magnitude and passive component tolerances, with different control methods (Table II).

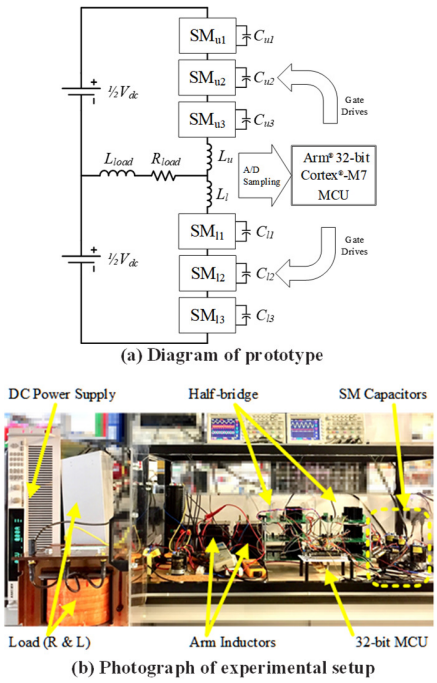

Fig. 18. Schematic diagram and photograph of the prototype scale-down single-phase MMC with three SMs per arm.

C. *Overall Comparison, in Terms of Fundamental Current Ripple*

Iterative simulations of methods for a range of SM capacitance and arm inductance tolerances show the overall relationship between the passive component tolerances and normalized fundamental frequency dc link current ripple

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magnitude with different voltage levels, in Fig. 16 and Fig. 17 respectively. The base of ripple magnitude normalization is the mean dc link current.

Based on the parameters in Table I, the overall relationship between vertical capacitance and inductance asymmetry (different capacitance and inductance tolerances between upper and lower arms of the same leg) and normalized magnitude of fundamental frequency dc link current ripple are shown in Fig. 16-I and Fig. 16-II respectively, based on the different control methods being examined in this paper. Under these simulated conditions, the fundamental ripple magnitude is generally below 5% with all control methods, for SM capacitance and arm inductance tolerances ranging from 0 to 10%. With no vertical balancing controller, no fundamental current appears in the dc link when SM capacitance and arm inductance tolerances are zero (ideal or vertical symmetry), but the 50Hz oscillation magnitude in the dc link current increases linearly with MMC passive component tolerance. This study also shows that as capacitance asymmetry increases, control methods I, II, IV and the direct fundamental frequency current elimination method remain capable of suppressing the dc link fundamental current ripple. Method-III, however, leads to the fundamental frequency current ripple magnitudes increasing with the increasing SM capacitance tolerance. The conclusions drawn from the above discussion of Fig. 16 are in accordance with the approximate theoretical analysis articulated mathematically in (23).

To further illustrate the impact of the switching voltage step (voltage per SM) on dc power quality, the same MMC system and control methods with different parameters, as listed in Table II, is investigated.

The plots in Fig. 17 for the 100kV dc link voltage MMC with each SM voltage of 5kV show the same trend as counterparts in Fig. 16 when the dc link voltage is 40kV and SM voltage is 2kV. In addition to the increased fundamental current ripples due to capacitance and inductance tolerances, Fig. 16 and Fig. 17 show further increase of the current ripple with the dc link voltage, meaning that the ripple amplitude is exacerbated by the increased average SM capacitor voltage (or switching voltage), confirming the theoretical discussion in section IV. The traces of two MMCs (40MVA and 100MVA) in Fig. 16 and Fig. 17 are for the same dc current (1kA), arm inductance and converter inertia in per unit.

TABLE II
SIMULATION PARAMETERS OF THE 100MVA MMC

Rated power	100MVA
DC voltage	100kV
AC grid line voltage	66kV
AC grid frequency	50Hz
Transformer leakage inductance	0.18pu
Transformer ratio	50/66kV
Arm inductance	15.3mH(0.2pu)
Numbers of SMs per arm	20
SM capacitance	2.7mF(40kJ/MVA)
Modulation carrier frequency	1.0kHz

In summary, the vertical passive component tolerances tend to cause drift of the differential-mode capacitor voltage sum from zero and fundamental frequency dc link current ripple for an MMC system, as pointed out in the mathematical expressions (23), (27) and (28). The arm-level SM capacitor voltage sum imbalance and fundamental frequency dc current ripple due to vertical parameter asymmetry displayed in the simulations waveforms confirm the main hypothesis and discussion in section IV. Voltage-based vertical balancing controllers (Methods I, II and IV), based on expressions (17) and (18), can eliminate the differential-mode capacitor voltage sum, and suppress the fundamental frequency oscillation in the common-mode loop to some extent. The proposed control method that directly suppresses fundamental components of the common-mode current in (27) and (28) regardless of arm voltage balance, shows superior performance in terms of dc link fundamental current ripple suppression.

VI. EXPERIMENTAL RESULTS

This section uses a prototype single-phase MMC shown in Fig. 18, with parameters in Table III and IV, to validate the previously presented analysis and simulations, particularly, with regard to the relationship between passive parameter mismatch, differential-mode capacitor voltage sum, and induced fundamental circulating current. As part of validation process, a number of experimental scenarios are presented, namely, no vertical balancing, and scenarios with Method-II (voltage-based vertical balancing), Method-III (energy-based vertical balancing) and the proposed direct fundamental circulating current elimination method. Table IV shows SM capacitances and inductances of the experimental test rig, with vertical symmetrical and asymmetrical capacitances. Besides capacitor voltage balancing, the horizontal voltage balancing controller that regulates the mean common-mode capacitor voltage sum of the phase-leg at rated dc link voltage (300V), is implemented in all scenarios. The sorting-based inner arm SM voltage balancing method with PD-PWM modulation is adopted.

TABLE III
PARAMETERS OF THE SINGLE-PHASE MMC PROTOTYPE

Rated power	1kW
DC voltage V_{dc}	300V
Load resistance R_{load}	5Ω
Load inductance L_{load}	12.5mH
Nominal arm inductance L_{arm}	5mH
Numbers of SMs per arm	3
Nominal SM capacitance C_{SM}	1.8mF
Modulation index	0.8
Modulation carrier frequency	2.0kHz

TABLE IV
VALUES OF THE PASSIVE COMPONENTS
(FOR BOTH SYMMETRY AND ASYMMETRY CASES)

	Symmetry	**Asymmetry**
C_{u1}	1.84mF	
C_{u2}	1.80mF	
C_{u3}	1.78mF	
C_{l1}	1.82mF	
C_{l2}	1.74mF	1.62mF
C_{l3}	1.79mF	1.66mF
L_u	5.5mH	
L_l	5.7mH	

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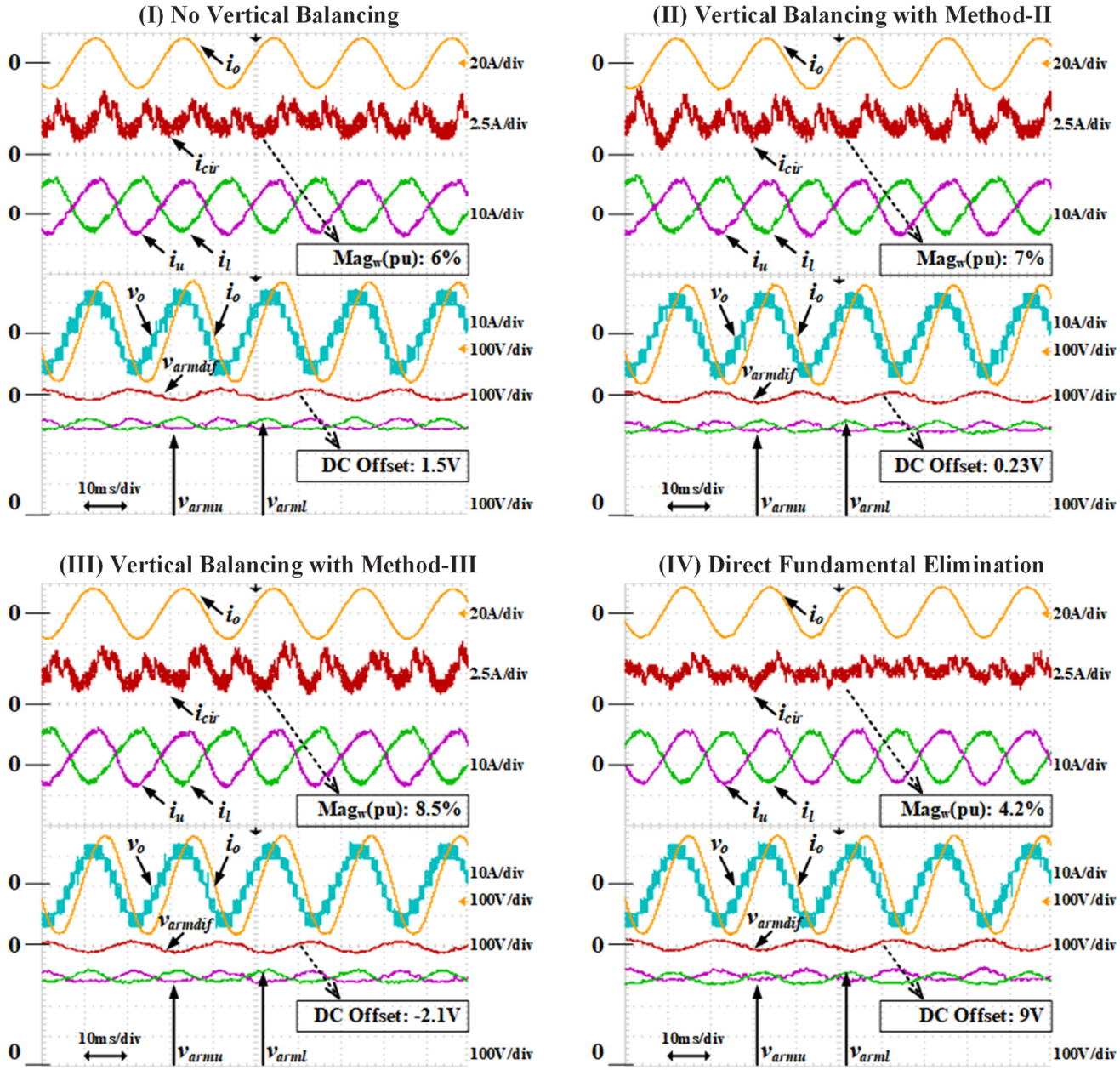

Fig. 19. Waveforms of no vertical balancing, Method-II, Method-III and the direct elimination method in vertical symmetry case.

Fig. 19 shows experimental waveforms with no vertical balancing, voltage-based vertical balancing, energy-based vertical balancing, and the proposed direct fundamental circulating elimination method, when the SM capacitors are near match in order to reflect the ideal case of vertical symmetry. The fundamental circulating current magnitude of the method without vertical balancing is smallest in symmetrical case because no active injected current is present, as shown Fig. 16 and Fig. 17. The magnitude of fundamental circulating currents that exist in the common-mode current are practically the same for the cases with voltage-based vertical balancing and energy-based vertical balancing, see Fig. 19-II and III. While the proposed direct elimination of fundamental current exhibits a reduction compared with that of the voltage/energy balancing methods, which can be seen in Fig. 19-IV, but with the penalty of creating substantial arm voltage imbalance, with the error in the dc offset of the differential mode capacitor voltage sum V_{armdif} amount to 9V (equivalent to SM capacitor voltage deviations of ±1.5% from their respective nominal values). With small SM capacitance value errors plus randomness of the unquantified errors introduced by semiconductor voltage drops, switching characteristics and other nonlinearities, the cases with no vertical balancing and energy-based vertical control show modest drifts or errors between the capacitor voltage sums across the upper and lower arms (see Fig. 19-I and III), while the voltage-based vertical balancing in Fig. 19-II shows the smallest dc voltage error

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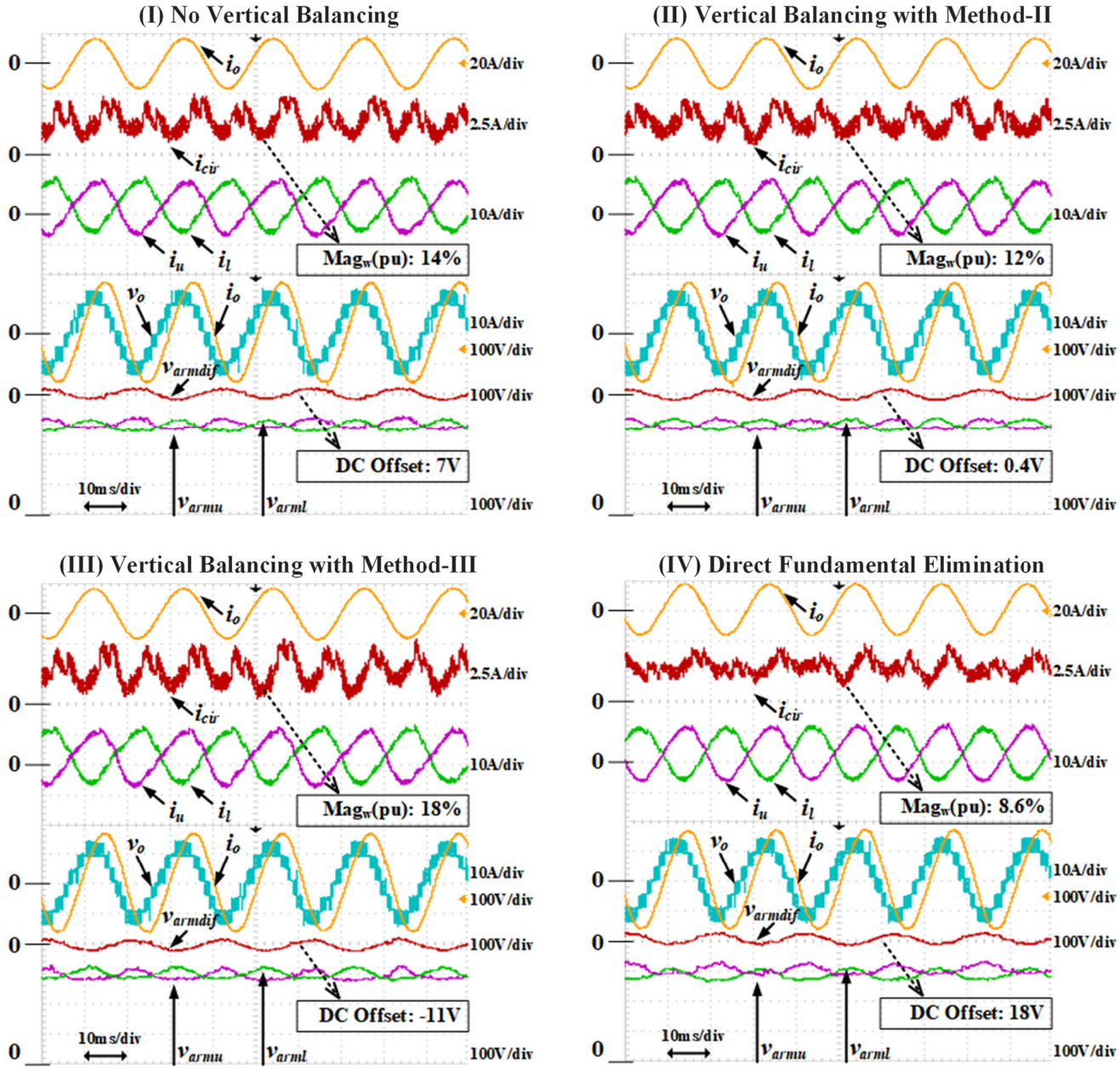

Fig. 20. Waveforms of no vertical balancing, Method-II, Method-III and the direct elimination method in vertical asymmetry case.

between the upper and lower arms. The differences in the quality of the output voltage and current waveforms between these methods are small (worst-case output phase voltage and current total harmonic distortions of 20.3% and 0.4% respectively).

In contrast, Fig. 20 shows experimental waveforms for the considered methods with the asymmetrical capacitance shown in Table IV. Magnitudes of the fundamental circulating current increase for all methods, and cases without vertical balancing and with the energy-based vertical balancing exhibit larger fundamental circulating currents and larger errors in the differential-mode capacitor voltage sums (large degree of voltage imbalance between upper and lower arms), see Fig. 20-I and III. On the other hand, the fundamental frequency circulating current magnitude is greatly suppressed by the proposed direct elimination method, but creates a voltage imbalance between the upper and lower arms, see Fig. 20-IV. Thus, capacitor voltages exhibit deviations of ±3V for each SM (±3% from their respective nominal values). The voltage-based vertical balancing method in Fig. 20-II shows the best overall performance in terms of compromise between fundamental circulating current magnitude and arm voltage imbalance. The results in Fig. 19 and Fig. 20 confirm the theoretical analysis and discussion presented in sections III and IV and simulations in Fig. 6. The differences in the quality of the output voltage and current waveforms between the methods are small (THD = 21.1% and 0.49% respectively).

In summary, the presented experimental waveforms

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TABLE V
SUMMARIZED FEATURES OF THE ASSESSED INTERNAL CONTROL SCHEMES

	Method-I	Method-II	Method-III	Method-IV	Direct Elimination
SM-Level Performance	Able to equally distribute the total arm voltage across SM capacitors. All switching devices operate at a fixed frequency.	Able to equally distribute the total arm voltage across SM capacitors, but switching devices operate at the frequency that varies within a limited range.			
Arm-Level (Vertical) Balancing	Able to suppress the capacitor voltage difference between upper and lower arms of each phase-leg to near zero even when passive components have significant tolerance.	Able to suppress the capacitor voltage difference between the upper and lower arms of each phase-leg to near zero even when passive components have significant tolerance.	The capacitor voltage difference between upper and lower arms of one phase-leg increases rapidly with capacitance tolerance.	Able to suppress the capacitor voltage difference between the upper and lower arms of each phase-leg to near zero even when passive components have significant tolerance.	Cannot ensure capacitor voltage difference between upper and lower arms of one phase-leg to be zero when passive components have significant tolerance.
AC Side Performance	Minimizes the risk of dc offsets in ac output voltages and currents, due to its vertical balancing capability.	Minimizes the risk of dc offsets in ac output voltages and currents, due to its vertical balancing capability.	Imposes potential risk of dc offsets in ac output voltages and currents due to inferior vertical balancing performance.	Minimizes the risk of dc offsets in ac output voltages and currents, due to its vertical balancing capability.	Imposes potential risk of dc offsets in ac output voltages and currents due to lack of actively vertical balancing capability.
DC Side Performance	Able to reduce the fundamental frequency ripple in dc link current in practical systems with vertically passive component tolerances.	Able to reduce the fundamental frequency ripple in dc link current in practical systems with vertically passive component tolerances.	Unable to reduce the fundamental frequency ripple in dc link current in practical systems with vertical capacitance tolerances.	Able to reduce the fundamental frequency ripple in dc link current in practical systems with vertically passive component tolerances.	Exhibits superior capacity of suppressing the fundamental frequency ripple in dc link current in practical systems with vertically passive components tolerances.
Leg-Level (Horizontal) Balancing	Maintains common-mode capacitor voltage sums of phase-legs to be practically balanced, avoiding the risk of momentary inrush currents during the operation near maximum modulation index.	Maintains common-mode capacitor voltage sums of phase-legs to be practically balanced, avoiding the risk of momentary inrush currents during the operation near maximum modulation index.	Creates unbalanced common-mode capacitor voltage sums across the phase-legs in practical systems with horizontal passive component tolerances. The risk of curtailing synthesis of the maximum ac output voltage increases in the phase-leg that possess larger equivalent capacitance. The phase-leg that possess smaller equivalent capacitance may experience over-voltage.	Maintains common-mode capacitor voltage sums of phase-legs to be practically balanced, avoiding the risk of momentary inrush currents during the operation near maximum modulation index.	Maintains common-mode capacitor voltage sums of phase-legs to be practically balanced, avoiding the risk of momentary inrush currents during the operation near maximum modulation index.

corroborate the detailed theoretical analysis presented in section IV, and the discussion of impacts of vertical asymmetry of the passive components on the MMC performance in Fig. 16 and 17. Philosophically, it can be argued that for an MMC with passive component tolerances, the voltage and equivalent energy based vertical controllers estimate an appropriate amount of fundamental voltage to be injected into the common-mode voltage of each phase-leg in order to force the differential-mode capacitor voltage sums to be zero, therefore, the fundamental current ripples in the common-mode and dc currents are the by-products. The proposed method estimates a suitable fundamental voltage to be injected into the common-mode loop of each phase-leg in order to directly eliminate the fundamental components from the common-mode and dc link currents, with the differential-mode capacitor voltage sum deviations being the by-products.

VII. CONCLUSION

Table V summarizes the main attributes and limitations of the different methods of managing MMC internal dynamics investigated in this paper.

This paper has presented a comprehensive review and assessment of a number of existing PR-based internal controllers that manage MMC horizontal and vertical balancing and dynamics when passive component tolerances are considered. The difference of distributed and non-distributed submodule capacitor voltage balancing (inner arm balancing) on the performance of horizontal and vertical balancing controllers is also taken into account. Simulations under a number of severe test scenarios (such as unrestrained step change in the reference active power and average capacitor voltage per leg, and single-phase-to-ground ac fault) and experimental results for different vertical balancing methods were presented. The main contribution and significance of the

research presented in this paper beyond those previously explored in the literature are as follows:

1) The presented theoretical analysis, simulations and experimentation show that submodule capacitance and arm inductance tolerances can lead to MMC performance deterioration, namely, the quality of ac and dc voltage and current waveforms, and voltage stress distribution between the upper and lower arms will be compromised;
2) Only vertical asymmetry of the submodule capacitances and arm inductances give rise to induced fundamental frequency ripple in the common-mode and dc link currents, and unequal dc voltage sharing between the MMC upper and lower arms, which can lead to dc offsets in the output phase currents and voltages. The presented detailed parametric studies revealed that these problems are acute for an MMC with larger switching voltages (voltage per SM capacitor). The horizontal asymmetry of the SM capacitances and arm inductances does not induce fundamental ripple into the common-mode and dc link currents or imbalance between upper and lower MMC arms of one phase-leg. Besides substantial differences in the energy storage of the three phase-legs, horizontal asymmetry leads to significant differences in control effort, which may affect utilization of the phase-legs (arm with larger or lower dc modulation index may suffer from under-utilization as its ability to synthesize ac voltage is curtailed);
3) Detailed investigation revealed that energy-based vertical and horizontal controllers may exacerbate deterioration of dc current waveform quality and the problem of voltage imbalance between MMC upper and lower arms when passive component tolerances are significant;
4) Detailed theoretical investigation on the mechanism by which the fundamental current is induced in the MMC common-mode and dc side has led to the development of a new direct fundamental component elimination method. The effectiveness of proposed method for suppressing the fundamental ripple in the common-mode and dc currents was confirmed using simulation and corroborated experimentally. But this improved performance is achieved at the expense of increased dc voltage imbalance between the upper and lower arms; and
5) Detailed quantitative and qualitative comparisons of several methods investigated in this paper reveal that the voltage-based vertical and horizontal balancing methods offer the best overall practical compromises between suppression of fundamental ripple in the dc current and dc voltage imbalance between MMC upper and lower arms.

In summary, the findings of this paper could be applied to optimization and prediction of MMC internal dynamics and inner/outer decoupling, and scenarios when the submodule fault management is activated to bypass faulted submodules.

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REFERENCES

[1] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," *2003 IEEE Bol. PowerTech - Conf. Proc.*, vol. 3, pp. 272–277, 2003.
[2] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit topologies, modeling, control schemes, and applications of modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 4–17, 2015.
[3] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, Control, and Applications of the Modular Multilevel Converter: A Review," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 37–53, 2014.
[4] J. Wang, J. Liang, C. Wang, and X. Dong, "Circulating current suppression for MMC-HVDC under unbalanced grid conditions," *IEEE Trans. Ind. Appl.*, vol. 53, no. 4, pp. 3250–3259, 2017.
[5] X. Li, Q. Song, W. Liu, S. Xu, Z. Zhu, and X. X. Li, "Performance Analysis and Optimization of Circulating Current Control for Modular Multilevel Converter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 2, pp. 716–727, 2016.
[6] Z. Li, P. Wang, Z. Chu, H. Zhu, Y. Luo, and Y. Li, "An inner current suppressing method for modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 4873–4879, 2013.
[7] Q. Tu, Z. Xu, Y. Chang, and L. Guan, "Suppressing DC voltage ripples of MMC-HVDC under unbalanced grid conditions," *IEEE Trans. Power Deliv.*, vol. 27, no. 3, pp. 1332–1338, 2012.
[8] Y. Sun, C. A. Teixeira, D. G. Holmes, B. P. McGrath, and J. Zhao, "Low Order Circulating Current Suppression of PWM based Modular Multilevel Converters Using DC-link Voltage Compensation," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 210–225, 2018.
[9] R. Picas, S. Ceballos, J. Pou, J. Zaragoza, G. Konstantinou, and V. G. Agelidis, "Closed-loop discontinuous modulation technique for capacitor voltage ripples and switching losses reduction in modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 4714–4725, 2015.
[10] S. Debnath, J. Qin, and M. Saeedifard, "Control and Stability Analysis of Modular Multilevel Converter Under Low-Frequency Operation," *IEEE Trans. Ind. Electron.*, vol. 62, no. 9, pp. 5329–5339, 2015.
[11] J. Pou, S. Ceballos, G. Konstantinou, V. G. Agelidis, and R. Picas, "Circulating Current Injection Methods Based on Instantaneous Information for the Modular Multilevel Converter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 2, pp. 777–788, 2015.
[12] M. Vasiladiotis, N. Cherix, and A. Rufer, "Accurate capacitor voltage ripple estimation and current control considerations for grid-connected modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4568–4579, 2014.
[13] W. Yang, Q. Song, and W. Liu, "Decoupled Control of Modular Multilevel Converter Based on Intermediate," *IEEE Trans. Ind. Electron.*, vol. 63, no. 8, pp. 4695–4706, 2016.
[14] X. Shi, Z. Wang, B. Liu, Y. Liu, L. M. Tolbert, and F. Wang, "Characteristic investigation and control of a modular multilevel converter-based HVDC system under single-line-to-ground fault conditions," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 408–421, 2015.
[15] J. W. Moon, J. W. Park, D. W. Kang, and J. M. Kim, "A Control Method of HVDC-Modular Multilevel Converter Based on Arm Current under the Unbalanced Voltage Condition," *IEEE Trans. Power Deliv.*, vol. 30, no. 2, pp. 529–536, 2015.
[16] S. Cui, H. J. Lee, J. J. Jung, Y. Lee, and S. K. Sul, "A comprehensive AC side single line to ground fault ride through strategy of a modular multilevel converter for HVDC system," *2015 IEEE Energy Convers. Congr. Expo. ECCE 2015*, pp. 5378–5385, 2015.
[17] B. Jacobson, P. Karlsson, G. Asplund, L. Harnefors, and T. Jonsson, "VSC-HVDC transmission with cascaded two-level converters," *CIGRE Sess.*, pp. B4–B110, 2010.
[18] G. P. Adam, K. H. Ahmed, S. J. Finney, and B. W. Williams, "AC fault ride-through capability of a VSC-HVDC transmission systems," *2010 IEEE Energy Convers. Congr. Expo. ECCE 2010 - Proc.*, pp. 3739–3745, 2010.
[19] Y. Liang, J. Liu, T. Zhang, and Q. Yang, "Arm Current Control Strategy for MMC-HVDC under Unbalanced Conditions," *IEEE Trans. Power Deliv.*, vol. 32, no. 1, pp. 125–134, 2017.

[20] L. Xiaoqian, S. Qiang, L. Jianguo, and L. Wenhua, "Capacitor Voltage Balancing Control based on CPS-PWM of Modular Multilevel Converter," in *Energy Conversion Congress and Exposition (ECCE), 2011 IEEE*, 2011, pp. 4029–4034.

[21] J. Qin, S. Member, and M. Saeedifard, "Reduced Switching-Frequency Voltage-Balancing Strategies for Modular Multilevel," *IEEE Trans. Power Deliv.*, vol. 28, no. 4, p. 6415, 2013.

[22] M. B. De Alvarenga and J. A. Pomilio, "Voltage balancing and commutation suppression in symmetrical cascade multilevel converters for power quality applications," *IEEE Trans. Ind. Electron.*, vol. 61, no. 11, pp. 5996–6003, 2014.

[23] K. Ilves, L. Harnefors, S. Norrga, and H. P. Nee, "Predictive sorting algorithm for modular multilevel converters minimizing the spread in the submodule capacitor voltages," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 440–449, 2015.

[24] D. Siemaszko, "Fast sorting method for balancing capacitor voltages in modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 463–470, 2015.

[25] H. Peng, R. Xie, K. Wang, Y. Deng, X. He, and R. Zhao, "A Capacitor Voltage Balancing Method With Fundamental Sorting Frequency for Modular Multilevel Converters Under Staircase Modulation," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7809–7822, 2016.

[26] M. Hagiwara and H. Akagi, "PWM Control and Experiment of Modular Multilevel Converters," in *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*, 2008, pp. 154–161.

[27] S. Du and J. Liu, "A study on dc voltage control for chopper-cell-based modular multilevel converters in d-statcom application," *IEEE Trans. Power Deliv.*, vol. 28, no. 4, pp. 2030–2038, 2013.

[28] K. Sekiguchi, P. Khamphakdi, M. Hagiwara, and H. Akagi, "A grid-level high-power BTB (back-to-back) system using modular multilevel cascade converters withoutcommon DC-link capacitor," *IEEE Trans. Ind. Appl.*, vol. 50, no. 4, pp. 2648–2659, 2014.

[29] N. Thitichaiworakorn, M. Hagiwara, and H. Akagi, "Experimental verification of a modular multilevel cascade inverter based on double-star bridge cells," *IEEE Trans. Ind. Appl.*, vol. 50, no. 1, pp. 509–519, 2014.

[30] M. Zhang, L. Huang, W. Yao, and Z. Lu, "Circulating harmonic current elimination of a CPS-PWM-based modular multilevel converter with a plug-in repetitive controller," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 2083–2097, 2014.

[31] P. Khamphakdi, M. Nitta, M. Hagiwara, and H. Akagi, "A Transformerless Back-To-Back (BTB) System Using Modular Multilevel Cascade Converters For Power Distribution Systems," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 1866–1875, 2015.

[32] B. Li, S. Shi, D. Xu, and W. Wang, "Control and analysis of the modular multilevel dc de-icer with statcom functionality," *IEEE Trans. Ind. Electron.*, vol. 63, no. 9, pp. 5465–5476, 2016.

[33] F. Sasongko, K. Sekiguchi, K. Oguma, M. Hagiwara, and H. Akagi, "Theory and Experiment on an Optimal Carrier Frequency of a Modular Multilevel Cascade Converter with Phase-Shifted PWM," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3456–3471, 2016.

[34] B. Tai, C. Gao, X. Liu, and Z. Chen, "A Novel Flexible Capacitor Voltage Control Strategy for Variable-Speed Drives With Modular Multilevel Converters," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 128–141, 2017.

[35] P. Münch, D. Görges, M. Izák, and S. Liu, "Integrated current control, energy control and energy balancing of Modular Multilevel Converters," *IECON 2010 - 36th Annu. Conf. IEEE Ind. Electron. Soc.*, pp. 150–155, 2010.

[36] A. Antonopoulos, L. Ängquist, and H.-P. Nee, "On dynamics and voltage control of the modular multilevel converter," *Power Electron. Appl. 2009. EPE'09. 13th Eur. Conf.*, pp. 1–10, 2009.

[37] M. Vasiladiotis, N. Cherix, and A. Rufer, "Impact of Grid Asymmetries on the Operation and Capacitive Energy Storage Design of Modular Multilevel Converters," *IEEE Trans. Ind. Electron.*, vol. 62, no. 11, pp. 6697–6707, 2015.

[38] A. E. Leon and S. J. Amodeo, "Energy Balancing Improvement of Modular Multilevel Converters under Unbalanced Grid Conditions," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 6628–6637, 2017.

[39] J. J. Jung, S. Cui, Y. Lee, and S. K. Sul, "A cell capacitor energy balancing control of MMC-HVDC under the AC grid faults," *9th Int. Conf. Power Electron. - ECCE Asia "Green World with Power Electron. ICPE 2015-ECCE Asia*, pp. 1–8, 2015.

[40] P. Hu, D. Jiang, Y. Zhou, "Energy-balancing Control Strategy for Modular Multilevel Converters Under Submodule," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 5021–5030, 2014.

[41] S. Cui, S. Kim, J. J. Jung, and S. K. Sul, "A comprehensive cell capacitor energy control strategy of a modular multilevel converter (MMC) without a stiff DC bus voltage source," *Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC*, no. Mmc, pp. 602–609, 2014.

[42] S. Fan, K. Zhang, J. Xiong, and Y. Xue, "An Improved Control System for Modular Multilevel Converters with New Modulation Strategy and Voltage Balancing Control," *IEEE Trans. Power Electron.*, vol. PP, no. 99, pp. 1–1, 2014.

[43] G. Bergna *et al.*, "A generalized power control approach in ABC frame for modular multilevel converter HVDC links based on mathematical optimization," *IEEE Trans. Power Deliv.*, vol. 29, no. 1, pp. 386–394, 2014.

[44] G. Bergna *et al.*, "An energy-based controller for HVDC modular multilevel converter in decoupled double synchronous reference frame for voltage oscillation reduction," *IEEE Trans. Ind. Electron.*, vol. 60, no. 6, pp. 2360–2371, 2013.

[45] R. Lizana, M. A. Perez, S. Bernet, J. R. Espinoza, and J. Rodriguez, "Control of Arm Capacitor Voltages in Modular Multilevel Converters," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1774–1784, 2016.

[46] M. Vatani, S. Member, M. Hovd, and S. Member, "Control of the Modular Multilevel Converter Based on a Discrete-Time Bilinear Model Using the Sum of Squares Decomposition Method," *IEEE Trans. Power Deliv.*, vol. 30, no. 5, pp. 2179–2188, 2015.

[47] H. Saad, X. Guillaud, J. Mahseredjian, S. Dennetière, and S. Nguefeu, "MMC Capacitor Voltage Decoupling and Balancing Controls," *IEEE Trans. Power Deliv.*, vol. 30, no. 2, pp. 704–712, 2015.

[48] J. J. Jung, S. Cui, S. Kim, and S. K. Sul, "A cell capacitor energy balancing control of Modular Multilevel Converter considering the unbalanced AC grid conditions," *2014 Int. Power Electron. Conf. IPEC-Hiroshima - ECCE Asia 2014*, pp. 1268–1275, 2014.

[49] S. Liu, J. Jiang, and Y. Wan, "Generalised analytical methods and current-energy control design for modular multilevel cascade converter," *IET Power Electron.*, vol. 6, no. 3, pp. 495–504, 2013.

[50] J. Wang, J. Liang, F. Gao, X. Dong, C. Wang, and B. Zhao, "A Closed-loop Time-domain Analysis Method for Modular Multilevel Converter," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7494–7508, 2016.

[51] Q. Song, W. Liu, X. Li, H. Rao, S. Xu, and L. Li, "A steady-state analysis method for a modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 28, no. 8, pp. 3702–3713, 2013.

[52] K. Ilves, A. Antonopoulos, and S. Norrga, "Steady-State Analysis of Interaction Between Harmonic Components of Arm and Line Quantities of Modular Multilevel Converters," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 57–68, 2012.

[53] A. Dekka, B. Wu, R. Lizana, and N. R. Zargari, "A comparison of voltage balancing versus energy balancing approach for modular multilevel converters," in *IECON Proceedings (Industrial Electronics Conference)*, 2016, pp. 3117–3122.

[54] R. Zeng, L. Xu, L. Yao, and S. J. Finney, "Analysis and Control of Modular Multilevel Converters under Unbalanced Conditions," *IEEE Trans. Ind. Electron.*, vol. 63, no. 1, pp. 71–81, 2016.

[55] N. R. Mehrabadi, R. Burgos, D. Boroyevich, and C. Roy, "Modeling and Design of the Modular Multilevel Converter with Parametric and Model-Form Uncertainty Quantification," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017, pp. 1513–1520.

[56] F. Zhang, C. Zhao, and J. Xu, "New control strategy of decoupling the AC/DC voltage offset for modular multilevel converter," *IET Gener. Transm. Distrib. Spec.*, vol. 10, no. 6, pp. 1382–1392, 2016.

[57] G. Liu, Z. Xu, Y. Xue, and G. Tang, "Optimized control strategy based on dynamic redundancy for the modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 339–348, 2015.

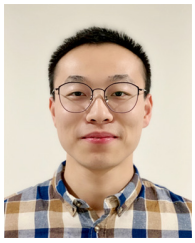
[58] D. Wu and P. Li, "Characteristics of nearest level modulation method with circulating current control for modular multilevel converter," *IET Power Electron.*, vol. 9, no. 2, pp. 155–164, 2016.

[59] L. Lin, Y. Lin, Z. He, Y. Chen, J. Hu, and W. Li, "Improved Nearest-Level Modulation for a Modular Multilevel Converter With a Lower Submodule Number," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5369–5377, 2016.

[60] Q. Tu, Z. Xu, and L. Xu, "Reduced Switching-frequency modulation and circulating current suppression for modular multilevel converters," *IEEE Trans. Power Deliv.*, vol. 26, no. 3, pp. 2009–2017, 2011.

[61] W. Li, L. A. Gregoire, and J. Belanger, "A Modular Multilevel Converter Pulse Generation and Capacitor Voltage Balance Method Optimized for FPGA Implementation," *IEEE Trans. Ind. Electron.*, vol. 62, no. 5, pp. 2859–2867, 2015.

[62] G. P. Adam, O. Anaya-Lara, G. M. Burt, D. Telford, B. W. Williams, and J. R. McDonald, "Modular multilevel inverter: pulse width modulation and capacitor balancing technique," *IET Power Electron.*, vol. 3, no. 5, p. 702, 2010.
[63] S. Rohner, S. Bernet, M. Hiller, and R. Sommer, "Pulse width modulation scheme for the modular multilevel converter," *Power Electron. Appl. 2009. EPE '09. 13th Eur. Conf.*, pp. 1–10, 2009.
[64] A. Marquez *et al.*, "Variable-Angle Phase-Shifted PWM for Multilevel Three-Cell Cascaded H-Bridge Converters," *IEEE Trans. Ind. Electron.*, vol. 64, no. 5, pp. 3619–3628, 2017.
[65] F. Sasongko and H. Akagi, "Low-Switching-Frequency Operation of a Modular Multilevel DSCC Converter with Phase-Shifted Rotating-Carrier PWM," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5058–5069, 2017.
[66] K. Ilves, L. Harnefors, S. Norrga, and H. P. Nee, "Analysis and operation of modular multilevel converters with phase-shifted carrier PWM," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 268–283, 2015.
[67] B. Li, R. Yang, D. Xu, G. Wang, W. Wang, and D. Xu, "Analysis of the phase-shifted carrier modulation for modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 297–310, 2015.
[68] C. D. Townsend, T. J. Summers, and R. E. Betz, "Phase-Shifted Carrier Modulation Techniques for Cascaded H-Bridge Multilevel Converters," *IEEE Trans. Ind. Electron.*, vol. 62, no. 11, pp. 6684–6696, 2015.
[69] A. Dekka, B. Wu, R. L. Fuentes, M. Perez, and N. R. Zargari, "Voltage-Balancing Approach With Improved Harmonic Performance for Modular Multilevel Converters," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 5878–5884, 2017.
[70] B. Bahrani, S. Debnath, and M. Saeedifard, "Circulating Current Suppression of the Modular Multilevel Converter in a Double-Frequency Rotating Reference Frame," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 783–792, 2016.
[71] M. Hagiwara and H. Akagi, "Control and Experiment of Pulsewidth-Modulated Modular Multilevel Converters," *IEEE Trans. Power Electron. power*, vol. 24, no. 7, pp. 1737–1746, 2009.
[72] J. Asakura and H. Akagi, "State-of-Charge (SOC)-Balancing Control of a Battery Energy Storage System Based on a Cascade PWM Converter," *IEEE Trans. Power Electron.*, vol. 24, no. 6, pp. 1628–1636, 2009.
[73] R. Lizana *et al.*, "Decoupled Current Model and Control of Modular Multilevel Converters," *IEEE Trans. Ind. Electron.*, vol. 62, no. 9, pp. 5382–5392, 2015.
[74] B. Yang, Q. Ge, L. Zhao, and Z. Zhou, "The Study of Dead-Time Commutation and Compensation in Dual Bridge Series Resonant DC / DC Converter," pp. 0–3, 2017.
[75] I. R. Ferreira Moreno Pinheiro Da Silva, C. B. Jacobina, and A. Cunha Oliveira, "Hybrid Single-Phase AC-AC Modular Multilevel DSCC Converters with Modulation and DC-Link Voltage Ripple Improvement," *IEEE Trans. Ind. Appl.*, vol. 53, no. 1, pp. 261–272, 2017.
[76] K. Li, L. Yuan, Z. Zhao, S. Lu, and Y. Zhang, "Fault-Tolerant Control of MMC with Hot Reserved Submodules Based on Carrier Phase Shift Modulation," *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 6778–6791, 2017.
[77] N. Thitichaiworakorn, M. Hagiwara, and H. Akagi, "Experimental verification of a modular multilevel cascade inverter based on double-star bridge cells," *IEEE Trans. Ind. Appl.*, vol. 50, no. 1, pp. 509–519, 2014.
[78] M. Hagiwara, R. Maeda, and H. Akagi, "Control and Analysis of the Modular Multilevel Cascade Converter Based on Double-Star," *IEEE Trans. Power Electron.*, vol. 26, no. 6, pp. 1649–1658, 2011.
[79] X. Shi, Z. Wang, B. Liu, Y. Li, L. M. Tolbert, and F. Wang, "Steady-State Modeling of Modular Multilevel Converter under Unbalanced Grid Conditions," *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 7306–7324, 2017.
[80] M. Saeedifard and R. Iravani, "Dynamic performance of a modular multilevel back-to-back HVDC system," *IEEE Trans. Power Deliv.*, vol. 25, no. 4, pp. 2903–2912, 2010.
[81] G. P. Adam and I. E. Davidson, "Robust and Generic Control of Full-Bridge Modular Multilevel Converter High-Voltage DC Transmission Systems," *IEEE Trans. Power Deliv.*, vol. 30, no. 6, pp. 2468–2476, 2015.
[82] A. Marzoughi, R. Burgos, D. Boroyevich, and Y. Xue, "Steady-state analysis of voltages and currents in modular multilevel converter based on average model," *2015 IEEE Energy Convers. Congr. Expo. ECCE 2015*, pp. 3522–3528, 2015.



Shuren Wang (S'18) received the first class B.Sc. and M.Sc. degrees in electrical engineering from Yangzhou University, Yangzhou, China, in 2013 and 2016, respectively.

He was with Bosch, TMR Energy, etc. He is currently working toward the Ph.D. degree in the University of Strathclyde, Glasgow, U.K. His research interests include energy conversion, power electronic converters, HVDC and integration of RES and ESS.

Grain P. Adam (M'12) received the B.Sc. and M.Sc. degrees (Hons.) from Sudan University for Science and Technology, in 1998 and 2002 respectively; and a PhD in Power Electronics from University of Strathclyde in 2007.

He is a researcher with University of Strathclyde in Glasgow, UK, since 2008. His research interests are fault tolerant voltage source converters for HVDC applications; modelling and control of HVDC transmission systems and multi-terminal HVDC networks; voltage source converter based FACTS devices; and grid integration issues of renewable energies.

Dr. Adam has authored and co-authored several technical reports, and over 100 journal and conference articles in the area of multilevel converters and HVDC systems, and grid integration of renewable power. Moreover, Dr. Adam has published two books in applications of power electronics in power systems and renewable energy. He is an active contributor to reviewing process for several IEEE and IET Transactions and Journals and conferences, and a full member of IEEE and IEEE Power Electronics Society.

Ahmed M. Massoud (SM'11) received the B.Sc. (first class honors) and M.Sc. degrees in Electrical Engineering from Alexandria University, Egypt, in 1997 and 2000, respectively, and the Ph.D. degree in Electrical Engineering from Heriot-Watt University, Edinburgh, U.K., in 2004.

He is currently a Professor at the Department of Electrical Engineering, College of Engineering, Qatar University. His research interests include power electronics, energy conversion, renewable energy, and power quality. He holds five U.S. patents. He published more than 100 journal papers in the fields of power electronics, energy conversion, and power quality.

Derrick Holliday has research interests in the areas of power electronics, electrical machines and drives. In 1995 he obtained the degree of PhD from Heriot Watt University and, since then, has held full-time academic posts at the Universities of Bristol and Strathclyde.

He is currently leading industrially funded research in the field of power electronics for HVDC applications, and is co-investigator on

research programmes in the fields of photovoltaic systems and the interface of renewable energy to HVDC systems. He has authored or co-authored over 70 academic journal and conference publications.

Barry W. Williams received the M.Eng.Sc. degree from the University of Adelaide, Australia, in 1978, and the Ph.D. degree from Cambridge University, Cambridge, U.K., in 1980.

After seven years as a Lecturer at Imperial College, University of London, U.K., he was appointed to a Chair of Electrical Engineering at Heriot-Watt University, Edinburgh, U.K, in 1986. He is currently a Professor at Strathclyde University, UK. His teaching covers power electronics (in which he has a free internet text) and drive systems. His research activities include power semiconductor modelling and protection, converter topologies, soft switching techniques, and application of ASICs and microprocessors to industrial electronics.