A novel current-feedback op-amp exploiting bootstrapping techniques

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The operation of the conventional current feedback operational amplifier (CFOA) is reviewed and its performance parameters used as benchmarks in the development of a new input stage architecture that provides a common-mode rejection ratio (CMRR) improvement of some 45 dB and offset voltage less than 10 mV.

Keywords: Analogue signal processing; Current-feedback op-amp; Current mode technique

1. Introduction

The conventional voltage op-amp (VOA) normally uses a long-tailed pair in its input stage (Gray and Meyer 1993). That gives rise to a high input-impedance at both the non-inverting and inverting input terminals. Moreover, it provides insensitivity to common-mode input signals. In contrast, the CFOA uses a complementary push-pull unity-gain voltage-follower in its input stage (Palumbo 1999). A major advantage of the CFOA, compared with its VOA counterpart, is its ability to provide a constant closed-loop bandwidth for closed-loop voltage gains up to typically 10. Another advantage is the very high slew-rate (SR), resulting from the class AB operation, making it ideal for video and telecommunication system applications (Alexander 1990). Unfortunately, the conventional CFOA has low CMRR, and a high DC voltage-offset due to the asymmetry in its architecture compared with the symmetric design of the VOA, which provide a much higher CMRR, and lower DC voltage-offset (Bowers 1988).

The structure of the conventional CFOA is reviewed to identify its performance limitations with respect to CMRR and SR. This analysis is used to develop a novel architecture for the CFOA with a CMRR and SR performance much closer to that obtained from a VOA, without degradation of the excellent SR performance of the conventional CFOA.

2. CFOA slew rate limitations

Consider the basic CFOA architecture, a schematic diagram of which is shown in figure 1. The SR for this configuration is sometimes quoted as being 'virtually

infinite', but definite limits do exist as the following brief discussion shows. D_1, D_2 in figure 1 model the base emitter junction of the input emitter followers. When a large differential voltage v_D is applied, in the direction shown, D_1 and Q_2 cut off and the equivalent circuit for evaluation of SR is shown in of figure 2.

Q_1 is supplied with a maximum step of base current, I_{bias}, that provides a maximum collector current i_{c1}, which can be estimated using transistor charge-control theory (Gray 1967)

$$i_{c1} \approx \beta_n I_{\text{bias}}\left[1 - \exp\left(-\frac{t}{\beta_n \tau_F}\right)\right] \tag{1}$$

In this equation β_n is the common emitter current gain of Q_1 at low frequencies and $\tau_F \approx 1/2\pi f_T$ is a transistor time-constant dependent on its geometry and doping levels.

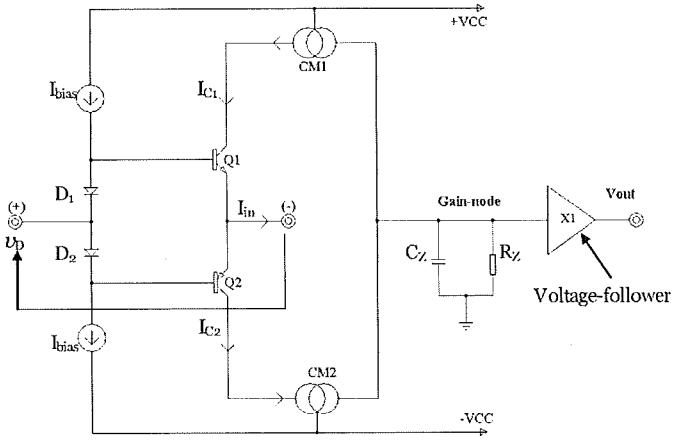

Figure 1. Effective CFOA schematic for slew-rate discussion.

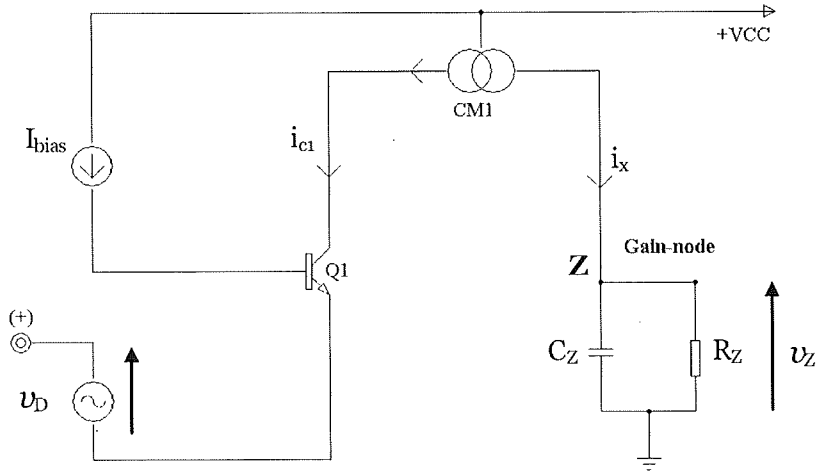

Figure 2. Reduced schematic from figure 1 for a large v_D.

The current i_{c1} is copied by the current-mirror CM1 and is equal to i_x. The equation for the voltage at node-Z, v_z, is

$$C_Z \frac{dv_Z}{dt} + \frac{v_Z}{R_Z} \approx \beta_n I_{\text{bias}} \left[1 - \exp\left(-\frac{t}{\beta_n \tau_F} \right) \right] \tag{2}$$

The maximum rate of change of v_z defines the SR and is obtained by setting $\tau_F = 0$. Then it follows from equation (2) that SR_+ is given by

$$SR_+ \approx \beta_n \frac{I_{\text{bias}}}{C_Z} \tag{3}$$

Since the input stage is top/bottom symmetrical, a similar result is achieved for a large negative value of v_D, in which case D_2 and Q_1 cut off. If for example $\beta_n I_{\text{bias}} = 2\,\text{mA}$ and $C_z = 1\,\text{pF}$, then $SR = 2000\,\text{V}/\mu\text{s}$.

The maximum value of the slew rate is obviously achieved with the maximum i_x and highest f_T, so any improvement over that obtained for the basic CFOA must take this into account. Ultimately the current available from the power supplies limits SR and this will, in turn, be dependent on supply-lead inductance and resistance.

3. Analysis of differential-mode operation of the CFOA

A simplified schematic of the standard CFOA architecture is shown in figure 3, where the non-inverting and inverting nodes are connected to a differential input signals. Under small signal condition the positive differential input signals is

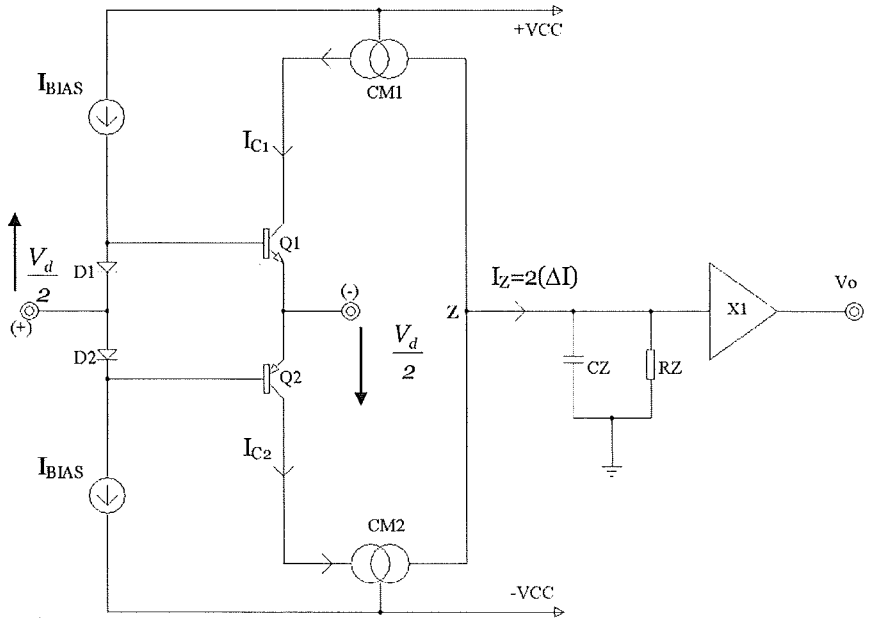

Figure 3. A standard CFOA, labelled to show differential-mode operation.

$V_2 = +Vd/2$ and the negative differential input signal is $V_1 = -(Vd/2)$. When the positive signal (V_2) is applied, the voltage at the base of Q_1 will rise, and the voltage at the emitter of Q_1 will fall due to the negative signal (V_1), increasing V_{BE1} of Q_1, resulting in an increase of I_{C1}. Similarly, V_{BE2} and I_{C2} of Q_2 will decrease. Under small-signal conditions the collector current, I_{C1}, of Q_1 will rise by ΔI and, similarly, the collector current, I_{C2}, of Q_2 will fall by ΔI (Vere-Hunt and Lidgey 1992).

These changes are then mirrored by CM1 and CM2 and appear at a high impedance gain-node (Z), where they subtract, giving a total signal current $I_Z = 2\Delta I$, resulting in an output voltage of $V_{\text{out}} = 2\Delta I.Z(z)$. Transistors Q_1 and Q_2 are configured as a class-AB complementary-pair stage. The operating point of these transistors is in the active region with the DC current set by the bias network comprising the two diodes D_1 and D_2 and the two current sources, I_{bias}.

Figure 4 shows a small-signal low-frequency differential mode half-circuit, which can be analysed to predict the circuit behaviour. The output current ($i_{C1} = i_{\text{out}(dm)}$) is given by

$$i_{C1} = g_m \cdot v_{BE1} + \frac{v_d}{2 \cdot r_{ce1}} \tag{4}$$

Since $v_{be} \approx v_d$, and r_{ce} is very high compared with $1/g_m$, equation (4) reduces to

$$g_{Tdm} \approx \frac{2i_{C1}}{v_d} = 2g_m \approx \frac{2I_{CQ}}{V_T} \tag{5}$$

where g_{Tdm} is the transconductance for differential-mode operation, g_m is the transconductance of one particular transistor in the input class-AB complementary-pair, I_{CQ} is the dc bias current, and V_T is the thermal-voltage. Thus, the differential-mode gain (A_{dm}) of the CFOA is

$$A_{dm} = \frac{2i_{C1} \cdot Z_z}{v_d} = g_{Tdm} \cdot Z_z \tag{6}$$

in which Z_Z is the (high) impedance at node Z.

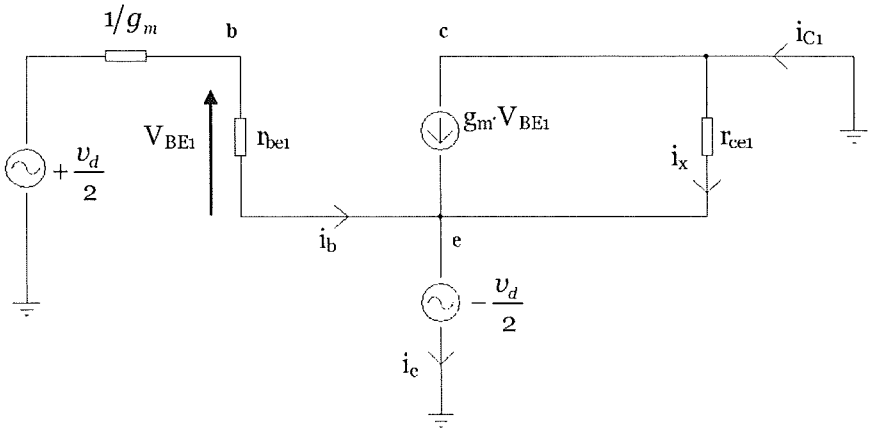

Figure 4. Small-signal differential-mode half circuit.

4. Analysis of common-mode operation of the CFOA

It has been established that the input stage of the CFOA is the main factor in determining the CMRR performance of the CFOA (Vere-Hunt and Lidgey 1991, Lidgey *et al.* 1998). A study of figure 5 has been made to investigate further the parameter that has a direct effect on common-mode operation, in order to understand fully the inner working of the CFOA, when a common-mode signal is applied to its input. It has been reported that a limitation to the CMRR performance is the finite output impedances of transistors in the input stage (Vere-Hunt and Lidgey 1991, Lidgey *et al.* 1998).

Refer to figure 6 which shows an appropriate equivalent circuit. Applying a positive common-mode input signal decreases the value of V_{CB} of Q_1, and as the Early voltage of this transistor is finite it results in a decrease in the collector current I_{C1} of Q_1 by an amount ΔI_{CM}.

Furthermore, the positive common-mode input voltage will cause the value of V_{CB} of Q_2 to rise and therefore the collector current I_{C2} of Q_2 to increase by the same amount (Lidgey *et al.* 1998). Hence, when the collector currents of Q_1 and Q_2 are mirrored by CM1 and CM2 to node (Z), the net current into the Z-node is

$$I_z \approx I_{C2} - I_{C1} = (\Delta I_{CM}) - (-\Delta I_{CM}) = 2\Delta I_{CM} \tag{7}$$

Since $I_{C1} \approx I_{E1}$, and $I_{C2} \approx I_{E2}$, then $I_{(-)} = I_{C2} - I_{C1}$, where $I_{(-)}$ is the inverting node input current.

Thus,

$$I_Z \approx I_{(-)} \approx I_{C2} - I_{C1} = 2\Delta I_{CM} \tag{8}$$

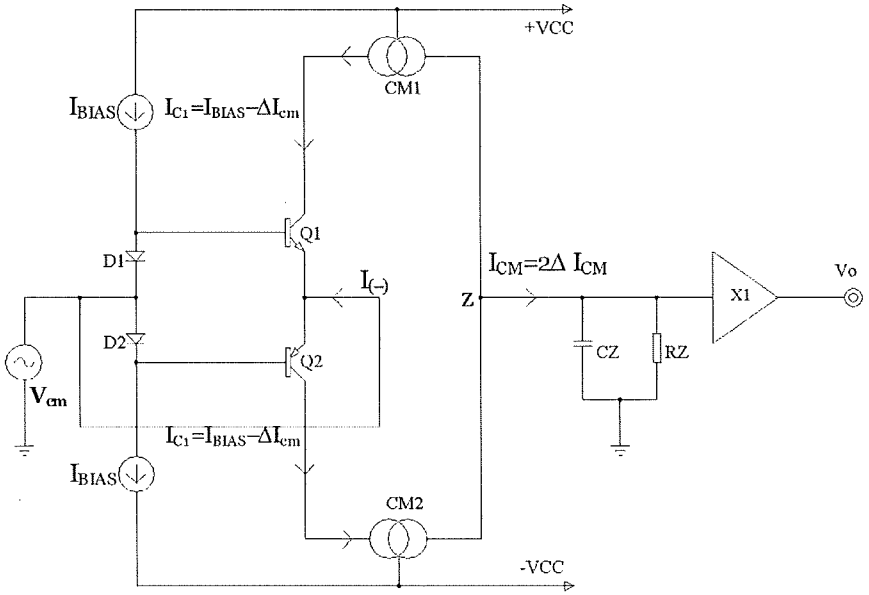

Figure 5. Effective circuit schematic of the CFOA with a common-mode input signal, V_{cm}.

Figure 6 shows the small-signal low frequency equivalent circuit for the input stage of the CFOA, driven by an input common-mode voltage signal. When a common-mode input voltage is applied to the circuit shown in figure 6, there is no signal voltage across the base-emitter terminals of Q_1, Q_2 two input transistors. Hence, both $g_{m1}V_{be1}$ and $g_{m2}V_{be2}$ signal current generators are inactive. The net result is that the circuit of figure 6 reduces to that shown in figure 7 and the output current from the coupled current-mirrors, i_{out}, is given by

$$i_{out(cm)} = -V_{cm} \cdot \left[\frac{I_Q}{V_{AN}} + \frac{1}{r_{\mu 1}} + \frac{I_Q}{V_{AP}} + \frac{1}{r_{\mu 2}}\right] \approx -V_{cm} \cdot \left[\frac{I_Q}{V_{AN}} + \frac{I_Q}{V_{AP}}\right] \tag{9}$$

The approximation sign is valid since $r_{\mu 1} \approx r_{\mu 2} >> r_{ce1} \approx r_{ce2} = r_{ce}$. Then the common-mode transconductance, g_{Tcm}, is

$$g_{Tcm} \approx \frac{i_{out(cm)}}{V_{cm}} = -2\left[\frac{I_Q}{V_{AN}} + \frac{I_Q}{V_{AP}}\right] \tag{10}$$

Thus, the r_{ce} values of Q_1, and Q_1 directly determine the A_{cm}.

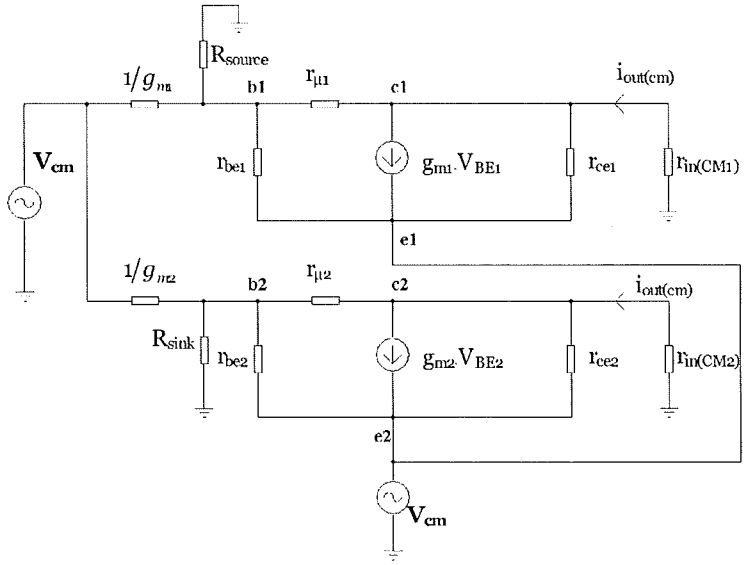

Figure 6. Small-signal low frequency equivalent circuit of the CFOA input stage for common-mode analysis, rin (CM1), rin (CM2) are negligible and neglected in the analysis.

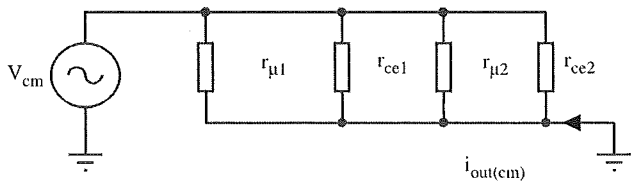

Figure 7. Reduced small-signal equivalent circuit for the Class AB bias voltage-follower.

It is essential at this stage to link g_{Tcm} and the common mode gain, A_{cm}, of the CFOA. Thus, (20) is given as

$$A_{cm} = \frac{i_{out(cm)} \cdot Z_z}{V_{cm}} = g_{Tcm} \cdot Z_z \tag{11}$$

5. Common-mode rejection ratio (CMRR)

The common-mode rejection ratio (CMRR), is defined as the ratio of the magnitude of the differential-gain, A_{dm}, to the magnitude of the common-mode gain, A_{dm}, (Comlinear Corporation 1988), thus:

$$\text{CMRR} = \left|\frac{A_{dm}}{A_{cm}}\right| \tag{12}$$

Substituting (6) and (11) into (12) gives,

$$\text{CMRR} = \left|\frac{i_{out(dm)} \cdot Z_z / V_d}{i_{out(cm)} \cdot Z_z / V_{cm}}\right| = \left|\frac{i_{out(dm)} / V_d}{i_{out(cm)} / V_{cm}}\right| = \left|\frac{g_{Tdm}}{g_{Tcm}}\right| \tag{13}$$

Equation (13) shows that the impedance at the Z point cancels out. Thus, having a higher, or lower, impedance gain-node (Z_Z) should not influence the value of the CMRR. By substituting (5), which defines g_{Tdm}, the transconductance for differential-mode operation, and (10), which defines g_{Tcm}, the transconductance for common-mode operation, into (13) we obtain,

$$\text{CMRR} = \left|\frac{g_{Tdm}}{g_{Tcm}}\right| = \left|\frac{2I_Q}{V_T} \cdot \frac{1}{2[(I_Q/V_{AN}) + (I_Q/V_{AP})]}\right| = \left|\frac{1}{V_T[(1/V_{AN}) + (1/)V_{AP}]}\right| \tag{14}$$

In the special case where $V_A = V_{AN} = V_{AP}$,

$$\text{CMRR} = \left|\frac{V_A}{2V_T}\right| \tag{15}$$

Table 1 summarizes the expected variations of CMRR, A_{dm} and A_{cm} with changing values of r_{ce1}, r_{ce2}, r_{e1}, and r_{e2}. To test this theoretical result, the circuit shown in figure 8 was simulated using SPICE. This was undertaken using Analog Devices XFCB device parameters, and the frequency responses of A_{dm}, A_{cm} and CMRR were obtained (see figure 9). The validity of equation (15) which has a simple a linear relationship between Early voltage and CMRR was confirmed, in simulation, by changing the Early voltages of the input devices and re-running the simulation for a range of Early voltage values. This is confirmed in figure 10, which is similar to figure 9, but with the Early voltages of the input devices quadrupled showing

Table 1. Effect of transister parameter variation on CMRR.

Increase parameter	CMRR	A_{dm}	A_{cm}
r_{ce1}, and r_{ce2}	Increases	No change	Decreases
r_{e1}, and r_{e2}	Decreases	Decreases	No change

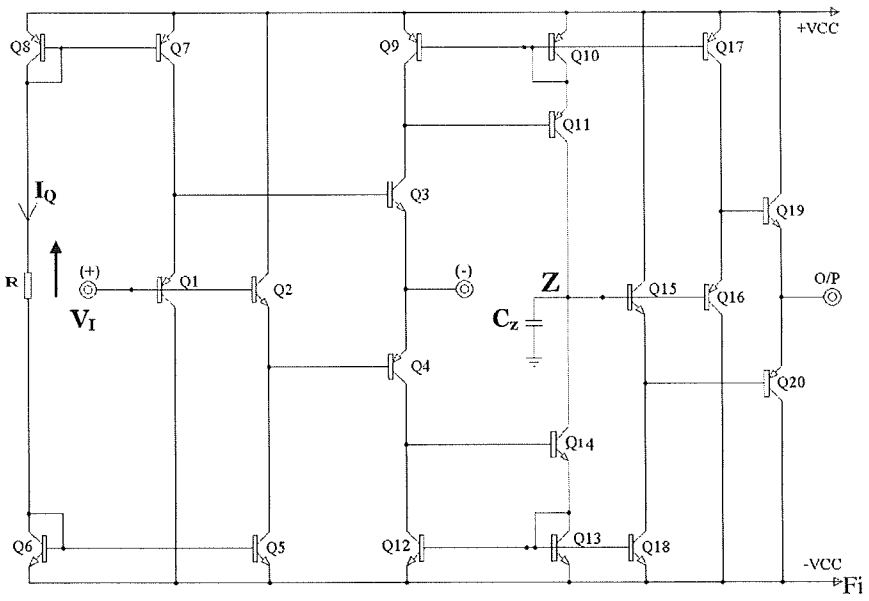

Figure 8. Circuit diagram of a basic CFOA (Franco 2002).

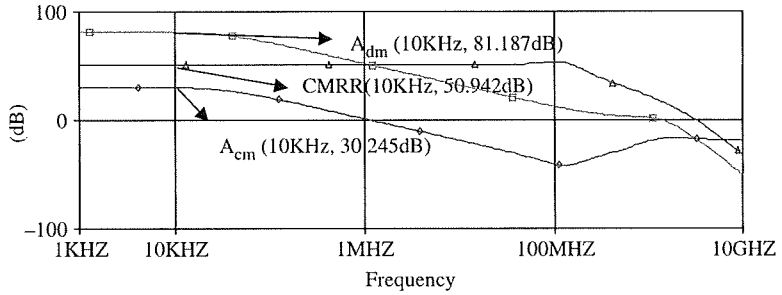

Figure 9. SPICE results for A_{dm}, A_{cm} and CMRR versus frequency for figure 8 using AD-XCFB process parameters.

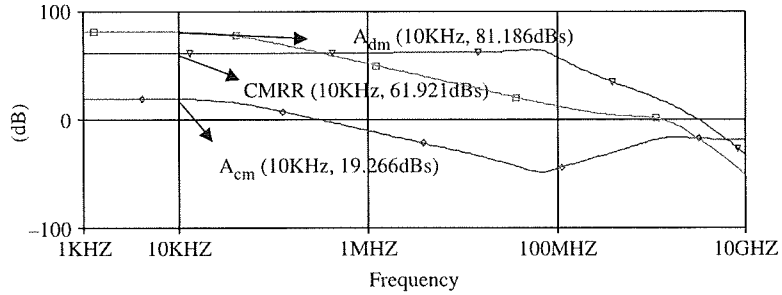

Figure 10. A_{dm}, A_{cm} and CMRR versus frequency, as in figure 9, except that V_A has been quadrupled for the input stage devices.

as anticipated (i) no change in A_d, (ii) a 12 dB reduction in A_c, and (iii) 12 dB increase in CMRR.

6. A CFOA using forward and reverse bootstrapping

The above analysis shows the dependence of A_{cm} and CMRR on Early voltage, and also indicates why the CMRR is limited to a modest 50 dB, which for many practical applications is too low. However, increasing the Early voltages of the input transistors to increase CMRR is not a practical option, and it is necessary to resort to circuit techniques, such as cascoding, to provide the required improvements in CMRR performance. Figure 11 shows an improved CFOA with a novel input stage that utilizes both forward and reverse boot-strapping to achieve the desired effect of increasing significantly the CMRR.

In figure 11, the buffered current mirrors, $(Q_7+Q_8+Q_9+Q_{19}+Q_{26})$ and $(Q_5+Q_6+Q_{10}+Q_{16}+Q_{33})$ are supplied with a common input current, I_Q, via the resistor R_Q. Since the action of the two buffered-mirrors is the same, only one is considered here, $(Q_7+Q_8+Q_9+Q_{19}+Q_{26})$, Q_{13}, with its base bias provided by the diode-connected transistors Q_{15} and Q_{17}, increases the output resistance of the Q_7 current source and in the same way Q_{14} cascodes Q_5 and increases the output resistance of Q_5. The input transistors Q_1 and Q_2 are cascoded by Q_{11} and Q_{12} respectively, and their base biases supplied via Q_{46}, Q_{47}, and Q_{48} and Q_{49}, respectively. Compared with the basic CFOA shown in figure 8, Q_3 is being cascoded with Q_{22} and Q_4 with Q_{24}. This provides 'forward' boot-strapping of the non-inverting input signal to the cascode transistors Q_3 and Q_4. Transistors Q_{22} is further cascoded by Q_{23} and, similarly, Q_{24} is further cascoded by Q_{25}.

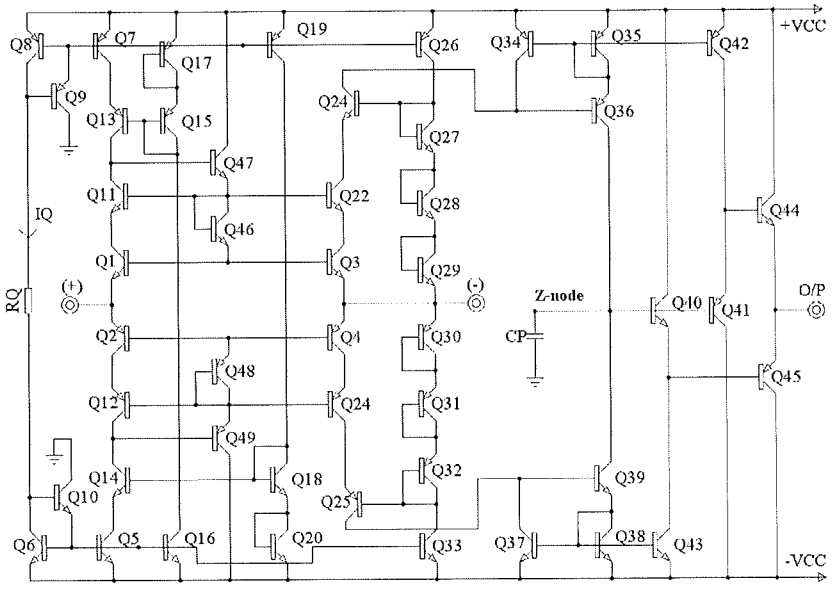

Figure 11. Circuit diagram of a CFOA using forward and reverse bootstrapping.

It should be noted that these 'second' cascoding devices are linked to the inverting-input terminal, and provide 'reverse' boot-strapping. The rest of the proposed new CFOA circuit is the same as shown in figure 8.

This novel input circuit topology gives higher gain-accuracy, and lower DC offset voltage and higher CMRR because the use of both casoding and boot-strapping results in a significant decrease in the common-mode currents within the input stage.

7. Circuit performance

SPICE was used to verify the operation and performance of the new CFOA and investigate how it compares with the conventional CFOA (Franco 2002). The total supply current was arranged to be below 2 mA, which is achieved with $I_Q = 0.2$ mA, and the power supply voltages were set to, $V_{CC} = \pm 5$ V. For comparative assessment the two CFOAs were simulated, namely (i) a conventional CFOA shown in figure 8, and (ii) the new CFOA shown in figure 11. Both CFOAs were simulated with the same technology parameters. Key performance data for the two CFOAs are shown in table 2 and figures 12 to 15. The simulated CMRR of the new CFOAs increases, dramatically, to over 96 dB, compared with value of just under 52 dB for the conventional CFOA. In addition, the input-referred offset-voltage in the new CFOA was 9.25 mV at unity closed-loop gain, approximately half that of the conventional CFOA input offset voltage of 20.6 mV at unity closed-loop gain. The decrease arises through the close matching of the base-emitter voltage of the same polarity.

The new CFOA input noise is reduced, dramatically to 40 nV/$\sqrt{\text{Hz}}$, from the conventional CFOA value of 67 nV/$\sqrt{\text{Hz}}$.

The bandwidth of both CFOAs, when configured as unity closed-loop voltage gain amplifiers, are almost the same, with a slight improvement in the new CFOA. A consequence of improving the CMRR and the input-referred offset-voltage is that the non-inverting input impedance is also increases, as shown in figure 16. The slew-rate of the new CFOA is increases to SR+ = 650.1 V/μs, and SR− = 454.2 V/μs,

Table 2. Comparison of the characteristics of the Conventional and the New CFOA.

	Conventional CFOA (Franco 2002) (Figure 8)	New CFOA (Figure 12)
CMRR	51.4 dB	96.7 dB
Bandwidth	55.7 MHz	59.9 MHz
Inverting input resistance (at 0 V d.c. input)	68.7 Ω	68.8 Ω
Non-inverting buffer input resistance (at 0 V d.c. input)	2.3 MΩ	3.4 MΩ
Noise (Voltage/$\sqrt{Hz}$)	66.8 nV	39.7 nV
Input offset voltage (at 0 V d.c. input)	20.6 mV	9.25 mV
Slew rates	SR+ = 569.6 V/μs SR− = 454.2 V/μs	SR+ = 650.1 V/μs SR− = 467.2 V/μs
Input dynamic range	−3 V, +3 V	−2V, +2V

in comparison with the conventional CFOA for which $SR+=569.6\,V/\mu s$, and $SR-=430.5\,V/\mu s$.

It is notable that the majority of the characteristics of the new CFOA are significantly better than those of the conventional CFOA, with the notable exception of the input dynamic range. The 'cost' of these improvements is the use of a greater

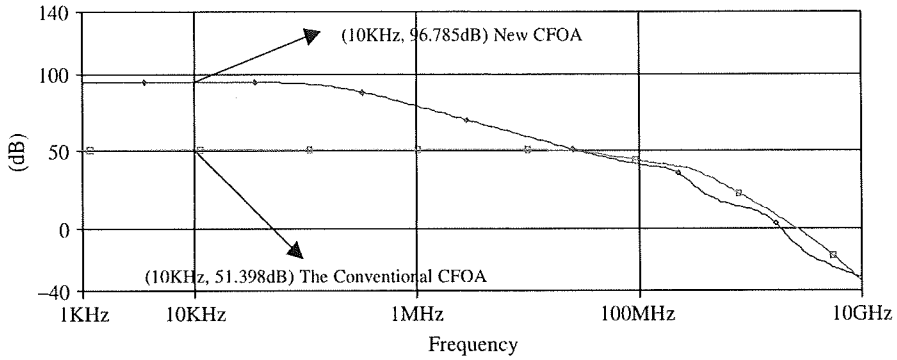

Figure 12. CMRR ~ Frequency.

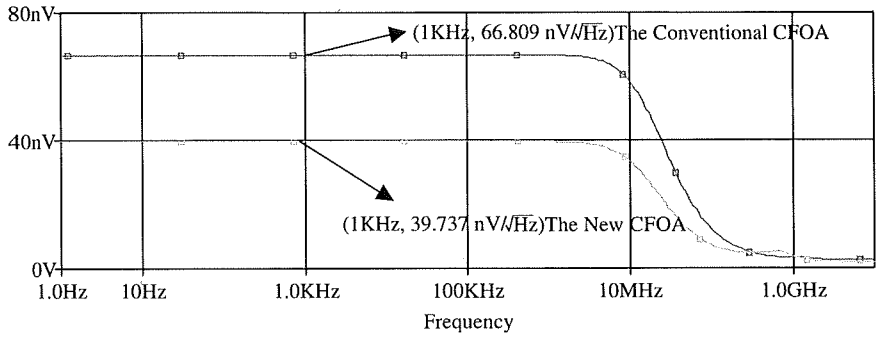

Figure 13. Noise measurement (Voltage ~ Frequency).

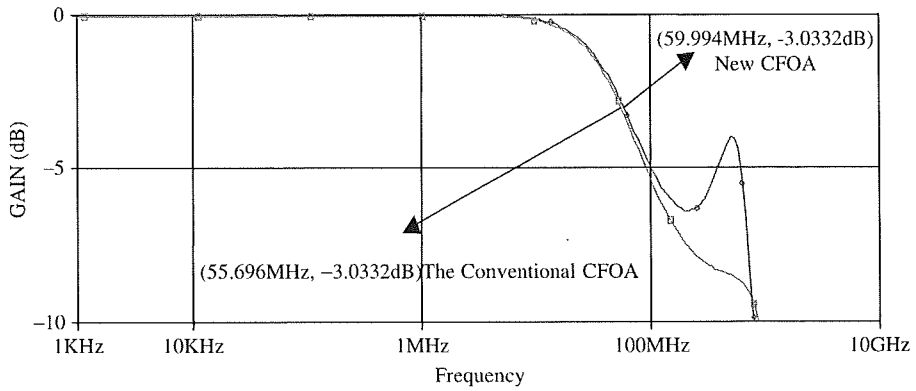

Figure 14. Frequency responses for unity closed-loop gain.

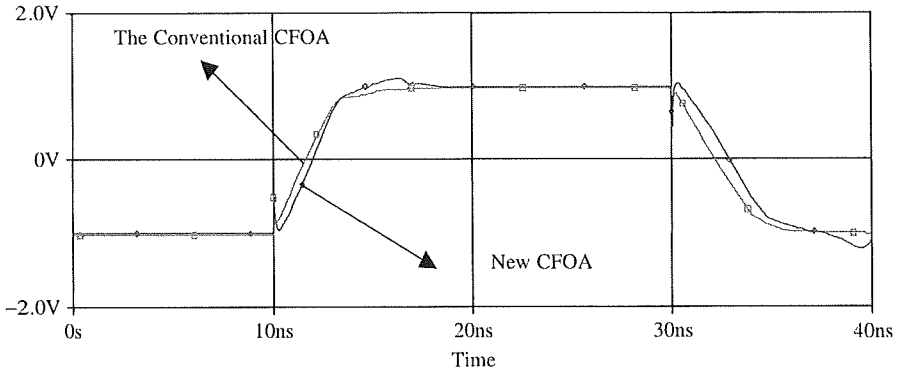

Figure 15. Transient response.

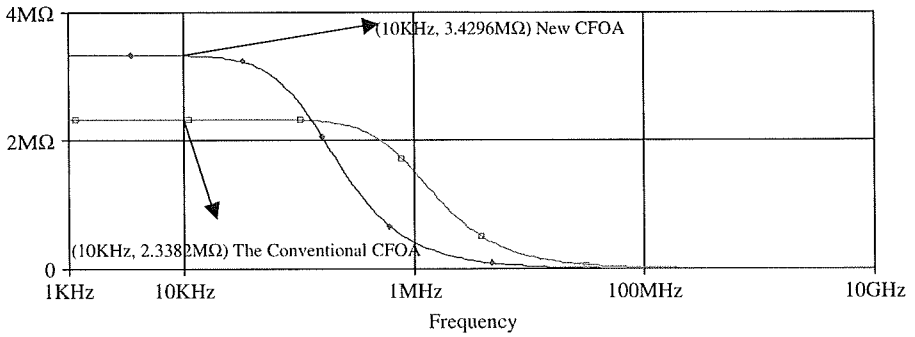

Figure 16. Input-impedance versus frequency for the CFOAs, each configured as a non-inverting unity-gain amplifier.

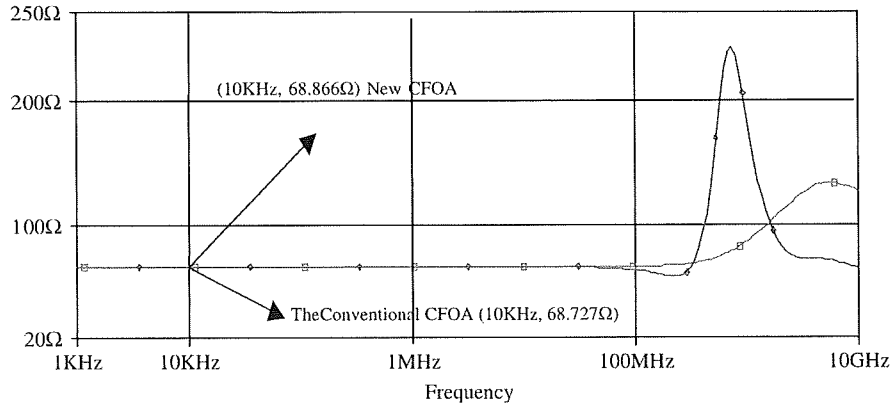

Figure 17. Input-impedance (inverting) ~ Frequency.

number of devices and poorer dynamic range and output swing capability, because of the stacking of the cascoded transistors.

8. Conclusions and future work

Analysis of the conventional CFOA has provided a deeper understanding of the internal operation of the circuit, and this work revealed that the main shortcomings of the CFOA are in the design of the input stage. This part of the amplifier is responsible for the poor CMRR performance compared with that of a voltage op-amp. Using the initial analysis of the conventional CFOA as a benchmark, a new CFOA, with improved DC and CMRR performance has been developed and presented here.

The design is based on combining two circuit techniques, namely forward and reverse bootstrapping. In comparison with the conventional CFOA, the CMRR increases by some 46 dB, and the input-referred offset-voltage has been reduced by a factor of two. Also, the majority of the other characteristics are better. However, the price paid for these improvements is a reduced output voltage swing for given rail voltages, because of vertical transistor stacking.

Clearly, the new CFOA does use more transistors but the performance advantages particularly in terms of CMRR improvement justify the increased complexity when this parameter is of paramount interest. The primary disadvantage is that moderately high power supply voltages are required. The authors are currently modifying the design to reduce the power supply requirements using folded-cascode type and other circuit techniques.

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