High Performance Circuit Techniques for Neural Front-End design in 65nm CMOS

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***Abstract*— Integrated low noise neural amplifiers become recently practical in CMOS technologies. In this paper, a low noise OTA technique has been proposed while keeping the power consumption constant. A capacitive feedback, ac coupled 46dB amplifier with high pass cutoff frequency close to the 90Hz has been achieved. The proposed amplifier has been implemented in 65nm CMOS technology; at room temperature circuit consumes 323uA current from 1.2V power supply. The circuit occupies 2627um^2 silicon area.**

Keywords—Neural amplifier, OTA, electrodes, Noise, Power.

I. INTRODUCTION

Neural recording enables us to understand human brain activity and its response to various deceases. Neural recording not only used to detect signals but also for stimulation understanding, brain stimulation is one of the effective ways of controlling intractable symptoms due to abnormal excessive neural activity in the brain [1]. Fig:1 shows the multi-channel neural recording system, it consists of a biological sensor and electrical system. Biological sensor converts neural signals into weak electrical signals through electrodes. These days multi-channel recording became very famous due to its fast and accurate estimation at several locations simultaneously. Electronics system is for small-scale amplification of the weak signals without adding significant noise, so front-end circuit is low noise amplifier (LNA) followed by a variable gain amplifier (VGA) as depicted in fig:1. VGA is to maintain the constant dynamic range irrespective of the biological signal strength so that ADC will not be overloaded.

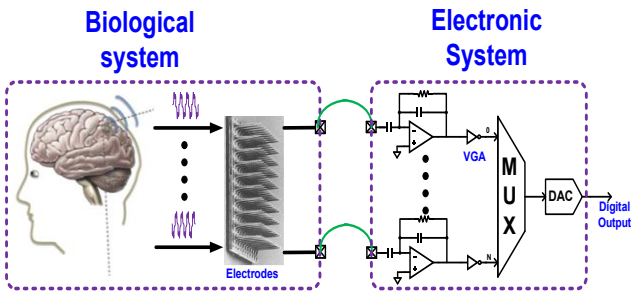

Fig. 1. Nueral recording system

Major challenges in the neural front end are minimizing the power dissipation, due to the heat problems and battery life to enable the wearable option. Neural signals are very weak in amplitude, which calls for high gain front end amplifier with very low input referred noise. Unfortunately minimizing the power dissipation while maintaining very low noise challenging [2]. From the bio-medical system point of view, apart from the thermal noise, there have been several other aggressors which could potentially degrade the performance. 60/50Hz power line interference, front-end flicker noise and high electrode offset voltage (EOV) due to the tissue interactions and electrodes very high impedance nature. EOV issue is quite annoying in practical usage which could frequently interrupt the continues monitoring. Under settling of large EOV, recorded signals in the same period are considered as contaminated and always rejected during post signal processing. Therefore, in order to facilitate robust recording EOV should be considered from the starting of the design. In the worst case offset due to the EOV could go as high as 300mV while using dry contact electrodes. To solve the EOV effects often ac coupled smart active electrodes have been becoming very popular, but expensive. Another solution could be using dc negative feedback to solve the offset, this often works well, but at the expense of power dissipation and minor input referred noise impact. Every DC cancellation loop will have high pass nature frequency response; hence it needs very large resistor and capacitor to enable the frequency of operation down to sub 1KHz frequency range. Apart-from offset, the power line interference and flicker noise is very challenging and still be a big obstacle for the fully integrated low power transceiver [3].

This paper has been organized as follows, section-II discusses existing amplifier design techniques, section-III explains the proposed inverter based low noise amplifier architecture and finally, section-IV summarizes the prototype simulation results and concludes the paper.

II. CHALLENGES IN NEURAL AMPLIFIER DESIGN

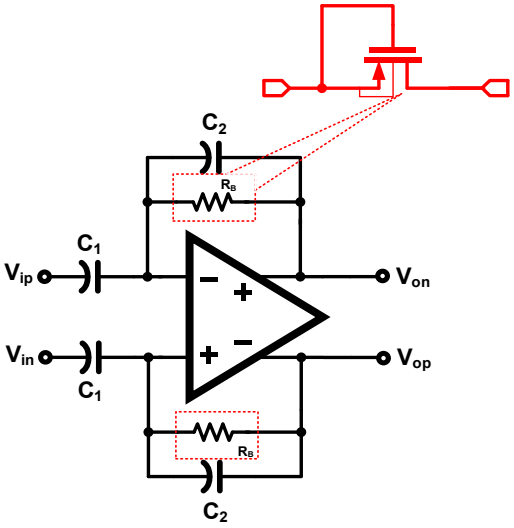

Fig. 2. Froendt-End LNA

There have been several popular front-end neural amplifiers, very popular one is 3-OTA instrumentation amplifier (IA) due to its high impedance, good Common Mode Rejection Ratio (CMRR) but lower power efficiency due to the usage of three OTAs and suffers from unacceptable input referred offset, hence not very suitable for integrated circuit especially in deep sub-micron technologies. From integrated challenges perspective, a single stage OTA with resistors or capacitors as feedback to set the closed-loop became very popular these days [4][5]. Fig. 2 shows the capacitive feedback neural amplifier and have inherent ac coupling at the input, where C_1, C_2 are the input and feedback capacitors respectively. Unfortunately, there is no DC negative feedback due to the capacitive feedback, hence need to provide a low impedance path at low frequency, often a resistor will be used in parallel with the feedback capacitor. The closed-loop transfer function can be expressed as the following.

$$\frac{V_0(S)}{V_i(S)} = \frac{C_1}{C_2}\left(1 - \frac{1}{A\frac{C_2}{C_1+C_2}}\right)\left(\frac{SC_2R_B}{1+SC_2R_B}\right)\left(\frac{1}{1+\frac{S}{W_u}}\right) \qquad (1)$$

Where W_U is the unity gain bandwidth of the OTA

Expression (1) revels that there is a high pass corner frequency in the response, means it must be much lower than the signal frequency of interest, for the present application it should be less than 100Hz, so often pseudo resistor will be the common choice which enables the usage of sub-threshold transistors to implement >10GΩ resistance [6]. Though there is less progress on the amplifier feedback nature (capacitive/resistive feedback), there have been tremendous improvements in the OTA architecture itself. Mainly the input referred noise depends on the OTA noise, hence for designing for low noise meeting stringent power budget is often a big problem in OTA design. Traditional OTA designs are based on the differential pair with active loads. In principle, there are telescopic, folded cascode, two stage and current mirror OTA architectures available in the literature to achieve higher gain as well better noise. Fig. 3 shows the telescopic Cascode amplifier with the Common mode feedback (CMFB) loop and there have been several derivatives implementing the active loads to achieve the heist possible gain despite the poor intrinsic device gain especially in deep submicron technologies.

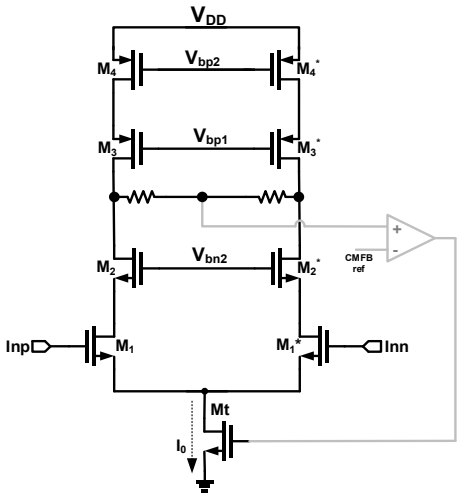

Fig. 3. Traditonal Cascode OTA

The most important figure of merit, which describes the power, noise trade-off is Noise efficiency factor (NEF) proposed in [7] expressed in (2).

$$NEF = \overline{V_{nrms}}\sqrt{\frac{2I_{bias}}{\Pi.V_T.4KT.BW}} \qquad (2)$$

Where $\overline{V_{nrms}}$ is rms thermal noise of the amplifier, BW is 3-dB closed loop bandwidth and Ibias is the total current consumption. For a single BJT device this factor is unity, hence higher the NEF means higher noise or more power consumption. The input referred noise of the of the OTA (fig. 3) can be expressed as follows.

$$\overline{V_{nrms}} = 4KT\gamma\frac{1}{g_{m1}}\left(1 + \frac{g_{m4}}{g_{m1}}\right) \qquad (3)$$

where g_m is the trans-conductance of the respective transistors, considered only the differential pair noise (M_1) and pmos current source load only (M_4) , because cascode transistors (M_2,M_3) noise is very less due to their large degeneration resistance. To maintain the output common voltage, a CMFB loop is very common, which senses the output common mode voltage with resistive network and corrects the tail current source with another OTA. This architecture has two problems, one is resistive network load the OTA hence gain will decrease unless otherwise these resistors are much larger than output impedance, which is very unlikely due to size constraint. There have been several switch capacitor CMFB techniques in the literature but unfortunately it requires a clock from the system [10][11], hence it is not very efficient from energy efficiency point of view. OTA used in CMFB loop also requires extra biasing power.

III. PROPOSEDN NEURAL AMPLIFIER

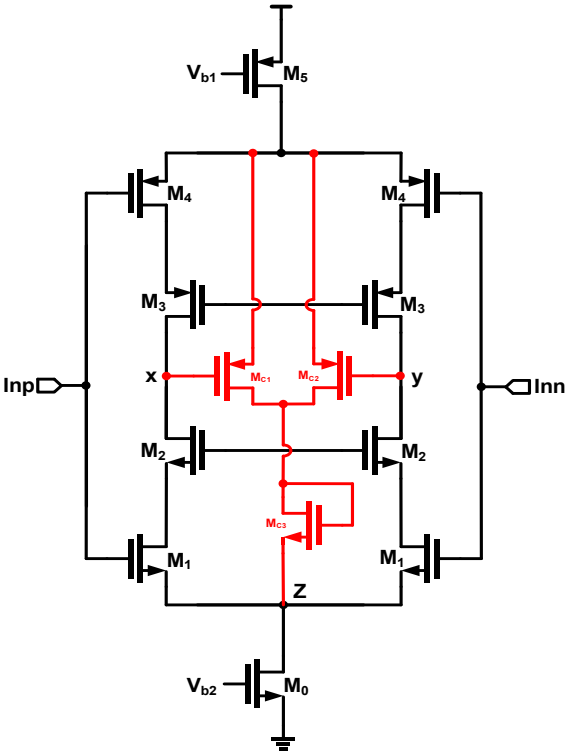

Fig. 4. Proposed low noise complimentary Cascode OTA

Input referred noise is strongly depends on the g_m of the OTA [8][9]. All the proposed architectures are relaying on only nmos or pmos differential pair, which will produce moderate gm. The motivation for the present proposal is converting the noise generating transistor also a signal generator (M_4 in fig. 3) so that noise will decrease while reusing the existing bias current to decrease the power dissipation. in the present paper, we used complimentary differential pair as an input stage with a cascode loads. Fig:4 shows proposed amplifier, M_1,M_4 devices acts as input devices to contribute gm, whereas M_2,M_3 acts as cascode loads. M_5, M_0 devices acts as bias current sources driven from bandgap reference, without these tail devices this structure like an inverter (class AB stage), with lot of distortion. Gain of the amplifier given by (4) and input referred noise is given by (5)

$$gain = \frac{g_{m1}+g_{m4}}{\frac{g_{01}g_{02}}{g_{m1}}+\frac{g_{03}g_{04}}{g_{m4}}} \qquad (4)$$

$$noise = \frac{4KTYg_{m1}+4KTYg_{m2}}{(g_{m1}+g_{m2})^2} \qquad (5)$$

(5) revels that input referred noise is divided by $g_{m1}+g_{m2}$ rather only one g_m as in case of the previously existing technique. To solve the CMFB problems existing in circuit shown in fig. 3, a novel simple CMFB has been used. M_{C1}, M_{C2} acts as common mode sensors and produce common mode current and inject current into tail node Z, such that if output common mode voltage decreases, injected current into the node Z and finally restores the common mode voltage. M_{C1}, M_{C2} doesn't respond for differential mode voltage because they will produce opposite phase current for this and they will circuit between these transistors hence injected current into node Z is zero. Another advantage of this CMFB is it doesn't load the amplifier due to the fact that it driving M_{c1}, M_{c2} gates hence no reduction in the OTA Gain and it doesn't require any OTA to realize negative feedback hence no additional power consumption also [10]. Another advantage is there is no need for frequency compensation and hence lot of area saving with bulky compensation capacitor since there is no OTA based loop and faster common mode step response.

IV. PROTOTYPE SIMULATION RESULTS

A prototype has been developed to demonstrate the noise reduction capability of the proposed technique in 65nm CMOS technology. Implemented the inverting amplifier (fig:2) with the proposed amplifier and conventional cascode amplifier to compare the performance improvement. The open loop-gain of the amplifier 68dB. Selected feedback capacitors values from the silicon area constraint are C_1=10pF and C_2=50fF. Higher the feedback capacitor (C_2) better the high pass corner frequency but higher C_2 also requires higher C_1 for a given closed loop gain, so we minimized the C_2 value but by increasing the feedback resistor to achieve the <100Hz high pass cutoff frequency. The simulated pseudo feedback resistance (R_b) is 35GΩ, this value limited by the fact that leakage current of the sub-threshold device and realizing very high beyond this will effect the linearity and distortion of the entire transceiver.

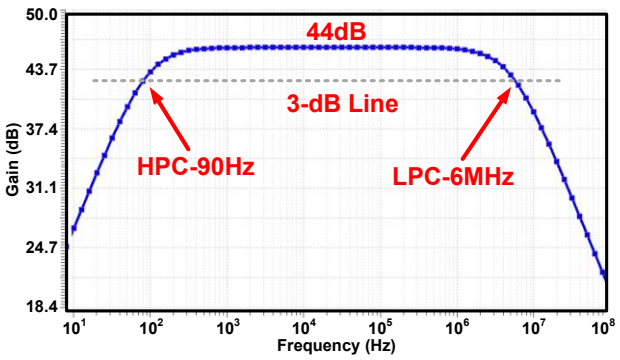

Fig. 5. Closed loop gain of the amplifier

Fig. 5 depicts the closed loop gain of the circuit, achieves 44dB mid-band gain, 90Hz high pass cutoff frequency (HPC) and 6MHz low pass cutoff frequency (LPC). For all kind of bio-logical signals sensing this frequency response is sufficient. Fig. 6 shows the simulated input referred noise of the amplifier, spot noise at 100KHz is -150dB and integrated RMS noise over the full frequency range is 0.97μV. As explained in the previous section, compared to the existing techniques (like cascode) the proposed one will

have 6dB less noise from theory and results in fig. 6 shows 4.7dB reduction.

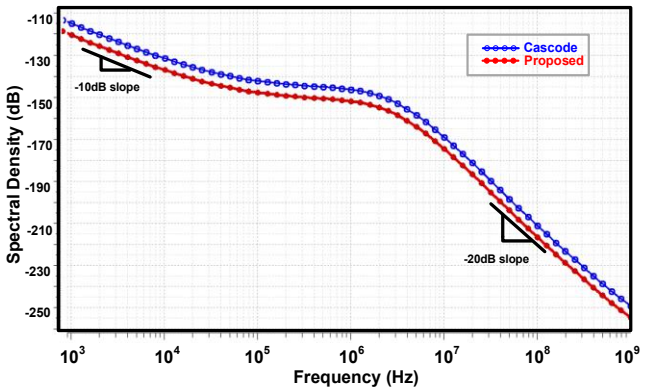

Fig. 6. Closed loop gain of the amplifier

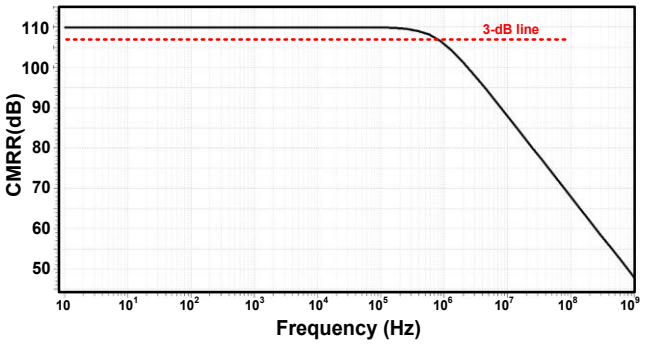

Fig. 7. Simulated CMRR

Fig. 7 shows the simulated CMRR under typical corner and 65^0 temperature, around 100dB CMRR up to 1MHz frequency. Since CMRR is heavily depends on the matching of the transistors, monte carlo simulations are necessary to bound minimum and maximum values, hence a 500-point monte Carlo simulation has been run to validate CMRR statistical properties. Fig. 8 depicts the CMRR histogram with a mean CMRR of 114dB and 3.5dB standard deviation. Fig. 9 shows the layout of the implemented circuit, occupies $2627um^2$ silicon area.

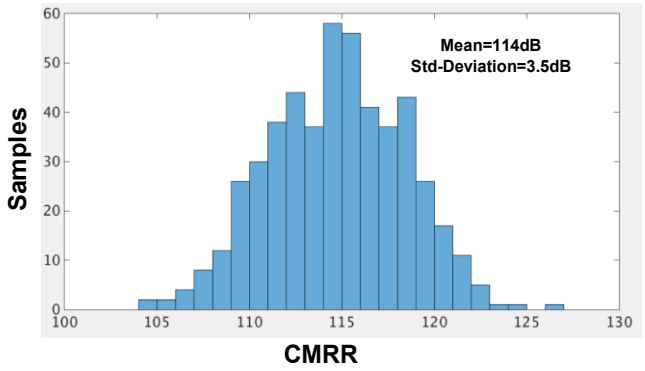

Fig. 8. Monte Carlo Results for CMRR

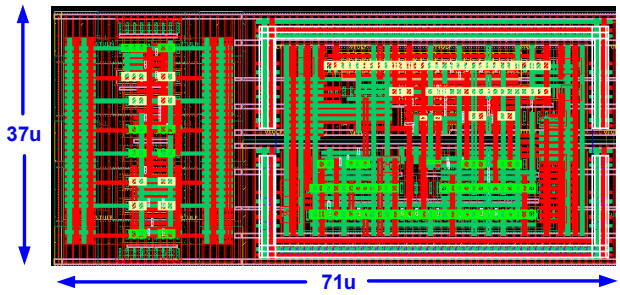

Fig. 9. Layout of the Proposed Circuit

V. Conclusion

In this paper, a low noise neural amplifier design technique has been proposed and implemented. Simulations shows 4.5dB noise spectral density reduction, circuit achieves 44dB mid-band gain while consuming 323µA current from 1.2V power supply voltage.

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