Technique for increasing the output impedance of CMOS regulated cascode circuits.

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Abstract A technique is proposed for the design of a modified CMOS regulated cascode having an output impedance significantly greater than that of a conventional regulated cascode. Simulation results for an illustrative design, operating at 10μA from a 1V supply, show an increase in output resistance from 636MΩ and output bandwidth of 55kHz for a conventional circuit to 6.68GΩ and 389kHz, respectively, for the proposed design.

Keywords Regulated cascode. Output- impedance. Band-width improvement. Current Mirror.

1. Introduction

According to one source [1] the MOSFET 'Regulated Cascode circuit (REC)' was first proposed in 1979 [2], though the configuration might well have been used earlier by bipolar circuit designers as a development of the well-known Wilson current mirror.

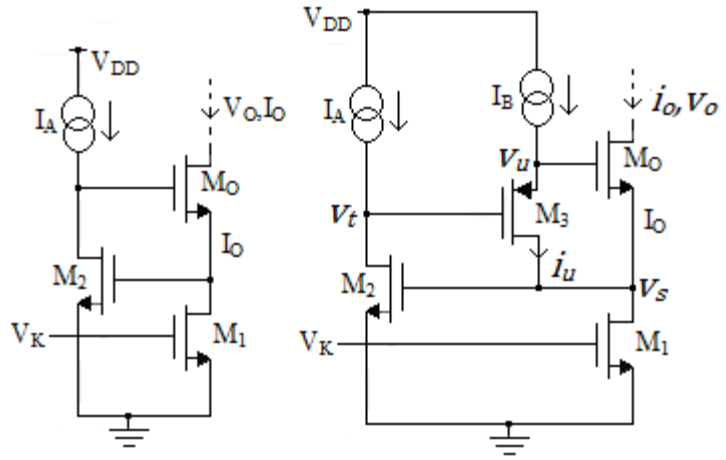
Over the years the RGC has been extensively used when a high output resistance is required, e.g., in the design of accurate current mirrors [3-5], current source [6-7] and neural stimulators [8]. However, the essential structure of the configuration has remained unchanged.

Here a 'modified RGC (MRGC)' is proposed and shown, theoretically and by simulation to be capable of producing an output-impedance significantly higher than that of the established design. In an illustrative example, a low power circuit intended for a biomedical

sensing application, the output impedance is shown to be increased by a factor of ten and the -3dB bandwidth of the output impedance by a factor of 7.

2. Circuit Description.

The circuit configuration of a basic conventional RGC, with which the modified circuit is being compared, is shown in Fig.1a.



(a) (b)

Fig.1 Conventional and proposed modified regulated cascode. (a) Conventional regulated cascode (RGC). (b) Proposed Modified Regulated Cascode (MRGC).

The MRGC in Fig.1b, differs from the RGC in that a source follower, comprising M_3 and its current source load I_B, links the drain of the common-source amplifying transistor M_2 to the gate of the output cascode transistor M_o. It will be seen from what follows that the current fed back from the drain of M_3 to the source of M_o can have a beneficial effect on the output impedance at the drain of M_o

In the analysis outlined below: r_{on}, g_{on}, and g_{mn} are respectively, the drain-source resistance, drain-source conductance and trans-conductance of transistor M_n (n=0,1.2,3); i_o, i_u, v_s, v_t, v_u, indicated in Fig.1b are the small-signal low-frequency changes in drain currents and nodal voltages that accompany an output voltage change, v_o .

Consider, first, the effect of M_3 on the output resistance, that is, the output impedance at those low frequencies where capacitive currents can be ignored in the analysis.

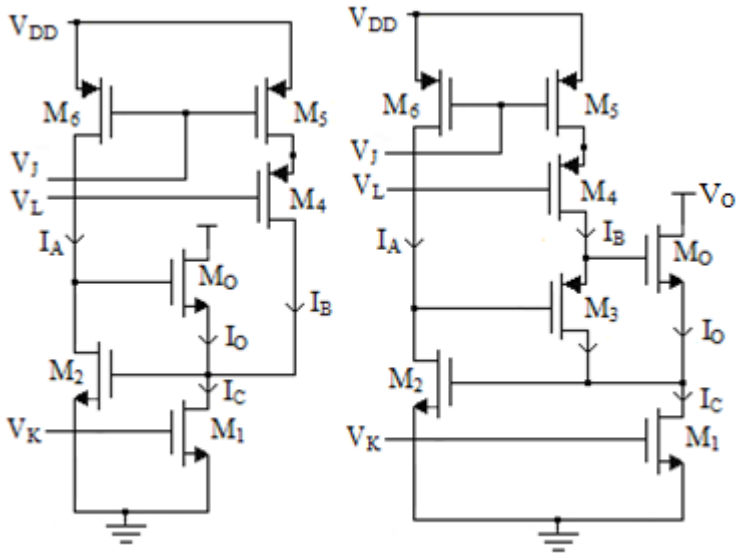
By inspection of Fig.1b,

$$v_s=(i_o+i_u)r_{o1} \quad (1)$$

$$v_t=-g_{m2}r_x v_s \quad (2)$$

$$v_u=Gv_t=-Gg_{m2}r_x v_s \quad (3)$$

$$i_u=-v_u/r_y \quad (4)$$



(a) (b)

Fig. 2 Conventional and proposed modified regulated cascode used in simulation tests. V_{DD}=1V, V_J, V_K and V_L are DC bias voltages obtained from current mirror biasing circuits; I_A=10μA, I_B=5μA, I_C=15μA, I_O=10μA. (a) Version of Fig.1a used in simulation tests on output impedance. (b) Version of Fig.1b used in simulation tests on output impedance.

In the equations: $r_x=r_{02}$ in parallel with the output resistance of current source I_A; r_y=output resistance of current source I_B; and , G is the voltage gain of the source follower. From (1) to (4), it is easily shown that

$$v_s=i_o r_{o1}/[1- Gg_{m2}r_x r_{o1}/r_y] \quad (5)$$

But for M_o,

$$i_o=g_{mo}(v_u-v_s)+g_{oo}(v_o-v_s) \quad (6)$$

Substituting for v_u from (3) and v_s from (5) it follows from (6) that the output resistance, R_{ob} for Fig.1b is,

$$R_{ob}=(v_o/i_o)\cong g_{oo}r_{oo}g_{m2}r_x r_{o1}/[(1/G)-(g_{m2}r_x r_{o1}/r_y)] \quad (7)$$

The derivation of (7) from (6) makes use of the sensible engineering approximation $Gg_{mo}g_{m2}r_x >> (g_{mo}+g_{oo})$. The output resistance, R_{oa}, for Fig.1a can be obtained from (7) by substituting $G=1$, $r_y=\infty$. Thus,

$$R_{oa} \cong g_{oo}r_{oo}g_{m2}r_x r_{o1} \quad (8)$$

This is an approximation given in the literature [9]. Thus, R_{ob} is greater than R_{oa} by a factor λ, where,

$$\lambda=(R_{ob}/R_{oa})=1/[(1/G)-(g_{m2}r_x r_{o1}/r_y)] \quad (9)$$

Straightforward circuit analysis yields,

$$G=(v_u/v_t)=[g_{m3}-(g_{o3}/g_{m2}r_x)]/[g_{m3}+g_{o3}+g_{oy}] \quad (10)$$

As G can be close to unity a safe design guide ensuring R_{ob}, and hence λ, is positive is,

$$r_y \geq g_{m2}r_x r_{o1} \quad (11)$$

The maximum value of λ is achieved for a choice of r_y satisfying the equality condition in (11) providing adverse parameter variations are taken into account.

Consider, next the effect of M_3 on the output impedance bandwidth. An appeal to the method of 'Zero value time-constant analysis' [10] using order-of-magnitude parameter values indicates that the bandwidth, f_{oa}, for Fig.1a is governed principally by the dominant time-constant $R_{oa}(C_{gdo}+C_{dbo})$, C_{gdo} and C_{dbo} being, respectively, the drain and gate-drain-substrate capacitance of M_o. The bandwidth, f_{ob}, of Fig.1b can exceed f_{oa} because, although

R_{ob}>R_{oa} , in this case current in C_{gdo} is returned to the source of M_o, so viewed from the drain of M_o, C_{gdo} appears smaller.

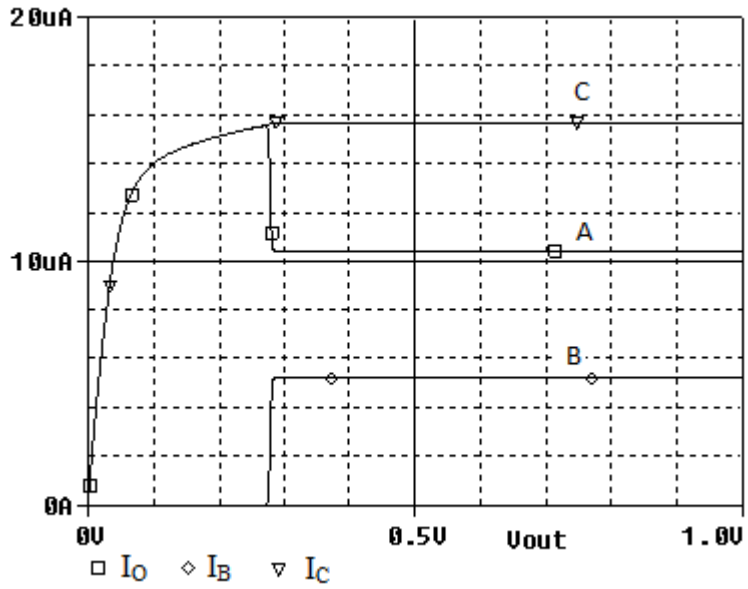


Fig. 3 Current curves I_O, I_B, I_C as a function of V_O for the circuit of Fig.2b.

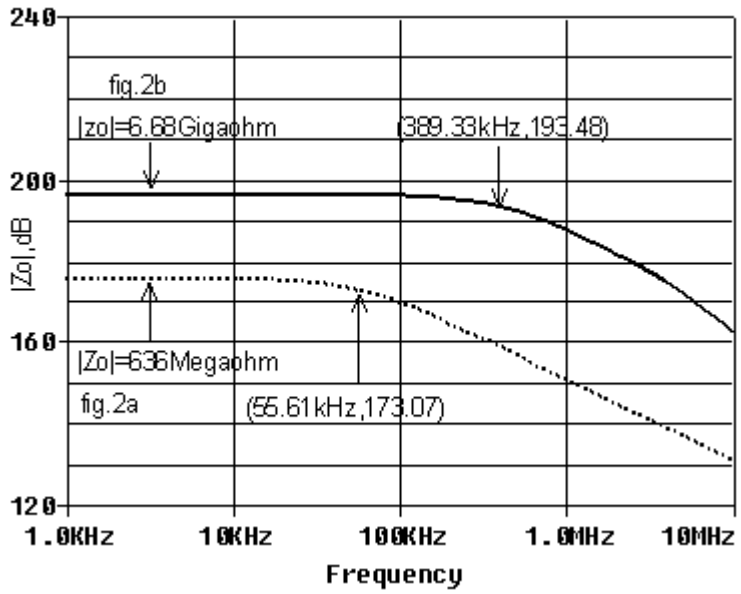


Fig. 4 Frequency response of the |Output impedance| in dB and Ohms for the RGC (dotted curve) and the proposed MRGC (solid curve).The dB reference level is 1Ω.

3. Results Figs. 2a, 2b show the versions of Figs.1a, 1b used in simulation tests, Fig.2a being configured to operate with the same DC operating conditions for M_O and M_1. All mosfets have the same channel length, L, of 0.35μm, except for M_4 which has L=1μm. The gate width, W, for each correspondingly subscripted MOSFET is as follows: W_1=15μm,W_2=W_3=W_6=10μm, W_4=7.5μm,W_5=6μm. Curves A, B and C of Fig.3 display, respectively, the output current I_O and the bias currents I_B and I_C of Fig.2b for the output voltage range 0 to 1V. As V_O increases from 0V, I_O is initially greater than the design target because M_4 and M_5 are off, and hence I_B=0, until V_O approaches 0.3V. For $V_O \geq 0.3V$, I_O appears to be constant. This is because its slope which defines the output resistance is not evident on the vertical scale used to show the circuit currents.

Table 1 Performance comparison of the relevant parameters of the MRGC with RGC.

Configuration	Minimum output voltage	Output impedance	Bandwidth
Regulated cascode (Fig.2a)	0.3V	636MΩ	55.6kHz
Proposed circuit (Fig.2b)	0.3V	6.68GΩ	389.33kHz

Cadence PSpice test results, for Figs.2a, 2b in Fig.4 show that the proposed MRGC exhibits a ten-fold increase in output resistance and a seven-fold increase in bandwidth when compared with the conventional RGC. A test for the stability of the negative feedback loop encompassing the source of M_O and the gates of M_3 and M_O showed stability with a phase margin of 47º. Finally, table 1 compares the performance of the relevant parameters of the MRGC in Fig.2b with the RGC in Fig.2a.

Conclusion A modified CMOS regulated cascode design (MRGC) has been proposed and shown, both theoretically and by simulation tests, to be capable of offering a significant improvement in output impedance compared with that of a conventional regulated cascode(RGC). This improvement occurs because the incorporation of a source follower in

the feedback loop between the amplifier and the output transistor gives rise to additional, calculable, negative feedback.

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