A compact high gain opamp for Bio-medical applications in 45nm CMOS technology

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***Abstract*—In this paper a low opamp compensation technique suitable for the bio-medical application has been proposed and intuitive explained the existing compensation techniques. The Present technique relies on the passive damping factor control rather power hungry damping. Implemented in 45nm CMOS technology and simulated with Spectre. Simulation results shows that 100dB dc gain, well compensated 25MHz bandwidth opamp while driving a 1pF capacitive load. Draws with 12uW power consumption from 1V supply and occupying 0.004875mm^2 silicon area.**

Keywords—Opamp, compensation, miller, capacitor, pole, PSRR, Noise, phase margin.

I. Introduction

There has been a significant amount of work on bio-medical transceivers in the recent days [1]. Mainly to sense Electrocardiogram (ECG) signals and brain waves to diagnosis or study the disease. The future plan of sensing is through implantable or wearable chip for the sake of flexibility and safety. Many existing biomedical implantable devices operate in 13.56MHz industrial, scientific and medical (ISM) frequency band. To enable higher battery efficiency, they have to be very compact for low cost as well very low active and standby power consumption. A typical bio-medical transceiver chain will have 60-70dB for the sake of detecting 0.1-10uV week signals. Always high gain open loop amplifier will have a problem of dc offset amplification. Having more than 10uV offset would saturate the transceiver. So to cancel offset either we need a slow DC-cancellation loop or low bandwidth ac coupling system [1]. Either of the two methods needs high gain, low noise and low power operational amplifiers. Modern fine CMOS technology was limited by the single stage gain, so three stage or multistage amplifier is requirement to meet the requirements. There has been a lot of research activity on low noise amplifiers, so the remaining biggest problem is a low area and unfortunately, three stage high gain opamp needs complicated frequency compensation strategy requires two compensation capacitors with bandwidth compromise. There has been a little research on high gain opamp without complicated frequency compensation. Rest of the paper organizes as follows. Section II describes the review of the existing compensation techniques, section III explains proposed compensation technique and design guidelines and IV describes simulation results of the test circuit.

II. Low-Voltage High Gain Opamp Compensation

Short channel length effect in CMOS technology causes poor transistor output impedance, which degrades intrinsic gain. In 45nm technology, transistor with an aspect ratio ($\frac{W}{L}$) of 3.9um/0.5um with 500um of bias current has just 17dB intrinsic gain. Decreasing bias current from 500uA to 2uA, shown 10dB of gain increase, but with 2uA bias opamp noise will be unacceptable for bio-medical applications. To increase the gain cascoding each transistor or cascading multi-stages are well-known approaches. But with the available low supply voltage restricted by technology (due to maximum electric field limitation) makes it difficult using cascode schemes and does not allow their use in the output stage. For the required gain of 70-80dB, cascading 3 stages or even more depends on the requirements.

For stable and healthy step response, closed loop system transfer should have Left half poles (LHP) and they need to be closer to real axis to have less ringing. A typical 3-stage opamp will have 3 poles, which needs to be separated by at least 3 x times in the frequency to have 60^0 phase margin. Several multi-stage frequency compensation techniques have been proposed, such as nested miller compensation (NMC) [2], modified nested miller compensation (NMCNR) [3], nested feedforward compensation (NGCC) [4] and damping factor control frequency compensation (DFCFC) [5]. Fig:1 (a) shows nested miller compensation. A 3-stage NMC opamp contains two miller capacitors from the output of each stage to the final stage output, forming two negative feedback loops. The transfer function of the fig:1 (a) can be derived as follows.

$$\frac{V_{o(s)}}{V_{in}(s)} = \frac{1}{\left(1 + S\frac{C_{m1}}{g_{m1}}\right)\left(1 + S\frac{C_{m2}}{g_{m2}} + S^2\frac{C_{m2}C_L}{g_{m2}g_{m3}}\right)} \quad (1)$$

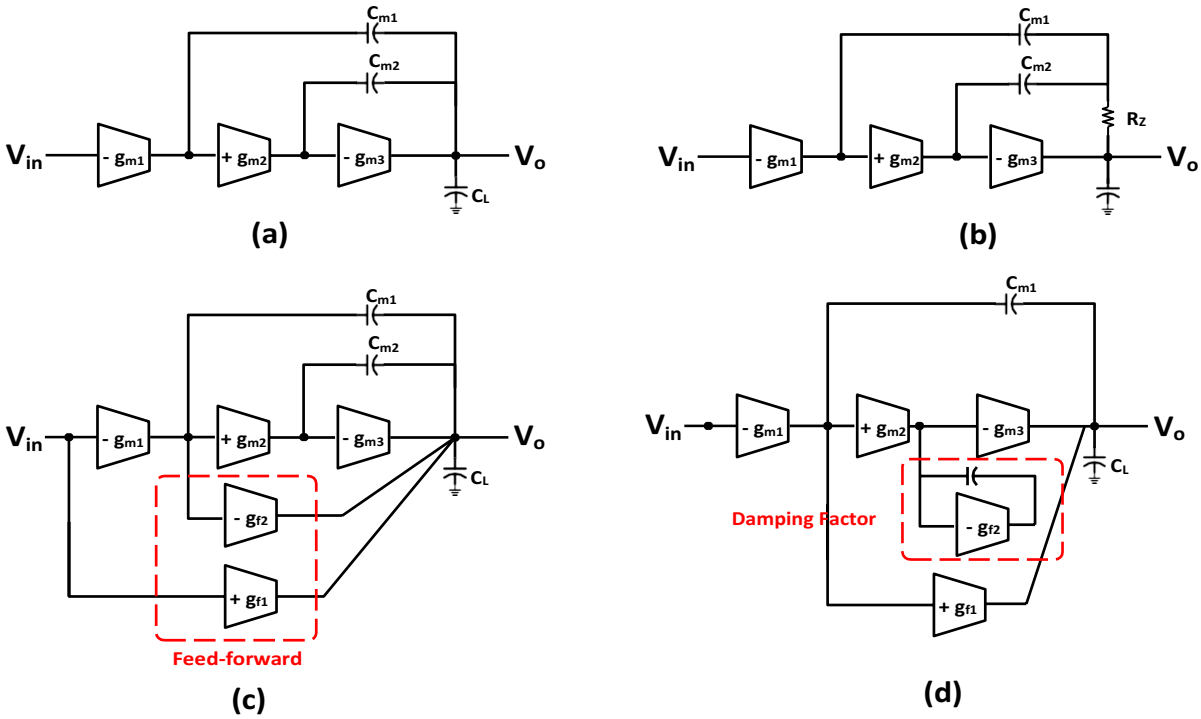

Fig. 1. Existing compensation techniques (a) NMC (b) NMCMR (c) NGCC (d) DFCFC

From equation (1), for stable step response we can derive the relation between compensation capacitors and load capacitor as follows

$$C_{m1} = 4\left(\frac{g_{m1}}{g_{m3}}\right)C_L \qquad C_{m2} = 2\left(\frac{g_{m2}}{g_{m3}}\right)C_L \tag{2}$$

Non-dominate poles depends on the compensation capacitor and load capacitor. For the 60^0 phase margin and $\frac{1}{\sqrt{2}}$ damping factor unity gain bandwidth (UGB) derived as follows.

$$\text{UGB} = \frac{1}{4}\left(\frac{g_{m3}}{C_L}\right) \tag{3}$$

For a given UGB and load capacitor (decided by the application), final stage trans-conductance has to be increased to maintain stability, so this is not suitable for low power applications. The desirable wish for the compensation is in to increase the resonance frequency and decrease the damping factor. The resonance frequency of the non-dominate 2nd order transfer function of equation (1) is always inversely proportional to $\sqrt{C_{m2}}$ and damping factor proportional to C_{m2}. Hence damping factor and resonance frequency goes in same direction [6], contrary to the wish. It is therefore desirable to decrease or find another way to compensate without using C_{m2}. Fig:1 (b) shows popular miller compensation with nulling resistor to cancel the RH zero. Fig:1 (c) shows NGC compensation, which is better than NMC due to the additional feedforward stages which create left half zeros and controls the damping factor efficiently. Eventually, feedforward stage decides the location of zero, which limits the opamp power consumption. Output voltage swing also limited by the feedforward stage so this architecture is not suitable for the present bio-medical application. Fig:1(d) shows DFCFC, where without using C_{m2} damping factor has been controlled through an amplifier with a small capacitive feedback around that. Transfer function can be expressed as follows.

$$\frac{1}{\left(1+S\frac{C_{m1}}{g_{m1}}\right)\left(1+S\frac{C_L g_{m3}}{g_{m2}g_{m3}+g_{f1}g_{f2}}+S^2\frac{C_{m2}C_L}{g_{m2}g_{m3}+g_{f1}g_{m3}}\right)} \tag{4}$$

Damping factor and resonance frequency can be controlled by a suitable value of g_{f2} and gain bandwidth product is strongly depends on C_{m1} (same as miller). Non-dominate poles are weekly depends on C_L and be easily positioned at high frequency. Phase margin can be adjusted by using appropriate values of C_{m1} and g_{f2}. Resonance frequency and quality factor expressed as follows.

$$w_o = \sqrt{\frac{g_{m2}g_{m3} + g_{f1}g_{m3}}{C_{m2}C_L}}$$

$$Q = \frac{1}{g_{f2}}\sqrt{\frac{(g_{m2}g_{m3}+g_{f1}g_{m2})C_{m2}}{C_L}}$$

Despites the advantages of complex pole Q control through gf2 without using large compensation capacitor, very difficult to implement damping factor block (g_{f2}) due to its implementation nature[8]. It has to operate in open loop to enable miller capacitor multiplication, but open loop amplifiers are prone to latch-up in the presence of a mismatch.

III. PROPOSED OPAMP COMPENSATION

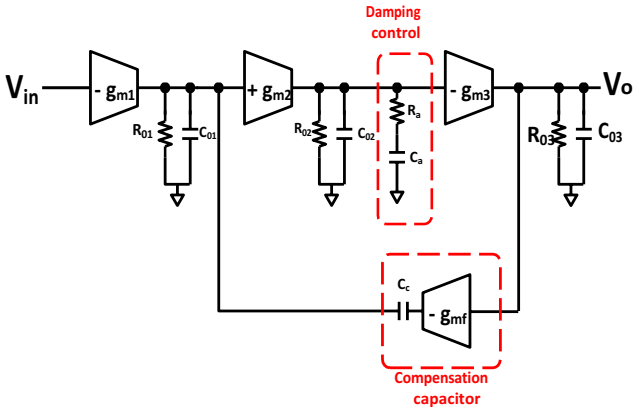

Fig. 2. Proposed compensation technique

The presented technique shown in Fig:2 is based on the passive damping control instead of active damping compensation [7] and a reverse miller compensation through a trans-conductance (g_{mf}) and compensation capacitor C_C. In case of NMC technique a compensation capacitor (C_{m2}), where damping factor depends on inversely proportional to R_{02}, so we need to have very less 2nd stage output impedance for high damping well behaved system. But small R_{02} will decrease 2nd stage gain, this limit the overall amplifier gain. So to solve this problem a passive damping circuit has been proposed.

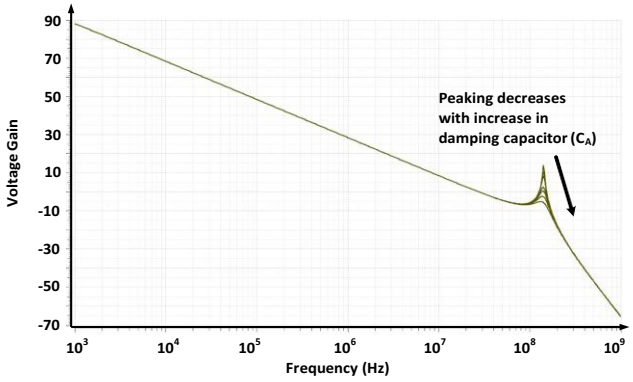

Fig. 3. Effect of series capacitor on damping

Basically, it is series RC circuit, which will be connected to the 2nd stage output. At low-frequency where capacitor impedance dominates, RC circuit doesn't have any impact on the amplifier gain. Series resistance(R_a) can be chosen very small to have higher damping without any compromise on the 2nd stage impedance. At high-frequency, series RC circuit can be approximated as resistor, but o/p impedance of 2nd stage will be fallen to very low value due to 2nd dominate pole at the output. The main advantage of this passive technique is no power overhead. A reverse miller capacitor has been used from the output of the first stage to output of the 3rd stage for creating dominate pole. Feedforward stage g_{mf} has been used to nullify the right half zero (RHZ), this will compromise the high frequency stability. A very small value (100us) of g_{mf} is sufficient to place RHZ far from unity gain bandwidth.

Transfer-function of the proposed system can be derived as follows.

$$\frac{A_{dc}\left(1+\frac{c}{g_{mf}}\right)}{\left(1+\frac{S}{P_{3dB}}\right)\left(1+S\frac{C_{01}C_L g_{m2}}{R_a C(g_{mf}-g_{m2})}+S^2\frac{C_{02}C_L R_a}{g_m-g_{m2}}\right)}$$

Where $_{dc} = g_{m1}R_{01}g_{m2}R_{02}g_{m3}R_{03}$

Unity gain bandwidth= $\frac{m1}{C_c}$

From the above transfer function for stable operation $g_{mf} > g_{m2}$. For low power operation g_{m2} can be minimized by maximizing other trans-conductance's. The present technique minimizes the power consumption through passive circuits, whereas published literature has been used very big capacitors or power hungry amplifiers. Both capacitors c_a,c_c can be adjusted to optimize the phase margin which will get acceptable peaking in the frequency domain. Fig:3 shows the effect of series capacitor on the open loop transfer-function, where it is clearly evident that series capacitor will strongly control the peaking, means damping control.

IV. IMPLIMENTAION DETAILS.

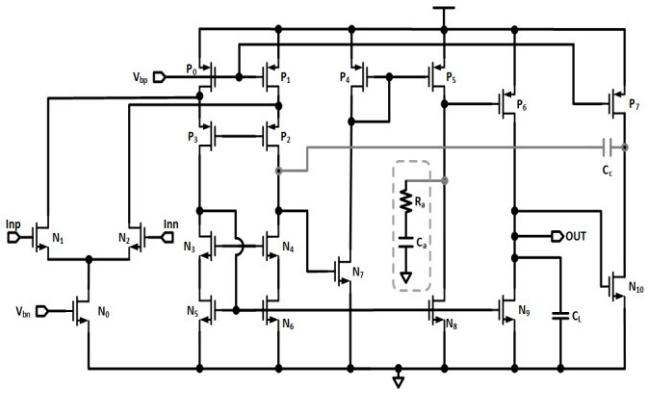

Fig. 4. Transister level schematic

Fig:4 shows the transistor level implemented schematic of a 3-stage amplifier. First stage is a folded cascade opamp implemented by N_0-N_6, where N_1, N_2 forms nmos input differential pair and other transistors are cascade loads.gm1, R_{01} are the trans-conductance of the differential pair and

output impedance. Second stage is realized with N_7-N_8, which forms non-inverting amplifiers. Third state inverting stage has been implemented with P_6-N_9. Transistor N_{10} forms feed-forward stage with C_C as a miller compensated capacitance connected in between the feedforward stage and 1st stage output, due to feedforward amplifier there is no right half zero (RHZ). 2nd stage amplifier has been loaded by RC series circuit to control the damping factor as explained in Fig: 1. Low frequency amplifier gain was around ~100dB. Differential pair tail current and cascade transistors biased with constant g_m beta multiplier bias circuit, to maintain constant bandwidth across PVT and supply voltage independent bias current [11]. Fig:5 shows the bias circuit, which works based on the following principle. To keep opamp gm constant across PVT, it needs to be biased with a PTAT nature current to compensate mobility degradation with temperature. In the constant g_m circuit Voltage across R_s is depends on the delta vgs of the N_1,N_2, which indeed has +ve temperature coefficient. This PTAT nature current makes opamp bandwidth less process and temperature dependent, hence it's stability as well.

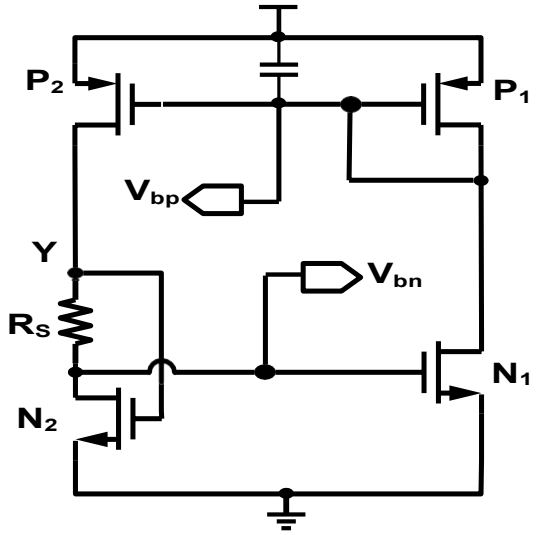

Fig. 5. Constant gm bias circuit

V. SIMULATION RESULTS.

Proposed opamp is implemented 45nm general purpose CMOS 1poly-8 metal technology. Simulated with post layout extracted circuit with Spectre and results as follows. Designed circuit has been working across wide temperature range and power supply range. Designed for 100dB nominal voltage gain, 25MHz unity gain bandwidth (UGB), 50^0 phase margin. The values of compensation elements, Ra,Ca,Cc are 4.7kΩ,0.3pF,1.7pF respectively. Opamp has been biased with 12uA from 1V power supply. Fig. 6 shows open loop frequency response. For low power consumption just enough target phase margin has targeted so it's variation should also be acceptable, so ran 300 Monte Carlo simulation and Fig: 7 shows the histogram of the phase margin with 3-sigma model files. Fig:8 shows the noise performance of the opamp, which shows -150dB noise at 1MHz spot and integrated rms noise ~890nV very much acceptable for bio-medical or high sensitive applications. Fig:9 shows the layout of the proposed circuit. Special care has been taken while laying the devices, like interdigitated style for current mirrors and common centroid matching for input differential pair. Shallow trench Isolation (STI) effect has been reduced by using sufficient number dummy devices on both sides of the critical devices and maintained enough distance between device edge and nwell to mitigate threshold voltage shift due to well proximity effect. Excluding decaps, this layout occupies 4875um^2.

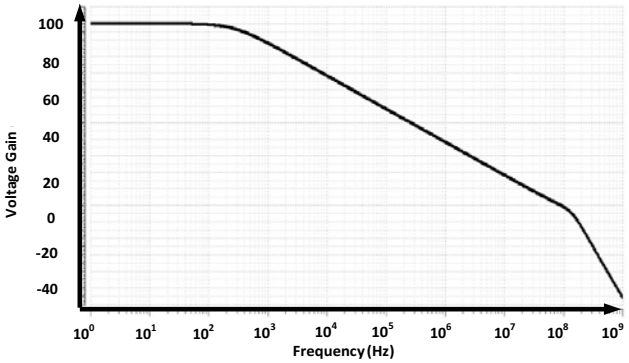

Fig. 6. Frequency response

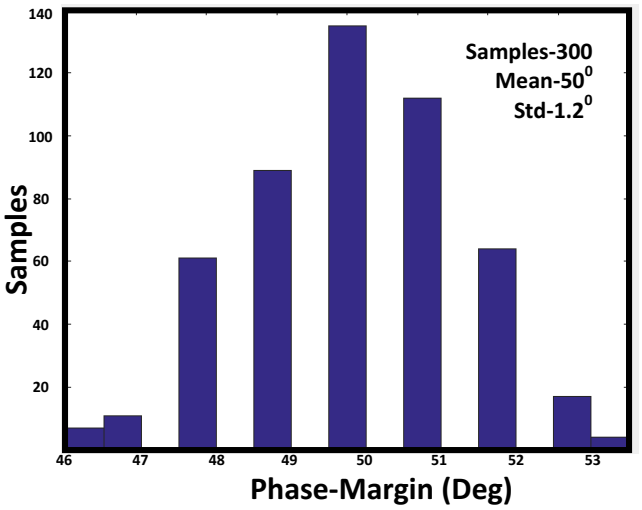

Fig. 7. Phase Margin histogram

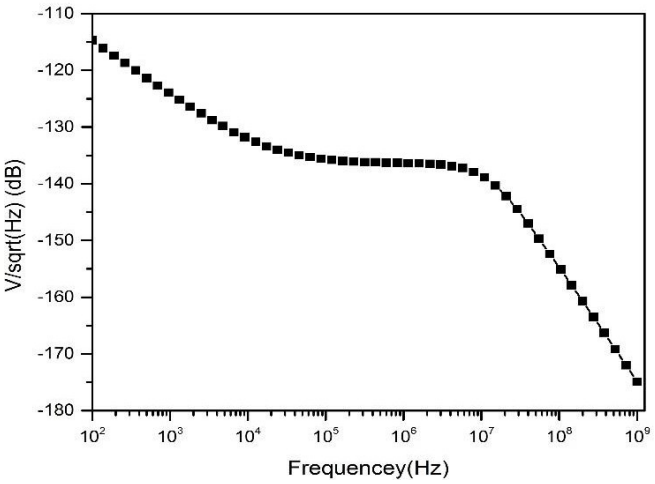

Fig. 8. Noise Spectral Density

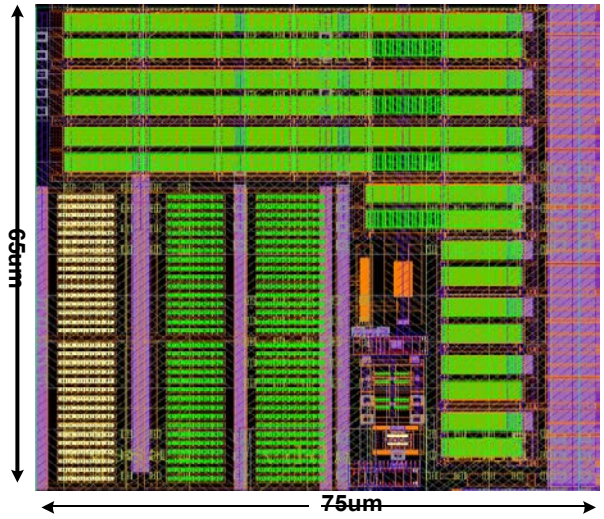

Fig. 9. Layout of bandgap reference..

VI. Conclusions.

Passive damping factor control bases compensation has introduced, wihtout having any additonal power consumption. Shows 3x power efficiency compared to start of art. Implimented in 45nm cmos,simulations shows 12uW power consumption when driving 1pF load capacitance. Standard deviation of Phase marging is $1.2^{0.}$

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