Parasitic Effects on Memristive Logic Architecture

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***Abstract*—The most of the memristor based applications which have been proposed so far have not considered the parasitic components. In this paper, we apply a generic memristor model which includes the parasitic effects to our proposed memristive logic architectures. First, we show that the current response of the memristor has the decaying oscillation when the unit step function is applied. Then we demonstrated that our specific memristive logic structure can almost eliminate those effects which are generated by the parasitic components of the memristor. In addition, the propagation delay and the variation of the memristive XOR gate are increased because of the parasitic components. With the delay analysis on cascaded memristive logic design, the experimental results show that our 3T-4M memristive XOR architecture can build the more robust delay based memristive physical unclonable function (PUF) comparing to the existing memristive PUF.**

***keywords*—** *memristor, hysteresis loop, memristive Logic gate, AND, OR, 3T-4M XOR, parasitic effects, physical unclonable function (PUF).*

I. Introduction

Conventional Metal Oxide Semiconductor (MOS) Transistor is reaching its minimal limit and it may stop shrinking in near future due to the cost increases in manufacturing. To keep increasing transistor density and maintaining the Moore's Law for a few decades, some chip manufacturers come up with new transistor typologies e.g. gate-all-around (GAA) nanowire transistors, III-V FinFET and vertical TFET etc.. Especially for the vertical transistor with nanoscale GAA design, it allows the tremendous increase in transistor density. However, apart from the pure transistor based chips, another emerging nanoscale electronic element, memristor, could be a highly promising alternative component for the evolution of the chips. The memristor as a two terminal device was proposed by Leon Chua in 1971 [1], and the first physical memristive device based on titanium dioxide (TiO_2) was fabricated at Hewlett-Packard lab in 2008 [2]. Since then, a number of memristor models have been proposed rapidly [2]–[9] with their own attributes (e.g. symmetricity and operating frequency) and have been applied in different areas such as high density memory design [10], [11], neuromorphic systems [12], [13] and logic design [14]–[21]. In the beginning, the proposed memristor models used for these applications did not consider the parasitic effects. Then, [22]–[24] proposed a generic memristor model with parasitic components and it corresponds more closely to the memristive device in the real world. In this paper, we discuss how the parasitic components of the memristor model effect our proposed memristive logic architectures [20], [21]; and we also present the certain advantages of our proposed 3T-4M logic architecture over the existing 6T-2M logic architecture [18] while dealing with the cascaded XOR structure. For example, delay based Physical Unclonable Function (PUF) [25], [26].

The paper is organised as follows. A generic memristor model with the parasitic components is reviewed in Section II. The parasitic effects of the generic memristor model on the memristive logic architecture are demonstrated in Section III. With the help of the cascaded XOR structure, Section IV shows that our proposed memristive logic architectures [20], [21] provide more reliable performance as compared to the existing memristive logic technique [18]. The paper is concluded in Section V.

II. Background

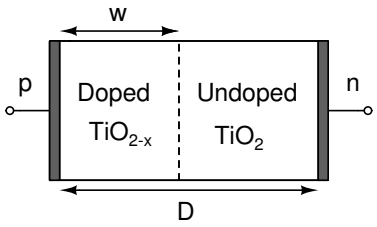
In this section, we give a brief overview of the TiO_x based memristor model with and without parasitic components.

A. Memristor Model without Parasitic Components

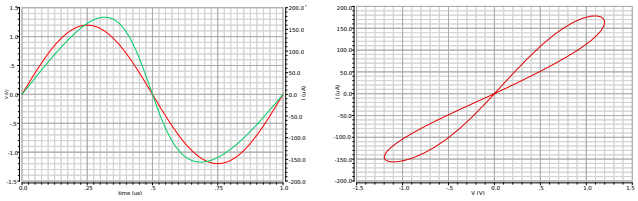
One of the most commonly used technologies for fabricating memristive devices are based on oxides [2], [27]. Fig. 1(a) shows a fundamental structure of a TiO_x based memristor. It consists of heavily doped TiO_{2-x} region with the width of w and zero doped TiO_2 region with the width of $D-w$, where D is the width of the device. When a positive voltage is applied to the positive terminal (p) of the device, the oxygen vacancies carried the positive charges in TiO_{2-x} region drift into the TiO_2 region. Therefore, the width w of the TiO_{2-x} region is increased and the device switches to a low resistance (R_{on}) state. However, when a positive voltage is applied to the negative terminal (n), the oxygen vacancies are attracted to the p-terminal. This results in a decrease of the width of TiO_{2-x} region. Therefore, the device switches to a high resistance (R_{off}) state. If there is no voltage applied to either terminal, the boundary between the two regions freezes. Hence, it allows the memristor to retain its previous state.

We applied the input voltage, $v(t) = A\sin(2\pi ft)$, to the memristor at 1MHz, where, $A = 1.2V$. The memristor current response as shown in Fig. 1(b) indicates that there is no phase shift between the input voltage and the output current. Hence, the memristor is pinched at the origin and Fig. 1(c) illustrates the memristor pinched hysteresis characteristic.

However, [22]–[24], [28] demonstrated that the pinched point of some real physical memristive devices may not placed at origin and it could disappear when the circuit operates above the certain frequency.



(a) A TiO_x based memristor model.



(b) The voltage and current in the memristor.

(c) Memristor pinched hysteresis loop.

Fig. 1. Basic memristor model and I-V characteristic.

B. Generic Memristor Model

To emulate the physical memristive device properly, the paper [22] and [23] proposed a generic memristor model as shown in Fig. 2(a), where m represents the memristor model without parasitic components. This generic model consists of the memristor basic model in parallel with a parasitic capacitor C_p and a current source I_p. Then, a parasitic inductor L_p along with a voltage source E_p is connected in series as shown in Fig. 2(a).

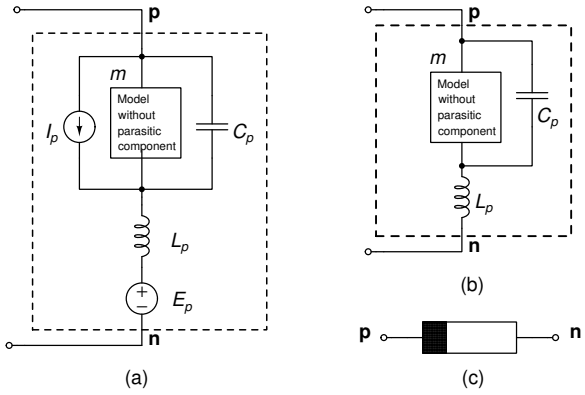
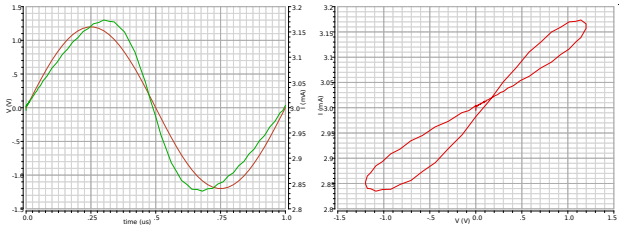


Fig. 2. Memristor with parasitic components.

To demonstrate the pinched hysteresis loop drifted from the origin, we assume that $C_p = 1pF$, $I_p = 3mA$, $L_p = 10nH$ and $E_p = 30mV$. We applied a sinusoidal voltage with 1.2V to the Fig. 2(a) at 1MHz. The result in Fig. 3(a) observes that the parasitic components induce the phase shift to the current response. Therefore, the pinched point drifts from the origin as shown in Fig. 3(b), thereby non-ideal pinched hysteresis loop [23]. The voltage source E_p and the current source I_p directly emulate the phase shift of the current response. Hence, Fig. 2(b) represents the simplified model which only considers the capacitor C_p and the inductor L_p as the parasitic components. The symbol of the Fig. 2(b) is illustrated in Fig. 2(c).



(a) (b)

Fig. 3. I-V characteristic of the Fig. 2(a): (a) The input voltage and the current response of Fig. 2(a), where the red signal is sinusoidal voltage and the green signal is the current response; (b) The non-ideal I-V pinched hysteresis loop for Fig. 2(a).

A number of memristor models have been proposed in [2]–[9]. However, in this case, the model applied for m in Fig. 2(b) should be asymmetric which is suitable for logic design. Therefore, the voltage controlled VTEAM model [9] as one of the most flexible models has been considered as m in Fig. 2(b) and coded in Verilog-A for all the memristive logic architectures described in the following sections.

All the designs in this paper were implemented and simulated in Cadence Virtuoso. The supply voltage is $V_{DD} = 1V$ and the transistors used for the following sections are all based on 32nm CMOS technology node.

III. Parasitic Effects on Memristive Logic Architecture

In this section, we applied the unite step function to the single memristor to investigate the decaying oscillation of the current response. Then the parasitic effects on memristive logic design will be analysed by implementing the new generic memristor model to the existing MRL [16] and our proposed memristive logic architecture.

A. Unit Step Response for the Single Memristor

To evaluate the parasitic effects on the memristive logic architecture, we demonstrated the unit step response for a single memristor model as shown in Fig. 2(b). The impedance of the memristor for the Low Resistance state (LRS) and the High Resistance State (HRS) are shown in Eq. (1) and Eq. (2) respectively.

$$Z_{\text{on}} = (R_{\text{on}} || Z_{\text{C}}) + Z_{\text{L}} = \frac{R_{\text{on}} \frac{1}{sC}}{R_{\text{on}} + \frac{1}{sC}} + sL \tag{1}$$

$$Z_{\text{off}} = (R_{\text{off}} || Z_{\text{C}}) + Z_{\text{L}} = \frac{R_{\text{off}} \frac{1}{sC}}{R_{\text{off}} + \frac{1}{sC}} + sL \tag{2}$$

Z_{C} represents the effective impedance of C_p which is $\frac{1}{sC}$. Similarly, Z_{L} represents the effective impedance of L_p which is equal to sL. Where, $\frac{1}{s}$ is the Laplace operator for the integration, and s is used for the differentiation. Hence, the current response of the memristor is calculated as follows:

$$I(s) = \frac{V(s)}{Z_{\text{on}}(s)} = \frac{\frac{1}{s}}{\frac{R_{\text{on}} \frac{1}{sC}}{R_{\text{on}} + \frac{1}{sC}} + sL} \tag{3}$$

Assuming $R_{\text{on}} = 500\Omega$, $C = 10pF$ and $L = 10nH$, we substituted these values into Eq. (3) and applied partial fraction expansion. The poles of the denominator are complex conjugates which are located in left half of the s-plane. Hence, the memristor generated the decaying oscillation and is referred as underdamped which is illustrated in Fig. 4.

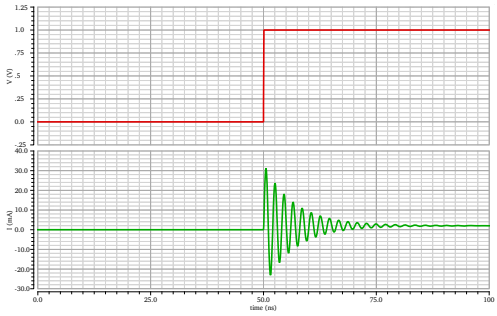


Fig. 4. Step response of the generic memristor model which is shown in Fig. 2(b): The first signal is the unit step input; The second signal is the current response of the memristor.

B. Parasitic Effects on Memristive XOR Logic Architecture

We applied the model as presented in Fig. 2(b) to the Memristor Ratioed Logic (MRL) architecture [16]. The fundamental idea behind the MRL is that it is used the programmable resistance of the memristive device to ensure that the circuit operates like a voltage divider for realising the Boolean OR and AND functions as shown in Fig. 5(a) and Fig. 5(b) respectively. The input/output behaviour of OR and AND operations based on the MRL architecture in Fig. 5 is presented in Fig. 7. Owing to the parasitic components of the memristor, the output logic OR and AND operations demonstrated the decaying oscillation effects which are shown in Fig. 7, especially, when the logic inputs are at the switching stages.

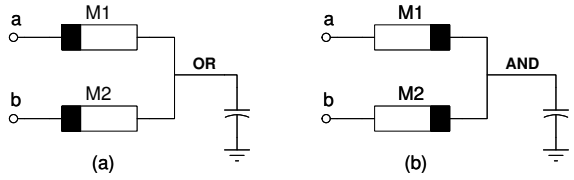


Fig. 5. Memristive AND-OR functionality; (a) OR function, (b) AND function.

In [20], [21], we proposed the purely memristive XOR architecture which consists of four memristors M_1, M_2, M_3 and M_4 as shown in Fig. 6(a). Here M_1 and M_3 are connected for logical AND gate. M_2 and M_4 are connected for logical OR gate. Then, the XOR operation can be generated by taking the voltage difference between V_{L1} and $V_{L2}(V_{L1} - V_{L2})$ as shown in Fig. 7. Most of the decaying oscillations generated by the parasitic components have been cancelled here. To realise the XOR operation, we integrated the NMOS transistor (NMOST) to the purely memristive XOR architecture as shown in Fig. 6(a). The gate and the drain terminals are connected to V_{L2} (AND) and V_{L1} (OR) respectively, where the load resistor R_{D} is used to bias the NMOST. This results a 1-transistor and 4-memristor (1T-4M) XOR architecture as shown in Fig. 6(b). However, by connecting the PMOS transistor (PMOST) to the voltages V_{L1} and V_{L2}, the memristive XNOR operation can be realised in Fig. 6(c) [20], [21]. The output of the 1T-4M XOR architecture is demonstrated in Fig. 7, as it can be said that the parasitic effects have been nearly eliminated by the NMOST.

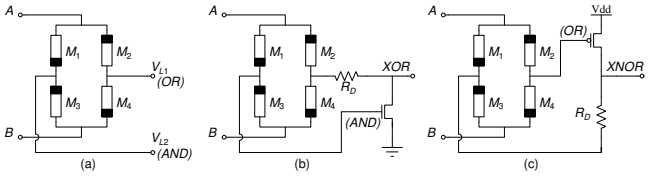


Fig. 6. The memristive XOR/XNOR functionality [20], [21]: (a) The purely memristive XOR functionality; (b) 1T-4M bufferless memristive XOR functionality; (c) 1T-4M bufferless memristive XNOR functionality.

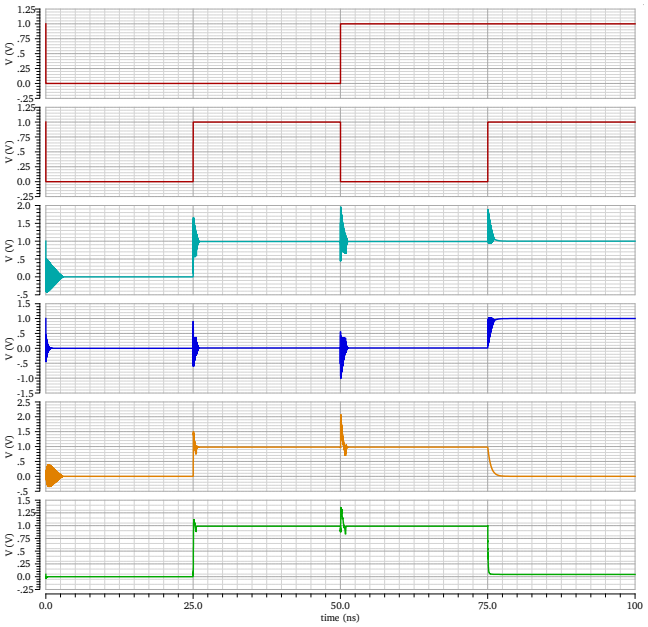


Fig. 7. Top two signals are the inputs a and b respectively; third: the output of V_{L1} (OR gate); fourth: the output of V_{L2} (AND gate); fifth: the voltage difference between the V_{L1} and V_{L2}; sixth: the output of the 1T-4M XOR architecture.

IV. Delay Analysis on Cascaded Memristive XOR Architecture

In this section, we will demonstrate that the parasitic components such as the C_p and L_p have been included in Fig. 2(b), then the single memristive XOR gate generates more propagation delay because of the increase in RC time constant. This kind of characteristics can be used for generating delay-based Physical Unclonable Function (PUF) [25], [26]; and by integrating with those parasitic components, memristive XOR gate can also increase the degree of the variation which is shown in Fig. 8. It is in somehow leveraged the randomness of the PUF. With the help of the 5-stage

memristive XOR gates cascaded, we show that our proposed 3T-4M buffered XOR architecture in Fig. 9(a) provides robust performance compared with other existing 6T-2M XOR architecture [18].

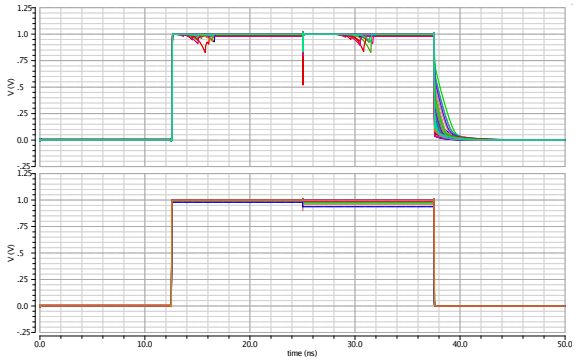


Fig. 8. Monte Carlo simulation on single memristive XOR architecture at 25MHz. The top signals are the outputs from the XOR gate with parasitic components; the bottom signals are the outputs from the XOR gate without parasitic component. 15% variation on the size of the memristor (10nm) has been taken here. (For the sake of simplicity, we sampled 50 points as the demonstration.)

To evaluate the time delay for each stage of the PUF, we utilised fully buffered 3T-4M XOR gate as shown in Fig. 9(a) and constructed them in the fashion represented in Fig. 9(c). It will become the basic PUF circuit if the D-type flip-flop is followed by the cascaded XOR gates. Here, C_0, C_1, C_2, C_3 and C_4 are the challenge bits. The output q from the D-type flip-flop is the response bit of the PUF. For the sake of simplicity, in this case, the challenge bits have been assumed by exactly the same logic level as $C_0 = C_1 = C_2 = C_3 = C_4$. This results the same XOR behaviour with the propagation delay between the node x and the node y which are labeled in Fig. 9(c). Assuming $R_{\text{on}} = 500\Omega$, $R_{\text{off}} = 80k\Omega$, $C_p = 50fF$ and $L_p = 15nH$, we run the simulation under 50MHz. The outputs from the node x and node y are illustrated in Fig. 10. The blue signal refer to the output from the first stage x and the green one refer to the output from the fifth stage y. The propagation time delay from the first stage to the fifth stage is approximately 0.519ns. Hence, our 3T-4M XOR structure provides about $0.519/5 = 0.104ns$ time delay at each stage.

Fig. 10 also represents that our proposed 3T-4M buffered XOR architecture can still derive the reliable performance even the signal travelling through multiple stages. To compared our architecture with other techniques, we apply the 6T-2M XOR architecture [18] as shown in Fig. 9(b) to the Fig. 9(c). One of the problems of this design is that the resistance of the R_{on} has to be big enough to ensure that the two NMOSTs can be biased properly. Hence, the value of R_{on} was assumed as 30kΩ in this case. However, when this 6T-2M architecture considers the parasitic components, the circuit in Fig. 9(c) becomes the multiple LC oscillation circuits connected in series and it increased the the total inductance of inductors. The output of the 5-stage cascaded 6T-2M XOR gates shows the oscillation as presented in Fig. 11. Therefore, our proposed 3T-4M buffered XOR cascaded architecture provides more reliable performance by comparing with the 6T-2M technique as shown in Fig. 11.

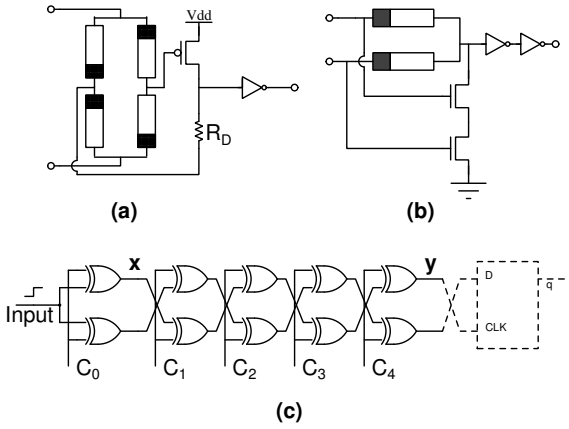


Fig. 9. Cascaded Memristive XOR gates. (a) 3T-4M buffered XOR architecture; (b) Existing 6T-2M XOR architecture [18]; (c) 5-stage cascaded memristive XOR gates.

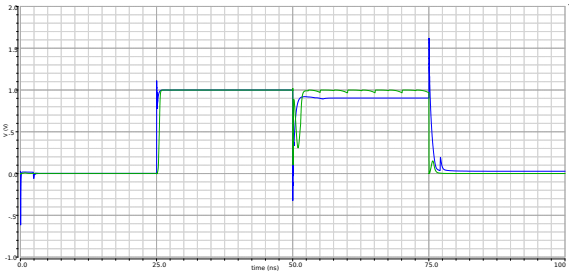


Fig. 10. The output of the memristive XOR gates between x and y. The blue signal is the output from the node x and the green signal from the node y.

V. Conclusions

This paper discusses the memristor parasitic effects on both the existing and the proposed memristive logic architecture. The parasitic components L_p and C_p are considered with the pure memristor model to form the RLC circuit which generate the decaying oscillation especially when the input logic state changes simultaneously. However, most of these parasitic effects are being cancelled by our 1T-4M XOR structure as the voltage difference is obtained from the output. In this paper, we also demonstrated that our 3T-4M buffered XOR gate produces more variation and propagation delay with C_p and L_p. With the help of the circuit of 5-stages cascaded memristive XOR architecture, we calculated the time delay for each stage which is approximately 0.104ns at 50MHz. In addition, by comparing with other 6T-2M XOR technique, the experimental results show that our 3T-4M structure can still provide more reliable performance even with parasitic effects. Overall, our 3T-4M buffered XOR architecture can be used to create the PUF with the high degree of the randomness.

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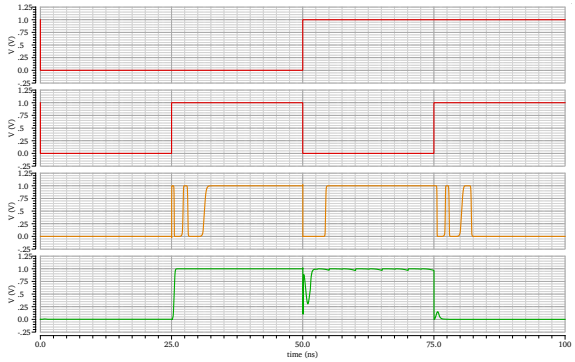

Fig. 11. Outputs of the cascaded Memristive XOR gates: the top two signals are the inputs; the third signal is the output of the 5-stage cascaded 6T-2M XOR architecture; the fourth signal is the output of the 5-stage cascaded 3T-4M XOR architecture.

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