A Start-up Assisted Fully Differential Folded Cascode Opamp

R. Nagulapalli, K. Hayatleh, S. Barker, B. Yassine, S. Zourob, S. Raparthy, N. Yassine

This paper explains the hidden positive feedback in the two-stage fully differential amplifier through external feedback resistors, and possible DC latch-up during the amplifier start-up. The biasing current selection among the cascode branches have been explained intuitively, With reference to previous literature. To avoid the latch-up problem irrespective of the transistor bias currents a novel, hysteresis based start-up circuit is proposed. An 87dB, 250MHz unity gain bandwidth amplifier has been developed in 65nm CMOS Technology and post-layout simulations demonstrate no start-up failures out of 1000 Monte-Carlo (6-Sigma) simulations. The circuit draws 126uA from a 1.2V supply and occupies the 2184um^2 area.

Keywords: Folded-Cascode, Latch-up, DC gain, leakage, CMOS scaling, Monte-Carlo, Slew-rate.

1. Introduction: Over the years, CMOS technology scaling down processes have followed Moore's law, which predicts the number of transistors per unit area doubles every two years, resulting in approximately 30% reduction in the transistor length. Positive consequences of this scaling include significantly decreased chip size, increase in circuit speed, and a reduction in power requirements [1]. Due to the reduced device dimensions, the drain to source electric field will increase, which causes carrier velocity saturation and eventually, electron mobility (μ_n) degradation. To maintain the internal electric field at a constant level, device engineers have opted to decrease the power supply voltage (V_{dd}), but the transistor threshold voltage is not similarly decreased due to digital leakage power limits. Digital design benefit from this scaling to a great extent due to lower V_{dd}, because the switching power can be expressed as CV_{dd}^2f, where C is the switching capacitance and f is the operating frequency. It is clear from this that power dissipation will decrease with V_{dd}. Unfortunately, downscaling negatively impacts analogue circuits in many ways. For example, the available V_{ds} for every transistor in a transistor stack is decreased, as well as its output impedance. This leads to low DC voltage gain and degraded output noise, therefore requiring a multi-stage amplifier to meet a specific DC gain target [2]. Cascode opamps are the only solution to achieve a high DC gain in scaled CMOS technology, due to their high output impedance. Telescopic and Folded cascode opamps are popular architectures in the literature, and both have advantages and disadvantages. The output voltage swing is limited by the input common mode voltage in a telescopic cascode opamp, whereas a folded cascode opamp can support higher voltage swings at the output, independent of input common mode voltage, but at the expense of higher power disspation and increased noise levels. Because of the increased use of digital circuitry, switching noise has been increased dramatically. This will affect the analogue circuit signal to noise ratio (SNR) and the sensitivity of the circuits will be compromised. Hence there is a need for fully differential circuits, which have several advantages in comparison to single-ended, such as: immunity to common-mode noise, double swing for a given power supply voltage (6dB increase in dynamic range) and reduced even-harmonics at the output.

The rest of the paper has been organized as follows. Section 2 describes the multiple feedbacks involved in two-stage folded cascode opamps and the DC latch-up problem, section 3 describes a proposed solution to make the amplifier robust against latch-up problems, and finally, section 4 describes the prototype simulation results and summarizes the paper.

2. Two-stage folded Cascode amplifier: Fig. 1 shows a conventional fully differential inverting amplifier, which gain set by the ratio of resistors R_1 and R_2. This circuit has two negative feedback loops. The feedback resistor R_2 is connected such that there will be negative feedback around the opamp for the differential mode signal of the opamp [3]. Fig. 2 (a) shows the internal implementation details of the opamp. Transistors M_1 to M_7 form the first stage, M_8 to M_9 form the second stage, and R_{cm} and OA_1 form the common mode feedback (CMFB) network. Fig. 2(b) depicts the Cascode bias generation scheme for the folded cascode opamp shown in fig. 2(a). Gate potentials of M_3 and M_9 are same, but to reduce the complexity we shown as two different terminals.

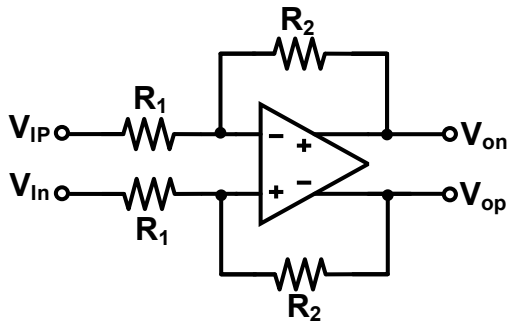

Fig. 1 Inverting Amplifier

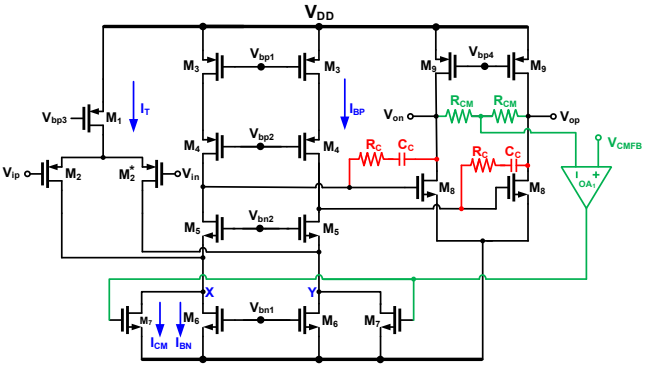

Fig. 2 (a) Folded Cascode Fully Differential Amplifier

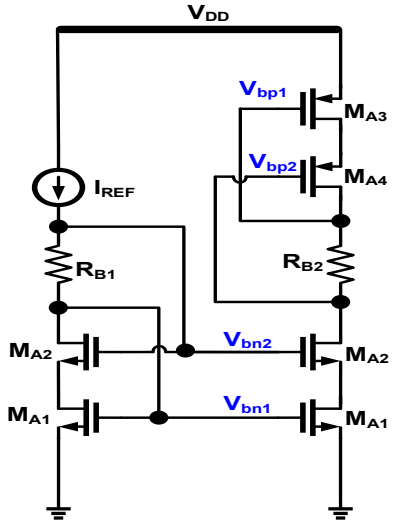

Fig. 2 (b) Bias voltage generation for Fig. 2(a)

To illustrate the common mode feedback path, a common mode equivalent circuit of Fig. 2 has been shown in Fig. 3. The first and second stages act as inverting stages, so the feedback through external resistors is positive, which could be considered an external feedback loop. Though positive feedback is risky and undesirable, it can't be avoided here because the feedback resistors (R_1,R_2) are connected in such a way that there will always be negative feedback and as a by-product of this connection an internal common-mode feedback through R_{cm} to OA_1 forms positive feedback. To have a stable DC operating point, internal feedback should always be stronger than the external feedback loop, otherwise, outputs may latch onto the rails. External positive feedback loop gain can be expressed, as shown in equation (1).

$$Lg_{ext} = A_1 A_2 \frac{R_1}{R_1+R_2} \quad (1)$$

Where A_1 is first stage gain, expressed as:

$$\frac{g_{m1}}{1+g_{m2}r_{01}} g_{m5} r_{05} r_{06} \sim \frac{g_{m1} g_{m5} r_{05} r_{06}}{g_{m2} r_{01}}$$

Where A2 is second stage gain expressed as: $g_{m8}r_{09}$

Where g_m and r_o are the transconductances, output-impedance of the respective transistor. Internal negative feedback CMFB loop-gain can be expressed, as shown in equation (2).

$$Lg_{int} = g_{m7}g_{m5}r_{05}r_{07}g_{m8}r_{08}A_{CM} \qquad (2)$$

Where A_{CM} is the gain of CMFB of OA_1. To ensure a stable DC common mode operating point, the positive feedback loop gain should be smaller than the negative feedback loop gain for all frequencies of interest ($Lg_{ext} \ll Lg_{int}$). In both equations (1) & (2), the 2nd stage gain ($g_{m8}r_{09}$) is common so as to have a stable operating point, which is always needed to make sure the first stage common mode gain is always smaller than the CMFB opamp gain. This is relatively easy to achieve because the first stage common mode gain is very low due to the degeneration effects of the tail transistor M_1. To simplify the frequency compensation of the CMFB loop, general practices are to split the load cascode device into two devices (M_6, M_7), where M_6 is driven by the constant bias, and only M_7 provides the loop gain, hence the common mode loop gain is decreased according to the ratio of M_6, M_7 dimensions [4]. Although this simplifies the frequency compensation, it weakens the negative feedback through internal CMFB loop, hence M7 can't be too small, in respect to its aspect ratio (W/L). Ideally, it should be small enough to improve the phase margin, but large enough to provide enough loop gain.

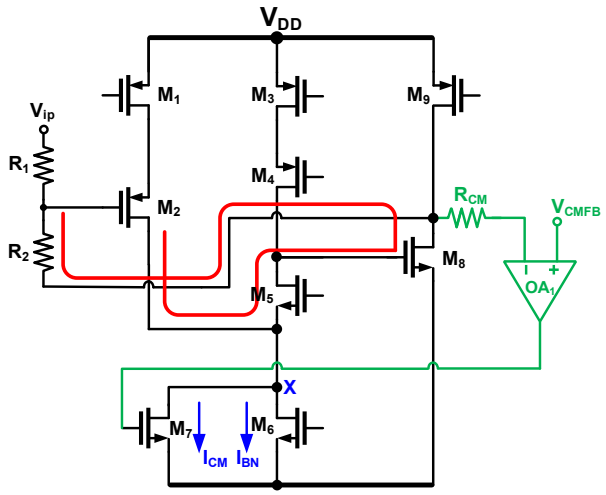

Fig. 3 Common Mode equivalent circuit of the amplifier

3. DC Latch-up Problem: The distribution of current amongst the opamp branches will determine many important parameters of the folded cascode opamp. The input differential pair small-signal trans-conductance (g_m) will decide the unity gain bandwidth of the opamp as given in (3), hence the tail current I_T will be fixed for a specific application. To make the first non-dominant pole frequency high enough to maintain a good phase margin, the minimum current I_{BP} is chosen to save power in the Cascode load transistors M_3, M_4, M_5.

$$\omega_u = \frac{R_1}{R_1+R_2}\frac{1}{C_L}\sqrt{I_T\mu_n C_{ox}\frac{W}{L}} \qquad (3)$$

This choice will not work to satisfy all the opamp requirements (Unity gain bandwidth, noise). The slewing process in a folded cascode is slightly more complicated than in other opamp architectures as explained next. The relationship between the branch currents is shown in equation (4).

$$I_{CM} + I_{BN} = I_{BP} + \frac{I_T}{2} \qquad (4)$$

If a large differential voltage is applied at the input of the opamp, the total tail current is steered towards M_2, and M_2* (Fig. 2a) will carry no current, hence M_5 current decreases to $I_{CM}+I_{BM}-I_T$ from $I_{CM}+I_{BM}-(I_T/2)$. If $I_{CM}+I_{BM}>=I_T$ then M_5 will carry finite current and the slew rate is given by I_T/C_C. An interesting consideration of the slew rate discussion would be observing what will happen if $I_{CM}+I_{BM}<I_T$. In such a case, M_5 would turn off and M_2 current would be $I_{CM}+I_{BM}$, hence M_2* would also carry current to satisfy KCL at the source of M_2. This is contrary to the general belief that during slewing one of a differential pair's transistors would turn off. In this case the slew rate is limited by I_{BP}, because M_5 would turn off and the slew rate would be given by I_{BP}/C_C, which is a low power option. In this case I_{BP} is smaller, but at the cost of large transient voltage dip at the node. There is a general tendency to set the currents in all branches to the same value, so that the slew rate is always decided by the tail current. This is especially important in switched capacitor amplifiers.

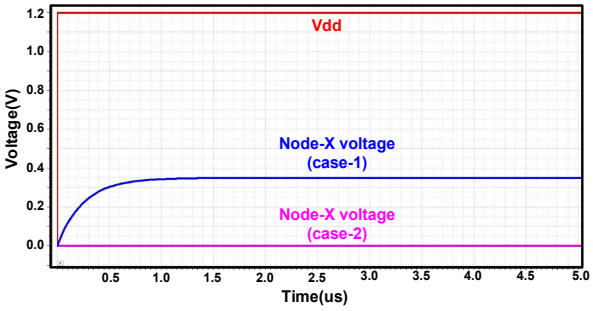

Fig. 4 Node X voltage start-up problem

Sometimes during start-up, or if there is any large transient dip in the power supply, node x (M_5 source) may become stuck at ground potential, and the input common mode stuck at V_{dd}. In this case, differential pairs turn off and there is no charging current to pull node x to the desired potential. The design should always make sure to have $I_{BP}>I_{BN}$, such there would be a pull-up current into node x. According to equation (4), if $I_{BP}>I_{BN}$, then $2I_{CM}>I_T$ would mean that CMFB should always control a current greater than half of the tail current. This is a very important conclusion for robust operation [4]. To demonstrate the problem, a folded cascode opamp was designed and initialized node x (Fig. 2) to 0V and the power supply voltage was stepped up to 1.2V. Fig. 4 depicts the simulation results. Case-2 is when the above condition violated by reducing the current, and clearly shows node x stuck at ground potential, making the opamp non-functional. Sometimes a spurious leakage of the cascode transistors, high-temperature effects, or even power supply ramp could bring the circuit out of the DC latch problem, but it is not safe to rely on these kinds of uncontrollable events [5]. Case-1 is corresponding to when the condition is met and node x moves towards the operating point (350mV in this case). Unfortunately, this condition can't always be met, or it would be easily violated when there is some process mismatch in the transistors. Fig. 5 shows the Monte-Carlo simulation results, out of 1000 simulations, 27 have been failed to start the opamp even though the condition met ($I_{BP}>I_{BN}$) because of process mismatch introduced by Monte-Carlo. One potential solution could be using the combination of an NMOS and PMOS input differential pair, often called a rail to rail opamp [4] to avoid the latch-up state at the cost additional power. Rail to rail amplifiers are prone to stability issues because the gain of the opamp is a function of the input common mode voltage. At a lower common mode voltage, only the PMOS input pair is active and for higher common mode voltage, the NMOS differential pair is active. At the mid rail common mode voltage both nmos and pmos differential pairs are active, which will result in higher loop-gain, hence prone to stability problems. Several new folded cascode opamps have proposed in the literature [6-11] with enhanced DC gain and bandwidth, but none of them discussed or addressed the latch-up issue explained above. Next section describes the proposed technique to address the latch-up issue.

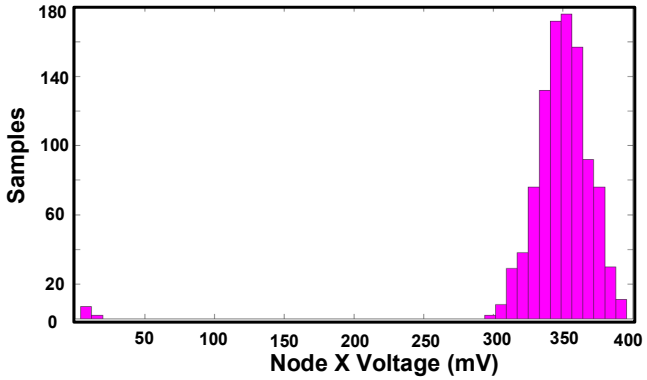

Fig. 5 MC sim showing Start-up failures (27 failures out of 1000 runs)

3. Proposed Solution: Rather than relying on design constraints [4], which are sensitive to device mismatch and use additional power, or utilising the rail to rail opamp which could give stability problems, a start-up assisted folded cascode would improve the robustness of the system and would solve the latch-up problem. When node x (Fig. 2) is stuck at very low voltage due to the problems mentioned in the section 2, a start-up circuit that senses this and pumps some current into it to assist its voltage ramping towards the operating point would solve the problem. Previously proposed start-up circuits operate on voltage comparison. The present proposal is purely based on current comparison, which makes design robust against PVT corners [12]. Fig. 6 shows the proposed start-up circuit, which relies on the current comparison principle. M_7 gate connected to the node x in the folded Cascode (Fig. 1), and M_2 is biased from a diode connected constant current transistor. When node x (Fig. 6) is stuck at ground potential M_7 current is zero, hence node c potential would rise to that of the supply. Because M_2 is a saturation region biased transistor with a finite V_{GS} to support zero current, its V_{ds} should be zero. Node z (Fig. 6) potential would reach very close to the ground because the M_3, M_4 combination is an inverter and transistor M_5, M_6 current would increase and pump current into node x (Fig. 6). Note that it seems like M_6 current flowing into an open circuit in Fig. 6. However, when it is connected to the main folded cascode opamp it would dump the current into the cascade transistors (M_6, M_7 in Fig. 3). The size of M_7 designed such that node C would reach ground potential, when the circuit moved out of the latch-up state (node x is settled to an appropriate potential), the start-up transistors M_5, M_6 will be turned off to save power. The inverter formed by M_3 and M_4 needs to behave like a comparator with a threshold closer to the supply so that when the potential of node C decreases to slightly less than V_{DD}, the inverter would turn off both M_5 and M_6. This was achieved by making transistor M_3 wider (connecting several in parallel) and transistor M_4 longer (several in series).

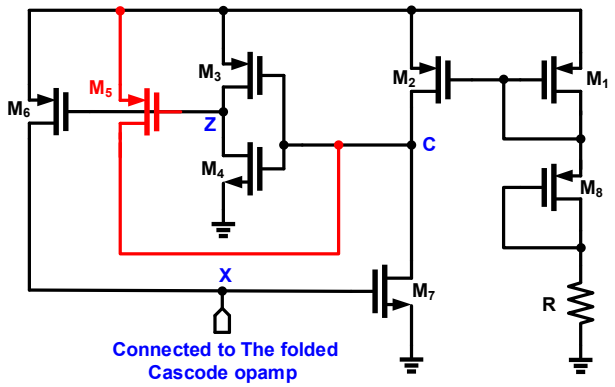

Fig. 6 Start-up circuit with Hysteresis

The start-up circuit's literature does not include any discussion regarding the inclusion of hysteresis [12][14]. Whenever there is leakage from devices (in modern technologies) start-up circuits could also be stuck at a potential depending on the leakage level. Hysteresis puts devices that are supposed to turn off into hard off mode, and vice versa. In Fig. 6, M_5 provides hysteresis and M_6 enables the start-up action by injecting current into the amplifier. When M_6 is required to pump current, M_5 acts as a pull-down node of voltage C such that M_6 is in hard on mode.

4. *Results*: A folded Cascode fully differential amplifier was designed using 65nm CMOS technology. To evaluate the start-up circuit functionality, in Fig. 6 the gate connection of M_7 and M_6 was broken and driven by the M_7 gate with a voltage source which terminated M_6 with a voltage source current. By sweeping the M_7 gate voltage, M_6 drain current was plotted in Fig. 7. It shows that the M_7 gate potential is close to the ground, M_6 is pumping 140uA into the amplifier (precisely into node x), which helps its start-up. As soon as the M_7 gate potential rises above 20mV, M_6 current drops, almost reaching ~21nA.

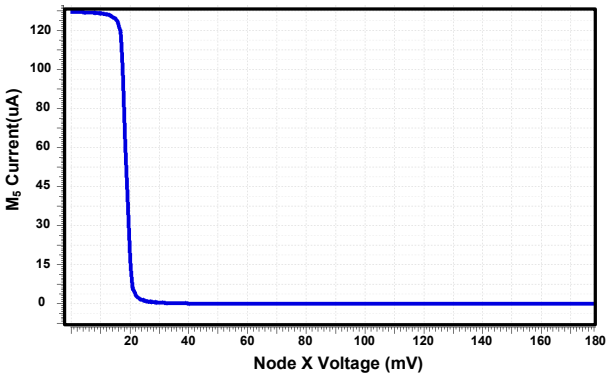

Fig. 7 Start-up Circuit Characteristics

A fully differential amplifier was simulated to check whether it still had a start-up issues. Fig. 8 shows the node x voltage histograms, reveals that node x voltage is not stuck near ground potential, hence no latch-up issue in 1000 runs. The node x voltage is close to 350mV (CMFB reference has been adjusted to make it 350mV) with a sigma of 13mV. Fig. 9 shows the open loop frequency response of the amplifier, and depicts an 88dB low-frequency voltage gain with a 250MHz unity gain bandwidth. Proposed amplifier has been configured in unity gain mode (R1=R2=10KΩ in Fig.1) to evaluate the large signal performance. Fig. 10 shows the step response for 100mV peak-peak single-ended input, as it is clear from the waveform, step response is settling without having any severe ringing because of well compensated loop with 62^0 phase-margin. The outputs (ON,OP) are having ~100mV amplitude with a common mode 600mV. Fig. 11 shows the total circuit layout, which occupies 2184um^2 of silicon area. The differential pair was laid out with a common centroid pattern to minimize the input referred offset. Current mirrors were laid out with a interdigitating pattern to minimize the current mismatch. Common-Centroid and inter-digitation techniques have been used in the layout to minimize the input referred offset. Differential-pair and cascode transistors sizes have been decided using gm/id methodology [13] and mismatch guidelines [15].

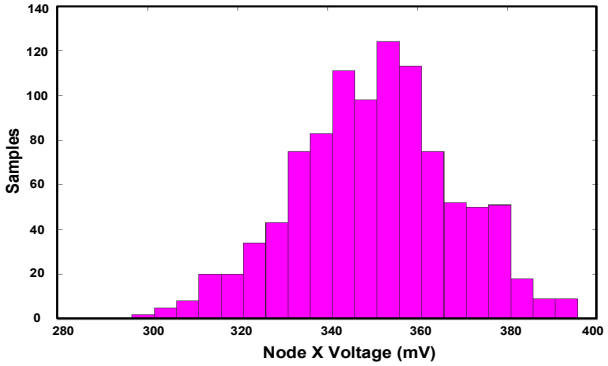

Fig. 8 Histogram of Node X voltage

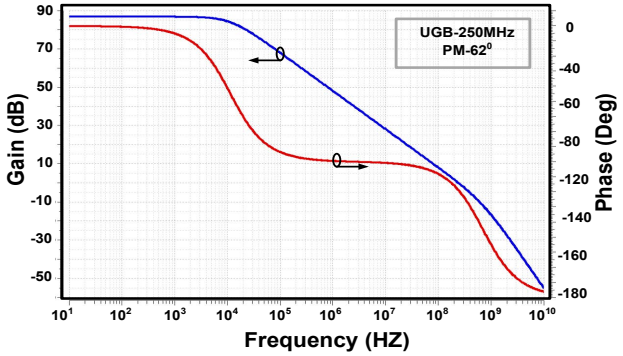

Fig. 9 Open Loop frequency response

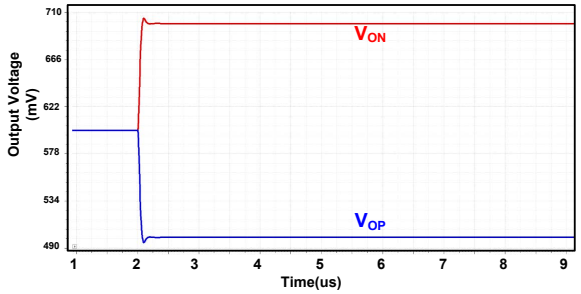

Fig. 10 Step response of the Proposed amplifier in inverting configuration.

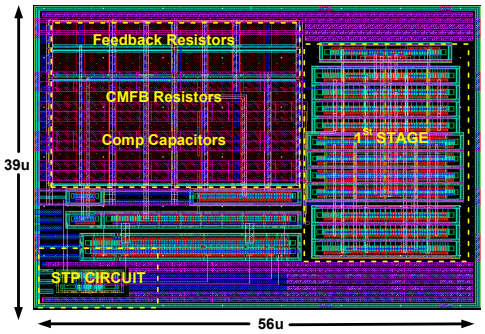

Fig. 11 Layout of the Proposed Solution

Table 1 Transistor sizes.

Transistors			
Folded Cascode		Start-up circuit	
Component Name	W/L (um/um)	Component Name	W/L (um/um)
M_1	72/3	M_1	1/4
M_2	36/3	M_2	1/4
M_3	52/2.6	M_3	3/.4
M_4	40/2.6	M_4	1/6
M_5	28/3	M_5	1/6
M_6	20/3	M_6	1/6
M_7	26/3	M_7	2/4
M8	14/1.2	M_8	1/4
M9	10/1		

Table II Performance comparison

Parameter	This Work	[4]	[10]	[11]
Supply Voltage (V)	1.2	3.3	1.2	1.5
Power (µW)	151	342	295	569
Technology (nm)	65	500	130	130
DC Gain(dB)	87	76	74	90
Bandwidth(MHz)	250	100	173	475
Start-up Circuit	Yes	No	No	No
Latch up Problem	No	No	Yes	Yes

Table -I shows the transistor sizes used in the design. Table-II shows the performance comparison of the proposed design with the recently published folded Cascode opamps. Table-II reveals that the present design is the only design which used start-up circuit to bring the circuit out of latch-up issue, whereas [4] also has no latch-up issue but it's power consumption is higher.

Conclusion: A hidden positive feedback and subtle start-up issues in a fully differential folded cascode has been discussed. This start-up issue could affect reliability of the circuit in the mass production. Many of the previous implementations hasn't considered this and some researchers addressed this issued by increasing the power dissipation. In this paper a start-up circuit has been added to the opamp to improve robustness without increasing power consumption. A Monte Carlo simulation performed to demonstrate the start-up failures, without start-up circuit shows 27 runs were not starting out of 1000 runs, whereas with the proposed solution had no failures from the same number of runs.

R. Nagulapalli, K. Hayatleh, S. Barker, B. Yassine, S. Zourob, S. Raparthy, N. Yassine
(*Faculty of Technology, Design and Environment, Oxford Brookes University, Wheatley Campus, Oxford, OX33 1HX, UK)*
E-mail: khayatleh@brookes.ac.uk

References

1.A.-J. Annema, "Analog circuits in ultra-deep-submicron CMOS", *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 132-143, Jan. 2005.
2. K. Bult, "The effect of technology scaling on power dissipation in analog circuits" in Analog Circuit Design, New York:Springer-Verlag, 2006.
3. W.M. Sansen, Analog Design Essentials, Springer-Verlag, 2006, ISBN 978-0-387-25746-4.
4. A. K. Gupta, V. Dhanasekaran, K. Soundarapandian, E. Sanchez-Sinencio, "Multipath common-mode feedback scheme suitable for high-frequency two-stage amplifiers", *Electron. Lett.*, vol. 42, no. 9, pp. 499-500, Apr. 2006.
5. A. Tauro, C. Marzocca, C. T. Francesco, A. Di Giandomenico, "common-mode stability in fully differential voltage feedback CMOS amplifiers", *Proc. 10th IEEE Int. Conf. Electron. Circuits Syst. ICECS'03*, vol. 1, pp. 288-291, 2003-Dec.
6. Joydeep Basu, Pradip Mandal, "Effect of Switched-Capacitor CMFB on the Gain of Fully Differential Op-Amp for Design of Integrators", *Circuits and Systems (ISCAS) 2018 IEEE International Symposium on*, pp. 1-5, 2018, ISSN 2379-447X.
7. S. Kumaravel, B. Venkataramani, S. Rishi, V. Sri Vijay, B. Shailendra, "An enhanced folded cascode OTA with push pull input stage", *Systems Signals and Devices (SSD) 2012 9th International Multi-Conference on*, pp. 1-6, 2012.
8. T. V. Prasula, D. Meganathan, "Design and simulation of low power high gain and high bandwidth recycling folded cascode OTA", Signal Processing Communication and Networking (ICSCN) 2017 Fourth International Conference on, pp. 1-6, 2017.
9. M. Akbari, "Single-stage fully recycling folded cascode OTA for switched-capacitor circuits", *ELECTRONICS LETTERS*, vol. 51, no. 13, pp. 977-979, June 2015.
10. A. D. Sundararajan, S. M. Rezaul Hasan, "Quadruply Split Cross-Driven Doubly Recycled-Doubling Recycled Folded Cascode for Microsensor Instrumentation Amplifiers", *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 63, no. 6, pp. 543-547, June 2016.
11. S. Zhang, Z. Zhu, H. Zhang, Z. Xiong, Q. Li, "A 90-dB DC gain high-speed nested gain-boosted folded-cascode opamp", *2015 11th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, pp. 357-360, 2015.
12. A. Boni, "Op-amps and start-up circuits for CMOS bandgap references with near 1-V supply", *IEEE J. Solid-State Circuits*, vol. 37, no. 10, pp. 1339-1343, Oct. 2002.
13. P.G.A. Jespers, B. Murmann, "Calculation of MOSFET Distortion Using the Transconductance-to-Current Ratio (g_m/I_D)", *Proc. ISCAS2015*, pp. 529-532, 2015.

14. R. Nagulapalli, K. Hayatleh, S. Barker, S. Zourob, N. Yassine, Sriadibhatla Sridevi, "A Microwatt Low Voltage Bandgap Reference for Bio-medical Applications", Recent Advances in Electronics and Communication Technology (ICRAECT) 2017 International Conference on, pp. 61-65, 2017.
15. K. R. Lakshmikumar, R. A. Hadaway, M. A. Copeland, "Characterization and modeling of mismatch in MOS transistors for precision analog design", *IEEE J. Solid-State Circuits*, vol. 21, pp. 1057-1066, Dec. 1986.