# Novel Techniques for Memristive Multifunction Logic Design

Xiaohan Yang, Adedotun Adeyemo, Anu Bala, Abusaleh Jabir
Department of Computing & Communication Technologies, Oxford Brookes University, Oxford, UK
E-mail:{15058456, 13121679, 15057719, ajabir}@brookes.ac.uk

***Abstract*—We present novel techniques for realising reliable low overhead logic functions and more complex systems based on the switching characteristics of memristors. Firstly, we show that memristive circuits have inherent properties for realising multiple valued MIN-MAX operations over the post algebra. We then present an efficient hybrid 1T-4M logic architecture for dual XOR/AND and XNOR/OR functionality, which can be seamlessly integrated with the existing CMOS technology. Although memristors are usually considered to operate at lower frequencies, however, recent advances in technology show their potentiality at high frequencies. To this end, we also explore the effects of high frequencies on their performance and thereby propose reliable high frequency design techniques based on our 1T-4M architectures. Experimental results, based on the design of full adders and multipliers over GF, show that the proposed designs require significantly lower power and overhead while maintaining reliable performance at low as well as at high frequencies compared to the existing techniques.**

***keywords*—** *Memristor; Memristive multifunction logic architecture; XOR gate; AND gate; OR gate; MIN-MAX post algebra; Memristive full adder; Memristive Galois Field multiplier; Physical Unclonable Function.*

## I. Introduction

Metal Oxide Semiconductor (MOS) Transistor-based chips are currently being limited by scaling difficulties and parasitic capacitance. Therefore, chip manufacturers are beginning to invest huge resources in order to explore alternative technologies for the evolution of computing devices. A memristor (short for 'memory-resistor'), a two terminal nanoscale electronic device, is a highly promising technology as an alternative. These devices, first theorised by Leon Chua in 1971, represent the missing link between charge ($q$) and flux ($\varphi$). A memristor represents data as resistance and it retains its previous resistance value after power has been removed, thereby remaining non-volatile [1], [2].

Since Hewlett-Packard fabricated the first physical memristive device based on titanium dioxide ($TiO_2$) in 2008 [2] (Fig. 1(a)), there has been increasing interests in different aspects of memristor applications. To this end, memristors have been applied in areas such as high density memory design [3], [4], neuromorphic systems [5], [6], secure and crypto (e.g. Physical Unclonable Functions (PUF) etc.) systems [7], [8], and logic design [7], [9]–[13]. It can be scaled to very small geometries and can be fabricated in layer upon layer, thereby providing a 3D structure for memristor chips.

Memristors can also be interfaced with the existing CMOS technology, owing to the fact that they both share similar fabrication properties [14]. The ability to fabricate chips in 3D in this fashion can help eliminate a key short coming of the CMOS technology, which suffers from the difficulties associated with 3D fabrication [15]. Hence, these types of interfacing allows 3D fabrication of hybrid memristor-CMOS designs, where the CMOS can be fabricated along with the bottom layer and the memristors are stacked over the CMOS layer [16], [17].

Most of the techniques for designing logic circuits with memristors require multiple sequential steps (clock cycles) and complex control logic to realise even the simplest logic function [9], [10], [13]. While there are some existing work on single cycle operation, these techniques fail to operate with realistic resistance values and also require power comparable to CMOS designs [7], [12]. To this end, firstly we propose a purely memristive logic architecture, consisting of only 4 memristors, for realising the XOR and inversion functions. This architecture can operate within a single clock cycle. Then we extend this architecture with just one transistor for seamless integration with the CMOS technology, thereby resulting in a hybrid 1T-4M architecture with dual XOR/AND and XNOR/OR functionality.

Based on the technological advances thus far, some of the materials considered for fabrication of memristors limit their operation to relatively lower frequencies. However, recent technological advances are seeing memristors operating at much higher frequencies [18]. This paper also explores this aspect and proposes parametric selection in their compact modelling to enable the devices to work at higher frequencies.

As we know, the CMOS technology suffers from significant parasitic capacitance, which reduces their reliability at high frequencies [19]–[21]. To circumvent this problem, one of our design objectives is to reduce the total number of transistors in the CMOS layer of our hybrid designs. This not only helps to enhance reliability at higher frequencies, but it also frees up chip area in the CMOS layer, which can only grow along the XY-axis, where additional CMOS exclusive functionality can be incorporated.

One of the key difficulties with traditional CMOS technology is its lack of ability for realising multiple valued logic (MVL). MVL has many applications, e.g. for memory and field programmable array designs, redundant number systems, etc. MVL can also help reduce interconnections on and off chip [22]. We show that certain configurations of memristors allow very efficient and simple realisation of MVL as MIN-MAX post algebra.

This paper is organised as follows. The basic structure of the memristor and the existing memristive logic architectures are reviewed in Section II. In Section III, we show that

memristors have inherent properties for realising operations over MIN-MAX post algebra. In this section, we also propose a one transistor and four memristors (1T-4M) multifunction logic architecture which can be seamlessly integrated with the CMOS technology. We analyse the effects of frequencies on the physical parameters of memristors in Section IV, thereby propose parametric selections in the memristive models for high frequency operations. In Section V, we show with the help of more complex systems that the proposed architecture can result in highly compact, low power, and reliable systems capable of operating at low as well as high frequencies. We have tested our designs exhaustively. Section VI presents the experimental results. Finally, the paper is concluded in Section VII.

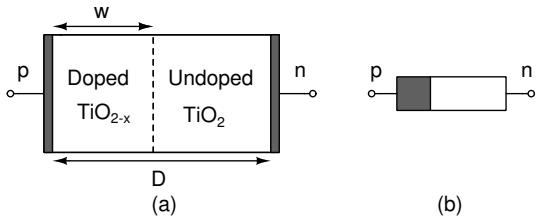



Fig. 1. Memristor: (a) Structure of the linear ion drift model; (b) Symbol of the single memristor.

## II. Background

In this section we provide a brief review of memristors and existing memristive logic architectures.

### A. Memristor

One of the most widely used technologies for fabricating memristive devices are based on oxides such as $NiO$, $TiO_x$, $HfO_x$ and $SiO_x$ [2], [18]. As an example, a simplified diagram of a $TiO_x$ based memristor is shown in Fig. 1(a). It is composed of a heavily doped $TiO_{2-x}$ layer with oxygen vacancies, placed above a zero doped $TiO_2$ layer and sandwiched between a pair of metallic electrodes. Here, $D$ is the width of the device and $w$ is the width of the doped region. $w$ acts as the state variable which depends on the previously applied voltage. The symbol of memristor is illustrated in Fig. 1(b), where p and n represent the positive and the negative terminals respectively.

When a positive voltage is applied to the p-terminal (and a negative voltage is applied to the n-terminal) of this device, the oxygen vacancies, which constitute positive charges drift into the zero doped region. It increases the width $w$ of the $TiO_{2-x}$ layer. This results in the device switching to a low resistance ($R_{on}$) state.

However, when a negative voltage is applied to the p-terminal (and positive voltage is applied to the n-terminal) the oxygen vacancies are attracted to the p-terminal. This results in the $TiO_2$ layer $D-w(t)$ widening and $TiO_{2-x}$ layer $w(t)$ decreasing. Hence, the device switches to a high resistance ($R_{off}$) state.

In contrast, when there is no voltage applied to either terminal, the boundary between the two titanium dioxide layers freezes. This allows the memristor to retain its previous state.

The memristance and the state variable of the basic memristor are related as follows [2]:

$$M(t) = R_{on}\frac{w(t)}{D} + R_{off}\left(\frac{1-w(t)}{D}\right), \quad (1)$$

$$\frac{dw}{dt} = \left(\frac{\mu_n R_{on}}{D}\right) i(t), \quad (2)$$

where, $R_{off}$ is the resistance of the $TiO_{2-x}$ layer (undoped region) and $R_{on}$ is the resistance of the $TiO_2$ layer (doped region). In Eq. (2), $\mu_n$ represents the average ion mobility. Fig. 2 shows the voltage-current characteristics of this device and the switching behaviour between $R_{on}$ and $R_{off}$. This figure clearly shows hysteresis, which is the key characteristics of a memory device.

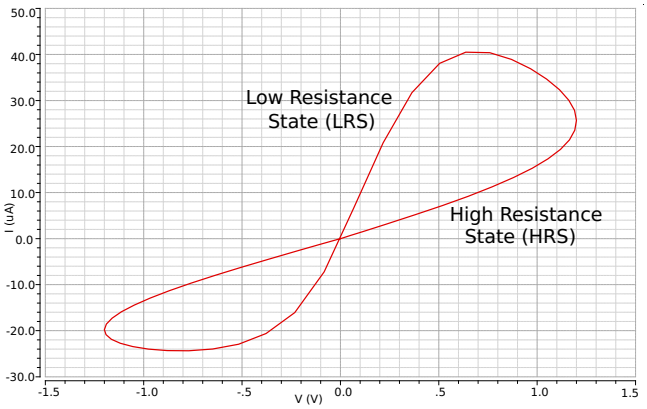
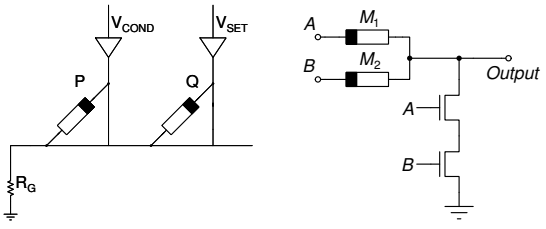



Fig. 2. Memristor voltage-current characteristics.

### B. Existing Memristive Logic Architecture

One of the earliest memristive logic architectures is the IMPLY logic function, which could be implemented as a memristor-based crossbar array [9]. Fig. 3(a) shows the basic IMPLY logic structure, where the two memristors $P$ and $Q$ are connected by the same horizontal wire with different voltages $V_{COND}$ and $V_{SET}$ applied simultaneously. Here the amplitude of $V_{COND}$ is smaller than the threshold voltage of the memristor, which prevents the device $P$ from switching to the previous state. The initial resistance of $P$ and $Q$ are the inputs of the logic gate. After applying two different voltages, $V_{COND}$ and $V_{SET}$, the output of the logic gate is the final changed resistance of the memristor $Q$. A simple IMPLY NAND gate in [9] requires three sequential steps.




(a) Basic IMPLY logic gate [9]. (b) Bufferless 2T-2M XOR gate [7].

Fig. 3. Existing memristive logic architectures.

Another crossbar based memristive logic architecture is the MAGIC logic gate [10]. All the basic boolean functions can be realised by this technique.

In contrast to the CMOS logic, both of these techniques use different resistances as the logic state and require multiple clock cycles to execute a single logic computation. These implementations also require that the memristors be initialised to a known state which could complicate the control circuit. All of these factors make it difficult to integrate with the existing CMOS technology. Both of the above techniques suffer from leakage current effect, known as the "sneak path" effect, which is common in memristive crossbar memory architectures [23]. The "sneak path" effect is the leakage current sneaking through the undesired cells with smaller resistances which is data dependent. These resistances cause overlapping of the two regions of the '0' and '1', which significantly reduce the noise margin (reliability). Hence, this deteriorates the accuracy of the read operation in crossbar architectures [24].

The technique of [13] proposed a hybrid memristive XOR function block with one memristor and four transistors. In this block, apart from the two normal inputs as conventional logic gates have, a third input is added as the control signal for controlling the read and write operations. The resistance of the memristor is the output of this block. Again, this technique requires multiple sequencial steps.

Unlike the previous techniques, Memristor Ratioed Logic (MRL) architecture [11] is based on the output voltage as the logic state. It uses the programmable resistance of memristive device to ensure that the circuit operates like a voltage divider for realising the Boolean OR and AND functions as shown in Fig. 4(a) and Fig. 4(b) respectively. In this diagram $a$ and $b$ are the two inputs and $V_{\rm x}$ and $V_{\rm y}$ are the OR operation and AND operations respectively. This MRL technique is capable of operating the logic computation within a single clock cycle. However deriving the Boolean 'NOT' operation by the purely memristive device is challenging with this technique. To extend this to more logic gates, e.g. NAND/NOR, a CMOS inverter is applied as 'NOT' operation combined with the MRL OR/AND logic.

The technique of [12] proposed a bufferless 4-transistor and 6-memristor (4T-6M) hybrid memristive XOR gate by using the MRL AND and OR gates and CMOS inverters based on the expression $A \oplus B = (A \wedge \overline{B}) \vee (\overline{A} \wedge B)$ directly. The area complexity of this technique is higher than pure CMOS XOR implementations [25], because it requires ten elements whereas the CMOS design requires six elements for bufferless design (Fig. 13).

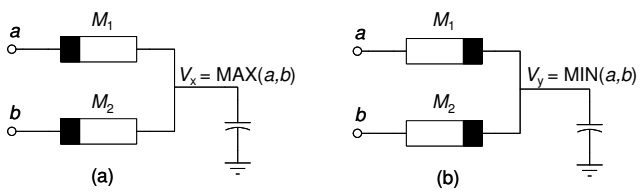



Fig. 4. Memristive MIN-MAX (AND-OR) functionality; (a) OR/MAX operation, (b) AND/MIN operation.

Based on the MRL OR gate (Fig. 4(a)), the technique of [7] proposed a hybrid memristive XOR architecture as shown in Fig. 3(b). It consists of two memristors ($M_1$ and $M_2$), and a pair of pull-down NMOS transistors. When both of the inputs $A$ and $B$ are equal to logic 1, the two transistors pull down the voltage appearing at the output to ground. This reduces the output to $\geq 0.2$V, where as it should be $\approx 0$V. This happens since the two NMOS transistors are connected in series, which results in their drain-to-source saturation voltage to be $V_{\rm DS} + V_{\rm DS} \geq 0.2$V when both of the inputs to the XOR gate are at logic 1. This may be too high to switch off a device connected in the following stages, especially with smaller technology nodes. This technique requires 2T-6M and 2T-4M elements for fully buffered XOR and XNOR functionality respectively. Additionally, it inherently requires memristors with very high $R_{\rm on}$ and even higher $R_{\rm off}$ to keep the transistors properly biased. This has the effect of slowing down any design owing to very large $RC$ time constants.

## III. Proposed Memristive Logic Architecture

In this section, we propose a 1T-4M multifunction logic architecture which can be seamlessly integrated with the CMOS technology. First, for completeness, we show that the MRL architecture naturally exhibits multiple valued MIN-MAX functions over post algebra [26].

### A. MIN-MAX Functionality

We have the following regarding the MIN-MAX functionality of MRL.

*Theorem 1:* The MRL in Fig. 4(a) realises the MAX operation and that in Fig. 4(b) realises the MIN operation in post algebra.

**Proof:** The proof follows by noting the voltage drops across the memristors for each input combination. [QED]

Theorem 1 reduces to the following for two valued logic.

*Corollary 1.1:* The MRL in Fig. 4(a) becomes an OR gate and that in Fig. 4(b) becomes an AND gate for two valued logic.

**Proof:** Follows trivially. [QED]

### B. Memristive XOR and Inversion Functionality

Most existing techniques for realising logic functions require multiple clock cycles to operate [9], [10], [13], and some require a hybrid of memristors and CMOS devices [7], [12]. Considering the merits and the demerits of these approaches, we propose a purely memristive XOR architecture as shown in Fig. 5(a). Fig. 5(b) shows the symbol for this architecture, which is used in the rest of the paper.

The purely memristive XOR architecture in Fig. 5(a) consists of four memristors $M_1$, $M_2$, $M_3$ and $M_4$. Here, $M_1$ and $M_3$ are connected for logical AND or MIN operation. $M_2$ and $M_4$ are connected for logical OR or MAX operation. The voltage difference between $V_{\rm L1}$ and $V_{\rm L2}$ behaves like XOR operation as shown in Table I. In Table I, the logical behaviour of the purely memristive XOR circuit is based on whether or not current flows from $V_{\rm L1}$ to $V_{\rm L2}$ through

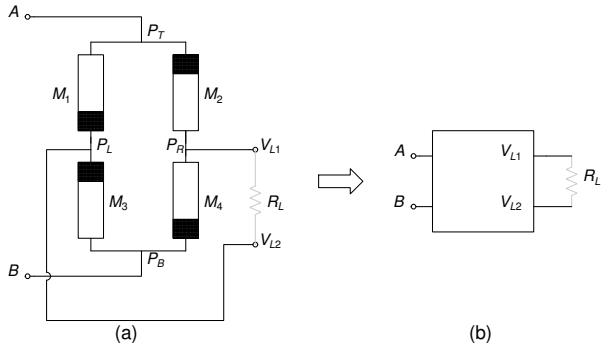



Fig. 5. Memristive XOR functionality. (a) Purely memristive XOR functionality, (b) Symbol used in the rest of the paper.

the load resistance $R_L$. In this table $V_1$ ($>$ the memristor threshold voltate $V_{\text{on}}$) is assumed to be equivalent to $V_{\text{DD}}$ in CMOS logic and represents the ON-state voltage, i.e. logic 1. Correctness of this architecture is summarised in Theorem 2.

*Theorem 2:* The pure memristor circuit in Fig. 5(a) realises the XOR functionality depicted in Table I.

**Proof:** The proof follows by considering each input combination and noting the high and low resistance states of each memristors. [QED]

These operations can take place in the same clock cycle as the inputs. Hence, the circuit in Fig. 5 exhibits XOR functionality in Table I in a single cycle. We note that $\forall A,B \in \{0,V_1\}$, the following are true for the circuit in Fig. 5.

$$V_{L1} = A \vee B \tag{3}$$
$$V_{L2} = A \wedge B \tag{4}$$
$$V_{L1} \geq V_{L2}. \tag{5}$$

Fig. 6 presents the output of the architecture in Fig. 5 for all the input combinations (i.e. 11, 10 01, 00). If we interpret the current flowing from $V_{\text{L1}}$ to $V_{\text{L2}}$ as logic 1, and the absence of this current as logic 0, then clearly this is XOR functionality.

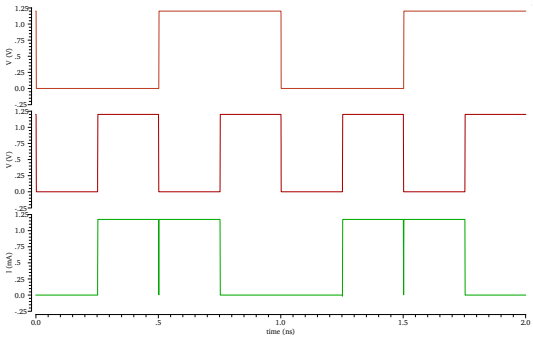


Fig. 6. Purely memristive XOR functionality. The top two signals represent the two input voltages and the bottom signal is the current which flows into load $R_{\text{L}}$.

Our proposed architecture trivially allows pure memristive inversion via XOR operation in a single cycle. For example, in Fig. 5(a), if we set $A = 1$ (i.e. $A = V_1$), then the output will correspond to the inverse of $B$, as shown by Rows 3 and 4 in Table I, i.e. $\overline{B} = 1 \oplus B$. Hence, we have the following.

TABLE I
PURE MEMRISTIVE XOR FUNCTIONALITY.

| Row | $A$ | $B$ | Output |
|---|---|---|---|
| 1 | 0 | 0 | $V_{L1} - V_{L2} = 0$V. $\Longrightarrow$ No current flows from $V_{L1}$ to $V_{L2}$. $\Longrightarrow$ Logic 0. |
| 2 | 0 | $V_1$ | $V_{L1} - V_{L2} \approx V_1$V. $\Longrightarrow$ Current flows from $V_{L1}$ to $V_{L2}$. $\Longrightarrow$ Logic 1. |
| 3 | $V_1$ | 0 | $V_{L1} - V_{L2} \approx V_1$V. $\Longrightarrow$ Current flows from $V_{L1}$ to $V_{L2}$. $\Longrightarrow$ Logic 1. |
| 4 | $V_1$ | $V_1$ | $V_{L1} - V_{L2} \approx 0$V. $\Longrightarrow$ No current flows from $V_{L1}$ to $V_{L2}$. $\Longrightarrow$ Logic 0. |

*Corollary 2.1:* The pure memristive logic architecture in Fig. 5(a), which realises the XOR functionality depicted in Table I, becomes an inverter when either of its inputs $A$ or $B$ is assigned logic 1 ($V_1$).

**Proof:** Follows trivially from Table I. [QED]

### C. 1T-4M Hybrid CMOS-Memristive Logic Architecture

In Section III-B, we proposed a novel pure memristive XOR logic architecture. Although this architecture works as an XOR gate, however, we interpreted the output logic value based on whether or not the current is flowing from $V_{\text{L1}}$ to $V_{\text{L2}}$. Clearly, this is not directly compatible with the existing CMOS technology. Our aim is to integrated our system so that it works seamlessly with the existing CMOS technology, and not replace it. To this end, we present in this section a highly efficient way of integrating our pure memristive architecture with the CMOS technology by using only a single MOS transistor (MOST). This results in a 1-transistor 4-memristor (1T-4M) architecture as shown in Fig. 7(a) and (c). By keeping the number of MOST to only one, we are also able to maintain reliable performance at higher frequencies, when parasitic capacitance begins to degrade performance.

The logic architectures for our proposed 1T-4M XOR/AND and XNOR/OR dual functionality appears in Fig. 7(a) and Fig. 7(c) respectively. Compared with existing memristive logic techniques (e.g. IMPLY and MAGIC), the 1T-4M architecture seamlessly integrates with CMOS technology without requiring extra control circuitry and the logic computation also finishes within one clock cycle.

For our designs, we assume that the NMOST and the PMOST operate in the saturation and cut off regions. We now prove the correctness of the proposed architectures.

First we have the following.

*Lemma 1:* The NMOST in Fig. 7(a) and the PMOST in Fig. 7(c) realise the following logic operations respectively.

$$V_{\text{XOR}} = V_{L1} \wedge \overline{V_{L2}} \tag{6}$$
$$V_{\text{XNOR}} = \overline{V_{L1}} \vee V_{L2}. \tag{7}$$

**Proof:** The proof follows by firstly noting Eq. (5). The only time $V_{\text{XOR}}$ in Fig. 7(a) is at logic 1 ($\approx V_1$V) is when $V_{L1} \approx V_1$V and $V_{L2} \approx 0$V. From Table I, clearly this happens

when either $A = V_1$ and $B = 0$ or $A = 0$ and $B = V_1$. At all other times either $V_{\rm XOR} = 0$ ($V_{L1} = V_{L2} = 0$) or the NMOST goes into saturation and $V_{\rm XOR} \approx 0.1V$ ($V_{L1} = V_{L2} \approx V_1$V). Again, from Table I this only happens when either $A = 0$ and $B = 0$ (i.e. no current flows in the circuit, thus resulting in $V_{\rm XOR} = 0$) or $A = V_1$ and $B = V_1$ (i.e. this drives the NMOST into saturation).

Similarly, in Fig. 7(c) the only time $V_{\rm XNOR} \approx 0$V is when $V_{L1} \approx V_1$V and $V_{L2} \approx 0$V. At all other times $V_{\rm XNOR} \approx V_1$V. Hence the proof follows. [QED]

We now show that our proposed architecture realises XOR/AND and XNOR/OR dual functionality.

*Theorem 3:* The 1T-4M multifunctional logic architecture in Fig. 7(a) realises the XOR/AND dual functionality and that in Fig. 7(c) realises the XNOR/OR dual functionality.

**Proof:** To prove that the circuit in Fig. 7(a) realises the XOR operation, we substitute $V_{L1}$ and $V_{L2}$ from Eq. (3) and Eq. (4) into Eq. (6) respectively, which yields

$$V_{\rm XOR} = V_{L1} \wedge \overline{V_{L2}} = (A \vee B) \wedge (\overline{A \wedge B}) = A \oplus B.$$

Now, regarding Fig. 7(c), Eq. (7) is merely the inverse of Eq. (6), i.e. $V_{\rm XNOR} = \overline{V_{\rm XOR}} = 1 \oplus A \oplus B$.

To show that the circuits also exhibit AND and OR operations while realising XOR and XNOR operations, firstly we note that according to Eq. (4) and Eq. (3), the circuits in Fig. 7(a) and (c) trivially realise the AND and OR operations at the gates of the NMOST and PMOST respectively. Since, neither gates of the NMOST and PMOST draw any current owing to gate isolation, therefore, this architecture realises the dual functionality of $V_{\rm AND}$ with $V_{\rm XOR}$ and $V_{\rm OR}$ with $V_{\rm XNOR}$ simultaneously as shown in Fig. 7(a) and (c) respectively.

Hence, the proof follows. [QED]

To ensure that the NMOST operates in saturation and cut off regions, the following design rules must be satisfied:

$$\begin{aligned} I_{D,sat} &= \frac{V_{\rm RD}}{R_{\rm D} + (R_{\rm on} || R_{\rm on})} = \frac{V_{\rm DD} - V_{DS,sat}}{R_{\rm D} + (R_{\rm on} || R_{\rm on})} \\ \implies R_{\rm D} + \frac{R_{\rm on}}{2} &= \frac{V_{\rm DD} - V_{DS,sat}}{I_{D,sat}} \end{aligned} \tag{8}$$

where, $V_{\rm RD}$ is the voltage across $R_{\rm D}$ and $I_{D,sat}$ is the NMOST saturation current. Hence, we have,

$$V_{\rm DD}\left(\frac{R_{\rm on}}{R_{\rm on} + R_{\rm off}}\right) < V_{\rm TH} \tag{9}$$

where, $V_{\rm TH}$ is the threshold voltage of the NMOST.

Similar design rule applies to the PMOST in Fig. 7(c).

Our 1T-4M architecture employs only one transistor, thereby ensuring that the output is $\approx 0.1$V when the transistor saturates, e.g. when both of the inputs are at logic 1. In contrast, the technique of [7] cannot ensure output voltage any less than 0.2V when both of its output transistors saturates. This larger voltage can be a critical factor, especially when driving very small technology nodes (Section II).

We have tested with several memristor models [27], [28], and the designs worked correctly for a range of $R_{\rm on}$ and $R_{\rm off}$. For low $R_{\rm on}$ a higher $R_{\rm D}$ maybe necessary to bias the transistor properly, while for higher $R_{\rm on}$, $R_{\rm D}$ may be eliminated. We demonstrated the performance of Fig. 7(a) by choosing different values of $R_{\rm D}$ as shown in Fig. 8. It is clearly shown that the range of $R_{\rm D}$ ($15k\Omega - 24k\Omega$) which is selected based on Eq. (8) and Eq. (9) provides the accurate performance, while with the smaller $R_{\rm D}$ e.g. $50\Omega - 800\Omega$, the transistor cannot be biased properly. In contrast to this, the technique of [7] (Fig. 3(b)) can only operate with very high $R_{\rm on}$ and $R_{\rm off}$ (Section II) thereby limiting its applications to certain types of memrisotrs and to low frequencies only.

It should be noted that the 1T-4M XOR/AND architecture in Fig. 7(a) is more power efficient compared to the 1T-4M XNOR/OR architectures in Fig. 7(c). This is because the former architecture is not directly drawing power from the supply voltage ($V_{\rm DD}$), whereas the latter architecture is.

Both of these circuits in Fig. 7(a) and (c) are weak, i.e. they may not guarantee a full voltage swing with sufficient current drive for a following stage. A two-transistor CMOS inverter buffer can be added at the outputs for both 1T-4M XOR and XNOR gates to obtain full-voltage swings as shown in figures (b) and (d). This yields 3T-4M 'strong' XOR/XNOR gate as compared to the 1T-4M bufferless XOR/XNOR gates. However, inline with the reasons stated in the previous paragraph, the 3T-4M fully buffered XNOR gate in figure (b), which draws power directly from the power supply only at the buffer stage, is more power efficient compared to the XOR gate in figure (d), which draws power in the pre-buffer stage also.

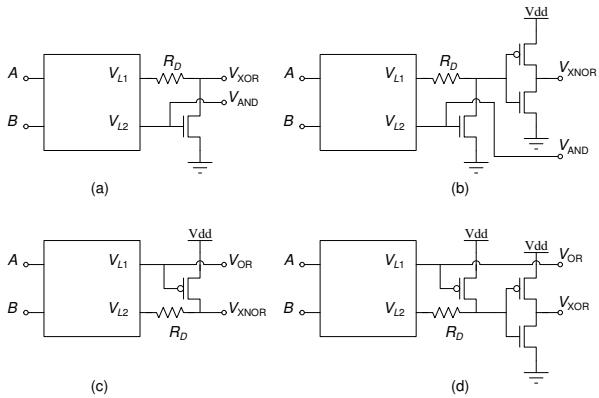



Fig. 7. Memristive XOR and XNOR gates with dual functionality. (a) 1T-4M bufferless XOR/AND dual functionality, (b) 3T-4M fully buffered XNOR functionality, (c) 1T-4M bufferless XNOR/OR dual functionality and (d) 3T-4M fully buffered XOR functionality.

## IV. High Frequency Operations

Memristors are usually considered to operate at lower frequencies owing to the limitations of the materials and the way they are used for their fabrication. However, low frequency ultra low power electronic device have critical applications, e.g. in medical electronics [29]–[31]. To this end, the proposed technique is well suited for such applications owing to their low power requirements (Table II and Section V). However, this is a highly evolving area and new materials are investigated for fabrication of more efficient and better performing memristors, especially at high frequencies.

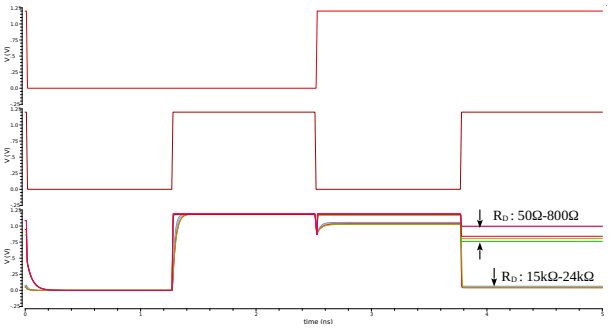



Fig. 8. The performance of XOR architecture affected by a selection of the load resistor $R_{\mathrm{D}}$. Here, $R_{\mathrm{off}} = 80k\Omega, R_{\mathrm{on}} = 500\Omega$. The top two signals represent the two input voltages and the bottom singals are the output $V_{\mathrm{XOR}}$ of Fig. 7(a) with different values of $R_{\mathrm{D}}$.

For example [18] presented a novel $SiO_{\mathrm{x}}$ based memristor with much better frequency characteristics, which also allows better integration with the CMOS technology. In line with these, we present the effects of high frequency on memristor models and the modification necessary for high frequency operations.

Various memristor models have been proposed in literature, e.g. [27], [28], [32]–[34]. However, not all of these models are suitable for logic design. The model proposed in [28], which our models and designs are based on, is a flexible memristor model that uses voltage as a threshold parameter and it is also based on modified Simmons tunnel barrier model [34], owing to the fact that the latter model is applicable only to specific materials and hence cannot be directly generalised.

To analyse the effects of frequency on the performance of this model, we need to consider the derivative of the state variable $w$ as follows [28]:

$$\frac{dw(t)}{dt} = \begin{cases} k_{\mathrm{off}} \cdot (\frac{v(t)}{V_{\mathrm{off}}} - 1)^{\alpha_{\mathrm{off}}} \cdot f_{\mathrm{off}}(w), & 0 < V_{\mathrm{off}} < v \\ 0, & V_{\mathrm{on}} < v < V_{\mathrm{off}} \\ k_{\mathrm{on}} \cdot (\frac{v(t)}{V_{\mathrm{on}}} - 1)^{\alpha_{\mathrm{on}}} \cdot f_{\mathrm{on}}(w), & v < V_{\mathrm{on}} < 0 \end{cases} \tag{10}$$

where $k_{\mathrm{off}}$ (a positive number), $k_{\mathrm{on}}$ (a negative number), $\alpha_{\mathrm{on}}$ and $\alpha_{\mathrm{off}}$ are constants; and, $V_{\mathrm{off}}$ and $V_{\mathrm{on}}$ are voltage thresholds. Here, $k_{\mathrm{off}}$ and $k_{\mathrm{on}}$ are in meters per second, whereas $\alpha_{\mathrm{on}}$ and $\alpha_{\mathrm{off}}$ do not have any unit [28].

The $k$ and $\alpha$ parameters are fitting parameters which are directly related to the physical behviour of the materials used to fabricate the memristors, as shown in [28]. For example, for ferroelectric memristor, $k_{\mathrm{off}}$ and $k_{\mathrm{on}}$ are considered to be $10^{-4}$m/s and -30m/s respectively and the parameter $\alpha_{\mathrm{off}}$ and $\alpha_{\mathrm{on}}$ are considered to be 5, etc.

The functions $f_{\mathrm{off}}(w)$ and $f_{\mathrm{on}}(w)$ behave like a window function which constrains the state variable $w$ to bounds of the device as defined in [27]. This derivative of the state variable $\frac{dw(t)}{dt}$ indicates the rate of change of $w$ which in this case describes how rapidly the memristor could switch between low and high resistance states. Based on memristor characteristics and Eq. (10), the width $w$ is directly dependent on the parameter $k_{\mathrm{off}}$ ($k_{\mathrm{on}}$). Here, apart from the other parameters, $k_{\mathrm{off}}$ and $k_{\mathrm{on}}$ mainly influence the rate of change of the magnitude of $w$. Fig. 9 demonstrates the variation of the state variable $w$ for different applied values of $k_{\mathrm{off}}$, where the memristor is driven by a 20MHz sinusoidal input with 1.2V amplitude. When $k_{\mathrm{off}}$ is increased, the slope of $w$ becomes steeper, which results in the device switching rapidly to a high resistance state.

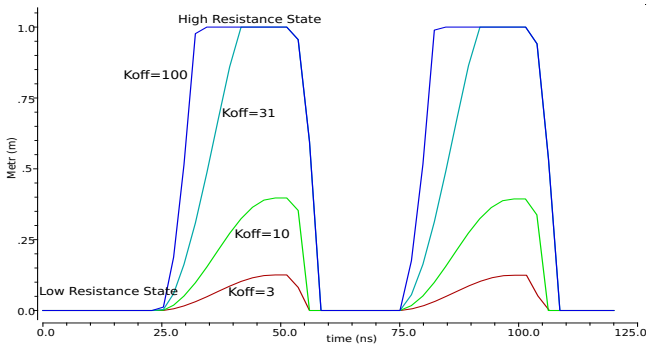



Fig. 9. Dynamic behaviour of state variable $w$ for a selection of the parameter $k_{\mathrm{off}}$. A 20MHz 1.2V sinusoidal voltage is applied in this simulation. Here, $R_{\mathrm{off}} = 80k\Omega, R_{\mathrm{on}} = 500\Omega$ and $k_{\mathrm{on}} = -200$m/s.

Similarly, when $|k_{\mathrm{on}}|$[1] is increased, the device quickly switches to a low resistance state as shown in Fig. 10. We also demonstrate this characteristic via applying more realistic stimulus such as square wave as shown in Fig. 11 and Fig. 12. The parameters $k_{\mathrm{off}}$ and $k_{\mathrm{on}}$ are fitting parameters which with correct values can be used to simulate the behaviour of a wide range of memristive devices with different materials. Hence, with the proper values of these parameters a memristor can also be modeled for operating at high frequencies, e.g. [18].

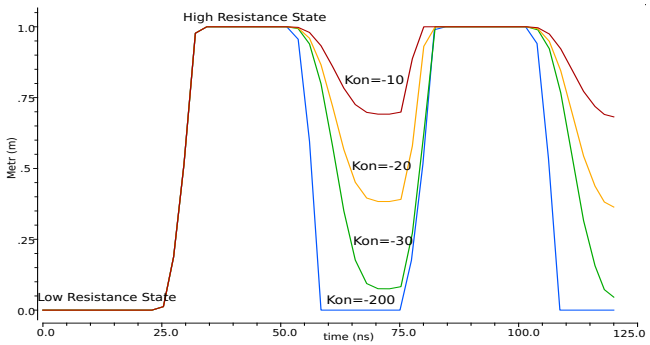



Fig. 10. Dynamic behaviour of state variable $w$ for a selection of the parameter $k_{\mathrm{on}}$. A 20MHz 1.2V sinusoidal voltage is applied in this simulation. Here, $R_{\mathrm{off}} = 80k\Omega, R_{\mathrm{on}} = 500\Omega$ and $k_{\mathrm{off}} = 100$m/s.

Based on these parametric selections, we compared the performance of the proposed architectures with other hybrid memristive logic designs, e.g. [7], at high frequencies. We used the same memristive model for all the designs for fairness. We also compared the performance of our designs with pure CMOS designs, e.g. in [25]. To this end, Table II presents the performance of our fully buffered 3T-4M XOR and XNOR gates at different frequencies as compared to (i) fully buffered 10T and 8T pure CMOS XOR (C-XOR) and

[1]The symbol $|x|$ represents the absolute value of a signed number $x$.

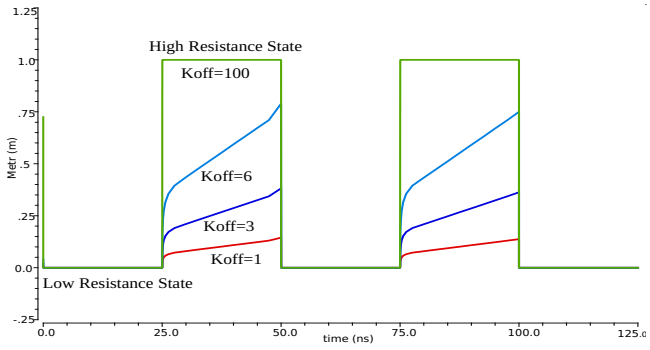



Fig. 11. Dynamic behaviour of state variable $w$ for a selection of the parameter $k_{\text{off}}$. A rectangular square wave of 20MHz with amplitude of 1.2V is applied in this simulation. Here, $R_{\text{off}} = 80k\Omega, R_{\text{on}} = 500\Omega$ and $k_{\text{on}} = -200$m/s.

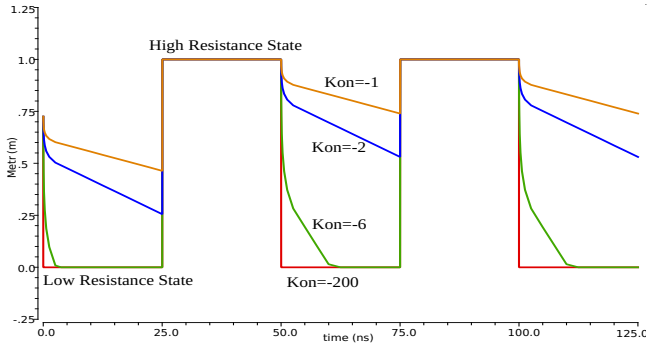



Fig. 12. Dynamic behaviour of state variable $w$ for a selection of the parameter $k_{\text{on}}$. A rectangular square wave of 20MHz with amplitude of 1.2V is applied in this simulation. Here, $R_{\text{off}} = 80k\Omega, R_{\text{on}} = 500\Omega$ and $k_{\text{off}} = 100$m/s.

XNOR (C-XNOR) gates [25], (ii) fully buffered AOI22 XOR and AOI22 XNOR gates [35], and (iii) fully buffered 6T-2M hybrid memristive XOR and 4T-2M XNOR gates proposed in [7].

Throughout the paper, we measured the average power drawn by the circuits as follows. The average power $P$ measured here is the energy $E$ consumed by the entire circuit divided by the simulation time as shown below:

$$E = \int_0^T V_{\text{DD}} \cdot i(t)dt \tag{11}$$

$$P = \frac{E}{T}, \tag{12}$$

where $V_{\text{DD}}$ is the supply voltage, $i(t)$ is the total instantaneous current drawn from $V_{\text{DD}}$ by a circuit at time $T$. $T$ is the simulation time.

The 10T/8T buffered CMOS XOR/XNOR gate constitutes a bufferless 6T stage, as shown in Fig. 13 [25]. The 6T-2M/4T-2M buffered hybrid memristive XOR/XNOR design constitutes a 2T-2M bufferless design as shown in Fig. 3(b) [7]. For the proposed 3T-4M XOR gate, $R_{\text{D}} = 24k\Omega$, $R_{\text{on}} = 500\Omega$ and $R_{\text{off}} = 40k\Omega$ are calculated based on Eq. (8) and Eq. (9). The same values of $R_{\text{on}}$ and $R_{\text{off}}$ are also considered for the design of the 6T-2M XOR gate [7]. The parameters $k_{\text{on}} = -200$m/s and $k_{\text{off}} = 50$m/s are selected based on the simulation results as shown in Fig. 9 and

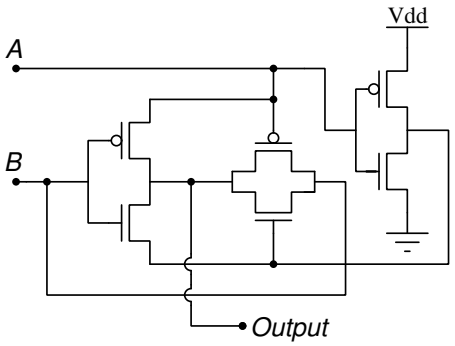



Fig. 13. Bufferless 6T CMOS XOR (C-XOR) gate [25].

TABLE II
PERFORMANCE ANALYSIS COMPARED TO EXISTING TECHNIQUES.

| Frequency → Architecture ↓ | 1GHz | | 2GHz | | 4GHz | | 8GHz | |
|---|---|---|---|---|---|---|---|---|
| | Power ($\mu$W) | Stat | Power ($\mu$W) | Stat | Power ($\mu$W) | Stat | Power ($\mu$W) | Stat |
| 3T-4M XOR | 14.38 | pass | 14.49 | Pass | 16.79 | Pass | 25.62 | Pass |
| 3T-4M XNOR | 1.71 | pass | 2.518 | Pass | 4.483 | Pass | 8.414 | Pass |
| 10T C-XOR [25] | 61.11 | pass | 67.93 | Pass | 72.01 | Fail | 76.57 | Fail |
| 8T C-XNOR [25] | 50.56 | pass | 54.55 | Pass | 56.50 | Fail | 59.78 | Fail |
| AOI22 XOR [35] | 7.32 | pass | 12.99 | Pass | 24.29 | Pass | 46.80 | Fail |
| AOI22 XNOR [35] | 6.077 | pass | 10.84 | Pass | 20.35 | Pass | 39.28 | Fail |
| 6T-2M XOR [7] | 19.14 | pass | – | Fail | – | Fail | – | Fail |
| 4T-2M XNOR [7] | 14.69 | pass | – | Fail | – | Fail | – | Fail |

Fig. 10. The values of the $k$ parameters which we considered in this paper are similar to those considered in [36]. As shown in [28], this appears to refer to Pt-Hf-Ti memristive devices [37].

Table II shows that our 3T-4M structure requires significantly less power than the 10T CMOS designs, while maintaining reliable performance even at high frequencies by comparing with the AOI22 designs.

For the 6T-2M hybrid structure, $R_{\text{on}}$ has to be high enough to bias the two NMOSTs which are connected in series as shown in Fig. 3(b). Hence, in this case, this circuit required $R_{\text{on}} = 30k\Omega$ and $R_{\text{off}} = 80k\Omega$. However, the 6T-2M hybrid structure was unable to reliably operate at frequencies higher than 1GHz for reasons explained in Section II and Section III-C. Additionally, our 3T-4M structure also outperformed the 6T-2M structure in terms of power requirement, with our 3T-4M XNOR gate requiring significanlty less power compared with the 4T-2M XNOR gate of [7].

Table II also shows that, clearly, the 10T/8T CMOS XOR/XNOR gate failed at 4GHz, and the AOI22 XOR/XNOR gate failed as frequencies are reaching 8GHz, whereas our 3T-4M gate reliably operated at frequencies of 8GHz or higher as shown in Fig. 14.

In Section V, we show that our multifunction memristive XOR/XNOR architecture offers compact and efficient design of more complex circuits.

## V. DESIGNING SYSTEMS

In this section, we demonstrate that our 3T-4M multifunction logic architecture can be used to design highly compact, reliable, and efficient systems. To this end, firstly

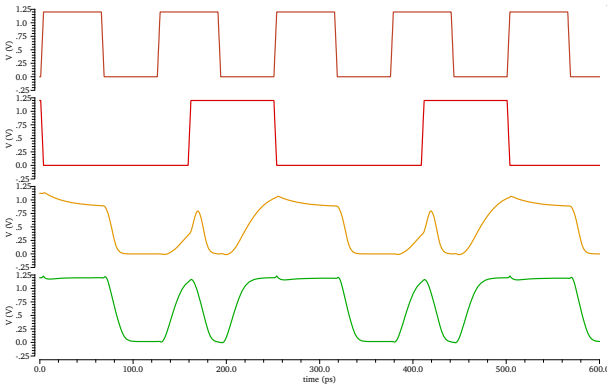



Fig. 14. Buffered XOR performance for 10T and 3T-4M XOR gate at 8GHz: top two signals are inputs; third: 10T CMOS XOR gate [25]; fourth: proposed 3T-4M XOR gate.

we consider a full adder design, and then we present the design of multipliers over the Galois Fields.

### A. Memristive Full Adder

A 2T-10M 'weak' full adder can be formed as shown in Fig. 15. This bufferless full adder mainly consists of two 1T-4M XOR/AND multifunction stages (Fig. 7(a)). The sum ($S$) and carry ($C_o$) outputs are formed as follows:

$$S = A \oplus B \oplus C_i \tag{13}$$

$$C_o = C_i(A \oplus B) \vee (A \wedge B) \tag{14}$$

In Eq. (14), the terms $A \wedge B$ and $C_i(A \oplus B)$ are shared from the first and second 1T-4M stages respectively.

The multifunction properties of the proposed architecture also permit highly compact fully buffered full adder designs. For instance, to obtain the sum output $S$, the output of a 3T-4M XNOR gate (Fig. 7(b)) can be fed into another 3T-4M XNOR stage, thus giving us

$$S = (1 \oplus A \oplus B) \oplus (1 \oplus C_i) = A \oplus B \oplus C_i.$$

The output $C_o$ can be formed by ORing the shared term $A \wedge B$ from the first 3T-4M XNOR stage with $C_i(A \oplus B)$ and then double inverting the output. In the term $C_i(A \oplus B)$, the term $A \oplus B$ is also a shared term from the first 3T-4M XNOR stage before the CMOS inverter. Hence, we only need two more memristors to simply form an AND gate. This yields the fully buffered 10T-12M structure as shown in Fig. 16.

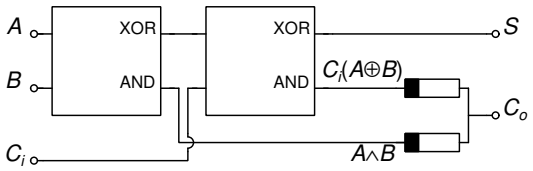



Fig. 15. 2T-10M 'weak' adder design.

For completeness, we have designed both bufferless and fully buffered full adders in all possible correct configurations of the proposed bufferless 1T-4M XOR/XNOR gates as well as the fully buffered 3T-4M XOR/XNOR gates. The

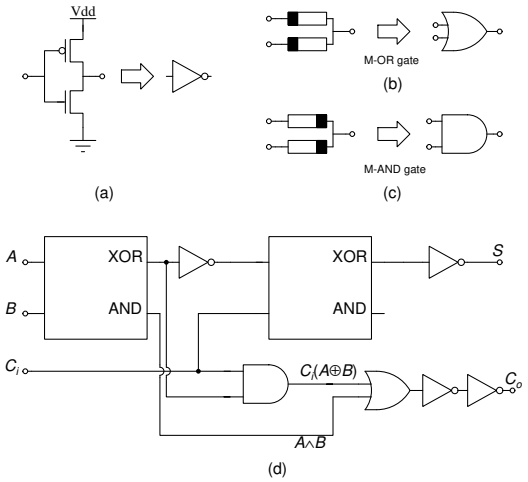



Fig. 16. 10T-12M fully buffered adder circuit; (a) CMOS inverter; (b) Memristive OR gate (M-OR); (c) Memristive AND gate (M-AND); (d) 10T-12M adder.

total number of elements for the bufferless designs varies from 12 to 16 elements, whereas the total number of elements for the fully buffered designs varies from 22 to 24 depending on how the XOR and XNOR stages were connected. Table III shows the results of the designs. In this table the columns 'Architecture', 'Unbuffered', and 'Buffered' represent which architecture combination we used, and whether the adder is unbuffered or fully buffered respectively. The columns 'Shared', 'Elem', and 'Tot' represent the shared terms, the total number of memristors and transistors used, and the total number of elements respectively. Table III clearly shows that the XOR-XOR architecture (Row-1) required the fewest number of elements. This design is also a significant improvement over the existing full adder designs e.g. 16T-18M [12] and 27T-2M [13].

TABLE III
FULL ADDER DESIGN WITH PROPOSED ARCHITECTURE.

| Architecture | Unbuffered | | | Buffered | | |
|---|---|---|---|---|---|---|
| | Shared | Elem | Tot | Shared | Elem | Tot |
| XOR-XOR | $A \wedge B$, $C(A \oplus B)$ | 2T-10M | 12 | $A \wedge B$, $A \oplus B$ | 10T-12M | 22 |
| XOR-XNOR | $A \wedge B$, $C(A \oplus B)$ | 4T-12M | 16 | $A \wedge B$, $A \oplus B$ | 12T-12M | 24 |
| XNOR-XOR | $C(A \oplus B)$ | 4T-12M | 16 | $C(A \oplus B)$ | 12T-12M | 24 |
| XNOR-XNOR | $A \vee B$ | 2T-14M | 16 | $A \vee B$/ $A \oplus B$ | 10T-14M | 24 |

### B. Memristive Galois Field Multiplier

The arithmetic operations over finite fields (or Galois fields), i.e. over the set GF($2^m$), where $m$ is a non zero positive integer, have critical applications in public-key cryptography systems and error-correcting codes among others [38]. Addition and multiplication are the two basic arithmetic operations over these fields. While an $m$-bit adder over GF($2^m$) only requires $m$ XOR gates working in parallel, multiplication is much more complex and requires a combination of many AND and XOR gates [39]. In this section, we present design methods for hybrid memristive polynomial

basis multipliers over GF($2^m$). We begin by showing a multiplier design over GF($2^2$) and extend this design over GF($2^4$).

*a) 2-bit Multiplier Over GF:* Let us assume that the two inputs of the 2-bit multiplier are $A=(a_1,a_0)$ and $B=(b_1,b_0)$. The polynomial representation of the elements over GF($2^2$) is $A(x)=a_1x+a_0$, and $B(x)=b_1x+b_0$. Here, '+' represents addition over GF, which is equivalent to the XOR operation (i.e. '$\oplus$') over GF(2). Then $A(x)\cdot B(x)=(a_1x+a_0)\cdot(b_1x+b_0)=a_1b_1x^2+(a_0b_1+a_1b_0)x+a_0b_0$. Here, the element $a_1b_1x^2$ with exponent greater than 1 is not in the field. Hence it needs to be reduced modulo the primitive polynomial, which in this case is $P(x)=x+1$. The final result is given as follows:

$$A(x)\cdot B(x) \mod P(x) = (a_0b_1+a_1b_0+a_1b_1)x+(a_0b_0+a_1b_1). \quad (15)$$

To simplify Eq. (15), we denote $C_0$, $C_1$..., $C_{m-1}$ to be the coefficients corresponding to the terms associated with $x^0$, $x^1$..., $x^{m-1}$ respectively. Then, Eq. (15) becomes

$$A(x)\cdot B(x) \mod P(x) = C_1x+C_0. \quad (16)$$

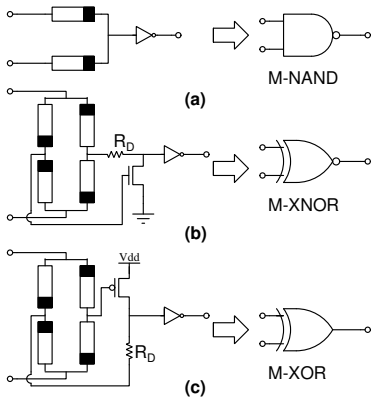



Fig. 17. Memristive logic symbol; (a) Memristive logic NAND gate; (b) Memristive logic XNOR gate; (c) Memristive logic XNOR gate

This 2-bit GF multiplier consists of four AND and three XOR gates based on Eq. (15). As we have shown in Section III-C and Table II, our 3T-4M XNOR gate is more power efficient compared to our 3T-4M XOR gate. Therefore, it is reasonable to replace as many XOR gates as possible with XNOR gates. To this end, we ensure reliable performance with low power by redesigning the circuit as follows:

- We use buffered memristive NAND (M-NAND) gates (Fig. 17(a)), instead of buffered AND gates. The buffered M-NAND gates require a single inverter, which is more power efficient compared to a buffered M-AND gate.
- We replace as many buffered 3T-4M XOR gates (Fig. 7(d)) as possible with our power efficient 3T-4M buffered XNOR gates (Fig. 7(b)).

Therefore, we modify Eq. (15) as follows to accommodate the above optimisation:

$$C_0=(a_1b_1\oplus 1)\oplus(a_0b_0\oplus 1)$$
$$C_1=\overline{(a_0b_1\oplus 1)\oplus(a_1b_0\oplus 1)}\oplus(a_1b_1\oplus 1). \quad (17)$$

The resulting design appears in Fig. 18.

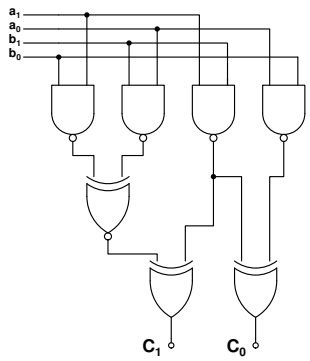



Fig. 18. Memristive GF($2^2$) Multiplier.

Although in this design we replaced only one XOR gate with a power efficient XNOR gate in Fig. 18, the number of XOR gates which can be replaced is much higher as the circuits are scaled up. We demonstrate this by designing a 4-bit multiplier over GF($2^4$) as follows.

*b) 4-bit Multiplier Over GF:* For designing a polynomial basis GF($2^4$) multiplier, we multiply the two inputs $A=(a_3,a_2,a_1,a_0)$ and $B=(b_3,b_2,b_1,b_0)$ and then modulo the result by a primitive polynomial, which in our case is $P(x)=x^4+x+1$. The final result appears in Eq. (18).

$$\begin{aligned}A(x)\cdot B(x) \mod P(x) = &(a_0b_3+a_1b_2+a_2b_1+a_3b_0+a_3b_3)x^3\\ &+(a_0b_2+a_1b_1+a_2b_0+a_2b_3+a_3b_2+a_3b_3)x^2\\ &+(a_0b_1+a_1b_0+a_1b_3+a_2b_2+a_2b_3+a_3b_1+a_3b_2)x\\ &+(a_0b_0+a_1b_3+a_2b_2+a_3b_1). \quad (18)\end{aligned}$$

This can be simplified as follows.

$$A(x)\cdot B(x) \mod P(x)=C_3x^3+C_2x^2+C_1x+C_0. \quad (19)$$

Now we replace all the AND gates with M-NAND gates and as many XOR gates as possible with M-XNOR gates. The new expression of each coefficient appears in the following:

$$C_0=\overline{(a_0b_0\oplus 1)\oplus(a_1b_3\oplus 1)}\oplus\overline{(a_2b_2\oplus 1)\oplus(a_3b_1\oplus 1)}$$
$$C_1=\overline{\overline{(a_0b_1\oplus 1)\oplus(a_1b_0\oplus 1)}\oplus\overline{(a_1b_3\oplus 1)\oplus(a_2b_2\oplus 1)}\oplus \overline{\overline{(a_2b_3\oplus 1)\oplus(a_3b_1\oplus 1)}\oplus(a_3b_2\oplus 1)}}$$
$$C_2=\overline{\overline{(a_0b_2\oplus 1)\oplus(a_1b_1\oplus 1)}\oplus\overline{(a_2b_0\oplus 1)\oplus(a_2b_3\oplus 1)}\oplus \overline{(a_3b_2\oplus 1)\oplus(a_3b_3\oplus 1)}}$$
$$C_3=\overline{\overline{(a_0b_3\oplus 1)\oplus(a_1b_2\oplus 1)}\oplus\overline{(a_2b_1\oplus 1)\oplus(a_3b_0\oplus 1)}\oplus (a_3b_3\oplus 1)}.$$

The resulting circuit appears in Fig. 19. As we can see in this figure, we need twelve 3T-4M XNOR gates and only four 3T-4M XOR gates.

The design methods presented in this section can be adopted for the design of $m$-bit multipliers over GF($2^m$), e.g. by modifying/combining with the methods presented in [39].

The performance of the systems developed in this section is analysed in Section VI.

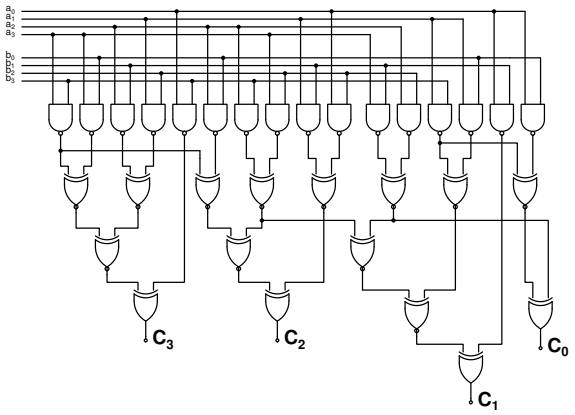



Fig. 19. Memristive GF($2^4$) Multiplier.

## VI. Experimental Results

All the memristors used in this paper are modelled based on [28] and coded in Verilog-A. All designs were implemented and simulated in Cadence Virtuoso. The supply voltage considered is $V_{\rm DD} = 1.2V$ and the transistors used here are based on the 32nm CMOS technology node. The saturation current for n-type and p-type transistors are $I_{D,sat} = 46.63\mu A$ and $I_{D,sat} = 47.6\mu A$ respectively. All the circuits in this paper, where appropriate, were tested with a load capcitance of 1fF and all the power measurements are based on the sum of the static and dynamic powers as reported by Cadence.

*a) Multifunction Gates:* As we already demonstrated in Section IV, the power and reliability performance of our design clearly outperforms both the CMOS based designs as well as the technique of [7] (Table II and Fig. 14). In addition, the techniques of [9], [10], [13] require multiple clock cycles to operate, whereas our technique can be operated in a single clock cycle. Hence, for fairness these were not compared with. The technique of [12] proposed a 8T-6M XOR gate design, which requires similar power as pure CMOS design simply because it requires more than twice the number of transistors and two more memristors compared to our designs. Hence, this technique is clearly less power efficient compared to the proposed designs.

*b) Full Adder Designs:* For the full adder designs in Section V-A we considered $R_{\rm on} = 500\Omega$, $R_{\rm off} = 40k\Omega$, and $R_{\rm D} = 10K\Omega$ based on Eq. (8) and Eq. (9). A reliable performance at high frequencies could be achieved with only $90.98\mu$W power consumption when $k_{\rm on} = -300$m/s, $k_{\rm off} = 52$m/s. The input and output wave forms for our 10T-12M fully buffered full adder design appear in Fig. 20 at 8GHz. Of course, needless to say, the design also works at lower frequencies. Adders designed with both pure CMOS [25] and memristive hybrid gates based on [7] failed at these frequencies and their power performance could not be compared. Hence, we also tested our adder design at 2GHz, i.e. the freuqency where the CMOS XOR/XNOR gate worked (Table II). At 2GHz the proposed adder required $40.77\mu$W, which is clearly better than a single CMOS XOR and XNOR gate at this frequency.

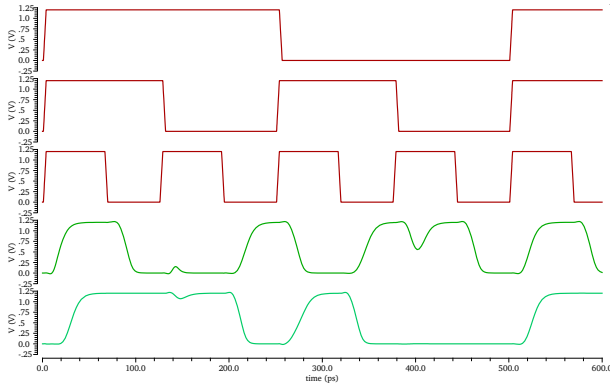



Fig. 20. 10T-12M buffered full adder at 8GHz frequency. Top three signals are the inputs $A$, $B$ and input carry, $C_i$, respectively, and the bottom two signals are the sum ($S$) and output carry ($C_o$) respectively.

*c) Multiplier Designs Over GF:* For the multiplier designs over GF in Section V-B, the power consumption of each individual memristive logic gate M-NAND, M-XNOR and M-XOR in Fig. 17 are $1.016\mu$W, $1.1774\mu$W and $29.11\mu$W at 1GHz respectively. The input and output wave forms of our GF($2^2$) multiplier circuit is shown in Fig. 21, which consumes $63.401\mu$W power. The proposed memristive GF($2^4$) multiplier results in considerably smaller area and requires lower power compared with pure CMOS implementation. The entire circuit requires approximately $153.984\mu$W power, which is much lower than $535.2\mu$W consumed by the same multiplier designed with pure CMOS technology. The total number of elements used for the memristive GF($2^4$) multiplier is 176 (96M-80T) which is much fewer than 264T used by the pure CMOS design. We also tested the 4-bit multiplier based on the XOR/XNOR gate in [7]. The latter design required 168 (64M-104T) elements, but it also required significantly more transistors compared to the proposed design. However, this design failed to operate at a relatively high frequency of 1GHz and hence the power figures could not be obtained. The technique of [12] yields designs with much higher number of transistors and memristors for the multiplier designs (e.g. 128M-136T or 264 elements for the GF($2^4$) multiplier).

## VII. Conclusions

This paper proposed novel memristive logic architectures for low power and reliable performance at low as well as high frequencies. Firstly, with the help of MRL, we showed that memristors can naturally represent multiple valued logic as MIN-MAX post algebra. We proposed an efficient multifunction logic architecture which can operate in single clock cycle with considerably fewer components and less energy. It is also capable of seamless integration with the CMOS technology for hybrid CMOS memristive chip

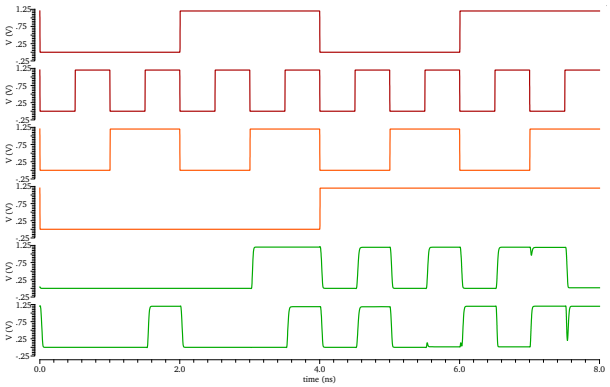



Fig. 21. Memristive GF($2^2$) Multiplier at 1GHz. Top four signals are the inputs $a_0$, $a_1$, $b_0$ and $b_1$ respectively. Bottom two signals are the outputs $C_0$ and $C_1$.

fabrication in 3D. We also demonstrated that with the proper selection of $k_{on}$ and $k_{off}$ parameters, this multifunction logic architecture can reliably operate at high frequencies where both CMOS devices as well as existing hybrid-memristor gates start to fail. The proposed logic architecture consumes significantly less power when compared with pure CMOS as well as existing hybrid memristive logic circuits.

We used the proposed 1T-4M multifunction architecture as the essential building block to implement a highly compact full adder design with very low power requirement. Finally, we presented design techniques for highly efficient memristive bit parallel multipliers over GF($2^2$) and GF($2^4$). These designs required considerably lower power compared to pure CMOS designs. The latter design technique can be generalised to $m$-bit multipliers, e.g. by combining with existing techniques [39]. Our experimental results demonstrated that the proposed memristive multifunction logic architecture can be effectively used to design power efficient low complexity systems alongside the CMOS designs.

Apart from applications in logic design, memristors with strong security primitives are finding applications in PUFs for the emerging hardware security solutions [8]. The first PUF circuit was proposed in [40] which leverages the physical variations of the chip to generate unique outputs. The XOR arbiter PUF is one of the most common delay-based PUFs, e.g. that in [7] which utilises a 6T-2M memristive XOR structure. [7] also demonstrated that a high degree of randomness could be derived by designing PUF with memristors. Our proposed logic structure has two more memristors and one fewer transistor than the XOR structure proposed in [7]. The presence of extra memristors in our structure increases the variation level which makes it well suited for delay-based PUFs.

## Acknowledgement

A preliminary version of this paper appeared at the IEEE 26th Power And Timing Modeling, Optimisation and Simulation (PATMOS) 2016 conference in Bremen, Germany as "Novel Memristive Logic Architectures."

## References

[1] L. Chua, "Memristor-the missing circuit element," *IEEE Transactions on Circuit Theory*, vol. 18, pp. 507–519, Sep 1971.

[2] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *nature*, vol. 453, no. 7191, pp. 80–83, 2008.

[3] Y. Ho, G. M. Huang, and P. Li, "Dynamical properties and design analysis for nonvolatile memristor memories," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, pp. 724–736, April 2011.

[4] M. Hartmann, P. Raghavan, L. V. D. Perre, P. Agrawal, and W. Dehaene, "Memristor-based (reram) data memory architecture in asip design," in *Digital System Design (DSD), 2013 Euromicro Conference on*, pp. 795–798, Sept 2013.

[5] M. Hu, H. Li, Y. Chen, Q. Wu, G. S. Rose, and R. W. Linderman, "Memristor crossbar-based neuromorphic computing system: A case study," *IEEE Transactions on Neural Networks and Learning Systems*, vol. 25, pp. 1864–1878, Oct 2014.

[6] N. Serafino and M. Zaghloul, "Review of nanoscale memristor devices as synapses in neuromorphic systems," in *2013 IEEE 56th International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 602–603, Aug 2013.

[7] J. Mathew, R. S. Chakraborty, D. P. Sahoo, Y. Yang, and D. K. Pradhan, "A novel memristor based physically unclonable function," *Integration, the VLSI Journal*, vol. 51, pp. 37–45, 2015.

[8] J. Rajendran, R. Karri, J. B. Wendt, M. Potkonjak, N. McDonald, G. S. Rose, and B. Wysocki, "Nano meets security: Exploring nanoelectronic devices for security applications," *Proceedings of the IEEE*, vol. 103, pp. 829–849, May 2015.

[9] S. Kvatinsky, G. Satat, N. Wald, E. G. Friedman, A. Kolodny, and U. C. Weiser, "Memristor-based material implication (imply) logic: Design principles and methodologies," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 22, pp. 2054–2066, Oct 2014.

[10] S. Kvatinsky, D. Belousov, S. Liman, G. Satat, N. Wald, E. G. Friedman, A. Kolodny, and U. C. Weiser, "Magic-memristor-aided logic," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 61, pp. 895–899, Nov 2014.

[11] S. Kvatinsky, N. Wald, G. Satat, A. Kolodny, U. C. Weiser, and E. G. Friedman, "Mrl-memristor ratioed logic," in *2012 13th International Workshop on Cellular Nanoscale Networks and their Applications*, pp. 1–6, Aug 2012.

[12] T. Singh, "Hybrid memristor-cmos (memos) based logic gates and adder circuits," *arXiv preprint arXiv:1506.06735*, 2015.

[13] Y. Zhou, Y. Li, L. Xu, S. Zhong, R. Xu, and X. Miao, "A hybrid memristor-cmos xor gate for nonvolatile logic computation," *physica status solidi (a)*, 2015.

[14] J. Cong and B. Xiao, "mrfpga: A novel fpga architecture with memristor-based reconfiguration," in *2011 IEEE/ACM International Symposium on Nanoscale Architectures*, pp. 1–8, June 2011.

[15] K. Sakuma, P. S. Andry, C. K. Tsang, S. L. Wright, B. Dang, C. S. Patel, B. C. Webb, J. Maria, E. J. Sprogis, S. K. Kang, R. J. Polastre, R. R. Horton, and J. U. Knickerbocker, "3d chip-stacking technology with through-silicon vias and low-volume lead-free interconnections," *IBM Journal of Research and Development*, vol. 52, pp. 611–622, Nov 2008.

[16] D. B. Strukov and R. S. Williams, "Four-dimensional address topology for circuits with stacked multilayer crossbar arrays," *Proceedings of the National Academy of Sciences*, vol. 106, no. 48, pp. 20155–20158, 2009.

[17] K.-T. T. Cheng and D. B. Strukov, "3d cmos-memristor hybrid circuits: Devices, integration, architecture, and applications," in *Proceedings of the 2012 ACM International Symposium on International Symposium on Physical Design*, ISPD '12, (New York, NY, USA), pp. 33–40, ACM, 2012.

[18] L. T.Sadi and A.Asenov, "Multi-scale electrothermal simulation and modelling of resistive random access memory devices," in *Power and Timing Modeling, Optimization and Simulation (PATMOS), 2016 26th International Workshop, Bremen*, Sept 2016.

[19] N. Caka, M. Zabeli, M. Limani, and Q. Kabashi, "Impact of mosfet parameters on its parasitic capacitances," in *Proceedings of the 6th WSEAS International Conference on Electronics, Hardware, Wireless and Optical Communications*, pp. 55–59, World Scientific and Engineering Academy and Society (WSEAS), 2007.

[20] L. Wei, F. Boeuf, T. Skotnicki, and H.-S. P. Wong, "Parasitic capacitances: Analytical models and impact on circuit-level performance,"

*IEEE Transactions on Electron Devices*, vol. 58, no. 5, pp. 1361–1370, 2011.

[21] J.-T. Lin, C.-H. Kuo, T.-Y. Lee, Y.-C. Eng, T.-F. Chang, P.-H. Lin, H.-H. Chen, C.-H. Sun, and H.-N. Chiu, "Improving reliability and diminishing parasitic capacitance effects in a vertical transistor with embedded gate," in *Physical and Failure Analysis of Integrated Circuits, 2009. IPFA 2009. 16th IEEE International Symposium on the*, pp. 75–78, IEEE, 2009.

[22] E. Dubrova, "Logic synthesis and verification," ch. Multiple-valued Logic Synthesis and Optimization, pp. 89–114, Norwell, MA, USA: Kluwer Academic Publishers, 2002.

[23] A. A. Adeyemo, J. Mathew, A. M. Jabir, and D. K. Pradhan, "Exploring error-tolerant low-power multiple-output read scheme for memristor-based memory arrays," in *2015 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFTS)*, pp. 17–20, Oct 2015.

[24] M. A. Zidan, H. A. H. Fahmy, M. M. Hussain, and K. N. Salama, "Memristor-based memory: The sneak paths problem and solutions," *Microelectronics Journal*, vol. 44, no. 2, pp. 176–183, 2013.

[25] S. S. Mishra, A. K. Agrawal, and R. Nagaria, "A comparative performance analysis of various cmos design techniques for xor and xnor circuits," *International Journal on Emerging Technologies*, vol. 1, no. 1, pp. 1–10, 2010.

[26] E. Dubrova, Y. Jiang, and R. Brayton, "Minimization of multiple-valued functions in post algebra," in *Proc. of the Intl. Workshop on Logic Synthesis*, 2001.

[27] S. Kvatinsky, E. G. Friedman, A. Kolodny, and U. C. Weiser, "Team: Threshold adaptive memristor model," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, pp. 211–221, Jan 2013.

[28] S. Kvatinsky, M. Ramadan, E. G. Friedman, and A. Kolodny, "Vteam: A general model for voltage-controlled memristors," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 62, pp. 786–790, Aug 2015.

[29] K. Li, Y. Pan, F. Chen, K. T. Cheng, and R. Huan, "Real-time lossless ecg compression for low-power wearable medical devices based on adaptive region prediction," *Electronics Letters*, vol. 50, no. 25, pp. 1904–1906, 2014.

[30] L. Turicchia, S. Mandal, M. Tavakoli, L. Fay, V. Misra, J. Bohorquez, W. Sanchez, and R. Sarpeshkar, "Ultra-low-power electronics for non-invasive medical monitoring," in *2009 IEEE Custom Integrated Circuits Conference*, pp. 85–92, Sept 2009.

[31] A. P. Chandrakasan, N. Verma, and D. C. Daly, "Ultralow-power electronics for biomedical applications," *Annual Review of Biomedical Engineering*, vol. 10, pp. 247–74, 2008.

[32] J. J. Yang, M. D. Pickett, X. Li, D. A. Ohlberg, D. R. Stewart, and R. S. Williams, "Memristive switching mechanism for metal/oxide/metal nanodevices," *Nature nanotechnology*, vol. 3, no. 7, pp. 429–433, 2008.

[33] D. B. Strukov and R. S. Williams, "Exponential ionic drift: fast switching and low volatility ofáthin-film memristors," *Applied Physics A*, vol. 94, no. 3, pp. 515–519, 2009.

[34] M. D. Pickett, D. B. Strukov, J. L. Borghetti, J. J. Yang, G. S. Snider, D. R. Stewart, and R. S. Williams, "Switching dynamics in titanium dioxide memristive devices," *Journal of Applied Physics*, vol. 106, no. 7, p. 074508, 2009.

[35] A. Pishvaie, G. Jaberipur, and A. Jahanian, "Improved cmos (4; 2) compressor designs for parallel multipliers," *Computers & Electrical Engineering*, vol. 38, no. 6, pp. 1703–1716, 2012.

[36] S. Kvatinsky, D. Belousov, S. Liman, N. Wald, and G. Satat, "Pure memristive logic gate," Sept. 10 2015. US Patent App. 14/641,482.

[37] E. Yalon, A. Gavrilov, S. Cohen, D. Mistele, B. Meyler, J. Salzman, and D. Ritter, "Resistive switching in $hboxHfO_2$ probed by a metal insulator semiconductor bipolar transistor," *IEEE Electron Device Letters*, vol. 33, pp. 11–13, Jan 2012.

[38] R. Lidl and H. Niederreiter, *Introduction to Finite Fields and their Applications*. Cambridge University Press, second ed., 1994. Cambridge Books Online.

[39] A. Reyhani-Masoleh and M. A. Hasan, "Low complexity bit parallel architectures for polynomial basis multiplication over gf($2^m$)," *IEEE Transactions on Computers*, vol. 53, pp. 945–959, Aug 2004.

[40] J. W. Lee, D. Lim, B. Gassend, G. E. Suh, M. van Dijk, and S. Devadas, "A technique to build a secret key in integrated circuits for identification and authentication applications," in *VLSI Circuits, 2004. Digest of Technical Papers. 2004 Symposium on*, pp. 176–179, June 2004.