A 0.6V pure MOS voltage Reference for Bio-medical applications with 40ppm/0c temperature drift

R Nagulapalli, K.Hayatleh, S. Barker, S.Raparthy, N Yassine, F J Lidgey

This paper exploits the well-known CMOS beta multiplier circuit to synthesize a voltage reference, which is well suitable for low voltage and ultra-low power bio-medical applications. The present technique uses only MOS transistors to generates PTAT and CTAT currents. Self-biasing technique has been used to minimize the temperature and power supply dependency. A prototype in 65nm CMOS has been developed, at room temperature it is generating 404mV reference voltage with 2.6mV drift over wide temperature range (from -40 to 125⁰C). This has been designed to operate with a power supply voltage down to 0.6V and consumes 1.4uA current from the supply. The simulated temperature coefficient is 40ppm/⁰C. Circuit occupies 0.0039mm2 area.

Introduction: A low voltage bandgap reference, specifically one that can operate on low voltage is always challenging. There is a growing requirement that operates in wide range applications including filters, memory, data converters, bio-medical applications [1]. Portable and wearable bio-medical devices are capable of detecting signals in areas such as electrocardiography(ECG) and electroencephalography(EEG), sensing these sensitive signals require high precision ADC (~12 bit), which requires highly accurate and low power voltage reference circuit.

The fundamental operating principle of a reference circuit is to generate scaled combination PTAT and CTAT current/voltage to generate temperature independent voltage. There have been several attempts to build this concept. A typical low voltage bandgap [2] uses BJT's to generate PTAT current and to fabricate in the standard CMOS process parasitic vertical PNP Bipolar Junction Transistor (BJT) has been used. This has three problems, one is these transistors are having poor current gain (β) and sensitive to process variation which could lead to temperature drift of the reference voltage. The second problem is the power supply voltage requirement, Vbe of the BJT (~0.7V) doesn't scale with the process and limits the supply voltage. The third problem is BJT bias current is significantly high compared to the counterpart (MOSFET), which is a big problem the for the bio-medical and wearable application. Hence there is a clear motivation for pure MOS transistor based designs.

Peaking current source has been modified as bandgap reference by exploiting the difference between V_{gs} of two transistors [3], but this requires cascading of transistors hence not suitable for low voltage and poor power supply rejection, which demands a Voltage Regulator. Another method is to generate reference based on extrapolated MOSFET threshold voltage (Vth) at very low temperature to realize low voltage operation [4], but this has unacceptable process variation which requires calibration. [5][6] are based on mutual cancellation of mobility and threshold voltage, but it is difficult to track both variations and often very sensitive to the transistor models very strongly, which might create yield problem while going for mass production. Most of the designs use op-amps in the core circuit to achieve high performance such as temperature independence, power supply insensitivity, but they come at the expense of power and area [7]. These designs require voltage headroom's also, which makes them not suitable for low voltage applications. This paper explores standard beta multiplier circuit to generate PTAT and CTAT currents and finally bandgap reference voltage generation. Some of the key metrics differentiate our work from the state of art is low power, low voltage, and less complexity. The rest of the paper organized as follows. Section 2 introduces the beta multiplier circuit and qualitative treatment of its PTAT and CTAT nature, Section 3 describes proposed reference circuit and implementation details. Finally, section 4 summarizes the simulation results and layout of the prototype

2. Beta Multiplier: Fig:1 shows the beta multiplier (constant g_m) conventional circuit [8]. The fundamental principle of working is to create a voltage drop equal to the difference between the V_{GS} of two transistors carrying same current but different sizes (W/L). Transistor M_3,M_4 connected in a such a way that V_{gs3}-V_{gs4} defines current through Rs. The current mirror formed by M_2,M_1 will force the same current through Transistors M_3,M_4. Though this is a very common circuit, feedback mechanism in this circuit is very subtle. Fig:2 shows the I-V characteristics of M_3,M_4. From the figure, circuit settles at the intersecting point of the two curves. During the circuit converging to the

desired operating, it can be either side of the intersecting point. If the current lesser than the desired one means I_1>I_2 and vice versa. If I_1-I_2>0, then circuit current must increase. Current can be increased by increasing voltage of the node A. So feedback should work in such a way that somehow node A has to increase if circuit detects I_1-I_2>0 and vice versa. Since M_1,M_3 connected in series, node A can detect the current difference and it increases according to i_1-i_2 polarity hence by connecting Node A to gate of the M_3, circuit acts as negative feedback circuit.M_3 aspect ratio (W/L) must be higher than M4, because V_{gs3} has to be lesser than V_{gs4}. To save power this circuit has been designed in the deep sub-threshold region by increasing the devices sizes and controlling resister R_s.

Drain current of the NMOS operating in the sub-threshold region can be expressed as follows.

$$I_D = \frac{W}{L} I_0 exp\left(\frac{V_{gs}-V_{th}}{\eta V_T}\right)\left(1 - exp\left(\frac{-V_{ds}}{V_T}\right)\right) \qquad (1)$$

Where $I_o = \mu_n C_{ox}(\eta - 1)V_T^2$, and W is the width is the length, $\mu_n$is electron mobility, $C_{ox}$is gate oxide capacitance, η is sub-threshold slope factor, V_T is thermal voltage, $V_{th}$is threshold voltage. For Vds>4VT (~100mV at room temperature), vds term in (1) is very less and Id is almost independent of vds, it is expressed as

$$I_D = \frac{W}{L} I_0 exp\left(\frac{V_{gs}-V_{th}}{\eta V_T}\right) \qquad (2)$$

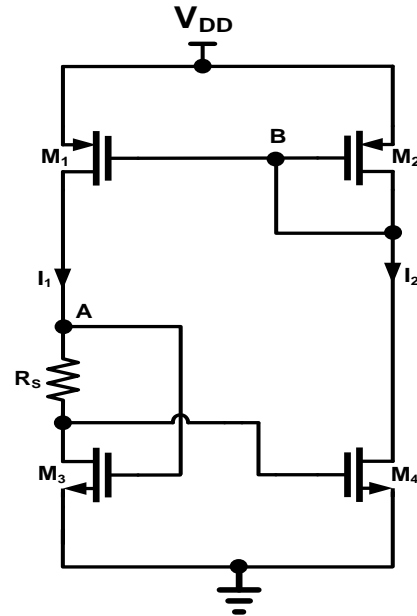$$V_{gs} = V_{th} + \eta V_T \ln\left(\frac{I_d}{\frac{W}{L}I_0}\right) \qquad (3)$$
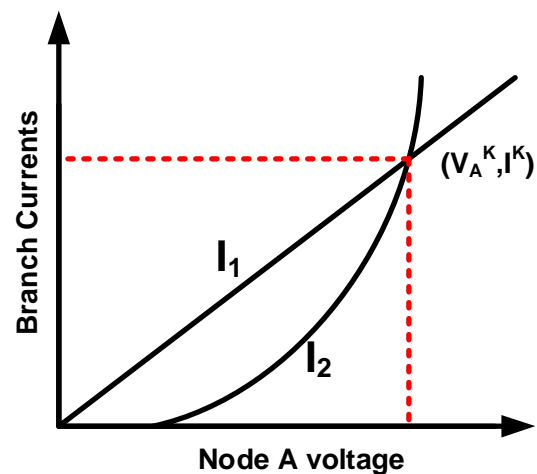

Fig. 1 Beta Multiplier circuit

Fig. 2 V-I characteristics of the beta multiplier

The circuit configuration as shown in fig:1(a) constrains the difference between vgs of M3, M4 in a relation given as follows.

$$V_{gs3} - V_{gs4} = I_1 R_s \qquad (4)$$

Substituting (3) into (4) results the transistor current as follows.

$$I_1 R_s = \eta V_T \ln\left[\frac{\left(\frac{W}{L}\right)_4}{\left(\frac{W}{L}\right)_3}\right] \qquad (5)$$

If the aspect ratio of M_4 is β times higher than M_3, then current can be expressed as

$$I_1 = \frac{\eta V_T \ln(\beta)}{R_s} \qquad (6)$$

From (6), the voltage drop across Rs is PTAT, because thermal voltage (KT/q) increases with temperature. A PTAT current carrying Transistor gate to source voltage (Vgs) and threshold voltage (Vth) decreases with temperature [12], because increasing temperature will increase electrons thermal energy and requires less voltage to invert the channel in the MOSFET and it can be approximated as a first order polynomial with a negative slope as follows.

$$V_{gs}(T) \sim V_{gs}(T_0) + K_{th}\left(\frac{T}{T_o} - 1\right) \qquad (7)$$

Where Kth is temperature coefficient of Vgs. Fig. 3 shows the simulated gate to source voltage of the transistor wrt temperature., it has been showing CTAT nature with $-0.3mV/^0C$ temp coefficient.
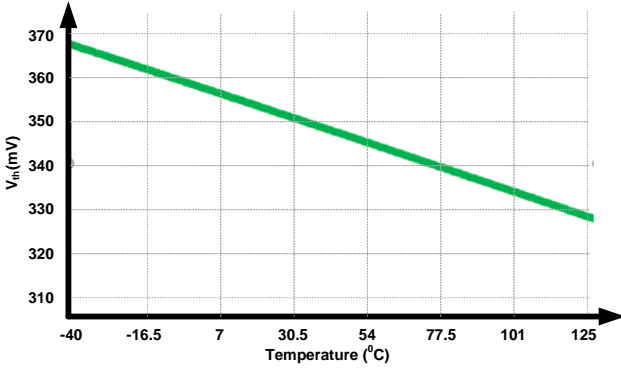

Fig. 3 Gate to source voltage wrt temperature

3. Proposed Bandgap reference circuit: As explained in the introduction, the idea of bandgap reference is scaled summation of PTAT and CTAT current's and convert into voltage. From the section 2, Beta multiplier bias current is having PTAT nature. Unfortunately, CTAT current is not available in beta multiplier, but Vgs3 will have CTAT nature, using a conventional voltage to current converter formed by OP_1,M_5,R_1 will create CTAT current through M5.Fig:2 shows the proposed full schematic of the bandgap reference. It contains Beta multiplier, V to I converter and current summation network. M_p carries PTAT current and M_c carries CTAT and hence the voltage across R2 is temperature independent voltage. To have a flexible design and minimize the resister values, used scaling factors α_1 and α_2 in the current mirrors M_1,M_p and M_5,M_c respectively.

Current through M_p is given by $\alpha_1 \frac{V_{gs3}}{R_1}$

Voltage across R2 is given by the following expression

$$\begin{aligned} V_{ref} &= \left[\alpha_1 \frac{\eta V_T \ln(\beta)}{R_S} + \alpha_2 \frac{V_{gs3}}{R_1}\right] R_2 \\ &= \left(\alpha_1 \eta V_T \ln(\beta) + \frac{R_S}{R_1}\alpha_2 V_{gs3}\right)\frac{R_2}{R_S} \end{aligned} \qquad (8)$$
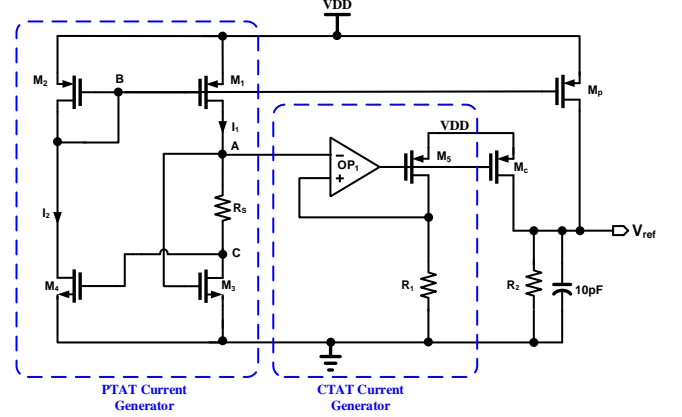

Fig. 4 Proposed bandgap Reference

For minimizing the temperature coefficient of the reference voltage, $\frac{\partial V_{ref}}{\partial T} = 0$ at a known temperature. Hence by differentiating (8) we can deduce the following condition.

$$\alpha_1 \frac{R_1}{R_s}\frac{\partial V_T}{\partial T}\ln(\beta) + \alpha_2 \frac{\partial V_{gs3}}{\partial T} = 0 \qquad (9)$$

At room temperature $\frac{\partial V_T}{\partial T} = 0.087mV/^0C$ and from previous section $\frac{\partial V_{gs3}}{\partial T} = -0.3mV/^0C$. We have chosen $\alpha_1 = \frac{1}{3}$, $\alpha_2 = 1$ for the design flexibility and $\beta=24$ for the layout matching between M_3, M_4. Substituting these values into (9) we can show that $\frac{R_1}{R_s}=3.255$ to keep a perfect balance between CTAT, PTAT current and hence minimum temperature drift.
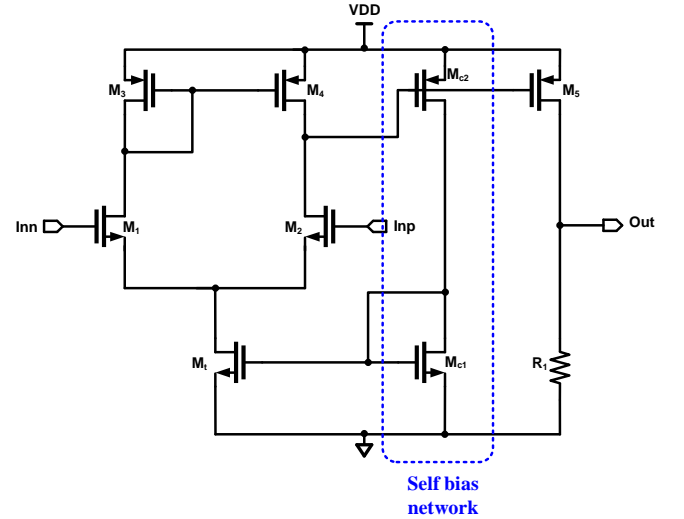

Fig. 5 Self-bias CTAT generator

CTAT circuit is a voltage to current converter with Vgs as input. As shown in Fig:4, OP_1 adjusts the current through M5 until the voltage drop across R1 equals to the Vgs of the M3. The bottle neck here is any offset in the opamp will also convert as current, which will create an error in the desired CTAT current, hence opamp needs to design with ultra-low offset. Increasing device sizes in the opamp will decrease the offset, but due to inverse square law relation between offset and device area [10], this method occupies a lot of silicon area. Very-efficient and well known way of minimizing the offset will be chopper stabilization method but this needs a clock generator and ripple filter [11]. Self-bias is one way of biasing analog circuits which will have minimal offset, less temperature drift, so we have chosen self-bias scheme [9] and Fig:5 shows the detailed implementation of the circuit. M_1,M_2,M_3,M_4,M_t forms the opamp and M_5,R_1 forms the current converter. M_{c2}, M_{c1} transistors produce bias voltage required for the M_t by sensing the output of the opamp. Unfortunately, self-biasing needs start up circuit to kick the circuit from undesired zero current operating point, for simplicity start-up circuit hasn't shown in fig:5.
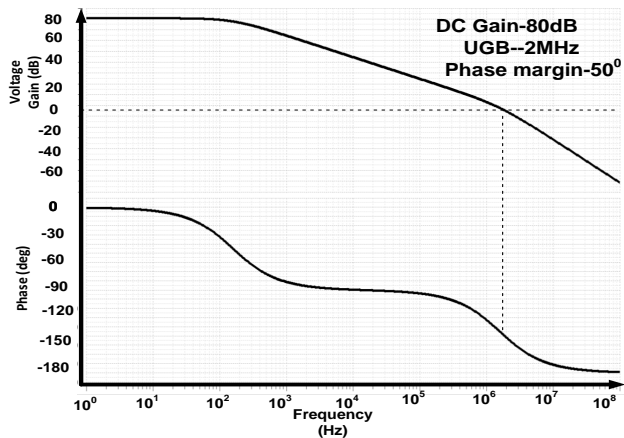
Fig. 6 Self-bias CTAT open-loop response

Fig:6 shows the open loop frequency response of the CTAT current generator, which has been designed with 80dB dc gain to minimize the systematic offset and 50^0 phase margin for a well-behaved transient response. To assess the efficiency of the self-bias strategy, opamp offset variation with temperature has been simulated and compared with a fixed bias (means Mt bias has been derived from a diode connected transistor carrying fixed current). Fig:7 shows the offset of the opamp, which shows 3x improvement with self-bias scheme.
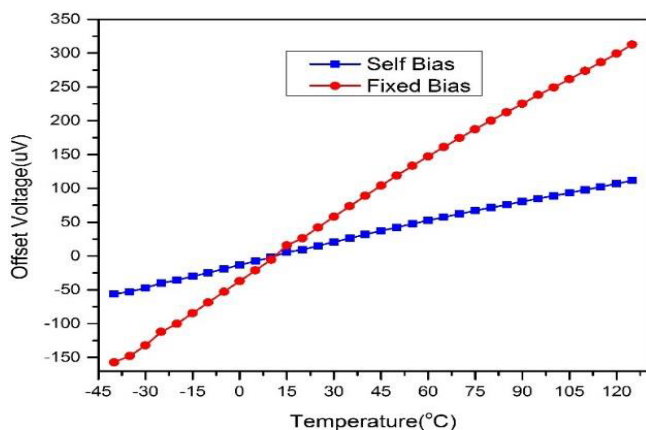

Fig. 7 Simulated Offset of the self-bias opamp

4. Bandgap reference simulation results:
Proposed circuit has been implemented in 65nm 1-poly 8-metal CMOS technology, Table-1 shows the parameters of the transistors and resisters used in the proposed voltage reference circuit.

TABLE I

Transistors			
Bandgap Reference		Self-Bias Opamp	
Component Name	W/L (um/um)	Component Name	W/L (um/um)
M_1	42/3.2	M_1	5/2
M_2	42/3.2	M_2	5/2
M_3	48/3	M_3	8/3
M_4	2/3	M_4	8/3
M_5	32/3	M_t	10/2
M_c	32/3	M_{c1}	5/2
M_p	14/3.2	M_{c2}	8/3

Resisters	
Component Name	Resistance (KΩ)
R_s	70
R_1	227.85
R_2	312

Simulations have been performed on layout extracted netlist and results as follows. Fig:8 shows the CTAT and PTAT, scaled summation of these currents produces reference voltage according to the equation (9).
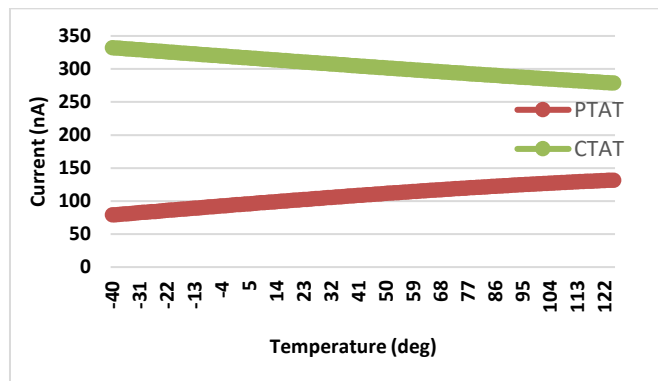

Fig. 8 CTAT and PTAT currents.

Fig:9 shows the bandgap reference voltage (voltage across R_2) variation from -40^0C to 125^0C. At room temperature reference voltage is 404mV, the maximum deviation of the voltage over full temperature range is 2.64mV means 0.65% accuracy and this design achieves 40ppm/^{0}C while powered from 0.6V supply. The circuit starts working properly when power supply voltage greater than or equal to 0.6V. Minimum working power supply voltage 0.6V limited by CTAT generator opamp. In the supply voltage range from 0.6 to 1V, reference voltage changes by 2.3mV means the supply or line sensitivity is 1.8%/V. Yield is the main parameter for volume semiconductor products, hence Monte Carlo variation is critical results for any sensitive circuits like the present one. Fig:11 depicts the histogram of the reference voltage, showing 2.166mV standard deviation with a mean of 404mV.
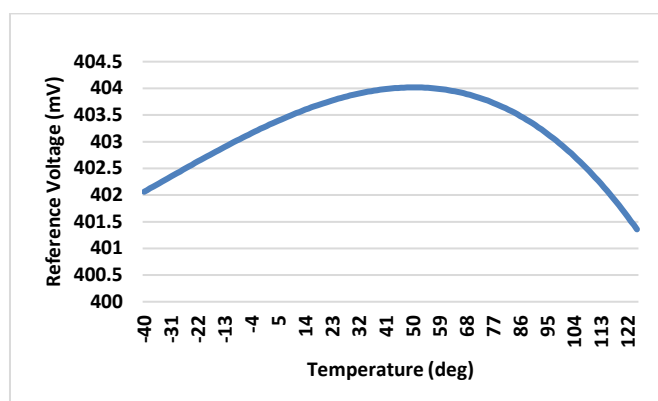

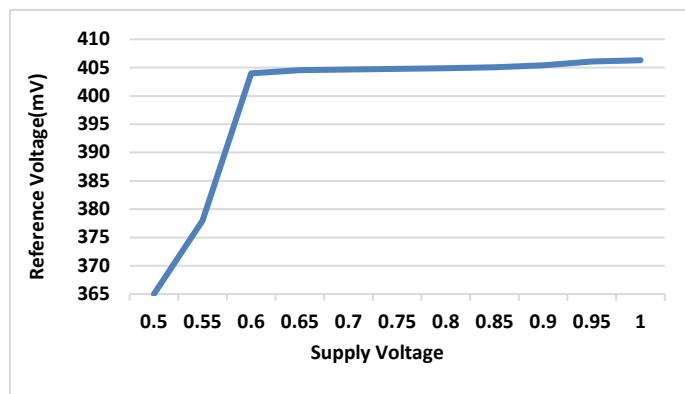**Fig. 9** Bandgap reference voltage wrt temperature.

Fig. 11 Line Regulation.

Fig:12 shows the simulated power spectral density (PSD) of the reference voltage. From the noise analysis of the circuit, flicker noise of transistor M_3,M_4 and channel thermal noise of the CTAT generator

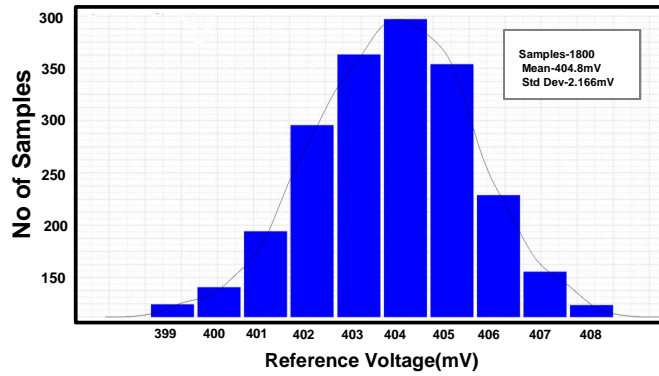opamp (OA$_1$) are the dominate noise contributors. The summary of the performance listed in table II.

Integrated Noise (.1-10KHz)	41	uV
Technology	65	nm
Area	3975	um^2

Fig. 11 Simulated distribution

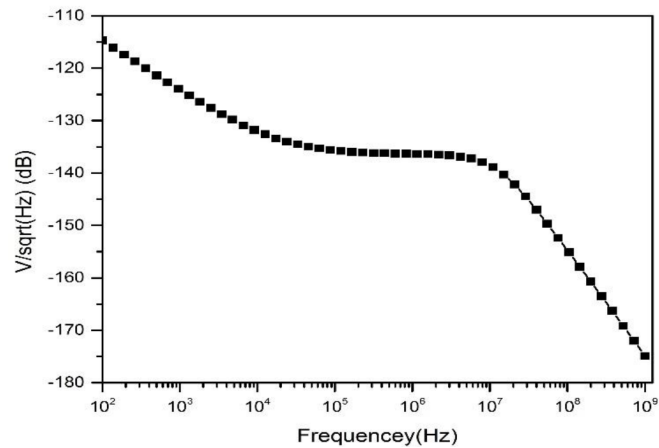**Fig. 12** Simulated PSD of the output voltage.

The layout of the proposed circuit is shown in Fig. 13, and the active area is 75um*53um. Every transistor has been laid with proper care towards Mismatch. Special care has been taken for well-proximity effect (WPE) and Shallow trench isolation (STI), by adding enough dummies for each device and keeping MOSFET away from NWELL [13].
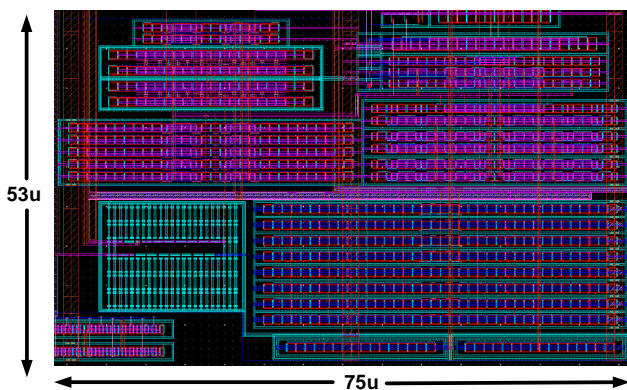

Fig. 13 Layout of the proposed Technique

TABLE II
Performance Summary

Parameter	Value	Units
Minimum Supply Voltage	0.6	V
Current consumption	1.4	uA
Output Voltage	404	mV
Temperature range	-40 to 125	^{0}C
Temperature Coefficient	40	ppm/^{0}C

Conclusion: A low voltage bandgap reference circuit has been proposed and demonstrated 40ppm/^{0}C temperature coefficient. With the help of Sub-threshold MOSFET current equation, closed form for the output voltage has been derived and it is closely matching with the simulation results. A transistor level Demonstration with the layout shown and all results have been explained in the last section.

R. Nagulapalli, K. Hayatleh, S. Barker and F J Lidgey
(*Faculty of Technology, Design and Environment, Oxford Brookes University, Wheatley Campus, Oxford, OX33 1HX, UK*)
E-mail: khayatleh@brookes.ac.uk

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