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A High Performance Single Cycle Memristive Multifunction Logic Architecture

X. Yang, A. A. Adeyemo, A. Jabir, and J. Mathew

We present a low complexity high performance memristive multifunction logic architecture for low power high frequency operations in a single cycle, which does not require additional control input/logic and multicycle setup/operation. It can be seamlessly integrated with the existing CMOS technology with just 1T-4M design and without additional overhead. Our technique can realise both XOR/AND or XNOR/OR operations simultaneously. Experimental results show that our technique significantly outperforms both CMOS and existing hybrid memristor-CMOS based designs in terms of chip area, power consumptions, and reliable performance especially at high frequencies. With the help of full adder designs, we also demonstrate that the multifunctionality of our architecture can result in highly compact designs.

Introduction: Memristors (short for ‘memory-resistors’) are nanoscale memory devices, which have found applications in high density memory design, neuromorphic systems, and logic design [1–9]. In logic design, most of the existing techniques require multiple clock cycles/steps and complex control logic for basic logic operations [2, 3, 7], which are not directly compatible with the existing CMOS technology. In contrast, we propose a one transistor and four memristors (1T-4M) multifunction (XOR/AND or XNOR/OR) logic architecture which can operate in a single clock cycle, i.e. the output appears in the same cycle the input is applied, and can be seamlessly integrated with the existing CMOS technology without additional overhead. One of the key advantages of memristors, and hence our approach, is that it is possible to fabricate memristors in 3D whereas with the CMOS technology only 2D fabrication is possible [4]. This allows memristors to be fabricated along the Z-axis stacked over a layer of CMOS layout along the XY-axis. In addition, the capacitance in transistors is a limiting factor for high frequency operations. We mitigate these by reducing the number of transistors in our designs. This significantly improves power consumptions and reliability of our designs at high frequencies with better chip area utilisation. The latter is possible because we are able to free up space in the CMOS layer for more functionality. Additionally, with the help of low complexity full adder designs we demonstrate that the multifunctionality feature of our architecture can result in highly compact systems. Our primary objective is to reduce the number of transistors in a 3D CMOS-memristor hybrid chip for ensuring lower power consumption and improved reliability at high frequencies. We also ensure a lower memristor count.

Memristive XOR Functionality: Fig. 1(a) shows the symbol of a memristor. Here V_p and V_n are its ‘positive’ and ‘negative’ terminals respectively. The memristor switches to low resistance R_{ON} when $V_p - V_n > V_M$, and switches to a high resistance R_{OFF} otherwise [6]. We propose a single cycle purely memristive XOR architecture as shown in Fig. 1(b). The XOR architecture incorporates four memristors M_1, M_2, M_3 and M_4 , where M_2 and M_4 , and M_1 and M_3 are connected for logic OR and AND operations respectively [5]. As summarised in Table 1, the voltage difference between V_{L1} and V_{L2} , i.e. the voltage across load R_L , behaves like XOR operation. In this table $V_1 (> V_M)$ is assumed to be equivalent to V_{DD} in CMOS logic and represents the ON-state voltage, i.e. logic 1. This is summarised in Lemma 1.

Table 1: Pure memristive XOR functionality.

Row	A	B	Output
1	0	0	$V_{L1} - V_{L2} = 0V$: No current from V_{L1} to $V_{L2} \implies$ Logic 0.
2	0	V_1	$V_{L1} - V_{L2} \approx V_1V$: Current from V_{L1} to $V_{L2} \implies$ Logic 1.
3	V_1	0	$V_{L1} - V_{L2} \approx V_1V$: Current from V_{L1} to $V_{L2} \implies$ Logic 1.
4	V_1	V_1	$V_{L1} - V_{L2} \approx 0V$: No current from V_{L1} to $V_{L2} \implies$ Logic 0.

Lemma 1: The pure memristor circuit in Fig. 1(b) realises the XOR functionality depicted in Table 1.

Proof: We consider each row in Table 1 separately.

Row-1: Follows trivially because no current flows in the circuit.

Row-2: In this case memristors $M_2 = M_3 = R_{OFF}$ because 0V appears at the positive terminal of M_2 through A, and V_1V appears at the negative

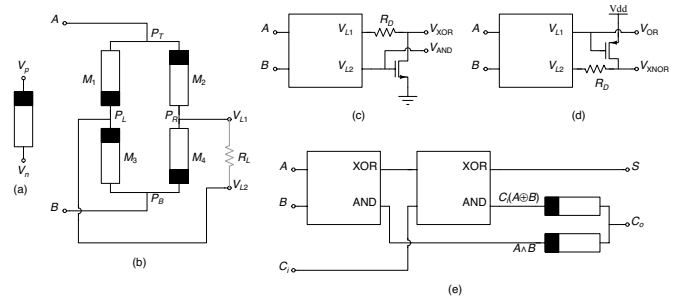


Fig. 1 (a) Memristor, (b) XOR functionality, (c) and (d) XOR/AND and XNOR/OR dual functionality, and (e) 2T-10M ‘weak’ ADDER design.

terminal of M_3 through B. In contrast, memristors $M_4 = M_1 = R_{ON}$ because their positive terminals are closer to V_1V and negative terminals closer to 0V. Because of voltage division the voltage at P_R rises towards V_1V , and that at P_L falls towards 0V. Hence the current flows from $B \rightarrow P_B \rightarrow P_R \rightarrow V_{L1} \rightarrow V_{L2} \rightarrow P_L \rightarrow P_T \rightarrow A$. Hence this is logic 1.

Row-3: This is similar to Row-2. Here $M_1 = M_4 = R_{OFF}$, while $M_2 = M_3 = R_{ON}$. Again the voltage at P_R rises towards V_1V , and that at P_L falls towards 0V. The current flows from $A \rightarrow P_T \rightarrow P_R \rightarrow V_{L1} \rightarrow V_{L2} \rightarrow P_L \rightarrow P_B \rightarrow B$. Hence this is logic 1.

Row-4: In this case both $P_L (V_{L2})$ and $P_R (V_{L1})$ are at the same voltage level and no current flows through R_L . Hence this is logic 0.

These operations can take place in the same clock cycle as the inputs. Hence the circuit in Fig. 1(b) exhibits XOR functionality in Table 1 in a single cycle. We note that $\forall A, B \in \{0, V_1\}$, the following are true for the circuit in Fig. 1(b).

$$V_{L1} = A \vee B \quad (1)$$

$$V_{L2} = A \wedge B \quad (2)$$

$$V_{L1} \geq V_{L2}. \quad (3)$$

Integration with CMOS Technology: Based on the architecture in Fig. 1(b), we now present 1T-4M designs, as shown in Fig. 1(c) and (d), for realising the XOR/AND and XNOR/OR operations in a single cycle. These are well suited for seamless integration with the existing CMOS technology without requiring any additional control input/logic, which most existing techniques require [2, 3, 7]. Here the NMOS transistor (NMOST) and the PMOS transistor (PMOST) are assumed to operate in the saturation and cut off regions. We present the following regarding the correctness.

Lemma 2: The NMOST in Fig. 1(c) and the PMOST in Fig. 1(d) realise the following logic operations respectively.

$$V_{XOR} = V_{L1} \wedge \overline{V_{L2}} \quad (4)$$

$$V_{XNOR} = \overline{V_{L1}} \vee V_{L2}. \quad (5)$$

Proof: The proof follows by firstly noting Eq. (3). The only time V_{XOR} in Fig. 1(c) is at logic 1 ($\approx V_1V$) is when $V_{L1} \approx V_1V$ and $V_{L2} \approx 0V$. At all other times either $V_{XOR} = 0$ ($V_{L1} = V_{L2} = 0$) or the NMOST goes into saturation and $V_{XOR} \approx 0.1V$ ($V_{L1} = V_{L2} \approx V_1V$). Similarly, in Fig. 1(d) the only time $V_{XNOR} \approx 0V$ is when $V_{L1} \approx V_1V$ and $V_{L2} \approx 0V$. At all other times $V_{XNOR} \approx V_1V$. Hence the proof follows.

Theorem 1: The circuit in Fig. 1(c) realises logic XOR (V_{XOR}) and AND (V_{AND}) operations simultaneously, and the circuit in Fig. 1(d) realises the logic XNOR (V_{XNOR}) and OR (V_{OR}) operations simultaneously.

Proof: According to Eq. (2) and Eq. (1), the circuits in Fig. 1(c) and (d) trivially realise the AND and OR operations respectively. To prove that Fig. 1(c) realises the XOR operation, we substitute V_{L1} and V_{L2} from Eq. (1) and Eq. (2) into Eq. (4) respectively. This yields $V_{XOR} = A \oplus B$. Now, regarding Fig. 1(d) Eq. (5) is merely the inverse of Eq. (4), i.e. $V_{XNOR} = \overline{V_{XOR}} = 1 \oplus A \oplus B$. Hence the proof follows.

The circuits in Fig. 1(b), (c), and (d) realise ‘weak’ (bufferless) outputs. However, one or more CMOS inverter buffer stages can be added at the outputs for full voltage swings and current drive. For example, a CMOS inverter connected to V_{XOR} in Fig. 1(c) converts it into a ‘strong’ XNOR gate, while the same converts the circuit in Fig. 1(d) into a ‘strong’

XOR gate. This yields 3T-4M buffered XOR/XNOR gates, which require considerably fewer transistors compared to 6T-2M [8], 8T-6M [5], 8T-1M [7], and 10T/8T [9].

Design Rule: Let $I_{D,sat}$ be the drain saturation current for the NMOST and PMOST. We describe the design rule for the circuit in Fig. 1(c). Similar design rule applies to Fig. 1(d). To ensure that the design works correctly, we need to ensure that the transistors operate in the saturation and cutoff regions.

(1) The NMOST is in saturation when $A = B = V_{L1} = V_{L2} \approx V_1V$. In this case $M_2 = M_4 = R_{ON}$, while $M_1 = M_3 = R_{OFF}$. Also as far as V_{L1} is concerned, $M_2||M_4 = R_{ON}||R_{ON}$. Hence, $I_{D,sat} = (V_{DD} - V_{DS,sat})/(R_D + R_{ON}||R_{ON}) \Rightarrow (R_D + R_{ON}/2) = (V_{DD} - V_{DS,sat})/I_{D,sat}$.

(2) The NMOST is in its cutoff region when $V_{L1} \approx V_1V$ and $V_{L2} \approx 0V$, i.e. when $A = V_1V$ and $B = 0V$ or $A = 0V$ and $B = V_1V$. In the first case $M_1 = R_{OFF}$ and $M_3 = R_{ON}$, and in the second case $M_1 = R_{ON}$ and $M_3 = R_{OFF}$. In both the cases M_1 and M_3 form a voltage divider w.r.t. V_{L2} . Hence, we need to ensure that $((V_1 \times R_{ON})/(R_{ON} + R_{OFF})) <$ the threshold voltage of the NMOST.

We have tested with several memristor models [6, 7], and the designs worked correctly for a range of R_{ON} and R_{OFF} . For low R_{ON} a higher R_D may be necessary, while for higher R_{ON} R_D may be eliminated altogether.

Full Adder Design: The multifunctionality of our proposed architecture offers compact design of more complex circuits. We demonstrate this by designing a full adder circuit. Fig. 1(e) shows a reference unbuffered (weak) XOR-XOR 2T-10M full adder design. Here, the sum $S = A \oplus B \oplus C_i$. The shared terms are $A \wedge B$ and $C_i(A \oplus B)$, which are Ored together to form the output carry $C_o = C_i(A \oplus B) \vee AB$. We have designed both buffered and unbuffered full adders, which we present in Table 2. The column ‘Architecture’ shows all possible ways of using the architectures in Fig. 1(c) and (d) in the first and second sum stages. The column ‘Buffered’ represents the designs with CMOS inverters to achieve full voltage swing at the outputs. In this column the XOR-XOR design is the most compact and provides highly reliable performance. A CMOS inverter is connected to each V_{XOR} output; the carry is double inverted. Hence we need $3T+3T+4T=10T$ and $8M+2M+2M = 12M$. This is a significant improvement over existing designs, e.g. 16T-18M [5] and 27T-2M [7].

Table 2: Full adder design with proposed architecture.

Architecture	Unbuffered			Buffered		
	Shared	Elem	Tot	Shared	Elem	Tot
XOR-XOR	$A \wedge B$, $C(A \oplus B)$	2T-10M	12	$A \wedge B$, $A \oplus B$	10T-12M	22
XOR-XNOR	$A \wedge B$, $C(A \oplus B)$	4T-12M	16	$A \wedge B$, $A \oplus B$	12T-12M	24
XNOR-XOR	$C(A \oplus B)$	4T-12M	16	$C(A \oplus B)$	12T-12M	24
XNOR-XNOR	$A \vee B$	2T-14M	16	$A \vee B$, $A \oplus B$	10T-14M	24

Experimental Results: For the experimental results, the memristors were coded in Verilog-A based on the VTEAM model [6] and the systems were designed and simulated in Cadence Virtuoso. We have used the 32nm technology node for the experiments with $V_1 = V_{DD} = 1.2V$, and $I_{D,sat} \approx 46.63\mu A$ for the NMOST and $I_{D,sat} \approx 47.6\mu A$ for the PMOST at 27C operating temperature. As an example of R_{ON} and R_{OFF} selection, if we set $R_{ON} = 500\Omega$ and $R_{OFF} = 2K\Omega$ [7], then based on Design Rule-1 $R_D \approx 24K\Omega$. Also this ensures about 0.24V drop across R_{ON} to satisfy Design Rule-2. A higher R_{OFF} , e.g. $R_{OFF} = 80K\Omega$, ensures better power performance.

We have compared the performance of our 3T-4M designs with CMOS based designs [9] as well as existing hybrid memristor-CMOS based designs [8]. The first two rows of Table 3 present the performance of the 3T-4M XOR and XNOR gates, while the last two rows present the performance of the 10T/8T CMOS XOR/XNOR gates [9]. The latter design is based on a ‘weak’ 6T XOR gate. All designs were tested with a 1 femto F load capacitance. The power, in microwatts (μW), is the average of the total static and dynamic powers. Clearly, both our designs require significantly less power than the CMOS designs, while maintaining consistent performance even at 8GHz. In addition, our buffered XNOR design is considerably more power efficient than our buffered XOR design. This is owing to the use of the NMOST vs PMOST and the way they are connected as shown in Fig. 1(c) and (d). Fig. 2 presents the performance of our design at 8GHz, where both the 10T CMOS and 6T-2M XOR gates [8, 9] failed.

Table 3: Performance analysis compared to CMOS design.

Frequency → Architecture ↓	2GHz		4GHz		8GHz	
	Power (μW)	Stat	Power (μW)	Stat	Power (μW)	Stat
3T-4M XOR	13.47	Pass	17.85	Pass	24.86	Pass
3T-4M XNOR	4.67	Pass	8.85	Pass	16.20	Pass
10T C-XOR	67.93	Pass	72.01	Fail	78.61	Fail
8T C-XNOR	54.55	Pass	56.50	Fail	59.78	Fail

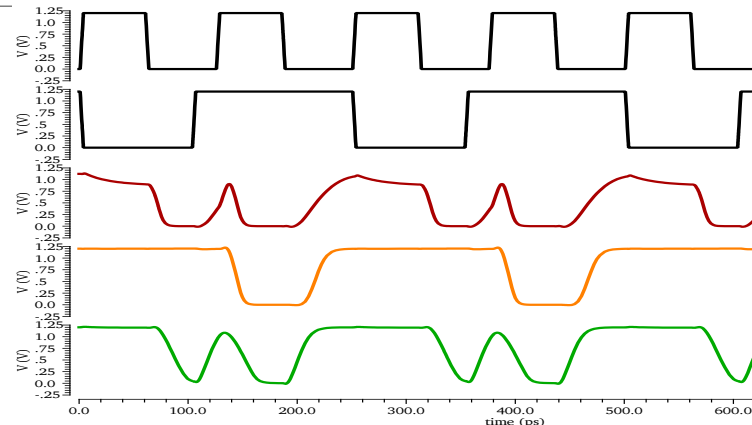


Fig. 2 Buffered XOR performance at 8GHz or higher: Top two signals are the inputs; 3rd: 10T CMOS [9]; 4th: 6T-2M [8]; bottom: proposed 3T-4M.

We have also tested the buffered full adder designs in Table 2 at various frequencies. The 10T-12M design from Row-1 (XOR-XOR) operated correctly at 8GHz and required $63.53\mu W$ power. This is lower than the power consumed by a single CMOS XOR gate (Table 3).

Conclusions: We presented an 1T-4M high performance multifunction logic architecture, which can be seamlessly integrated with the existing CMOS technology. Our designs required considerably fewer transistors and memristors compared to existing techniques. The experimental results showed that the proposed designs are capable of outperforming existing CMOS as well as hybrid CMOS-memristor designs in terms of chip area, power consumption, and reliable performance, especially at high frequencies.

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