A novel current reference in 45nm cmos technology

R. Nagulapalli, K. Hayatleh, S. Barker, S Zourob
Faculty of Technology, Design and Environment
Oxford Brookes University, Wheatley Campus, Oxford
OX33 1HX United Kingdom.
Raja.cedt@gmail.com

A Venkatareddy
Electronics and Communication
NIT Goa, Goa
India
reddyvenkat59@gmail.com

***Abstract*—In this paper a novel CMOS temperature and supply voltage independent current reference has been proposed. This design is based on the subtraction of two scaled version PTAT (proportional to absolute temperature) currents to provide a temperature independent current reference. The design was simulated with Spectre, and implemented in 45nm CMOS technology. Simulation results shows that the proposed current reference achieves temperature coefficient of 22ppm/^{0}C against temperature variation of -40^{0}C –120^{0}C and line sensitivity of 337ppm/V against supply variation of 0.6–1.8V, while consuming 135uW from 1.8V supply and occupying 5184um2**

Keywords—current reference; PTAT; voltage independent; temperature independent; MOS.

I. INTRODUCTION

The Current Reference circuit is an essential building block in many modern digital and analog circuits. It provides an accurate and temperature independent current as a reference for the rest of the circuitry. The attribute of any reference circuit is that its current should be independent of temperature and supply voltage, have low standby power, low noise and ideally lower cost. The most common solution is based on the sum of PTAT (proportional to temperature) and CTAT (complementary to absolute temperature) methods to cancel the temperature variation, which can be implemented in a standard CMOS technology by exploiting parasitic vertical bipolar junction transistors (BJTs) [1-2]. Unfortunately, BJT-based references usually occupy more die area compared to other solutions with the same power consumption, thus the cost of the chip increases. Often, models of BJTs are incorrect by a significant percentage, and the current gain (β) of a vertical BJT is smaller, and sometimes even less than 1. Therefore, it is generally preferred to have a MOSFET only current reference if it can provide comparable performance to bandgap reference [3]. But this work relays on subthreshold biasing of the main transistors, which has significant temperature and process dependent and often subthreshold transistors model could off large percentage. The current reference proposed in [4] uses temperature dependency of MOS threshold voltage, but this shows significant process variation, which leads to the need for calibration circuitry for accuracy. Other types of current references [5-6] compensate for the temperature dependence of the carrier mobility to further improve the temperature performance. Unfortunately, these references are seriously influenced by threshold voltage variation caused by process variations, trimming must be implemented when high performance is needed. A low power current reference is proposed in [7], but this needs multiple threshold transistors, which leads to extra mask costs.

II. PROPOSED CIRCUIT PRINCIPLE

The main principle behind the proposed reference follows. By subtracting two PTAT references with different slopes we can get zero temperature coefficient. For example, if we assume that the first PTAT reference has α temp coefficient and the 2nd PTAT reference has β temp coefficient, then by subtracting β times first reference current from α times the second reference will give a theoretically perfect temperature compensation. Since this technique relies on subtraction, any process variation which are common to both PTAT's will cancel, hence providing a very stable reference.

III. PTAT DESIGN

Out of available PTAT current generators a CMOS beta multiplier [9] as shown in fig. 1 was chosen because it is self-biasing arrangement and does not require the use of BJTs. MOSFETs P2, P1 are used to force the current through each leg of the circuit. The size of MOSFET N1 is made larger than N2, and therefore its trans conductance is also larger due to same current and larger size, so that the difference in the gate to source voltage of N1 and N2 is dropped across Rs.

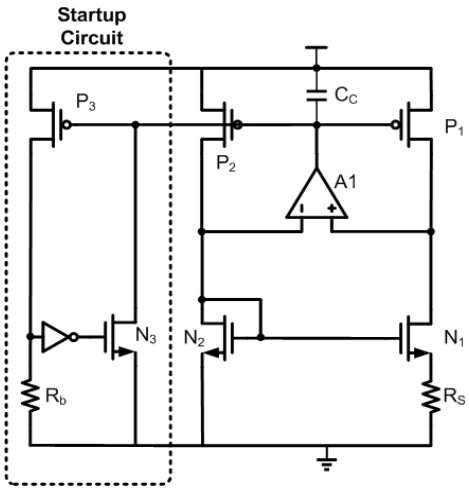

Fig. 1. Self bias PTAT circuit

For example, if Transistor N1 has a size ratio of K times compared to the size of N1, such that Vgs1 is $\frac{1}{\sqrt{K}}$ smaller than Vgs2. Opamp A1 forces the PMOS to have equal currents with a larger loop gain, and makes sure drain to source voltage of P1, P2. Resister Rs is degenerating Transistor N1, hence it creates negative feedback, with a loop gain of gmn1.Rs, whereas the total circuit configuration has positive feedback, with a loop gain of

$$\frac{\frac{1}{gmn_2}}{R_S+\frac{1}{gmn_1}} \qquad (1)$$

Where gmn1 and gmn2 are the transconductances of transistors N1 and N2. The relation between gmn1,gmn2 is given by $gmn_1 = \sqrt{K}.gmn_2$ (2)

For stable reference, always the negative feedback loop gain should be larger than the positive feedback loop gain. Overall loop gain can be derived as

$$Loopgain = \frac{1}{2-\sqrt{\frac{1}{K}}} \qquad (3)$$

From equation (3), we can conclude as long as K is greater than 1, the reference loop will be stable. In the present design, it has been chosen as 4. By applying KVL around N1, N2, Rs loop

$VGS_{n2} = VGS_{n1} + IR_s$ and by substituting square law of MOSFET current

$$V_{th} + \sqrt{\frac{2I}{U_n C_{ox}\frac{W}{L}}} = V_{th} + \sqrt{\frac{2I}{KU_n C_{ox}\frac{W}{L}}} + IR_S \qquad (4)$$

By solving equation (4) we can deduce Current through N1 as follows.

$$I_{N1} = \frac{2}{U_n C_{ox}\left(\frac{W}{L}\right)}\frac{1}{R_S^2}\left(1-\frac{1}{\sqrt{K}}\right)^2 \qquad (5)$$

From the equation (5), it is evident that current is having PTAT nature because mobility is inversely proportional to temperature. Intuitively, the voltage across resister Rs is the difference of two NMOS V_{GS} which is again PTAT, hence the current is also PTAT. More importantly, the slope of the current versus temperature characteristics depends on resistor Rs, so by using different values of resister we could get different slopes. To get the temperature independent current, PTATs with different values of K (ratio of both NMOS sizes) can be used. Since it is a self-biased reference, to force the circuit into non-zero current more a startup circuit consists of Rb,N3,P3, Inverters. Whenever there is no current, transistor N3 pulls some current from node x, such that the circuit will move towards its desired operating point. The self-bias loop has been compensated by creating a dominate pole with 0.5pF capacitor from supply to the opamp.

The opamp used in the PTAT reference should have sufficient gain as well as less offset. The major problem with offset is that it will vary with the temperature, which in turn disturbs the PTAT operation. Often, chopper stabilization is the preferred choice for zero offset amplifier, but this technique requires a low-frequency clock and a large RC filter to filter the clock feedthrough in the reference current. To have minimal offset and without using external components, a self-bias principle based opamp has been used as shown in Fig. 2. Transistors M_{21}-M_{25} form a differential pair with a current source load. Global feedback sets Vn, which is the voltage from opamp output to ground and is used to control the drain current in M26. This current is fedback through M27 and M25 to self-bias the input differential pair. Transistor M28 is replica of M22 and level shifts Vn down to equalize the drain-source voltages of M27 and M25, avoiding a systematic gain error in the self-bias loop. Though this opamp is self-biased, it does not require any startup circuit because the PTAT circuit will kick-start from zero current operating point.

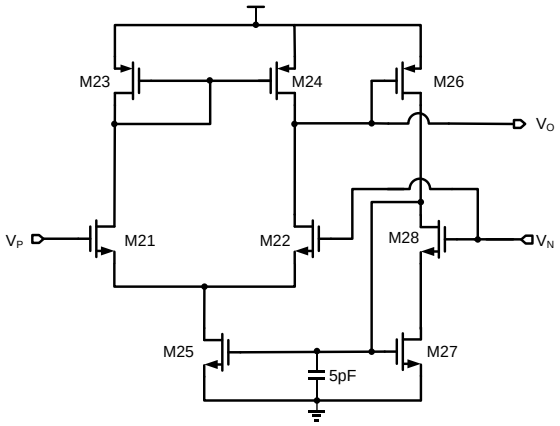

Fig. 2. Self bias opamp

To operate M_{25} in saturation, opamp input common mode voltage should be greater than the sum of M_{21} V_{gs} and overdrive voltage of M_{25}. To keep the self-bias loop stable, a 5pf capacitor has been used as a compensation capacitor at the gate of M_{25}. Size of all transistors chosen were very large to minimize mismatch. Total static current used in the opamp is ~2.5uA and most of the devices are in sub-threshold such that it can work with low current. Loop gain across PVT (process, Voltage, temperature) corners is 40dB, and worst case offset voltage is ~0.3mV. Fig. 3 shows the opamp offset across 100 Monte Carlo points (ran with 3-Sigma models). Fig. 4 shows how offset voltage varies across temperature, and describes offset with self-bias, and without self-bias (a fixed bias has been used for M_{25})

Checking whether a start up a works reliably or not is always a difficult task. There has not been any systematic approach for startup circuit reliability testing in any of the previously reported work. In this case, testing was done by adding a voltage source between the opamp

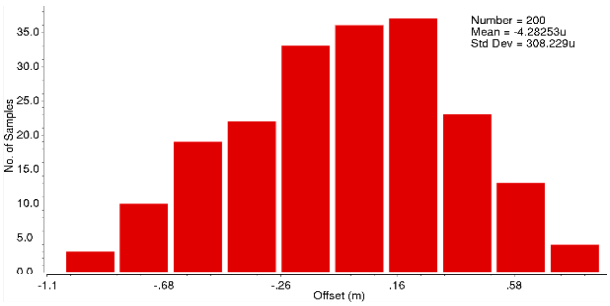

Fig. 3. Opamp offset

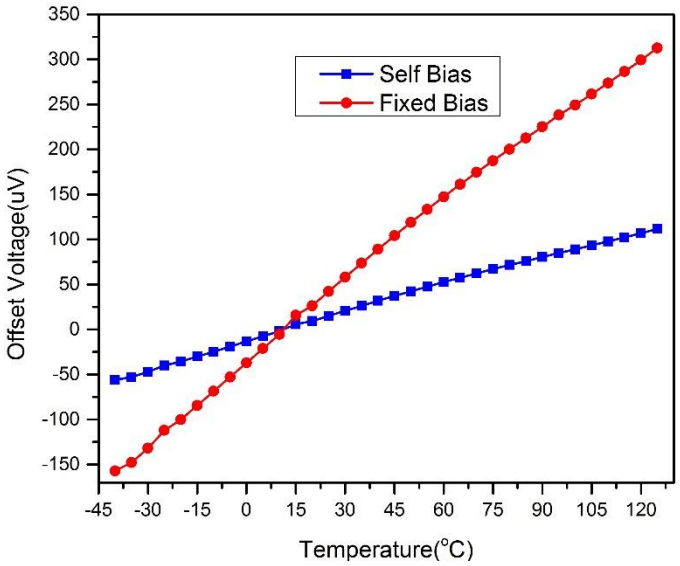

Fig. 4. Opamp offset variation with Termpearture

output (Gates of the pmos transistors) and the ground, and swept in the simulation and plotted the current through voltage source. If the circuit has a single operating point, then current will cross zero ampere point one time. Graph crosses zero ampere point when voltage source value equal to the actual opamp output bias value.

IV. Current Reference Implimentation Details

As outlined in the introduction, the current reference generator proposed is based on the subtraction of two PTAT currents with a scaling factor (6 in the present design, which varies with

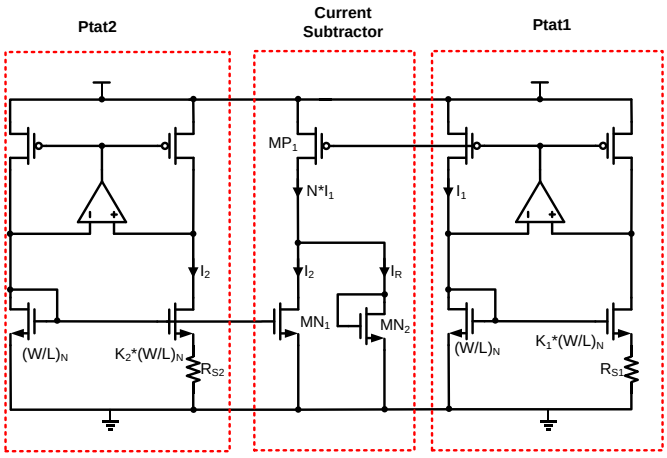

Fig. 5. Opamp offset

differing technologies). Fig. 5 shows a circuit diagram without the start up circuits. PTAT-2 current is flowing through MN_1 and a 6 times scaled version of PTAT-1 current is flowing through MP_1. To subtract these two currents, MP_1, MN_1 are connected in series, such that difference in the current flows into any available low impedance node. A diode connected transistor MN_2 is used to extract the difference current. This circuit provides protection against supply variation, because whenever the supply voltage changes, the opamp creates the same effect on PMOS transistors gate, hence up to the loop bandwidth frequency any supply noise will be rejected by the loo. This supply rejection is very important, especially in applications where there is lot of supply noise being generated though simultaneous switching noise by digital gates in SOC (System on Chip) configurations. Different device currents can be quantified as follows.

$$I_{MP1} = N \frac{2}{U_n C_{OX} \frac{W}{L}} \frac{1}{R_{S1}^2} \left(1 - \frac{1}{\sqrt{K1}}\right)^2 \quad (6)$$

$$I_{MN1} = \frac{2}{U_n C_{OX} \frac{W}{L}} \frac{1}{R_{S2}^2} \left(1 - \frac{1}{\sqrt{K2}}\right)^2 \quad (7)$$

$$I_{MN2} = N \frac{2}{U_n C_{OX} \frac{W}{L}} \frac{1}{R_{S1}^2} \left(1 - \frac{1}{\sqrt{K1}}\right)^2 - \frac{2}{U_n C_{OX} \frac{W}{L}} \frac{1}{R_{S2}^2} \left(1 - \frac{1}{\sqrt{K2}}\right)^2 \quad (8)$$

Mobility μ_n varies with temperature as $\mu_{n=} \mu_o \left(\frac{T}{T_0}\right)^{-2}$

Differentiating the equation (8) with respect to temperature and equating to Zero, gives the relationships amongst N, K_1, K2, Rs_1, Rs_2 to minimize temperature drift. The temperature and supply independent current reference circuit does not require more than two transistors in a branch, and this is the reason why the circuit is working properly up to 0.6V starting from 1.8V.

V. Current Reference Simulation Results

The proposed circuit is implemented in TSMC 45nm 1P9M CMOS process, and post layout simulations were carried out on the extracted circuit. Simulation on the temperature characteristic is carried out from -40℃ to 125℃ (industrial temperature range). Fig. 6 shows the change of I_{REF} with respect to temperature. The reference current is 30uA with a fluctuation of 110nA from -40℃ to 125℃, which shows a temperature coefficient (TC) of 22 ppm/℃.

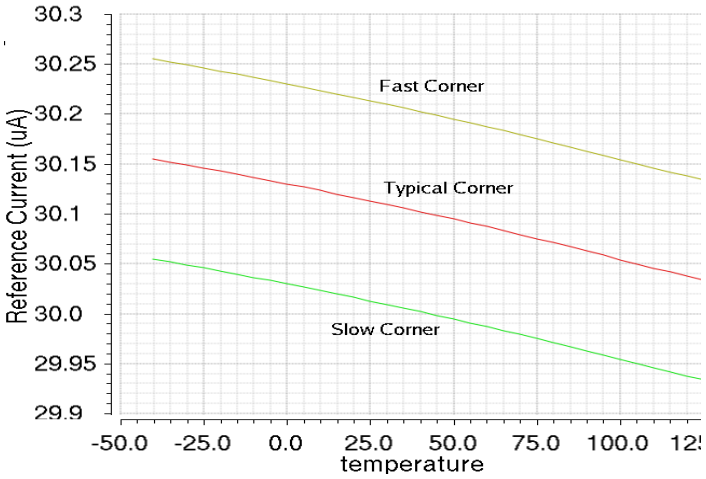

Fig. 6. Change of Iref versus temperature

Simulations were carried out for fast, slow, typical corner variations and total variation is 200nA. Such a small variation is due to the cancellation of all variations common to both PTAT generators. Like any reference generator, accuracy is very important, because this indicates how much variation the circuit will exhibit when it is mass production. 200 Monte Carlo simulations were run on the total circuit at -40^{0}C, and the circuit is accurate up to 0.1% of the mean designed reference current. The mean is 30uA and the sigma is 30nA. Fig. 7 shows the Monte Carlo variation of the reference current. The reference generator current is within 1% of the designed value of 30uA when its power supply dropped up to 0.6V from 1.8V. The minimum power supply voltage is limited by the self-bias opamp operation, but not the PTAT reference core. Fig. 8 shows how the current varied when power supply is swept from 0 to 1.8V.

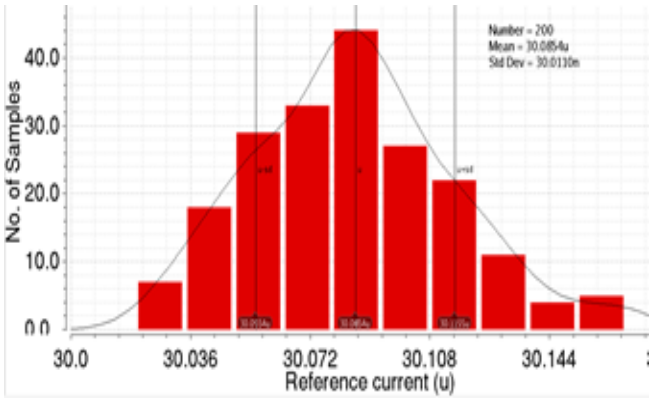

Fig. 7. Montecarlo variation of reference current

The layout of the proposed circuit is shown in Fig. 9, and the active area is 81um*64um. Every transistor has been laid with care to minimize mismatch. Special care has been taken to minimize the well proximity effect (WPE) and Shallow trench isolation (STI), by adding enough dummies for each device and keeping MOSFET away from NWELL.

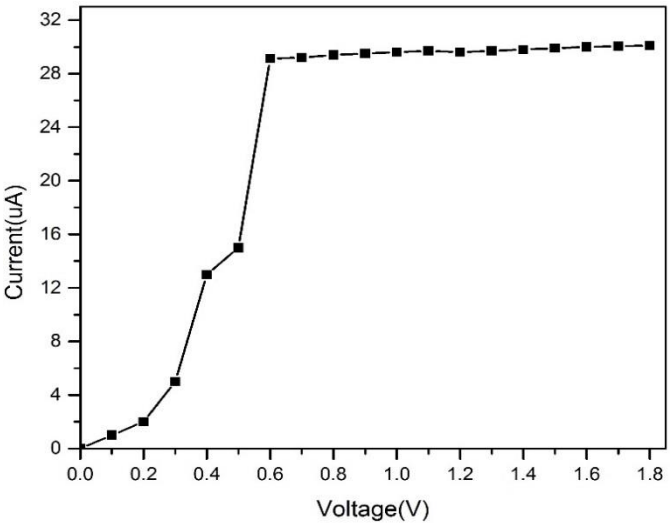

Fig. 8. Power supply voltage verses reference current

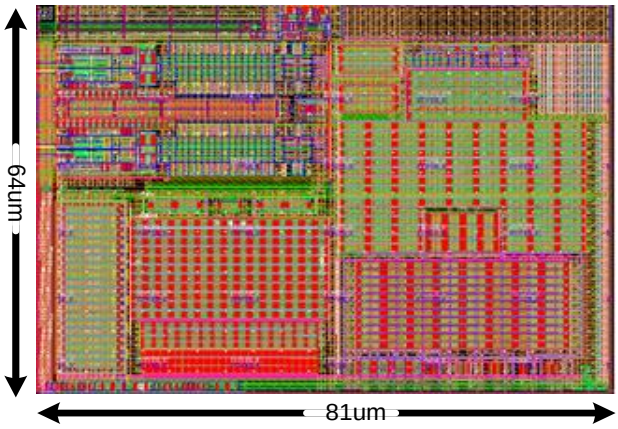

Fig. 9. The Layout of the reference generator.

VI. Conclusion

This paper has proposed an improved Constant current reference generator which has been implemented in 45nm CMOS, and presented all the relevant test results. This circuit generates 30uA current with a temperature drift of 22ppm/^{0}C in the temperature range -40 to +125^{0}C. Designed for 1.8V power supply voltage, it dissipates 135uW power and is accurate within 0.1%.

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