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Electrical characteristics of nearly relaxed InAs/GaP heterojunctions

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The electrical properties of lattice mismatched InAs/GaP heterojunctions are examined. In spite of a high dislocation density at the heterointerface, the current versus voltage characteristics show nearly ideal behavior with low reverse leakage currents and high breakdown voltages. The forward current varied exponentially with bias displaying ideal factors of 1.10 or less. Band offsets estimated from current–voltage and capacitance–voltage analysis are consistent with previous estimates based on differences in Schottky barrier heights. © *1997 American Institute of Physics*. [S0003-6951(97)00112-5]

Compound semiconductor devices are typically grown on substrates with a matching lattice constant. For lattice mismatched systems, various kinds of strain relaxation layers are used to reduce the density of threading dislocations which propagate into the active layers. These 60°-type, threading dislocations typically pin the Fermi level and provide nonradiative recombination centers that degrade the optical and electrical performance of devices. Recently, Chang et al. reported that by growing InAs directly on GaP(100) by molecular beam epitaxy (MBE), the epilayer relaxes via the formation of an array of 90°-type, edge dislocations at the heterointerface.¹ The density of the threading dislocations is relatively low. This nearly relaxed InAs/GaP material system with low threading dislocation densities shows promise for device applications. For example, the nearly relaxed InAs layer (typically 2-20 nm thick) is lattice matched to the In_{0.8}Ga_{0.2}As/In_{0.8}Al_{0.2}As system, which could provide a lattice matched heterostructure system for long-wavelength emitters and detectors and other small band gap devices. To assess the device potential for this technology, we examine the electrical characteristics of nearly relaxed InAs/GaP heterojunctions. In spite of the large lattice mismatch ($\approx 11\%$) and high density of 90°-type dislocations, the electrical characteristics are surprisingly good, showing nearly ideal forward and reverse bias behavior.

The growth of InAs on GaP was performed in a solid source GEN-II MBE system equipped with valved phosphorous and arsenic crackers. Valved phosphorus crackers have been demonstrated to be a viable growth technique for phosphides in solid-source MBE.²⁻⁴ Both InGaP and InP based devices have been achieved. In this letter, InAs was grown on GaP forming an abrupt heterojunction with an 11% mismatch.¹ The GaP(100) substrate was heated to 660 °C for oxide desorption, then GaP was grown at 600 °C. For some samples, a 20 period GaP/AlGaP (5 nm/5 nm) superlattice was incorporated as a barrier for impurities diffusing from the substrate. (Low temperature photoluminescence measurements showed that the intensity of the sulfur-bonded exiton was greatly reduced by this technique.) After growth of *N*- or *P*-type GaP, the substrate temperature was lowered to 350 °C for the growth of InAs. A thin (2-20 nm) InAs layer was deposited two dimensionally under slightly In-rich conditions followed by a thicker (200 nm) $In_{0.8}Ga_{0.2}As$ layer which is closely lattice matched to the nearly relaxed InAs. Subsequent atomic force spectroscopy (AFM) studies showed a high density of defects thought to be In droplets caused by the In-rich growth conditions necessary for twodimensional growth. (Subsequent optimization of growth parameters has greatly reduced the density of these defects.)

Four different samples, which represent the four possible InAs/GaP isotype and anisotype heterojunctions, were grown. These samples are denoted as n^+N , p^+P , n^+P , and p^+N , where the capital letter refers to the large band gap side (GaP) and the small letter to the small band gap side (nearly relaxed InAs). The film structures, targeted thicknesses, and doping densities are summarized in Fig. 1. Diodes were fabricated by first patterning with photoresist then depositing a 200/100/10 nm Au/Ti/Au metallization layer for Ohmic contacts (the same metallization was used for both n^+ - and p^+ -In_{0.8}Ga_{0.2}As top layers). Mesas were then formed by selectively wet etching the exposed In_{0.8}Ga_{0.2}As and the underlying InAs until the GaP interface was reached. The diode sizes ranged from 30×40 to $480 \times 750 \ \mu m^2$. Backside ohmic contacts for both N^+ - and P^+ -GaP substrates consisted of pure In.

Current–voltage measurements were performed using an HP-4145 parameter analyzer in a dark environment, and the capacitance–voltage measurements were performed at frequencies between 10 kHz and 1 MHz using an HP-4275A impedance analyzer. To extract activation energies, samples were tested under vacuum using an HP-4142 while varying the temperature from 200 to 300 K.



FIG. 1. Illustration of the film structures used for the $In_{0.8}Ga_{0.2}As/$ InAs/GaP diodes.

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FIG. 2. Linear current vs voltage characteristics of four typical diodes. The size of the diodes was $90 \times 120 \ \mu m^2$ and the measurement temperature was 23 °C.

Figures 2 and 3 show the measured I-V characteristics of typical diodes. As shown in Fig. 2, the forward biased currents displayed a "turn-on" voltage that increased in the order p^+P , n^+P , n^+N , and p^+N , which suggests that $\Delta E_C > \Delta E_V$, as expected for this material system.⁵ In reverse bias, all diodes showed low leakage currents and breakdown voltages consistent with avalanche breakdown in the GaP. The differences can be attributed to differences in the doping density of the GaP layers. Critical fields of 8×10^5 and 1×10^6 V/cm were estimated for the n^+N and p^+P structures, respectively; these values are about 80% of the theoretical values.⁶ Edge effects at the corners of the rectangular diodes or field enhancements at the defects revealed by AFM are possible causes for the lowered critical field. The "soft" breakdown characteristics displayed in Fig. 2 may indicate thermionic field emission.⁷

Figure 3 shows the forward-biased I–V characteristics of typical diodes. All devices displayed an exponential characteristic with an ideality factor, n, between 1.04 and 1.10 over at least three orders of magnitude. At a given bias, the magnitude of the forward current decreased in the order, p^+P , n^+P , n^+N , and p^+N , which reflected the differences in turn-on voltages observed in the linear plots. We note that some of the p^+N diodes displayed a small shunt leakage current, but no such leakage was observed in the other diodes. This may indicate that the p^+ -InAs layer in the anisotype heterojunctions is somewhat more susceptible to defects possibly because of Fermi-level pinning near the conduction band.

The forward biased currents can all be fit to a Schottkybarrierlike expression of the form,



FIG. 3. Logarithmic forward current vs voltage characteristic of the four diodes. The size of the diodes was $270 \times 360 \ \mu m^2$ and the measurement temperature was $23 \ ^{\circ}C$.

$$J = A^{**}T^2 e^{-q\phi_b/k_B T} [e^{qV/nk_B T} - 1],$$
(1)

where A^{**} is an effective Richardson contact, *n* is the ideality factor, and ϕ_b the barrier height. A form like this might be expected for the isotype heterojunctions which operate much like Schottky barriers, but Schottky-barrierlike characteristics also occur in anisotype heterojunctions when the barrier height is large.⁸ By performing temperature-dependent measurements from ≈ 200 to 300 K and plotting $\ln(J/T^2)$ versus 1/T at a fixed bias, the barrier heights were deduced, and the results are listed in Table I.

Reverse biased C–V measurements were also performed. No hysteresis was observed as the bias voltage was swept, and the results were independent of frequency between 10 kHz and 1 MHz. Plots of $1/C^2$ versus V_{rev} were linear, so the doping density of the lightly doped GaP could easily be deduced. The results, along with the built-in voltages as obtained from the intercept voltages, are also listed in Table I.

The measured I–V and C–V characteristics are generally consistent with the expected band offsets for this material system,⁵ but a precise determination is clouded by several uncertainties. One is the nature of transport across the heterointerface, which involves an indirect semiconductor, GaP, and a direct one, InAs.⁹ Other uncertainties include Fermi level pinning which may occur at the interface as well as possible interface charges and dipoles. As a first order analysis, we ignore these complications and interpret the results in terms of ideal band line ups. For n^+N (p^+P) diodes, the barrier height is the conduction (valence) band discontinuity minus the position of the Fermi level within the

TABLE I. Summary of the I-V and C-V measurements and the conduction and valence band discontinuities deduced from the I-V barrier heights and C-V intercept voltages.

	I–V			C–V		
Diode	n	ϕ_b (eV)	ΔE (eV)	$N_B(\mathrm{cm}^{-3})$	V_{bi} (V)	ΔE (eV)
$p^{+}P$ $n^{+}N$ $p^{+}N$ $n^{+}P$	≈ 1.10 ≈ 1.07 ≈ 1.08 ≈ 1.04	0.59 0.98 1.40 1.13	$\Delta E_V = 0.59$ $\Delta E_C = 1.01$ $\Delta E_C = 0.90$ $\Delta E_V = 0.60$	$\begin{array}{c} 3.3 \times 10^{17} \\ 1.1 \times 10^{17} \\ 1.6 \times 10^{17} \\ 1.3 \times 10^{17} \end{array}$	0.79 1.19 1.44 1.05	$\Delta E_V = 0.88$ $\Delta E_C = 1.35$ $\Delta E_C = 1.06$ $\Delta E_V = 0.63$

 $n^+(p^+)$ InAs. For n^+ -InAs, we estimate that the Fermi level lies about 0.23 eV within the nonparabolic conduction band. At the same time, however, heavy doping effects in the n^+ -InAs will shrink the band gap by roughly 0.2 eV thereby lowering the Fermi level.¹⁰ Accounting for these effects, we extracted barrier heights of the isotype heterojunctions from the I–V and C–V data and report the results in Table I.

For the p^+N (n^+P) anisotype heterojunctions, the barrier height is the conduction (valence) band discontinuity plus the band gap of the nearly relaxed InAs, plus the Fermilevel penetration into the valence (conduction) band of the relaxed InAs. We estimate the band gap of the nearly relaxed InAs to be ≈ 0.5 eV, the band gap of In_{0.8}Ga_{0.2}As, which has the same lattice constant. Again, we have the same uncertainties regarding the position of the Fermi level and the band gap narrowing effects. Accounting for them, we estimate the band offsets for the anisotype heterojunctions and report the results in Table I.

As estimated from Schottky barrier height differences, and band line ups for this material system are expected to be $\Delta E_C \approx 1.4 \text{ eV}$ and $\Delta E_V \approx 0.4 \text{ eV}$.⁵ Although there is some spread in the results, Table I shows that the observed conduction band discontinuities were much larger than those for the valence band. For ideal heterojunctions, we expect $\Delta E_C + \Delta E_V + E_G$ (nearly relaxed InAs)= E_G (GaP)=2.27 eV. This is roughly true for the C–V results of the anisotype heterojunctions and the I–V results, but the C–V results for the isotype heterojunctions give anomalously high values. The smaller ΔE_C obtained from the p^+N I–V data as compared to the n^+N data could be explained by Fermi-level pinning of the relaxed p^+ -InAs/N-GaP interface, and the high values obtained by C–V analysis for the isotype heterojunctions may indicate the presence of interfacial charges. In summary, the vertical transport properties of isotype and anisotype nearly related InAs/GaP heterojunctions were examined. The resulting I–V characteristics have nearly ideal, Schottky-barrierlike, forward bias characteristics, and low leakage in reverse bias. The conduction band offsets are larger than the valence band offsets and their magnitudes are in general agreement with expectations. This near-ideal behavior is obtained in the presence of a high density of dislocations in the plane of the heterointerface. These results suggest a number of potential device possibilities with p^+P^+ InAs/GaP heterojunctions suitable for providing Ohmic back contacts and the n^+N and anisotype junctions providing rectification.

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- ¹J. C. P. Chang, T. P. Chin, and J. M. Woodall, Appl. Phys. Lett. **69**, 981 (1996).
- ²G. W. Wicks, M. W. Koch, J. A. Varriano, F. G. Johnson, C. R. Wie, H. M. Kim, and P. Colombo, Appl. Phys. Lett. **59**, 342 (1991).
- ³J. N. Baillargeon, A. Y. Cho, F. A. Thiel, R. J. Fischer, P. J. Pearah, and K. Y. Cheng, Appl. Phys. Lett. **65**, 207 (1994).
- ⁴T. P. Chin, W. L. Chen, G. I. Haddad, J. C. P. Chang, and J. M. Woodall, J. Vac. Sci. Technol. B **14**, 2225 (1996).
- ⁵S. Tiwari and D. J. Frank, Appl. Phys. Lett. **60**, 630 (1992).
- ⁶S. M. Sze, *Physics of Semiconductor Devices* (Wiley, New York, 1981).
- ⁷E. H. Rhoderick and R. H. Williams, *Metal-Semiconductor Contacts*, 2nd
- ed. (Clarendon, Oxford, 1988), pp. 89-140.
- ⁸M. S. Lundstrom, Solid-State Electron. 29, 1173 (1986).
- ⁹A. A. Grinberg, Phys. Rev. B **33**, 7256 (1986).
- ¹⁰S. C. Jain, J. M. McGregor, and D. J. Roulston, J. Appl. Phys. 68, 3747 (1990).