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M. P. Patkar

Purdue University, School of Electrical Engineering

T. P. Chin

Purdue University, School of Electrical Engineering

J. M. Woodall

Purdue University, School of Electrical Engineering

Mark S. Lundstrom

Purdue University, School of Electrical Engineering, lundstro@purdue.edu

Michael R. Melloch

Purdue University, School of Electrical Engineering, melloch@purdue.edu

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Very low resistance nonalloyed ohmic contacts using low-temperature molecular beam epitaxy of GaAs

M. P. Patkar, T. P. Chin, J. M. Woodall, M. S. Lundstrom, and M. R. Melloch^{a)}
School of Electrical Engineering, Purdue University, West Lafayette, Indiana 47907-1285

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Ex situ nonalloyed ohmic contacts were made to *n*- and *p*-type GaAs using low-temperature molecular beam epitaxy. For *n*-type GaAs, Ag, and Ti/Au nonalloyed contacts displayed specific contact resistivities of mid $10^{-7} \Omega \text{ cm}^2$. For *p*-type GaAs, nonalloyed Ti/Au contacts with specific contact resistivities of about $10^{-7} \Omega \text{ cm}^2$ were obtained. © 1995 American Institute of Physics.

Alloyed ohmic contacts have been used extensively for GaAs devices. In this technique, the contacts are made by depositing the metal/dopant film followed by annealing, which forms an ohmic contact. Alloyed Au–Ge contacts for *n*-GaAs and Au–Zn contacts for *p*-GaAs have resulted in ρ_c on the order of $10^{-6} \Omega \text{ cm}^2$.^{1–4} However, alloyed contacts produce rough interfaces that do not make good reflectors needed for many optoelectronic devices. For nonalloyed contacts, a high doping density at the surface is required to produce a tunneling contact. Unfortunately, for Si-doped, *n*-type GaAs, the bulk doping density is limited to $N_D - N_A \approx 5 \times 10^{18} \text{ cm}^{-3}$. During molecular beam epitaxy (MBE) of Si-doped, *n*-GaAs, however, very high values of $N_D - N_A$ ($\approx 10^{20} \text{ cm}^{-3}$) occur in a thin layer at the surface because of the Fermi level being pinned at the surface.⁵ Such a layer should facilitate nonalloyed ohmic contacts, but the native oxide that forms and the subsequent oxide etch that is done prior to metal evaporation removes most of this high space charge density layer at the surface. *In situ* deposition of Ag on MBE Si-doped GaAs has, however, produced ohmic contacts with a ρ_c of mid $10^{-7} \Omega \text{ cm}^2$.⁵ Schubert *et al.*⁶ have demonstrated nonalloyed contacts with a ρ_c of $2.5 \times 10^{-6} \Omega \text{ cm}^2$ to *n*-GaAs using a delta-doped layer a few lattice constants below the GaAs surface. Yamamoto *et al.*⁷ have shown that *ex situ* nonalloyed ohmic contacts can be formed on low-temperature grown (LTG) GaAs with a ρ_c of $1.5 \times 10^{-3} \Omega \text{ cm}^2$. In this letter, we describe a new technique that passivates the high space charge density layer on the surface of MBE *n*-GaAs with a layer of LTG GaAs thereby permitting *ex situ* nonalloyed ohmic contacts with a ρ_c of mid $10^{-7} \Omega \text{ cm}^2$.

Nonalloyed ohmic contacts are readily made to p^{++} GaAs, but for Be concentrations above $\approx 5 \times 10^{19} \text{ cm}^{-3}$, high concentrations of interstitial Be occur. Interstitial Be is a donor that compensates the doping, and it diffuses rapidly at low temperatures, which leads to stability problems. Low-temperature growth (LTG) has been used in the past to improve the Be doping efficiency in GaAs⁸ and InGaAs devices.⁹ In this letter, we describe a LTG and a subsequent anneal that drives interstitial Be onto acceptor sites giving a higher *p*-type doping, giving a lower ρ_c , and improving the film's stability.

Consider first the nonalloyed contacts to *n*-GaAs. Si can

act as a donor or an acceptor in GaAs with the equilibrium ratio of donors to acceptors given by⁵

$$\frac{N_D}{N_A} = K(T) \times \frac{n_i^2}{n^2} \times P_{\text{As}_2}, \quad (1)$$

where $K(T)$ is a temperature-dependent constant incorporating the equilibrium arsenic pressure over GaAs. P_{As_2} is the arsenic dimer pressure, n is the concentration of electrons in GaAs, and n_i is the intrinsic carrier concentration in GaAs. During MBE of GaAs using an excess As flux, the Fermi level is pinned at the surface such that $E_c - E_f$ is approximately midgap,¹⁰ so at the surface, the electron concentration n is very near n_i . According to Eq. (1), therefore, almost all the Si atoms should go onto donor sites at the surface. In the bulk, however, n is much greater than n_i , and according to Eq. (1), some Si atoms switch from donor sites to acceptor sites causing the N_D/N_A ratio to decrease.

To preserve the surface layer of *n*-GaAs with high Si concentration ($\approx 10^{20} \text{ cm}^{-3}$) even after exposing the sample to the atmosphere, the surface must be passivated. We chose this passivation layer to be LTG, undoped GaAs, which has an excess of As scattered through its volume causing numerous midgap states¹¹—the band diagram is shown in Fig. 1. Carrier transport through the high space charge density *n*-GaAs layer is by tunneling, and transport through the LTG GaAs layer is expected to be due to defect assisted tunneling.

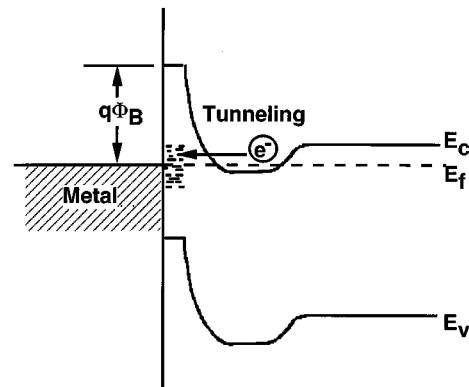


FIG. 1. Schematic band diagram for *n*-GaAs contacts. The diagram shows tunneling conduction through the high space charge density layer. The carriers then hop through the midgap states in low-temperature grown GaAs.

^{a)}Electronic mail: melloch@ecn.purdue.edu

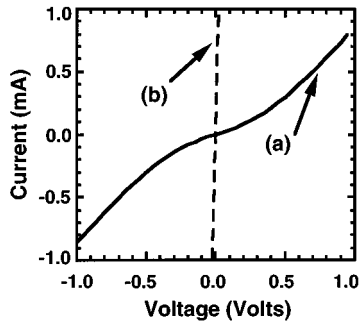


FIG. 2. I - V characteristics for Ag contacts: (a) solid line, without low-temperature grown GaAs layer and (b) dashed line, with low-temperature grown GaAs layer.

Turning now to Be-doped, p -GaAs, the ratio of Be atoms on acceptor sites to Be atoms on donor sites is given by¹²

$$\frac{N_A}{N_D} = K'(T) \times \frac{n_i^2}{p^2} \times (P_{As_2})^{0.5}, \quad (2)$$

where $K'(T)$ is a temperature dependent constant, P_{As_2} is the arsenic dimer pressure, p is the hole concentration in GaAs, and n_i is the intrinsic carrier concentration in GaAs. If heavily doped p -GaAs is grown at low temperature by MBE, excess As will be incorporated in the p -GaAs bulk. If this LTG p -GaAs is annealed subsequently under As over pressure, the excess As in the bulk should drive the interstitial Be atoms onto acceptor sites, while the excess As should go onto regular As sites in the lattice.

The n -GaAs and p -GaAs structures described above were grown by MBE in a Varian GEN II system. For the n -GaAs structures, the heavily doped n -GaAs layer was grown on a semi-insulating GaAs substrate at 600 °C using As_4 instead of As_2 . The V/III flux ratio was approximately 2. A resistively heated Si filament was used to produce high fluxes of the n -type dopant. The LTG caps on the heavily doped n -GaAs layers were grown at 250 °C. Films with LTG caps with thicknesses ranging from zero to 50 Å were grown. The p -GaAs structures consisted of a GaAs film heavily doped with Be grown on a semi-insulating substrate. Three structures were grown; a p^{++} -GaAs layer grown at 600 °C, a p^{++} -GaAs layer grown at 300 °C, and a p^{++} -GaAs layer grown at 300 °C that was annealed at 600 °C under As over pressure.

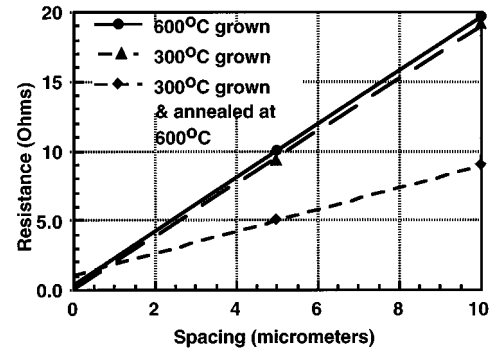


FIG. 3. Resistance vs spacing for various transmission lines made on p -GaAs contact structures.

Transmission line measurements (with the contact spacing varying from 5 to 320 μm) were used to characterize the specific contact resistivity. The transmission lines were fabricated by using conventional photolithographic and wet etching techniques. Ag and Ti/Au were used as metals for the contacts to n -GaAs because we expect their reactivity with GaAs to be less than that of Au (i.e., there would be less possibility of Ag or Ti spiking through the thin LTG GaAs and the thin high space charge density layers). We evaporated 1000 Å of Ti and 1000 Å for the Ti/Au contacts and 2500 Å of Ag for the Ag contacts. The contacts to p -GaAs were made using the Ti/Au metallization.

Figure 2 shows a comparison of the measured I - V characteristics for Ag contacts to the n -GaAs structure with and without the LTG GaAs cap. As anticipated, the sample without a cap did not yield an ohmic contact. This is probably due to the high space charge density layer being removed during the native oxide formation and the subsequent oxide etch done prior to the metal evaporation. Figure 3 plots the resistance versus spacing between the contacts for various samples. The intercept of a least-squares fit gives the contact resistance, and the slope of the line gives the sheet resistance of the channel in ohms per square.¹³ Since the contacts were not annealed, the sheet resistance of the channel underneath the contact was the same as the sheet resistance in between the contacts. The dimensions of the contacts and the spacing between them were measured under an optical microscope using a precalibrated grating. The transfer length model was then used to analyze the data and extract a contact resistance.^{14,15}

Tables I and II summarize the results of the measure-

TABLE I. Variation of the ρ_c and source/drain resistance with thickness of the LTG cap layer for n -GaAs contacts.

Thickness of the low-temperature grown cap layer (Å)	ρ_c for Ti/Au contacts ($\Omega \text{ cm}^2$)	Source/drain resistance for Ti/Au contacts ($\Omega \text{ mm}$)	ρ_c for Ag contacts ($\Omega \text{ cm}^2$)	Source/drain resistance for Ag contacts ($\Omega \text{ mm}$)
0	3.1×10^{-5}	1.1	6.9×10^{-3}	33.7
5	5.5×10^{-6}	0.42
20	4.4×10^{-7}	0.10	2.8×10^{-7}	0.09
30	2.4×10^{-7}	0.07
50	4.5×10^{-7}	0.09	1.6×10^{-6}	0.14

TABLE II. Specific contact resistivity and source/drain resistance for *p*-GaAs contacts.

Description of the sample	Specific contact resistivity ($\Omega \text{ cm}^2$)	Source/drain resistance (Ω/mm)
600 °C grown sample	1.6×10^{-8}	0.013
300 °C grown sample (nonannealed)	9.5×10^{-8}	0.003
300 °C grown sample (annealed under As over pressure at 600°C)	2.7×10^{-7}	0.037

ments of different *n*-GaAs and *p*-GaAs contact structures. For the *n*-GaAs contact structures, ρ_c of well below $10^{-6} \Omega \text{ cm}^2$ were obtained for the contact structures with LTG cap thicknesses of 20, 30, and 50 Å. Figure 4 shows the variation of the specific contact resistivity with the thickness of the LTG cap layer. The specific contact resistivity seems to decrease with the increase in the LTG cap thickness for cap thicknesses from zero to 20 Å and then seems to increase slightly after that. The low resistance for the LTG capped structures can be attributed to the fact that the high space charge density layer is protected by the LTG cap layer thus allowing a tunneling ohmic contact to be formed. The ρ_c seems to increase for LTG cap thicknesses less than 20 Å. This is probably due to part of or all of the LTG cap along with a portion of the high space charge density layer being removed during the native oxide formation and oxide etch done prior to the metal evaporation, causing the depletion layer at the contact to extend into the *n*-GaAs bulk, where the space charge density is not as high. Ti/Au contacts exhibit lower specific contact resistivities than Ag contacts to *n*-GaAs without an LTG cap. This indicates that Ag is more reactive than Ti and consumes more of the high space charge density layer.

The contacts on heavily Be-doped *p*-GaAs grown at 600 °C and the contacts on heavily Be-doped *p*-GaAs grown at 300 °C exhibited a ρ_c of about $10^{-8} \Omega \text{ cm}^2$. The specific contact resistivity for the heavily Be-doped *p*-GaAs sample grown at 300 °C and annealed under As over pressure at 600 °C was higher than the other two samples, however, the channel resistance for this sample was one-half of that of the

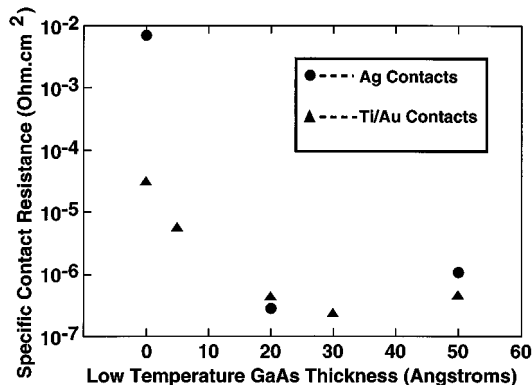


FIG. 4. Specific contact resistivity vs thickness of the low-temperature grown GaAs layer. The specific contact resistivity increases for thicknesses of the low-temperature grown layer below about 20 Å.

other two samples. This supports our hypothesis that, upon annealing, excess As in the LTG GaAs causes the interstitial Be to go onto acceptor sites, which decreases the channel sheet resistance. This result not only assures high Be doping efficiency but also assures that the Be in high concentrations does not diffuse rapidly during subsequent high-temperature processing steps. The increase in contact resistance for the annealed film is probably due to outdiffusion of Be from a few monolayers of GaAs near the surface since the surface was not passivated during the 600 °C anneal. This problem could be fixed by coating the nonannealed sample with Si_3N_4 prior to the 600 °C anneal.

In summary, we have developed a method for making nonalloyed contacts to *n*-GaAs by protecting the high space charge density layer on the surface. Specific contact resistivities of mid $10^{-7} \Omega \text{ cm}^2$ have been obtained. Heavy Be doping used in *p*-GaAs contact layers gives specific contact resistivities of about $10^{-8} \Omega \text{ cm}^2$. Annealing LTG, Be-doped ($\approx 10^{20} \text{ cm}^{-3}$) GaAs under As over pressure lowers its sheet resistance because excess As in the bulk pushes interstitial Be onto acceptor sites.

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- ¹M. Witner, T. Finstad, and M-A. Nicolet, *J. Vac. Sci. Technol.* **14**, 935 (1977).
- ²N. Lustig, M. Mularami, M. Norcott, and K. McGann, *Appl. Phys. Lett.* **58**, 2093 (1991).
- ³J. Gyulai, J. W. Mayer, V. Rodriguez, A. Y. C. Fu, and H. J. Gopen, *J. Appl. Phys.* **42**, 3758 (1971).
- ⁴B. R. Pruniaux, *J. Appl. Phys.* **42**, 3575 (1971).
- ⁵P. D. Kirchner, T. N. Jackson, G. D. Pettit, and J. M. Woodall, *Appl. Phys. Lett.* **47**, 26 (1985).
- ⁶E. F. Schubert, J. E. Cunningham, W. T. Tsang, and T. H. Chiu, *Appl. Phys. Lett.* **49**, 292 (1986).
- ⁷H. Yamamoto, Z-Q. Fang, and D. C. Look, *Appl. Phys. Lett.* **57**, 1537 (1990).
- ⁸J. L. Lievin, C. Dubon-Chevallier, F. Alexandre, G. Leroux, J. Dangla, and D. Ankri, *IEEE Electron Device Lett.* **EDL-7**, 129 (1986).
- ⁹R. A. Mertzger, M. Hafiji, W. E. Stanchina, T. Liu, R. G. Wilson, and L. G. McCray, *Appl. Phys. Lett.* **63**, 1360 (1993).
- ¹⁰A. D. Katmani, P. Chiaradia, H. W. Sang, Jr., and R. S. Bauer, *J. Vac. Sci. Technol. B* **2**, 471 (1984).
- ¹¹R. M. Feenstra, J. M. Woodall, and G. D. Pettit, *Mater. Sci. Forum* **143-147**, 1311 (1994).
- ¹²F. H. Pollack, P. Parayanthal, and J. M. Woodall, Solar Energy Research Inst., final report for subcontract ZL-4-03032-9, submitted August 1985.
- ¹³M. Shur, *GaAs Devices and Circuits* (Plenum, New York, 1987).
- ¹⁴H. Murrmann and D. Widman, *IEEE Trans. Electron Devices* **ED-16**, 1022 (1969).
- ¹⁵H. H. Berger, *Solid State Electron.* **15**, 145 (1972).

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