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Silicon Nitride Deposition, Chromium Corrosion Mechanisms and Source/Drain Parasitic Resistance in Amorphous Silicon Thin Film transistors

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SILICON NITRIDE DEPOSITION, CHROMIUM CORROSION

MECHANISMS AND SOURCE/DRAIN PARASITIC RESISTANCE

IN AMORPHOUS SILICON THIN FILM TRANSISTORS

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ABSTRACT

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Hydrogenated amorphous silicon (a-Si:H) based thin film transistors (TFTs) are finding increased application as switching elements in active-matrix liquid crystal displays (AMLCDs). Extensive research has been focussed on optimizing fabrication conditions to improve materials quality and on reducing channel length to increase device speed. However, the basic physics and chemistry have not yet been fully understood. In addition, little attention has been paid to the significant effect of source/drain parasitics.

The work described in this thesis is closely related to the speed and stability issues on the discrete device level. Specifically, the influence of gate nitride deposition and its NH_3 plasma treatment has been studied. The competing effects of nitridation reaction and radiation damage were found to cause an interesting trade-off between the device stability and speed. Further effort was devoted to the analysis of an important TFT failure phenomenon. Both electrical and spectroscopic techniques were utilized for gate Cr corrosion studies. It was determined that the corrosion was largely promoted by the CF_4 plasma exposure of Cr during the fabrication. Finally, new test structures were designed, fabricated and characterized to study the source/drain parasitic resistance.

CHAPTER 1
INTRODUCTION

1.1 Background

Thin film transistors (TFTs) have been under research for the past thirty years, but it is only in the last decade that an explosive growth has occurred in this field. Advances made in office automation and consumer electronics have stimulated increasing research activities directed at the development of a new generation of input/output devices. As the portable TV and computer became more popular it has spurred work on large area, high resolution, compact, and light weight liquid crystal display (LCD) panels. However, the conventional multiplexing or matrix addressing techniques are no longer adequate towards this end and new addressing schemes employing TFT switched arrays have to be used. Aside from the high contrast ratio and viewing angle that can be achieved, this approach allows the design of display panels with a relatively large number of scan lines and a much better grey scale to be produced.

Several TFT technologies for this purpose have been developed using a variety of semiconductor materials. These materials include hydrogenated amorphous silicon (a-Si:H), polycrystalline silicon, CdS, CdSe, InAs, InSb, PbTe, PbSe, Te and laser-crystalized silicon. Both a-Si:H and poly-Si TFTs have desirable features compared to other materials used in earlier TFTs. Besides requiring a high processing temperature of around 600 °C, polysilicon TFT also suffer from high OFF current levels such that the current ON/OFF ratio is about the same as that of a-Si:H TFT. At the present level of development, it appears that the a-Si:H TFT technology is more mature and promising. In fact, it is the leading technology in the portable TV displays now on the market, and in the computer and instrument displays that will soon join them. Advantages of a-Si:H are the proven capability of large-area deposition, the low temperature growth and fabrication process, which is compatible with cheap glass substrates, and the use of conventional Si photolithographic processes. Although the electron mobility of a-Si:H is

relatively low, films of this material exhibited extremely high dark resistance. The resulting TFTs thus have a very low OFF current as well as having a high ON/OFF current ratio. The low off-current eliminates the need of a storage capacitor adjacent to the LC for display and for other similar applications. Excellent photoconductive properties of a-Si:H and the ability to integrate photosensors and transistors over very large areas on glass substrates has also led to the development of page-wide TFT addressed document scanners.

AMLCDs today have the potential to replace almost every CRT application in terms of performance. However, they will not significantly penetrate major consumer and industrial display markets—such as television receivers, computer terminals, and automobile dashboards—until the panels can be manufactured at a cost competitive with CRTs. The foremost cost driver is the fabrication yield due to the large-area substrate involved and the lack of suitable production equipment. The second major factor responsible for the high production cost is the circuitry required to address and drive the active matrix. All the driver circuitry for the AMLCD in use today is in the form of crystalline silicon LSI chips and they are mounted on the sides of the display panel. Therefore, it is highly desirable to have "on board" circuits adjacent to the TFT switch matrix and have them implemented in the same technology on the same substrate. This would reduce the number of lead connections and hence the system cost, and also improve display reliability. The large current handling line drivers and multiplexing circuits give a degree of flexibility in the logic architecture and partitioning.

1.2 Thesis Overview

As a matrix switching elements, a-Si:H TFTs obviously have met success because the operation frequencies required are generally only in the order of a few tens of KHz. For other high speed analog and digital circuits applications, significant improvement of its current drive capability and stability need to be achieved. Although a-Si:H TFT devices have been under intensive study in the last decade, there is much room both for further understanding of the fundamental device physics and for improvement of device technologies. This thesis consists of several parts which are closely related to the speed and stability issues on the discrete device level. The goal is to promote a better understanding of the relationship between device performance and processing parameters, especially the composition of the gate nitride, and of the effect of source/drain parasitic resistance.

Chapter 2 contains a review of the relevant literature on the basic properties and preparation of a-Si:H and SiN$_x$ along with the technologies and performance of a-Si:H TFTs. Also included in this chapter are the application of a-Si:H TFTs in AMLCDs and a description of other present day TFT issues.

Chapter 3 details the effort in the deposition and characterization of the PECVD a—SiN$_x$:H gate insulator and its incorporation in initial a-Si:H TFTs. An integral part of this chapter describes the further optimization of the gate nitride in terms of the deposition RF power densities and the effect of NH$_3$ plasma treatment.

In Chapter 4, a normal staggered a-Si:H TFT process is described first and then device failures due to anomalous gate Cr corrosion are analyzed and reported. By using both electrical and spectroscopic techniques, the analysis goes further to the correlation between Cr corrosion, plasma processing and the TFT device design. A possible electrochemical corrosion mechanism is postulated.

Chapter 5 discusses the design, fabrication and characterization of the new TFTs and other test structures for source/drain parasitic resistance studies. Finally, the thesis investigation is summarized and recommendations for future work are given in Chapter 6.

CHAPTER 2
LITERATURE REVIEW

2.1 Introduction

The thin film transistor (TFT) has been under almost continuous research and development since the first practical device was reported by P.K. Weimer in 1962[1]. Initial research on TFTs made use of evaporated polycrystalline CdSe and, to some extent, cadmium sulfide (CdS) thin films. The CdSe TFTs were used for the scanning circuits of photoconductor arrays[2]. TFTs using amorphous silicon were first demonstrated in 1976 by Neudeck[3]. The evaporated a-Si was of poor quality because it had a large density of states in the mobility gap. However, the epoch-making work by Spear and LeComber[4] demonstrated that high quality n- and p-type amorphous silicon films could be deposited by doping with hydrogen in addition to donor and acceptor impurities through the glow discharge decomposition of SiH_4 gas. This stimulated research on hydrogenated amorphous silicon (a-Si:H) devices such as transistors, photovoltaic cells, and photoconductor-coated drums for copy machines, all of which required the low-temperature deposition of silicon on glass or similar substrate. The first commercial application of a-Si:H films was in the field of solar cells. Since such devices had a relatively simple structure and small area, they were suitable vehicles for the study of the properties of a-Si:H films and enabled the optimization of the deposition systems required.

Resulting from the accumulated experience with the deposition technique developed for producing a-Si:H p-n diodes for solar cells, plasma-enhanced chemical vapor deposition (PECVD) systems became available for production use. As a result of this progress, the first demonstration of an a-Si:H TFT by LeComber, Spear and Ghaith[5] led rapidly to a extensive research in many laboratories throughout the world. Although the semiconducting properties of a-Si:H are inferior to single crystal silicon, its promise for applications under the broad heading of large area integration has made a-Si:H TFT attractive as switching elements in active-matrix (AM) liquid crystal displays (LCDs) and

optical character or page readers.

Although the speed of a-Si:H TFTs at the moment are adequate for the switching transistor in the matrix, they are not fast enough for the peripheral driver circuits and other logic circuit applications, i.e., the data shift register. In part, this is due to the fundamentally low carrier mobilities of a-Si:H and therefore the lack of sufficient drive current to charge the parasitic capacitances of the AMLCD. Perhaps more important is that the field is in the very early stage of understanding both the fundamental materials properties and the device physics. There is much room for substantial improvement—a lot of problems and a lot of possibilities. This chapter will focus the present level of understanding of a-Si:H TFT technologies and device physics. The review begins with those properties of a-Si:H that are relevant to thin film transistors. Next, a overview will be given to the progress of a-Si:H TFT technologies and device modeling effort. A brief section will be then contributed to the most important a-Si:H TFT application, that of the AMLCD. Also discussed are some of the key issues that limit the performance of today's a-Si:H TFTs.

2.2. The Active Semiconductor Layer — a-Si:H

2.2.1 Basic Properties of a-Si:H

2.2.1.1 Atomic Structure

In contrast to the case of crystalline solids, amorphous solids are disordered materials. They possess no long-rang structural configuration which means there is no unit cell and no lattice. However, amorphous materials can exhibit a high degree of short-range order. For ideal a-Si, it has generally been accepted that a good first approximation to the bulk structure is the continuous random network model. The model states that (a) each Si atom has exactly four first-neighbor atoms at the same bond length as in the crystal forming a regular tetrahedron on the average, and (b) variations in the interbond angles[6] (~5%) among these neighbors lead rapidly to a loss of local order and ultimately to the absence of long-range order and therefore crystallinity.

In real a-Si, however, there are intrinsic and extrinsic defects as well as impurities. Phillips[7] has pointed out that it would be impossible to construct an infinite continuous random network without extremely large internal strain and stress. Broken bonds will therefore be formed to release the internal

tension.

In a crystal, we only need the basis vector and the translation vector to describe the position of every atom. In amorphous silicon, however, we would need three coordinates for every atom in the material. Clearly, this is impossible, with 10^{24} atoms/cm^3. As a result, one asks simpler questions like: what is the average distance to the nearest neighbors and how many neighbors are there? Thus, a type of statistical description of atomic arrangement is sought. The radial distribution functions (RDFs) can reveal this kind of information. RDFs are obtained from diffraction (x-ray, electron, neutrons) data by Fourier transformation of the intensities, after effects like incoherent and multiple scattering have been removed and geometrical phenomena like the polarization effect have been taken into account. Figure 2.1a shows radial distribution curves for amorphous silicon and for crystalline silicon as obtained by Fourier analysis of electron diffraction data[9] It was found that the first neighbor peaks in the two materials had both the same position and width, ie, Si is tetrahedrally coordinated in the crystal and also in the amorphous Si sample. Further, the nearest-neighbor separation in amorphous Si is unchanged from the crystalline case to within 1 or 2%[8, 9]. The second neighbor peak in the amorphous Si had the same position, but was slightly broader than the corresponding peak in the crystalline material. But the very strong third neighbor peak of the crystalline Si, due to 12 third neighbors, was almost completely missing from the amorphous Si's RDF. Figure 2.1b shows how tetrahedral coordination leads to the fcc unit cell of crystalline Si and how a tetrahedral structure can be preserved in the network model of amorphous Si due its one additional degree of rotational freedom.

2.2.1.2 Density of States Distribution

From the tight-bonding approximation, it can be expected that the electronic structures of both crystalline Si and amorphous Si are mainly determined by their short-range bonding structures. Therefore, their density of states should not be very different. However, the fluctuations of bond lengths and angles in the random network could introduce localized states into the energy band gap. Figure 2.2 shows a schematic representation of the density of states function. From the figure it is seen that amorphous Si has essentially two types of localized gap states, intrinsic and extrinsic[10, 11]. The intrinsic localized states are defined as those arising from the distribution of bond angles and lengths, and the extrinsic localized states are those arising from defects and impurities. Therefore, the total density of these deep midgap states also
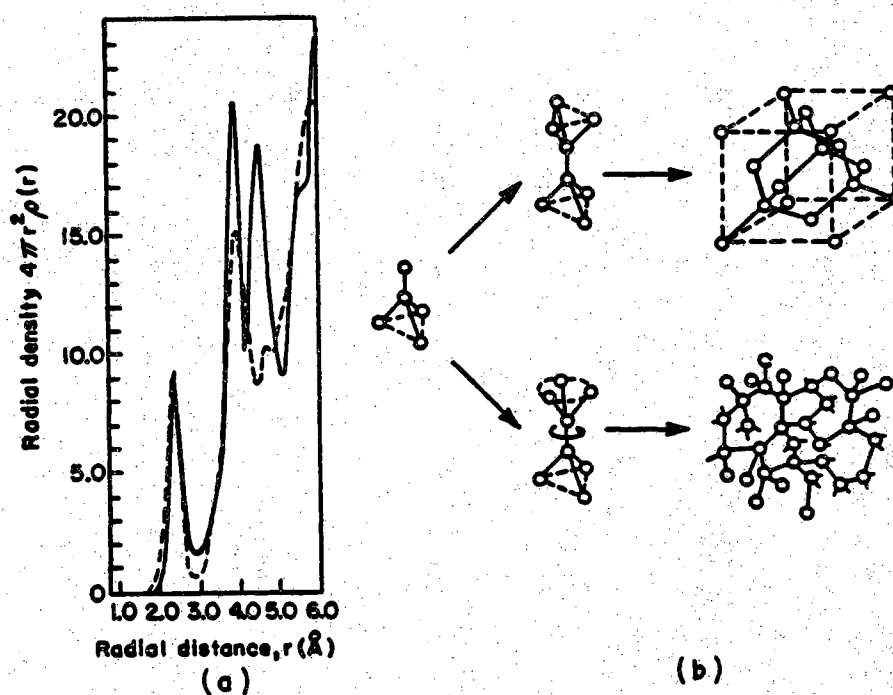
Figure 2.1   (a) Radial distribution curves for an amorphous Si(---) and crystalline Si(—). (b) The manner in which the basic tetrahedral unit can lead to a crystal or to an amorphous, random network material [8]
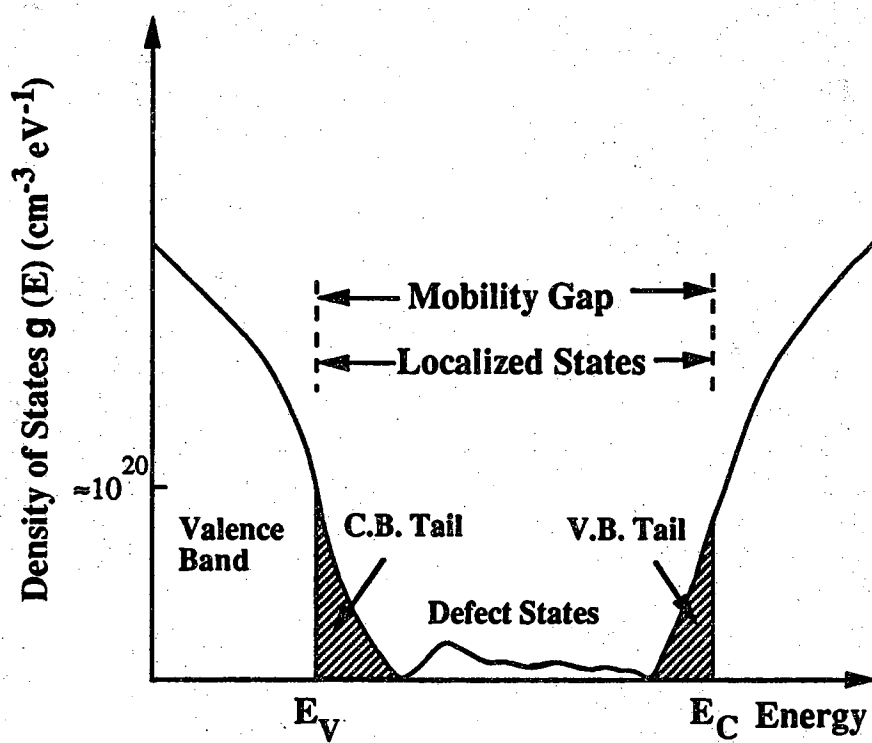
Figure 2.2   Band model of a-Si. E_v and E_c are the mobility edges of the valence band and of the conduction band, respectively. From Ref[10] .

depends on the doping level as determined from several independent experiments[12-14]. Street [15] has proposed a model that can in principle account for the observed relation that the density of dangling bonds is proportional to the square root of the dopant concentration.

2.2.1.3 Electrical Transport Properties

Electrical transport in amorphous semiconductors is much more complex than it is in crystalline semiconductors. This is basically because electric current can be carried by electrons and holes in extended as well as localized states in these materials. Thus for amorphous semiconductors, the current density (J) must be written in general as

$$J = J_E + J_L \qquad (2.1)$$

Here J_E is the extended-states contribution and J_L the localized-states contribution. Figure 2.3 shows a schematic illustration of electron transport mechanisms in amorphous semiconductors, using the format of an energy level diagram in real space[16]. Two mechanisms can be identified, ie, the band transport in extended states and hopping transport between localized states. Their relative importance largely depends on temperature (two-channel model).

At very low temperatures conduction can occur by thermally assisted tunneling between states very near the Fermi level. At higher temperatures carriers are exited into the localized states of the band tails. Carriers in these states contribute to conduction by variable range hopping from one site to another. In all probability these sites are not at the same energy; ie, transitions A and B in Figure 2.3. Consequently, hopping is a phonon-assisted tunneling process. Every time the localized electron moves, it emits or absorbs a phonon and the steps, which necessitate absorption of a phonon, are rate limiting. This makes hopping a thermally activated process. It has been described by Mott[17] and is characterized by the relation

$$\sigma = \left[\frac{e^2}{2(8\pi)^{1/2}} \right] \nu_{ph} \left[\frac{N(E_F)}{\alpha k T} \right]^{1/2} e^{-(A/T^{1/4})} \qquad (2.2)$$

where

$$A = 2.1 \left[\frac{\alpha^3}{k N(E_F)} \right]^{1/4}, \qquad (2.3)$$

ν_{ph} is the phonon frequency in Hz, α is the rate of wave function fall-off at a site, $N(E_F)$ is the density of states at the Fermi level in $\#/cm^3 - eV$ and "e" is

BNAD TRANSPORT
IN EXTENDED STATES

$-E_C$

HOPPING TRANSPORT:
$-E_F$ TUNNELING BETWEEN
LOCALIZED STATES

$-E_V$
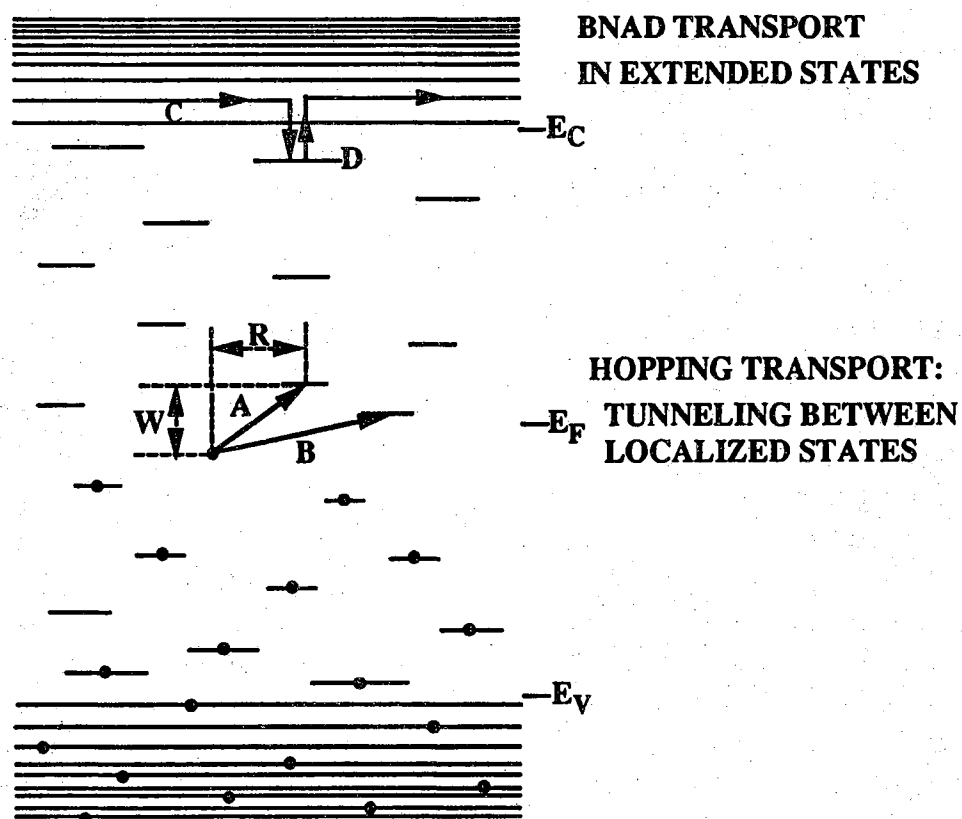
Figure 2.3   Energy level schematic for electronic conduction mechanisms in an a-Si. Energy is represented in the vertical direction, distance in the horizontal direction. From Ref[16] .

the charge of an electron in Coulombs. This relation has been verified experimentally.

At still higher temperatures the electron is excited to the level labeled C in Figure 2.3, an extended state above the conduction-band edge E_c, and contributes to the conductivity in a way similar to that of a conduction electron in crystalline Si; i.e., both are products of a non-temperature-activated mobility, determined by the scattering of electrons from one delocalized site to another, and a temperature-activated number density:

$$\sigma = e\mu_{dL}(T)N(T)e^{-\Delta E/kT} \tag{2.4}$$

where $\Delta E = E_C - E_F$ and N is a band effective density of states. However, because of the enhanced scattering caused by the disorder and the trapping and release events by localized states, the carrier mobility in the extended states of a-Si is much lower than that in crystalline Si.

Since the mobilities of the extended states are expected to be orders of magnitude larger than those of localized states (the mobility gap), and since, among the localized states, mobilities can vary by orders of magnitude due to its temperature-activated nature, the conductivity of a-Si can be tremendously affected by shift in carrier populations. For example, if light appreciably shifts the carrier population into localized states with large hopping mobilities or into extended band states, large changes in the conductivity will result. Hence many amorphous semiconductors are strong photoconductors. In addition, the conductivity can also be affected by high electric fields. The effects basically result from changes in population caused by the interaction of coulombic potential of a localized site and that of external field.

2.2.1.4 The Effect of Hydrogen in Amorphous Silicon

In plasma deposited amorphous silicon hydrogen itself is of course the most numerous impurity. In a way similar to its presence in crystalline silicon, this impurity does not introduce localized states in the band gap. Instead hydrogen serves primarily to passivate the defects already present in the amorphous system and thus to decrease the density of defect states in the mobility gap. This first order effect stems from the passivation or compensation of the dangling bonds. Because the Si-H energy levels lie away from the bandgap, therefore presumably they do not interfere with the near bandgap transport and the optical phenomena.

Direct evidence that hydrogen passivates dangling bonds is seen by the disappearance of the electron spin resonance (ESR) signal in hydrogenated a-Si as compared to pure a-Si. The ESR signal originates from unpared electron spins which are produced by dangling bonds.

The way the hydrogen is incorporated into a-Si:H also affects the observed properties[18, 19]. Several studies[20] have been conducted to identify the bonding configurations based on Infrared absorption and Raman scattering experiments. The material is described as an Si:H alloy where there are multiple, as well as single, H-atom attachment. NMR experiments[21, 22] show that about 4 atomic percent of hydrogen can be incorporated as dilute hydrogen while the rest is found in clusters of 5 to 7 hydrogen atoms[23]. This structural inhomogeneity can be described by means of a two-phase model: a phase, a, of low defect density and with hydrogen bonded mainly in the form of SiH_x (x=1) groups. This phase is imbedded in a second phase, b, of poor quality, i.e., a high defect density. In phase a a fraction of the monohydride is atomically dispersed, the remainder is clustered. Phase b contains large amounts of hydrogen, which is bonded not only in the form of SiH_x (x=1), but also as SiH_x ($x>1$) and as $(SiH_2)_n$ ($n>1$) chains. In good quality material phase a dominates. Infrared spectroscopy is used to identify the presence of SiH_x ($x \geq 1$) groups and $(SiH_2)_n$ ($n>1$) chains and to determine the total hydrogen content. Good quality material contains 2~15% atomic hydrogen only bonded as SiH_x ($x=1$). With increasing hydrogen content the amount of dihydride and polymer-like chains increases, as does the amount of SiH_x ($x=1$) clustering, while the film properties deteriorate.

A well known property of a-Si:H is the creation of metastable states either under the influence of light (Staebler-Wronski effect) or due to carrier accumulation generated by an electric field (like in TFTs). It is believed that Si-Si bonds and Si-H bonds are broken. The breaking of an Si-H bond is followed by diffusion of the free hydrogen atom through the a-Si:H material. This free hydrogen atom is able to break weak Si-Si bonds.

Besides hydrogen, the passivation of dangling bonds can also be achieved with other monovalent atoms, such as chlorine and fluorine, which have a larger electronegativity than hydrogen. In fact, it has been found that glow discharge a-Si:F:H has better doping efficiency and lower density of states in the mobility gap[24].

2.2.2 Deposition of a-Si:H Films

Hydrogenated amorphous silicon films are most commonly deposited by plasma enhanced CVD (PECVD) or glow-discharge deposition in SiH_4[25]. There are many other methods of obtaining a-Si:H films. The electrical and optical quality of the films produced by other techniques is at best comparable with PECVD film. These other methods are the reactive sputtering in an $Ar-H_2$ atmosphere[26], microwave[27], VHF glow discharge[28], chemical vapor deposition followed by plasma hydrogenation[29], E-beam evaporation followed by hydrogen ion implantation[30], and chemical vapor deposition from higher silane[31], homogeneous CVD[32], photo-CVD[33], and hydrogen remote plasma CVD (HRP CVD)[34].

The remote plasma-enhanced CVD is developed under the promise of obtaining a material with a high density, low defect concentration and a good step coverage. Here hydrogen radicals are produced in a separate chamber and led to the reaction chamber where mixing with silane occurs. The hydrogen radical concentration can be controlled independently and the growing film is not in contact with the plasma. In photo-CVD, reactive fragments are produced by mixing mercury with the gas and UV radiation of a mercury lamp is used for initialization of the reactions. Because the PECVD a-Si:H is inherently hydrogen rich and hence of higher quality, a-Si:H as used in TFTs is usually deposited by this method. Since the research conducted in this project is concerned with a-Si:H/ SiN_x, both prepared by this technique, the rest of this section will address only this process.

2.2.2.1. General Principles of PECVD Process

PECVD is a gas-phase reaction in a low-temperature plasma that forms a thin solid film on a substrate. A plasma or glow discharge is a partially ionized gas composed of equal number of positive and negative charges, as well as a host of neutral species in both ground and excited states. Typically, the plasma is formed by applying an electric field across a volume of gas. In an electric field, free electrons are created and gain sufficient kinetic energy (about 1-10 ev) from the field. This corresponds to an average electron temperature on the order of $10^4-10^5 K$. When they make inelastic collisions with neutral molecules and atoms, the internal energy of the gas molecules becomes high and the molecules can then be excited, dissociated, and ionized. This excited state is equivalent to a high-temperature state, and the effective reaction can thus proceed at a low temperature.

The process of film formation by PECVD can be broken down into three major stages[35] as described below.

1. Radical and ion generation

Due to the non-maxwellian distribution of electron energies in the discharge, collisions between electrons and gas molecules can result in ionization and also give rise to the efficient formation of neutral radicals. The number of electrons in the high energy tail of the distribution that are capable of ionizing neutral species in the discharge is considerably less than the number of electrons capable of molecular dissociation. As a result, the degree of ionization is usually much less than the degree of molecular dissociation.

2. Radical adsorption and ion incorporation

Because of their high sticking coefficients, the radicals can be easily adsorbed on the substrate surface, where they are subject to a variety of physicochemical interactions, including electron and ion bombardment, rearrangements, reactions with other adsorbed species, new bond formation, and consequently film formation and growth. Under a certain choice of operating parameters or the introduction of impurities that can act as nucleation sites, nucleating reactions can occur. This results in undesirable particulate formation and causes defects in the growing films.

3. Adatom rearrangement

This involves the surface diffusion of adsorbed atoms into stable sites and the desorption of reaction by-products from the growing surface. Adatom diffusion and desorption rates are strongly influenced by the substrate temperature, with higher temperature favoring films with fewer entrapped by-products, higher density, and more uniform composition. In fact, PECVD process is surface reaction limited and these films are in general not stoichiometric.

The above discussions indicate that a fundamental understanding of gas-phase plasma chemistry and physics, along with surface chemistry modified by radiation effects, is needed in order to define film growth mechanisms. These phenomena ultimately establish film deposition rates and properties. The complex interactions involved in PECVD are outlined in Figure 2.4. If the basic or microscopic plasma parameters (neutral-species, ion, and electron densities; electron energy distribution; and residence time) can be controlled,
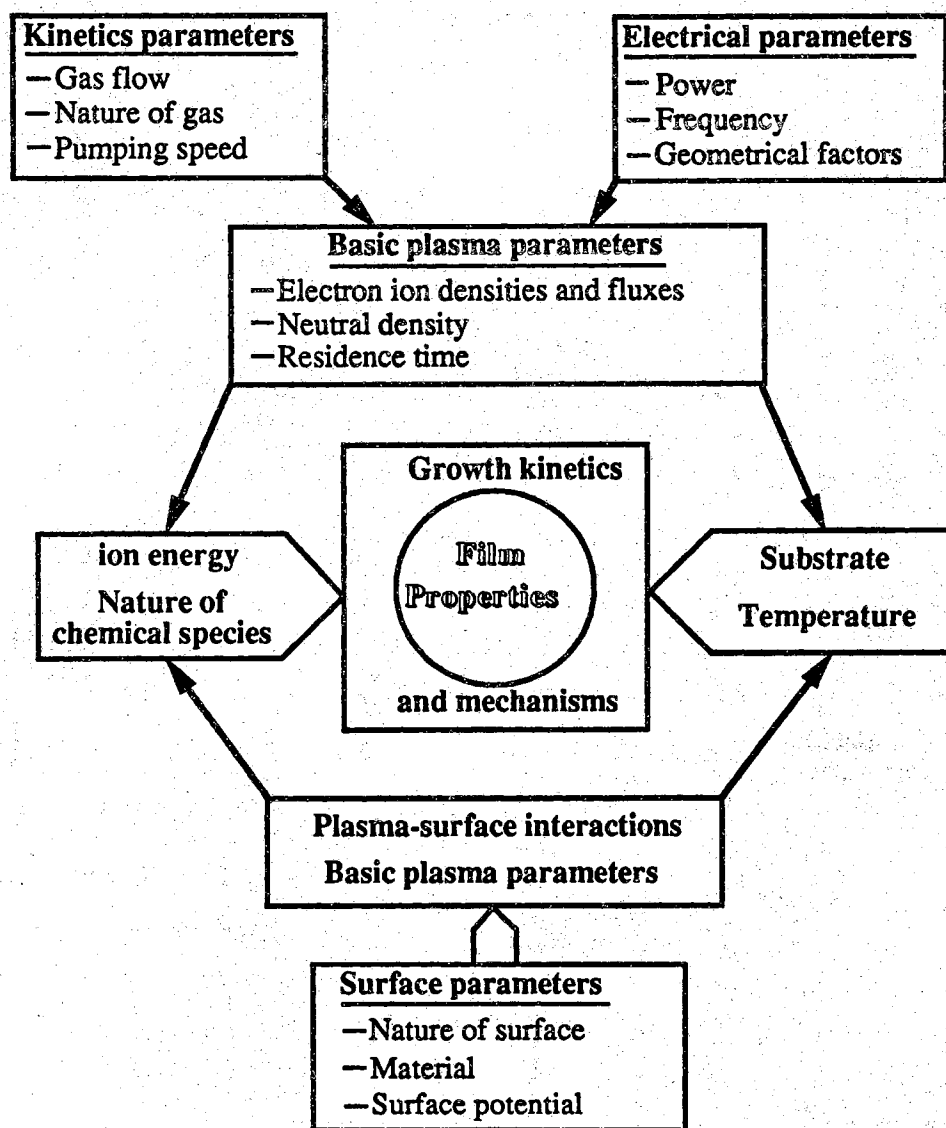
Figure 2.4   Interaction complexity of homogeneous and heterogeneous plasma processes that determine film properties in PECVD.

the gas-phase chemistry can be defined. Many macroscopic plasma variables (gas flow, discharge gas, pumping speed, rf power, frequency, etc.) can be changed to alter the basic plasma conditions. However, the precise manner in which a change in any of these variables affects basic plasma parameters is currently unknown. Therefore, depending on the particular application, deposition conditions must be carefully characterized and optimized for each type of PECVD unit used.

2.2.2.2. Plasma Enhanced CVD of a-Si:H

Although the production of a-Si:H from SiH_4 (or from mixtures of SiH_4 with inert gases or H_2) is chemically one of the simplest reactions imaginable, the fundamental reactions involved in film formation and the structure-property relationships are not yet clearly defined. In general, gas-phase reactive species are primarily H, SiH, SiH_2, SiH_3, and their positive ions[36]. The influence of parameters on the quality of a-Si:H, such as rf power[37], pressure[38], substrate temperature[39-42], substrate bias[43], electrode distance[44] and the use of a triode instead of diode reactor[45] has been well established, just as has the dilution of silane gas with inert carrier gases, such as the noble gases[46].

The rf power level must be just sufficient to maintain the glow discharge. A rise in the rf power level increases the number of defects such as microvoids and promotes a columnar film morphology. High rf power levels lead to strong ion bombardment of the growing film. Therefore, power densities are typically at the lower end of the range from 0.1 to 2.0 W/cm^2. For discharge in pure SiH_4, the pressures are typically 5 to 250 mT; pressures as high as a few torr may be used if the SiH_4 is diluted in H_2 or an inert gas to prevent gas-phase particulate formation. A too low pressure increases the influence of ion bombardment. Pressures which are too high lead to gas phase polymerization resulting in the formation of dust particles which give rise to pinholes in the film. In addition, the substrate temperature has an important influence on the microstructure and compositions of the as-deposited films. High quality films are obtained with substrate temperatures in the range 200—300 °C. An increase in substrate temperature in general results in an increased growth of microcrystalline films thus increasing the electron mobility and reducing the density of localized states. The material is stable up to about 300 °C, above which Si-H bonds begin to break and hydrogen concentration decreases as a result of its effusion[42]. Also, undoped a-Si:H crystallizes near 620 °C[47] to form polysilicon. Thus high temperatures must be avoided on all a-Si:H

processing if the film is to remain amorphous and hydrogen rich. However, a low substrate temperature, just as a high pressure and rf power level, leads to the formation of films with a high total hydrogen concentration. Not only SiH groups, but also SiH_2 groups and $(SiH_2)_n$ ($n>1$) chains are present, which gives rise to a material with poor electronic properties.

A low background concentration of contaminants in the films, which originates from system leakage and desorption from the chamber, is obtained by a large gas flowrate. Choosing the flow rate too high results in transportation of active species outside the reactor before diffusion can take place to the substrate surface, which results in a decrease of the growth rate. Also, the extent of the departure of the system from the quasi chemical equilibrium strongly influences the deposition kinetics and the attainment of a quasi-equilibrium depends on whether or not the residence time of species is smaller than the characteristic time of the reaction or the overall reaction time constant. Normally a flow rate is chosen in the range 10—100 sccm. Diluting the silane gas with inert gases such as He, Ne, Kr, and Ar deteriorates film properties. The influence of the carrier gas is dependent on the molecular mass of gas molecules. The deterioration is stronger for dilution with gases having a higher molecular mass.

2.2.3 Substitutional Doping of a-Si:H

Until n- and p-type doping had been demonstrated in glow discharge a-Si:H[4], it was generally believed that amorphous semiconductors could not be doped by the introduction of impurities. This was based on the arguments that all bonds of a trivalent or pentavalent dopant atom introduced into the random network would be satisfied by bond rearrangements. The success of the doping was attributed to the very low overall density of gap states in glow discharge a-Si:H where the introduction of impurities could displace the Fermi level several tenths of an electron volt.

Gas phase doping in a-Si:H, both n- and p-type, is achieved by introducing phosphine (PH_3) or diborane (B_2H_6) into the reactor. In Figure 2.5, the room temperature dark conductivity σ_{RT} is plotted as a function of the doping impurity concentration. It shows that σ_{RT} can be controlled over some ten orders of magnitude, from 10^{-12} $(\Omega cm)^{-1}$ to 10^{-2} $(\Omega cm)^{-1}$, with both n- and p-type doping, as the Fermi level is moved over approximately 1.2 eV.
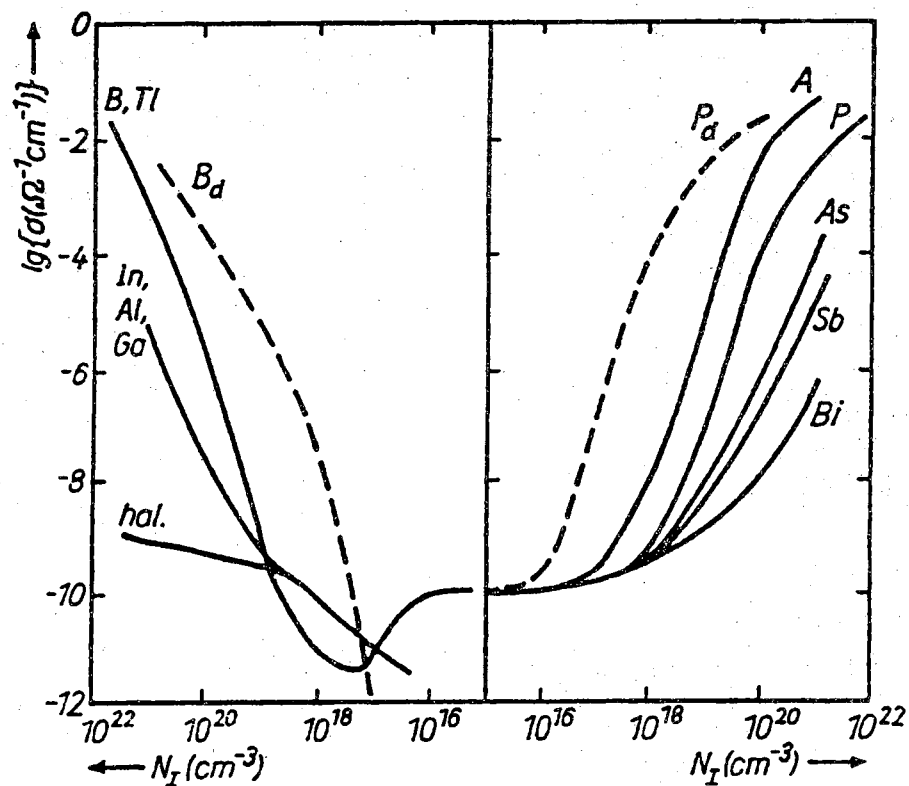
Figure 2.5   Dependence of the electrical conductivity of a-Si:H on the concentration of gas-phase doping and implanted impurities, Including dopant from groups I(A), III, V, and VII (halogens) of the Periodic Table. Dashed lines are for gas-phase doping and solid lines are for ion implantation[48].

In crystalline device technology, ion implantation has become important doping technique. With the success of doping a-Si:H from a gaseous source, it appeared of fundamental and applied interest to explore the feasibility of this technique in the doping of amorphous semiconductors. Muller et al[49] demonstrated that n- and p-type a-Si:H doping could indeed be accomplished with ion implantation. Later work has also shown that it is possible to dope this material by implantation of the other substitutional impurities As, Sb, Bi, Al, Ga, In, Ti and the interstitial impurities Na, K, Rb and Cs[50]. Figure 2.5 also shows the conductivity dependence upon the implanted impurity concentration for impurities of groups I, III, V, and VII of Periodic Table. The impurities were in this case implanted into a-Si:H films at substrate temperature near 280 $^\circ C$ which is near the film deposition temperature. It is clear that ion implantation results in the introduction of donors or acceptors and the same range of control of the conductivity can be achieved. However, the doping efficiency is 50 to 100 times lower than that of gas phase doping. It was also found that the maximum efficiency was observed for implantation at temperatures near to that of a-Si:H deposition. By using hot-substrate implantation, intensive reconstructions such as the electrical activation of impurity atoms and dangling passivation take place as the implant progressed. Therefore, the overall damage to the a-Si:H is lower in the cases of a hot substrate than for room temperature implants followed by annealing at the same temperature. Ion implantation will be particularly useful for fabrication high-speed a-S:H TFT CMOS-like circuits, where both n- and p-type doping are required on the same substrate.

2.2.4 Contacts to a-Si:H

As with any device research, a low resistance metal/a-Si:H contact is indispensable for an unperturbed external access to the intrinsic device. Ideally, the contact resistance of such metal contacts should be negligible relative to bulk (space-charge-limited) or spreading resistance of a-Si:H layer. But this is rarely achieved in practice and, from a practical point view, a satisfactory ohmic contact is one that does not perturb device performance to any significant extent. Until recently, the importance of the contact resistance is rarely addressed in a-Si:H devices such as solar cells and thin film transistors. This is because its contribution is generally assumed to be negligible compared to the intrinsic resistance throughout its region of operation. However, as the down scaling of TFT devices continues in both channel length and a-Si:H thickness, contact resistance is becoming a limiting factor in device

performance.

Since the metal/a-Si:H barrier height is relatively insensitive to the metal work function and the presence of surface states make it virtually impossible to engineer an accumulation ohmic contact, a good low resistance ohmic contact to an undoped a-Si:H film cannot be achieved by simply evaporating a low work function metal onto the a-Si:H surface[51] or vice versa[52]. By strict definition, all metals form reasonable Schottky barriers on a-Si:H[53]. In practice, however, the ohmicity of an metal/a-Si:H contact depends on such factors as the metal reactivity, the interface quality, a-Si:H conductivity and to a lesser degree on metal work function[54,55]. Although the variation of the potential barrier height (ϕ_b) with the metal work function (ϕ_m) is not simple and linear, an empirical relationship between the contact behavior and barrier height (for as-deposited metal on undoped as-deposited a-Si:H) is as follows[54,55]: (a) an ohmic contact can be achieved if $0 < \phi_b/E_g < 0.3$, and (b) a quasi-ohmic contact can be achieved if $0.3 < \phi_b/E_g < 0.5$. For example, metals such as Eu, Y, Sc, or Mg form exceptionally good ohmic contacts, while others like Al, Cu, Mo, or V form very poor quasi-ohmic contacts to undoped films. Metals such as Ho, Hf, Er, or Ti create fair quasi-ohmic contacts to undoped films at room temperature. The above observation should be taken with caution because the reactivity of the metal and the final interface condition are even more important than work function. With all these complications, the most efficient method in achieving a good ohmic contact, like in crystalline case, is to use a tunneling contact by heavily doping the a-Si:H film in the vicinity of the metal/a-Si:H interface.

Several investigations have been performed to study the effects of annealing and doping on the metal/a-Si:H contact performance[56-59]. In general, metal silicides formed after annealing improve the quality of the interface and decrease its specific contact resistance. For device applications, the effect of contact performance on device operation has also been shown in several a-Si:H TFT investigations[60,61]. Devices with the doped source/drain contact regions yielded significantly higher ON-current than those without the doped contact regions. High quality source/drain contacts have also been achieved using ion implantation doping[62,63]. Remarkably, a post metalization anneal was found to improve the ON-current by at least three orders of magnitude[62]. This was attributed to the intermixing of Al/Si followed by microcrystallization and hence the increased doping efficiency. However, there was no hard evidence for this explanation. In addition, surface conditions were not specified immediately before Al metalization, e.g., if there

was significant layer of oxide either due to ion implantation or air exposure. The systematic study by Bare et al[63] demonstrated that the effective combination of heated implants for better doping efficiency and a BHF dip before metalization for oxide removal led to improved contacts.

2.3 The Gate Insulator

As in crystalline MOSFET, The quality of the gate insulator is very vital to the performance of a-Si:H TFT's. As always, an ideal gate insulator should possess the following characteristics and properties: (a) possess a large dielectric constant and a high breakdown field; (b) contain a trap density as low as possible to allow the production of stable devices; (c) have a controllable and reproducible composition and structure; (d) its interface with a-Si:H should display a minimum of surface states, and a low quantity of fixed charge. Since the formation of the insulator layer must also be compatible with the low temperature process, a special challenge exists in making even one of these requirements completely satisfied. In fact, a significant amount of effort in a-Si:H TFTs research has been in seeking a better gate insulator. Over the past several years, different insulators have been studied as the gate insulator in a-Si:H TFTs. Besides PECVD SiN_x, many others include PECVD SiO_2[64], low temperature thermal oxide[65], photo CVD TaO_x/SiN_x[66], SiO_xN_y[67], PECVD SiO_xN_y/SiN_x[68], and fluorinated silicon nitride[69].

For high temperature SiO_2, it is a excellent gate insulator due to its larger bandgap and lower density of both bulk and interface traps. However, PECVD SiO_2 has been found generally to have poor electrical characteristics. This material tended to be porous, showing substantial leakage currents as well as low electric field breakdown. Recently, a new PECVD SiO_2 was developed by a carefully control of plasma parameters such as N_2O to SiH_4 ratio, gas flow rate, pressure and rf power[70,71]. It is claimed that the oxide quality is approaching that of thermally grown films. This oxide has also been used as a gate dielectric in a-Si:H TFTs[64]. Although its leakage current was low, no appreciable improvements in TFT characteristics were obtained over TFTs with $a-SiNx:H$ gate insulator. Moreover, stability tests have not been performed.

In the low-temperature thermal oxidation method, strong oxidizing agents in the liquid phase ($HNO_3:H_2SO_4$=2:1)[72] or HNO_3 vapor[65] were used to oxidize the a-Si:H. This method resulted in an excellent interface because the oxide was grown inside the a-Si:H layer. Among others, one limitation is that

the growth rate is too low ($\sim$25 $\mathring{A}/h$) so that a deposited second insulator is often needed.

Work has also been done by engineering the SiN_x composition near the a-Si:H interface. Inserting a thin Si-rich nitride between a-Si:H and a N-rich nitride[73], was reported. In this case the field-effect mobility, subthreshold slope, and stability have all been improved. However, it is still not clear whether Si-rich or N-rich nitride makes a better interface with a-Si:H, especially in regarding TFT stability.

The development of these and other gate dielectrics for a-Si:H TFT is obviously still at its primitive stage and extensive research is needed for any of them to take the place of PECVD $a-SiN_x{:}H$. The popularity of $a-SiN_x{:}H$ may be attributed to its ease of deposition, large technology base, and extensive research over many years. Because of the immense number of publications in this field and the restricted space of this thesis only a few characteristic references are given below.

Silicon nitride thin films were first deposited with a PECVD system by Sterling and Swann in 1965[74]. The reactant gases tried were SiH_4/N_2[75], SiH_4/NH_3[76], and $SiH_4/NH_3/N_2$[77, 78]. Generally, if SiH_4-N_2 reactant gas is used, the N_2/SiH_4 ratio needs to be kept high (100-1000) to avoid the formation of silicon-rich films[79, 80]. This can lead to low deposition rates, but also gives low hydrogen content. On the other hand, because NH_3 can dissociate at much lower energy than N_2, NH_3/SiH_4 ratios can be considerably lower[35]. They usually result in higher hydrogen content in the film, but offers better thickness and refractive index uniformity[81]. As a compromise, $SiH_4-N_2-NH_3$ reactant gas seems to be more popular in industrial production.

As stated previously, the PECVD system for silicon nitride formation has many operating variables. Because the charge trapping centers in SiN_x is generally attributed to Si dangling bonds[82-84], it is desired that PECVD silicon nitride be stoichiometric or slightly N-rich and its properties be close to those of high temperature CVD silicon nitride. Much research effort has been devoted to achieve this goal. In general, an increase in rf power density increases the N/Si ratio in the film[79, 85, 86]. Because the bonding energy of the Si-H bond is less than those of the N-H and N-N bonds, an increase in rf power should increase the concentration of reactive nitrogen species relative to the number of reactive silicon species and thereby decrease the Si/H ratio in the film. At high power densities and at high temperatures, the N/Si ratio

approaches the stoichiometric value 1.33.

PECVD SiN_x, made from various combinations of $SiH_4/NH_3/N_2$ and inert gas carriers, contains up to 30 atomic % hydrogen. With the understanding of Si—H bond's involvement in the Staebler-Wronski effect, researchers began looking into the effect of hydrogen in $a-SiN_x{:}H$. Surprisingly, it showed that there was no correlation between the densities of the dangling bonds and Si—H bonds[87,88]. Further, it has been found that an increase in the density of Si—H bonds increases the etch rate in buffered HF[89] and causes a deterioration in the characteristics of a MOSFET with a nitride passivation layer. In addition, the Si—H bonds might be associated with charge-trapping sites, as shown experimentally[90,91] and theoretically[92]. However, Robertson and Powell have shown theoretically that Si—H bonds form the states outside the band gap[82]. Thus the role of Si—H bonds as charge-trapping centers is still not clear. One possibility may be the Si—H bond breaking event resulting in a Si dangling bond. A recent charge injection study also demonstrated the correlation between the $SiN_x{:}H$ charging rate and the Si—H density[93]. Nevertheless, there has been an intense effort to minimize the hydrogen content, or somehow avoid the harmful effects of Si—H. Inspired by the superior properties of a-Si:F film, researchers begin to deposit fluorinated silicon nitride (SiN:F) films. Initial results show much better electrical characteristics than with $SiN_x{:}H$ films[69,94].

2.4 a-Si:H TFT Technologies

2.4.1 Basic TFT Configurations

Conventionally, various configurations of thin film transistors have been classified into four basic structures as shown in Figure 2.6, depending on the order of deposition of the gate electrode, the semiconductor layer, the gate insulator layer, and the source-drain contacts. The resulting structure is either coplanar (source/drain and gate electrodes on the same side of the semiconductor film) or staggered (source/drain and gate electrodes on the opposite side of the semiconductor film). By inverted structure, it says that the gate electrode is the first layer deposited on the substrate.

At present, inverted-staggered structure is most widely used in practical applications. There are several technological reasons which favor this structure. First, the gate insulator, a-Si:H and a third heavily doped a-Si:H microcrystalline Si layer can be deposited sequentially in the same deposition system in one pump-down of the system. This not only decreases

Staggered

Inverted-Staggered

Coplanar

Inverted-Coplanar

Electrode   Semiconductor   Insulator
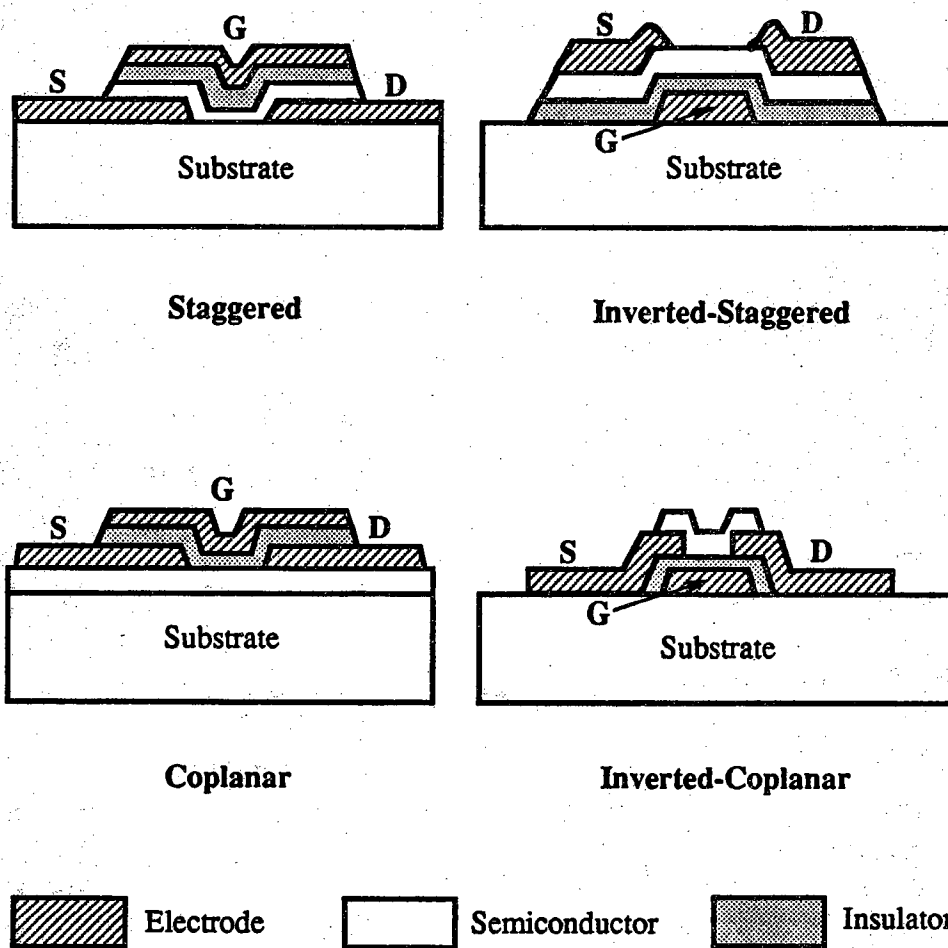
Figure 2.6   Basic thin film transistor configurations

contamination but also reduces turn-around time. Second, SiN_x deposition temperature is not limited by a already existing a-Si:H layer. Finally, the interface between SiN_x and a-Si:H is of better quality in terms of both interface states density[95] and a-Si:H TFT performance[96]. It was found that the different interfaces are the result of specific chemical effects during growth and a compositional asymmetry of the two interfaces. The Bottom nitride/a-Si:H interface is not abrupt and there is a significant N-tail carried over into a-Si:H over a distance greater than about 50 $\mathring{A}$ [97]. For illustration, a basic SiN_x gate technology is briefly described. The starting substrate can be glass, ceramic, quartz or anything that remains adequately smooth and flat in the processing temperature range ($<350\,^\circ C$) of the a-Si:H TFT. A gate metal electrode, typically 500-1000 $\mathring{A}$ thick, is first deposited and then patterned. The gate dielectric, usually SiN_x or silicon dioxide, then the a-Si:H and the n^+ a-Si:H layers are deposited by the PECVD method. An Al layer, about 1 μ thick, is then deposited over the source and drain regions after etching back the n^+ layer over the channel region. This completes the fabrication process.

2.4.2 Novel a-Si:H TFT Technologies

One of the major limitation of conventional a-Si:H TFT devices is the low ON-current, which limits the dynamic performance to 10-20 MHz range. While an increase in mobility may prove to be difficult to achieve, an increased frequency response can be obtained by device engineering and geometric considerations.

Dual-gate TFTs, as shown in Figure 2.7a, have been developed in order to increase the ON-current[98]. By applying a gate bias to both the gates, two conducting channels are formed. The drain current in the dual-gate mode is always larger than the sum of the two drain currents obtained from single-gate operation. This attributed to the overlap of the two accumulation regions and potential redistribution along the channel. Recently, a new buried double-gate TFT structure was reported to obtain high ON-current and high reliability[99]. As shown in Figure 2.7b, This novel structure can be fabricated simply by adding a gate electrode, G2, and an upper gate insulator, SiN2, to the conventional inverted-staggered TFT. In comparison with conventional a-Si:H TFTs, the ON-current of this device is three times as high and the threshold voltage shift is about one third for the same gate electric field.

Another new device reported by Hack et al [100] is a double injection transistor which has a large ON-current. It has a n^+ cathode and a p^+ anode so that the gate electrode modulates a conducting channel formed by both
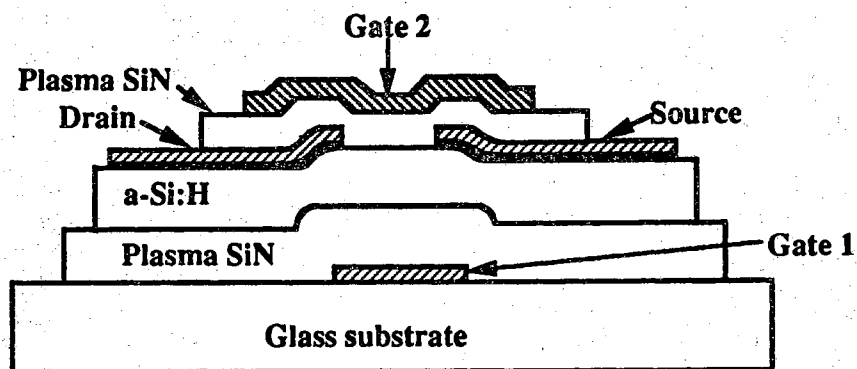
(a)
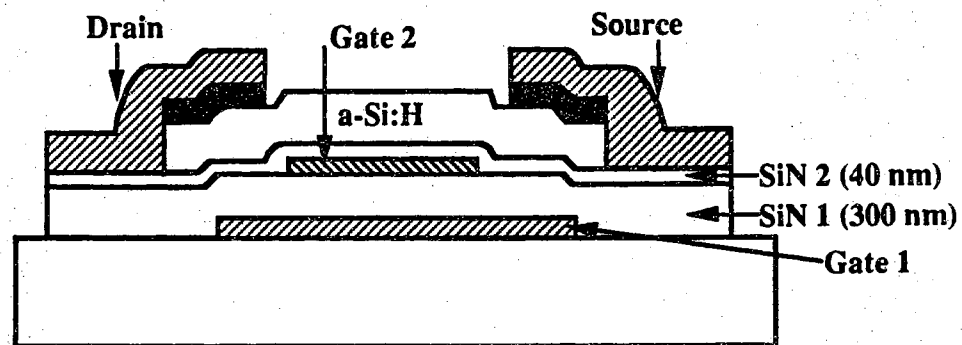
(b)

Figure 2.7   (a) Schematic of a dual-gate a-Si:H TFT[98]. (b) Cross sectional view of the buried double-gate TFT showing an additional buried gate, G2, and a very thin gate-insulator, SiN2[99].

electrons and holes. Since both types of carriers are present, the channel is capable of sustaining a much larger amount of charge without violating the charge neutrality condition, leading to higher ON-current. The off-current is quite high, and thus such a device would be used as a current driver where a large dynamic range required for charge storage is not necessary.

Perhaps the simplest way to increase the operation frequency is to reduce the channel length, provided that parasitic effects are not important. However, it is very difficult to reliably make devices with a channel length shorter than 5 μm by using conventional photolithographic process over a large substrate area. To overcome this engineering aspect, Uchida et al[101] developed a vertical type TFT where the active transistor is formed along the side walls of a metal-insulator-metal structure, Figure 2.8a. The active a-Si:H-SiN-metal layers, deposited in a second high vacuum pumpdown, is etched down anisotropically by reactive ion etching until flush with the the drain metalization. This step reduces the overlap capacitances drastically and results in a very small total input capacitance of 0.55 pF/mm. The experimental cut-off frequency for this device is 3 MHz.

For the conventional lateral TFT, self-alignment methods have been explored to decrease parasitic capacitance[102, 103]. A cross sectional view is shown in Figure 2.8b. This process ensures proper gate alignment with source and drain contact metallization by performing the photolithography for source/drain definition by backlighting from under the glass substrate. The opaque gate area defines the inner edge of the source/drain metal so that they are perfectly aligned to the gate. The n^+ layer is finally etched back to the intrinsic layer by RIE.

2.5 Characteristics of a-Si:H Thin Film Transistors

2.5.1 Introduction

The basic principles for an a-Si TFT are similar to that of enhancement mode insulated gate field effect transistor (IGFET). When a potential is applied at the gate, an accumulation layer of carriers is induced close to the insulator/semiconductor interface. This provides a high conductive channel between the source and drain electrodes. However, there are features distinct from the single-crystal devices. This stems from the relatively large density of localized states in the band gap of amorphous semiconductors. In addition, there is always the ohmic conduction between the source and drain which mainly affects the off current.
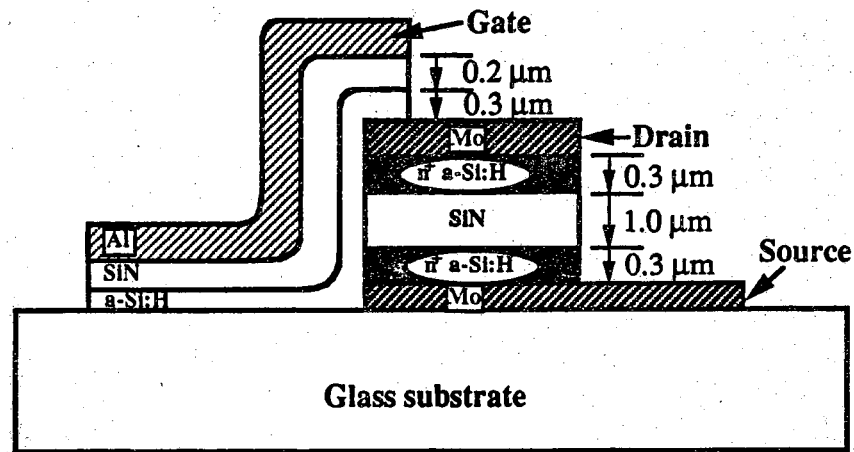
(a)
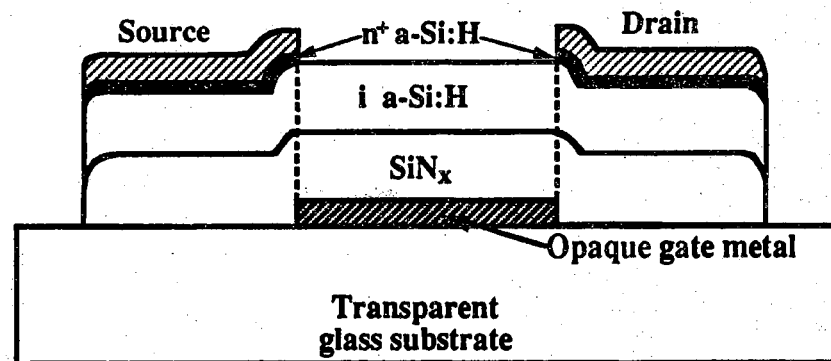
(b)

Figure 2.8   (a) Schematic cross section of the vertical type TFT structure[101]. (b) Cross sectional view of an inverted-staggered self-aligned TFT.

The characteristics required of a-Si:H TFT depend on the application for which it is to be used. In general, the parameters used to characterize a-Si:H TFTs are I_{on}/I_{off} ratio, field effect mobility μ_{fe}, threshold voltage V_T, and stability.

2.5.2 Physics and Operation

Like a crystalline MOSFET, an a-Si:H TFT has two basic modes of operation, namely, the subthreshold and the above threshold regimes. However, there are distinct differences between these two kind of insulated-gate field effect transistors.

The basic operation of the transistor can be understood by reference to Figure 9, where the band-bending and the occupancy of the electronic states are illustrated with a simple density of states diagram. To start with, the energy bands are close to the flat-band condition at zero gate voltage if no interface states or fixed charge in the insulator are assumed. For an a-Si:H TFT operated in the subthreshold regime, nearly all the induced charge goes into the deep localized states in the energy gap of a-Si:H as well as any interface states present. With an increase in gate voltage, more states are filled by a larger number of accumulated charge carriers, so that the Fermi level moves closer to the edge of the conduction band for a n-channel TFT and that of the valence band for a p-channel TFT. This leads to a superlinearly increase in the concentration of mobile carriers in the extended states[105]. However, due to the unsymmetrical distribution of donorlike and acceptorlike states in the energy band gap, it takes a much larger charge of carriers (holes) to fill the donor-like localized states by applying negative bias to the gate than it takes to fill the acceptor-like states by applying positive bias. Together with the inherently larger band mobility for electrons, this means that the on-current is much larger for n-channel a-Si:H TFTs than for p-channel TFTs.

As the gate voltage continually increasing, the Fermi level enters the bandgap tail states. This is the above threshold regime. In this regime, most of the induced charge goes into the tail states with only a small fraction going into the extend states. Hence the field effect mobility is much less than the band mobility. A truly crystalline-like regime can occur only when virtually all localized states are filled and the Fermi level at the a-Si:H/insulator interface is within about kT/q of the band edge. Then most of the induced charge goes into the extended states and the field-effect mobility is close to the band mobility[106]. This condition would require an electric field as high as 5×10^6 V/cm in the insulator with a relative permittivity of about 3.9.

$V_G = 0$ $V_G < V_T$ $V_G > V_T$

E_c E_f E_v
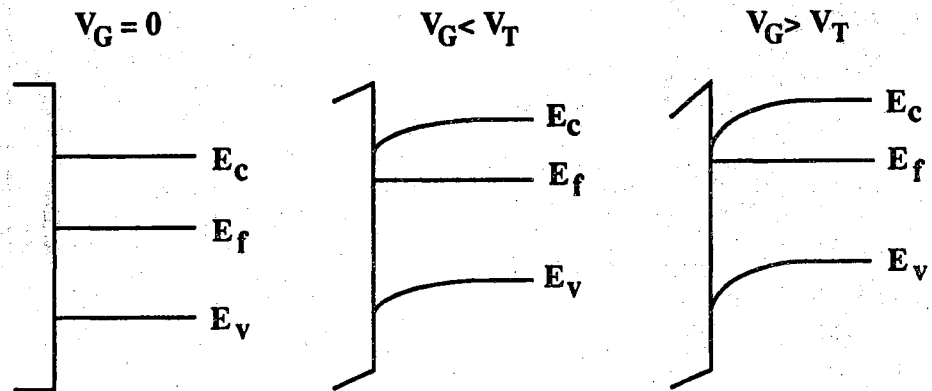
Band bending profiles

E_c E_f

$n_{DEEP} > n_{BT}$ $n_{DEEP} < n_{BT}$
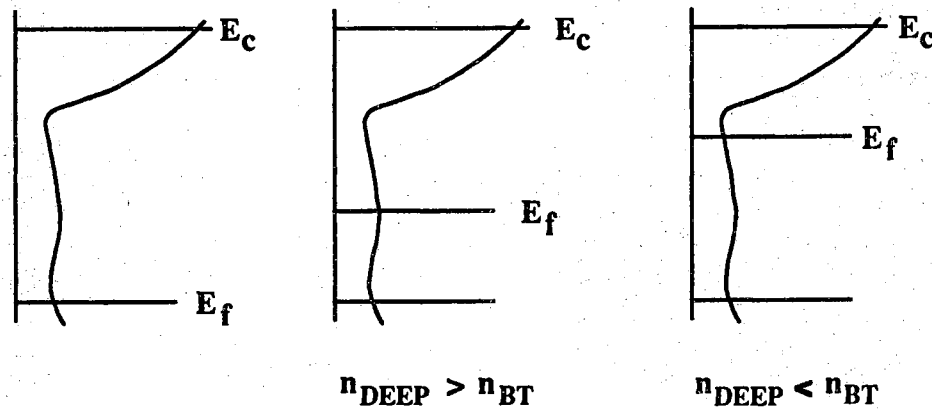
Occupancy of states

Figure 2.9   Schematic illustration of the basic operation of an a-Si:H TFT, showing the energy band-bending (top) and the occupancy of the localized states; n_{deep} is the number of electrons in deep states and n_{BT} is the number of electrons in tail states[104].

Due to technological difficulties, practical a-Si:H TFTs are usually n-channel accumulation devices. The static characteristics has been modeled by a number of groups[107-110]. Chung and Neudeck[109] derived accurate analytical expressions for the static characteristics which take into account the bulk defect states and interface defect states. It shows good agreement with experimental results. The characteristics shows three distinct regions of operation. For $V_G - V_{FB} < V_T$ and $V_G - V_{FB} - V_D \geq 0$, the device is essentially in the subthreshold regime and the drain current is given by

$$I_D = \frac{WP}{la_2} e^{a_2(V_G - V_{FB} - \Delta V_{FB})} [1 - e^{-a_2 V_D}]. \tag{2.5}$$

In the transition region when $V_G - V_{FB} \geq V_T$ and $V_G - V_{FB} - V_D > V_T$, it gives

$$I_D = \frac{WA}{l\eta} \beta^{\eta-1} [V_{GT}{}^\eta - (V_{GT} - V_D)^\eta]. \tag{2.6}$$

When $V_G - V_{FB} \geq V_T$ and $V_G - V_{FB} - V_D < V_T$,

$$I_D = \frac{WA}{l\eta} \beta^{\eta-1} V_{GT}{}^\eta \tag{2.7}$$

Where

$$V_{GT} = V_G - V_{FB} - V_T.$$

In the above equations, W and l are the width and length, respectively. V_G is the gate voltage, V_{FB} the flat band voltage. V_T, A, η, β, a_2 are model parameters. Because the field-effect mobility is a function of the gate voltage, plots of the square root of saturation current $I_D^{1/2}$ vs V_G are generally no longer straight lines. In practice, therefore, the threshold voltage is obtained by a two parameter least-square fit to the data in saturation using the following equation

$$I_D = K(V_G - V_T)^\gamma, \tag{2.8}$$

where K and γ are functions of different material parameters.

Besides the unipolar operation of a-Si:H TFTs mentioned above, a TFT with source and drain contacts which are ohmic for majority and minority carriers could also be switched between n-channel and p-channel modes. This is termed the ambipolar characteristic. In addition to the ohmic injecting contacts, the use of a high-quality gate insulator and a low level of interface state density are required in a-Si:H TFTs in order to observe the ambipolar behavior at reasonable gate voltages. This is because the fixed charge in the gate insulator would shift the flat band voltage and hence hinder the formation

of a p-channel (for negative shifts) or a n-channel (for positive shifts). For this reason, thermally grown SiO_2[111] was usually used for the gate insulator. Very recently, the ambipolar behavior was also observed for a-Si:H TFTs employing a PECVD SiN_x and Boron-implanted source/drain contacts[112].

Evidence of the ambipolar behavior of a-Si:H TFTs was observed by Neudeck and Malhotra in 1975[113] and formal investigation of this property was published by Pfleiderer et al[114-116]. More recently, numerical models were also developed which can predict the output drain characteristics over many decades of drain current for a single set of input parameters[117, 118]. The operation of an ambipolar a-Si:H TFT is best illustrated by Figure 2.10. As indicated in the figure, four regions of operation can be identified. The characteristics in the first two regions are not much different from that of a unipolar device. However, as the device enters region 3, the effects of the enhanced hole layer near drain end begin to show up and the current increases at a faster rate. In region 4, the current initially increases exponentially. This is because the n-channel conduction essentially does not change while the p-channel conduction increases as the drain voltage (V_D) increases.

2.6 a-Si:H TFT Applications

As mentioned previously, a-S:H TFTs have been widely adopted as switching elements in commercially available liquid-crystal flat panel displays, as image sensors and as logic circuits. However, the major drive for the development of a-Si:H TFT technology is in the area of active-matrix liquid crystal displays (AMLCD). The TFT-addressed LCD has a much more complicated structure than the direct-drive multiplexed TN LCD because of the addition of TFT array. In realizing a AMLCD, many factors must be taken into account. In addition to considerations for discrete transistors such as their structure, operation and characteristics, problems such as addressing scheme, uniformity and defects over large areas must also be solved. In this section, various issues of a-Si:H TFTs as used in AMLCD will be reviewed and discussed.

2.6.1 Fundamental Physical Arrangement and Operation of the AMLCD

A cross-sectional view of one TFT switched pixel is shown in Figure 2.11. On the lower glass plate, the TFT array is fabricated as well as the transparent driving electrodes for the individual pixels, usually a layer of indium tin oxide (ITO). On the upper glass plate, a common electrode, also made of ITO, is fabricated. For the glass substrates, quartz, hard glass, or soda-lime glass can
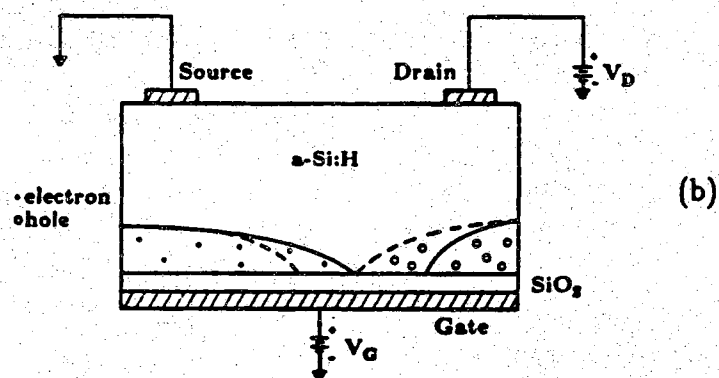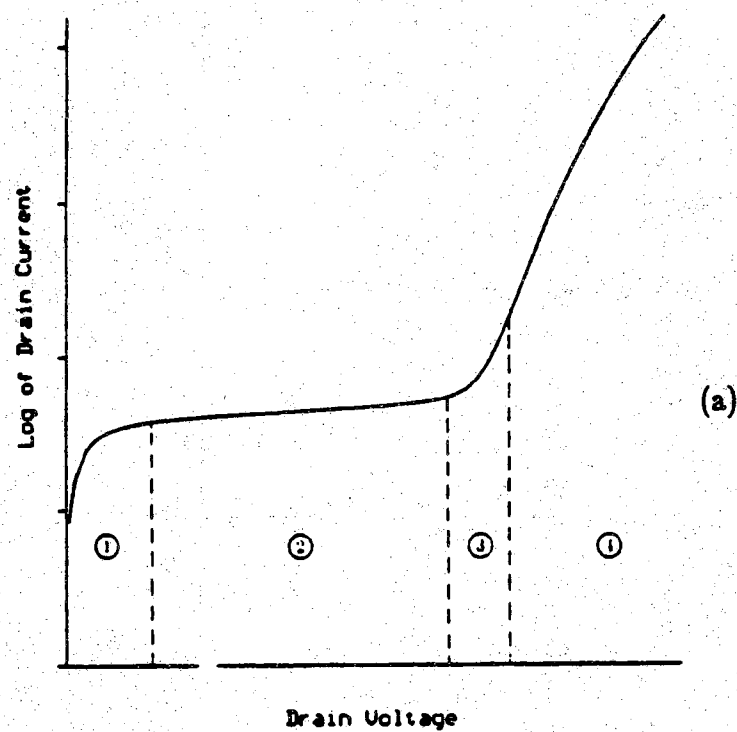
Figure 2.10 (a) Ambipolar regions of operation; (b) Shrinking electron and expanding hole layers in an ambipolar a-Si:H TFT beyond pinch-off (dashed-lines show changing boundaries of electron and hole layers as V_D is changed). From Ref. 52.

Glass Substrate
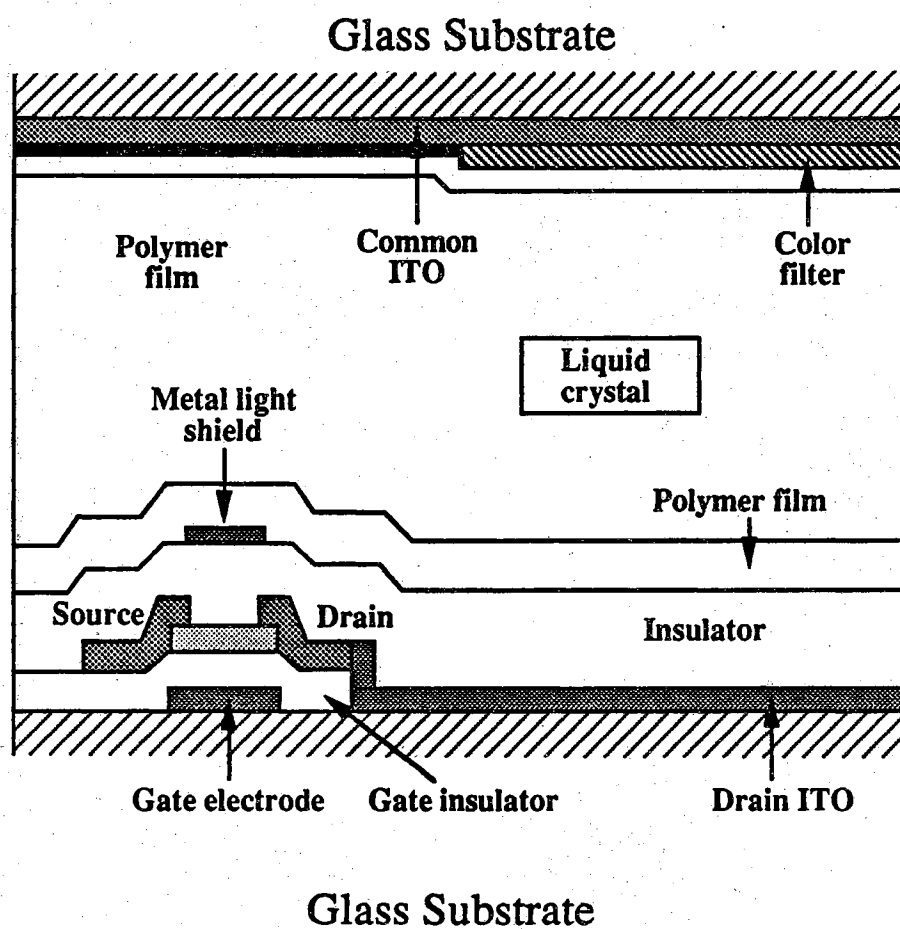
Figure 2.11   A cross sectional view of one pixel in a LCD showing the TFT.
From Ref. [53].

be used, provided they can withstand the TFT processing environment including temperature and etching solutions. The liquid-crystal material, in most cases a TN type, is contained between the glass substrates as a layer 5-7 μm thick. In operation, the liquid-crystal elements are driven by AC voltages applied between the pixel electrodes and the common electrode. It should be noted that for proper operation, the electrode surfaces must be suitably treated to appropriately align the liquid-crystal molecules, and polarizers must be provided on the external surfaces of both glass plates.

The circuit arrangement of the complete TFT LCD is shown in Figure 2.12. As indicated, there are (M×N) pixels addressed by N data lines and M gate lines. This is electrically equivalent to a MOSFET dynamic memory circuit. The drive circuits for these lines may be located outside the display and connected to these lines, or they may be integrated along the edges of the display substrate, fabricated from TFTs based on the same semiconducting material.

The use of TFT active matrix is to separate the function of the nonlinearity from the LC material itself and use the transistor to provide the needed nonlinearity. Ideally, the TFT active matrix can be considered as an array of pixel switches. In operation, the gate lines are sequentially activated during a frame time, turning on successive rows of TFTs. During the time a row of TFTs is turned on, the signal voltages corresponding to that row are transferred from the drive circuits to the pixel electrodes through these TFTs. After this row of TFTs is turned off, the capacitive charges stored on the pixel electrodes may be retained until this row is addressed again provided the OFF resistance of TFTs is large enough. To avoid electrolytic effects within the LC material, a zero average dc voltage needs to be maintained on the pixel by reversing the polarity of the signal voltage each field. An example of the driving waveforms and resulting pixel voltage waveforms appearing on an ON pixel are shown in Figure 2.13. V_G is the amplitude of the gate signal and $\pm V_s$ represents the signal voltage. V_{p11} is the resultant pixel electrode voltage.

2.6.2 Electrical Requirements

A TFT used in an active matrix can never be an ideal switch and it has finite ON resistance as well as OFF resistance. As such, the minimum requirements placed on its electrical characteristics depend on the display application. For simplicity, a bilevel display, which has only two states —ON and OFF, will be considered in the following discussions.
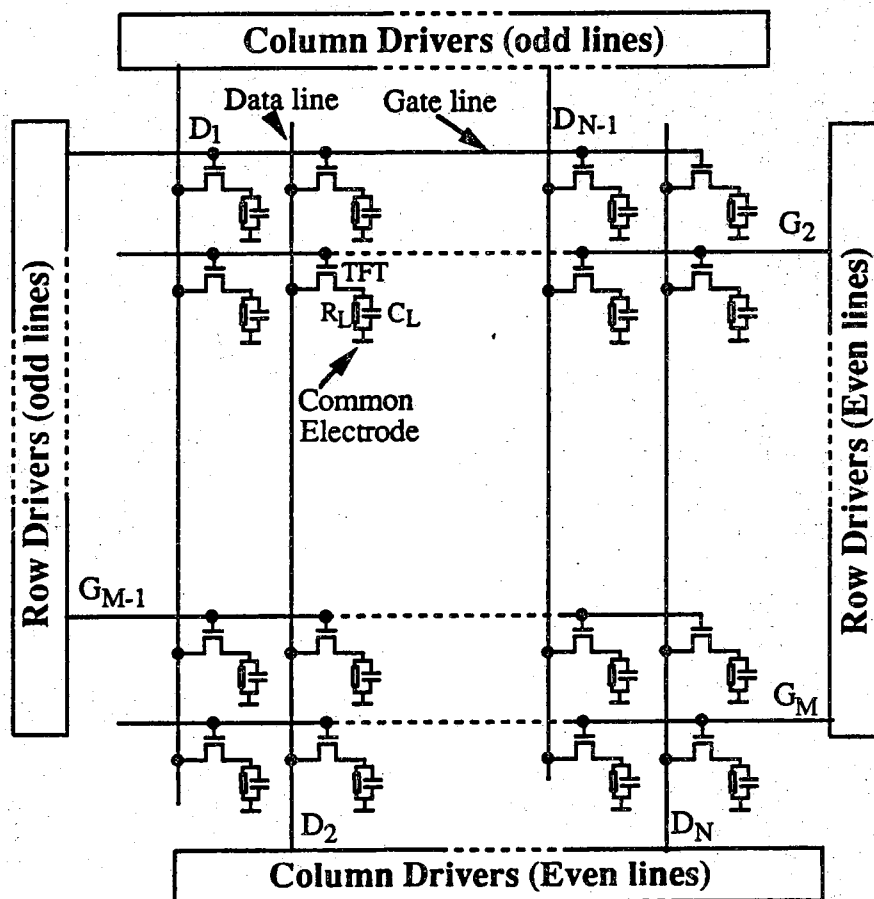
Figure 2.12   Circuit arrangement of TFT LCD: usually, the column and row drivers are positioned along the four edges; gate lines correspond to scan lines, and display data is transferred through the data lines to each pixel.
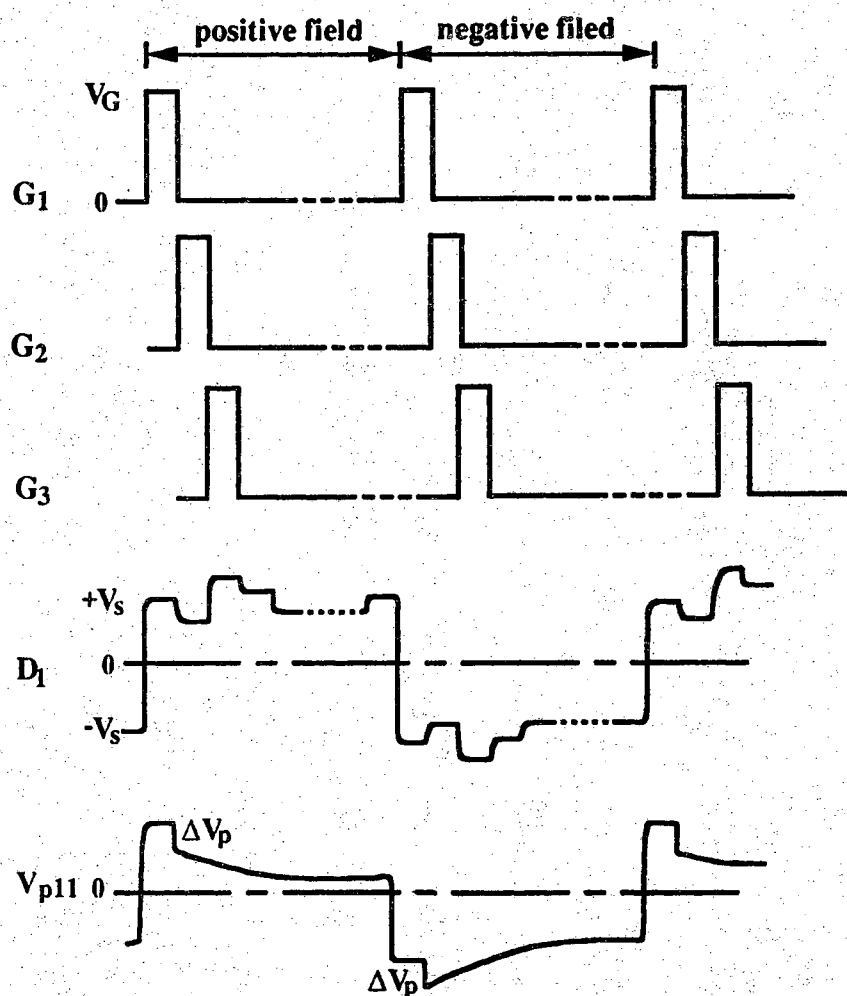
Figure 2.13   Driving waveforms for TFT LCD: one frame consists of a positive and negative field. The input signal on an activated data line has a voltage swing $\pm V_s$; similar signal voltages are applied to the other activated data lines in accordance with the picture content; V_p is the pixel voltage.

The requirement of the ON state is based upon the need to charge the pixel capacitor to $+V_{on}$ from $-V_{on}$ during the row select time $(\frac{T}{M})$. If the dependence of the TFT ON characteristics on the pixel voltage and the non-uniform charging current during the entire charging cycle are considered, then the drive current requirement for the TFT is [119]

$$I_{on}=2F_{on}C_{LC}M/T \qquad (2.9)$$

Where F_{on} is an engineering factor, typically of magnitude 1~10, to account the non-ideal factors and C_{LC} is the LC capacitance. This is in effect to require that the RC time be less than $1/F_{on}$ of the charging period (row select time).

The basic requirement for the active matrix TFT switch is that the leakage current through the TFT should not result in an ON pixel losing sufficient charge to appear partially or fully OFF. This is a soft requirement in the sense that the data pulse could be increased to compensate for the decay. If a voltage decay ΔV_{on} during a field time T is the maximum for insignificant change of the ON pixel brightness, the TFT leakage current at room temperature must be

$$I_{off} \le F_{off} \Delta V_{on} C_{LC}/T, \qquad (2.10)$$

where F_{off} is also an engineering factor to account for the leakage current increase at higher temperatures or under strong ambient light. For example, the leakage current of the TFT doubles with every 10-degree rise in temperature, assuming the activation energy of the semiconductor film to be 0.6 eV. If the TFT LCD is required to operate up to 60 °C, then F_{off} factor should be at most 0.1.

To have a general feel of the electrical requirements, typical values for the above variables will be assumed. For the LC material, we assume a capacitance C_{LC} of 0.6 pF (dielectric constant $\epsilon_r \simeq 10$, $d=10^{-11}cm$, $A=6\times10^{-4}\ cm^2$) and a threshold V_{on} of 1.5 V. Generally, the human eye can easily detect flicker below 25 Hz, so the minimum frame frequency must be more than 30 Hz or the field time T should be at most 1.6×10^{-2} sec. Further, if we use $F_{on}=5$, $F_{off}=0.1$ and $\Delta V_{on}=0.1\ V$ for 90% charge retention, then

$$I_{on}>6M\times10^{-10}\ A, \qquad (2.11)$$

and

$$I_{off}<6\times10^{-13}\ A. \qquad (2.12)$$

For M=1000, then the ON current and ON/OFF current ratio should be

larger than 6×10^{-7} A and 10^6, respectively. It should be mentioned that the above analysis applies only to bilevel display where a low degree of uniformity is acceptable. For a gray-scale display, it requires a much better degree of uniformity in TFT characteristics as well as more stringent conditions for I_{on}, I_{off} and the current ratio. Indeed, the tolerance on the voltage accuracy determines the number of gray-scale steps.

2.6.3 a-Si:H TFT Technologies in AMLCD

By far a-Si:H TFT is the most widely used switching elements in AMLCD mainly because satisfactory switching characteristics and the ability of fabrication over large areas. In addition, the requirement for a glass substrate is much relaxed due to its low temperature process—typically less than 300 $^\circ C$. Inexpensive low temperature glasses such as Corning 7059 or even soft soda-lime glass can be used. This is one advantage over poly-Si TFTs which require a substrate of hard glass with a softening point above 650 $^\circ C$ such as Coring 1733, Hoya NA 40 and Asahi AN.

For a discrete device of the commonly used inverted-staggered structure, the processing issues has been discussed in a previous section. In AMLCD, a light-shield layer external to the TFT may be required on the source/drain side to reduce light-induced leakage current. If, however, amorphous Si film is very thin (eg, 300—500 $\overset{\circ}{A}$), the need for the light-shield layer may be avoided. Another limitation is the device size. Here the device dimensions can not be radically designed as large as required to satisfy the ON-current requirements. A trivial upper bound is imposed by the available size of the pixel. If the device gets too large it will reduce the transmission of the pixel to unacceptably low levels. A more important upper bound is caused by parasitic capacitances intrinsic to the particular device such as the gate-source and source-drain capacitances. These typically scale with the geometry; this is, as the dimension W increases, the parasitic capacitances increase and a larger voltage shift appears in the pixel voltage.

One advantage of the TFT-addressed LCD compared to direct-drive LCDs is that it offers the possibility of fabricating the driver circuits on the same substrate as the display. This would avoid troublesome connections between the LCD and driver LSIs, reduce system cost and improve display reliability. For example, A 1000×1000 pixel color display requires 4000 external connections to drive circuits. By fabricating the drive circuitry simultaneously with the active matrix, the total number of external leads can be reduced to 50. The design and operation of the row drivers are less of a problem than the

column drivers since all the circuits are fully digital and their operating speed is relatively low. For interlaced TV operation, the row drivers must operate at 16 KHz[120]. Assuming a gate length of 10 μm, the required switching speed can be achieved with a field effect mobility of less than 0.5 $cm^2/V-s$. Therefore both a-Si and poly-Si are "in principle" suitable. A low-speed gate-line-integrated driver has been developed using a-Si:H TFT technology[121]. On the other hand, the column drivers must operate at frequencies of 8 MHz for black and white or 23 MHz for color[120]. A minimum mobility of 8 $cm^2/V-s$ is required and therefore a-Si TFT is not suitable for proper operation unless very short channel devices are employed.

Another problem area in a-Si:H TFTs is their uniformity and stability. The former depends mainly on the manufacturing equipment and the processing technology, but the instability is associated with an undesirable physical property of the amorphous state semiconductor and gate insulator. Advances in both process technologies and device modeling are needed to improve the materials quality and to design a better driving scheme.

2.7 Problems and Future Developments

2.7.1 Introduction

At present, the best a-Si:H TFT has the inverted-staggered structure with SiN_x as the gate insulator. It gives an on/off current ratio of 10^7, μ_{fe} of $0.8cm^2/V-s$ and a threshold voltage of about 2 V. Its performance is adequate for active matrix switching for a LCD. But for the peripheral driver circuits and other high speed applications, significant improvement of its current drive capability and reliability need to be achieved. In view of the large amount of research effort devoted to its process optimization, it seems that further improvement of its performance by optimizing the PECVD deposition conditions will not be dramatic as long as we stick to the inverted-staggered configuration and the present materials. Clearly, thin film microelectronics involving a-Si:H TFTs is presently in a very early stage of development. There is much room for substantial improvements. The two major issues, i.e., increase of speed and elimination of threshold voltage shift, must be solved before further applications in analog and digital circuits in large electronics can be fully exploited.

2.7.2 Speed Consideration

The standard amorphous silicon TFT is an n-channel enhancement type device. In the off state the very low conductivity of intrinsic amorphous silicon, which has a band gap of about 1.72 ev, inhibits current flow from source to drain. The off currents are on the order of pico-amps. The conductivity can be increased by 8 to 9 orders of magnitude by application of a positive gate voltage. On currents are generally on the order of micro-amps. It is limited by the inherently low electron drift mobility in bulk a-Si:H and by the even lower field effect mobility due to a higher density of defects and wider tail states distribution near the semiconductor-insulator interface. Improvement of this interface implies optimization of the gate insulator deposition conditions as well as the a-Si:H; especially in the early stages of deposition.

In general, there are three approaches to increase the current drive capability and thus improve the operation speed of the a-Si:H TFT. First, the carrier mobilities are increased by improving the a-Si:H and the insulator quality as well as improving the a-Si/insulator interface quality. As stated earlier, this is expected not to be significant. Second, carrier transit time across the channel is reduced by reducing the channel length and therefore the maximum operating frequency f_m is increased since $f_m = \mu_{FE} V'/2\pi L^2$, where $V' = V_D$ is the source-drain voltage in the linear region and $V' = V_G - V_T$ is the voltage in the saturation region. Third, a new circuit is invented for a-Si:H TFTs.

The second approach is generally believed to be the most effective way for improving the operation speed of a-Si:H TFTs. This is based on the assumption that TFT performance is governed by the surface field model which successfully analyzes long channel behavior and that it scales to short channels. However, due to the use of conventional photolithographic techniques (masks alignment and photo etching) for large area electronics, new TFT structures and fabrication technologies have to be used. At present, there already appear several approaches, (a) Vertical TFTs. This represent the simplest approach to higher speeds. (b) Self-aligned TFT structures. It is possible to obtain a short channel device without overlapping source and drain capacitance.

Both methods can produce submicron devices. However, it is necessary to recognize, first of all, that the source-drain transit time is not the only factor limiting speed and performance. The effective field effect mobility, μ_{fe}, deduced from the TFT characteristics in saturation, is also limited by geometrical or

extrinsic effects including contact resistance and/or bulk series resistance. The latter is expected to be important in inverted-staggered TFT's where electrons must traverse through a intrinsic a-Si:H region on their way to and from the channel. Both effects are most significant at large gate voltages, when the channel conductance is largest, and for short channel devices. Due to this parasitic resistance between source/drain and the device channel, it has been determined that there is little improvement for the I_{on}/I_{off} ratio and even a decrease in field-effect mobility below a gate length of about 2 micron[103]. It is obvious that shrinking devices, particularly reducing channel lengths, leads to undesirable short channel effects which must be understood before small geometry a-Si:H TFTs can be realized.

2.7.3 Stability Consideration

One of the advantages for using a-Si:H TFTs is the possibility of using low-temperature processes and inexpensive glass substrates. However, with low-temperature materials there is always an issue of stability. In the case of SiN_x gated a-Si:H TFTs, the most prominent feature is the decrease of the source-drain current with time or threshold voltage shift for a static gate bias. Stability issues of a-Si:H TFTs has been studied intensively by a number of research groups, and its improvement is essential for reliable long-term performance. Figure 2.14 shows the result of Powell[122] illustrating the temperature dependence of the drift. The primary instability mechanisms have been identified as the charge trapping in the silicon nitride gate insulator or near the interface and the creation of metastable states in the a-Si:H channel under gate bias[123, 124].

The first mechanism has a logarithmic time dependence and has a very small temperature dependence[123]. It is believed that the rate limiting process governing the threshold voltage shift is the charge injection from the a-Si:H to the silicon nitride with charge trapping near to the semiconductor interface and with no redistribution of the trapped charge in the nitride. It is therefore expected to be strongly dependent of the quality of the gate insulator, in articular the trap density at or near the a-Si:H/ SiN_x interface.

The second mechanism is characteristic of a-Si:H TFTs. If a voltage is applied to the gate, electrons are drawn from the bulk of the a-Si:H layer and localized deep bandgap states will instantly become filled. Also conduction-band tail states arising from weak $Si-Si$ bonds have a probability of capturing an electron. These bonds are likely to break when occupied by an electron, as suggested by Street and Thompson[125]. The instability of the a-
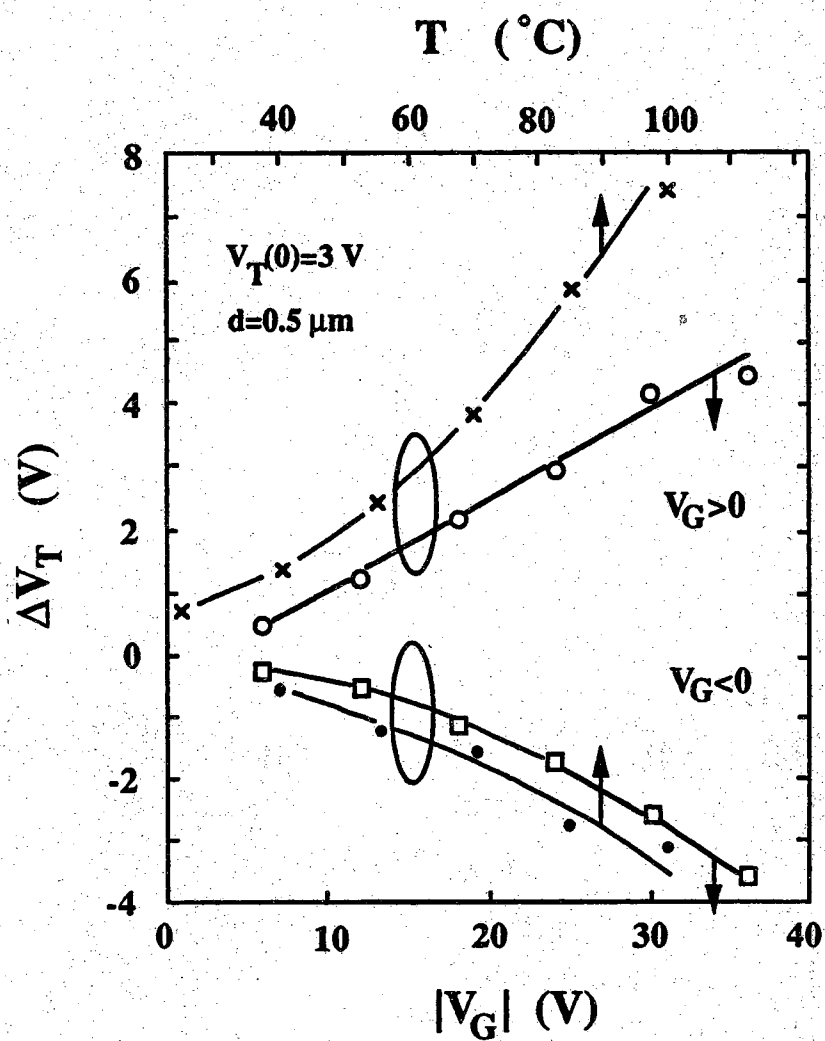
Figure 2.14 The dependence of threshold voltage shift upon voltage and temperature, for a fixed time of 6×10^6 sec, for two polarities of gate voltage. From Ref[122].

Si:H network therefore depends on the degree of band bending as induced by the gate voltage. The additional trapped charge implies a reduction of band bending and therefore less conduction electrons are available to the channel, as is illustrated in Figure 15. The bond-breaking event can be described by the reaction[126]

$$2T_4^0 + e^- \rightarrow T_4^- + T_4^0 \rightarrow T_3^- + T_3^0,$$
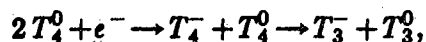
where T_4 is the notation for a fourfold coordinated Si atom and T_3 is a dangling-bond defect. The superscripts denote the charge condition. This shift in the TFT threshold voltage can be reversed by annealing at 150 $^\circ C$ for about 2h, as is the case with the Staebler-Wronski effect.

Like the case of MOS transistors, the reliability of a-Si:H TFTs is also evaluated by means of the bias-temperature (BT) test, in which maximum-rating DC voltages are applied at elevated temperatures[127]. In the operation of the TFT LCD, the TFT is always driven by a pulse signal. If the pulse-temperature (PT) test is used instead of the BT test, the measured lifetime becomes much better. However, it is not clear which method is most accurate. The required lifetime of an LCD depends on the application. Typically it is more than 1,000 hours, but in some cases, it may be more than 10,000 hours. The prevailing strategy seems to be to use a variable gate bias to compensate for the drift induced by the gate pulses.

Created defects

E_F

Si_3^-

a-Si:H   SiNx   Gate
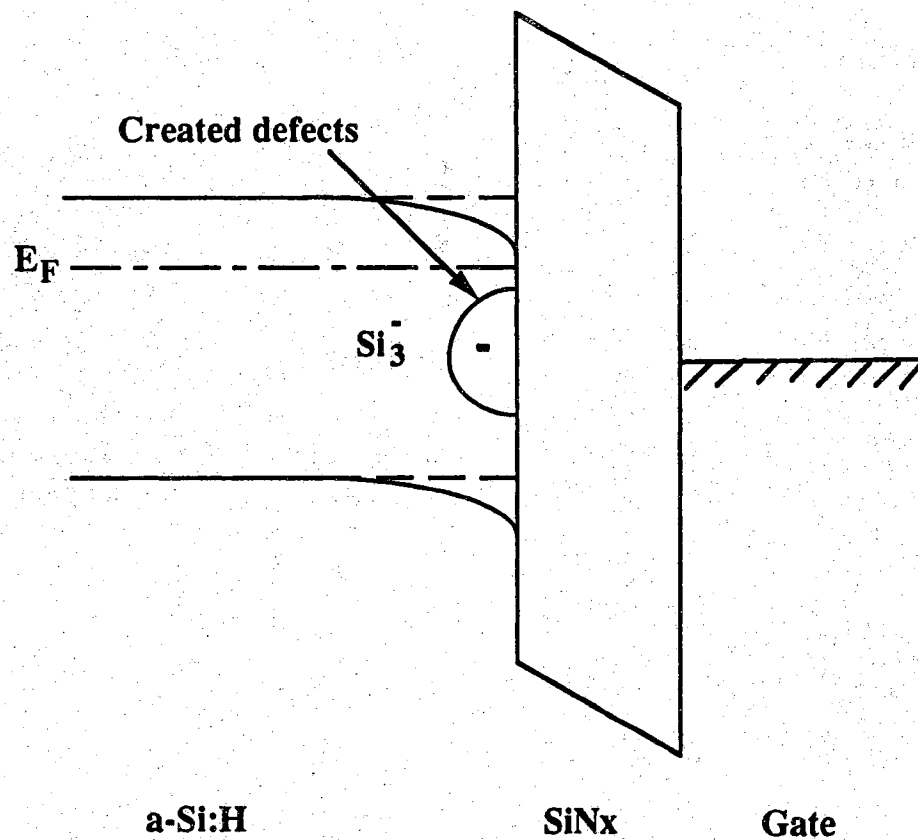
Figure 2.15   A schematic illustration of the metastable states creation process
in a a-Si:H TFT.

CHAPTER 3
a-Si:H THIN FILM TRANSISTOR PROCESS DEVELOPMENT

3.1 Introduction

As stated in Chapter 2, an inverted-staggered a-Si:H TFT employing PECVD $a-SiN_x:H$ as the gate insulator is the most widely used configuration both in practical applications and in basic research. In order to investigate the parasitic effects on a-Si:H TFT performance, it was first necessary to be able to fabricate the basic TFT structures. Previous work on a-Si:H TFTs at Purdue University either employed thermal SiO_2 as the gate insulator or used PECVD SiN_x which was grown elsewhere. Therefore, plasma deposition of SiN_x at Purdue and its characterization was the first step in this project. From these initial optimization results, a-Si:H TFTs were fabricated and tested. Devices with this newly developed gate insulator show a significant improvement in performance and they are comparable to those with silicon nitride deposited from other laboratories. Finally, further studies were performed on the effects of processing parameters such as rf power and NH_3 plasma treatment for nitride deposition. This chapter details these process development efforts.

3.2 Development of High Quality PECVD $a-SiN_x:H$

3.2.1 Test Structure

As stated previously, no charge traps, or as little as possible, and a small leakage current are required for a good gate insulator. To accurately define the properties of $a-SiN_x:H$, a suitable test structure should be designed first. Ideally, it should give us information about the trap density in $a-SiN_x:H$, besides leakage current, and it should be easy to fabricate when compared with TFTs. This appears to be a very difficult task because there is no standard method which satisfies the two requirements. To the author's knowledge, only one method, using a MNOS structure, was experimentally used for obtaining

the bulk trap density of SiN_x[128]. The disadvantages are the growth of a very thin oxide and the need for a complex measurement setup for avalanche injection and charge centroid determination. This is no better than fabricating TFTs directly.

One of the simplest possible structures is the metal-insulator-metal (MIM) sandwich. There exist other theories which can in principle give the insulator trap parameters in this structure. These techniques rely either on the space charge-limited conduction (SCLC) mechanism[129] or on the isothermal current-time characteristics[130, 131]. The SCLC method has been widely used for obtaining the gap states of a-Si and the trap density of some insulators. Two requirements, however, need to be fulfilled in order to observe the SCLC of significant magnitude. First, at least one of the two electrodes must make an ohmic contact. This requires that there is an inexhaustible supply of free carriers in the dielectric near the injecting electrode. Second, the insulator must be relatively free from trapping defects. If the trap density N_t is too large, the field across the sample may cause break down before the trap filled limit is reached. The last requirement may turn out to be the most stringent in the present study because low temperature $a-SiN_x:H$ is notorious for its large trap density. On the contrary, one of the basic assumptions used in the isothermal I-t theory is the presence of two blocking contacts. As such, the donor-type density N_t is included in the formulation by considering the transient charge storage in the Schottky barrier depletion region. The question is whether it is applicable to the present case because it has not been to date verified experimentally.

In view of all the uncertainties stated above, it was a very difficult task to find a simple as well as reliable test structure. The MNM sandwich structure was chosen because it can at least give the leakage current of $a-SiN_x:H$ thin films. Because there is no clear cut basis on which it can be decided whether a contact is "ohmic" or blocking before the contact is established, the applicability of two trap-extraction methods is unknown.

The MNM test capacitors are of square shape with lateral dimensions of 100, 200, 300, 500, and 1000 μm. Figure 3.1 displays a cross-sectional view of this MNM test structure. This structure is very simple and involves only three masking levels. In fabricating the MNM-C's, two-inch, thermally oxidized Si wafers were used as the substrate. After patterning the sputter-deposited bottom metal (Cr or Al-Si), $a-SiN_x:H$ was then deposited in a PECVD system using various gas compositions. Mesa etch of the $a-SiN_x:H$ was performed in the same plasma system using CF_4 gas. The structure was completed by
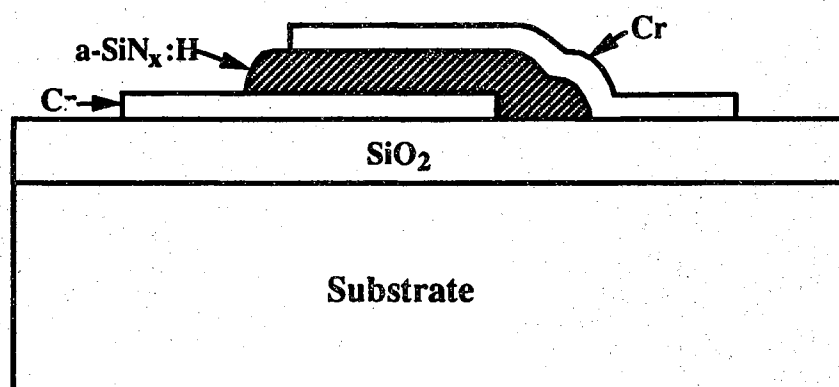
Figure 3.1   Cross-sectional view of the MNM test structure.

sputter-depositing and patterning of the top metal (Cr or Al-Si).

3.2.2 Plasma Deposition of $a-SiN_x:H$

The reactor used for $a-SiN_x:H$ deposition was the TECHNICS Planar Etch II-A system with a PD II-B deposition module. This capacitively-coupled plasma-enhanced CVD system contains a vacuum chamber with radial gas input and an axial exhaust, a 30 KHz 500 W solid state power supply, and has 11 inch diameter electrodes separated by 1 inch. The lower electrode contains a substrate heater controllable up to 350 °C and serves as the deposition platen. The vacuum chamber is evacuated with a 400 l/min two-stage, direct-drive Alcatel model 2012A mechanical pump. To reduce wear on mechanical pump parts subjected to Si particulates during deposition, the pump is equipped with a Motor Guard model 111300 oil purification system. The deposition process gases are metered into the vacuum chamber under the control of MKS model 2295B-00100 mass flow controller via a small gas ring located underneath the deposition platen. An MKS type 253A-1-40-2 exhaust valve controller (EVC) maintains the desired chamber pressure during deposition. The gases exhausted from the chamber are passed through an exhaust gas heater at 800 °C for thermal decomposition to insure the removal of all toxic and flammable gas products prior to exhausting them into the surrounding environment.

The PECVD system for silicon nitride film growth has many operating variables. The large variable space has made the control and reproducibility of film properties and composition difficult, if not impossible. However, it was found[132] that rf power input and NH_3/SiH_4 gas ratio had the largest effects on film properties such as refractive index and N/Si ratio. Pressure was somewhat less important, while substrate temperature had little or no effect. All variables except temperature had significant effects on film growth rate and hydrogen content. Therefore, only the feed gas composition was varied during this initial optimization process. All other parameters were fixed at some particular set of values which were known to give good silicon nitride according to the literature. These parameters were

RF power=50 W
Temperature=300 °C
Pressure=330 mT - 600 mT.

Depositions are performed by loading substrates into the vacuum chamber and evacuating the chamber to less than 70 mT. Nitrogen gas is then fed into the chamber at 50 sccm, while the deposition platen is heated to the desired deposition temperature. At this temperature, the N_2 is switched off and the

appropriate deposition gases are metered into the chamber at preset flow rates. The EVC is set at the desired deposition pressure and the plasma ignited by turning on the rf generator to a preset value. The deposition proceeds until the desired thickness of the deposited material is obtained. At the completion of the deposition, the RF generator, substrate heater and deposition gas switches are turned off and the EVC opened. After the channel readings on MFC becomes zero, N_2 is then allowed to flow through the chamber until its temperature is reduced to below 120 $^\circ C$.

3.2.3 Electrical Characterization of the MIM Capacitors

3.2.3.1 DC Conduction Measurements

The DC conduction measurements were carried out using a stepped bias source on the HP 4140B pico-ammeter/DC voltage source, which was controlled by the HP 9845B desktop computer via the HP-IB interface bus. Most of the samples were found to have a low leakage current typically below $10^{-8} A/cm^{-2}$ at a field 1 MV/cm. Capacitors with different contact metals such as $Cr/SiN_x/Al-Si$ as well as $Cr/SiN_x/Cr$ showed the same I-V characteristics at either polarity. Therefore, $Cr/SiN_x/Cr$ structures will be implied in the following discussion unless otherwise stated.

Figure 3.2 shows the room temperature current density vs the square root of the electric field measured on three MIM structures. They are representative samples from all the compositions fabricated. It is obvious that the film conductivity is a strong function of $N_2/NH_3/SiH_4$ flow ratio (i.e., composition) and the electric filed. The gas flow ratios are 0/30/18, 0/50/5 and 50/50/5 in sccm for curves (a), (b) and (c) in Figure 3.2, respectively. At fields below about 1 MV/cm, all samples showed ohmic characteristics. Leakage current are similar for films deposited without N_2 addition. Films deposited with N_2 addition have a leakage current at least one order of magnitude lower. At higher fields, there appears a much larger difference in leakage current. Current density varies exponentially with the square root of the field for films without N_2 addition (ie, curve (a) and (b)), while curve (c) is still near ohmic. Therefore, films with a higher NH_3/SiH_4 ratio and N_2 addition have a higher quality as far as leakage current is concerned.

The linear relationship in the high electric field region for curves (a) and (b) suggests that the electronic conduction mechanism in the PECVD $a-SiN_x:H$ is either bulk limited Poole-Frenkel emission or electrode limited Schottky emission. For Schottky emission, the theoretical $Jvs\mathscr{E}$ relationship is
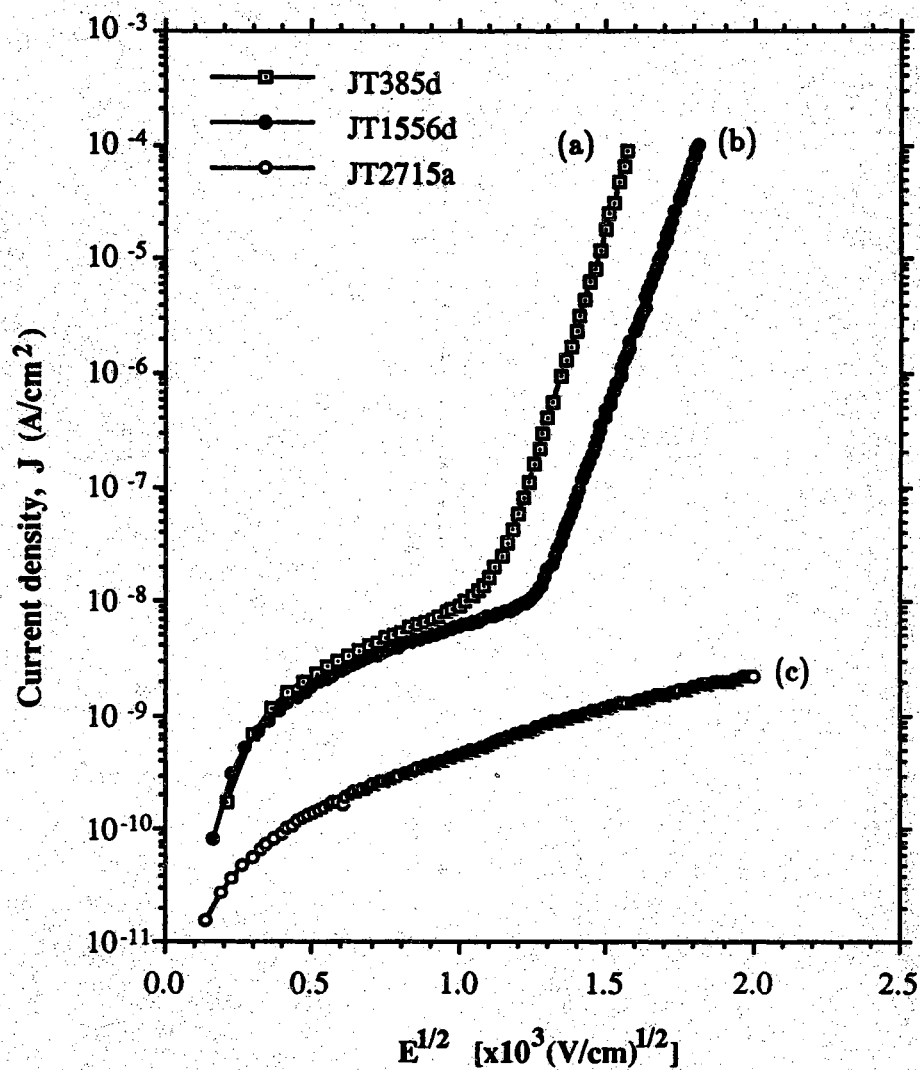
Figure 3.2   Current density vs square root of electric field for MIM capacitors at room temperature. The feeding gas flow ratios are as following: (a) $N_2/NH_3/SiH_4=0/30/18$, (b) $0/50/5$, (c) $50/50/5$ in sccm unit.

given by

$$J = A T^2 \exp\left[\frac{-q(\phi'_B - \sqrt{q\mathscr{E}/4\pi\epsilon_0\epsilon_d})}{kT}\right], \tag{3.1}$$

while Poole-Frenkel emission can be expressed as

$$J = C\mathscr{E}\exp\left[\frac{-q(\phi_B - \sqrt{q\mathscr{E}/\pi\epsilon_0\epsilon_d})}{kT}\right], \tag{3.2}$$

where A is the Richardson constant, C is a constant determined by the trap density, ϕ'_B and ϕ_B are the Schottky barrier height and Poole-Frenkel barrier height, and ϵ_0 and ϵ_d are the dielectric constant of free space and the dynamic dielectric constant, respectively. Equation (3.2) can be further rewritten as

$$\sigma = C\exp\left[\frac{-q(\phi_B - \sqrt{q\mathscr{E}/\pi\epsilon_0\epsilon_d})}{kT}\right], \tag{3.3}$$

in terms of conductivity σ with

$$\epsilon_d = 14.67/T^2[slope\,(log\sigma/\mathscr{E}^{1/2})]^2. \tag{3.4}$$

Therefore, if a Poole-Frenkel conduction mechanism dominates, a plot of $log\sigma$ vs $\sqrt{\mathscr{E}}$ gives a slope being twice that of the Schottky plot. The dynamic dielectric constant ϵ_d so determined identifies the conduction mechanism because it must satisfy the following self-consistent criteria

$$\epsilon_\infty \leq \epsilon_d \leq \epsilon_s, \tag{3.5}$$

where ϵ_∞ and ϵ_s are the optical and static dielectric constants respectively.

Figure 3.3 shows the high field Poole-Frenkel plot for the two films without feeding N_2. A least square fit to the data results in a dynamic dielectric constant of 2.66 for T385d and 3.44 for T1556d. For PECVD $a-SiN_x{:}H$ films, the refractive index is usually in the range of 1.75~2.36[133]. This corresponds to a optical dielectric constant range of 3.06~5.57. Although the Schottky plot also showed a straight line at high fields, it gave a dynamic dielectric constant below 1. Therefore, we conclude that the data are closely represented by a Poole-Frenkel model. The same conduction mechanism has also been observed for CVD Si_3N_4 films[134] and for PECVD $a-SiN_x{:}H$ alloy films[85, 135-138].

Besides the leakage current test, the main purpose for our DC conduction experiments is neither to add another piece of evidence for the conduction mechanism nor to quantitatively determine the barrier height or trap density. Rather, a qualitative relation between the conduction and the trap parameters
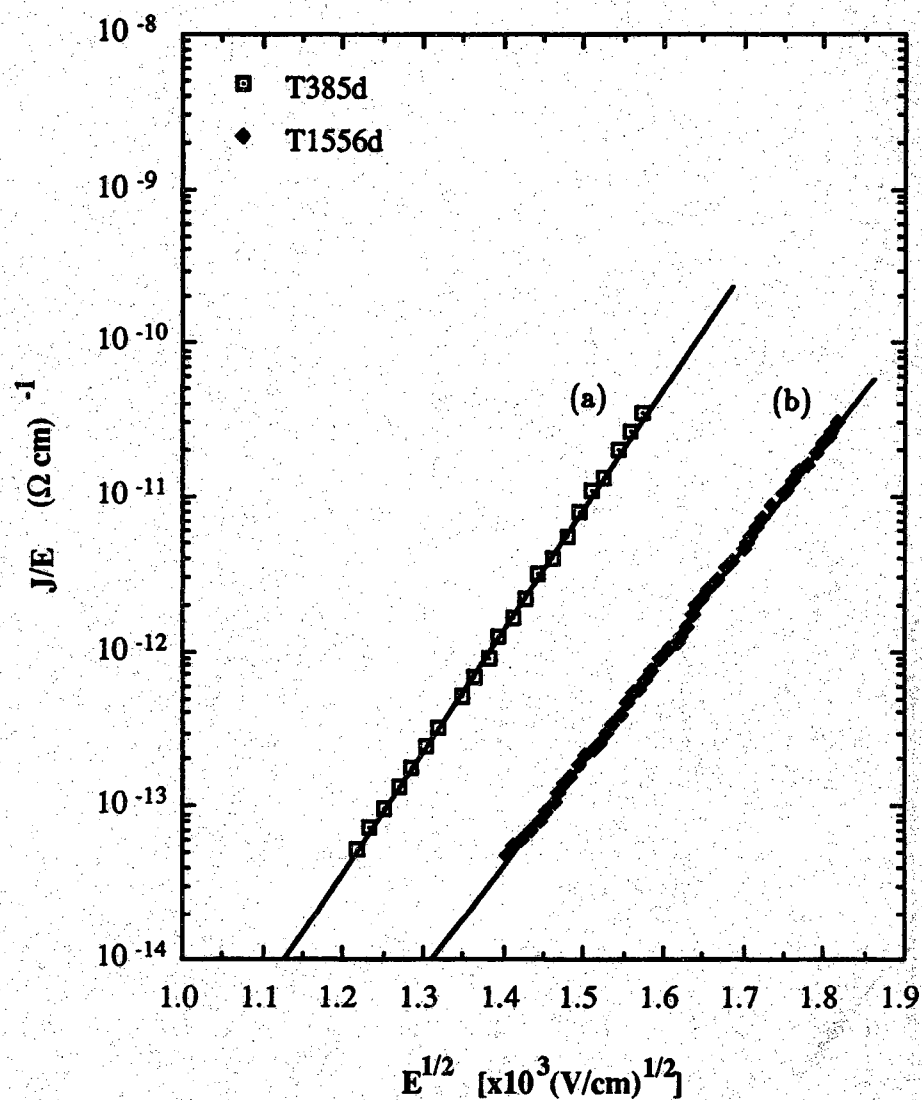
Figure 3.3 High field Poole-Frenkel plot for MIM capacitors at room temperature. (a) $N_2/NH_3/SiH_4 = 0/30/18$, (b) $0/50/5$ in sccm unit.

will serve our goal of process optimization. Specifically, we are interested in the zero field intercept σ_i of the $\log\sigma$ vs $\sqrt{\mathscr{E}}$ plot, where σ_i is given by

$$\sigma_i = logC - \frac{q\phi_B}{2.3kT} \ . \tag{3.6}$$

Obviously, a higher barrier height ϕ_B is desirable for a lower leakage current. Although the constant C is a function of trap density, it is usually not used for the interpretation of experimental data. First, the value of C depends on many material specific parameters such as the density of states of donors N_d, acceptors N_a and traps N_t. Secondly, σ_i is a very weak function of the trap density. In PECVD $a-SiN_x:H$, it is calculated that Si dangling bonds are the only intrinsic gap defect state[139]. In a sense, the Si dangling bonds can act as both trap and donor centers. This would give a trap density dependence of C only through the mobility term if we assume $N_d = N_t$ and use the expression $C = e\mu N_c(N_d/N_t)^{\frac{1}{2}}$ given by Simmons[140,141]. In a first approximation, $logC$ will be neglected and σ_i is assumed to be a function of ϕ_B only. Because a higher barrier height can also mean a lower defect density, σ_i might be a good indicator for both leakage current and defect density; that is, we want a σ_i as small as possible. Indeed, Maeda et al found that the barrier heights and dielectric strength become larger and stronger for films deposited at higher substrate temperature and rf power density, i.e., for film structure approaching that of a perfect Si_3N_4 film[85].

According to the above arguments, it can be inferred that film T1556d has a lower defect density than film T385d since σ_i of the former is about one order of magnitude smaller. Above all, film T2715a, deposited from the gas flow ratio of $N_2/NH_3/SiH_4$ =50/50/5 (in sccm), should have the lowest defect density because the I-V characteristics is still near ohmic up to 4 MV/cm.

3.2.3.2 Capacitance Measurement

The capacitance of the MIM sandwich was measured using an HP 4275A multi-frequency LCR meter. Ten discrete operating frequencies were available between 10 KHz and 10 MHz in 1-2-4 increments. The bridge normally provides 4½ significant digits of accuracy, but can supply an extra significant digit at the expense of longer measurement times by using the "high resolution" mode. To minimize external noise and wiring capacitances, the packaged devices and LCR meter were connected to each other through coaxial cables and devices were kept in the dark. The total parasitic capacitance in the

system was corrected by the zero-offset operation of the bridge and the circuit mode was in the parallel configuration. The static dielectric constant ϵ_s was then calculated from

$$\epsilon_s = C_{geo} d / A \epsilon_0, \tag{3.7}$$

where d, A, and C_{geo} are the sample thickness, sample area and geometrical capacitance. In general C_{geo} need not be equal to the measured capacitance C_m, as the latter may also include effects due to electrode layers, edge and stray fields.

To determine the appropriate frequency at which $C_m \simeq C_{geo}$, capacitors with different sizes and different compositions were first measured as a function of frequency. In general, measured capacitances decrease with frequency, especially near the higher end. For capacitors smaller than 2.5×10^{-3} cm^2, the relative decrease in C_m is in the range of 9%~20%. However, the dielectric loss for $0.1 cm^2$ capacitors is approximately 73%. Figure 3.4 illustrates the results for a sample of thickness $0.29 \mu m$ and area $0.01 cm^2$. It is noted that the capacitance tends towards a saturation value at lower frequences below about 400 KHz. The general shape is very similar to a Debye-type relaxation behavior although the relaxation time seems to be a little small. Because ac conductance was not measured, a Cole-Cole plot is not presented to verify this frequency dependence. Nevertheless, a least square fit is performed to see if one can get reasonable static dielectric constant ϵ_s, optical dielectric constant ϵ_∞, and relaxation time constant τ. By multiplying $A\epsilon_0/d$ to the Debye relaxation equation

$$\epsilon' = \epsilon_\infty + \frac{\epsilon_s - \epsilon_\infty}{1 + \tau^2 \omega^2}, \tag{3.8}$$

a three-parameter least-square fit gives 1.4, 7.5 and 3.4×10^{-8} s for ϵ_∞, ϵ_s, and τ respectively. The curve fitting is shown as the solid line in Figure 3.4 and should be considered very good. The resulting ϵ_∞ and ϵ_s values well agrees with literature values. This seems to indicate that the equivalent parallel circuit is a good model for the nitride films. Therefore, the static (zero-frequency) dielectric constants ϵ_s of all $a-SiN_x:H$ films were calculated from capacitances measured at 100 kHz.

The calculated static dielectric constants spread to a wide range between 7.3 and 14.3 although 85% of the values are lying in the range 7~9. Figure 3.5 gives dielectric constants histograms which were calculated from different sized capacitors on dice of the same wafer. The $a-SiN_x:H$ was deposited at a
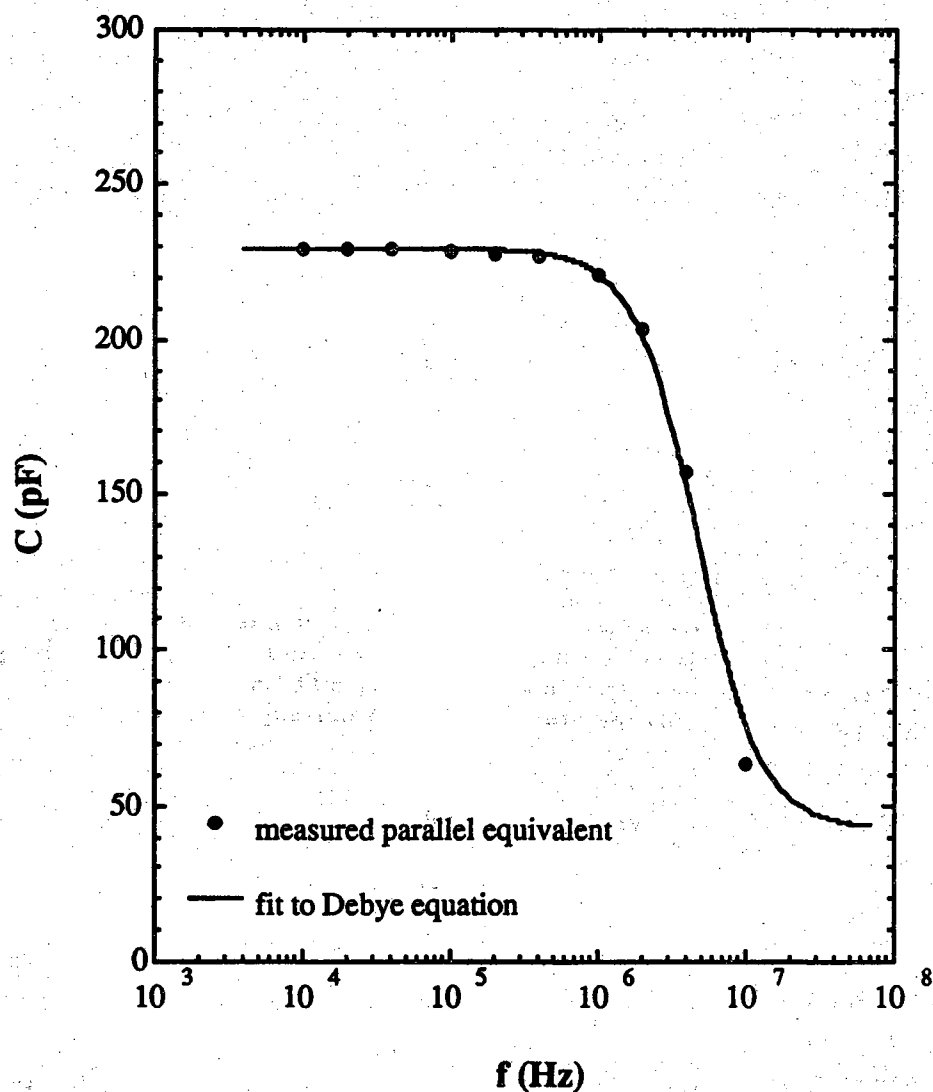
Figure 3.4   Plot of capacitance vs frequency for a $Cr-SiN_x-Cr$ capacitor (SiN_x thickness=0.29 μm and $A=0.01$ cm^2) at room temperature. The solid line is a least square fit to the Debye relaxation equation for the real value of the permittivity.
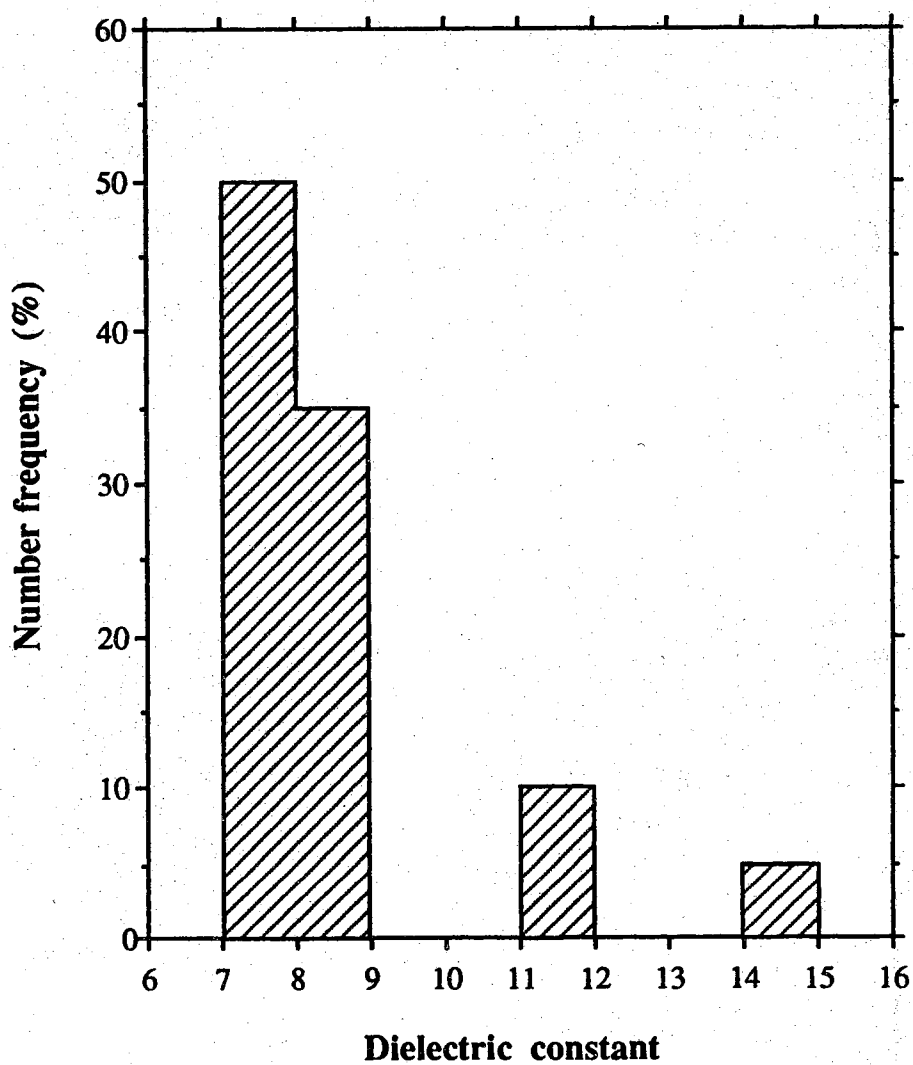
Figure 3.5   Frequency histogram of static dielectric constant for capacitors with a—SiN$_x$:H deposited at a feeding-gas composition of N$_2$/NH$_3$/SiH$_4$= 50/50/5 (in sccm).

feeding-gas composition of $N_2/NH_3/SiH_4$=50/50/5 (in sccm). However, there appears a general pattern between the dielectric constant and the capacitor size. Generally, the apparent dielectric constant increases with decreasing capacitor size and its standard deviation is less than 0.1 for a given size. This size effect is shown in Figure 3.6 in terms of dielectric constant vs lateral dimension of the square capacitors.

To understand the larger apparent ϵ_s values for smaller capacitors, one must consider parasitic and contact effects. Most importantly, it should be borne in mind that the experimental MNM capacitors are two terminal devices because guard electrodes were not implemented. As such, they are subject to fringing and stray capacitance effects. Fringing effects give rise to an edge capacitance C_e that causes the measured capacitance C_m to be higher than the true geometric value C_{geo} and its weight increases with decreasing capacitor size. If these parasitic capacitance can be expressed in terms of farads per centimeter of parameter, C_p, then the measured capacitance C_m would have the following form

$$C_m = C_0 A + C_p P , \tag{3.9}$$

where P is the parameter of the capacitor. Therefore, the measured apparent dielectric constant ϵ_m should also have a correction term added to the true dielectric constant as is given by

$$\epsilon_m = \epsilon_r + \frac{C_p d}{\epsilon_0} \frac{P}{A} . \tag{3.10}$$

If the above assumption holds, ϵ_m should be a linear function of (P/A) and the y-intercept gives the true dielectric constant ϵ_r. As shown in Figure 3.7, the measured data points are very well represented by a straight line. This gives a true dielectric constant of 6.6 and the parasitic capacitance C_p of 59.5 pF/cm. It is estimated that C_e due to fringing effects should be a small fraction of C_p even for the smallest capacitors (1×10^{-4} cm^2) measured. Therefore, there must be other stray capacitances which are proportional to (P/A). In passing, the electrode contact effect can not be neglected. One example would be a MIM capacitor with blocking contacts. In this case, the measured capacitance becomes frequency independent and equal to the geometric capacitance only at very high frequency [142, 143]. However, this seems to be not the case here because the Schottky barrier capacitance is also proportional to the capacitor area.
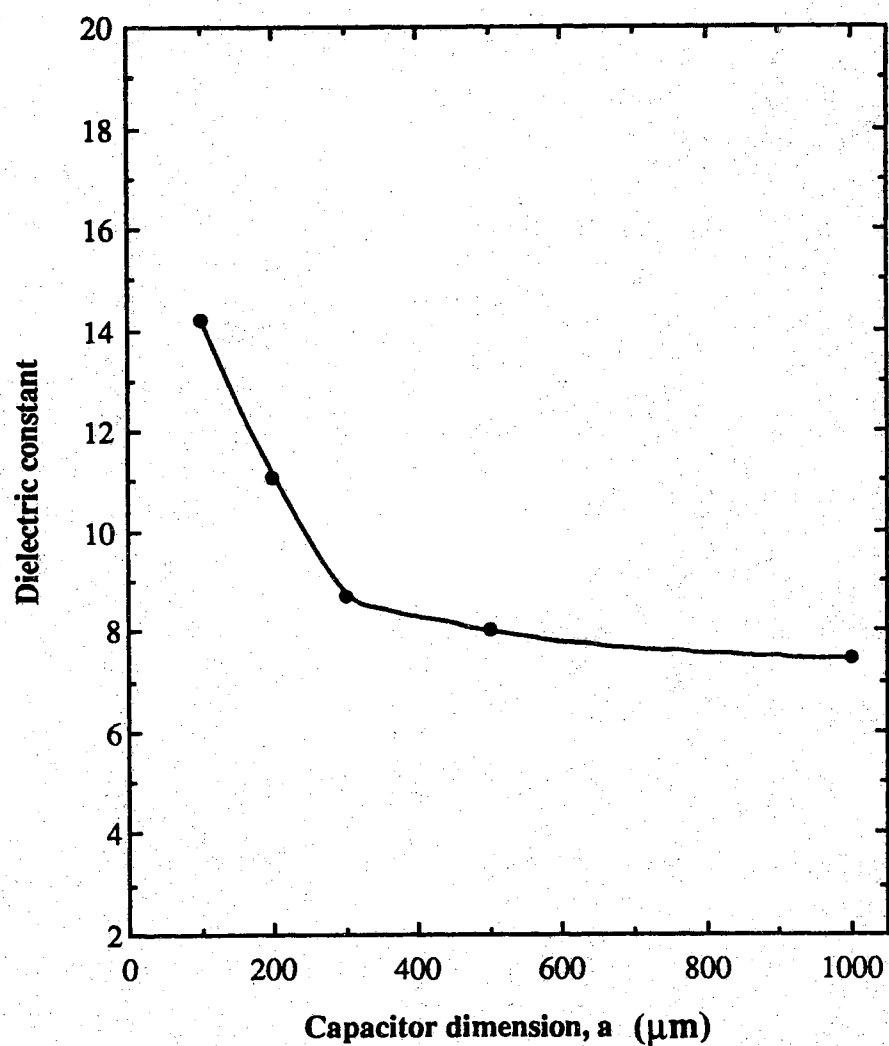
Figure 3.6   Calculated dielectric constant vs lateral dimension of the square
capacitors with a–SiN$_x$:H deposited at a gas composition of
N$_2$/NH$_3$/SiH$_4$= 50/50/5 (in sccm).
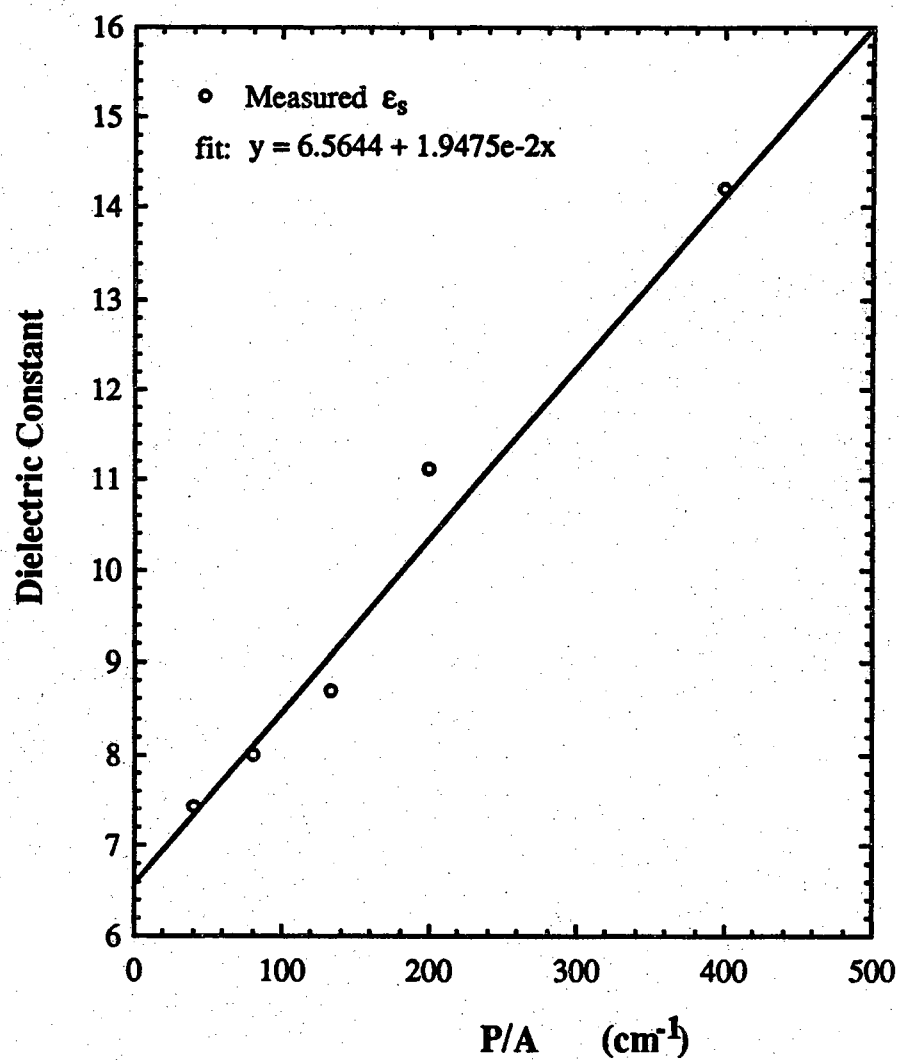
Figure 3.7 Measured apparent dielectric constant as a function of the area normalized parameter.

3.3 Fabrication and Performance of Initial a-Si:H TFTs

3.3.1 Introduction

The main reason for going into the troublesome characterization of $a-SiN_x:H$ was to find an optimal set of deposition parameters and to fabricate a-Si:H TFTs without external insulators. Although the optimization described in the last section is definitely incomplete due to, among others, time limitation, a better condition is obviously the one using $SiH_4/NH_3/N_2$ as the inlet gas composition. To demonstrate this conclusion, TFTs using the optimized nitride as the gate insulator were fabricated. This would also serve as the starting point for future optimization and for investigating the device physics.

To establish a performance baseline from which to compare the performance of the TFTs made with the optimized $a-SiN_x:H$ films and other films previously used here, the old TFT mask set was used for the fabrication. Except for the SiN_x deposition step and the sputter-deposited Cr gate metalization, the TFT device structure and the fabrication processes are the same as those described elsewhere[144]. However, for continuity and understanding, only an illustrative description is given in this document.

3.3.2 Device Structure and Fabrication Steps

The a-Si:H TFT device is of the inverted-staggered structure as shown in Figure 3.8. The entire structure was fabricated on a 2 inch silicon wafer with thermally grown SiO_2, which neither influences the device characteristics nor the fabrication process. Three masking levels were used for the fabrication of this structure. They were the gate metal definition, a-Si:H/$a-SiN_x:H$ island etching, and source-drain ion implantation/metalization. The drawn dimensions of the devices were as following. One group of the devices had a fixed channel width of 950 μm and varied channel lengths of 25, 50, 75, 100, 150, and 200 μm. There were also devices with a channel length of 10 μm and channel widths of 450 and 950 μm respectively. The following outline highlights the fabrication steps in the processing of the initial TFTs. Figure 3.9 illustrates the cross-sectional views at each of the major steps.

1. Gate metallization (MASK 1)

   After defining the gate metal pattern using positive photoresist, chromium film was deposited using the PERKIN ELMER sputtering system and liftoff was performed in acetone with the help of ultrasonics. To get a
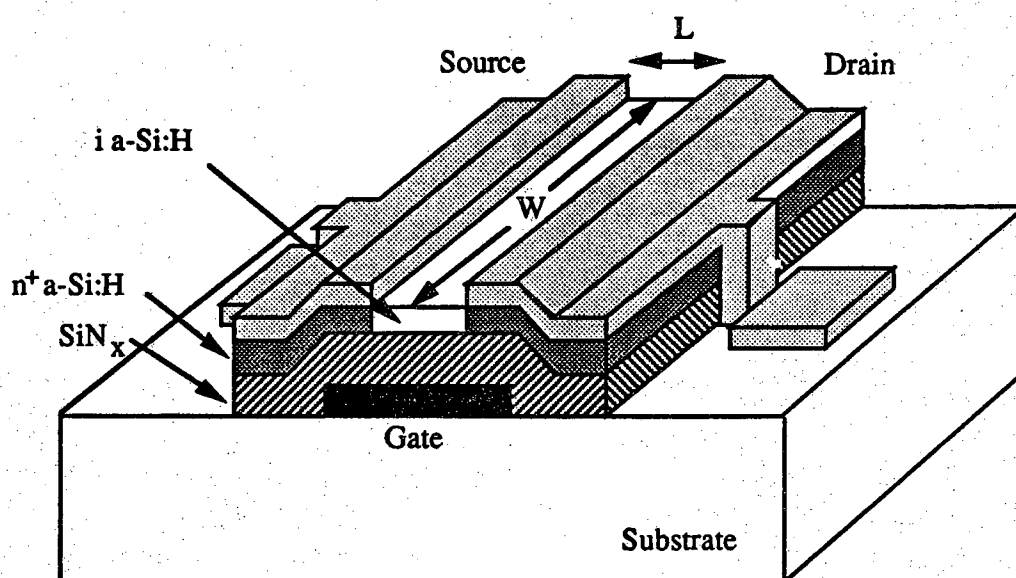
Figure 3.8   A three dimensional view of the a-Si:H thin film transistor.
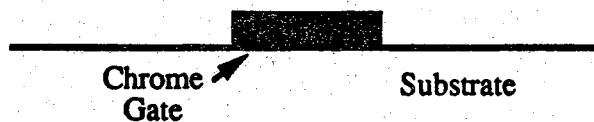
(a) Deposit and define the chrome gate using the first mask
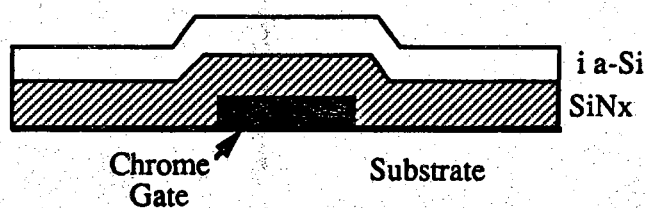
(b) Deposit SiNx and i a-Si:H using PECVD
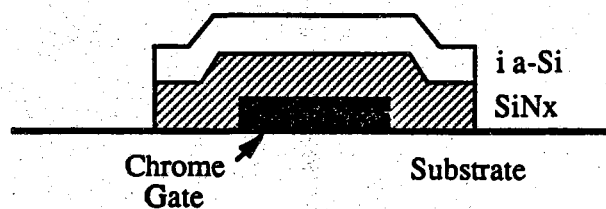
(c) Define SiNx and i a-Si:H using second mask and plasma etch the unwanted regions

Figure 3.9   Cross sections of the TFT after major fabrication steps.
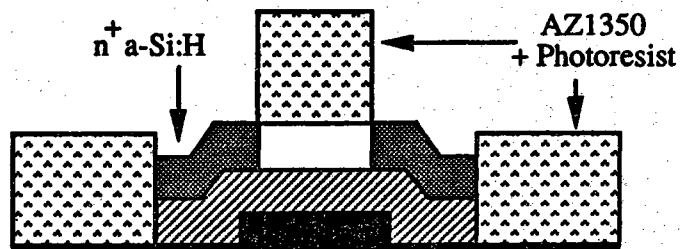
(d) Define postive resist mask and ion implant phosphorus to form source- drain contact regions
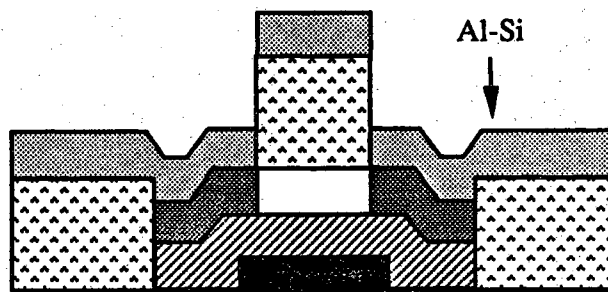
(e) Deposit Al-Si over the entire wafer surface
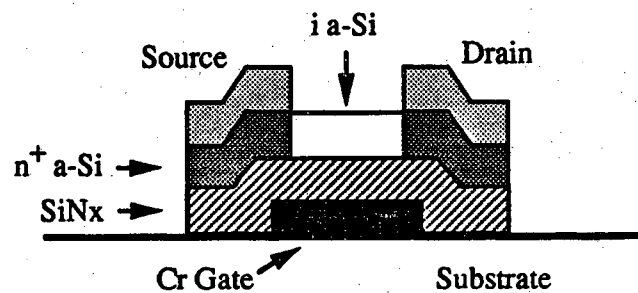
(f) Liftoff the Al-Si to obtain the final device cross-section

Figure 3.9 (Continued.)

clean and smooth chrome surface and to prevent photoresist damage, a combination of sputter deposit and bias sputter modes were used during the film deposition. By trial and error the following conditions were obtained:

    1) presputter target for 30 minutes as usual,
    2) sputter deposit Cr on wafers for 2 minutes:
        Ar pressure=6 mT
        forward power=100 W
    3) bias sputter for 15 minutes:
        Ar pressure=6 mT
        forward power=100 W
        substrate bias=25 V

This gave a chromium thickness of 850$\overset{\circ}{A}$.

2. $a-SiN_x:H$ and a-Si:H deposition

Load the wafer into the TECHNICS plasma system and deposit $a-SiN_x:H$ with the following conditions:

        RF power=50 W
        Temperature=300 ° C
        Pressure=612 mT
        $NH_3/N_2/SiH_4$=50/50/5 (in sccm)
        Time=7 minutes

This yields approximately 1500 $\overset{\circ}{A}$ of nitride.

It should be mentioned that before growing the a-Si:H film the change-over of gasses may be very important. This was done by purging the system with 50 sccm SiH_4 until the temperature became stable at the new setting.

The a-Si:H was then deposited using the following condition:

        RF power=6 W
        Temperature=260 ° C
        Pressure=350 mT
        SiH_4=50 sccm
        Time=18 minutes

The deposition was performed at a rate of 39 $\overset{\circ}{A}/min$ resulting in about 700 $\overset{\circ}{A}$ of a-Si:H. However, the deposition rate very much depends upon the wafer location on the ground electrode with the worst variation of

300%. This is largely because of the reactor design such that the inlet gas dispersing is non-uniform. In addition, the lower pressure used also contributes to the non-uniformity. It has been verified that the film thickness is very uniform across the whole ground electrode if a gas pressure of 500 mT is used while keeping the residence time constant. Therefore, a wafer is always kept at a fixed location for different runs.

3. Plasma etching of SiN_x and a-Si:H (MASK 2)

Islands of the a-Si:H/SiN_x were defined using positive photoresist. The unwanted parts were then etched off in the CF_4 plasma under the following condition:

> RF power=80 W
> Pressure=200 mT
> CF_4=20 sccm
> Time=10 minutes.

4. Source/Drain implantation (MASK 3)

A double layer of AZ 1350J-SF photoresist was used for the ion implantation mask. By simply repeating the positive photoresist procedure twice, a 2.3 μm layer was obtained. An Accelerators, Inc. AIM 210 implanter was used to implant phosphorus ions with a dose of $10^{16} cm^{-2}$, energy of 30KeV and with a beam current less than 50 μA.

5. Metallization and Anneal

After source/drain implantation, about 0.1 μm of Al-Si was sputter deposited in the PERKIN ELMER sputtering system. The photoresist mask for ion implantation also served as the liftoff pattern here. Care must be taken not to damage the Al contact feature since the ion implanted photoresist is difficult to remove in acetone. To improve contact performance, a post metallization anneal was then performed in the TECHNICS plasma system. Annealing conditions were:

> Temperature=200 ° C
> Pressure=550 mT
> N_2/H_2=30/45 (in sccm)
> Time=30 minutes

3.3.3 Performance of Initial a-Si:H TFTs

The a-Si:H TFT characterization measurements were performed on the same HP data acquisition system as described in the DC conduction of $a-SiN_x:H$. Both transfer (I_D vs V_G) and output drain (I_D vs V_D) characteristics were measured through the control of the software program TFTIVB. The transfer characteristics were retraced back to the start voltage to examine the device hysteresis, while the output drain characteristics included only a forward voltage sweep. A hold time of 10 second was used to allow settling of the device current at each applied voltage.

The probe-level characteristics of a-Si:H TFTs fabricated in this initial run are shown in Figure 3.10 to Figure 3.12. Figure 3.10 shows the transfer characteristics which is representative of 15 tested devices. It gives subthreshold slope of 0.47 V/decade, a maximum hysteresis width of 0.48 V, and current ON/OFF ratio of larger than 10^7. The best results among the tested are shown in Figure 3.11 and Figure 3.12 with its transfer and output characteristics. The most obvious attribute in Figure 3.11 is its very small hysteresis. In terms of most standards used for characterization, the performance of these devices is at least comparable to those state of the art results reported in the literature. To help realizing the importance of the aforementioned $a-SiN_x:H$ optimization process, it is most revealing to directly compare the present devices with those fabricated using the same process. Figure 3.13 illustrates the transfer characteristics of devices using unoptimized Purdue $a-SiN_x:H$. The $a-SiN_x:H$ was deposited at a gas pressure of 330 mT and a NH_3/SiH_4 ratio of 30/18 (in sccm). Temperature and rf power were the same as used in the present case. The unacceptably large hysteresis was shown to be the result of a significant charge trapping in the gate nitride[144].

The hysteresis exhibited by the transfer characteristics has been attributed to charge trapping in $a-SiN_x:H$, interface state traps, and the bulk a-Si:H traps. The transfer curve does not give information about each individual trapping mechanism but only their combined effect. However, for devices fabricated under the same process and using the same a-Si:H, then the hysteresis width is indeed a figure of merit which can be used to compare charge trapping effects in the gate nitride. Looking back at the deposition conditions of the MNM $a-SiN_x:H$ T385d, one notices that they are almost the same as those used for the unoptimized nitride of Figure 3.13. Therefore, their leakage and trapping properties should very much resemble to each other. In Section 3.2.3.1, it was argued that $a-SiN_x:H$ deposited with N_2 addition (T2715a) should have a lower defect density than those deposited without N_2
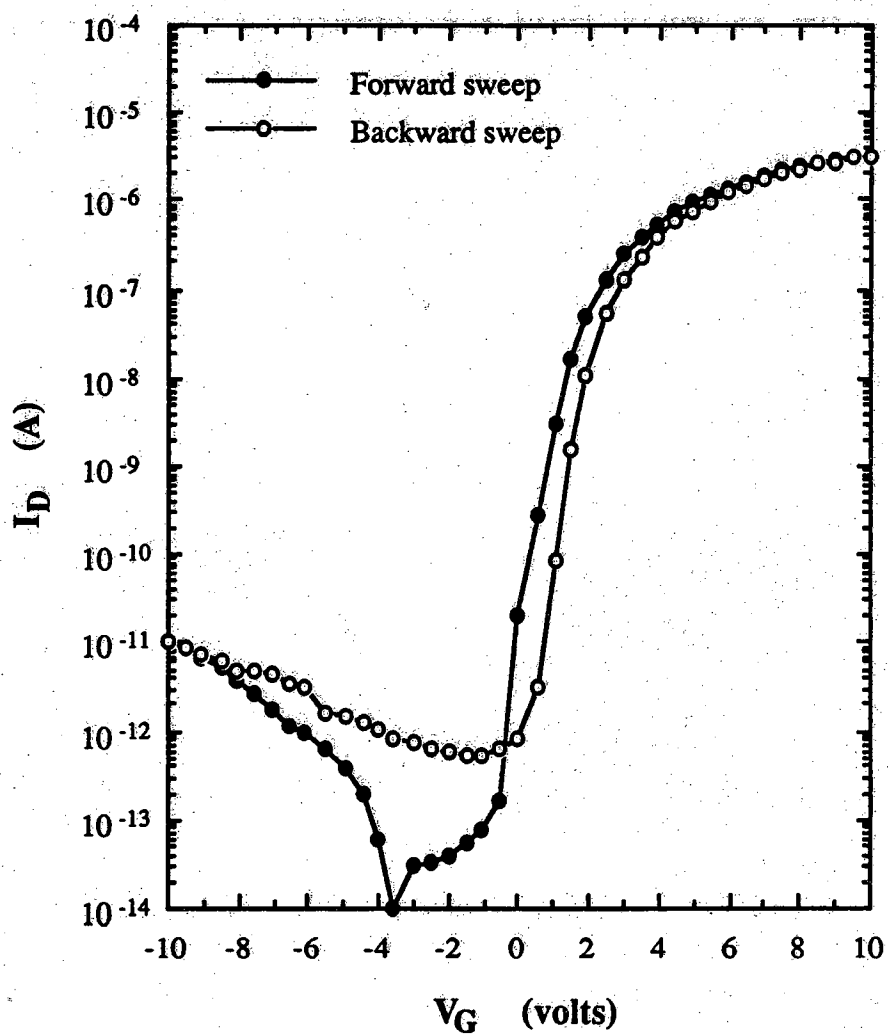
Figure 3.10   The typical transfer characteristics of the initial TFTs with Purdue SiN$_x$. Device #T1-6441 (W/L=950/100=9.5, V$_D$=2 V).
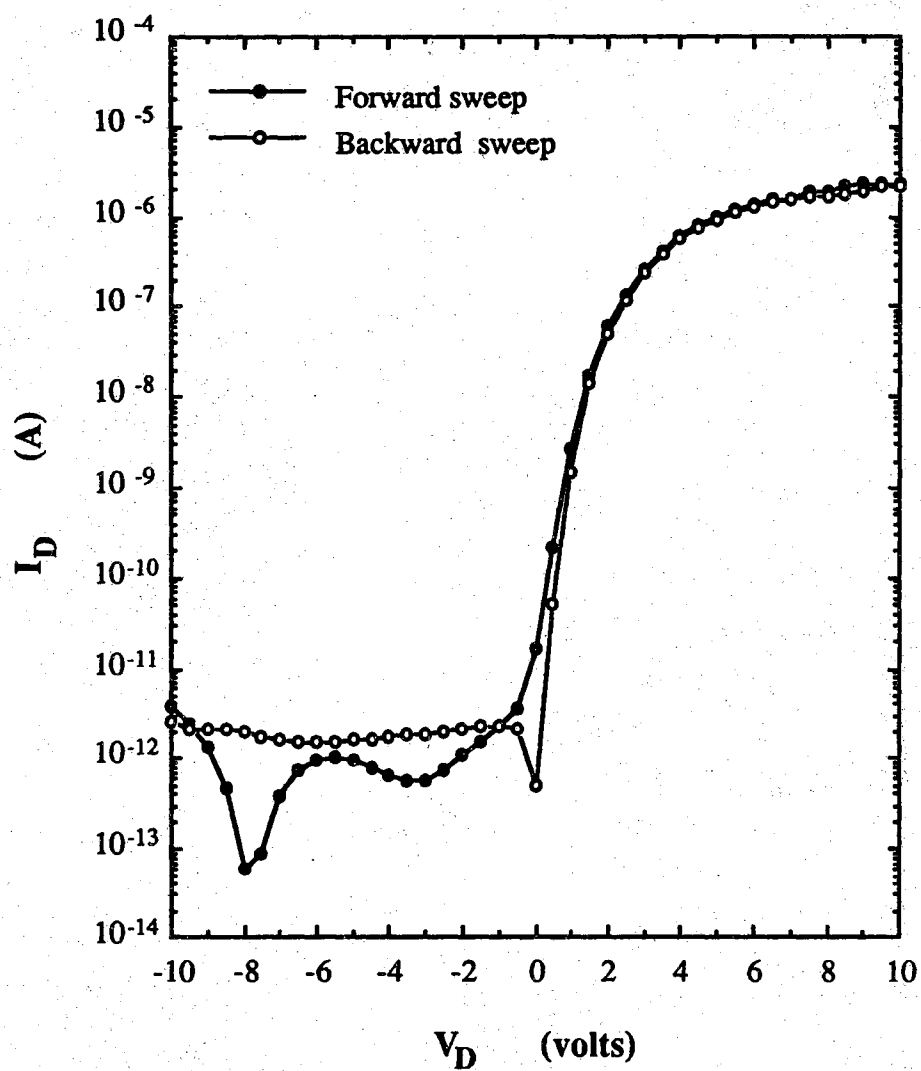
Figure 3.11   The best transfer characteristics of the initial TFTs among 15 measured devices with Purdue SiN_x. (W/L=9.5, V_D=2 V).
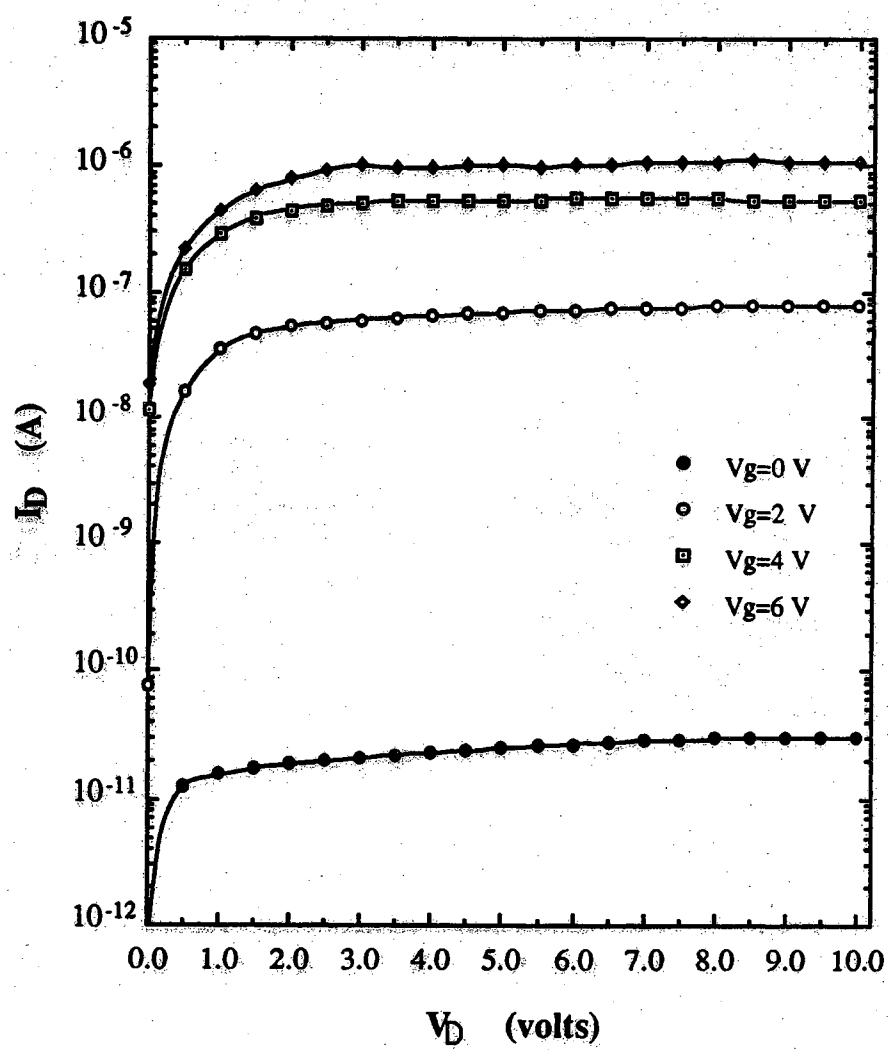
Figure 3.12   The output characteristics of the device in Figure 3.11.
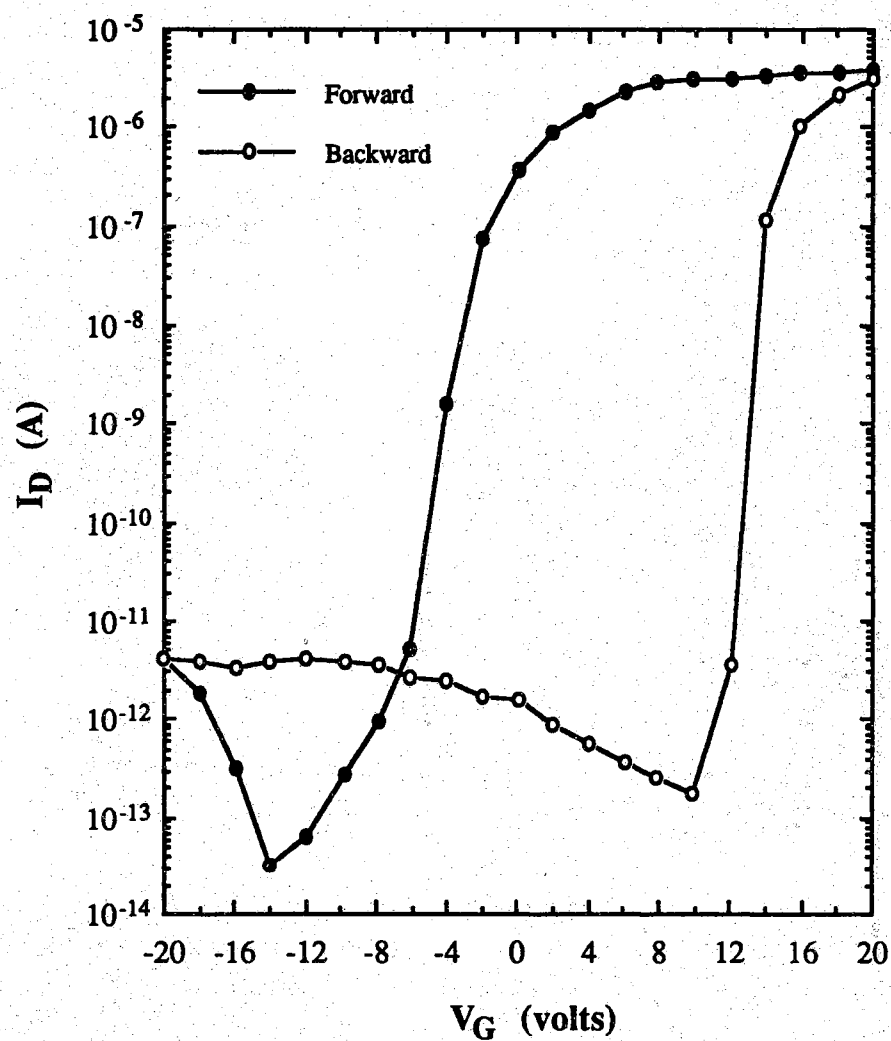
Figure 3.13 The transfer characteristics of a-Si:H TFT with unoptimized Purdue a—SiN$_x$:H deposited at NH$_3$/SiH$_4$=30/18 (sccm)[144] .

and under a higher SiH_4 to NH_3 flow ratio (T385d, T1556d). It appears that the conclusion drawn from MNM DC conduction still holds in $a-SiN_x:H$ gated a-Si:H TFTs as far as hysteresis is concerned. Therefore, MNM device can be a simple and useful test structure for optimizing not only leakage current but also trapping characteristics.

3.4 Effect of RF Power and NH_3 Plasma Treatment of the Gate Nitride

3.4.1 Introduction

As mentioned in Chapter 2, much of the research on improving material quality in a-Si:H TFTs has been focused on gate a-$SiN_x:H$. This is because it is a three element alloy and its quality as a gate material is greatly dependent on its deposition conditions. Many research groups have published results concerning this aspect. However, the basic physics and chemistry have not yet been fully understood. The preliminary work on $a-SiN_x:H$ deposition as described in Section 3.2 only investigated the influence of the inlet gas compositions. Although significant improvement in TFT characteristics was achieved, there may be much room for further work in view of the large variable space of the PECVD system. One of the more important macroscopic parameters is the rf power density. It was found that the nitrogen concentration increases with increasing rf power density. The hydrogen concentration and fixed surface charge density in $a-SiN_x:H$ decrease with increasing rf power density[145]. However, the high energy particles (primarily ions) at high rf power may create more defects in the growing $a-SiN_x:H$ films. Hence there seems to be an optimal power density between these two extremes.

Plasma technologies have been used extensively in the last decade not only for the fabrication of very large scale integrated (VLSI) circuits, but also for the modification of various material properties. This has led to the development of plasma nitridation techniques for both bare silicon surfaces and thermal oxidized Si[146-149]. It was observed that nitridation of silicon can occur by NH_3 plasma treatment and it resulted in MISFETs with high field-effect mobility[150]. The nitridation reaction is also chemically possible with other materials. Indeed, $a-Si_3N_4:H$/a-Si:H superlattices have been fabricated by using the plasma enhanced nitridation of a-Si:H[151]. This low temperature technology would give another degree of freedom in a fabrication process. However, studies have shown that plasma-induced defects in the SiO_2/Si structure are similar to those created by other radiation sources, which results in the trapping of positive charge in the oxide, generation of interface states,

and neutral traps. In the fabrication processes of a-Si:H TFTs, NH_3 is a common deposition gas and its plasma consists of various nitriding species and excited hydrogen which is often beneficial due to its ability for dangling bond passivation. Therefore, it would be very interesting and important to know whether the NH_3 plasma will improve or degrade the interface properties of the a-SiN_x:H/a-Si:H structure.

In the experiments of this section, the a-SiN_x:H gate insulator, deposited at different rf power densities, was first treated with NH_3 plasma, and this was then followed by a-Si:H deposition as is typical for staggered inverted TFTs. Results were obtained directly from a-Si:H TFTs by measuring their transfer characteristics and by other bias-temperature stressing experiments.

3.4.2 Device Fabrication and Characterization

The TFTs used in this work have the same structure and fabrication sequence as detailed in subsection 3.3.2. The differences is in the deposition of SiN_x gate insulator and its plasma treatment. For all wafers, a-Si:H films were deposited from a glow discharge of pure SiH_4, at a substrate temperature of 260°C and rf power of 6 W. The gas pressure was 0.35 Torr and flow rate was 50 sccm. For the deposition of SiN_x, the substrate temperature was fixed at 320°C and the gas pressure at 0.6 Torr, and the flow rates of gases were $NH_3/N_2/SiH_4 = 50/50/5$ (sccm). The rf powers used were 25, 50 and 100 W.

For those runs with NH_3 plasma treatment immediately following SiN_x deposition, a pump-out of residual gases was followed by 10 minutes of NH_3 plasma treatment performed at a rf power density of 40.8 mW/cm^2 with a gas pressure of 0.5 Torr and flow rate of 50 sccm. The gas change-over prior to a-Si:H deposition was done by purging the system with 50 sccm of SiH_4 and by repetition of pump-down (<90 mT)/purge (600 mT) for three times.

Electrical characteristics of the TFTs were measured on packaged devices with an HP 4140B pico-ammeter/DC voltage source, which is controlled by an HP 9000 series 236 computer through the software program TFTIVT. The threshold voltage and field effect mobility were determined from the x intercept and slope of the square law model[152]. All current was measured with a hold time of 10 s after each voltage change.

3.4.3 TFT Subthreshold Characteristics

Figure 3.14 is representative of the transfer characteristics of a-Si TFTs deposited at an rf power of 100 W with no plasma treatment, while Figure 3.15 for the corresponding plasma treated devices. All devices measured showed an current on/off ratio of larger than 10^7 with an off current, for $V_g < 0$, less than 10^{-13}, the noise level of the present measurements. However, differences exist in the two important parameters of the transfer characteristics, namely 1) the subthreshold slope (S), defined as the inverse of logarithmic $I_D - V_G$ slope which is $dV_{GS}/d(logI_D)$ and 2) the width of hysteresis.

The subthreshold slope S is directly related to the ability to shift the Fermi level through the distribution of gap states N(E) and therefore is an useful measure of the effective density of gap states N_i [3] in the bulk a-Si:H and any interface states present between the insulator and a-Si:H. An approximate relation can be written as[153]

$$N_i = \frac{\epsilon_o}{\epsilon_{si}} \left(\frac{\epsilon_{ins}}{k_B T d_{ins}} S \right), \tag{3.11}$$

where ϵ_o is the permittivity of free space, ϵ_{si} and ϵ_{ins} are the dielectric constants of amorphous silicon and gate insulator, respectively, T is the measurement temperature and d_{ins} the thickness of the gate insulator. For all devices, the a-Si:H was deposited under the same conditions. The gate nitride deposition conditions were identical except for rf power levels of 25, 50 and 100 watts. For those NH_3 plasma treated SiN_x surfaces, the conditions were also kept constant. Hence, the subthreshold slope S gives information exclusively about the interface; i.e., the smaller the S, the smaller the interface state density. Figure 3.16 shows the subthreshold slope dependence on rf power of SiN_x deposition and on NH_3 plasma treatment. It can be seen that S decreases with increasing rf power density, especially at higher values. At the time of this writting, the N/Si ratio of the gate $a-SiN_x:H$ has not been experimentally determined under the different rf power densities. However, research on PECVD $SiN_x:H$ has already indicated that N/Si ratio increases with rf power[79, 154]. Although the correlation between N/Si ratio and the $SiN_x:H/a-Si:H$ interface property is still not fully understood, the results of Figure 3.16 tend to agree that higher rf power deposition and therefore more N-rich $SiN_x:H$ make a better interface with a-Si:H[155].

The NH_3 plasma treatment caused a general increase in subthreshold slope for all rf power depositions of gate nitride, as seen in Figure 3.16. This effect may be explained as follows. First, energetic species such as electrons,
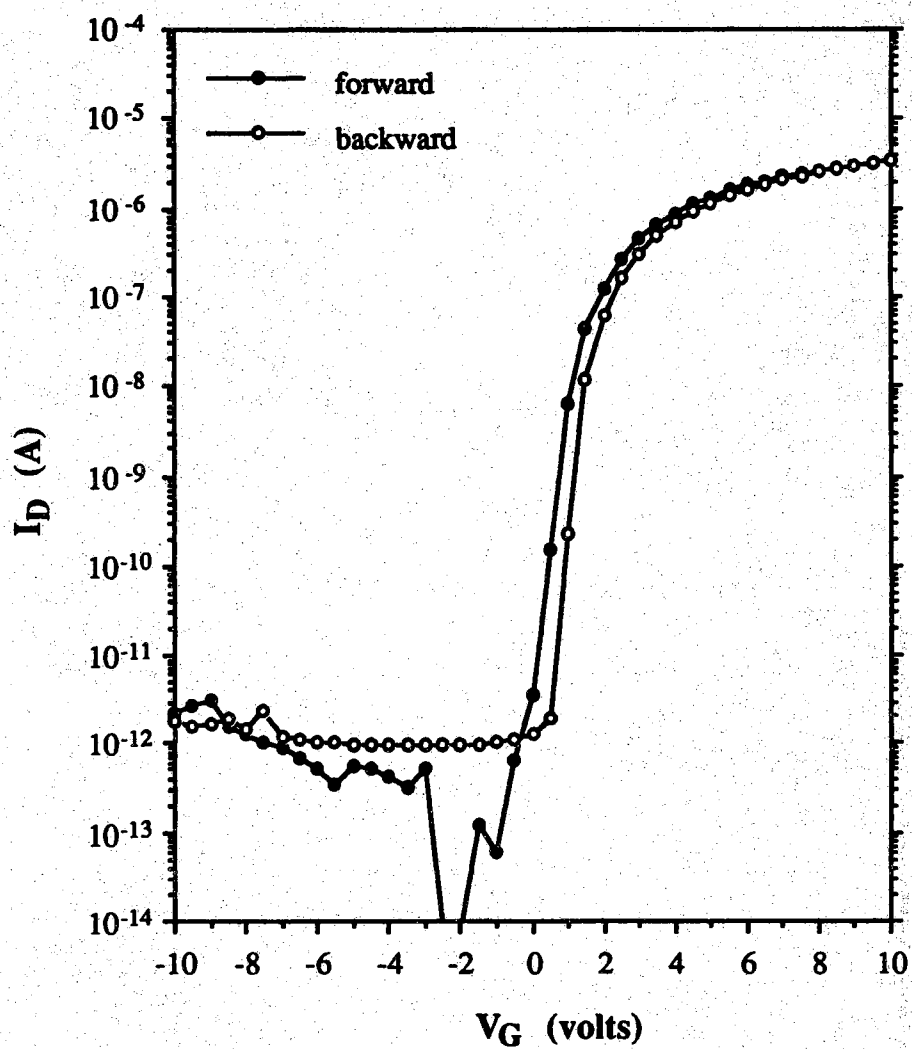
Figure 3.14   Transfer characteristics ($V_{ds}=2$ V) for a gate nitride deposited at 100 W, without NH_3 plasma treatment.
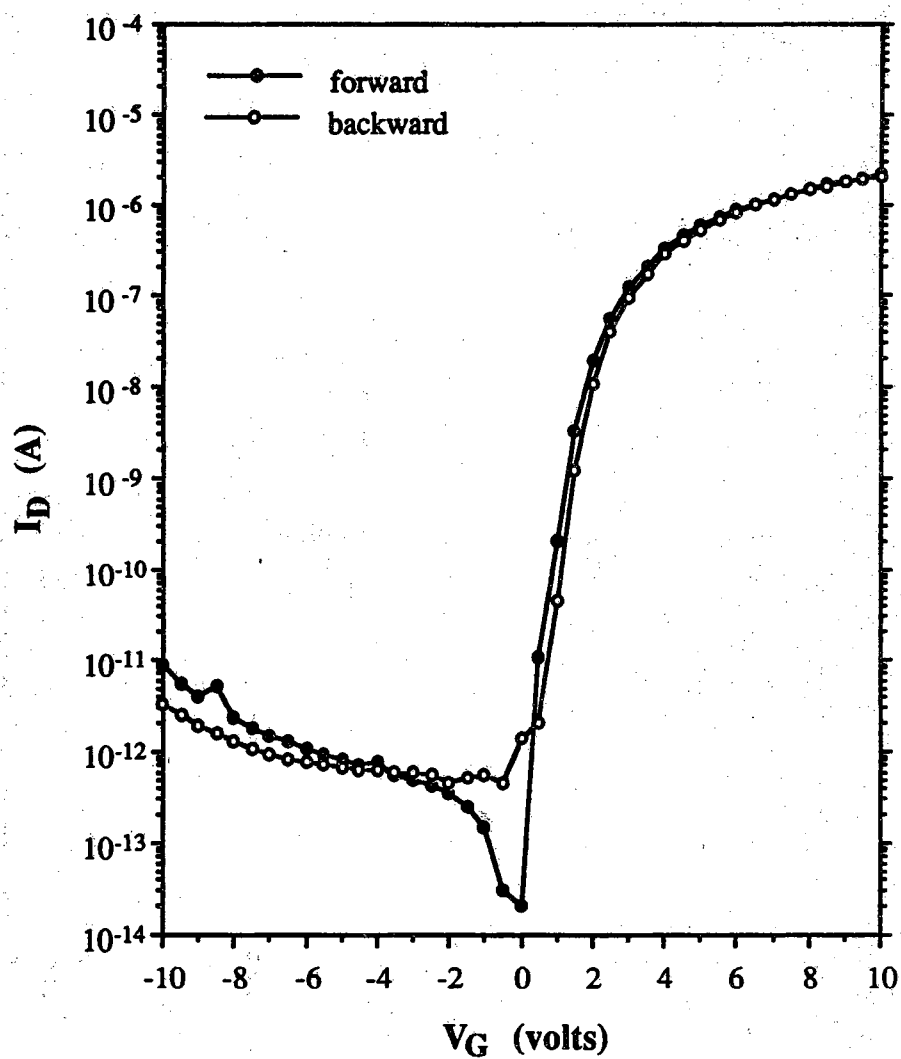
Figure 3.15 Transfer characteristics (V_{ds}=2 V) for a gate nitride deposited at 100 W, with NH_3 plasma treatment.
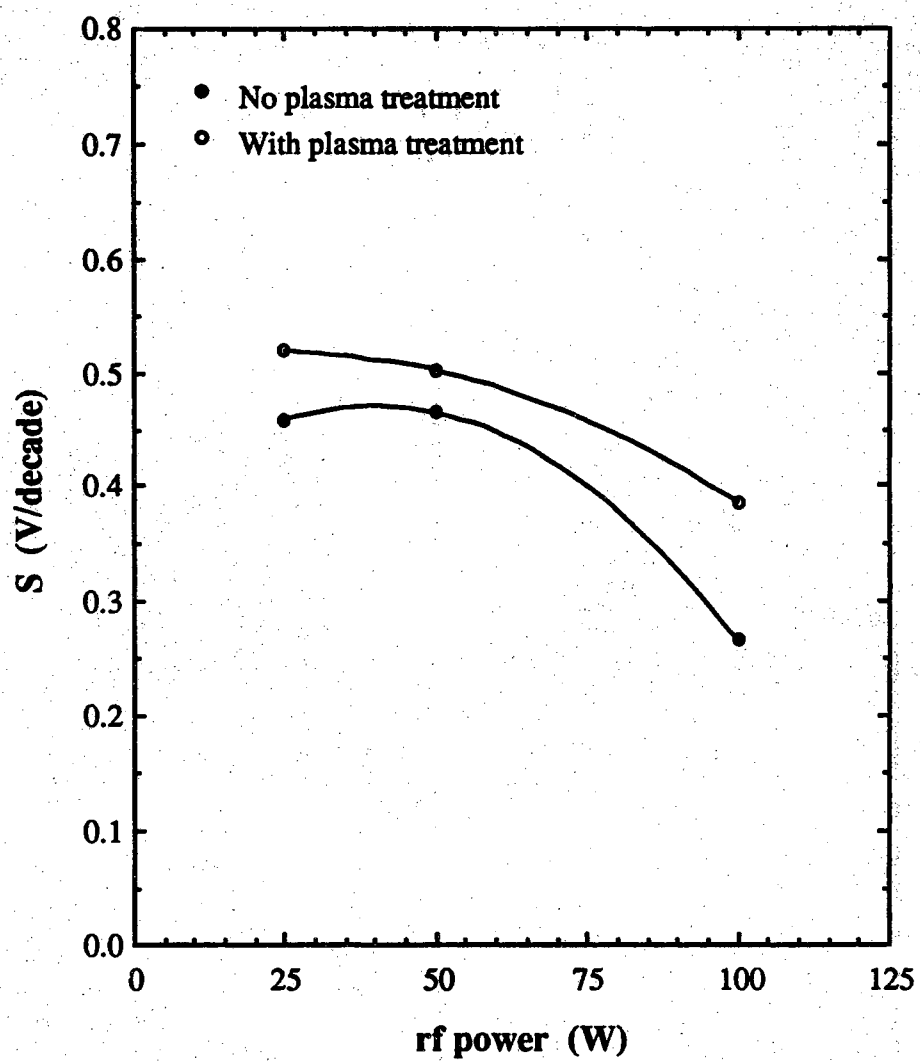
Figure 3.16   Subthreshold slope dependence on rf power of gate nitride deposition and on NH₃ plasma treatment.

ions and photons in the plasma may induce radiation damage, creating interface defects/traps and therefore increasing the TFT subthreshold slope. Second, plasma surface nitridation and/or amination may occur. The latter makes the SiN_x surface more N-rich which leads to a lower subthreshold slope. One or both of these competing effects could occur. However, for the particular plasma conditions used in the present experiment the first mechanism appears to dominate the plasma-surface interaction as far as the effective interface states is concerned. The larger increase in S at 100 W is consistent with the assumption that SiN_x:H there may already be N-rich and therefore radiation damage may be the entire reason.

3.4.4 Threshold Voltage and Field Effect Mobility

As discussed in Chapter 2, in the presence of a continuous distribution of localized states, varying the gate voltage alters the ratio of free to trapped electrons resulting in a gate field-dependent mobility. The saturation drain current in the above threshold regime is usually expressed as[105]

$$I_D^{sat} = K(V_G - V_T)^\gamma \qquad (3.12)$$

Where K and γ are functions of different material parameters. Thus, unlike the case of crystalline MOSFET, plots of $I_D^{1/2}$ vs V_G are generally no longer straight lines. In addition, a contribution to the curvature may arise due to variation in the TFT series resistance with gate voltage. However, when this curvature is minimized, the standard square law MOSFET expression is very helpful for the purposes of comparison and process optimization. Therefore, the model was used in this study to extract threshold voltage and carrier mobility parameters. The saturation condition was met by connecting the gate and drain electrodes together. The threshold voltage and field effect mobility are then obtained from the x intercept and the slope of a linear fit to the $I_D^{1/2}$ vs V_G characteristics. For all devices measured, the fitting is quite good (see Figure 3.20).

The threshold voltage in a-Si:H TFTs is also sensitive to deep interfacial charge (Q_{it}) as well as trapped charge (Q_{tr}) in the gate insulator. Therefore, any variation in these charges causes a shift in V_T given by

$$\Delta V_T = -\frac{\Delta Q_{it} + \Delta Q_{tr}}{C_{ins}} \qquad (3.13)$$

where C_{ins} is the gate nitride capacitance per unit area. Figure 3.17 shows the square-law threshold voltage dependence on rf power and the influence of NH_3
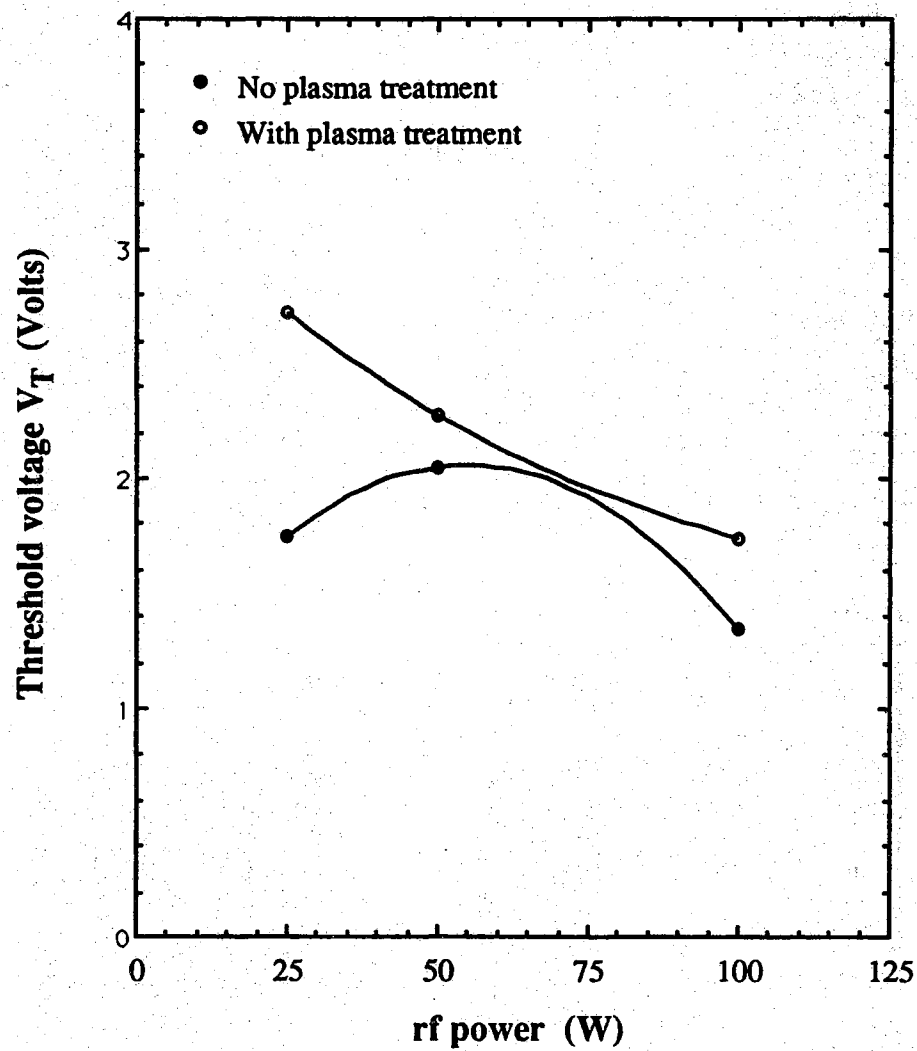
Figure 3.17   Threshold voltage variations at different rf power of gate nitride deposition and the effect of NH_3 plasma treatment.

plasma treatment. The data points are averaged values over at least three devices. Although the data for untreated devices are somewhat scattered, high rf power deposition at 100 W appears to lead to a lower threshold voltage. This indicates a lower interface states and is correlated well with its lower subthreshold slope exhibited in Figure 3.16. Also shown in Figure 3.17 are the increased threshold voltages for all plasma treated devices.

The field effect mobility calculated from the square law model is shown in Figure 3.18. Again, larger rf power deposition of the gate insulator is preferred for a higher field effect mobility. When increasing the rf power from 25 W to 100 W, an increase in field effect mobility, from 0.29 to 0.37 $cm^2/V-s$, was obtained. This is once again consistent with the above conclusion that gate nitride deposited at higher rf power has a better interface with a-Si:H. However, a mobility degradation as large as 40% occurs after NH_3 plasma treatment. This reduction is believed due to buildup of interface traps and generation of fixed charges, and therefore the increased Coulomb scattering by charged centers at the interface. The slow trapping on those interface states close to the band edge may also contribute to the degradation. Both the threshold voltage and field effect mobility variations indicate that NH_3 plasma treatment creats additional interface states.

3.4.5 Field-Induced Instability

As discussed previously, a continuous application of a positive gate voltage causes a threshold voltage shift and therefore the observed hysteresis in the I_D vs V_G characteristics. It is a measure of device quality, especially near the interface, and needs to be minimized for LCD applications. The clockwise direction of the hysteresis is consistent with increased negative charge in the gate insulator. This may be the result of a transfer of electrons from the a-Si:H channel into the $a-SiN_x:H$ during the positive part of the cycle, populating available states at or close to the a-Si:H/$a-SiN_x:H$ interface. These states remain filled for the duration of the measurement and thus screen the channel region of the device during the high to low swing of the gate voltage. Therefore, the amount of trapped charge, Q, near or at the $a-SiN_x:H$/a-Si:H interface may be estimated from the relation

$$Q = C_{ins} \delta V \tag{3.14}$$

Here, C_{ins} is the capacitance of the gate insulator and δV is the amount of hysteresis. For the present experiment, a delay time of 10 seconds was used after each voltage change and the entire transfer curve took about 14 minutes
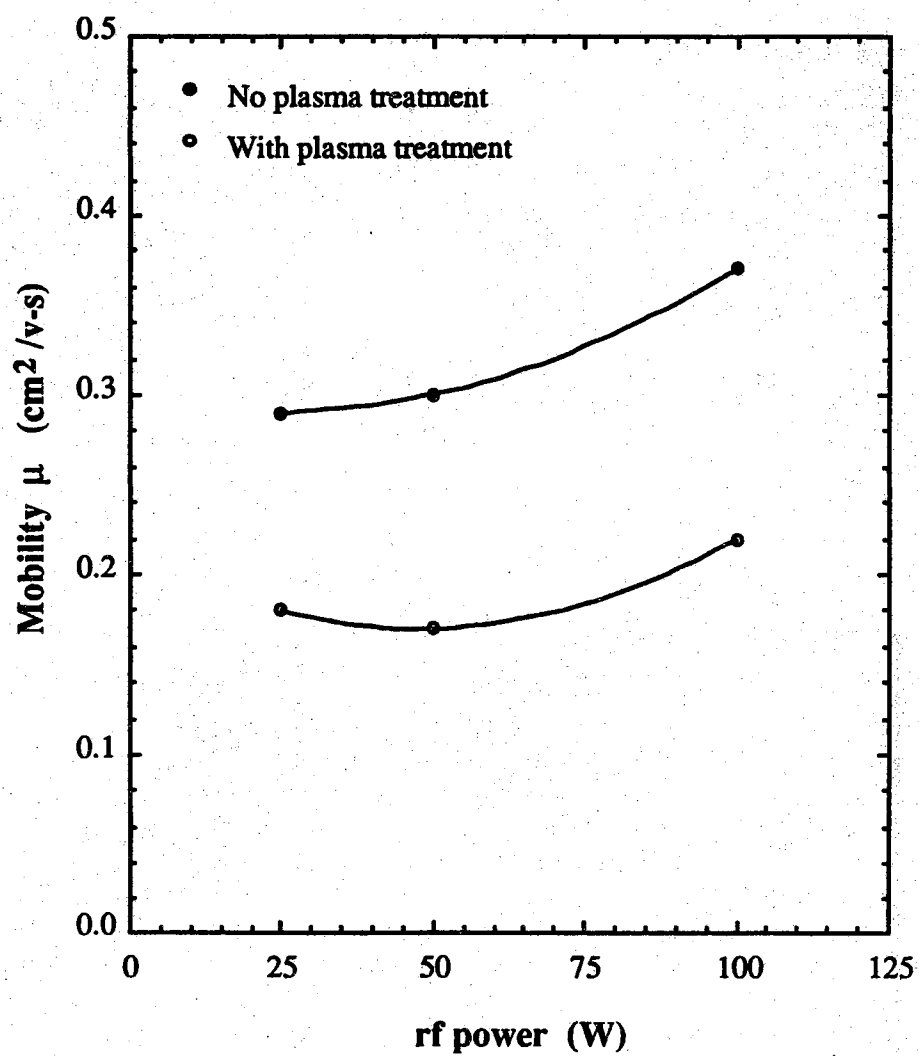
Figure 3.18   The field effect mobility as a function of rf power of gate nitride deposition and the influence of NH₃ plasma treatment.

to complete. This longer measurement time causes the electron trapping deeper into the gate nitride, kinetically allows the generation of metastable states in a-Si:H, and makes these effects more significant. Therefore, the width δV of I_D vs V_G hysteresis itself is a very convenient measure of device stability. For a gate voltage swing from -10 V to +10 V, all devices give a hysteresis δV of less than 0.7 V. Another interesting feature is that the NH_3 plasma treated devices exhibit at least a 25% reduction in the hysteresis width. As such, the average values are 0.4 V for gate nitride deposited at 25 W and 0.3 V for those deposited at 50 W and 100 W.

Another commonly employed method as a stability test is the bias-temperature stress (BTS). Here the BTS measurements were performed after the method used by Powell[127]. A gate voltage of 10 V was continuously applied and a constant temperature of 80 ° C was maintained. The source-drain current was then continuously recorded for 4×10^4 s at a drain voltage of 0.5 V. The low source-drain voltage is used to maintain a uniform field in the gate insulator layer. Transfer characteristics and threshold voltage were measured both before and after the BTS.

Figure 3.19 displays the transfer characteristics before (curve A) and after voltage stresses. It shows that the prolonged application of a positive gate voltage affects the characteristics in two different ways: 1) it shifts the flat-band voltage V_{FB}, which is approximately equal to the value of V_G at which I_D exceeds 10^{-12} A, by about 5.2 V (curve B); 2) it causes a increase of the subthreshold slope from 0.431 V/decade to 0.473 V/decade. Both effects contribute to the shift of the threshold voltage V_T from 1.65 V to 7.22 V as exhibited in in Figure 3.20. Prolonged application of a negative gate voltage for the same length of time reverses the shift of V_{FB} and V_T (curve C), which are -0.2 V and 2.51 V, respectively. A much longer stress time is needed to reverse the flat-band voltage to the original value of -1.55 V. It is important to note that negative gate voltage stress also increased the subthreshold slope from 0.473 V/decade to 0.599 V/decade. The increase of the subthreshold slope, or the flattening of the $I_D - V_G$ characteristics, reveals the additional states in the bulk of the a-Si:H film, or at the interface, are created. These additional states are metastable, and it has been suggested[156,157] that they are Si-dangling bonds, as in the case of photodegradation. In order to completely restore the initial state A, the specimen has to be annealed at temperatures near 200 ° C.

Figure 3.21 to Figure 3.23 give the time dependence of drain currents $I_D(t)$ normalized by the initial values of $I_D(1)$ for the three rf power values used. It can be seen that the rate of decay of $I_D(t)/I_D(1)$ is smaller for all the
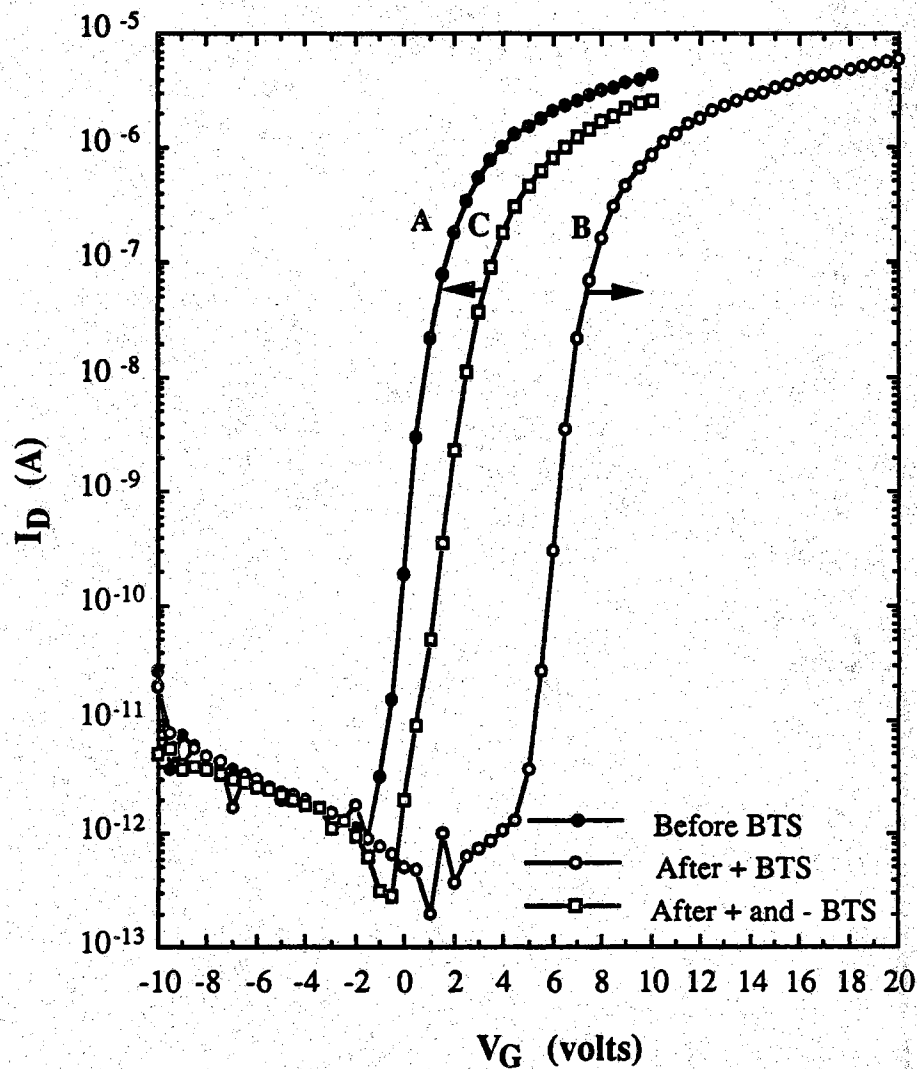
Figure 3.19 Room temperature transfer characteristics (V_D=2 V) both before and after bias-temperature stresses at T=80 °C, V_G=10 V, and V_{DS}=0.5 V. A: before stress; B: after 12 hours of positive gate stress; C: after 12 hours of positive and 12 hours of negative gate stresses.
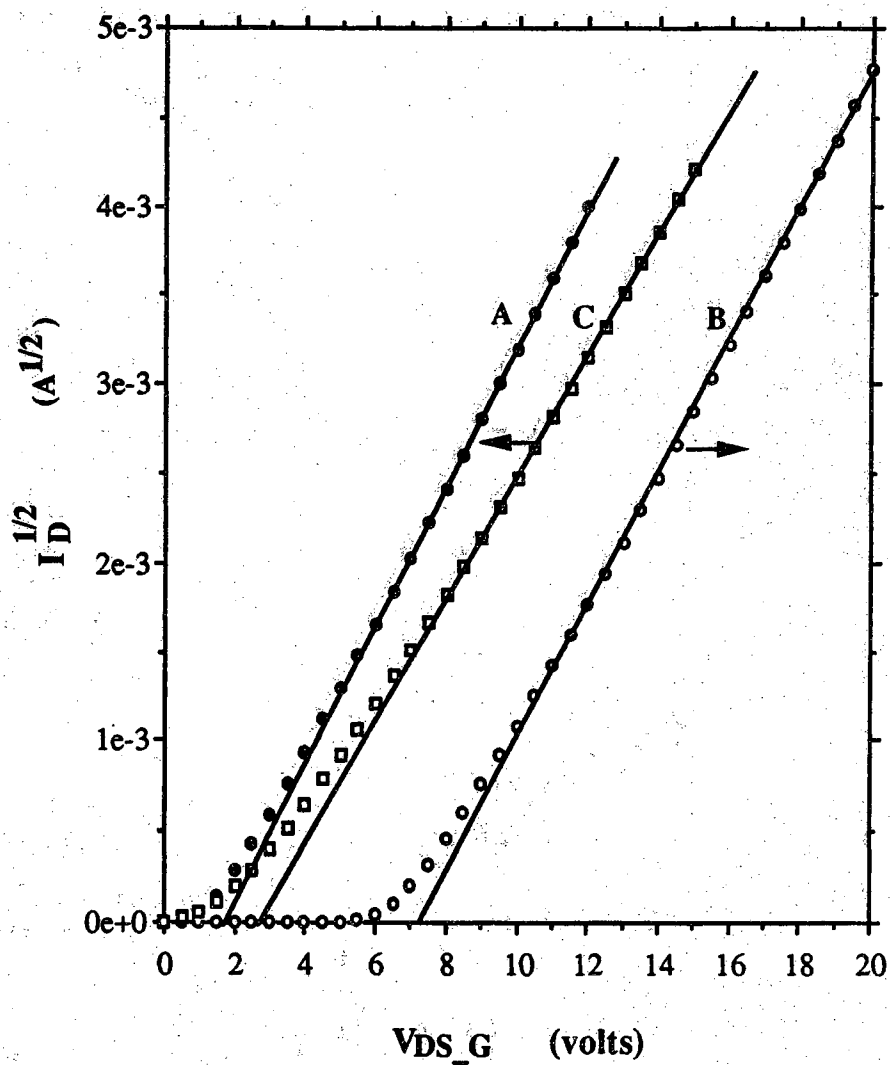
Figure 3.20   Saturation characteristics $I_D^{1/2}$ vs V_{DG_S} for the extraction of the field effect mobility and threshold voltage of a-Si:H TFTs before and after bias-temperature stress.
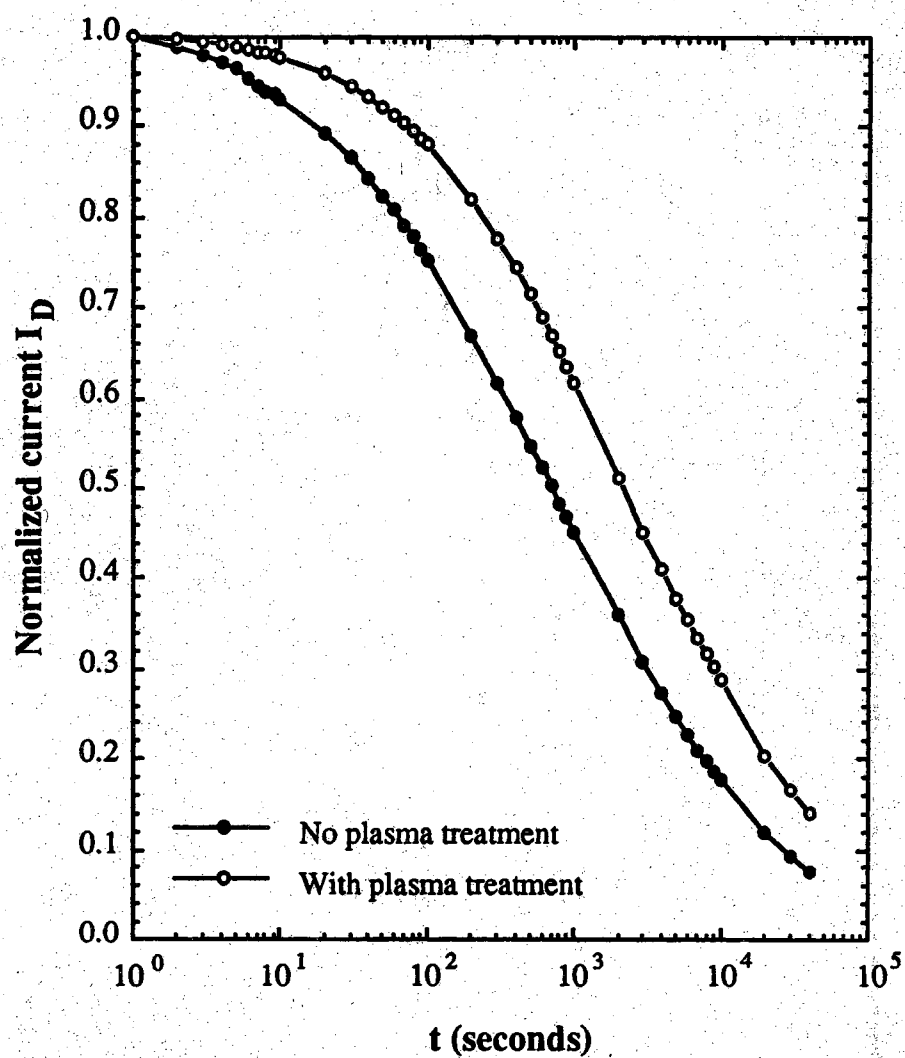
Figure 3.21 Normalized time dependence of the On-current of a-Si:H TFTs under a gate bias stress of 10 V. The gate nitride was deposited at a rf power of 50 W.
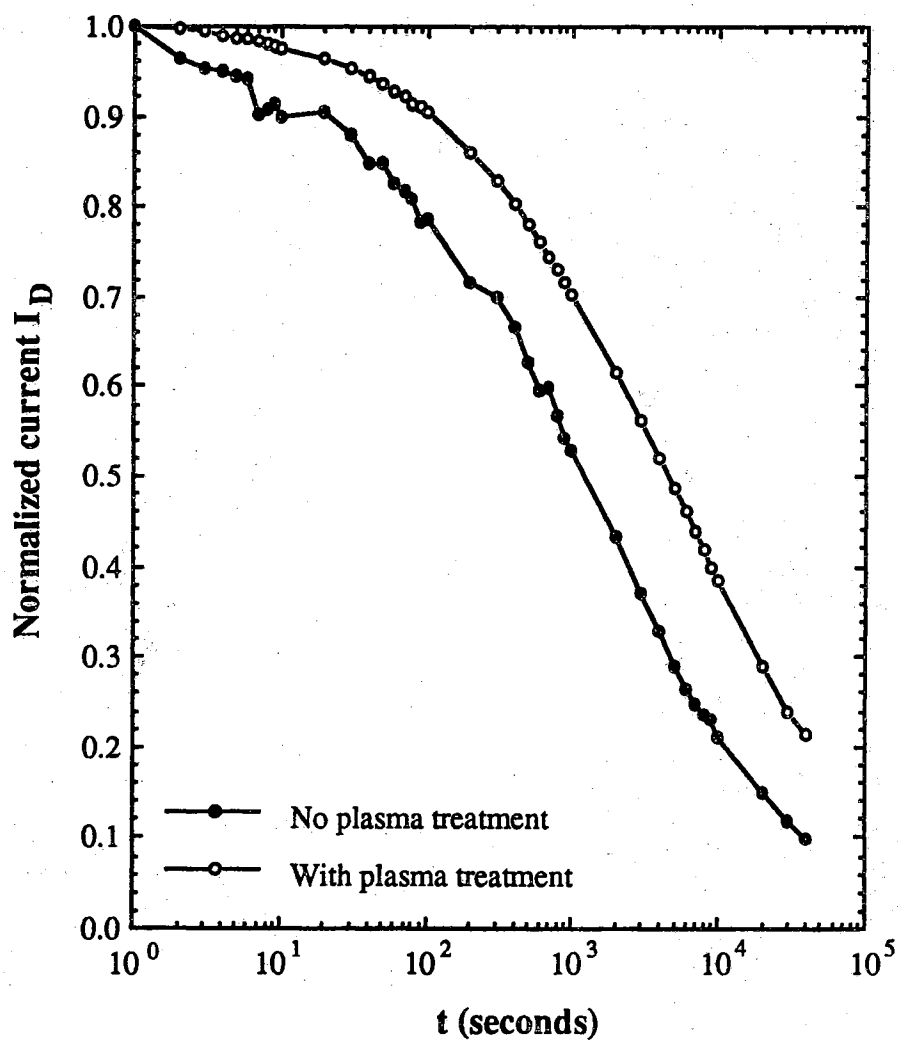
Figure 3.22   Normalized time dependence of the On-current of a-Si:H TFTs under a gate bias stress of 10 V. The gate nitride was deposited at a rf power of 25 W.
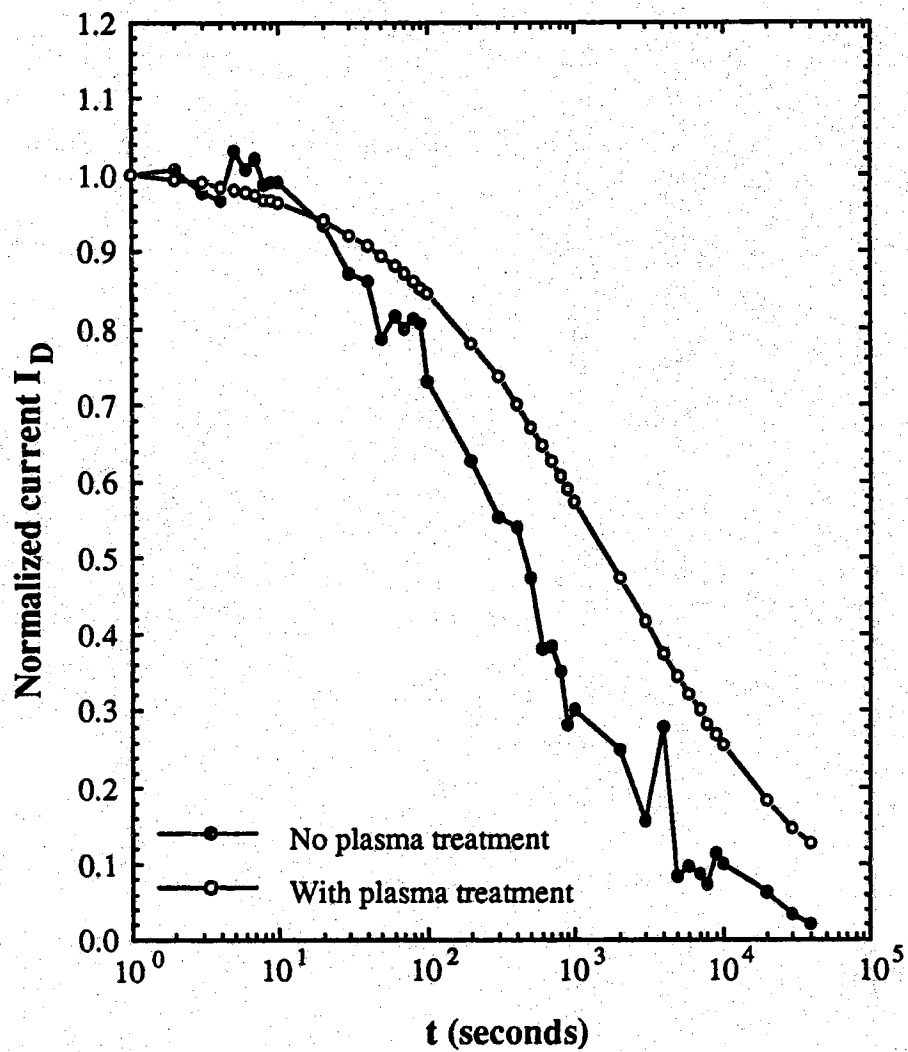
Figure 3.23 Normalized time dependence of the On-current of a-Si:H TFTs under a gate bias stress of 10 V. The gate nitride was deposited at a rf power of 100 W.

NH_3 plasma treated devices, especially for time less than 100 s. Figure 3.24 shows the absolute ON-current decay curves corresponding to Figure 3.22. Although the initial current is lower in the plasma treated device, the absolute final current is larger than the device without plasma treatment.

The time dependence of $I_D(t)/I_D(1)$ has been attributed to a shift of threshold voltage V_T[123] and a decrease of field-effect mobility. The threshold voltage shift is mainly due to charge trapping in slow states which are located in the $a-SiN_x{:}H$ near the interface and due to metastable states created in a-Si:H below the flat-band Fermi level. The relative contribution of these two mechanisms depends on bias stress voltage, temperature as well as the fabrication conditions of a-Si:H TFTs[104]. The decrease in field-effect mobility or the increase in subthreshold slope S is related to the generation of additional states above the flat-band Fermi level at or near the interface of a-Si:H. Both of these effects have been observed in the BTS experiments. The flat band voltage shift is as large as 6 V. The subthreshold slope increase is about 16% and the degradation of field effect mobility is less than 6%. These two degradation mechanisms are believed to be independent processes[158]. Since the a-Si:H layers for all devices were nominally deposited under the same condition, it can be assumed that contribution to the $I_D(t)/I_D(1)$ current decay from a-Si:H are the same. Further support for this view can be determined from Table 3.1 which lists the subthreshold slope and mobility ratios after and before BTS. These ratios are very close, within the errors of experiment and data analysis, for NH_3 treated and the corresponding untreated cases. Therefore, the difference in $I_D(t)/I_D(1)$ decay must come from the difference in SiN_x quality near the interface. It has been argued[82, 83] that silicon dangling bonds are responsible for charge trapping in $a-SiN_x{:}H$. The charge injection can occur by direct tunneling from states in a-Si:H into traps in $a-SiN_x{:}H$ and/or by Fowler-Nordheim tunneling into the nitride conduction band, followed by deep trapping[123]. Therefore, N-rich nitride should be more resistant to electron injection because it has less silicon dangling bonds (traps)[159] and because its larger band gap and hence the corresponding energy barrier for electron injection. Recently, charge injection measurements on $Al/SiN_x/$c-Si capacitors further confirmed that N-rich nitride had lower charging rate[93]. From the above arguments and results of previous sections, it is justified to postulate that the NH_3 plasma treatment resulted in nitriding reaction or amination and the resulting gate insulator is less susceptible to field-induced threshold voltage shift.
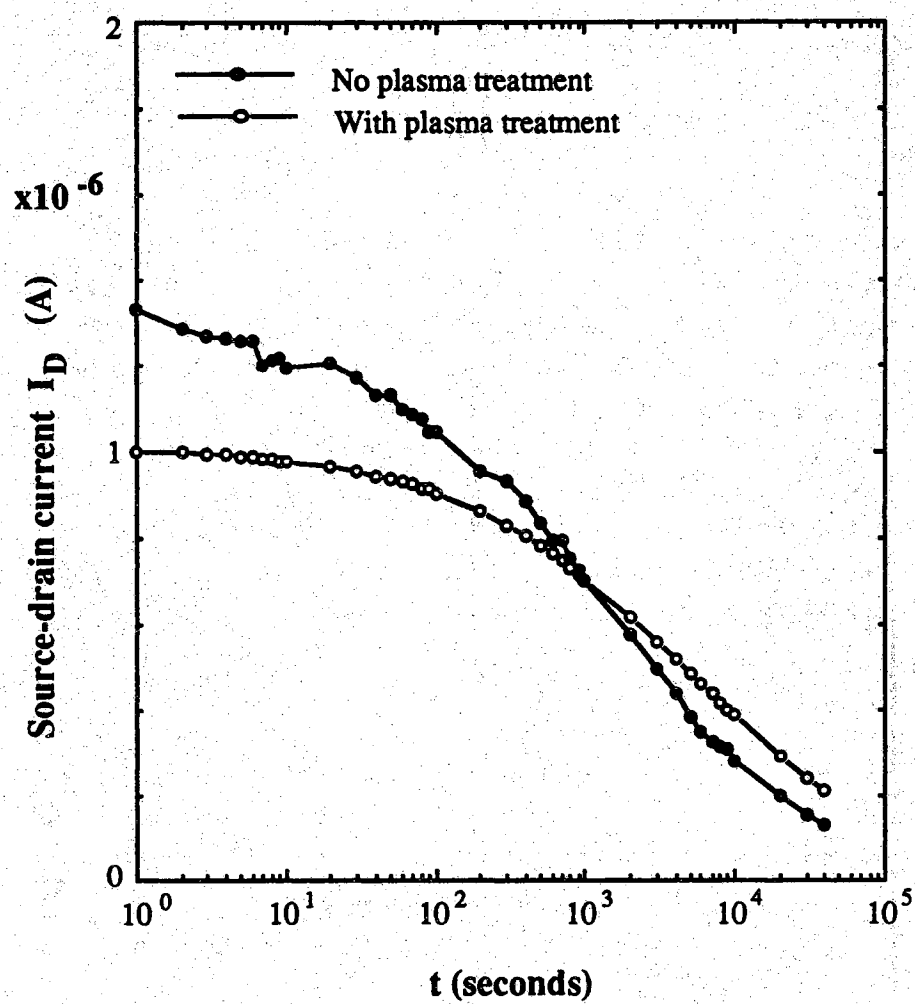
Figure 3.24   Absolute ON-current decay corresponding to Figure 3.22.

Table 3.1 Subthreshold slope and mobility ratios after and before BTS.

Ratio	NH$_3$ plasma	rf power of nitride deposition		
		25 W	50 W	100 W
$\dfrac{S_{after}}{S_{before}}$	no	1.13	1.16	-
	yes	1.16	1.18	1.16
$\dfrac{\mu_{after}}{\mu_{before}}$	no	0.95	0.94	0.86
	yes	0.97	0.95	0.98

The observations in this section demonstrate that NH_3 plasma treatment is beneficial as far as device stability is concerned. However, the true plasma-surface reaction is still open for examination. Further spectroscopic analysis should shed light on the elemental composition of the nitride surface and resolve the interaction mechanism. As for the application side, in view of the single plasma conditions used in the present experiment, studies on the plasma treatment with respect to rf power, gas flow, pressure and temperature may improve the stability enhancement without inducing much degradation in mobility.

3.4.6 Conclusion

The electrical characteristics of a-Si:H TFTs were studied for different deposition conditions of gate nitride and for the effect of NH_3 plasma treatment. In general, devices with gate nitride deposited at higher rf power give larger field effect mobilities, lower subthreshold slope and threshold voltage. Under the particular conditions used, it is found that NH_3 plasma treatment causes a general increase in subthreshold slope and threshold voltage. Field effect mobility degradation was also observed. However, the positive effect is that the NH_3 plasma treated devices exhibit higher stability as exhibited by smaller hysteresis of transfer characteristics and by higher resistance against prolonged positive gate field application. An exact model of the plasma interaction with the a-SiN_x:H surface could not be developed only on the basis of the present electrical measurements without a spectroscopic analysis. However, it is suggested that both radiation damage and nitridation/amination can occur. In view of the single plasma conditions used for the surface treatment of gate nitride, it may be possible to manipulate the near-interface nitrogen content of the gate nitride by adjusting macroscopic plasma parameters without noticeable radiation damage.

CHAPTER 4
STAGGERED a-Si:H TFTs AND FAILURE MECHANISMS

4.1 Introduction

Much research effort on a-Si:H TFTs has been focused on the conventional inverted-staggered structure because of its higher materials and interface quality. However, the complementary structure, normal staggered, has its own merits. First, it is easier to make connection between the source electrode and the pixel electrode. Second, the gate bus-line can be made sufficiently thick, resulting in small bus-line resistance. Third, it is possible to fully integrate a-Si:H TFT switching elements and poly Si TFT driver circuits on the same substrate by using excimer laser annealing technology[160]. In addition, the TFT itself is a good structure to study the top insulator quality. Because a passivation layer (usually a—SiN_x:H) is often indispensable for the inverted-staggered structure, its interface with a-Si:H over the active channel region is paramount in affecting the leakage current. Therefore, to fully take advantage of this structure, much progress is needed to understand and improve the a-Si:H/a—SiN_x:H interface.

A set of three masks and the fabrication process have been developed to fabricate this a-Si:H TFT structure and to study the relationship between process and device characteristics. During the course of this effort, however, a new device failure mechanism was found due to a pure solid state electrochemical corrosion of the gate Cr. This was also believed to be responsible for the previously observed device failures in the inverted-staggered structure. This chapter first details the device design and fabrication processes of the normal staggered a-Si:H TFTs. The remaining part will be devoted entirely to the analysis and remedy of this failure mechanism.

4.2 Staggered a-Si:H TFT Structures and Processing

A three dimensional view of the normal-staggered a-Si:H TFT structure is shown in Figure 4.1. It uses chromium for both source/drain and gate metalization, and incorporates a phosphorus implanted n^+ layer to reduce the contact resistance. As in the inverted-staggered case, the starting substrate is also a thermally oxidized Si wafer. However, because the a-Si:H back surface is in direct contact with the thermal oxide in this structure, a very careful pre-clean procedure is necessary to prevent a large off-state leakage current. For freshly oxidized substrates, no additional cleaning was performed. Otherwise, wafers were cleaned by using the all-purpose "RCA clean" procedure with the help of ultrasonic agitation.

The major steps of the process are sketched in Figure 4.2. Because the process technologies of each step were already detailed in Chapter 3, only a brief process flow is given as follows. On a thermally oxidized wafer, a sputter-deposited Cr ($\sim$800 Å) was first patterned to form the source and drain contacts. The wafer was then transferred into a TECHNICS PECVD system. After a 5 min H_2 plasma clean, two layers, a-Si:H and a$-$SiH$_x$:H with nominal thickness of 500 Å and 1500 Å, were then deposited consecutively in a single pumpdown at a temperature of 260 $^\circ$C. Conditions for a-Si:H deposition were the same as those for inverted-staggered TFTs. For a$-$SiN$_x$:H, the rf power used was 100 W and the N$_2$/NH$_3$/SiH$_4$ flow ratio was 50/50/5 in sccm. Next, a 1500 Å Cr film was deposited and patterned as the top gate. For devices with ion implanted source/drain regions, the a$-$SiN$_x$:H was then wet etched (in BHF for $\sim$5 min) using gate Cr patterns as the mask. This follows the patterning of a-Si:H film over the source and drain region by using CF$_4$ plasma etching (100 s). The device was completed by a blanket phosphorus implantation and a final thermal anneal at a temperature of 200 $^\circ$C.

4.3 Characteristics of Staggered a-Si:H TFTs

Probe-level tests were performed in the way as described in Chapter 3. Devices were unpassivated but under a constant dry N$_2$ flow during the entire measurement. Unfortunately, all devices died during the initial transfer characteristic measurements. In a humid atmosphere, the gate Cr was destroyed very quickly, as soon as the gate voltage exceeds about +6 V starting from -20 V. Observing under the probe station microscope, the corrosion products appeared to be a gel with gas evolution. Figure 4.3 shows a micrograph of a typical failed a-Si TFT due to this reaction.
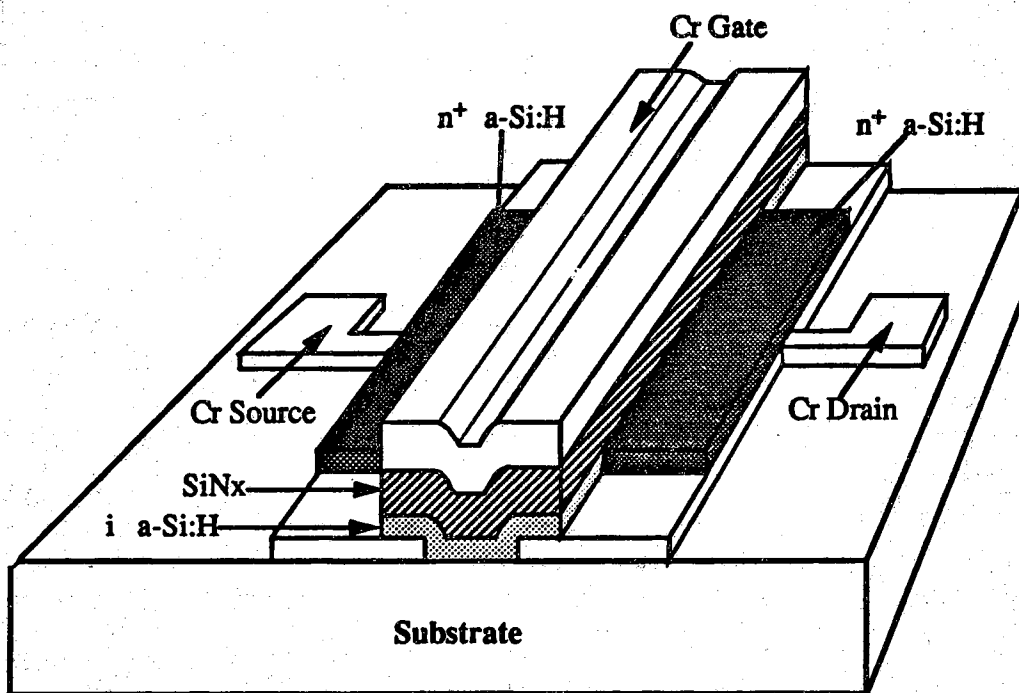
Figure 4.1 A three-dimensional view of a normal staggered a-Si:H TFT structure.
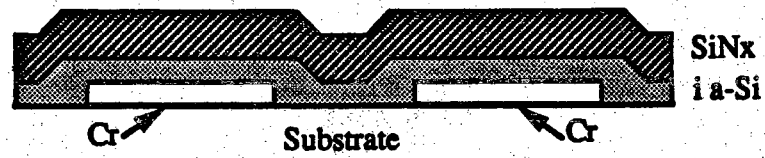
(1) Define source/drain contact Cr and deposit a-Si/SiNx
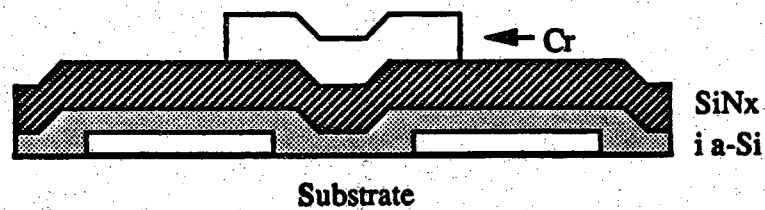
(2) Define Cr gate pattern
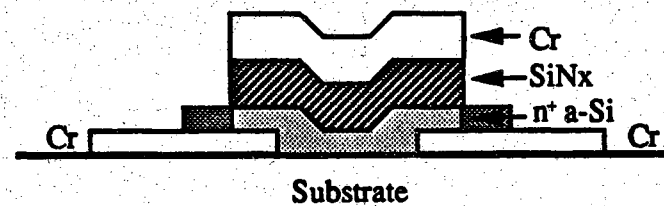
(3) Final structure after etching SiNx/a-Si using BHF/CF$_4$

plasma and phospherus ion implantation.

Figure 4.2   Normal staggered a-Si:H TFT process flow.
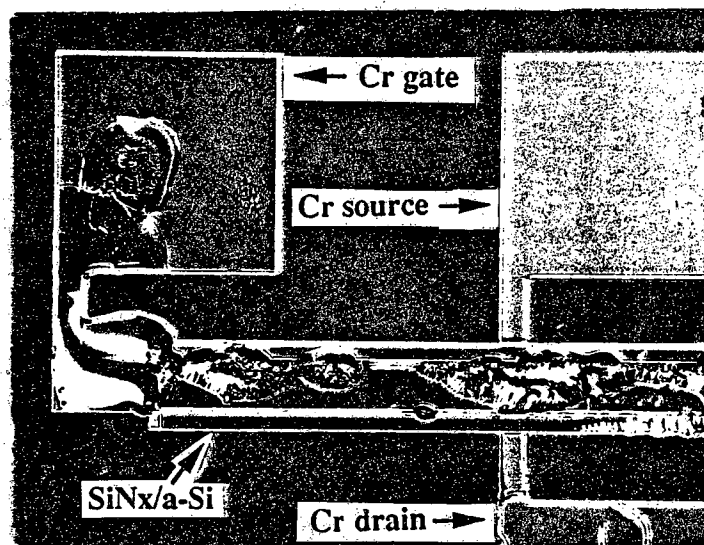
Figure 4.3   Photograph of a corroded normal-staggered TFT device.

The Cr reaction is electrochemical in nature because it can only be initiated under an electric field and the polarity of the field is crucial. The gate Cr corrodes only when it is at the positive probe in relation to either source or drain metal contact.

To understand the necessary conditions of the Cr reaction and therefore prevent it from occurring, a series of experiments were conducted. It was observed that the Cr reaction is much slower if dry N_2 is blown over the wafer surface while under electrical measurement. This led to the speculation that either water content or O_2 in the air may play an important role in the reaction. To further verify this assumption, two approachs were adopted. First, devices were packaged and tested in a low humidity desiccator. The pump-down and N_2 back-fill cycle was repeated at least three times and devices were conditioned under this environment for 1 hr before each test. Second, a passivation PECVD SiN_x of 2000 Å thick was deposited over the whole wafer and holes were opened only at those areas with probe pads which are least 200 μm apart. It was indeed found that the Cr reaction entirely disappeared. However, it was not clear whether the reaction is between Cr and O_2/H_2O only or Cr, SiN_x and O_2/H_2O. An indirect experiment excluded the possibility of Cr reaction with SiN_x. A layer of Al-Si with a thickness about 1000 Å was deposited in between SiN_x and Cr, and under the otherwise same processing conditions, the Cr reaction occurred in the same manner.

Figure 4.4 and Figure 4.5 illustrate the transfer and output characteristics of a passivated, normal staggered a-Si:H TFT without source/drain ion implantation. With the understanding of a large contact resistance, it is very reasonable to observe a current ON/OFF ratio of 10^6 for a gate voltage swing from 0 to 20 V. Although a considerably improved characteristic was expected when ion implanted S/D is employed, this was not pursued further. Instead, the analysis of the failure mechanism appeared to be more important and interesting.

4.4 Electrochemical Corrosion of Gate Cr

4.4.1 Introduction

In last section, the failure of normal staggered a-Si:H TFTs was observed while under electrical testing. Clearly, the destroying of the Cr gate metalization was the sole cause. It was latter found that the Cr reaction was also responsible for the failure of some of the inverted-staggered a-Si TFTs. The corrosion appearance in this structure is shown in Figure 4.6. However, the
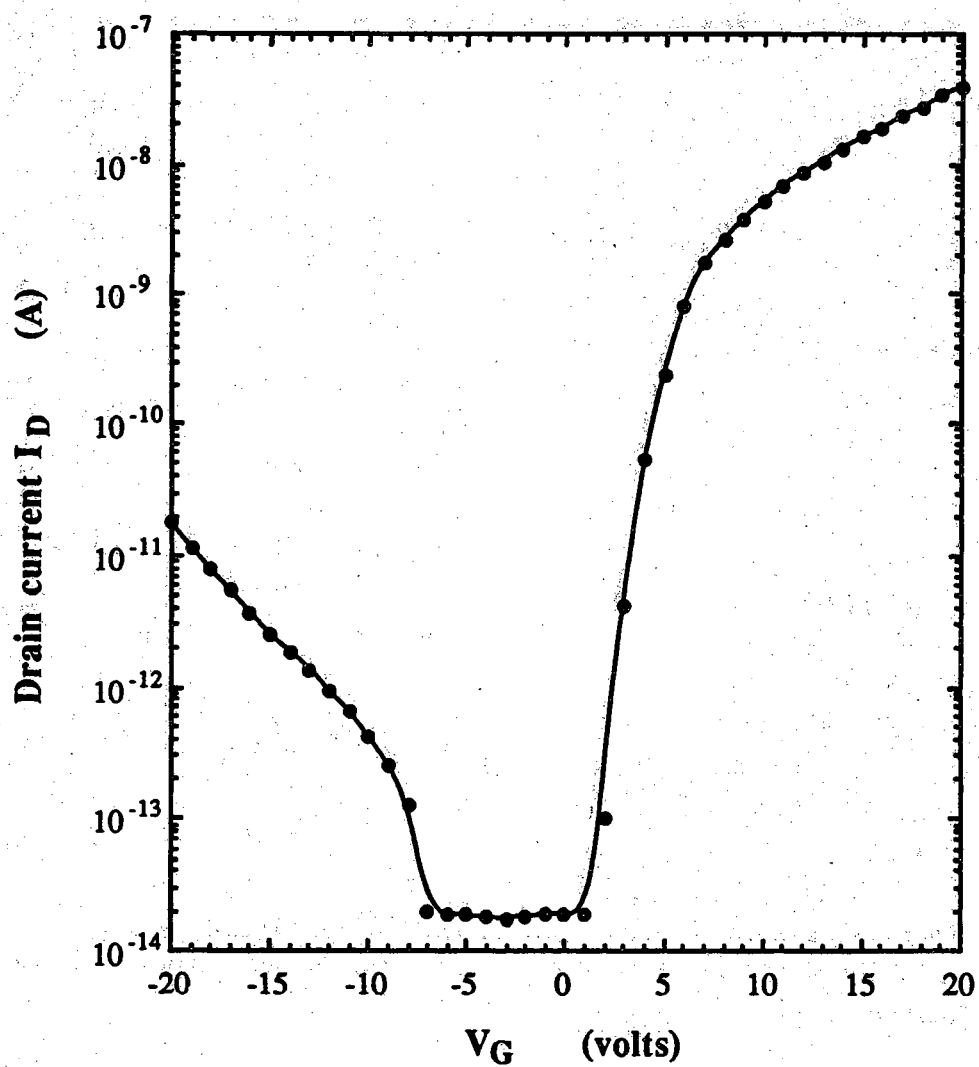
Figure 4.4   Transfer characteristics of a passivated, normal staggered a-Si:H
TFT without source/drain implant. $V_D = 2$ V and W/L=10.
Device TNT05-47.
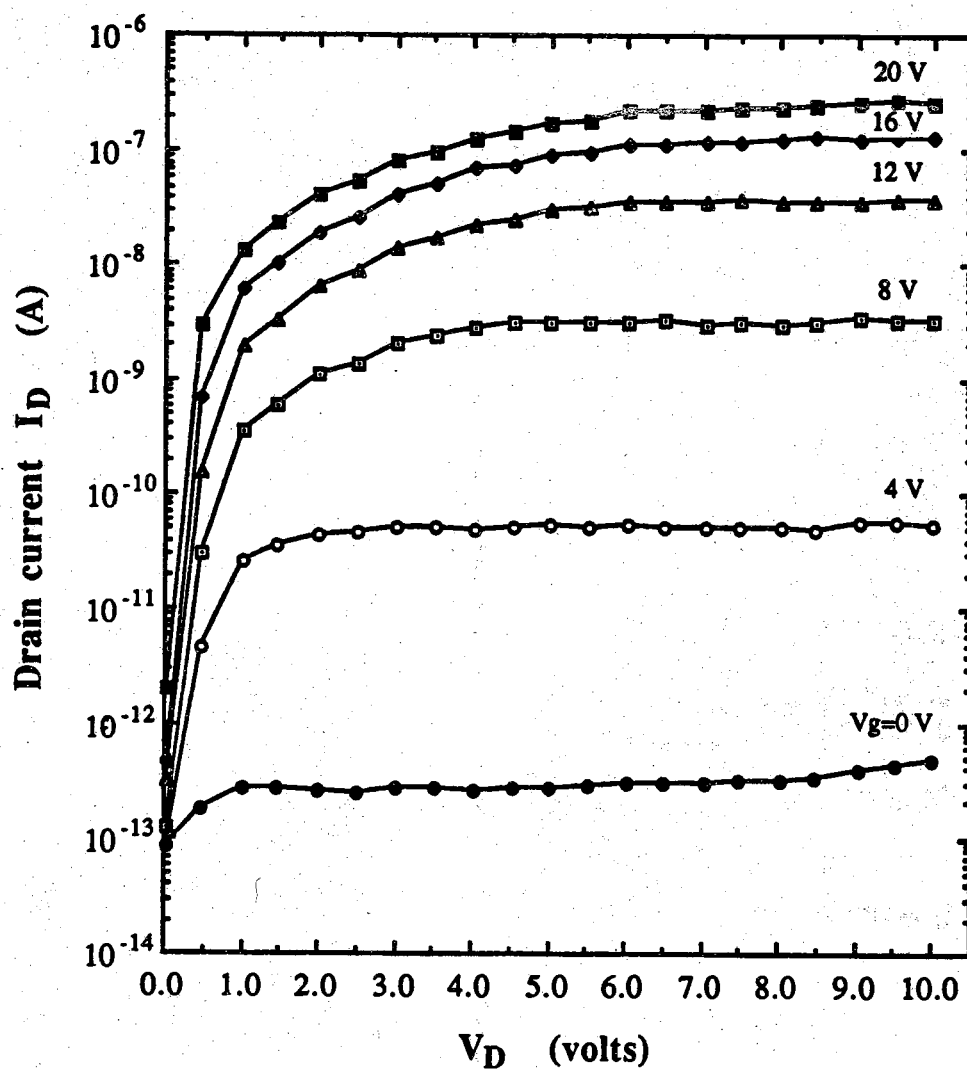
Figure 4.5   Output characteristics of a passivated, normal staggered a-Si:H TFT without source/drain implant. $V_D=2$ V and W/L=10. Device TNT05-47.
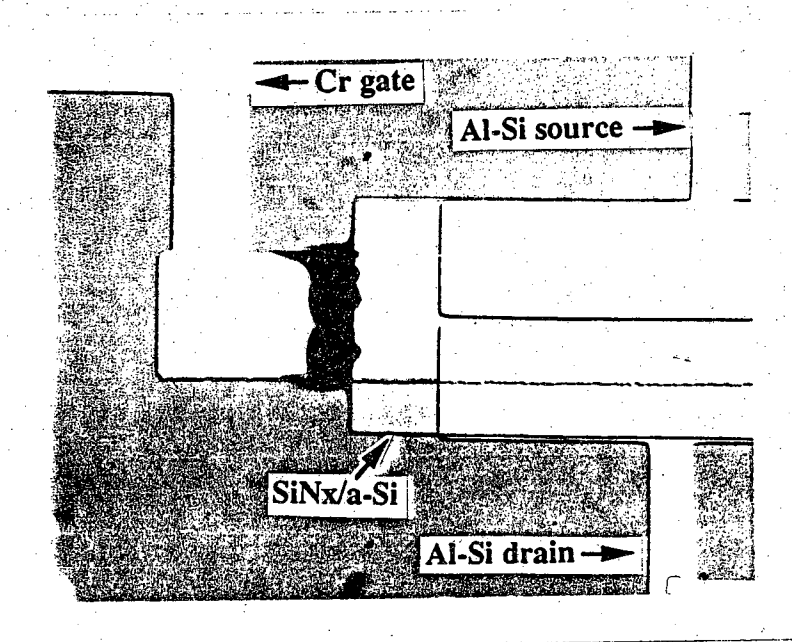
Figure 4.6   Photograph of a corroded inverted-staggered TFT device.

devices were destroyed only after a long time storage in the atmosphere and a sequence of different electrical tests in an undefined environment which can have a relative humidity between 35% and 80%. For intact devices, there was no corrosion, in at least a year for the latter case. Therefore, the study of the corrosion mechanism is of interest both for a fundamental understanding and for device reliability concerns.

Without any solid proof though, CF_4 plasma etching residuals on Cr surface was first suspected to cause the corrosion. For both inverted-staggered and normal staggered a-Si:H TFT configurations, CF_4 plasma was used to pattern a-Si:H and a$-SiN_x$:H. In the normal course of fabrication, the gate Cr was exposed to the CF_4 plasma either due to over-etching of a-Si:H/a$-SiN_x$:H or purposefully used as an etching mask in some areas. Although the chromium film does not etch in the sense that the etching products are not volatile, its surface can be altered leading to potential problems such as corrosion. Extensive literature can be found on the surface modification of Si and Al-Si[161-164]. It has been reported that chlorine contamination during Al-Si etching can be very detrimental to the metalization layer, since small amounts of chlorine ions can cause considerable corrosion.

The interaction of chromium surface with plasma generated F-containing radicals has not been documented extensively. In particular, to the author's knowledge, chromium corrosion in the semiconductor devices due to tetrofluorocarbon plasma exposure has not been reported. The following sections details the electrochemical corrosion behavior of chromium in specially designed capacitor structures. The effect of CF_4 plasma exposure and various post-etch treatments are presented and analyzed. X-ray photoelectron spectroscopy (XPS) and Auger electron spectroscopy (AES) were used for surface analysis and corrosion product identification. Experimental results are used to describe the possible corrosion mechanisms involved.

4.4.2 Experimental Structures and Characterization Methods

A common feature, as is relevant in this study, of the two different TFT structures is shown in Figure 4.7. In inverted staggered TFTs, the minimum dimension d, which will be called d_{passi} hereafter, is 25 μm and only the bottom Cr is possibly exposed to CF_4 plasma due to over etching. For normal staggered TFTs, d minimum is approximately zero and the CF_4 plasma exposure time is 100 s at the same area. The two Cr films (or Cr and Al-Si films) are separated by a-Si:H and a$-SiN_x$:H layers. From an electrochemical point of view, this structure should be equivalent to a $Cr/SiN_x/Cr$ capacitor.

Therefore, further corrosion studies were performed on these capacitors fabricated using the mask set as described in Chapter 3.
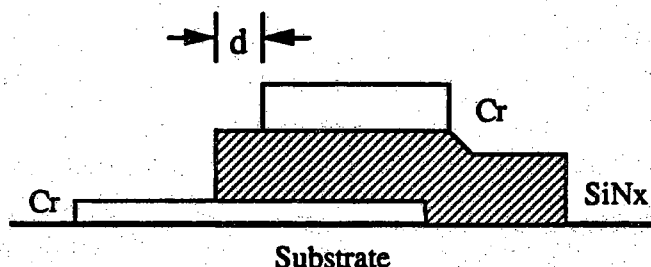
Figure 4.7   A common feature in the two TFT configurations that is of interest.

Electrical characterization of and comparative studies on Cr corrosion in $Cr/SiN_x/Cr$ structures were made in the same way as for TFT characterization. All devices were tested under a relative humidity between 44% and 46% in the laboratory atmosphere without N_2 blowing over the wafer surface.

Electron spectroscopy techniques, SEM and TEM together with electron energy loss spectroscopy (EELS) were utilized for surface analysis and corrosion product identification. The x-ray photoelectron spectroscopy (XPS) were obtained by using a Perkin-Elmer PHI 5300 spectrometer whose Mg(1253.6 eV)/Al (1486.6 eV) dual anode x-ray source was operated at 15 KV and 300 or 400 W, respectively. Background pressure in the analysis chamber was always less than 1×10^{-9} Torr. The binding energies were obtained by assuming that the C 1s band of hydrocarbon contaminants appears at a binding energy of 285.0 eV.

In all cases, all the specimens were sputter-deposited Cr. Because the XPS instrument can not probe a sample smaller than about 1.5 cm^2, the Cr film was patterned into large squares (1 cm by 1.5 cm) on Si wafers in the case of

studying the effects of the CF_4 plasma. For corrosion product studies, the samples were in the form of $Cr/SiN_x/Cr$, which were corroded on purpose by applying a voltage across the capacitor with the top Cr positive. The final surface is such that no Cr island is left as seen under an optical microscope. This turned out to be very difficult for a capacitor size of 1 cm by 1.5 cm because the top electrode was isolated once the periphery was first corroded. Therefore, the specially designed capacitor had 52 probe pads along the periphery for each Cr electrode. Even with this structure, it still took several hours to corrode the complete top Cr film electrochemically.

To further confirm the corrosion products and observe the SiN_x behavior after Cr corrosion, a cross-sectional TEM was also used to observe the layered structures. Auger spectra were taken initially and after 30 minutes of Argon sputtering to check the composition deeper into the corrosion products,

4.4.3 Experimental Results

4.4.3.1 The Effect of CF_4 Plasma Treatment

While pure Cr is quite an active metal with a redox potential of -0.74 V, it becomes passive not only under the influence of oxidizing agents but also of dissolved oxygen; that is, it spontaneously passivates in atmosphere[165]. Therefore, Cr corrosion must be induced by the subsequent processing steps after Cr film patterning. The most probable step is the CF_4 plasma etching of a-Si/SiN_x. It is already known that postetch corrosion of Al metalization is due to high level chlorine containing residuals which are deposited on metal sidewalls during plasma etching. If CF_4 plasma exposure is indeed the decisive factor, then it would explain why Cr gate corrosion is much severe in the normal staggered structure than that in the inverted-staggered structure. In the first configuration, regions of the Cr gate are exposed to CF_4 plasma in the whole etching process while in the latter configuration only parts of the Cr gate are exposed during the overetch period, which might be shorter.

To simplify the test structure and the fabrication process, it was noticed that a common feature of interest in the TFT structures is that of a stacked capacitor with different lengths of passivation SiN_x d_{passi} as illustrated in Figure 4.7. Special $Cr/SiN_x/Cr$ capacitors were as shown in Figure 4.8 fabricated and processed differently to test the effect of CF_4 plasma etching. Figure 4.8(a) shows the top and cross-sectional view of the initial test structure. The top and bottom Cr electrodes have the same size and the SiN_x over-runs the Cr by 25 μm. During its fabrication, photoresist was used as
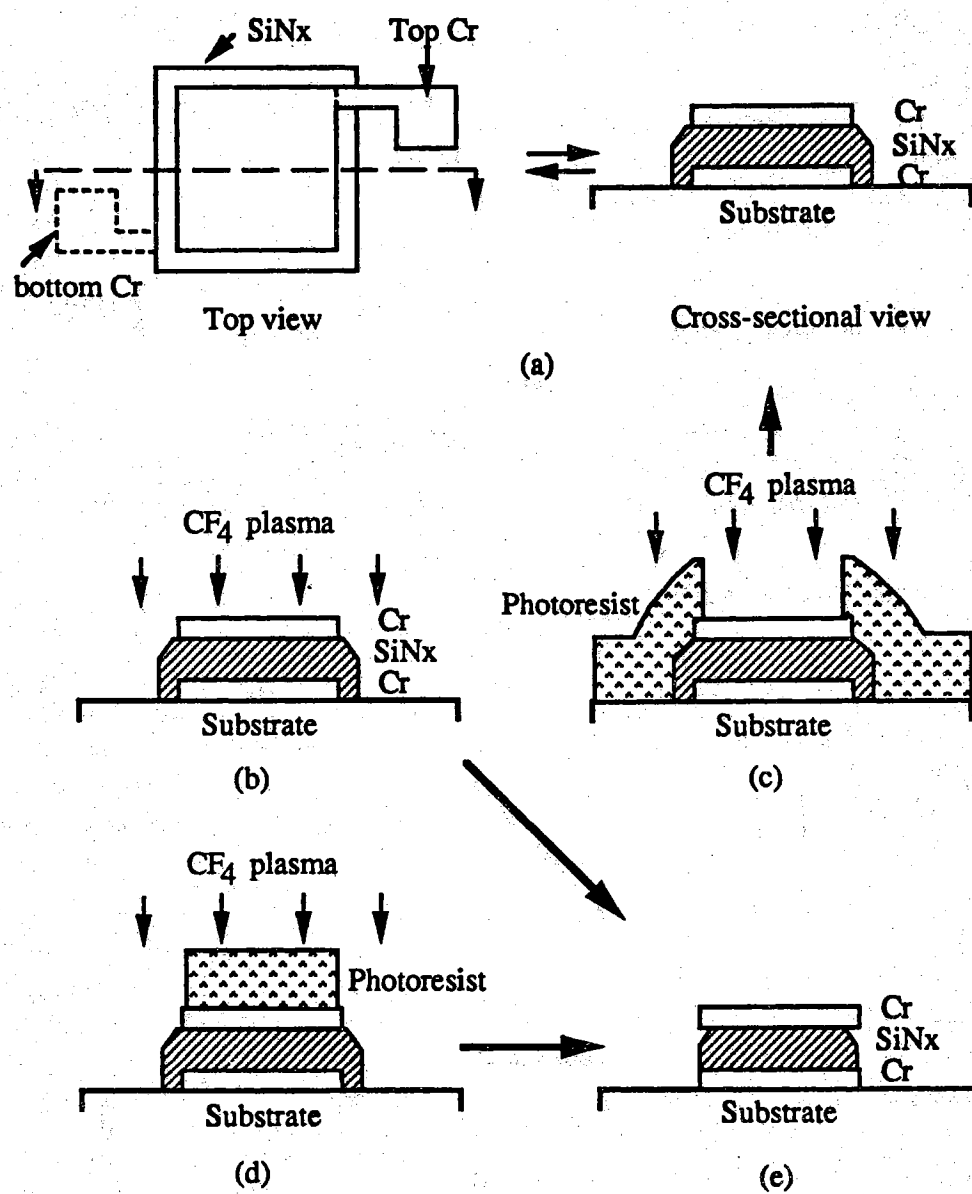
Figure 4.8   Differently processed structures of $Cr/SiN_x/Cr$.

mask so that Cr films were not exposed to CF_4 plasma. All capacitors of different sizes ranging from 100 by 100 μm to 1000 by 1000 μm had a very low leakage current and can sustain a voltage as high as 100 V without Cr corrosion. However, top Cr electrodes corroded very quickly for the structure of Figure 4.8(e) which was obtained by a flooding etch of structure (a) using CF_4 plasma (4 minutes), as is illustrated in Figure 4.8(b). Polarity requirements are the same as for TFT structures, i.e., Cr corrodes only when the top Cr electrode is at a positive potential. Corrosion was initiated along the periphery as well as in the inner area with the forming of many pits. The immediate corrosion product had a gel appearance and the front grows quickly over the entire area. It stops only when the probe pad connection is destroyed. The corrosion threshold voltage V_{corr} is about 5.6 V. However, It should be mentioned that V_{corr} does not have a well defined value and it depends on how long a voltage is held.

To verify the electrochemical nature of the corrosion, the devices were each immersed in deionized water and a fixed dc voltage of 6 volts was applied with top Cr at positive. For the structure of Figure 4.8(a), gas bubbles evolved from the cathode pad. Voltage was interrupted and water was removed to see the corrosion feature. Half of the top Cr film was missing near the cathode probe side and the exposed SiN_x has the original color. With the structure as processed in Figure 4.8(b), the differences were that the reaction was much more violent and only a small Cr island was left near the center after interruption.

Two major factors may cause the Cr corrosion in the flooding-etched structure. They are (1) fully air-exposed bottom Cr and (2) plasma etching of top Cr surface. To see which one is more important, capacitors were further processed. In process of Figure 4.8(c), only the top Cr surface is exposed to CF_4 for 1 min, 2 min, 4 min, 6 min and 8 min duration while without etching away the periphery SiN_x. For those samples with an etching time less than 8 min, it was found that there was no Cr corrosion during a voltage sweep from 0 to 20 V. With 8 min etching, one or two corrosion pits may appear but usually do not grow over large area. In the process of Figure 4.8(d), the periphery SiN_x was etched away with the top Cr surface masked by photoresist (about 5 μm Cr along the edge is exposed). Nine out of ten tested devices did not show any corrosion. The one corroded had a size of 1000 by 1000 μm and the corrosion was limited to a small area at the edge. However, leakage current is more than one order of magnitude larger even for devices without corrosion. Figure 4.9 shows the DC IV characteristics of the capacitors corresponding to the original
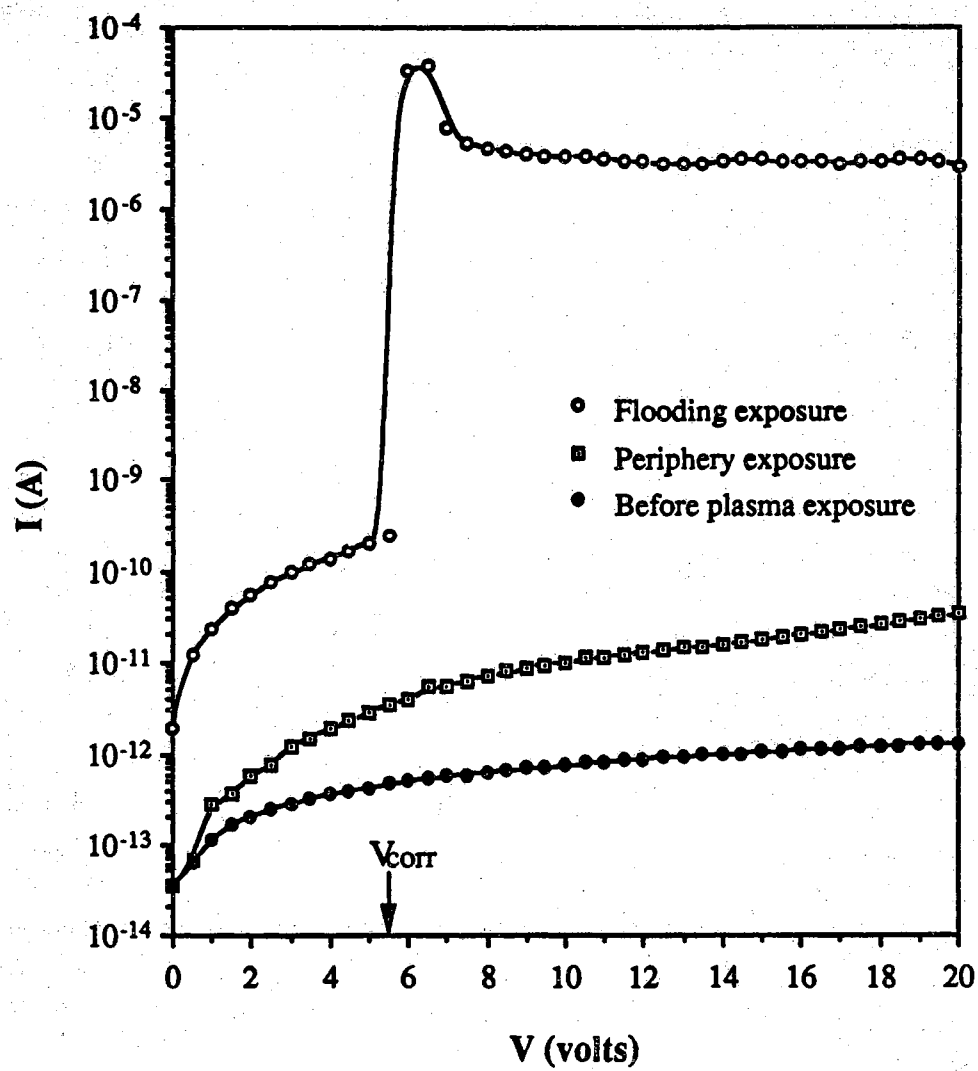
Figure 4.9   I-V characteristics of Cr/SiN$_x$/Cr capacitors with or without corrosion.

structure of Figure 4.8(a), flooding-etched of Figure 4.8(b) and peripheral etching of Figure 4.8(d). They all have a dimension of 500 by 500 μm. The leakage current of Figure 4.8(c) is almost the same as Figure 4.8(a) for 4 min etching and it is not included.

4.4.3.2 Surface Analysis by XPS

From previous sections, it is evident that CF_4 plasma treatment of the Cr surface induced the electrochemical corrosion. However, it was still not known what the real consequence of the plasma-surface interaction was in terms of the surface chemistry. Plasma-surface interactions are a very complicated issue. A variety of phenomena can occur such as surface film deposition and etching, sputtering, ion implantation, enhanced physicochemical adsorption and collision induced surface reconstruction. The complex interplay of these factors makes it extremely difficult, if not impossible, to predict reactions that can take place. Therefore, surface analysis tools such as XPS become indispensable.

Sputter-deposited Cr films were examined with XPS before and after CF_4 plasma exposure and are shown in Figures 4.10 and 4.11. Prior to plasma exposure, the surface is covered with native chromium oxide. This is typical of the surface of air-oxidized Cr samples. The XPS signal contains a metal and a Cr oxide part with an average chemical shift of 2.3 eV as shown in Figure 4.12. The main Cr 2p peak positions for oxide and metal are at 576.5 eV and 574.0 eV with a spin-orbit splittings of 9.8 eV and 9.3 eV, respectively. The O 1s signal shows a peak at 530.5 eV, which should be correlated to an O^{2-} species. These are consistent with reported values and hence the native oxide can be considered as Cr_2O_3.

Following plasma treatment of the Cr film with pure CF_4, the surface composition changes. Here the dominant peak observed is the fluorine peak. Oxygen is also observed but with a much smaller content. In Figure 4.13, the Cr 2p peak is at 580 eV with a spin-orbit splitting of 10 eV. Table 4.1 lists the binding energies of some O- and F-containing chromium compounds that are likely to occur in the course of this study. In comparing with binding energies and spin-orbit splittings in this table, it is evident that most of the surface Cr is present in the form of CrF_3. A further look at the expanded Cr 2p region indicates that more than one type of environment may exist since two different Cr $2p_{3/2}$ signals can be resolved at 580.0 eV and 577.2 eV, respectively. The modified surface can therefore be considered to have the composition of a mixture of CrF_3 and Cr_2O_3. However, chromium is mostly in the fluorinated state. A rough least-square curve fit indicates that the Cr surface has more
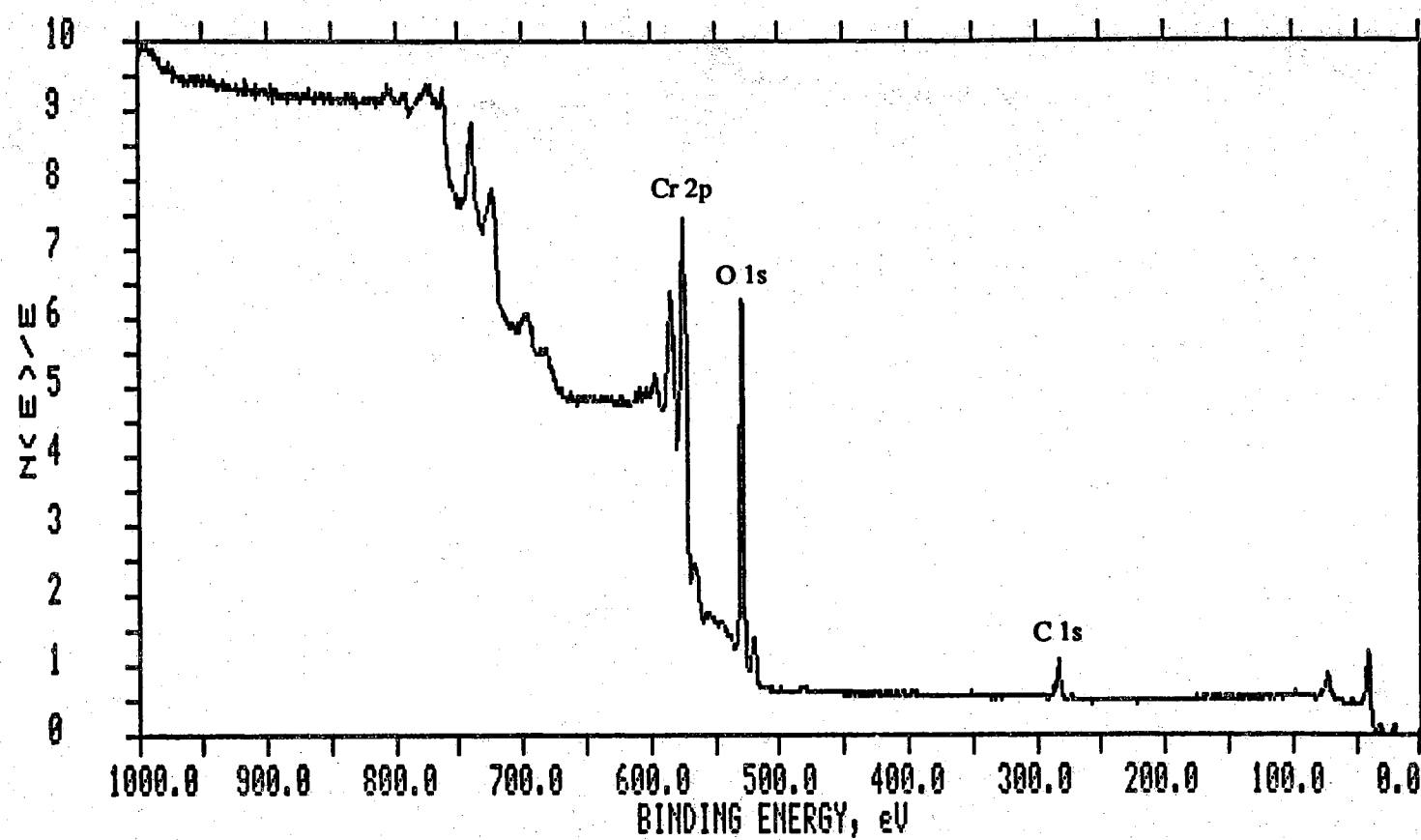
Figure 4.10 XPS survey spectrum of Cr surface before CF_4 plasma exposure.
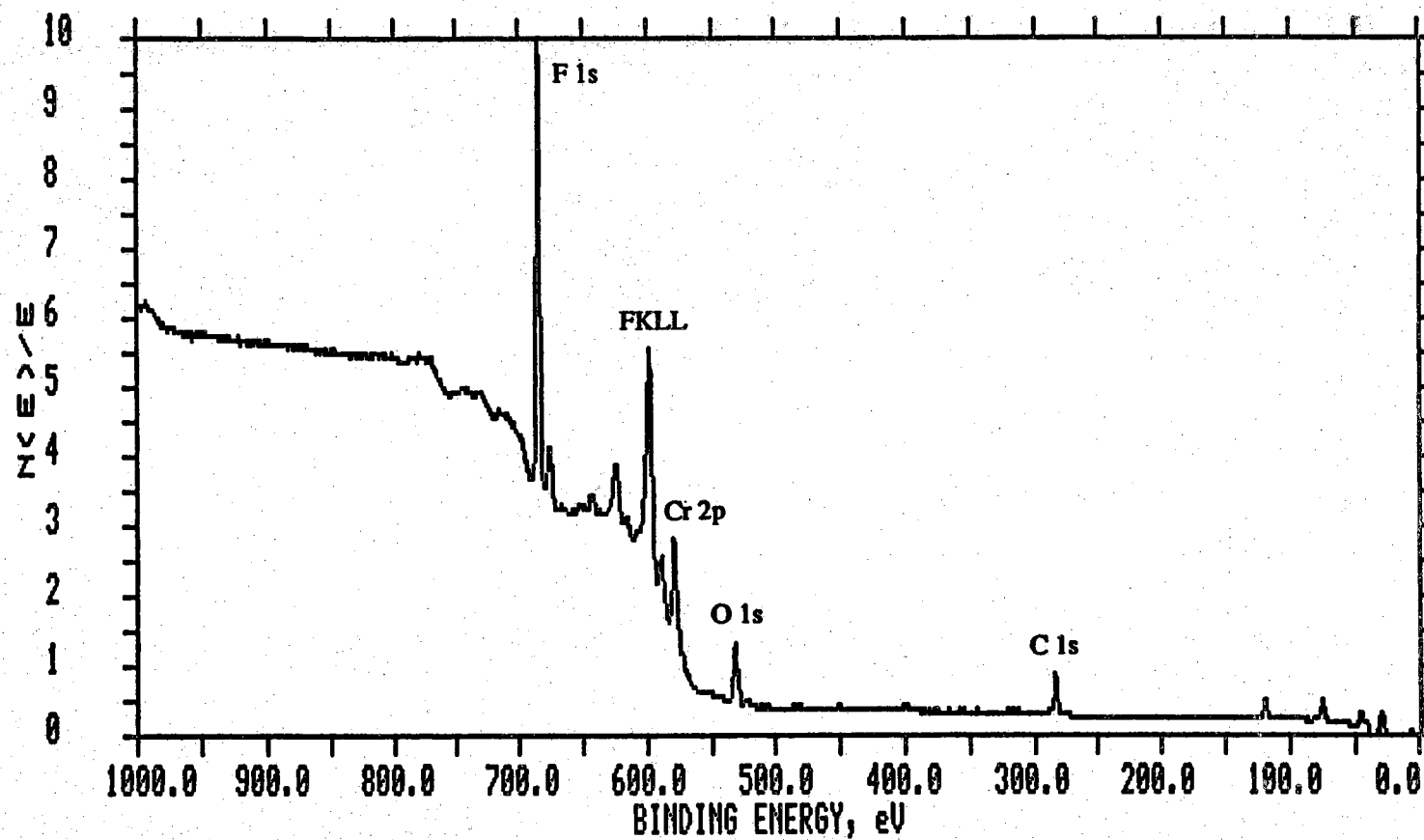
Figure 4.11 XPS survey spectrum of Cr surface after CF_4 plasma exposure.
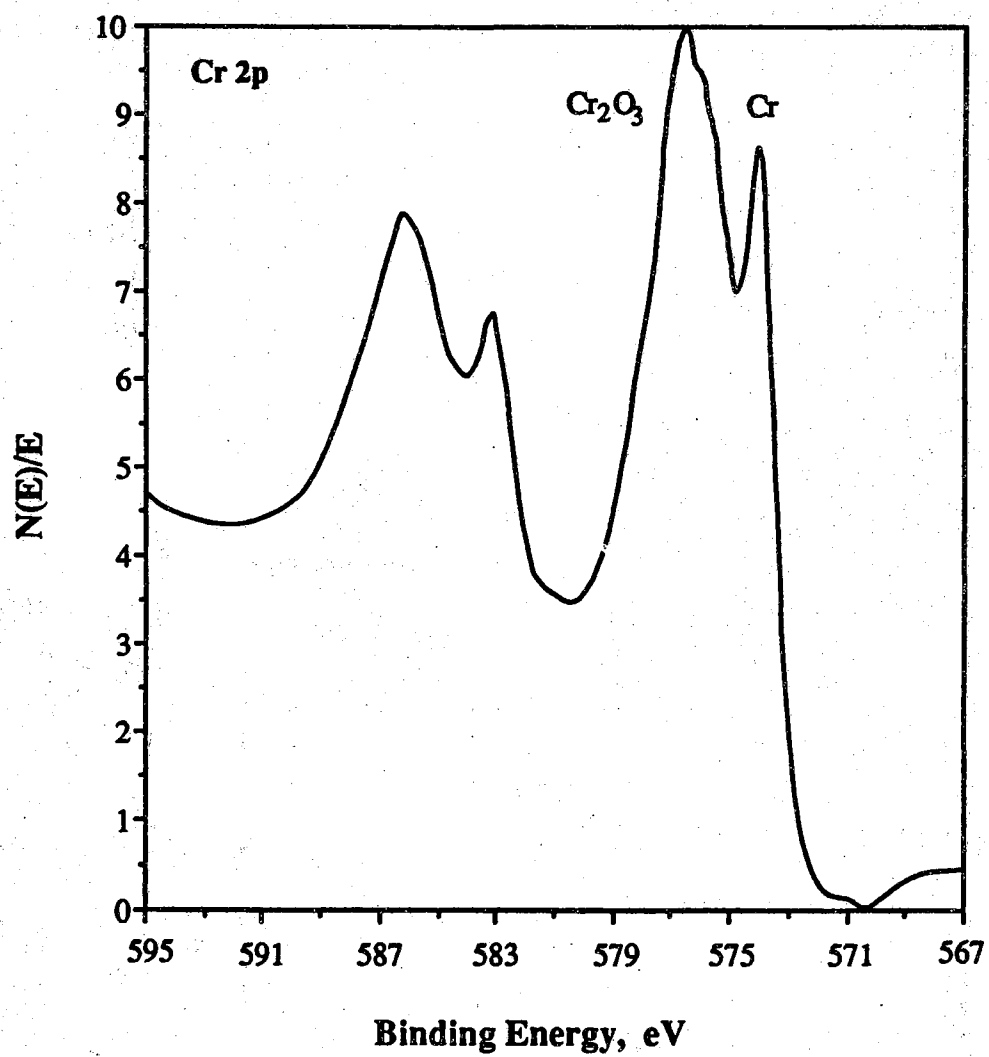
Figure 4.12   Cr 2p spectrum of Cr surface before CF$_4$ plasma exposure.
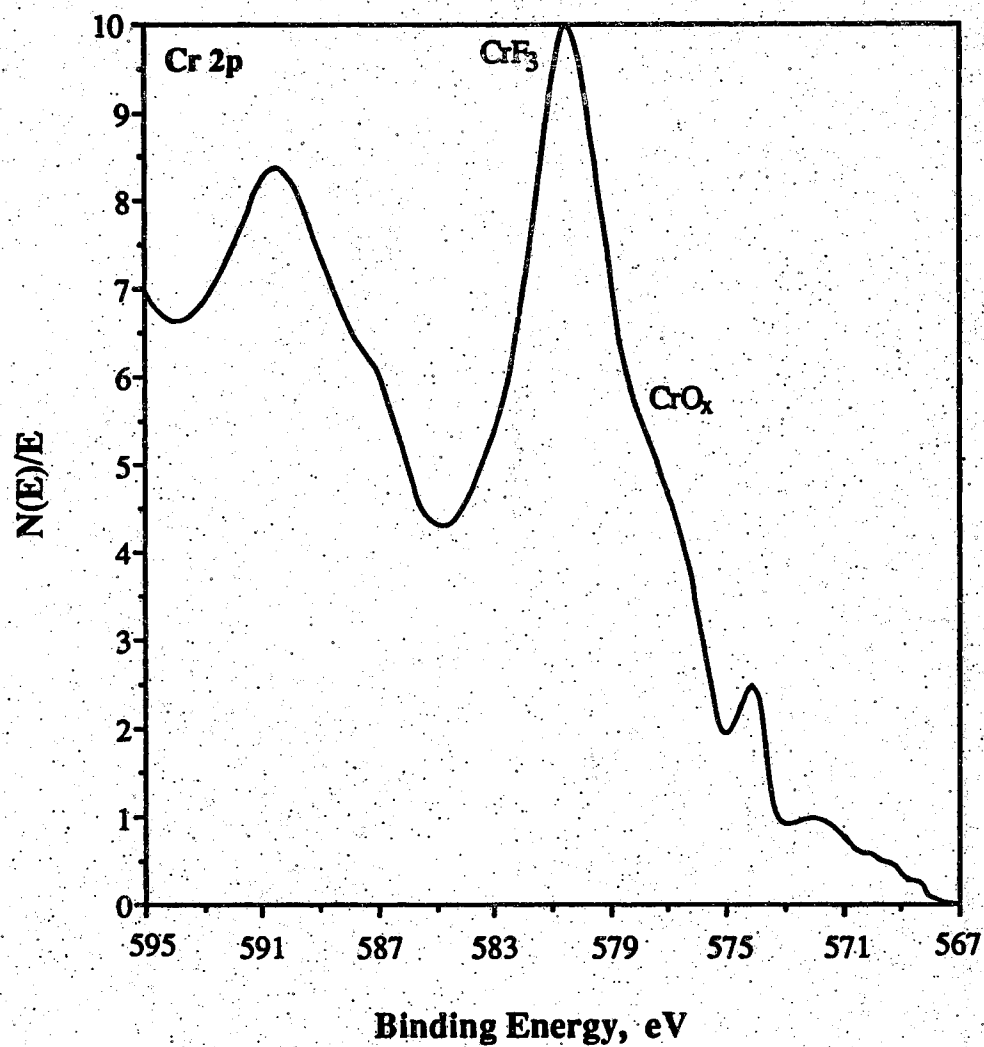
Figure 4.13   Cr 2p spectrum of Cr surface after CF_4 plasma exposure.

Table 4.1   Binding energies of Cr 2p photoelectron peaks and spin-orbit splitting for some O- and F-containing compounds

Compound	Binding energy (eV)[a]		Spin-orbit splitting (eV)	Reference
	Cr $2p_{3/2}$	Cr $2p_{1/2}$		
CrO_3	579.1	588.2	9.1	(166)
	580.3	589.4	9.1	(167)
	579.9	588.9	9.0	(168)
CrO_2	576.3	586.0	9.7	(169)
Cr_2O_3	576.8	586.4	9.6	(170)
	576.3	586.0	9.8	(170)
	576.6	586.3	9.7	(170)
$Cr(OH)_3$	577.0	586.8	9.8	(170)
CrF_3	579.4	589.3	9.9	(166)
	579.2	589.1	9.9	(167)
CrF_2	578.1	587.7	9.6	(166)
Cr metal	574.2	583.5	9.3	(170)
	574.4	583.7	9.3	(166)

[a]Binding energies: corrected to Au 4f(7/2) as 84.0 eV or C 1s as 285.0 eV.

than 3 F atoms for each Cr atom.

4.4.3.3 Effect of Postetch Treatment

In the case of Al metalization etched by chlorine-based chemistry, various post-etch treatments have been proposed to reduced postetch corrosion[161-164]. These include H_2O or solvent rinse, annealing or oxidation, CF_4/O_2 plasma, O_2 plasma, and nitric acid treatments. The basic principle of these techniques is either to reduce the residual chlorine content or to repassivate the surface by oxidation. In this study, various post-treatments were also carried out after CF_4 plasma etching of the capacitors as shown in Figure 4.8(b). Then, their effects were directly checked against the corrosion test. The post-treatments used in this part of the study are as follows: (1) deionized H_2O rinse at 25 °C for 3 min; (2) 10 min soak in concentrated HNO_3 (70.5%) + H_2O rinse + baking at 120 °C in air for 20 min; (3) O_2 plasma treatment for 20 min at a rf power of 150 W; (4) H_2O rinse + O_2 plasma treatment for 20 min; (5) O_2 plasma treatment at 200 °C. All O_2 plasma treatments were performed in the planar plasma system for 20 min at 450 mT and 150 W. Unfortunately, Cr corrosion occurred after all these treatments.

4.4.3.4 Corrosion Product Identification

Visually, the corrosion product has a brown color. The corroded top surface was examined with XPS and a survey spectrum is shown in Figure 4.14. Figure 4.15 and Figure 4.16 give the Cr 2p and O 1s spectrum. One obvious change is the greatly increased intensity of the O 1s peak. This indicates that the corrosion reaction may be a chromium oxidation. The main Cr 2p peak is at 579.7 eV with a spin-orbit splitting of 9.2 eV. In comparing with Table 4.1, it is possible that some Cr is present as Cr(VI) in the corrosion products since the spin-orbit splittings of Cr(III) compounds are larger than those of Cr(VI) compounds. From the Cr 2p spectrum, it can also be seen that the Cr $2p_{3/2}$ peak has a weak shoulder at the low binding energy side with a position of 577.1 eV. This observation suggests that Cr(III) species like Cr_2O_3 and $Cr(OH)_3$ may be formed and incorporated within the film. The O 1s signal can be split into two peaks at 530.7 eV and 532.8 eV. Air-oxidized Cr samples show only the peak at 530.7 eV, which should be correlated to an O^{2-} species. The O 1s signal at 532.8 eV is attributed to H_2O and OH^- species[171]. To summarize, XPS surface analysis indicates that the corrosion products are a mixture of chromium oxide and hydroxide of higher-valent Cr species like Cr(III) and Cr(VI).
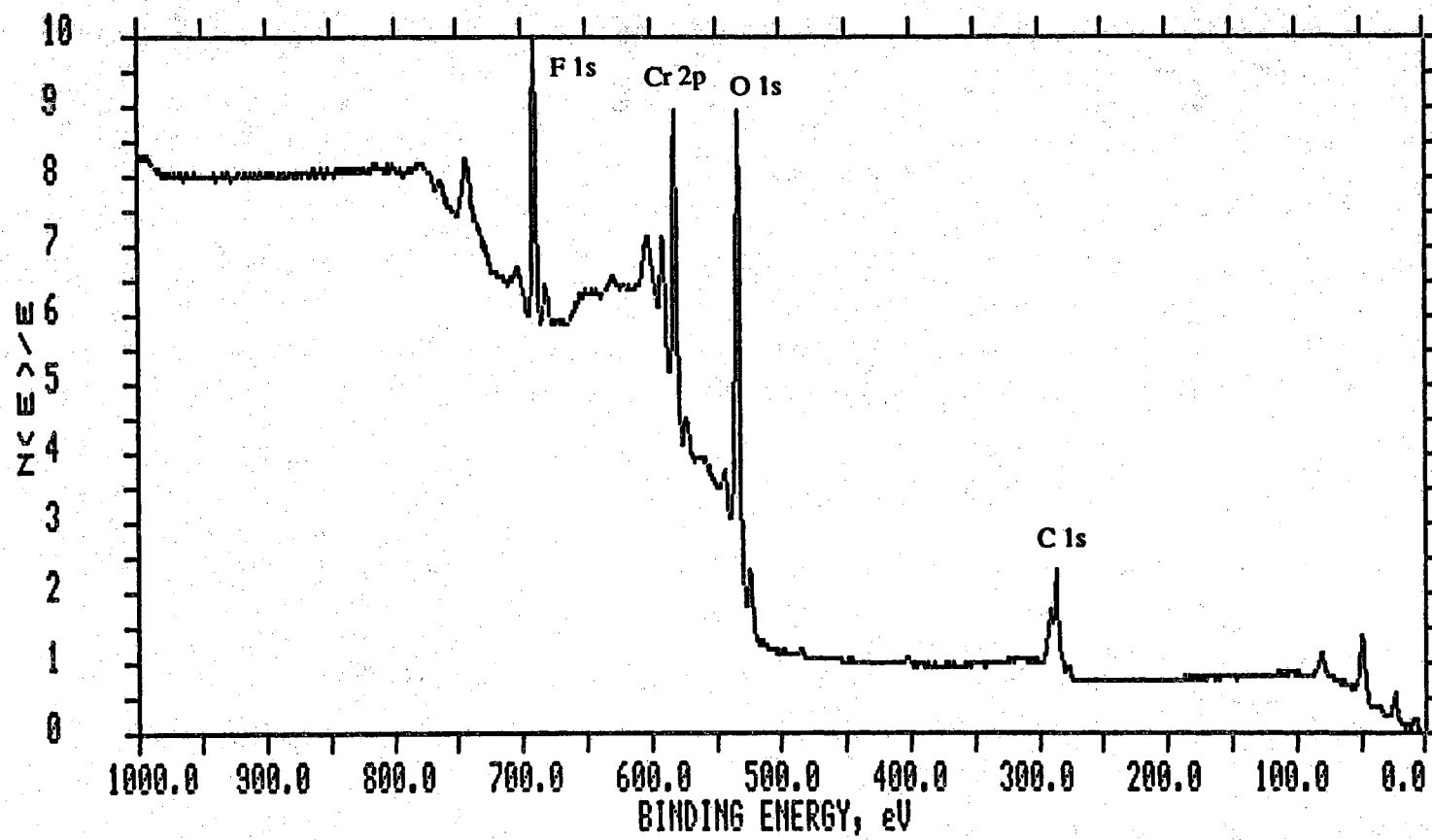
Figure 4.14   Survey spectrum of corroded Cr surface.
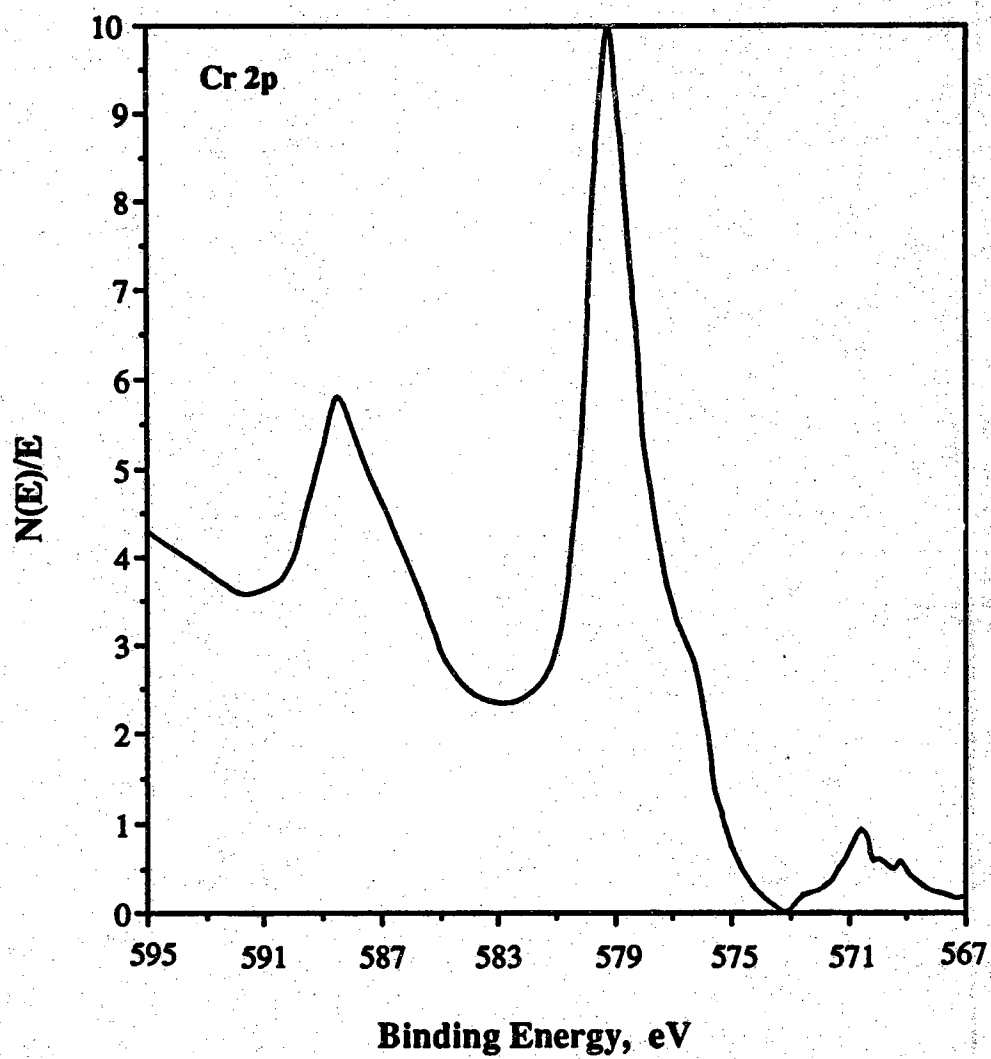
Figure 4.15   Cr 2p spectrum of corroded Cr surface.
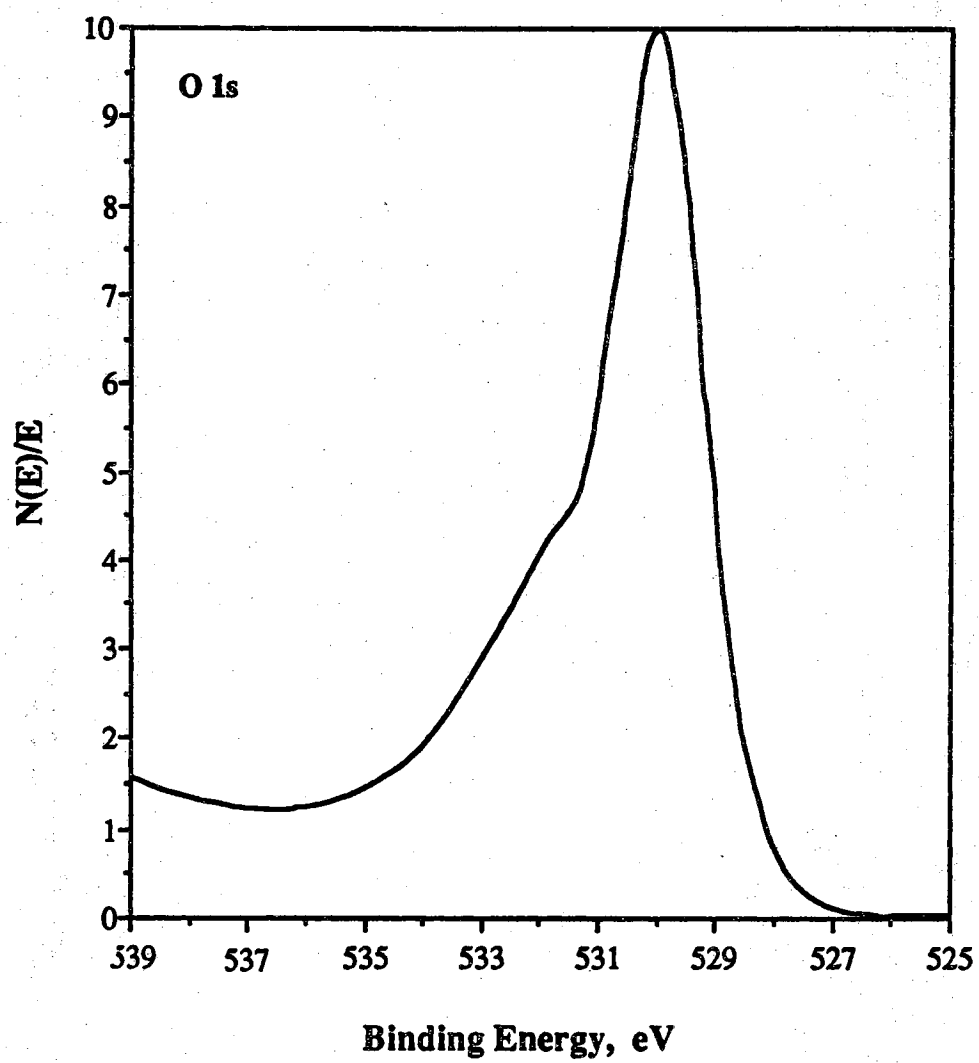
Figure 4.16 O 1s spectrum of corroded Cr surface.

Auger spectrum was also taken on the same sample. Peak positions and peak to peak height of the desired transitions were qualitatively the same both before and after 30 min of sputtering. The whole Cr layer has been oxidized and fluorine species are now distributed over the entire corrosion product. A cross sectional TEM picture in Figure 4.17 shows a clear interface of Cr/SiN_x and SiN_x/Cr corrosion products. EELS analysis indicated that the top Cr layer consists of Cr/oxygen and the SiN_x/bottom Cr layers are intact. This further verifies that there was no reaction between SiN_x and top Cr film.

4.4.4 Discussion

4.4.4.1 Cr Surface Modification by CF_4 Plasma

As mentioned, Cr surfaces exposed to CF_4 plasma can have various chemical and physical effects. For example, many metals such as Al and Ag can be heavily fluorinated in a O_2/CF_4 plasma[172]. In the present case, XPS measurement shows that the Cr surfaces are highly fluorinated, while the corrosion tests indicated that this is an important cause of the corrosion. The surface chemical composition was assumed to be CrF_3 by comparison with published data. However, other fluorides may also be present. For example, chromyl fluorides and chlorides are known to occur[173, 174]. In some cases, the latter have been known to form during plasma etching of Cr films using O_2-CCl_4 mixtures[175]. In CF_4 plasma, CrF_3 is a reasonable product because a general method to prepare this compound is the fluorination reaction of Cr either in liquid or gas phase[176]. Chromium trifluoride is so inert that it is insoluble in water and hot hydrochloric, sulphuric, and nitric acids attack it only slightly[177, 178]. In fact, it has been used for passivation of chromium and other metal surfaces due to its high resistance to corrosive halogen or halide and its impermeability to water vapor[179, 180]. These may be the reasons why various post-etch treatments were not effective in avoiding the Cr corrosion problem in $Cr/SiN_x/Cr$ capacitors.

Besides the change in chemical composition, energetic particle bombardment causes bond breakage, amorphization, preferential sputtering and defect formation[181]. Associated with these are the creation of surface cavities, inclusions and various fault in the surface. As a result, there will exist a number of points in the film where it is less thick, less strong or more permeable than elsewhere. Pitting corrosion can therefore take place at these spots.
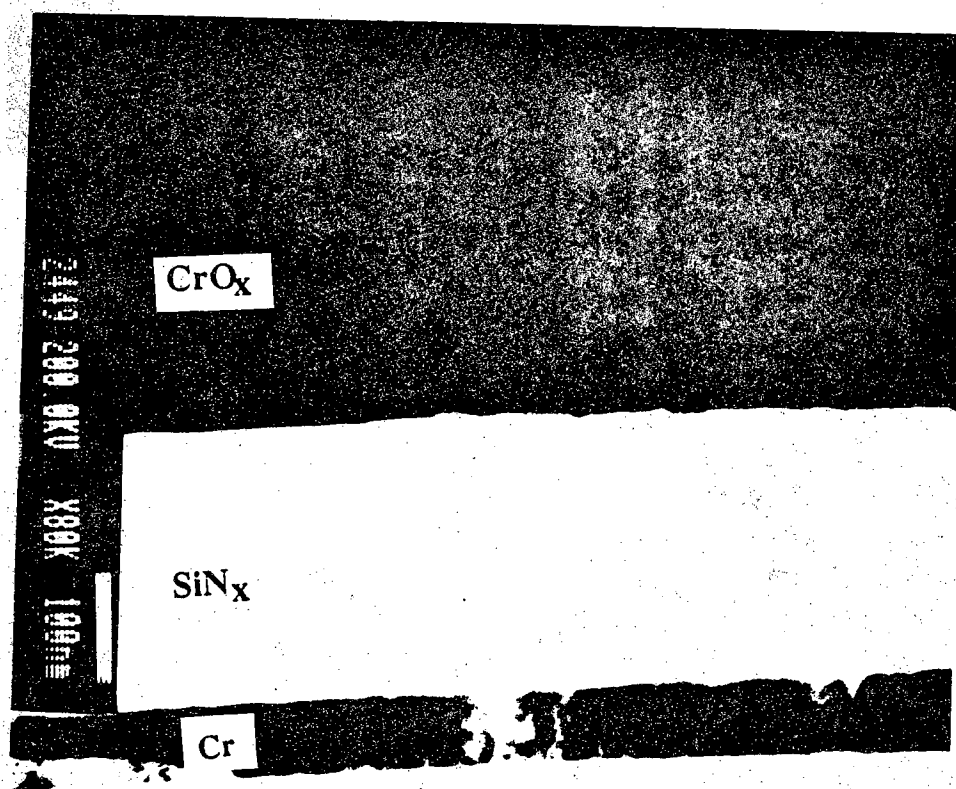
Figure 4.17 Cross sectional TEM picture of a corroded $Cr/SiN_x/Cr$ capacitor.

4.4.4.2 Corrosion Mechanisms

4.4.4.2.1 Corrosion Mechanism in Immersed Electrolytes

From corrosion product analysis in the previous section, it is obvious that the Cr corrosion is an electrochemical oxidation. In classical electrochemistry, the anode and cathode in an electrochemical cell are coupled through either an aqueous electrolyte or by a solid state ionic conductor. Electrochemistry of the corrosion and passivation of Cr in acid solutions has been previously studied in detail[182, 183]. No reports appeared in the literature for the structure of a solid state capacitor, although it should be similar in principle. Under deionized water immersion, the corrosion cell components may be identified very easily as

$$Cr \mid Cr_2O_3, CrF_3 \mid H_2O, OH^- \mid H_2(g) \mid Cr$$
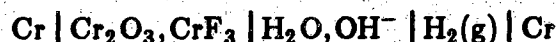
From the view of electrochemical thermodynamics, anodic oxidation or dissolution and cathodic reduction can occur under a large enough over potential. This could result in a series of soluble Cr-containing species such as Cr(II), Cr(III), bichromate $HCrO_4^-$ or dichromate $Cr_2O_7^{2-}$, depending upon the pH as seen in a standard Pourbaix diagram for the system Cr—H_2O[184]. The applied voltage was so large in this case that it may be well in or above the transpassive region. The complete removal of Cr near the cathode connection side indicates the corrosion products are indeed soluble in water and that the dissolution of top Cr starts at the edge near the cathode side. The latter can be understood if the anode and cathode distance in the electrolyte is considered. This also explains why a small Cr island was left in the inner area for CF_4 plasma etched capacitors, where the anode and cathode are coupled together along the whole periphery.

4.4.4.2.2 Atmospheric Corrosion

In the moist atmosphere, it is not obvious to see where the corrosion cell components are located and how they are coupled together. Its corrosion mechanism may or may not be similar to that under water immersion. If the anode and cathode could still be considered to be two Cr films separated by SiN_x, then two possible coupling routes can exist, in principle, for CF_4 plasma flooding-etched structures. The first is via periphery where both top and bottom Cr films are exposed to the atmosphere. The second is through SiN_x at some spots which are weak enough so that moisture and ions can penetrate due to the plasma treatment. In either case, the thickness of the moist film of at

least in the order of tens of molecular layers is required to serve as electrolyte[165] and therefore couple the anode and cathode together.

Several mechanisms have been identified for condensation of moisture on metal surfaces at a relative humidity of less than 100%. First is capillary condensation where the vapor pressure above a concave meniscus of water is less than that in equilibrium with a plane water surface. It is therefore possible for moisture to condense in narrow capillaries from an atmosphere of less than 100% relative humidity. Secondly the adsorption condensation — formation of an extremely thin layer of condensed molecules of H_2O which are bound to surface by Van der Waals' force. The third mechanism is by chemical condensation. This occurs when soluble corrosion products or atmospheric contaminants are present on the metal surface. When the humidity exceeds that in equilibrium with a saturated solution of the soluble species, a solution, initially saturated, is formed until equilibrium is established with the ambient humidity. All three mechanisms can occur simultaneously or each dominates at different stages during the corrosion process.

The experiments performed on structures in Figure 4.8 unambiguously show that coupling is of the first kind through the periphery, at least for a 4 minute plasma exposure. For the structures where passivation SiN_x was etched away as shown in Figure 4.8(b) and 4.8(c), a crevice exists along the whole periphery due to the nature of isotropic etch. Therefore, capillary condensation can take place there which would couple the two Cr films together either prior to testing or during the polarization stage. Once this happens, anodic oxidation of the top Cr films will be initiated at places where it has more negative electrode potential as well as moisture condensation. It is known that atoms at dislocations and defects have higher chemical free energy and constitutes chemically active sites. Those sites having the highest energy have a correspondingly more negative single potential and anodic dissolution might be expected to occur chiefly at these locations. If a macroscopic crack, crevice or a foreign particle happens to reside at the same place, then a corrosion pit would first appear there. CF_4 plasma exposure of the Cr films can well promote the formation of these pitting sites. Although SEM examination and surface-profile did not indicate noticeable differences in surface smoothness after plasma etching, many effects in the plasma such as ion bombardment, surface reconstruction and fluorination could in fact peptize the native Cr oxide, making the protective surface layer discontinuous and providing H_2O direct access to the metal layer.

The pitting corrosion in structures as processed in Figure 4.8(c) with longer exposure time than 8 min is probably caused by a different mechanism such as the second kind mentioned above. Here the local damage is much more severe and the fluorine penetration is so deep that a pin hole in the SiN_x could be generated electrochemically. The pit can not grow if a dehydrated corrosion product fills the hole and thus shuts off the ionic/water path.

For the flooding-etched capacitor structure, a further look at the corrosion process shows that the immediate corrosion product has a gel appearance and the corrosion front moves very fast. The experimental results and discussions above both support the conclusion that it is essential to bring the metallic film in contact with water for atmospheric corrosion to occur and grow. This is therefore considered to be indicative of the requirement for the presence of bulk water in the corrosion reaction. However, it is indeed difficult to believe that a macroscopic water layer is residing on the whole surface prior to corrosion at a relative humidity of 45%. Chemical condensation can make this happen. However, this seems to be not the case because both Cr_2O_3 and CrF_3 are insoluble in water and therefore not deliquescent. The in situ observation of the corrosion processes in atmosphere and under a moist air burst is crucial in understanding this point. The main difference is that many more pits are initially created under the latter condition while the growth rate and appearance are the same. Therefore, it is possible that the water supply is maintained by the corrosion product. Further information can be inferred from the testing results of Figure 4.8. The behavior of either no corrosion or little corrosion along the periphery only for the structure of Figure 4.8(d) is highly likely to indicate that Cr fluoride of a higher oxidation state is responsible for the water condensation. As mentioned in the water immersion case, a series of Cr oxidation states can appear in the corrosion product and therefore the fluorides. It is known that CrF_4 is deliquescent[185] and many of the complex fluorides and oxyfluorides of higher oxidation states Cr(IV), Cr(V) and Cr(VI) are easily hydrolyzed[176]. High concentration of these corrosion products will tend to expose a lower vapor pressure surface to the environment, thus, since the solution will try to come to equilibrium with the gas phase by absorbing more water vapor and diluting the solution; it will collect more water until an equilibrium between the solution partial pressure and the atmospheric partial pressure of water is approached if not achieved[186, 187]. Thus corrosion can continuously grow from the junction between Cr and the corrosion products.

Since the experiments in this work are not vigorously electrochemical and are only intended to show the causes of atmospheric Cr corrosion in the solid

state cell structure, it is very difficult, if not impossible, to give an actual reaction pathway of the whole corrosion process. Although curve (c) in Figure 4.9 looks like a potentiostatic i—v curve in the active and passive regions, the decreasing of current a few volts above V_{corr} is due to a complete dissolution of anodic Cr film and a loss of water. At this stage, anodic corrosion products are directly in contact with the cathode. It should be mentioned again about the chemical composition of the final corrosion products. XPS analysis showed that there are Cr(VI) compounds present which should be soluble in water if they are in the isolated state. However, in the solid matrix of Cr_2O_3 or Cr hydroxide their insolubility in water is understandable. Further, redox chemical reactions can occur after anodic dissolution because of the high oxidation potential of chromate and of the less conductive corrosion products which has a less positive potential than the Cr film. The latter would render the higher oxidation state of Cr species thermodynamically unstable. One example could be the following reactions:

$$CrO_4^{2-}+3Cr^{2+}+2H_2O=2Cr_2O_3+4H^+$$

for which the standard driving emf $\mathscr{E}=1.13V$. The net result is that stable Cr(III) oxide or hydroxide is precipitated. As such, the gel appearance is gradually gone due to water consumption in the above reaction.

4.4.4.3 Implication to a-Si:H TFT Device Design and Testing

The corrosion behavior of and the conclusion drown from $Cr/SiN_x/Cr$ capacitors have direct relevance to a-Si:H TFT devices. This is because the corrosion mechanisms are believed to be the same for the two kind of structures. First, it is apparent that CF_4 plasma exposure of Cr films in the devices is always a potential cause of possible electrochemical corrosion in a humid environment. Photoresist is an effective mask to the fluorination reaction. Second, the passivation length of SiN_x, d in Figure 4.7, should be large enough to prevent the two metal layers from coupling. This may impose a problem in device design since it may limit the final circuit density. At the very least, a zero d design is not a good practice especially when there is CF_4 plasma exposure at the same area. Without a passivation layer over the whole surface, as is usually done for device research in the early stage, care must be taken to avoid testing in a humid atmosphere in order to avoid device failure.

4.5 Summary

Normal staggered a-Si:H TFTs were fabricated to show a current on/off ratio of larger than 10^5 for a gate voltage swing from 0 to 20 V even without source/drain implant. However, if no passivation layer was employed or special care in testing was not taken in testing, devices were quickly died in a humid atmosphere as soon as the gate voltage reaches above +6 V.

Failure of unpassivated a-Si:H TFTs has been shown to be due to electrochemical corrosion of gate Cr films. Studies on differently processed $Cr/SiN_x/Cr$ capacitors indicated that the corrosion was largely promoted by CF_4 plasma exposure of the metal surface. XPS analysis shows that Cr surface is heavily fluorinated and it consists of chromic fluoride with a small fraction of oxide. It is suggested that the electrochemical cell is coupled via periphery for plasma exposure times of less than 6 min. For longer exposure times, pitting corrosion may have a different mechanism. The corrosion reaction was found to be limited by water availability. For plasma exposed structures, chemical condensation of a water layer, due to deliquescent corrosion products, was suspected to cause the corrosion growing quickly over the entire surface.

CHAPTER 5
EXPERIMENTAL STUDY OF THE SOURCE/DRAIN
PARASITIC RESISTANCE EFFECTS IN a-Si:H TFTs

5.1 Introduction

As stated in Chapter 2, the performance of a-Si:H TFTs can also be influenced by many geometrical or extrinsic factors such as the channel length[103], a-Si:H thickness, source/drain to gate overlap [188], and source/drain (S/D) contact quality [63]. In static characteristics, these factors manifest themselves as a lumped parasitic resistance, R_p. The R_p effect has long been recognized because of a current crowding near the origin of the output characteristics [98]. For properly processed devices incorporating a n^+ a-Si:H layer, at least a quasi-ohmic contact can be routinely obtained. However, the magnitude of the parasitic resistance can still affect the transconductance to a large degree. This is specially true for short channel devices where a decrease in the field mobility with the decrease of the channel length has been observed [103]. This effect has been generally attributed to the increased weight of the parasitic resistance at small channel lengths. Therefore, much effort is needed to study the source/drain parasitic resistance effect before full advantage of short channel devices can be utilized. On the technology side, it is helpful to further reduce the contact resistance by employing a n^+ microcrystalline a-Si:H contact layer and by reducing the intrinsic a-Si:H thickness. More importantly, however, the parasitic resistance components and their modeling should be studied. This would not only reveal the limiting components but also provide knowledge for better device design and more accurate circuit simulation. Very recently, several groups began to make these efforts [189,190]. However, the a-Si:H TFTs studied employed a deposited n^+ a-Si:H layer and many aspects of the parasitic components are still not clear.

The inverted-staggered a-Si:H TFTs investigated in this thesis utilizes an ion implantation step to obtain the ohmic source/drain contacts. Because the

ion implant goes through the entire a-Si:H layer, the effect and behavior of the source/drain parasitic resistance may be quite different from those having an intrinsic layer between the n^+ and the channel. For comparison, Figure 5.1 illustrates the inverted-staggered a-Si:H TFTs with two different contact structures. With a successfully developed a-Si:H TFT process, this chapter is entirely devoted to the experimental study of the parasitic resistance effect.

5.2 Test Device Structures and Characterization

Test structures were used to extract the total a-Si:H TFT parasitic resistance, sheet resistance R_s of implanted n^+ a-Si:H films, and the specific contact resistance of Al-Si to n^+ a-Si:H. Specifically, these structures can be classified into four types:

(a) TFTs with constant channel width to length ratio W/L and with L ranging from 40 to 0.5 μm. These devices were used to obtain the total parasitic resistance R_p. For small drain voltages, V_D, at high gate drive it is assumed [103] that the TFT ON resistance R_{on} consists of the channel resistance R_{ch} and the parasitic resistance R_p. That is,

$$R_{on} = \frac{\partial V_D}{\partial I_D} \Big|_{\substack{V_G \\ V_D \to 0}} = R_{ch} + R_p. \tag{5.1}$$

Using the gradual channel approximation, the channel resistance in the linear region is then given by

$$R_{ch} = \frac{L}{W \mu C_i (V_G - V_T)}, \tag{5.2}$$

where C_i is the gate nitride capacitance per unit area and W, L, and V_T are intrinsic device channel width, length and threshold voltage, respectively. The parasitic resistance R_p can be extracted by measuring the ON resistance from the linear regions of TFT output characteristics and plotting $R_{on} \times W$ as a function of L.

(b) a-Si:H TFTs with constant channel width W and length L but different source/drain overlap dimensions d_o. Values of 0.5, 1.0, 1.5, 2.0, 4.0, 6.0, 8.0 and 10.0 μm were designed for d_o in the test structures. The channel width and length were fixed at 100 and 10 μm, respectively.

(c) Contact and sheet resistance measuring test structures were also used. Because the metal/semiconductor contact resistance depends on the detailed processing conditions, it is highly desirable to have contact test
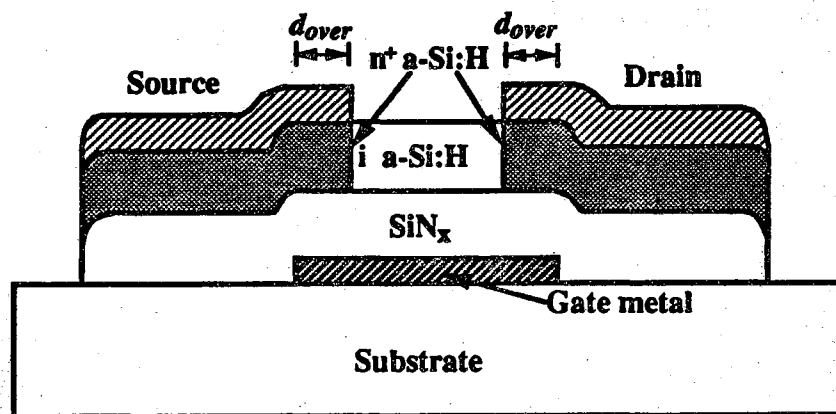
(a)
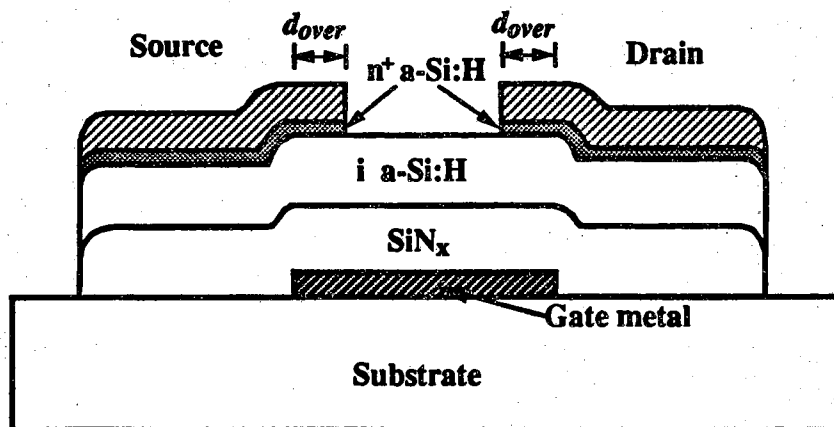
(b)

Figure 5.1 Inverted-staggered a-Si:H TFT structures. (a) a TFT with ion implanted source/drain contacts, (b) a TFT with deposited n^+ a-Si:H contacts.

structures in the same die as the a-Si:H TFTs. Two types of structures were designed for this purpose. First, a transmission line model (TLM) was used for both the n^+ a-Si:H sheet resistance $R_{s(impl)}$ and the specific contact resistance ρ_c of Al-Si/n^+ a-Si:H system. This TLM pattern is shown in Figure 5.2 with $d=10$ μm, $w=200$ μm and $l=1, 2, 4, 8$, and 16 μm. The resistance between any two ohmic pads of width w and separation l will be given by

$$R = 2R_c + \frac{R_{s(impl)}}{w} l \tag{5.3}$$

and thus a plot of R vs. l will give the sheet resistance by the slope $R_{s(impl)}/w$ and the contact resistance by the y-intercept. This should give a much more accurate value because of the relatively large width and of the least-square curve fitting procedure.

A four terminal (Kelvin) resistor (FTR) and square-shaped van der Pauw structures were also designed for the specific contact resistance ρ_c and for sheet resistance $R_{s(impl)}$ and $R_{s(intr)}$ measurement. The areas were 25 $\mu m \times 25$ μm for the FTR and $100 \mu m \times 100$ μm for the van der Pauw patterns.

(d) Cr/SiN_x/a-Si:H capacitors. Capacitors with both intrinsic and n^+ a-Si:H were designed for SiN_x/a-Si:H interface diagnosis. Capacitor sizes were $60 \mu m \times 60 \mu m$ and $80 \mu m \times 80 \mu m$.

The major fabrication steps were already detailed in previous chapters. The only difference is the addition of the contact and sheet resistance test structures. As such, one more mask level was needed to separate the ion implantation and source/drain metalization steps. Because of the much smaller device geometries and more stringent alignment requirements, 10× reticles were first produced on a Cambridge e-beam pattern generator and the final Cr mask set were obtained by using an eletromask optical stepper. All lithographic steps were done on a SUSS MJB 3 mask aligner. For the devices under consideration, the nominal thicknesses of $a-SiN_x$:H and a-Si:H are 2210 $\mathring{A}$ and 1500 $\mathring{A}$, respectively. Figure 5.3 shows the four-level mask layout. To minimize the charge trapping effect, devices were characterized at room temperature by using an HP 4145A semiconductor parameter analyzer in conjunction with an HP model 9000 computer.
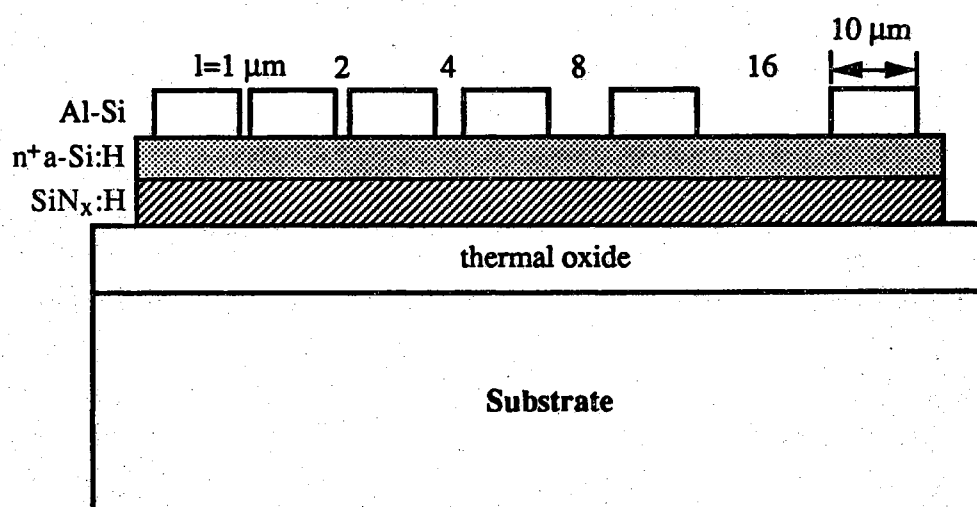
Figure 5.2   The TLM pattern used for contact resistance measurement.
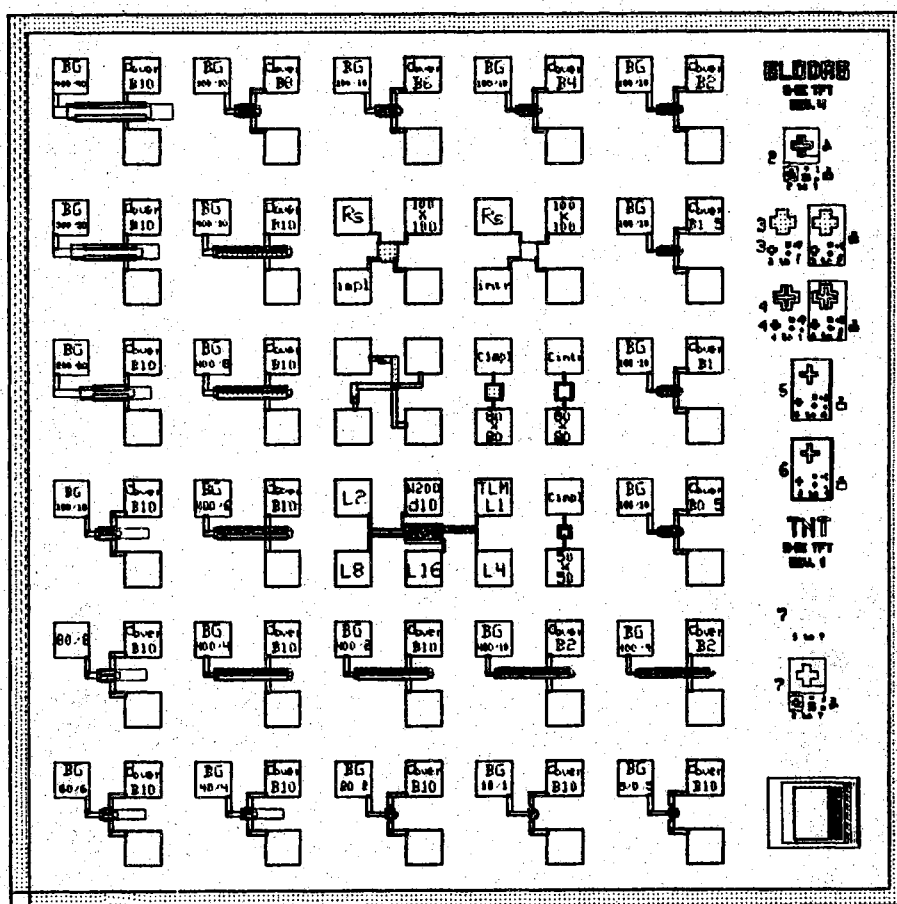
Figure 5.3   The test chip mask layout used in this study.

5.3 Channel Length Effect on TFT Performance

For constant W/L ratios, the effect of parasitic resistance can be clearly seen in the output characteristics of a-Si:H TFTs with different channel lengths. Figure 5.4 shows the output drain current at two gate voltages (10 V and 20 V) for devices with channel lengths of 40, 6 and 2 μm. At a drain voltage of 25 V, a 48% reduction in drain current is observed as the channel length is decreased from 40 μm to $2\mu m$. The drain current also saturates at an increasingly higher drain voltage with decreasing channel length. These observations can be attributed to either a lower apparent field effect mobility, a larger apparent threshold voltage or both because of the increased weight of parasitic resistance to intrinsic channel resistance. However, it is interesting and important to further investigate the channel length dependence of the apparent field effect mobility and threshold voltage.

Using the gradual channel approximation and assuming that the field effect mobility is independent of gate voltage, the saturation current can be described as

$$I_D^{sat} = \frac{\mu_A C_i W}{2L}(V_G - V_{AT})^2 , \tag{5.4}$$

where μ_A and V_{AT} are the apparent field effect mobility and threshold voltage. If the parasitic resistance is ohmic, then

$$V_{AT} = V_T + I_D^{sat} R_p/2 . \tag{5.5}$$

Therefore, the apparent threshold voltage as determined in the $I_D^{1/2}$ vs V_G plot should be independent of channel length. Figure 5.5 shows the square root plot of the drain saturation current vs gate voltage. Device saturation was ensured by connecting the drain and gate terminals together. The extracted apparent threshold voltage V_{AT} and mobility μ_A are shown in Figure 5.6. The apparent mobility is decreased by 50% as the channel length is reduced from 30 μm to 2 μm. However, the apparent threshold voltage is increased by only 14%, which is approximately within the error bounds of processing nonuniformity and measurements. This is in sharp contrast to TFT devices with a deposited n^+ a-Si:H layer [190], where the apparent threshold voltage could change by more than 40%. The small variation of effective threshold in the present case probably indicates an ohmic source/drain parasitic resistance. Indeed, the source/drain regions of our devices are quite different from those reported because of the phosphorus ion implantation used to form the n^+ contact regions.. For implant conditions used in the present devices, SUPREM III
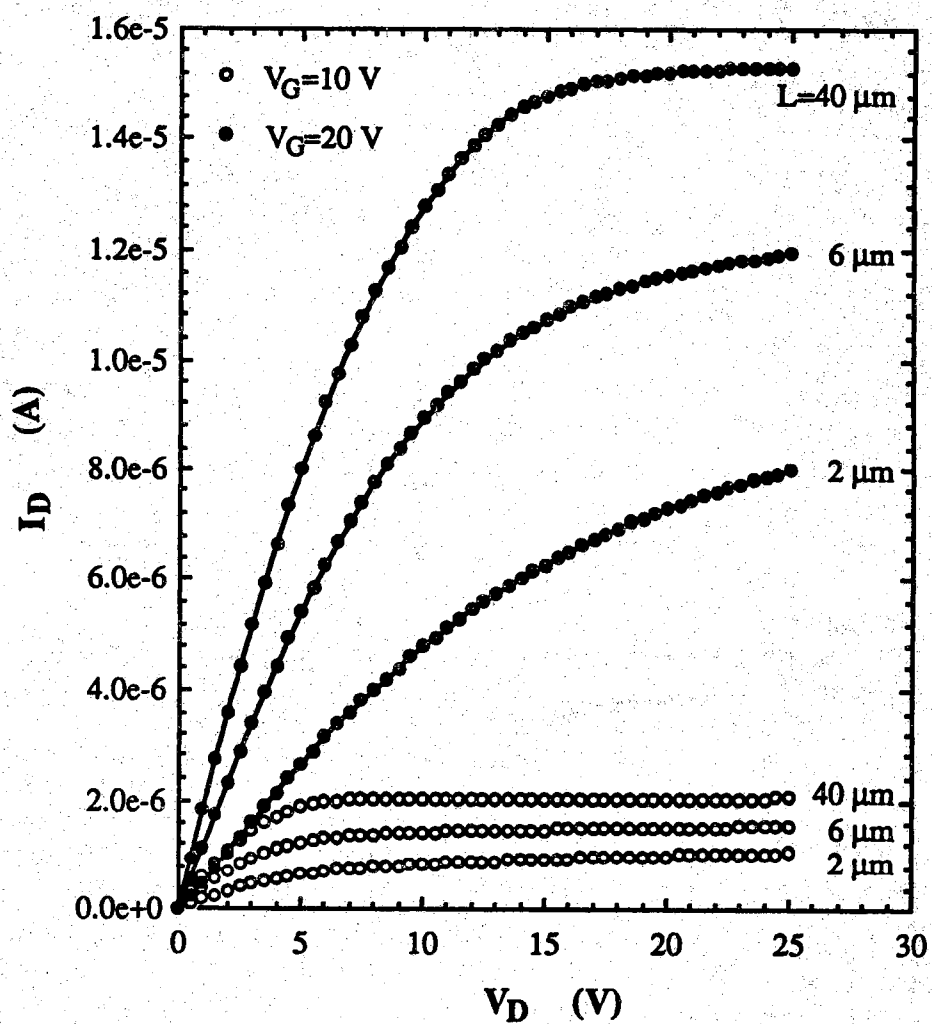
Figure 5.4 Output characteristics I_D vs V_D for TFTs with different channel lengths of 40, 6, and 2 μm. W/L=10.
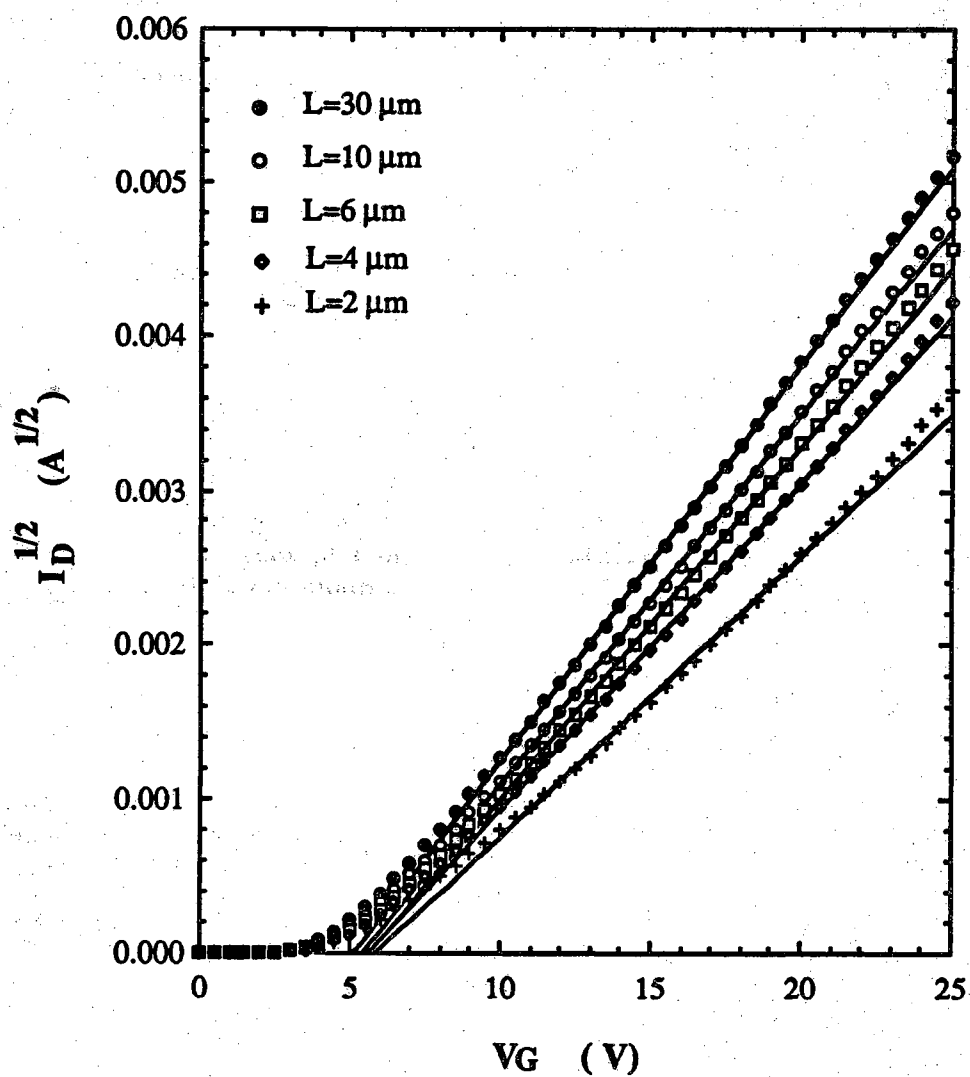
Figure 5.5   Square root plot of the drain saturation current vs gate voltage for different channel lengths. $V_D = V_G$.
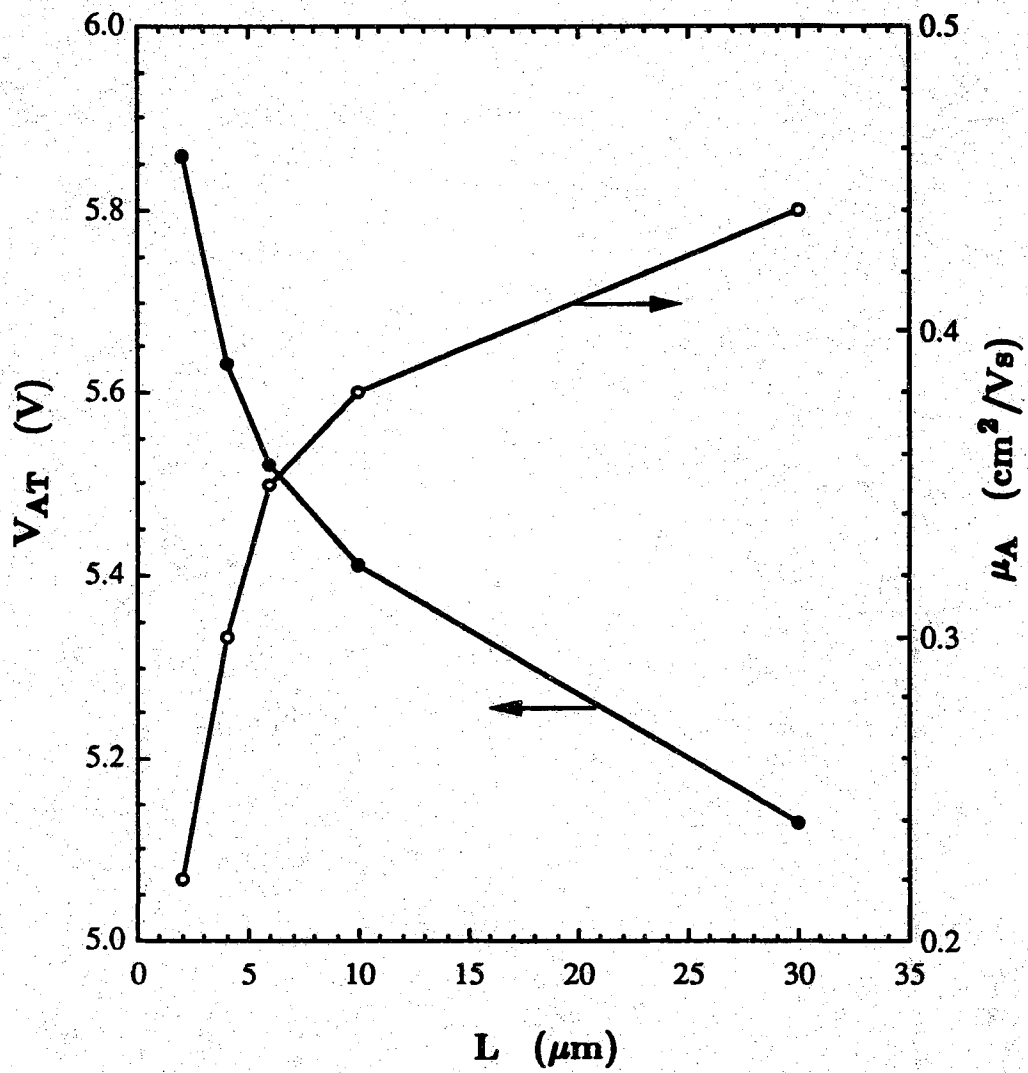
Figure 5.6   The variation of apparent threshold voltage and apparent mobility in the saturation regime as a function of the channel length.

simulation shows that the phosphorus chemical concentration is about 2×10^{15} atoms/cm^3 at the a-Si:H/$a-SiN_x$:H interface. The lack of an intrinsic a-Si:H layer under the contacts eliminated such nonlinear effects as the space charge-limited conduction (SCLC). Therefore, the parasitic source/drain resistance can be considered approximately ohmic.

With the above arguments, equations (5.1) and (5.2) are then applicable to the extraction of parasitic resistance parameters. The TFT ON resistance R_{on} can be measured in the linear region of the output characteristics as shown in Figure 5.7. For each device with L ranging from 2 to 40 μm, the drain current was measured at 0.05 V increments for a gate voltage ranging from 6 V to 20 V. The resulting width-normalized ON resistance $R_{on}\times W$ is then given in Figure 5.8. This plot contains a rich information about both intrinsic and parasitic device characteristics. In the following, each of these properties will be qualitatively analyzed to get some physical insight into the parasitic resistance effects.

The slope of the $R_{on}W$ vs L plot, i.e., the channel sheet conductance, contains only intrinsic device parameters independent of the channel length, as predicted by equation (5.2). Therefore, by plotting $[\Delta R_{on}W/\Delta L]^{-1}$ vs gate voltage V_G, given in Figure 5.9, the intercept and slope of a linear least-square fit give the intrinsic device threshold voltage V_T and field effect mobility. This yields $V_T=5.32$ V and $\mu=0.44$ cm^2/Vs. They are very well in agreement with those values determined from the saturation characteristics when L=30 μm. Therefore, it is inferred that TFT devices with L>30 μm can be considered as long channel devices and their characteristics are free from parasitic resistance effects. Indeed, both the transfer and output characteristics are identical for devices with W/L=300/30 and 400/40.

To further investigate the parasitic resistance elements, the sheet resistance $R_{s(impl)}$ of the implanted a-Si:H and the specific contact resistance ρ_c has been independently measured by using the TLM pattern in the same die as the TFTs. In Figure 5.10 we show the resistance vs. contact spacing for an Al-Si/n^+ a-Si:H TLM pattern. All R vs. l data were fitted by the linear least squares method. The slope and y-intercept of the straight line resulted in a sheet resistance $R_{s(impl)}$ of 107.9 $M\Omega/\square$ and a contact resistance R_c of 278.3 $K\Omega$. If the ion implantation is uniform throughout the whole a-Si:H layer (t=1500 $\mathring{A}$), then resistivity is given by

$$\rho_{impl}=tR_s=1.6\times10^3 \ \Omega\cdot cm \tag{5.6}$$

which is in agreement with reported values for room-temperature implanted a-
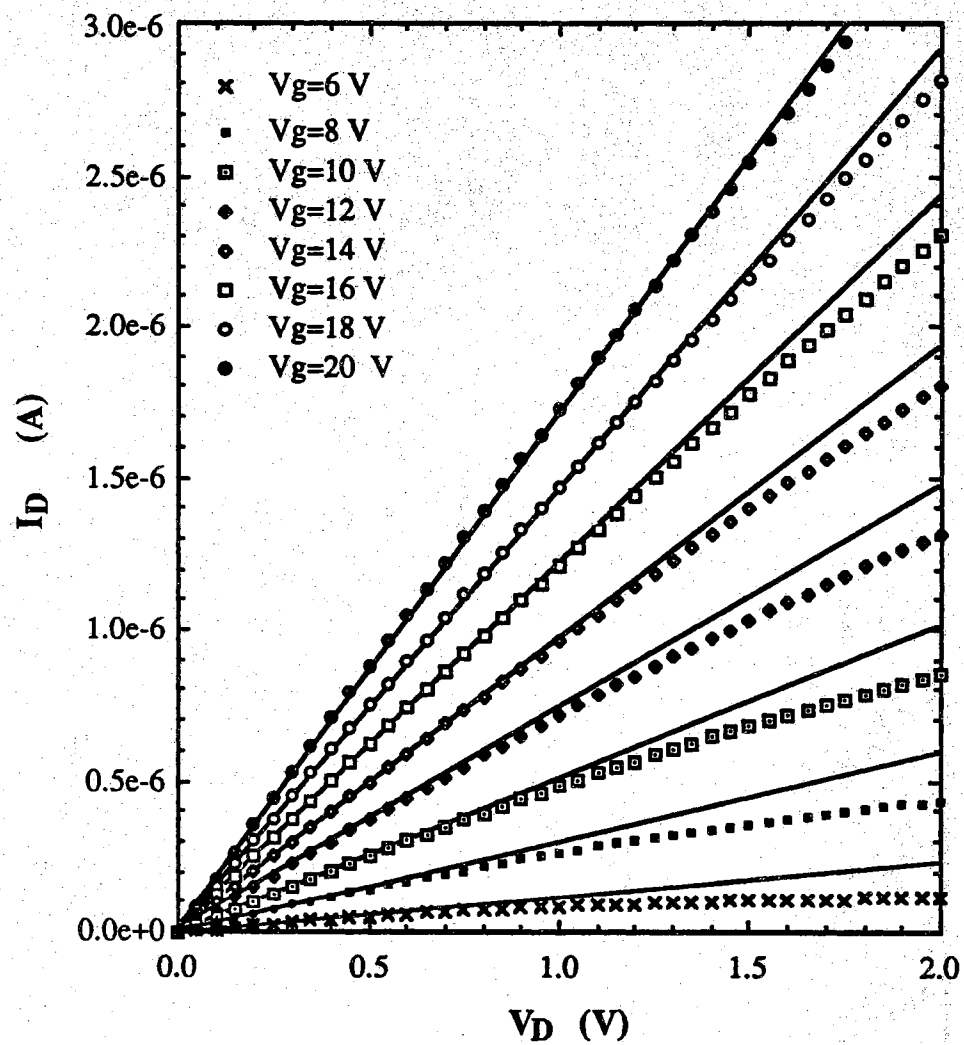
Figure 5.7 An example of the ON resistance measurement in the linear regions of the a-Si:H TFT output characteristics. W/L=400/40.
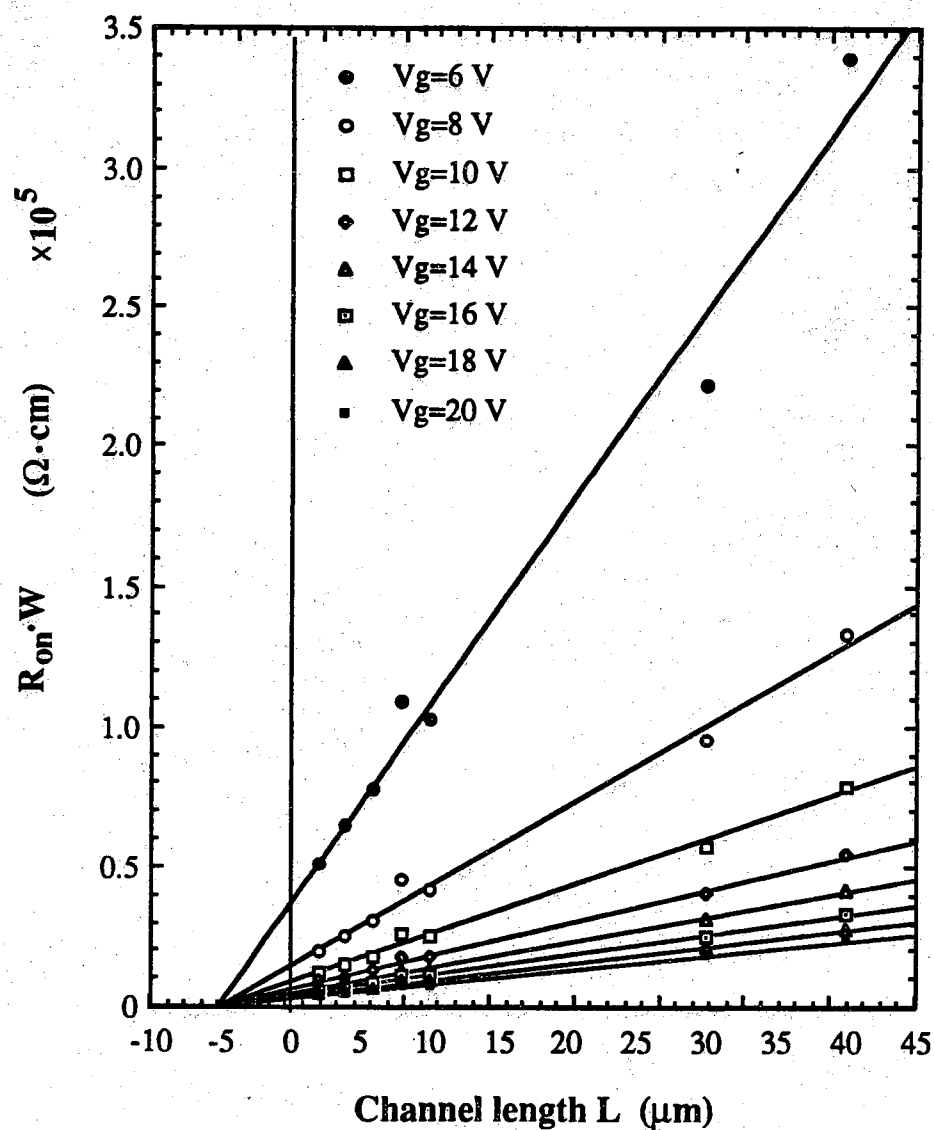
Figure 5.8 Width-normalized ON resistance as a function of channel length at different gate voltages. The solid lines represent the linear least-square fit of the data.

$$y = -6.9578e\text{-}8 + 1.3087e\text{-}8x$$
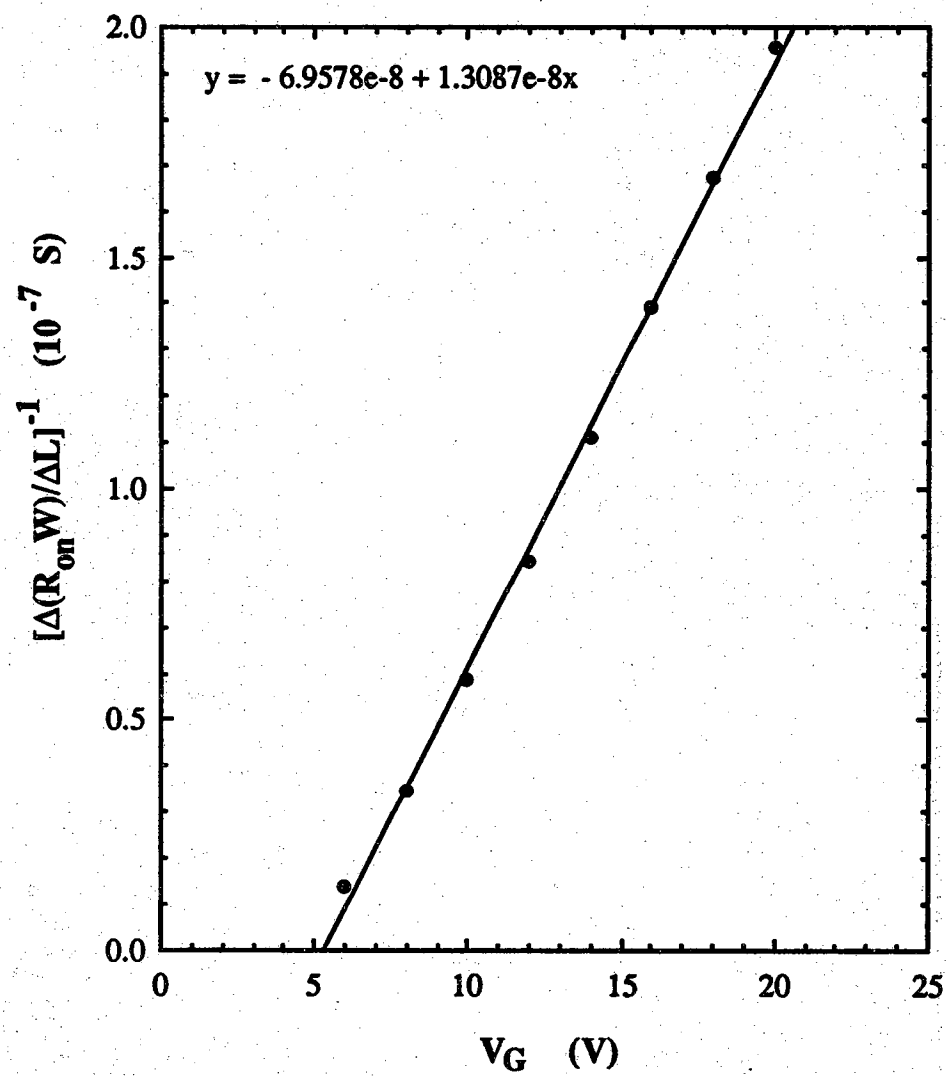
Figure 5.9   Channel sheet conductance as a function of gate voltage.
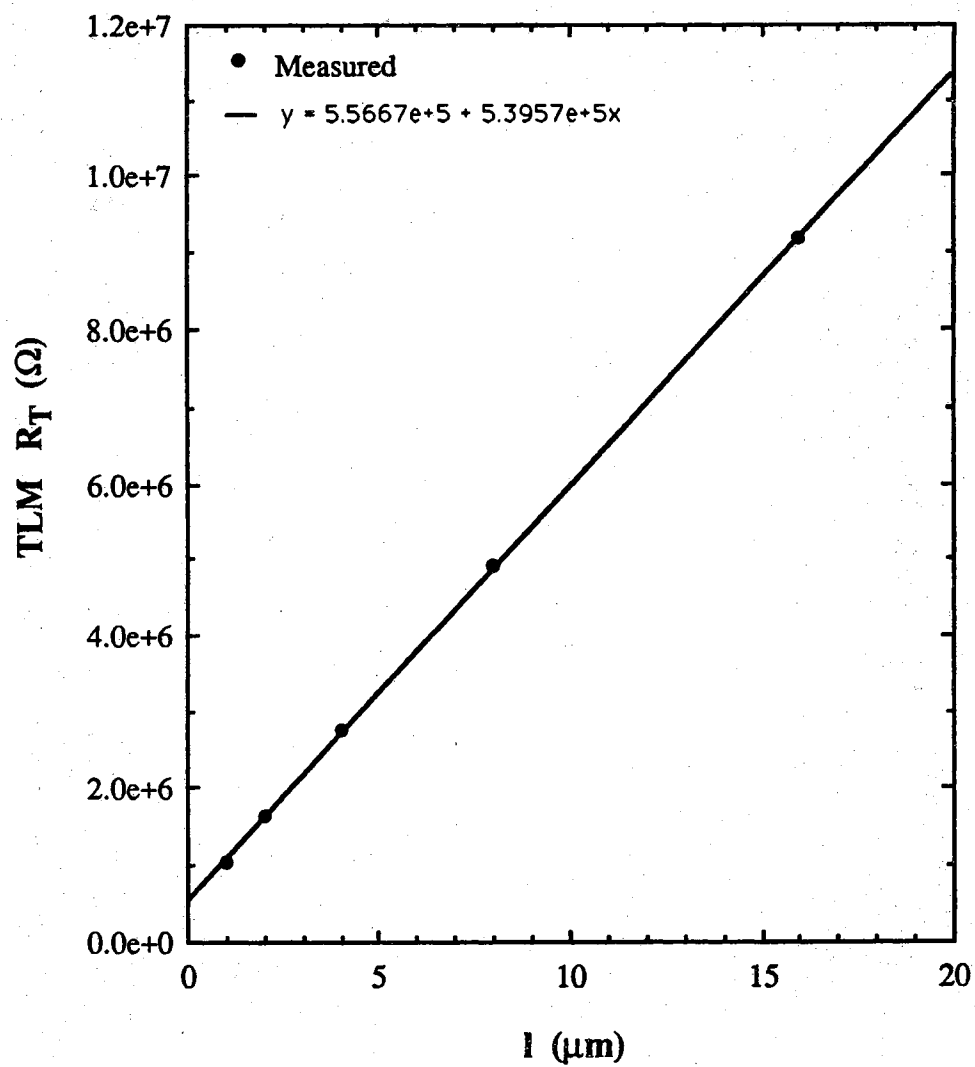
Figure 5.10 Resistance vs. contact spacing of an Al-Si/n^+ a-Si:H TLM pattern.

Si:H films [49]. Assuming the metalization process does not change the film sheet resistance and $d \gg L_T$, then the x-intercept of the linear fit gives a transfer length L_T of 0.52 μm. This corresponds to a specific contact resistance

$$\rho_c = R_{s(impl)} L_T^2 = 0.29 \ \Omega \cdot cm^2 \ . \tag{5.7}$$

The ρ_c value is in a reasonable range in comparing with the ρ_c vs. resistivity chart given by Kanicki [54]. The lower ρ_c in the present case is probably due to contact annealing after the metalization step. If we are looking at the expanded region of Figure 5.8, we can see that the $R_{on} W$ vs. L curves merge at $-l_0 = -5.2$ μm which gives to a gate-voltage independent parasitic resistance $(R_p W)_0$ of 314.7 $\Omega \cdot cm$. This would correspond to the contribution from the S/D n^+ a-Si:H layers and Al-Si/n^+ a-Si:H contacts when the maximum effective contact length l_{ec} has been reached. In a first guess, if we assume that $l_{ec} = l_0/2$ the specific contact resistance can be estimated by

$$\rho_{ec} = \frac{1}{4}(R_p W)_0 l_0 = 4.1 \times 10^{-2} \ \Omega cm^2 . \tag{5.8}$$

The estimated value appears much smaller than the independently measured one. This probably indicates that the actual current flux is much more spread out over the contact because of the heavily doped n^+ a-Si:H bulk layer. Indeed, the maximum effective contact length can be calculated by

$$l_{ec} = 2(\rho_c + \rho_{c(impl)})/(R_p W)_0 = 19.8 \mu m \tag{5.9}$$

where $\rho_{c(impl)} = R_{s(impl)} t^2$, the contribution from ion implanted layer. The calculated l_{ec} value is exactly the physical contact-window length, which is the ultimate limit for current flow. It should be mentioned that the above agreement can not be universal because the maximum l_{ec} depends upon many parameters including but not limited to the contact geometry, the a-Si:H sheet resistance, the contact resistance and the a-Si:H thickness. In the present case, the exact match is due to the combination of an ion implanted n^+ a-Si:H, a larger source/drain to gate overlap. l_0 may be viewed as a characteristic length for the accumulation channel under the source/drain region. A smaller l_0 means a larger current spreading under the contact and therefore a smaller parasitic resistance. Nevertheless, it is incorrect to simply take $l_0/2$ as l_{ec}. Because of the two totally independent techniques for the extraction of ρ_c, $\rho_{c(impl)}$ and $(R_p W)_0$, this physically sound comparison may verify the reliability of both measurements.

Figure 5.11 shows the gate voltage dependence of the width-normalized parasitic resistance. Clearly, the parasitic resistance is largely modulated by the
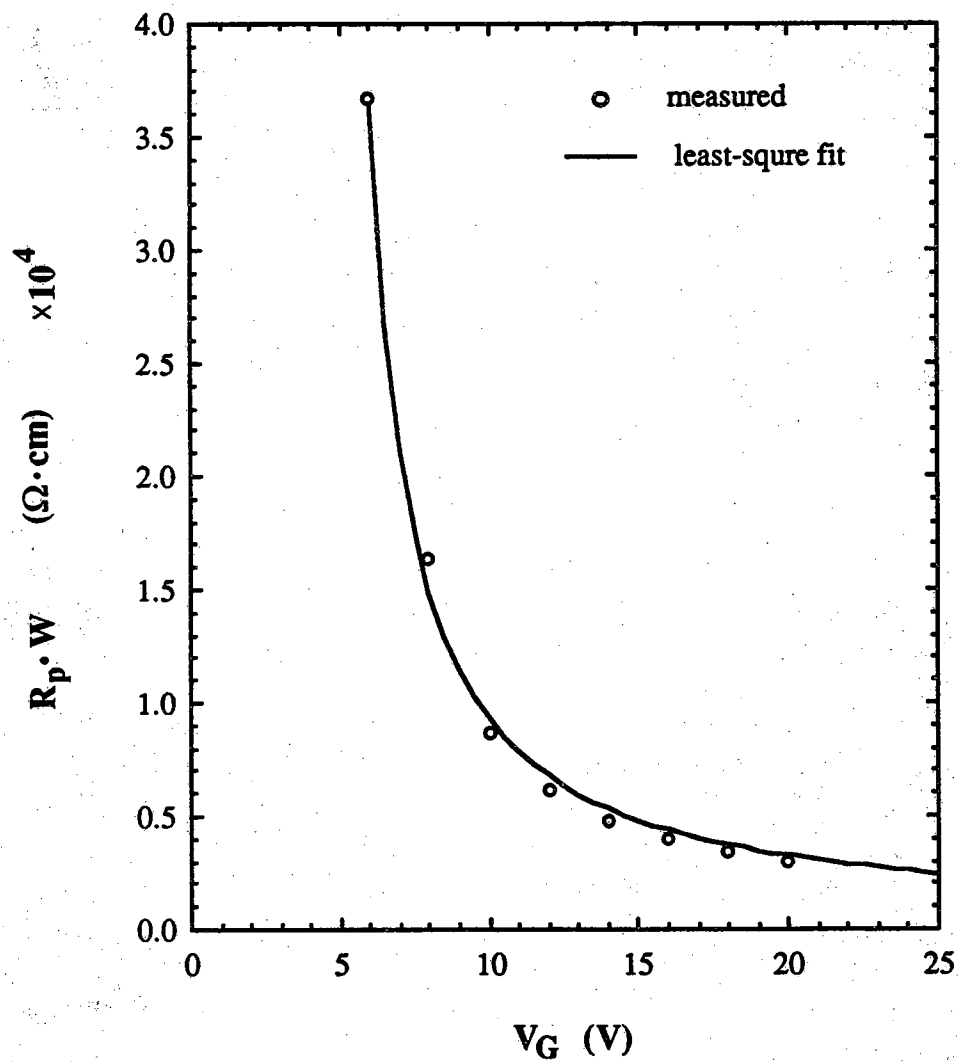
Figure 5.11   Width-normalized parasitic resistance as a function of the gate voltage.

gate voltage because of the presence of source/drain to gate overlaps. An analytical modeling of the parasitics is extremely difficult because of the two-dimensional or distributed nature of the resistance. With the absence of current spreading in the n^+ a-Si:H layer, an inverted-staggered a-Si:H TFT structure can be modeled as a two-layer transmission line [191] with bias dependent sheet resistances. However, because the much larger resistance of the intrinsic a-Si:H layer and the linear I-V characteristics of our ion implanted source/drain contacts, the intrinsic a-Si:H layer over the channel region can be neglected and the implanted region under S/D can be lumped into a effective specific contact resistance ρ_{ec} to the channel. A one layer transmission line model (TLM) [192] is then appropriate as was used by Busta et al. [103]. The parasitic resistance R_p is therefore given by

$$R_p = 2R_{ec} = 2\frac{R_{sc}L_T}{W}\coth(d_c/L_T),\qquad(5.10)$$

where R_{sc} is the sheet resistance beneath the source/drain implant area, d_c is the length of the contacts and $L_T=(\rho_{ec}/R_{sc})^{1/2}$. If we assume that the channel current abruptly terminates at the outer edge of source/drain to gate overlap regions [188], that is, $d_{ec}=d_o$, it can be shown [189] that

$$L_T=[\rho_{ec}\mu_c C_i(V_G-V_{TC})]^{1/2},\qquad(5.11)$$

where μ_c and V_{TC} are field effective mobility and threshold voltage under the overlap regions. They are different from the corresponding parameters under the channel region because of the source/drain implant. Also, the assumption of $d_{ec}=d_o$ may be not true for implanted source/drain regions because the current distributes over a wider range. Accordingly, a parasitic resistance calculation based on these equations seems to be not only difficult but also erroneous.

With the above arguments, an empirical model for the parasitic resistance is obviously an advantage for both of its simplicity and the ease of parameter extraction. Because all lines merge at $L=-l_0$ in Figure 5.8, the parasitic resistance $R_p W$ must satisfy the following equation

$$R_p W = \frac{l_0}{\mu C_i(V_G-V_T)} + (R_p W)_0.\qquad(5.12)$$

That is, the parasitic resistance can be regarded as a minimum effective contact resistance in series with a accumulation channel resistance of length l_0. In a sense, Kanicki et al. has used the same expression by taking $L+l_0$ as the effective channel length. However, the reasoning there was quite different for

this correction term. It was attributed to the presence of a oxide layer at the contact interface. In fact, this work seems to indicate that the l_0 correction term should be always present as long as there is a source/drain to gate overlap. In any sense the second term in equation (5.8) is relatively small at not too large a gate voltage. Therefore, the $R_p W$ vs. V_G data should be fitted quite well to the first term. The least-square curve fit is shown as the solid line in Figure 5.11. This results in a threshold voltage V_T of 4.56 V and a field effect mobility μ of 0.17 cm^2/Vs. These values are physically very reasonable for the n^+ region because of the ion implantation which should reduce both V_T and μ.

5.4 Source/Drain to Gate Overlap Dependence

In Section 5.3, we only investigated the channel length dependence of TFT performance with fixed source/drain to gate overlap d_0. Based on those arguments, the source/drain parasitic resistance should also depend upon d_0 because it will affect the current distribution under the contact. As an illustration, Figure 5.12 shows the TFT output characteristics for three different d_0 values. Apparently, the I_D dependence on d_0 is very similar to its dependence on channel length as given in Figure 5.4. At a drain voltage of 25 V, the drain current reduction is 48% as d_0 is decreased from 2 μm to 0.5 μm. Clearly, the parasitic resistance is indeed increased as the overlap d_0 is decreased.

For comparison, the MOSFET square-model saturation characteristics are also given in Figure 5.13. In general, the apparent field effect mobility is decreased as the overlap d_0 is reduced. The apparent threshold voltage is constant (5.9 V) for d_o between 4 μm and 1 μm, but is 7.9 V for d_0=0.5 μm. The apparent mobility is reduced from 0.38 μm at d_0=4 μm to 0.25 cm^2/Vs at d_0=0.5 μm. Because of the large curvature at d=0.5 μm, the linear-fitted values may not be well represented.

Because the effect of parasitic resistance is much more severe in the linear region than in the saturation regime, the TFT ON resistance has also been measured as was done in the last section for devices with constant W/L ratio but different overlaps d_0. However, because the channel length is fixed for each overlap dimension, the parasitic resistance was obtained by subtracting the channel resistance from the total ON resistance. This may not give much error as long as the TFTs are well turned on. In general, the device parasitic resistance decreases with increasing gate voltage and increasing source/drain to gate overlap. Figure 5.14 illustrates the typical gate voltage dependence of the parasitic resistance R_p. At larger gate voltages R_p begins to saturate. Also, the
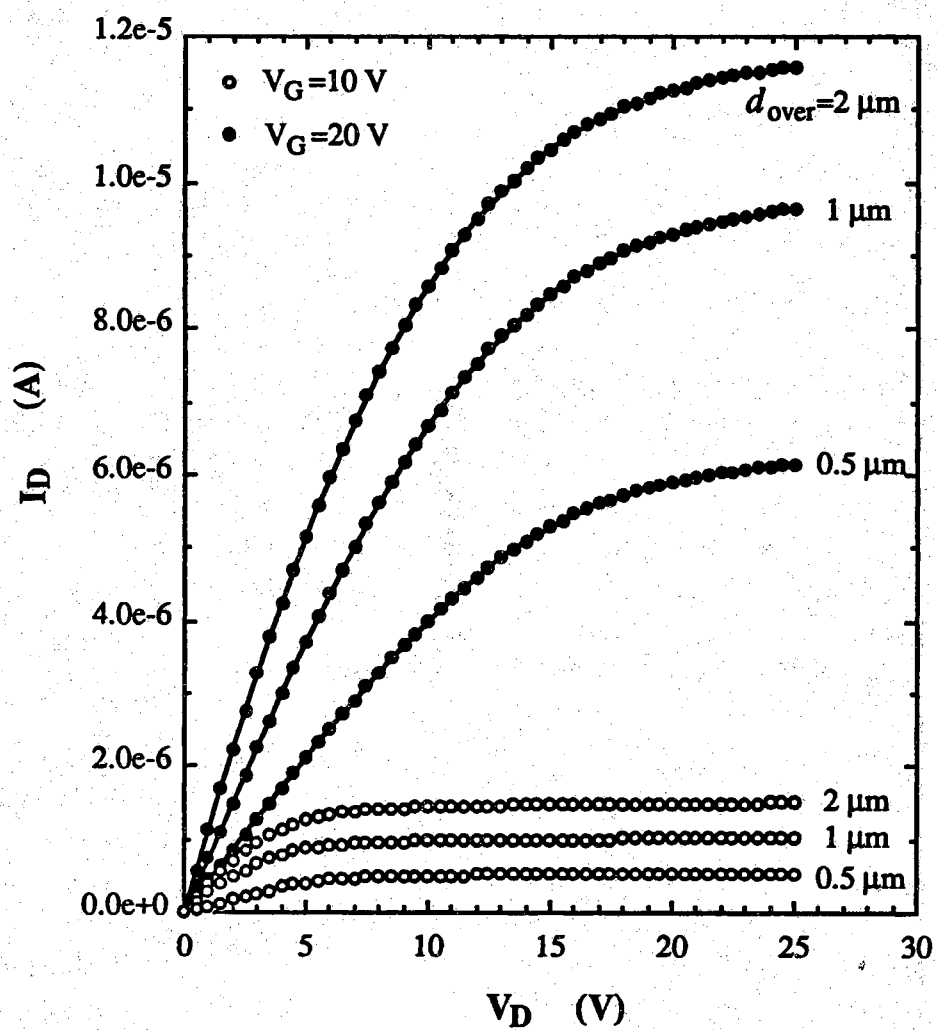
Figure 5.12 a-Si:H TFT output characteristics for different source/drain to gate overlap d_o dimensions. W/L=100/10.
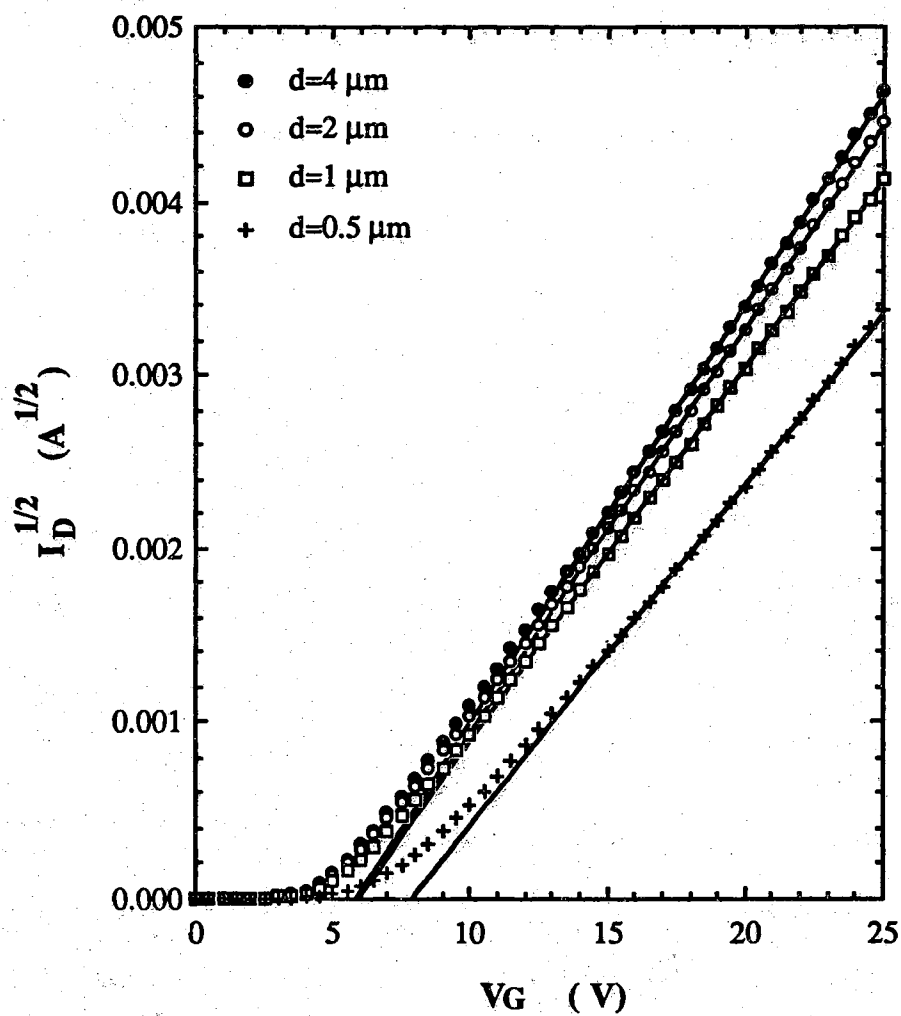
Figure 5.13   A square-root plot of TFT saturation characteristics $(V_D = V_G)$ for different source/drain to gate overlap d_o dimensions. W/L=100/10.
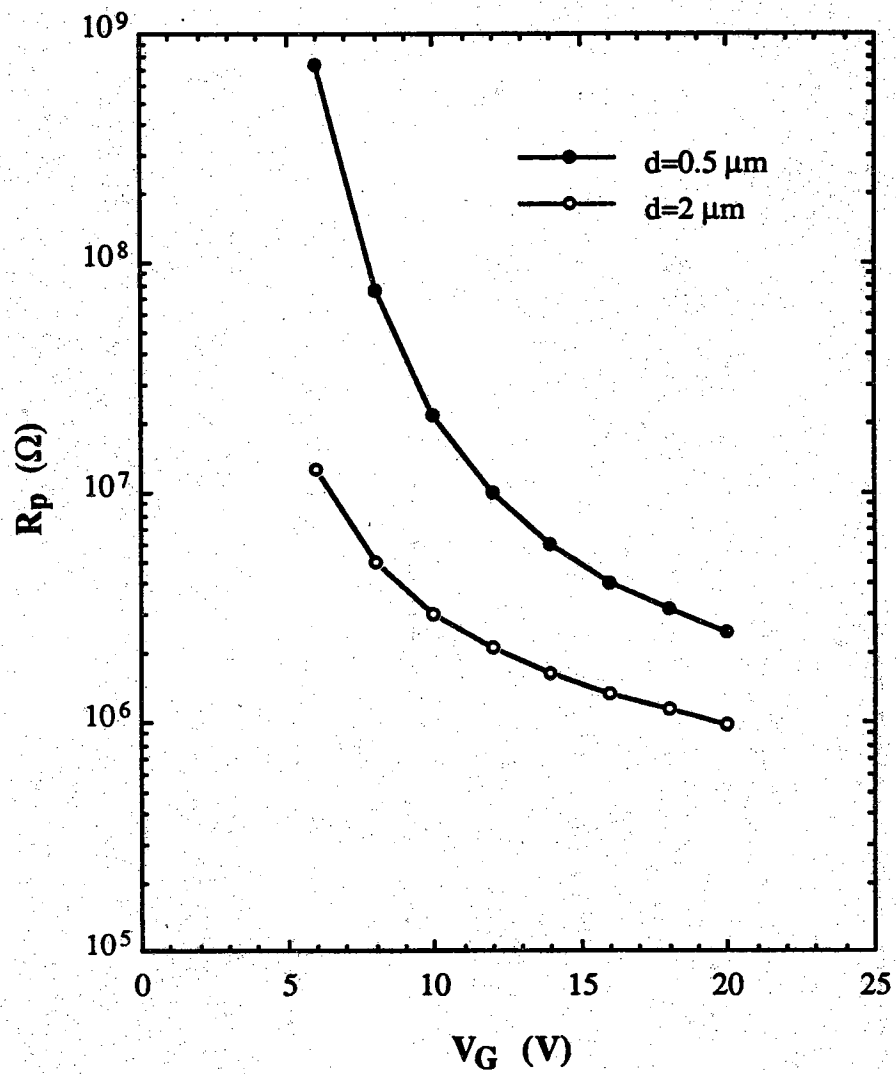
Figure 5.14   Parasitic resistance vs. gate voltage for two different source/drain to gate overlap dimensions. W/L=10.

R_p vs. d_o curves begin to level off above about 4 μm as shown in Figure 5.15. From the discussions in Section 5.3, the dependence on gate voltage V_G and overlap d_0 can be easily understood qualitatively. The apparent saturation of R_p above d_0=4 μm indicates that there is a characteristic length as previously treated [188].

5.5 Summary

In conclusion, the source/drain parasitic resistance effect of inverted-staggered a-Si:H TFTs has been experimentally studied for different gate lengths and source/drain to gate overlap dimensions d_0. For a channel length less than about 30 μm, the apparent field effect mobility decreases with decreasing channel length and d_0. Remarkly different from reported, however, the apparent threshold voltage only changed a small amount with channel length. This has been attributed to an ohmic parasitic resistance because of the implantation used to form the n^+ region. By measuring the sheet resistance and specific contact resistance in the same die as the TFTs, a comparison is made to delineate the parasitic resistance components. It is believed that a much clearer physical picture has been presented in regarding to its gate voltage dependence. Specifically, the sheet resistance of the n^+ region and the Al-Si/n^+ a-Si:H contact contribute a small value to the total parasitic resistance. The spreading of current under the source and drain contacts is much more critical. The advantage of both the ion implantation and the source/drain to gate overlap is to make the current distributed over a wider contact area and thus reduce the parasitic resistance. However, there is a characteristic length for the overlap, above which no influence was observed. For a constant overlap, the parasitic resistance can be viewed as a gate voltage-modulated channel resistance in series with a constant minimum contact resistance.
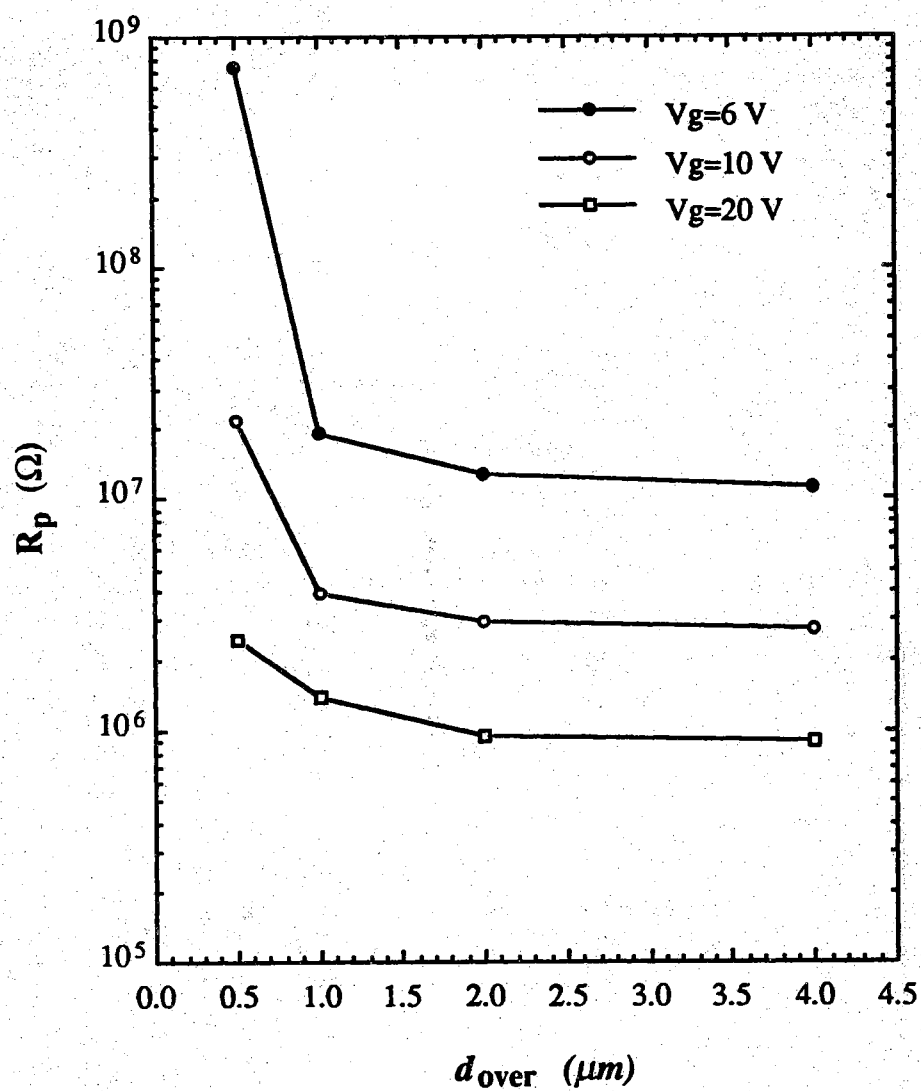
Figure 5.15 Parasitic resistance vs. source/drain to gate overlap dimensions at three different gate voltages. W/L=10.

CHAPTER 6
CONCLUSIONS AND RECOMMENDATIONS

6.1 Conclusions

This thesis consists of the technology development and source/drain parasitic resistance study of a-Si:H TFTs. The investigation began with the development of a high quality $a-SiN_x:H$ gate insulator. Its real performance was then tested in a-Si:H TFTs and its further optimization was performed against deposition rf power and an NH_3 plasma treatment. Also an integral part of the research was concerned with anomalous failure mechanisms of both inverted staggered and normal staggered a-Si:H TFTs. The relationship between plasma processing conditions, device design and Cr gate corrosion were analyzed to postulate a possible electrochemical corrosion mechanism. With the above advances and understanding, new TFT and test device structures were then designed to investigate the effect of source/drain parasitics resistance. A set of four mask levels were used to fabricate these devices. Important parameters such as total parasitic resistance, contact resistance and sheet resistance were then extracted from simple electrical characterizations.

High quality $a-SiN_x:H$ films were achieved using an improved set of optimized deposition parameters. These parameters consisted of the rf power level and inlet gas compositions. a-Si:H TFTs using this gate nitride showed excellent characteristics with both a high current ON/OFF ratios and a negligible amount of hysteresis. This investigation indicated that N-rich nitride was obtained by using a higher rf power level and by adding N_2 to the inlet gas mixture. These nitrides had both a low leakage current and a better interface with a-Si:H, as evidenced by measurements of MIM structures and by the TFT subthreshold and field effect mobility results. The effect of NH_3 plasma treatment is two fold since both radiation damage and a nitridation reaction occurred. First, the plasma treatment degraded the TFT mobility, subthreshold slope and threshold voltage by creating more interface traps and

charged centers. Second, it improved the TFT stability against temperature and gate field stress. Therefore, a compromise had to be made between TFT speed and stability if an NH_3 treatment of the gate nitride was to be used.

The a-Si:H TFT failure mechanisms was first discovered in the normal staggered TFT configuration where the gate Cr was destroyed as soon as a gate voltage exceeded about +6 V. Later it was found that inverted-staggered TFTs also failed in the same way but at a slower rate. This prompted a systematic investigation of the failure mechanism for both a fundamental understanding and for its prevention. By comparing the corrosion behaviors of differently processed capacitors, at a constant relative humidity of 45%, it was found that the corrosion was largely promoted by the CF_4 plasma exposure of the Cr during the fabrication. Also the distance between the Cr films, which served as an anode and a cathode, was very critical. Based on these results, it was proposed that the electrochemical cell is coupled via device periphery and the continued fast growth of corrosion in the plasma exposed case is caused by the chemical condensation of water due to deliquescent corrosion products.

The effect of source/drain parasitic resistance R_p has been experimentally studied. The observations indicated that parasitic resistance will be an important factor for devices with a channel length of less than about 30 μm. In general, the apparent field effect mobility decreases with decreasing channel length. However, the apparent threshold voltage is relatively constant. This has been attributed to a ohmic parasitic resistance due to the use of an ion implanted n^+ region. The results showed that the limiting component is the current spreading resistance. In this regard, both the source/drain ion implantation and source/drain to gate overlap reduce the total parasitic resistance.

6.2 Recommendations for Future Research

Another important aspect of the source/drain contacts is their injecting properties. For unipolar device operation, it is desirable that the contacts inject one type of carriers only. In this way the "on" and "off" conditions are very well defined, which enhances the on/off current ratio. However, the high-level injection of both electrons and holes is necessary for ambipolar a-Si:H TFTs. Ion Implanted source/drain region usually shows one type of carrier injection. It was only found recently that a-Si:H TFTs with boron implanted source/drain also showed ambipolar behavior. The on current for n-channel operation essentially stayed at the same level as the phosphorus implanted devices while the on current for p-channel operation was greatly enhanced. It is

injected into the channel region due to large number of R-G centers at the P^+/i a-Si:H interface. But the non-blocking characteristic for electrons is certainly related to the ion implantation conditions and the film thickness.

To obtain an unipolar p-channel a-Si:H TFT by suppressing the electron current or to improve the ambipolar characteristics, it is necessary first to understand the underlying physics and fabrication conditions resulting its behavior. It is recommended that an investigation is performed to determine the physical mechanism, both for P^+ and for N^+ source-drain contacts. Experimental work involves the variation of ion implantation conditions or the thickness of the implantation caping layer. A p^+-n diode could be made to examine the reverse biased leakage.

It would be very interesting and of technological importance to know the relationship between the parasitic resistance and the a-Si:H layer thickness or alternatively the ion implantation conditions. Systematic study of this effect could lead to knowledge of the current transport mechanism under the contacts and the effective contact areas. A modeling effort is needed to quantify the source/drain parasitic resistance. It is believed that our devices behave quite differently from those employing a plasma-deposited n^+ a-Si:H layer, especially in regarding to the current spreading under the source/drain overlap regions. It also can be seen if the anomalous ambipolar behavior mentioned in last subsection depends on the i-layer thickness. The mask set for all of the above mentioned studies now is available and no further changes are needed. For inverted-staggered a-Si:H TFT structures, a total of six mask levels has been designed. The level 6 mask is used specially for making dual-gate devices. However, the passivation mask (level 5) should always be utilized. Otherwise, the devices may fail very quickly because of the Cr-gate corrosion mentioned in Chapter 4.

At this stage of development, 2D device simulation becomes very helpful in that it would help to explain the various experimental results described previously and also to get insight of the device physics. The effect of the i-layer thickness, source/drain overlap dimensions could be simulated. At the very least, current vectors or equipotential lines under the source/drain contacts should be obtained to show the current spreading behavior and to identify visually the limiting components of the source/drain parasitic resistance. Based on the simulation results, further improvement of the existing structure and the possible design of new TFT structures can then be made.

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APPENDIX

a-Si:H TFT Run Sheet

1. Oxidize wafer
   (1) Ultraclean Si wafers
       15 min in 1 H_2O_2:H_2SO_4
       5 seconds dip in BHF
       rinse in DI water
       N_2 blow dry
   (2) Wet oxidation
       temperature=1100 ° C
       3 min push in N_2
       30 min H_2 burn oxidation
       3 min pull in N_2

2. Define gate pattern
   (1) Apply adhension promoter HMDS for 10 min
   (2) Apply AZ 1350J-SF positive photoresist
       spin @4000 rpm for 30 seconds
   (3) Softbake resist @90 ° C for 15 min
   (4) Expose gate mask
       exposure time: 7.5 seconds
       exposure mode: HP
   (5) Develop resist
       developer: 1 AZ developer:1 DI
       time: 25 seconds
       rinse in DI: 40 seconds
   (6) Inspect pattern

3. Sputter deposit chromium
   (1) Presputter Cr target for 20 min
   (2) Sputter deposit Cr (~800 Å)
       Ar pressure=6 mT, F.Power=100 W, time=10 min

4. Lift-off Cr
       drop wafer gently into ACE filled beaker
       soak for 10 min
       transfer beaker in USC and keep for 5 min
       DI rinse
       N_2 blow dry

Inspect pattern

5. PECVD SiN$_x$ and a-Si:H deposition
   (1) Deposit SiN$_x$ (~1500 Å)
       N$_2$/NH$_3$/SiH$_4$ flow: 50/50/5 in sccm
       pressure: 650 mT
       temperature: 320 °C
       rf power: 100 W
       time: 10'17"
   (2) Gas change-over
       pump-down (<70 mT)↔50 sccm SiH$_4$ purge (>600 mT)
       for three times
   (3) Deposit a-Si:H (~700 Å)
       SiH$_4$ flow: 50 sccm
       rf power: 6 W
       pressure: 350 mT
       temperature: 260 °C
       time: 18 min

6. a-Si:H and SiN$_x$ definition
   (1) Apply adhension promoter HMDS for 10 min
   (2) Apply AZ 1350J-SF positive photoresist
       spin @4400 rpm for 40 seconds
   (3) Softbake resist @90 °C for 15 min
   (4) Align and expose mask #2
       exposure time: 6 seconds
       exposure mode: HP
   (5) Develop resist
       developer: 1 AZ developer:1 DI
       develop time: 30 seconds
       rinse in DI: 40 seconds
   (6) Inspect pattern
   (7) Hardbake resist @120 °C for 20 min

7. Plasma etching of a-Si:H and SiN$_x$
       rf power: 80 W
       CF$_4$ flow: 20
       prossure: 200 mT
       time: 5 min

8. Source/drain implant definition
   (1) Apply adhension promoter HMDS for 10 min
   (2) Apply AZ 1350J-SF positive photoresist
       spin @4000 rpm for 30 seconds
   (3) Softbake resist @90 °C for 15 min
   (4) Align and expose mask #3
       exposure time: 7.5 seconds
       exposure mode: HP
   (5) Develop resist
       developer: 1 AZ developr:1 DI

develop time: 25 seconds
rinse in DI: 40 seconds
(6) Inspect pattern
(7) Hardbake resist @120°C for 15 min
(8) Repeat steps (2)-(6)

9. Ion implantation
implant: phosphorus
energy: 25 Kev
dose: 1×10^{16}

10. Define source/drain metal pattern
(1) Apply adhension promoter HMDS for 10 min
(2) Apply AZ 1350J-SF positive photoresist
spin @4000 rpm for 30 seconds
(3) Softbake resist @90°C for 15 min
(4) Align and expose mask #4
exposure time: 7.5 seconds
exposure mode: HP
(5) Develop resist
developer: 1 AZ developer:1 DI
time: 25 seconds
rinse in DI: 40 seconds
(6) Inspect pattern

11. Sputter deposit Al-Si (∼900 Å)
Ar pressure: 8 mT
F. power: 100 W
time: 25 min

12. Lift-off Al-Si
30 min ACE soak, 4 min in USC
DI rinse and N_2 blow dry
Inspect pattern

13. Anneal contacts
system: TECHNICS
temperature: 200°C
N_2 flow: 30 sccm
H_2 flow: 45 sccm
Pressure: 500 mT
time: 30 min

14. Electrical characterization