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Study of a New Silicon Epitaxy Technique: Confined Lateral Selective Epitaxial Growth

P. J. Schubert G. W. Neudeck

TR-EE 90-32 May, 1990

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TABLE OF CONTENTS

LIST OF TABLES	
	a de la companya de Esta de la companya d
LIST OF FIGURES	viii
	이는 것 같은 것 같은 것이 가지 않는 것이 같은 것이 있다. 같은 것은 것 같은 것이 같은 것이 같은 것이 같은 것이 같은 것이 같이 있다.
AB51RAU1	·····X1
CHAPTER 1 - INTRODUCTION	1
1.1 Purpose of Work	1
1.2 Brief Description of CLSEG	
1.3 Overview of Thesis	2
CHAPTER 2 - BACKGROUND	
2.1 Design Considerations	3
2.1.1 Scaling of devices and isc	lation 3
2.1.1 Seaming of devices and isc 2.1.2 Advanced devices and isc	lation structures 4
2.1.2 Advanced devices and isc 2.1.3 Three dimensional integr	ation 7
2.1.5 Three dimensional model 2.2. Device Isolation by SOI	7
2.2 Device isolation by Seria	7
2.2.1 Auvantages of Soliming SO	Ψ
2.2.2 Methods of achieving SO	9
2.2.2.1 Duried insulation /	of polycilicop
2.2.2.2 Freelystambation (2.2.2.2 Freitaxial Latoral ($\mathbf{O}_{\mathbf{v}} = \mathbf{v}_{\mathbf{v}} $
2.2.2.3 Epitaxiai Baterar 2.2.3 Requirements for ideal S	OF 13
2.2.3 Requirements for ideal of 2.3 Selective Enitavial Crowth (SI	74
2.3 Delective Epitaxial Growin (El	ariale 14
2.3.1 Deleterity and mask may	rowth 15
2.3.2 Tre-clean and epitaxial g	10w 011
2.3.3 DELECUS III DEG	
2.5.4 Interface properties and (10 V 10 CD
2.4 WIOHVALIONS IOF OLDEG	
2.4.1 Growin studies	ZI
	<u>^</u>

Page

iv

			Page
2.4.3 Advanced device construction	1		22
CHAPTER 3 - PROCESSING	,		23
		· · · · ·	
3.1 Generic Fabrication Sequence		·····	23
3.2 Cavity Construction	,		25
3.2.1 Bottom layer	,		25
3.2.2 Sacrificial layer		• • • • • • • • • • • • • • • • • • • •	26
3.2.3 Top layer			27
3.3 Cavity Layout	• • • • • • • • • • • • • • • • • • • •	•••••	28
3.4 CLSEG Growth Conditions			29
CHAPTER 4 - CHARACTERIZATION C)F CLSEG SILICON	•••••	34
		1997 - 1997 -	
4.1 Growth Properties of CLSEG			34
4.1.1 Seed hole orientation			35
4.1.2 Growth rate			37
4.1.3 Aspect ratio	• • • • • • • • • • • • • • • • • • • •	•••••	44
4.1.4 Faceting		••••••	46
4.1.5 Uniformity		• • • • • • • • • • • • • • • • • • • •	49
4.1.6 Morphology and defects		••••••	51
4.1.7 Cavity end effects		•••••	53
4.1.8 Merged CLSEG	• • • • • • • • • • • • • • • • • • • •		54
4.2 Electrical Properties of CLSEG		••••••	
4.2.1 Device fabrication and layout	t	•••••	56
4.2.2 Measurement techniques	• • • • • • • • • • • • • • • • • • • •		58
4.2.3 Process effects on CLSEG did	odes	••••••	63
4.2.4 MOSFETs in CLSEG		••••••	69
4.2.5 Bipolar transistors in CLSEC	۲ 7		71
4.3 Best Conditions for CLSEG Fabric	cation	••••••	75
CHAPTER 5 - A NOVEL CLSEG BJT D	EVICE	•••••	80
		· · · · · · · · · · · · · · · · · · ·	ana an sin Daoine
5.1 Fabrication of Under-diffused Loca	al-SOI BJTs	•••••	81
5.2 Results of Under-diffused BJT	•••••	•••••	83
5.3 PISCES Computer Simulation	•••••••••••••••	•••••	87

Page

vi

CHAPTER 5 - DISCUSSION	
6.1 Discussion of Results	88
6.1.1 Growth results	
6.1.2 Electrical results	91
6.1.3 Advanced device results	93
6.2 Comparison to Current Technology	94
6.2.1 CLSEG as an isolation technology	95
6.2.2 CLSEG as a device construction tool	97
6.2.3 CLSEG for growth studies	
CHAPTER 7 - CONCLUSIONS	99
7.1 Significance of Results	
7.2 Further Investigation Possibilities	100
7.3 Summary of Thesis	102
	100
LIST OF REFERENCES	104
APPENDIX	115
	121

LIST OF TABLES

vii

Tabl	$\mathbf{e}^{\mathbf{e}}$, where $\mathbf{e}^{\mathbf{e}}$, the second s	Page
4.1.	Comparison of CLSEG lateral growth rate to ELO vertical growth rate	.41
4.2.	CLSEG growth rate versus thickness of top and bottom layers in a barrel reactor at 950° C and 50 Torr	42
4.3.	CLSEG growth rate versus top layer thickness in a pancake reactor at 950° C and 150 Torr	43
4.4	CLSEG diode ideality factors versus process and design parameters	64
4.5	Measured parameters from MOSFETs in CLSEG, homoepitaxy, and substrate silicon material	72
4.6	Measured parameters from bipolar junction transistors in CLSEG, homoepitaxy, and substrate silicon material	78
5.1	Measured parameters from under-diffused bipolar junction transistors in CLSEG material compared to a non-under-diffused device in homoepitaxy material	85
6.1	Mean free path of $SiCl_2$ at various deposition conditions for selective epitaxial growth	90

LIST OF FIGURES

Figu	Page
2.1	Cross section of LOCOS isolation technique showing bird's beak6
2.2	Cross section of trench isolation technology
2.3	Cross section of SIMOX buried oxide SOI technology10
2.4	SOI by polysilicon recrystallization (a) before and (b) during scanning with a laser heat/light source10
2.5	Epitaxial Lateral Overgrowth (ELO) technique (a) showing (b) merging and (c) planarization12
2.6	Sidewall Gate Controlled Diode after Klaasen [101]20
3.1	CLSEG process flow24
3.2	Perspective view of CLSEG cavity showing via hole placement
3.3	Layout of masks used to form a CLSEG cavity
4.1	Electron Channeling Patterns of (a) CLSEG, (b) homoepitaxy, and (c) substrate silicon
4.2	Growth rate of ELO versus $[pp_{HCl}]^2/[pp_{DCS}]$
4.3	Growth rate of ELO versus masking oxide thickness
4.4	CLSEG growth rate versus cavity depth (width)45
4.5	SEM cross sections showing typical CLSEG films47
4.6	SEM cross sections showing high aspect ratio CLSEG films

viii

ix

4.7	SEM cross section showing ELO overgrowth at end of CLSEG cavity .50
4.8	Micrograph of empty cavities prior to CLSEG growth, showing extreme deflection (top) and no deflection (bottom)52
4.9	Photomicrograph of CLSEG slabs showing end effect55
4.10	SEM cross section of merged CLSEG with ELO in background56
4.11	Minimum layout of diode and cross section in (a) CLSEG, (b) homoepitaxy, and (c) substrate material
4.12	Minimum layout of MOSFET and cross section in (a) CLSEG, (b) homoepitaxy, and (c) substrate material
4.13	Minimum layout of bipolar transistor and cross section in (a) CLSEG, (b) homoepitaxy, and (c) substrate material
4.14	Ideality factor versus post-epi anneal temperature with the bottom oxide removed and intact, for CLSEG grown in a pancake reactor at 950° C and 150 Torr
4.15	Histograms of ideality factor (a) and leakage current (b) with and without the bottom oxide layer removed for barrel-grown samples at 1000° C and 50 Torr, with nitride on oxide as the top layer, and a cavity height of 0.86 microns70
4.16	Transistor output curves (a) and plot of $ln(I_D)$ versus gate voltage (b) for MOSFETs in CLSEG (left) and homoepitaxy (right) material73
4.17	Gummel plot (a), β versus I _C curve (b), and transistor output curves (c) for representative vertical bipolar transistor fabricated in local-SOI CLSEG material76
4.18	PISCES simulation of I_C versus V_{CE} output curve trace with V_B =0.6 volts for the CLSEG BJT structure of Figure 4.17. QF is the underside oxide interface state density in #/C-cm ² , and T is the CLSEG thickness in microns

Figure

Page

х

5.1	 Key CLSEG BJT process steps for the underside diffusion proc (a) CLSEG with top and bottom dielectric layers removed, (b) plasma deposited masking oxide, and (c) after N⁺ deposition and drive. 		
• * •			
5.2	Perspective drawing of under-diffused vertical bipolar transistor in CLSEG local-SOI material	84	
5.3	Transistor output curves for under-diffused vertical bipolar transistor in CLSEG local-SOI material	86	
6.1	Process for whole-wafer SOI using CLSEG	96	
7.1	One mask-step CLSEG process	101	

ABSTRACT

Schubert, Peter J. Ph.D., Purdue University, May 1990. Study of a New Silicon Epitaxy Technique: Confined Lateral Selective Epitaxial Growth. Major Professor: Dr. Gerold W. Neudeck

This work describes a significant new advance in the technique of silicon selective epitaxy called Confined Lateral Selective Epitaxial Growth (CLSEG). CLSEG is a method for forming thin films of single crystal silicon on top of an insulating layer or film. Such thin films are generically termed Silicon-On-Insulator (SOI), and allow dielectric isolation of integrated circuit elements, making them more efficient (faster with lower power), more resistant to radiation, and smaller than conventional integrated circuits. ionizing radiation than CLSEG offers advantages over current conventional integrated circuits. methods of achieving SOI by being easily manufactured, inherently reproducible, and having greater design flexibility. CLSEG is also adaptable to vertical stacking of devices in a circuit, in what is called three-dimensional integration, for even greater reductions in area. In addition, CLSEG can be used for a wide variety of sensor and micromachining application. This thesis describes the design and development of CLSEG, and compares it to the current state of the art in the fields of SOI and Selective Epitaxial Growth (SEG).

CLSEG is accomplished by growing silicon selective epitaxy within a cavity; which is formed of dielectric materials upon a silicon substrate. The resulting SOI film can be made as thin as 0.1 micron, and tens of microns wide, with an unlimited length. In particular, there is now strong evidence that surface

xi

diffusivity of silicon adatoms on the dielectric masking layers is a significant contributor to the transport of silicon to the growth surface during SEG.

CLSEG silicon material quality is evaluated by fabricating a variety of semiconductor devices in CLSEG films. These devices demonstrate the applicability of CLSEG to integrated circuits, and provide a basis of comparison between CLSEG-grown silicon and device-quality substrate silicon. Then, CLSEG is used to fabricate an advanced device structure, verifying the value and significance of this new epitaxy technique.

In the final two chapters, CLSEG is evaluated as a technology, and compared to the current state of the art. Then, a method is presented for forming CLSEG with only one photolithography step, and a process is described for making a SOI film across an entire silicon wafer using CLSEG. These techniques may indicate the feasibility of using CLSEG for three dimensional integration of microelectronics. It is hoped that this work will establish a firm basis for further study of this interesting and valuable new technology.

CHAPTER 1

1

INTRODUCTION

1.1 Purpose of Work

The purpose of this work is to introduce a new technology for the fabrication of next-generation of SOI type integrated circuits. The technique developed for this purpose can be used as an inter-device isolation method; or as a tool for the construction of advanced semiconductor devices. In addition to accomplishing these goals, this technique has also proved to be a valuable research method for the study of silicon selective epitaxy. It is the objective of this thesis to fully explain the concept, development, and characterization of this new technology; and to pave the way for future studies.

1.2 Brief Description of CLSEG

The name Confined Lateral Selective Epitaxial Growth (CLSEG) [1] has been chosen to identify the key features of this structure and technique. By creating a cantilevered dielectric thin film above an oxidized silicon substrate, a cavity is formed which has insulating materials for its walls. From a small seed hole to the substrate deep within, the cavity can be selectively filled with singlecrystal silicon to form thin but wide slabs of Silicon-On-Insulator (SOI) material.

CLSEG is a low temperature technique which uses only conventional process equipment. It is adaptable to MOS or bipolar technologies, and has the structural versatility to be applicable to three dimensional integration, micromachining, and advanced device concepts. This makes CLSEG an important technological choice for tomorrow's SOI type of integrated circuits.

1.3 Overview of Thesis

Chapter 2 presents the background needed to adequately explain the need and value of CLSEG technology. The trend towards more densely-packed integrated circuits through circuit and device design is discussed briefly to set the stage for this work. In-depth reviews are given for SOI device isolation and Selective Epitaxial Growth (SEG) because they are crucial to the understanding of CLSEG; and are the root technologies from which CLSEG is spawned.

In Chapter 3, the process and design techniques for successful CLSEG are laid out. Chapter 4 presents the characterization results of this work; and is divided into growth studies and electrical evaluation. At the end of this chapter is a section describing the near optimal conditions for producing device-ready CLSEG.

Chapter 5 introduces an advanced BJT device structure created using CLSEG, as and example of the wide array of applications for this technique. In Chapter 6 the results are discussed in light of the background material of Chapter 2. Finally, Chapter 7 presents a summary of the results, and points out several possible avenues for further investigation.

CHAPTER 2

3

BACKGROUND

2.1 Design Considerations

The integrated circuit industry continually seeks to improve the performance, functionality, and cost of their products to satisfy consumer demand for electronics. With the advent of planar technology in the early 1960's, discrete devices gave way to integrated circuits. This advance dramatically improved both functionality and cost; and later performance, as understanding of surface science improved. This integration also required that individual components and devices be isolated from one another to prevent current leakage and capacitive coupling. From this point, continued advances in silicon have been made in three ways: (1) scaling of devices and device isolation; (2) new designs of circuits, devices, or device isolation; and (3) stacking of layers of integrated circuits for three dimensional integration. Each of these avenues for improvement are considered briefly below.

2.1.1 Scaling of devices and isolation

Scaling of devices and isolation is the reduction of all physical dimensions by a linear factor α ($\alpha > 1$). In MOS technology, for example, both the length and width of the channel region are reduced by $1/\alpha$, and gate oxide thickness is made $1/\alpha$ times thinner. To preserve circuit functions without redesign, and to maintain overall power density on a chip, these scaling shrinks require an increase of the doping level (by α) and a reduction of $1/\alpha$ for both current and voltage [2]. The benefits of scaling are that packing density (gates/area) increases by α^2 , and the power-delay product (power/gate × delay/gate) decreases by $1/\alpha^3$ for MOS and $1/\alpha^2$ for bipolar technologies. However the tradeoffs of scaling are that parasitic capacitances and resistances increase in significance. Current density in interconnect lines increases, leading to reliability problems; and device "off" current increases, making circuits more susceptible to soft errors and narrowing dynamic operating ranges [2]. A further limit to scaling when device sizes approach carrier wavelengths [3] is that classical mathematical models to describe individual devices no longer apply. Circuits and devices must be treated as distributed or quantum systems rather than lumped elements. This makes circuit simulation, layout, and parameter extraction much more difficult and costly.

4

Semiconductor fabrication technology also imposes limits to scaling. Such processing difficulties as: layer to layer misregistration; defects due to airborn particulates, [4] and catastrophic breakdown from electrostatic discharge can offset the advantages of scaling. Further advances in conventional microfabrication are becoming increasingly difficult. Because of this, more study is being turned to novel device structures and isolation technology.

2.1.2 Advanced device and isolation structures

Perhaps the most significant, but less predictable contributor to advances in integrated circuits are innovative circuit designs, new device structures, or novel device isolation schemes. A classic example is the advent of the onetransistor DRAM cell which made possible the 256 kbit DRAM. This involved both a new circuit design and a novel device structure. More recently, advanced bipolar devices, such as the Super Self-Aligned Technology (SST) [5] reduce the number of masking levels needed for fabrication, reduce device area and parasitics, and hence operate at higher speeds, than conventional bipolar transistors. Of most interest to this thesis are advances in isolation technology. At the present stage of development, it is improvements in device isolation that show the greatest potential for further improvements in packing density, speed, and functionality.

The function of inter-device isolation is to separate the electrical operation of adjacent devices. This greatly simplifies circuit design, layout, and simulation; makes circuits more efficient (lower power, wider dynamic range), and increases the threshold for latch-up. Latch-up is sustained in bipolar or CMOS planar technologies when a parasitic npnp structure is biased so that it's composite gain ($\beta_{npn} \times \beta_{pnp}$) exceeds unity. The onset of latch-up usually requires that the circuit be powered down to reset it. Thus, it is highly desirable to avoid latch-up, and this is an important consideration when evaluating isolation technologies.

Historically, devices were isolated by diffused p-n junctions, because of its compatibility in processing. Junction isolation is terribly inefficient due to large area consumption, large parasitic capacitance (dielectric constant of silicon junction capacitors is $\epsilon = 11.7$), and non-negligible leakage currents. Latch-up could be prevented by increasing doping levels and device-to-device spacing, yet at the expense of the other factors.

Currently, the most common isolation technique is some variation on the LOCOS (LOCal Oxidation of Silicon) method. In LOCOS the active device areas are covered with silicon nitride, so that during an extended oxidation step, a thick oxide is formed only in the field regions. An implant is usually placed in the field regions prior to oxidation to increase the MOS inversion voltage there. This prevents interconnect lines from inadvertantly creating leakage paths between devices.

LOCOS suffers from two limitations. First, leakage paths still exist through the substrate, allowing the possibility of latch-up. Second is the well-known "bird's beak" phenomenon at the transition between the field oxide and the active region (see Figure 2.1). This is caused by oxygen diffusion under the nitride mask, growing unwanted oxide there, and lifting up the nitride. This results in an effective loss of 0.5 to 1.5 microns on all sides of the active device region. This area loss can be reduced by using the SILOS (Sealed Interface Local Oxidation of Silicon) [6] technique, but at the expense of stress in the substrate.

With advances in Reactive Ion Etching (RIE) and low pressure chemical vapor deposition (LPCVD) came the advent of trench isolation, shown in Figure 2.2. The near-vertical walls of the trench etch allow device spacing almost as small as lithographical considerations will allow, and puts a dielectric wall between adjacent devices. But trench isolation technology has some serious drawbacks. When the trench walls are oxidized, stress induced at the inside corners [7] generates defects [8]. Leakage currents along trench sidewalls is another serious problem with trench isolation [9]. Finally, because the substrate is still in contact with the active device region, high junction capacitance and latchup are still a problem.

A similar technology to trench is SEG isolation [10] where seed holes are etched into thick oxides and refilled with Selective Epitaxial Growth (SEG). This allows greater flexibility in processing, and eliminates oxidation- induced



6

Figure 2.1 Cross section of LOCOS isolation technique showing bird's beak.



P SUBSTRATE

Figure 2.2 Cross section of trench isolation technology.

stress defects; but still suffers from most of the same problems as trench isolation.

Perhaps the ultimate isolation technology is SOI in which active device regions are completely surrounded (even underneath) by high-quality dielectric material. In this way, latch-up can be completely eliminated, and capacitances are greatly reduced since the dielectric constant of silicon dioxide is $\epsilon=3.9$. SOI is discussed in detail in a later section.

2.1.3 Three dimensional integration

As with Sullivan's skyscrapers of the early 1900's, when area is at a premium, one expands upwards to create more volume. This is the concept for 3-D integration, where devices are built in stacked layers of semiconductor material - separated by thin film insulators. 3-D integration is very attractive for putting more circuit functions an a chip without increasing the area or the chip pinout. Also, device interconnections can be made more efficiently, and circuit speed will increase. Current problems with 3-D integration include: power dissipation; thermal redistribution of existing junctions; and crystal quality of successive layers. If these difficulties can be adequately addressed, 3-D integration could be as significant an advance as planar technology was 30 years ago.

2.2 Device Isolation by SOI

The defining feature of Silicon-On-Insulator (SOI) is a thin film of singlecrystal silicon formed on an insulating layer. The SOI region can be localized for individual device isolation, or extend over an entire wafer. In various SOI methods, the underlying insulating layer can be the substrate itself, or be formed on top of another silicon layer or a silicon substrate.

2.2.1 Advantages of SOI

SOI has tremendous promise for future device isolation because of the following advantages:

(1) latch-up can be completely eliminated.

(2) parasitic capacitances are very low [11].

(3) Isolation leakage currents negligible.

(4) very high packing density.

(5) no p-well or n-well drive-ins.

(6) radiation hardness greatly improved [12].

(7) Higher junction breakdown voltages [13].

(8) higher MOSFET mobility and lower subthreshold slope [3].

(9) less short channel effects in MOSFETs [2].

(10) applicable to 3-D integration (in some cases).

One of the main advantages of CLSEG is its use as an SOI isolation technology. Thus, it will be instructive to review several of the most promising SOI methods in the current state-of-the-art.

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2.2.2 Methods of achieving SOI

There are currently six or more approaches to SOI in the technical literature. Of these, wafer bonding and etch-back [13, 14, 15], Oxidation of Porous Silicon (OPS) [16], and heteroepitaxy of silicon on insulator [17, 18, 19, 20] are either too difficult to fabricate, too early in development, or result in deficient material quality, and will not be considered here. The SOI technologies with the most promise are buried insulator, polysilicon recrystallization, and Epitaxial Lateral Overgrowth (ELO). These three will be considered in detail below.

2.2.2.1 Buried insulator / SIMOX

A powerful method for realizing SOI is by the formation of buried insulators in silicon wafers by large dose, high energy ion implantation. For the case of oxygen as the implant species, this technique is called SIMOX for Separation by Implanted Oxygen [21]. Beginning with a bare silicon wafer, an oxygen or nitrogen dose of roughly 2.0×10^{18} atoms/cm² is implanted at 150 keV or greater [22]. This energy is sufficient to place the peak of the implant distribution about 300 nm beneath the surface (see Figure 2.3). After a high temperature anneal, the implanted species reacts with silicon to form either SiO₂ or Si₃N₄. The SOI film left on top is typically 100 nm thick, which is too thin for most SOI applications. This requires an epitaxy step to make a SOI film of adequate thickness, and to improve the crystal quality.

MOSFETs built in buried insulator films have majority carrier mobilities nearly equal to that of substrate devices [23, 24]. Vertical Bipolar Junction Transistors (BJT) with common emitter current gains (β) of up to 100 have also been realized with buried insulators [25, 26].

The problems with buried insulators stem from the inordinant damage caused by such an implant. MOSFET leakage currents of 50 pA per micron of channel width have been reported [24], more than 2 orders of magnitude larger than for bulk devices. Minority carrier lifetimes in SIMOX SOI films are typically one order of magnitude smaller than for standard device wafers [21], and the surface recombination velocity is two orders higher.

Although buried insulator SOI technology is a somewhat conventional process, its most severe limitations are the long implant times, the high temperature anneal, and the modest crystal quality. Wafer warpage is also significant in buried insulator wafers. This leads to lithography problems such as run-out, linewidth variations, and etch non-uniformities. These factors also preclude the used of buried insulator technology from 3-D integration [12].

2.2.2.2 Recrystallization of polysilicon

Another SOI technique that is very popular is the recrystallization of polycrystalline (or amorphous) silicon films. Typically, a seed hole is formed through a thermal oxide on a silicon wafer, and polysilicon is deposited, as shown in Figure 2.4. Recrystallization is accomplished with a heat/light source such as a laser, moving strip heater, or stationary lamp. The polysilicon is melted, and upon re-solidification, adopts the crystal orientation of the substrate. A thermal gradient or a moving heat/light source then serves to extend the single crystal region over the oxide as shown at the bottom of Figure 2.4. With recrystallization, SOI silicon thicknesses of 0.5 microns to several microns thick can be formed, can be extended over very great distances laterally, and can cover non-planar topography as well [27].

At its present stage of development, undoped recrystallized silicon SOI films have lifetimes 2 orders of magnitude lower than in bulk wafers [21]. MOSFETs built in such films have mobilities in the same range as substrate devices [28, 29, 30], but have leakage currents up to 20 nA/ μ m [31]. Dislocations occur every one to several microns [32,33] making circuit fabrication very difficult. BJTs in recrystallized films have β 's up to 75 [31], but ideality factors at the emitter base junctions range from $\eta=1.2$ [29] to 1.42 [33]. This indicates the dominance of recombination due to bulk defects. A further problem with these defects is preferential doping [28], leading to further reductions in device yield and performance.



Figure 2.3 Cross section of SIMOX buried oxide SOI technology.



Figure 2.4 SOI by polysilicon recrystallization (a) before and (b) during scanning with a laser heat/light source.

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Recrystallization is not adaptable to 3-D integration due to the large thermal gradients and high temperatures. But a similar technique, known as Lateral Solid Phase Epitaxy (LSPE) is well-suited in some ways to stacked devices. LSPE is structurally identical to recrystallization, but uses lower temperatures and stationary heat/light sources [34]. It is observed that polysilicon realigns to the crystal orientation of the substrate without the need for melting. Lateral crystallization distances up to 6 microns can be achieved by this method [35]; although very heavy doping with phosphorus can extend these distances to tens of microns [34, 36]. Reasonable crystal quality and devices have been built in the first 2 lateral microns of LSPE films [35], but beyond this, crystal quality falls off rapidly. LSPE growth fronts tend to be non-uniform [34] and generates large quantities of dislocation defects where growth fronts converge [27, 37]. LSPE is obviously fraught with technical difficulties, but, if overcome, could become a strong candidate for SOI device isolation and 3-D integration.

2.2.2.3 Epitaxial Lateral Overgrowth (ELO)

ELO is an extension of Selective Epitaxial Growth (SEG is covered in detail in the next section) which can be used for SOI device isolation. In SEG, epitaxy process conditions are adjusted to allow silicon to grow on already-exposed silicon surfaces, while simultaneously preventing deposition on oxide or nitride surfaces. Figure 2.5 (a) shows an ELO structure which has grown from the substrate, through a seed hole in an oxide layer, then up and over the oxide mask. Growth fronts from adjacent seed holes can be merged to form a contiguous film, as in Figure 2.5 (b). With further growth, the facets at the merge front will grow faster than the horizontal growth front, and eventually catch up to the horizontal planes, forming a smooth silicon surface [38,73].

To be classified as SOI, devices in ELO must be built in the lateral wings over the oxide. But to take advantage of the dielectric isolation, the silicon thickness there should be less than 1 micron. The major disadvantage of ELO is its inability to cover large lateral distances without exceeding a reasonable vertical height. The aspect ratio of an ELO growth is defined as the lateral growth distance divided by the vertical growth height, and is a key figure of merit for ELO technology. Several researchers have claimed high aspect ratios [39, 40, 41], but in recent years, reports indicate aspect ratios are limited to about unity, except perhaps at the very early stages of growth [42]. The reason for the early claims of high aspect ratio may have been due to incomplete



Figure 2.5 Epitaxial Lateral Overgrowth (ELO) technique (a) showing (b) merging and (c) planarization.

understanding of deposition mechanisms, and thin oxide degradation, leading to a misinterpretation of results [43].

To be useful as an SOI isolation technology, the as-grown ELO film must be thinned in the vertical direction. This is indicated in Figure 2.5 (c). Thinning methods include polishing [44], plasma etch-back planarization [45]; and for merged ELO, oxidation [46] or an isotropic silicon etch [38]. The only reports of devices in thinned ELO are for MOSFETs which seem to perform reasonable well [38, 47]. Studies of the interface between ELO and underlying oxide showed a reasonably low $(1.7 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1})$ density of midgap traps [48]. However, lifetime measurements in SOI ELO are one to two orders worse than in a standard device wafer [49].

ELO is still a strong candidate for 3-D integration because of the good material quality, the ability to grow ELO at low temperatures, and the ability to make whole wafer SOI [50, 42]. To make SOI over an entire wafer, merged ELO is masked and etched over the seed hole to expose the substrate. The substrate is selectively oxidized (ELO is covered with nitride sidewall spacers), and a second ELO step then regrows silicon over the oxidized substrate. After minor planarization, a whole-wafer SOI film results.

2.2.3 Requirements for ideal SOI

The SOI methods outlined above all suffer shortcomings which offset the advantages listed in section 2.2.1. Below are presented the requirements for an ideal SOI technology.

LAYOUT REQUIREMENTS

- (1) SOI over large areas, or local-SOI suitable for individual devices (high aspect ratio).
- (2) Controllable dimensions of local-SOI, and flexibility of seed hole (if any) placement.
- (3) Few or no masking steps.
- (4) Optional substrate contact.
- (5) Latchup-immunity.
- (6) Easy alignment for multiple SOI layers (3-D integration).
- (7) Adaptable as an interconnect level.

PROCESS REQUIREMENTS

- (1) Use only conventional equipment and methods.
- (2) No large thermal gradients (to avoid wafer warpage and stress).
- (3) Low number of process steps.
- (4) Quick turn-around for SOI steps.
- (5) Seed hole removal (if desired) with etch or LOCOS.

DEVICE REQUIREMENTS

(1) High quality bulk crystal.

- (2) High quality interface with insulator.
- (3) Controllable silicon and insulator thicknesses.
- (4) Uniform silicon thickness.
- (5) Backside accessible for buried layers.

(6) 3-D integrable (low temperature, stackable).

At present there is no single technology which can fulfill all of these requirements. In this work, it will be shown that CLSEG satisfies a majority of these, making it well-suited for SOI device isolation applications.

2.3 Selective Epitaxial Growth (SEG)

SEG is a special epitaxy technique useful for fine (small) device isolation [51, 52, 53, 54]; and, as ELO, for advanced device structures [47, 48, 55, 56]. SEG was first reported in 1962 [57] when an oxide-masked wafer in an epi reactor showed an absence of silicon nucleation on the oxide at the periphery of the seed holes. In the next subsection, we review the conditions for selective growth, the effects of different masking material, and consequences of the etch method used to create the seed hole.

2.3.1 Selectivity and mask materials

Several years after the first SEG, Jackson [58] discovered that HCL gas added to the epitaxy process gasses improved considerably the selectivity of growth by etching silicon adatoms on the mask surface. However, too much HCl gas will result in net etching of silicon, not growth. This defines a window of selectivity, which changes at different temperatures, pressures [59, 60], and silicon surface ratio [61, 62] (exposed silicon area divided by total wafer area). To ensure good selectivity it is important to keep the mask surface free of contaminants or particles [63, 64]. Oxide is a better mask material than silicon nitride for selectivity, since nitride is 10 to 1000 times more likely to initiate nucleation [65, 66, 67, 68].

The SEG process conditions can cause degradation of the mask material under certain conditions. Nitride is more stable than oxide [69], but tends to crack when its thickness exceeds several hundred nanometers [69, 70]. Thin oxides are susceptible to pinholes [63], especially at higher temperatures and lower pressures [43]. Oxide degradation is not a problem for thicknesses above 150 nm, for the range or class of epitaxy process variables used in this work.

Seed holes are etched either with aqueous solutions or by RIE plasma. Some researchers have found that the scalloped mask edge profile caused by wet etching leads to stacking fault defects in SEG [62, 56]. On the other hand, RIE leaves corrugated sidewalls [71, 60], and causes radiation damage to the silicon substrate [72], both of which can cause defects in the SEG growth. There are two ways to get the best of each etch: (1) RIE 90% of the masking film thickness, then complete with a wet etch; or (2) RIE completely through, then grow a sacrificial oxide to heal the radiation damage, and finally removed with a wet etch. Both of these methods have been used successfully.

2.3.2 Pre-clean and epitaxial growth

An important difference with standard whole-wafer epitaxy is that SEG mask materials (especially oxide) generally cannot withstand the typical high temperature HCl preclean [63, 64, 56]. The HCl etches silicon at high temperatures, which would undercut the mask [60]; but even without the HCL, at high temperatures, silicon dioxide at the Si-SiO₂ interface will sublimate according to:

 $Si+SiO_2 \rightarrow 2SiO_{(g)}$ (1)

However it is vitally important to remove any native oxide (1 - 10 nm thick) that appears on bare silicon surfaces when exposed to air. The reaction in (1) can be used to remove native oxide while leaving the oxide mask intact provided the temperature does not exceed 1000° [60, 74] or 1050°C [64]. Still, this prebake in hydrogen gas or vacuum must exceed a critical temperature, defined by the O₂ and H₂O content of the ambient, to be effective [75].

Although any silicon source gas used for conventional epitaxy can be employed for SEG, Dichlorosilane SiH_2CL_2 (DCS), is used most commonly. This is because DCS deposits at lower temperatures and produces HCl, thus requiring less input HCL gas. It is found experimentally that low temperatures ($< 1000^{\circ}$ C) and reduced pressure (< 150 Torr) are very beneficial to SEG. Recent work has demonstrated SEG at temperatures as low as 600° to 650° C [76, 77, 78], although so far, low defect material has only been achieved down to roughly 800° C [79] at ultra-low pressures.

The benefits of low temperature stem partly from the transition to a regime where deposition is surface reaction limited [80, 81, 78, 81]. Reduced pressures also bring deposition into the surface controlled regime [64, 51, 59, 82]. At higher temperatures and pressures, deposition is diffusion-limited, meaning that gas phase diffusion through the boundary layer controls growth. Since the steady state concentrations of silicon-containing species is larger over the mask than over the growing silicon, a lateral concentration gradient is produced. Because of this gradient, more silicon is deposited at the edge of a SEG seed window than in the center, making the growth rate higher there. The resulting profile of the SEG is concave downwards in a phenomenon called "smiley" because of its semblance to a grin.

In the surface-controlled regime, deposition of silicon is temperature controlled. Silicon adatoms, and silicon species such as $SiCl_2$ [65], are adsorbed onto the mask and silicon surfaces alike. They then do a random walk until they find a suitable nucleation site on a silicon crystal surface or a piece of dirt. Surface mobility of silicon is high [63], and reports of diffusion distances range from several microns [83, 84, 40] (considering mean distance between mask nucleation sites), to 10 - 100 microns [56, 85, 81, 86]. Growth in this regime can result in flat SEG and ELO profiles [64, 87, 51, 82, 88, 80, 89].

Only recently has it been reported that changes in masking oxide thickness affect growth rate. The likely mechanism for this is the variation in surface emissivity due to different film thicknesses. This in turn affects the radiative heating of the epitaxy gasses and influences the growth rate. For pancake-type reactors (flat, horizontal susceptor with rf energy applied from beneath) growth rate increases for thinner oxides [86]. It is interesting to note that growth rates in this study seem to depend on global average oxide thickness (areas roughly 400 microns in diameter). Local variations in oxide thickness have little effect on growth rate. In the results section of this work, it will be shown that for a barrel-type reactor (cylindrical, vertical susceptor heated from outside the bell jar by infra-red lamps) the growth rate versus oxide thickness is more complex. This behavior may be related to light reflections and absorptions in the oxide layer, as well as the interaction between surface radiative heating and backside conduction from the susceptor (which is heated by infra-red radiation passing

through the silicon).

2.3.3 Defects in SEG

It is a fact of nature that defects exist in all crystals at temperatures above absolute zero [90]. Although such defects as dislocations can give added strength to certain metal crystals, for electronic crystal, the density of defects should be as low as possible. The inhomogeneous nature of SEG provides ample opportunity for defect generation, and considerable effort has been devoted to their reduction. In this section, the results of these studies are reviewed.

It was determined that rectangular seed holes oriented along $\{001\}$ equivalent directions on a <100> oriented substrate have the lowest density of defects [108, 92, 71, 49], and gives a uniformly flat top surface [60, 108, 93, 94, 64]. Other seed hole orientations generate facets at the sidewall interface, thus reducing active device area. The mechanisms for facet formation and for defect generation at the sidewall are similar. Regardless of sidewall orientation, silicon atoms which abut the sidewall are forced to accept fewer than 4 covalent bonds to other silicon atoms. Because of the lack of oxygen or nitrogen, solid chemical bonds to the sidewall are prevented.

Along $\{011\}$ equivalent sidewalls, adatoms can occupy one of two positions of nearly equal energy. One of these sites corresponds to a defect and can occur when the adatom at the sidewall is incorporated after the atom next closest to the wall. This results in a twin defect (on <001> substrates) and will propagate into the growing SEG at a 35.3° angle to the direction of growth. By a similar argument, the growth rates of different atomic planes in the crystal are affected by the presence of the sidewall. For $\{011\}$ equivalent sidewalls, a <311> facet is formed at the edge of the seed hole [108], thus encroaching on the active device area. But along $\{001\}$ equivalent sidewalls, there is no ambiguity in the sites available for adatom incorporation. This is responsible for the low defect density and the absence of growth defects in $\{001\}$ SEG seed holes. Still, irregularities in the walls of $\{001\}$ seed holes, or undercut of the masking layer, can generate twins, dislocations, or stacking faults.

Defects in CLSEG arise from three sources. One is the sidewall stacking defects described above, which can be practically eliminated with $\{001\}$ oriented seed holes. The second is stress due to mismatch of thermal expansion coefficients; and the third is defects incorporated into the bulk SEG during growth.

When the SEG wafers are heated to receive the epitaxy, the masking layer and substrate both expand, changing the size of the seed hole. The SEG fills this seed hole, whose dimensions then change upon cooling of the wafer, generating stress in the SEG [95]. Sidewall defects, whether due to stress or growth defects, extend from 0.2 to 1.5 microns laterally into the SEG film [96, 62], and can be reduced by growing at lower temperatures [71, 72, 42, 82, 52, 96].

Bulk defects generally occur from some form of contamination in the epi reactor system. High purity gasses are essential to good film quality. Several workers single out HCl gas as a major source of contamination [60, 40, 97]. Although of high purity in the bottle, HCl gas is very corrosive, and can pick up metallic impurities from the gas handling system. For low temperature epitaxy, an insidious source of contamination is residual moisture and oxygen in the gas stream or in the bell jar [81]. The temperature and the partial pressures of O_2 and H_2O in the system, these species can form oxygen clusters [76] or clumps of SiO₂ can form at the growing interface. This can generate defects in the film such as stacking faults; or benevolently, the growing SEG can envelop the clusters and continue on uninterrupted. When this occurs, a vague rounded square structure can be seen on the top of the SEG using Nomarski polarization microscopy. These are apparently not defects, but merely growth phenomenon [76, 98].

To implement SEG into production processes, it is important that growth rates are uniform across a wafer. Improved injector nozzles or gas bottles [99] can help, but SEG is susceptible to a loading effect where the growth rate depends on the silicon surface ratio of a particular seed hole pattern on a wafer. The loading effect is apparently associated with smiley since it is also minimized at lower temperatures [98, 100, 87], and reduced pressures [87]. In any case, as the trend towards lower temperatures and pressures continues, loading effects will be less of a problem. However, at lower temperatures, growth tends to be surface reaction limited so that small variations in surface temperature can have significant influence on local growth rates.

2.3.4 Interface properties and devices

At the current level of understanding, the most significant obstacle to SEG development is the presence of leakage currents in devices with junctions that intersect the sidewall interface [52, 53, 92, 62]. These leakage currents may or

may not arise from defects within the silicon. As the above review has shown, visible sidewall defects can be greatly inhibited with proper technique. This would seem to imply that the properties of the interface itself are largely responsible for leakage currents.

A stentorian effort has been made to characterize the exact nature of this interface [101]. Klaasen used a new device called a sidewall gate-controlled diode (shown in Figure 2.6), with the gate oxide being the sidewall interface itself. Unfortunately, the sidewalls in this device are rife with sharp angles and irregularities, which can generate considerable number of defects. This precludes a more definitive evaluation of the sidewall interface, until the processing difficulties can be overcome.

The bulk of research into sidewall leakage currents has been empirical. It is found that sidewall leakage currents are reduced by growing SEG at lower temperatures [52, 71], and at reduced pressures [72, 53, 92]. A likely model for the sidewall leakage is incomplete bonding between Si and SiO₂, leading to enhanced diffusion there [53]. It has been claimed that in-situ hydrogen anneals during SEG growth may help to neutralize interface states here [48], and that a post-SEG oxidation can heal this interface [99]. Studies of SEG growth (or ELO) on existing oxide revealed interface mid-gap trap densities in the 10^{11} cm⁻² eV⁻¹ range [48, 52], which is adequate for MOS operation. Devices built in the bulk of SEG material, away from the interface, demonstrate nearbulk quality crystal [102, 74, 80, 79, 49, 52]. However, reported leakage currents for n-MOSFETs which have source/drain regions that abut the SEG interface are several orders of magnitude higher than for LOCOS isolated devices [92]. Walled diodes similarly exhibit higher leakages than LOCOS isolated diodes, as described above.

Published research indicates that sidewall growth defects can be practically eliminated, and that interface trap densities can be made quite low. However the question remains as to how sidewall leakage currents are generated. If this problem can be understood and easily solved, SEG and ELO techniques may find far greater application. In the next section, the CLSEG technology is shown to be an ideal research tool for the study of SEG sidewall interfaces.

2.4 Motivations for CLSEG

The CLSEG concept arose out of frustrations and limitations of ELO technology. Not until very recently have other workers reported similar



20

SUBSTRATE

Figure 2.6. Sidewall Gate Controlled Diode after Klaasen [101].

concepts [109,110]. During the course of the investigation, a plethora of uses and justifications for CLSEG have been discovered. By confining SEG within a dielectric cavity, several important shortcomings of ELO have been overcome, and a host of further applications have become readily available. In this section, the motivations for pursuing CLSEG research are outlined.

2.4.1 Growth studies

An important use for CLSEG is the study of the Si/SiO_2 interface in selective epitaxy. By constraining growth to proceed parallel to the surface of a wafer, the SEG/insulator interface is made wider and easily accessible, compared to conventional SEG. This provides a convenient working surface for interface characterization studies. CLSEG can also be used as a tool to examine the reaction and growth mechanics of SEG. With a CLSEG cavity structure, silicon species transport may be quite different than for conventional SEG or ELO.

A further application is in understanding differences in the wafer-heating behavior of the two standard reactor types: barrel and pancake reactors. The top insulating layer of the empty CLSEG cavity prior to growth is not in good thermal contact with the substrate. This can lead to temperature differences within the cavity (i.e. top wall versus bottom wall), which can significantly affect selective growth. The study of growth in cavities of different heights or materials may give clues to the nature and location of the CVD reactions which give rise to selective epitaxial growth. A related area of interest for CLSEG uses is in the study of structural silicon geometries on oxidation and defect generation. Similar to trench oxidation, CLSEG can be used in a variety of configurations to study these effects. As with growth studies, the planar nature of the CLSEG film makes it suitable for efficient characterization.

2.4.2 Device isolation

CLSEG is a low temperature process, uses only conventional process steps, forms a uniformly thick film, and is easily isolated from the substrate. Stacking and alignment of CLSEG layers is readily done, making it suitable for 3-D integration. Using a two-step process (described briefly above) CLSEG can be used to form a SOI layer over an entire wafer. Finally, all these benefits from CLSEG can be achieved with only a single masking step. This will be described

21

in the Future Investigation Possibilities section of the last chapter.

2.4.3 Advanced device construction

The applications of CLSEG can be pursued at great length, but only a few will be presented in the Conclusions chapter. Several features of CLSEG lend this technique to new ways of constructing bipolar and MOS transistors and circuits. CLSEG allows a very high aspect ratio for local SOI applications. Because of the physical connection to the substrate through the seed hole, the bottom oxide can be removed, making the backside of the SOI film accessible for doping. Self-isolation of CLSEG films is possible this way, even with the substrate connection intact. CLSEG provides an extra level of interconnect if needed. Being high quality silicon, the resistance through the CLSEG layer can be made quite low. And finally, CLSEG as a structural technique is applicable to micromachining and sensor fabrication.

CHAPTER 3

PROCESSING

In this chapter the fabrication sequence for CLSEG is described first in generic terms to introduce terminology and provide and overview for the remainder of the chapter. Subsequent sections describe the CLSEG cavity construction, the cavity layout, and CLSEG growth conditions in the epitaxy reactor.

3.1 Generic Fabrication Sequence

Figure 3.1.a shows the first three steps in the fabrication process. Beginning with a silicon substrate, a thermal oxide is grown and is referred to as the bottom oxide, since it will form the lower wall of the CLSEG cavity. Optional at this point is the deposition of a silicon nitride layer, if this material is preferable for the lower cavity wall. A seed hole is etched through the bottom oxide, and bottom nitride if present (not shown). Then a thin oxide is optionally regrown on the exposed silicon of the seed hole, and called the seed hole oxide.

In Figure 3.1.b, a film has been deposited and etched, as shown. This film is the sacrificial layer, and may be made of polysilicon, amorphous silicon, oxide, nitride, or other processing material. The three-dimensional shape of the sacrificial layer after etching will establish the dimensions of the CLSEG cavity when the process is finished. Note that it is important that the sacrificial layer cover at least part of the seed hole.

In the next step, shown in Figure 3.1.c, a layer or stack of layers of material is formed on top of the sacrificial layer. This layer or stack is called (collectively) the top layer. A third mask step is used to etch a hole, called the via hole, through the top layers(s). This step exposes the sacrificial layer. In Figure 3.1.d the sacrificial layer has been selectively etched away. The thin seed





hole oxide (if any) is also etched off, exposing the substrate in the seed hole. This step has defined the cavity which is now ready to be filled with singlecrystal silicon. Figure 3.1.e shows the result of the selective epitaxial growth step. Beginning at the exposed substrate surface, silicon deposits preferentially (selectively) and epitaxially, and grows up and out of the seed hole. As the growth front encounters the top layer, epi growth is constrained to proceed laterally, filling the cavity. The aspect ratio for the CLSEG film thus created is defined as the lateral distance from the right edge of the seed hole to the rightmost limit of lateral growth, divided by the vertical height of the CLSEG film. This completes the essential steps for generic CLSEG fabrication. In the next section, the issues concerned in actual fabrication are addressed.

3.2 Cavity Construction

In this section the factors pertinent to material choices for the bottom layer(s), sacrificial layer, and top layer(s) are described in more detail. Actual dimensions used for successful CLSEG fabrication are summarized at the end of this section.

3.2.1 Bottom layer

The most important function of the bottom layer is to provide electrical isolation between the CLSEG silicon and the substrate silicon. When CLSEG is referred to as silicon on insulator, it is this bottom oxide which is the insulator. Other properties important to the bottom layer are: the ability to withstand the high temperatures of the epi step; that it must remain intact during the etch of the sacrificial layer; that it provide a good interface for SEG growth; and that it is a readily-available material. The two choices for the bottom layer(s) considered for this work are: (1) thermal oxide alone; and (2) low-pressure chemical vapor deposited (LPCVD) silicon nitride atop thermal oxide. Thermal oxide by far provides the best interface for SEG, and it has a much lower dielectric constant than nitride, making it the obvious choice. However, in the case that the sacrificial layer is oxide, a thin nitride layer is needed to provide etch selectivity.

The bottom layer thickness would usually be chosen to achieve a low value of CLSEG to substrate capacitance. Two other issues must also be considered in choosing this thickness. When the sacrificial layer is deposited, its top surface
(in most cases) will reflect the step height at the seed hole. If no steps are taken to smooth this step, a perturbation is formed in the top layer above the seed hole. It is found that defects can be formed at this perterbation during CLSEG growth. To minimize this effect, either the bottom layer should be made as thin as is acceptable, or planarization methods employed. The second issue is that later processing sometimes requires that the bottom layer be etched out from beneath the CLSEG silicon, for example to introduce dopant atoms to the CLSEG underside. The gap left by the bottom layer removal must be large enough to admit these dopant atoms. Finally, the bottom layer thickness, if it is oxide alone, must be thick enough to withstand the SEG conditions [43]. This requires that the oxide thickness be at least 100 nm, or, more conservatively, 150 nm thick. Bottom layer thickness must be chosen judiciously considering device design as well as process requirements.

A final consideration regarding the bottom layer is the method of etching the seed hole, either by isotropic or anisotropic means. As described in Chapter 2, there is evidence that the scalloped edges from isotropic etching leads to stress in SEG films. However, anisotropic etching leaves vertical ridges in the bottom layer sidewall which lead to defects there. A combination of both etching types is reported to have optimal effects. However, the only defects observed in CLSEG appear to arise near the seed hole edge, so the etch technique must be chosen with care.

3.2.2 Sacrificial layer

The first consideration in the choice of a material for the sacrificial layer is etch selectivity. Typical cavities for this work are 8 microns from seed hole to via hole, plus a three micron seed hole width, requiring a lateral etch of 11 microns. Since the top and bottom layers are typically fractions of a micron thick, etch selectivities of at least 100:1 are necessary. Three materials have been considered for their ease and uniformity of deposition, and ability to withstand high temperatures. These are: plasma-enhanced CVD (PECVD) silicon nitride; phosphorus-doped low temperature oxide (N⁺ LTO); and either amorphous (α -Si) or polycrystalline (poly) silicon deposited by CVD. PECVD nitride can be etched using a boiling mixture of phosphoric acid and water. This etch is entirely selective to silicon, has a selectivity over 100:1 for thermal oxide, but only about 20:1 compared to LTO, which may be used as a top layer. N⁺ LTO is etched using dilute solutions of buffered HF (NH₃F:HF:H₂O = 1:1:6.5) with an etch rate proportional to the phosphorus content. This etch is also entirely selective to silicon, and selective to at least 500:1 to LP nitride (used as top and/or bottom layers). Poly or α -Si can be etched in several ways. One is to use a mixture of nitric acid with a very small amount of ammonium floride, which is reported to be highly selective to oxide; but was not investigated for this work. The silicon etch used for this work was a mixture containing mostly ethylene diamine (ED). This ED silicon etch is selective to oxide in the order of 10,000:1 at 90° C. Selectivity to nitride was not quantified, per se, but is at least 1000:1. Despite the advantages of the ED silicon etch with the polysilicon sacrificial layer, this system was the last to be investigated, largely because of the highly toxic nature of the ED solution. Yet, not surprisingly, the ED silicon etch produced the best results.

Other factors to consider in choosing the sacrificial layer material are internal film stress, surface smoothness and planarity; and the ability to withstand the deposition temperatures of the top layer. PECVD nitride was the first material used, but is ruled out due to high film stress. With a PECVD nitride sacrificial layer, oxide can be used for the top and bottom layers to provide the best surface for CLSEG growth. However, microcracks develop in the nitride layer, and form long fissures in the oxide layers, exposing the substrate. During CLSEG growth then, ELO grows out of the fissures, catastrophically damaging the wafer for device fabrication.

3.2.3 Top layer

The top layer is the cornerstone of CLSEG fabrication since it makes possible all the advantages this technique has over ELO. The main property demanded of this crucial film (or films) is that it remain rigid and not sag, buckle, deflect, or deform. Since CLSEG is really a deposition and not a "growth", it does not push against the top layer. Thus whatever shape the top layer assumed just prior to the CLSEG epitaxy step establishs the dimensions of the SOI film. The features to consider when choosing the top layer material(s) are: modulus (stiffness), internal stress, coefficient of thermal expansion, conformality of deposition (or growth), etch selectivity, interface properties with SEG, and possibly thickness and surface emissivity.

To meet these requirements, the best results achieved to date have been obtained using a sandwich of LP nitride on thermal oxide (grown from α -Si, which converts to poly at the oxidation temperatures). Oxide alone as a top layer, whether LTO, spun-on, or oxidized poly, is not stiff enough, at least in thicknesses less than 0.5 microns. Poly cannot easily be used because, if any of it is left exposed during the epi step, its thickness will increase by roughly the lateral growth distance of the CLSEG. This is clearly unacceptable. Much of the development work on CLSEG was done using N^+ LTO as the sacrificial layer and LP nitride as the top and bottom layers. However, CLSEG films grown between nitride walls produced devices with high leakage currents, even after stripping the nitride and reoxidizing. Also the modest etch selectivity required special care during processing, since the dilute HF weakens the top layer nitride, especially to the inside corners of the cavity.

The materials and dimensions which have produced the best cavity are summarized below, and are described in process flow form in Appendix A. They are: (1) bottom layer of thermal oxide only with thickness between 250 and 500 nm; (2) A seed hole oriented along $\{001\}$ equivalent directions, defined using anisotropic etch, and seed hole oxide thickness of 20 nm; (3) a sacrificial layer of α -Si (for smooth top surface) of thickness between 0.5 and 1.2 microns; then oxidized to 100 nm (this forms the top layer oxide for the inside wall of the cavity); and (4) a top layer of LP nitride, with thickness between 110 and 150 nm (thicker layers may tend to crack). However even with these optimized results, the cavity layout is crucial to successful CLSEG, and is described in detail in the next section.

3.3 Cavity Layout

CLSEG cavities are like a bridge or a house in that the design is as important to preventing its collapse as are the materials used. A main goal of CLSEG cavity layout is to make the lateral distance as large as possible while preventing the top layer from sagging. A simple cantilever, as shown in Figure 3.1.d and for the materials used here, will not stay supported for cavities that are either very wide or very long (into the paper). The first step to avoid cavity collapse is to leave intact the top layer at the two ends of the cavity lengthwise. This supports the top layer from 3 sides, but sagging is still observed for cavities more than 25 microns long. The next step is to allow the top layer to be continuous across the width of the cavity, in at least a few places. This is accomplished with the via hole mask, by making the via holes periodic along the length of the cavity. Figure 3.2 shows a cut-away perspective view of the cavity described in three dimensions.



Figure 3.2 Perspective view of CLSEG cavity showing via hole placement.

Sec. 1

In Figure 3.3, a plan view of the cavity shown in Figure 3.2 is depicted, with appropriate distances labeled in microns. The length of the cavity is unlimited, but typical lengths range from 50 to 150 microns. The slight rounding of the sacrificial layer mask helps avoid thinning of the top layer at the corners during deposition and cavity etch. The seed hole width of 3 microns was chosen for convenience, but can be made considerable smaller. In fact, the minimum seed hole width is limited only by lithography, as evidenced by the ELO which grew through microcracks in the oxide, as described in the last section. The spacing between via holes (shown as 5 microns in the figure) must be at least close enough to permit complete clearing of the cavity. Since silicon gases or adatoms must pass through the via holes to cause growth in the cavity, again a close spacing is preferred. On the other hand, the wider this spacing can be made, the more supported the top layer will be. The effects of via hole spacing are discussed further in section 4.1

CLSEG cavity design is quite flexible. CLSEG has been grown in cavities which turn inside or outside corners, or which have the seed hole in the center and via holes on either side. A wide variety of layout choices are possible, depending on the specific application. This is another advantage of CLSEG over ELO, which must always have the seed hole at the center of an approximately radially isotropic growth.

The maximum aspect ratio of a CLSEG film is set by the lateral spacing between the seed hole and the via holes (assuming no process limitations). It is interesting to note that if the CLSEG continues beyond the via hole, it will continue growing isotropically (neglecting facets) like ELO, even growing back over the top layer. This opens up the possibility of stacked cavities filled with a single growth step. For most applications this overgrowth is undesirable, and can be avoided by making the cavity slightly wider. The next section describes the growth conditions for CLSEG, and will conclude this chapter on CLSEG processing.

3.4 CLSEG Growth Conditions

Two different epitaxy reactors were used to grow the CLSEG for this work. The first is a pancake-type reactor which has a flat and round horizontal susceptor heated from below by radio-frequency (rf) energy. Wafers are laid on the susceptor which is enclosed by a bell jar. Gasses enter from the center of the susceptor and are evacuated with a mechanical pump. This system is



Figure 3.3 Layout of masks used to form a CLSEG cavity.

currently capable of reduced pressure operation down to 150 Torr. The second is a barrel-type reactor which has a tapered cylindrical susceptor which holds the wafers, and is suspended within a bell jar. The quartz bell jar is surrounded by infrared lamps which provide heat to the wafers and the susceptor. Gasses are introduced at the top of the bell jar and evacuated from the bottom by a mechanical pump. The minimum pressure of this system is 4 Torr, but with typical gas flow rates, the minimum deposition pressure is approximately 40 Torr.

The first step in the growth of selective epitaxy is to prepare the silicon surfaces by in situ removal of native oxides. The standard epitaxy procedure of high temperature HCl pre-cleans are not suited for SEG since it etches the silicon and undercuts the oxide or nitride masks. CLSEG in situ precleans for both reactors begins with a hydrogen gas only bake under reduced pressure at 950° or 975° C for 5 minutes. This is sufficient to remove native oxide without undercutting the mask oxide, as described in section 2.3 above. In the pancake reactor, but not the barrel reactor, this is followed by adding HCl gas under the same conditions for 30 seconds. There is little evidence that this step is necessary or even helpful, but it is not likely to impair crystal quality. However, the HCl etch may provide a better surface to grow from if any residual damage was present in the silicon surface.

The deposition step has been carried out at both 950° and 1000° C for each reactor; with deposition pressure kept at 150 Torr for the pancake, and 50 Torr for the barrel reactor. Dichlorosilane (SiH_2Cl_2) gas and HCl gas are mixed into the hydrogen carrier gas flow during deposition. In the barrel reactor, phosphine gas is also added to dope the CLSEG n-type. In the pancake reactor, the intrinsic SEG (no dopant added intentionally) is high-resistivity n-type with no dopant added. The key to selective deposition of silicon on silicon, but not on oxide or nitride is to carefully choose the ratio of dichlorosilane to HCl. The dichlorosilane gas is the silicon source, and is thought to decompose into $SiCl_2$ + H_2 at high temperatures [41]. When the SiCl₂ molecule encounters a surface site in the presence of hydrogen, the silicon is deposited as an adatom and releases the chlorine atoms as HCl. The HCl gas added intentionally serves a dual purpose. First, it tends to inhibit the decomposition of SiCl₂, which aids selectivity because silicon deposits preferentially on silicon already present. Second, it may or may not help to etch away any silicon adatoms which may nucleate as unwanted solid on the oxide or nitride mask. By proper adjustment of the ratio of these two input gasses, net deposition occurs only on alreadypresent silicon surfaces, leaving the mask free of nucleation. For both reactors, at either temperature, selective growth is achieved when SEG growth rate is less than 0.25 microns/minute. All of the experiments reported in the next two chapters target growth rates at between 0.15 and 0.25 microns/minute.

At the same time as the CLSEG is grown, SEG also grows on large areas of the wafer which have seed holes exposing the substrate, but do not lie within a cavity. These regions are referred to as homoepitaxy islands, since away from the edges (where they are technically ELO) they behave similarly to whole-wafer homoepitaxy. The reason for growing these islands is to support control devices for comparison with CLSEG devices.

After CLSEG growth, semiconductor devices are fabricated within the lateral SOI regions. Parameters extracted from these devices are used to evaluate CLSEG material quality and to compare it to homoepitaxy or substrate material quality. The growth and electrical characterization of CLSEG is presented in the next chapter.

CHAPTER 4

CHARACTERIZATION OF CLSEG SILICON

Perhaps the most surprising fact of CLSEG growth is that it can be done at all. Conventional theories of epitaxy growth mechanics would leave one skeptical towards the idea of growth within a deep and narrow cavity laid flat on the face of a wafer. Instead, this novel technique has revealed new insights into selective epitaxial growth and provided some very interesting results. In this chapter, the growth properties of CLSEG are described in detail, followed by electrical characterization of devices built in CLSEG. At the end of the chapter, near-optimal conditions for CLSEG fabrication are presented as a summary.

4.1 Growth Properties of CLSEG

To provide a control or a standard of comparison for CLSEG growth rates and electrical quality, SEG is grown from large seed holes with no top layer over it at the same time as the CLSEG is grown. As this SEG overgrows the edges of the seed hole, it is called ELO (Epitaxial Lateral Overgrowth). But well inside the edges of the seed hole, this selectively grown material will be referred to as homoepitaxy islands, since it is functionally no different than whole-wafer homoepitaxy. Growth rates of homoepitaxy islands are obtained by measuring the thickness from the original substrate interface to the highest point, which usually occurs in the ELO near the edge.

Another factor that will significantly affect the interpretation of results is that two types of epitaxy reactors were used to grow CLSEG. One is a pancake-type reactor in which wafers are placed face up on a flat, round susceptor heated from below by radio frequency (rf) energy. A bell jar contains the process gasses and a mechanical pump allows for reduced pressure operation. With the current system configuration, pressure is limited to 150 Torr, which is a function of the rf generator and induction coil design. The second is a barrel reactor in which wafers are leaned against a tapered cylindrical susceptor and lowered into a bell jar. Infrared lamps heat the wafers, gasses, and the susceptor from outside the bell jar, which can be evacuated to 4 Torr. The differences in these reactors and the pressures used during deposition have a profound impact on CLSEG devices and growth.

4.1.1 Seed hole orientation

In the field of SEG, it is now generally accepted that seed holes oriented along $\{001\}$ equivalent directions on a <100> substrate allows SEG with the lowest defect densities and leakage current along the sidewall. For this work, all CLSEG and homoepitaxy island seed holes are so-oriented. From this seed hole, the CLSEG grows up and then over the masking bottom layer; encounters the top layer, and then grows only laterally. Because the SEG must in effect grow around a corner (growing first vertically through the seed hole, then laterally over the masking layer), it is necessary to determine the crystal orientation of the CLSEG silicon to verify that it still follows that of the substrate. To this end, a technique called Electron Channeling Pattern (ECP), or rocking curves, was used. In a scanning electron microscope (SEM), the electron beam is focused on the area to be analyzed, and the sample is pivoted (rocked) back and forth with the measured area as the pivot point. Equivalently, in a transmission electron microscope, the beam can be rocked instead of the sample; making possible smaller measurement areas. The electron beam encounters different crystal orientations as the sample is rocked, and produces an image or pattern which is unique to the crystal orientation normal to the surface of the sample. Also, the sharpness of the pattern is indicative of the relative crystallinity of the sample, since amorphous samples produce no pattern.

Figure 4.1 shows three ECPs taken from CLSEG silicon, homoepitaxy silicon (SEG), and substrate silicon on a single die site. This pattern is indicative of the <001> crystal plane in silicon and demonstrates that CLSEG silicon grown on <001> silicon maintains the <001> orientation. Qualitatively, the equivalent sharpness of the patterns also shows that CLSEG is indeed single-crystal material.



Figure 4.1 Electron Channeling Patterns of (a) CLSEG, (b) homoepitaxy, and (c) substrate silicon.

4.1.2 Growth rate

Preliminary studies of ELO behavior prior to CLSEG provided useful data for the understanding of several growth phenomenon. In the pancake reactor at 150 Torr, growth rate has been found to decrease in linear proportion to the ratio of the partial pressure of HCl squared to the partial pressure of dichlorosilane (DCS) [103]. In the regime of interest to this work, the growth rate can be modeled at constant temperature and pressure, as:

G.R. = A - B×[pp_{HCl}]²/[pp_{DCS}]. (2)

Growth rate is also found to be inversely related to masking oxide thickness [86]. Both of these studies were repeated for the barrel reactor at 50 Torr to verify that similar processes were at work. Figure 4.2 shows the dependence of ELO growth rate on $[pp_{HCl}]^2/[pp_{DCS}]$ for three oxide thicknesses, along with the growth rate from a bare target wafer. These data clearly show the negative proportionality region for growth rates up to 0.15 to 0.20 microns/minute. Above this growth rate, the dependence on gas ratio is confounded by a dependence on the oxide thickness. Figure 4.3 demonstrates a surprising growth rate dependence on oxide thickness for $[pp_{HCl}]^2/[pp_{DCS}]$ values in the negative proportionality regime. To the author's knowledge, this peak in growth rate versus oxide thickness has not been reported in the literature. The reason for this behavior is not well understood but may be caused by changes in surface emissivity or reflectance properties of the masking oxide with its thickness. Clearly growth rate dependence on mask thickness can be very complex; an effect which will be further exacerbated by the use of multiple films as is done with CLSEG.

The first step in characterization of CLSEG growth rate is to compare it to the growth rate of ELO. In the data below, CLSEG growth rate is measured laterally and taken visually; and ELO growth rate is measured vertically with a moving-stylus profilometer. For both, unless otherwise stated, 9 points are measured on each 5 inch wafer and averaged; typical standard deviations are 15% to 20% of the mean value. Due to the variable nature of epitaxy reactor characteristics, the gas flow ratios were adjusted before each run to give a growth rate in the 0.15 to 0.20 micron per minute range for 950° C operation, and 0.18 to 0.25 microns per minute for runs at 1000° C; together with those conditions which minimized polysilicon nucleation on the mask layer.

Table 4.1 presents comparisons of CLSEG and ELO growth rates taken from the same wafer for runs on both types of reactor. The test pattern is



Figure 4.2 Growth rate of ELO versus $[pp_{HCl}]^2/[pp_{DCS}]$.

38



39

Figure 4.3 Growth rate of ELO versus masking oxide thickness.

identical among all the data, so that loading effect does not change within this comparison. However, gas flow rates, deposition temperatures, and deposition pressures are not equal between the two reactors so that a meaningful comparison is not possible. The purpose of this table is merely to demonstrate that ELO and CLSEG growth rates are similar regardless of reactor type, indicating that similar processes are at work. The data for the barrel reactor represent averages of 5 points over three wafers in identical epi runs.

While considerable variability is present in these measurements, the general trend is consistent. In either reactor, CLSEG in cavities roughly 1.0 microns high has a growth rate within 10% of the ELO growth rate. These data are significant as they indicate that the silicon transport mechanism and growth mechanics for CLSEG and ELO are the same. In section 6.1.1 of Chapter 6, the implications of these findings on the understanding of selective epitaxial growth are considered more thoroughly.

In the Chapter 2, it was noted that SEG growth rates depend on the average oxide thickness over a rather large area (roughly 400 microns radius). In Table 4.2 the effects of different bottom oxide and top nitride layer thicknesses is seen on both CLSEG and ELO growth rates. All data is from cavities using poly or α -Si as the sacrificial layer, and were grown in a barrel reactor at 950° C and 50 Torr pressure. For this range of thicknesses, growth rates decrease with increasing thickness of either oxide or nitride.

Table 4.3 shows a similar result for a pancake reactor at 950° C and 150 Torr. In this experiment, only the top layer was changed. Using an N⁺ LTO sacrificial layer with either a nitride alone, or a nitride plus LTO top layer, the growth rate changes by 7%. Thus it is possible to fine tune the growth rate by adjusting the masking layer thickness, or to have different growth rates at different points across a wafer. Another interesting result is the effect cavity height has on growth rates. In a pancake reactor at 950° , 150 Torr, averaged growth rate drops only 11% (from 0.231 to 0.207 microns/minute) when the cavity height shrinks 66% from 1.04 to 0.35 microns. It is worthwhile to note that the N⁺ LTO sacrificial layer etched out at roughly the same rate also for both cavity heights.

This weak dependence on cavity height is rather surprising, and begs the question of how thin can a cavity be made and still receive appreciable growth. When etching out a cavity with N^+ LTO as the sacrificial layer and nitride over thermal oxide as the bottom layers, the bottom layer oxide gets etched out a short distance (about 2 microns) under the nitride. Even though this gap under

Epitaxy run Parameters	$egin{array}{c} { m CLSEG} \ { m growth \ rate} \ (\mu{ m m/minute}) \end{array}$	ELO growth rate $(\mu m/minute)$	difference in growth rate in percent
Pancake, 950° 150 Torr xp24-3,4	0.185	0.173	+ 6.7%
Pancake, 950° 150 Torr xp27-1	0.160	0.145	+ 9.8%
Barrel, 950° 50 Torr xp25-1	0.195	0.215	- 9.8%
Barrel, 1000° 50 Torr various xp28	0.253	0.252	+ 0.8%

Table 4.1 Comparison of CLSEG lateral growth rate to ELO vertical growth rate.

Table 4.2 CLSEG growth rate versus thickness of top and bottom layers for a barrel reactor at 950° C and 50 Torr.

GROWTH RATES (μ m/minute)				
Bottom oxide thickness (nm)	top nitride thickness (nm)	CLSEG	ELO	
132	110	0.238	0.266	
250	120	0.195	0.215	
250	200	0.181	0.207	

Table 4.3 CLSEG growth rate versus top layer thickness in a pancake reactor at 950° and 150 Torr.

Top layer	CLSEG growth rate	
147 nm nitride	0.192 μ m/min	
100 nm nitride		
100 nm LTO	0.179 $\mu m/min$	

the nitride is only 0.1 microns high, it fills with epitaxy during CLSEG growth. This indicates that cavities at least this thin can be filled with CLSEG.

The final consideration of CLSEG growth rate is its dependence on lateral cavity width. The CLSEG test structures on each die site across the wafer include a bank of cavities whose widths extend from 3 to 12 microns in 1 micron increments. After CLSEG growth in a barrel reactor at 1000° and 50 Torr, the top layers were etched off, and CLSEG widths measured with a split-image manual linewidth measurement system. Growth rates in cavities from 3 to 12 microns were measured twice each, and then repeated at three neighboring die sites, and the results averaged. Figure 4.4 shows the data graphed as growth rate versus cavity depth. The most interesting result here is that growth rate only deviates $\pm 1.07\%$ from the average value for cavity widths differing by a factor of 4. The curve drawn through these points is for visual clarity only, since the relative error is of the same magnitude as the variance of the data. However, the smooth (not discontinuous) nature of this curve may suggest a trend. The maximum "slope" to the data occurs between the points for 8 and 11 micron cavities. If we discount the 12 micron cavity width on account of it being on the edge of the test pattern, we can extrapolate this slope to find at what cavity width the growth rate would be zero. The intercept on the cavity width axis for this crude analysis is 101 μ m. This corresponds roughly to the range of silicon adatom diffusion lengths cited by several authors. Of course a cavity 100 microns wide would not be supported with the current materials and design. The longest cavities made to date are 20 microns wide; which do have CLSEG growth inside; but sag considerably.

4.1.3 Aspect ratio

The original concept for CLSEG arose out of a need for the high aspect ratios (> 5) unattainable with ELO technology. Early development work on CLSEG focused first on attaining aspect ratios large enough to begin building devices in the lateral silicon-on-insulator regions. Through a steady progression of advancements in cavity construction and design, CLSEG films with aspect ratios of 8 are now attained routinely for films 1.0 microns thick. CLSEG 8 microns wide gives enough area to fabricate a wide array of semiconductor devices using 2.5 micron lithography. Figure 4.5 shows two SEM cross-sectional micrographs of cleaved CLSEG samples, demonstrating a roughly 8:1 ratio of lateral to vertical dimensions. The highest aspect ratios attained to date were



Figure 4.4 CLSEG growth rate versus cavity depth (width).





achieved with cavities 0.25 microns high, and lateral growth of about 7 microns, shown in Figure 4.6. Unfortunately, the nitride top layer lifted up at the end of the cavity to 0.5 microns. Thus the aspect ratio is at least 14, but less than 28. This is a new result for as-grown films.

Aspect ratios near 10 should be sufficient for many local SOI applications and for making whole-wafer SOI as will be described in section 6.2.1. However, higher aspect ratios may be desirable for increasing design flexibility. This involves making the cavity either thinner or wider or both. The evidence above indicates that cavities as thin as 0.1 micron can be filled; and thinner cavities than this are probably not needed for MOS or bipolar devices. If thinner cavities are needed for quantum silicon devices, the CLSEG films can be further thinned by oxidation or etching. The lateral limit to growth will be imposed either by cavity construction or growth conditions. Cavities built using the design and materials of Figure 3.3 are limited to 15 microns before top layer sag chokes off the cavity. It may be possible to extend this distance indefinitely by periodically providing a support pillar in the top layer (this is done by leaving a tiny hole in the sacrificial layer exposing the bottom layer). Of course, this pillar may interrupt the lateral growth, causing defects and non-useful area. Etch selectivity is also a concern for very wide cavities since the top and bottom layers will be exposed to the sacrificial layer etchant for long periods of time. possibly jeopardizing their strength and integrity. The limit due to growth mechanics is difficult to estimate due to lack of a cogent theory of silicon transport during selective silicon epitaxy. If adatom diffusion lengths are indeed on the order of 50 or 100 microns, then perhaps cavities this deep can be filled. Such an epi run would take at least 3 hours, and deposition selectivity must be made nearly perfect to avoid nucleation-induced defects. Attaining higher aspect ratios in CLSEG is probably better justified as a means for understanding SEG transport and growth mechanisms.

4.1.4 Faceting

Faceting in SEG growth was a major concern for many years because the nonplanar facets made diffusion control and lithography more difficult. Currently with $\{001\}$ oriented seed holes on <100> wafers, SEG at reduced pressures and low temperatures can be made facet-free quite readily [94]. Faceting in ELO over the mask layer is deleterious since it makes the task of thinning or planarization very difficult. Yet, in ELO, control of faceting by



Figure 4.6 SEM cross sections showing high aspect ratio CLSEG films.

adjusting the HCl gas flow during a selective epitaxy run, enabled adjacent ELO growth fronts to be merged without leaving a void at their juncture [38]. Recent work at Purdue University has shown this to be possible without the need to adjust HCl gas flows [91]. In CLSEG, faceting does not present a problem because the usable top surface will be kept planar by the top layer. In fact, as seen in Figure 4.5, the only facet visible in the CLSEG growth front is the <010> plane (perpendicular to the <100> substrate). This indicates that within the cavity, for the growth conditions used, the growth rate of the <001> plane is slowest (except in the corners) and thus defines the shape of the growth front. However, Figure 4.7 shows an interesting cross section where the via hole, behind the plane of the cleavage, has been overgrown by ELO, with its characteristic faceting. The shape of this ELO shows a predominant <011> facet, indicating that outside the cavity, the <011> growth rate is now the slowest. A tentative explanation of this phenomenon will be offered in chapter 6.

4.1.5 Uniformity

The uniformity of SOI film thickness is of utmost importance to the performance of devices built in these films. Thickness affects channel mobility for MOSFETs, breakdown voltages of junctions, parasitic resistances, and other electrical properties. A significant advantage of CLSEG is that the final film height is independent of the epitaxial growth rate. This makes CLSEG tolerant to non-uniformities in temperature and gas flow which must be tightlycontrolled in conventional SEG. CLSEG achieves this by converting any growth rate inconsistencies into changes in lateral dimensions, which are typically less critical to SOI device performance. However, sagging and deflection of the top layer can erode this important advantage.

Figures 4.5 through 4.7 show several CLSEG growth and are fairly representative of observed behavior. Lifting of the top layer is seen in Figure 4.6; and a slight decrease in CLSEG film thickness can be observed in Figure 4.5 due to top layer sag. The sag or deflection of the top layer is a function of film thickness, film stress, cavity design, and many other variables; and can be observed prior to CLSEG growth under Nomarski-polarized light. Rainbow bands of color appear in the top layer as its height above the bottom layer changes. Figure 4.8 shows two extremes of this effect; the top photo (with spinon-glass as top layer) showing enormous fluctuations, while only a few bands are



50

Figure 4.7 SEM cross section showing ELO overgrowth at end of CLSEG cavity.

 visible in the bottom photo (oxide and nitride as top layer). The best results observed so far show roughly 10% or less change in film thickness across an 8 micron wide SOI film, in a cavity 12 microns deep. This non-uniformity is a local effect and is reproducible across an entire 5 inch diameter silicon wafer since it does not depend on the growth rate. Compared to thinned ELO, this represents a trade-off in growth non-uniformity. For ELO, changes in growth rate across a substrate translate into non-uniformities of thinned film thickness; whereas in CLSEG these variations translate into different cavity widths - a less critical dimension. The 10% local non-uniformity of CLSEG due to top layer deflection is probably acceptable for circuit fabrication, but further improvements in this area would be very beneficial.

4.1.6 Morphology and defects

A great deal of information about the quality of the epitaxy can be deduced from a visual inspection. Such defects as "haze" or stacking faults are immediately visible under a bright light, and especially highlighted using Nomarski microscopy. This holds true for CLSEG as well: smooth surfaces, crisp faceting and uniform growth fronts are generally indicative of good quality silicon crystal.

Visually-good CLSEG and ELO from both reactors has been obtained. Yet, as will be discussed in section 4.2.3, devices in pancake-grown CLSEG are generally inferior to barrel-grown material. The reason for this is believed to be the higher minimum deposition pressure for the pancake reactor, but could also be caused by the difference in heating methods between the two reactors, or by uncertainty in the measurement of the actual deposition temperature. In principle, the lower deposition pressures should lead to fewer defects and higher electrical quality epitaxy. Experiments to elucidate pressure dependence are ongoing.

The observed types of defects which do occur in CLSEG, ELO, and homoepitaxy differ between the two reactors. Homoepitaxy grown in the pancake reactor is smooth and specular, but the facets in the ELO regions are slightly scalloped with an occasional edge defect. These edge defects appear to be stacking faults which originate at the seed hole edge and leave a triangularshaped notch in the ELO growth front. Pancake-grown CLSEG also experiences occasional irregularities in the growth front which leaves a jagged edge, in extreme cases. These CLSEG defects presumably originate at the seed hole edge



Figure 4.8 Photomicrograph of empty cavities prior to CLSEG growth, showing extreme deflection (top) and no deflection (bottom).

(a)

(b)

52

and then propagate along the growth front, as in ELO. Barrel-grown homoepitaxy is shiny, but exhibits vague rounded squares with visible diagonals, somewhat reminiscent of stacking faults. ELO and CLSEG in the barrel reactor are remarkably clear of visible edge defects and have regular, even growth fronts.

A standard procedure in evaluating epitaxy is to use a defect decoration etch. The Wright etch is commonly used for epitaxy in $\langle 100 \rangle$ silicon, and was used on barrel-growth epitaxy to reveal the nature of growth defects. This decoration etch showed first that the rounded squares on homoepitaxy did not get preferentially etched, and so are not stacking faults. This phenomenon has been observed by others [38] and is explained as a perturbation in the growth caused by a tiny patch of SiO₂ left on the substrate surface prior to growth. The homoepitaxy overgrows this patch (like ELO), and continues growing; nondefective but slightly lagging the growth around it. The result is a divot or small depression in the epitaxy surface which appears as a rounded square, but is not a surface defect. The SiO₂ patch presents a problem only if intersected by a depletion region, and should be removed prior to growth by an optimized pre-clean.

None but a rare defect is revealed in CLSEG or ELO lateral regions by the Wright etch. However, a moderate density of small defects are observed directly over the seed hole edges on CLSEG only, not on ELO. These defects do not appear to propogate through the CLSEG, so are probably not formed at the seed hole edge in the bottom layer, but may be generated by the perturbation in the top layer, as discussed in section 3.2.3. SEM photographs of CLSEG occasionally show very shallow triangular features in the top surface of the CLSEG over the seed hole edge (see for example Figure 4.5). Further, since ELO is free of defects in this case, this lends further credence to the theory that these CLSEG defects arise at the top layer. A possible solution to this source of defect is to coat the sacrificial layer with planarizing spin-on-glass before depositing the top nitride layer. This will help to smooth out the perturbation in the top layer and perhaps reduce defect generation there.

4.1.7 Cavity end effects

At either end of the cavity CLSEG growth front is angled, resulting in a trapezoidal shape to the lateral growth. Figure 4.9 is a micrograph which shows the end effects in CLSEG and how devices are formed in the center of this slab,

away from the ends. Using the layout of Figure 3.3, and by placing the via holes closer to or further from the ends of the cavity, this effect can be exacerbated but not improved. If unavoidable, this end effect could be a distinct disadvantage to CLSEG.

For CLSEG 8 microns wide in the center, this end effect will extend 8 to 10 microns in from the end of the cavity. The slope or angle of this leg of the trapezoid, measured from a line parallel to the seed hole is typically in the range $[35^{\circ}, 42^{\circ}]$ regardless of reactor type, but is a slightly larger angle on average for pancake-grown CLSEG. If this were a crystal facet, one would expect it to be either the <110> at 45° or the intersection of the <311> plane with the <001> surface of the bottom layer at 18.4°, both of which are commonly observed in ELO and SEG, and depend on gas flow ratios and other conditions. A test structure was used to investigate the effect of via hole layout on the angle of the end effect. If, at the side end of the cavity, the edge of the via hole is parallel to the edge of the seed hole (as in Figure 3.3), the end effect angle is at a maximum. If the via hole is moved away from the end of the cavity, the end effect angle becomes more acute. This behavior can be explained qualitatively as follows. Regular ELO grown from a square seed hole forms an octagonal outline with <110> facets defining the edges diagonally away from the corners of the $\{001\}$ oriented seed holes. This facet is thus assumed to define an upper limit to the angle of the CLSEG end effect, at least with the current layout design. Then, as the via hole is moved away from the cavity end, the supply of silicon containing species causing epitaxial growth is reduced, resulting in an end effect angle of less than 45° . In section 4.3, a new design is presented to potentially correct or at least minimize this undesireable effect.

4.1.8 Merged CLSEG

Figure 4.10 shows one of the more interesting applications of CLSEG, that of merging the growing silicon from two facing cavities. The dark horizontal bar surrounded by lighter-colored material in the SEM photograph is a gap left after the bottom oxide was etched out in this cleaved cross section. The light material above the dark bar is single-crystal silicon grown from facing cavities and merged in the center. No void or preferential cleavage is evident on the merge plane, indicating potentially device-quality material there. The large faceted blocks above the merged CLSEG are the ELO which grew out of the via holes just behind the plane of the cleave. These ELO bumps can be readily



Figure 4.9 Micrograph of CLSEG slabs showing end effect.

 $\{\lambda_i\}_{i \in \mathbb{N}} \leq \lambda_i$



Figure 4.10 SEM cross section of merged CLSEG with ELO in background.

planarized or polished off, leaving an SOI film that is twice as wide as possible with a single CLSEG growth (14 microns in this case). This CLSEG merging technique is used to advantage, as described in section 6.2.1, to make wholewafer SOI using a two step epitaxy process.

4.2 Electrical Properties of CLSEG

The ultimate goal of CLSEG fabrication and crystal growth is to use the silicon material for building semiconductor devices of high quality. This section presents the results of CLSEG characterization via electrical evaluation of devices built in CLSEG. The first two subsections describe the device construction and the measurement techniques used to extract device parameters. Following this are the actual results, together with the effects that various design and process steps have on electrical parameters.

4.2.1 Device fabrication and layout

The design rules for device layout on CLSEG, homoepitaxy, and substrate silicon use a 2.0 micron minimum feature size, with an alignment tolerance of 1.25 microns. Minimum device sizes are limited by contact hole dimensions $(2.0\times2.5\text{microns})$ and by metal pitch (4.5 micron lines + 4.0 micron spacing). Three microns was the minimum spacewidth used on dark field masks (using positive photoresist); and CLSEG slabs were 8 microns wide with cavity lengths extending 12 microns beyond the device regions to allow for end effects.

Each type of device fabricated (diode, MOSFET, bipolar transistor) was laid out with at least three sizes; a minimum area device following the design rules, a slightly larger one with more generous tolerances, and a much larger device with typically 5 times the area of the minimum device. The final devices required 7 mask levels, three for cavity formation, one each for n-type and ptype regions, and one contact and one metal mask. Layout of the last 4 masks, which define the devices, was repeated identically on a CLSEG slab, on a large area homoepitaxy island, and on the substrate. This allows for control devices for comparison with CLSEG devices, which provide a basis for evaluation of CLSEG material quality. An important note to consider when laying out future mask designs is that photoresist will have different thicknesses over the substrate than over CLSEG, than over ELO. It may be prudent to bias mask sizes accordingly. Figures 4.11, 4.12, and 4.13 show the minimum size layout plus schematic cross sections in CLSEG, homoepitaxy, and substrate silicon of the diode, MOSFET, and bipolar junction transistor (BJT) respectively, used for this work. Note that the substrate silicon is actually a 5 micron n-doped epilayer grown on a <100> CZ wafer using standard conventional epitaxy conditions. The three types of devices are fabricated simultaneously using the process flow described in detail in Appendix A. In brief, for generic materials, these steps following the n-doped CLSEG and homoepitaxy growth are:

(a) remove top layer(s)

(b) optionally remove bottom layer(s)

(c) perform post-epi oxidation (at various temperatures)

(d) mask and implant p-type region

(e) mask and implant N^+ region

(f) anneal implants and oxidize at 900° C

(g) mask and etch contact windows

(h) deposit, mask, and etch metal

(i) microalloy (sinter) at 450° C in N₂/H₂.

The boron p-type regions define the diode, the MOSFET source and drains, and the BJT base regions. The N⁺ regions are arsenic, and form the BJT emitter and ohmic contact to the n- doped CLSEG, homoepitaxy, and substrate regions. Typical film thicknesses are: $t_{oxide}=250$ nm over the N⁺ regions; $t_{oxide}=130$ nm elsewhere; and $t_{metal}=1000$ nm for Al/Cu/Si metallization. The p-channel MOSFETs use a non-self-aligned metal gate over the 130 nm gate oxide.

4.2.2 Measurement techniques

Several electrical parameters were used to make comparisons between devices and to assess crystal perfection. One of the most sensitive and easily compared parameters is the junction ideality factor (η) , which is extracted from the diode forward characteristics by empirical fit to the Schockley equation:

$$I_{\rm D} = I_{\rm S}[\exp(qV_{\rm D}/\eta kT) - 1] \quad (3)$$

where I_D and V_D are the diode current and voltage, I_S is the saturation current, and kT/q is the thermal voltage. For the BJT, η for the emitter-base junction was extracted from the Gummel plot. The Gummel plot graphs base current and collector current against a voltage which is applied simultaneously to the base and the collector with the emitter grounded. DC current gain (β) versus



59

Figure 4.11 Minimum layout of diode and cross section in (a) CLSEG, (b) homoepitaxy, and (c) substrate material.



Figure 4.12 Minimum layout of MOSFET and cross section in (a) CLSEG, (b) homoepitaxy, and (c) substrate material.



Figure 4.13 Minimum layout of bipolar transistor and cross section in (a) CLSEG, (b) homoepitaxy, and (c) substrate material.

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collector current is also extracted from the Gummel plot as the ratio of I_C to I_B at a given voltage.

P-MOSFET threshold voltage (V_T) is obtained by measuring drain to source current (I_{DS}) versus gate voltage with -0.1 volts applied to the drain. The linear region of this curve is extrapolated back to zero drain to source current to find V_T . Carrier mobility for holes (μ_p) is derived from the slope of this curve (the transconductance g_m) using:

$$\mathbf{g}_{\mathbf{M}} = \frac{\delta \mathbf{I}_{\mathbf{DS}}}{\delta \mathbf{V}_{\mathbf{GS}}} = \frac{\mathbf{Z}}{\mathbf{L}} \mu_{\mathbf{p}} \mathbf{C}_{\mathbf{i}} \mathbf{V}_{\mathbf{DS}} \qquad (4)$$

where Z and L are the channel width and length respectively, and C_i is the gate capacitance per unit area. Subthreshold slope (S) for the P-MOSFET is also obtained from this plot, allowing two important parameters to be extracted from the same measurement. As the channel region first begins to conduct, I_{DS} increases exponentially at first. By measuring the semilog slope of this curve, S is derived from:

$$S \equiv \ln 10 \times \Delta V_{\rm G} / \Delta (\ln I_{\rm D}) \qquad (5)$$

Leakage currents for diodes were taken from a sweep of reverse bias; and for BJTs and MOSFETs as the collector-to-emitter or drain-to-source current with the base current or gate voltage set to zero respectively, respectively. Output curves for BJTs and MOSFETs were set up as for leakage currents above, but a family of curves is generated by stepping either the base current or gate voltage, as the case may be.

Collector resistance (r'_{C}) for BJTs was measured using Gertrue's method [104], where the voltage between points of equal β on a plot of I_{B} versus V_{CE} is divided by the difference in collector current between the points. This method reputedly gives the best agreement with calculated values of r'_{C} .

In the next subsection, we consider the effects of process variables on CLSEG diode behavior in some detail. The ensuing two sections then discuss performance of MOSFETs and BJTs in CLSEG material as compared to control devices. The final section will serve as a review for this lengthy chapter and summarize the conditions which have produced the best CLSEG films and devices.

4.2.3 Process effects on CLSEG diodes

Diodes were the primary measuring tool used for CLSEG material characterizations. In this subsection, processing and design influences on the diode ideality factor are considered predominantly. This easily measured device parameter (η) is a practical barometer of crystal quality. It is relatively insensitive to surface effects, is independent of device dimensions (for large enough areas, i.e. >10 microns²), and has a small variance across a wafer. Eta (η) is numerically equal to 2.0 in poor material, and approaches unity (1.0) in ideal high-quality crystal; indicating that forward diffusion current dominates recombination currents. Reverse leakage current (I_o measured at -3 volts) was also used, to evaluate surface effects on CLSEG diodes.

Table 4.4 is a compilation of CLSEG diode data taken over a 12 month period. Listed by column are the wafer lot and number, the cavity height, the sacrificial layer material, the reactor type used and its temperature, the treatment of the bottom layer (removed or intact) before the anneal, and temperature of the post-epi anneal/oxidation, the relative size of the implant dose, and the implant energy. On the right is the ideality factor (η) with the sample standard deviation and sample size, and the reverse leakage current density, if applicable.

One persistent issue in this study was the choice of epitaxy reactor type. Since both types of reactor were used for the results below, the question of comparing machines must be addressed. It should be noted that epitaxy conditions for either reactor were optimized solely for growth selectivity; no attempt was made to optimize epitaxy conditions for device performance. While CLSEG growth results are nearly identical from the pancake or the barrel reactor, electrical behavior of devices may be different. The pancake heats the wafer from below, the barrel from above; and this could cause important differences in the silicon growth along the top cavity wall. Such a disparagy was not the subject of this work. However, several tentative conclusions can be drawn. Results from wafer 18/2 (lot # / wafer #) agree very closely with wafer 21/3, both with an LTO sacrificial layer. The process flow for each lot was virtually identical except that lot 18 was grown in a pancake reactor at 150 Torr, and lot 21 in a barrel reactor at 50 Torr (both at 950° C). A comparison of 22B/7 and 24/4 with a polysilicon sacrificial layer shows similar results. However, the excellent η values from wafer 28/8, obtained with barrel-grown CLSEG at 1000° C and 50 Torr are better than any results so far from pancake-grown material. Still, it is very likely that further optimization to the

wafer	sac.	R&T	B&T	Imp	<u> </u>	J,	N
16/1	1.12 L	P950	R 950	P- 73	1.46 +.06	.000306	6
18/2	1.1 L	P950	R 900	P- 75	$1.22 \pm .02$.000617	6
21/3	1.13 L	B950	R 900	P- 75	$1.23 \pm .08$.00106	7
22B/7	1.09 P	B950	R 900	P- 75	$1.34 \pm .05$.000021	7
24/4	1.09 P	P950	R 900	P- 50	$1.43 \pm .05$	-	7
24/6	1.09 P	P950	R 900	P- 50	$1.43 \pm .19$	-	7
25/2	1.04 P	P950	R 900	P- 55	$1.89 \pm .08$	•	6
25/7	0.35 P	P950	R 900	P- 55	$1.20 \pm .02$		5
27/4	_0.98 A	P950	I 1200	P- 55	$1.64 \pm .04$	-	4
27/8	0.98 A	P950	R 1200	P- 55	$1.60 \pm .10$	-	7
27Ś/5	0.98 A	P950	I 450	P- 55	$1.64 \pm .08$	-	10
27S/5	0.98 A	P950	R 450	P- 55	$1.23 \pm .07$	_	5
27S/6	0.98 A	P950	I 450	P- 55	$1.53 \pm .16$	-	15
27S/6	0.98 A	P950	R. 450	P- 55	$1.29 \pm .06$	-	9
27T/1	0.98 A	P950	I 900	P- 5	$1.36 \pm .11$	-	5
7T/10	0.98 A	P950	I 450	P- 55	$1.57 \pm .07$	-	6
27T/7	0.98 A	P950	R 900	P- 55	$1.43 \pm .12$	-	8
28/11	0.86 A	B1000	I 900	P+ 55	$1.05 \pm .02$.000137	25
28/12	0.86 A	B1000	I 1000	P+ 100	$1.09 \pm .02$.00675	8
28/13	0.86 A	B1000	R 1000	P- 55	$1.11 \pm .01$.000040	9
28/5	0.86 A	B1000	R 900	P- 55	$1.18 \pm .0$.000010	6
28/6	0.86 A	B1000	R 900	P+100	$1.14 \pm .07$.000627	28
28/7	0.86 A	B1000	R 900	P+ 55	$1.14 \pm .01$.00832	6
28/8	0.86 A	B1000	R 1000	P+ 55	$1.05 \pm .01$.000056	11
28/9	0.86 A	B1000	R 1000	P+ 100	$1.14 \pm .02$.00435	8

Table 4.4 CLSEG diode ideality factors versus process and design parameters (see below for key).

Notes: (1) wafer is lot #/wafer #, (2) sac. is cavity height and sacrificial layer material; L for LTO, P for poly, and A for α -Si, (3) R&T is the reactor type and temperature; B for barrel and P for pancake, (4) B&T is the bottom layer treatment; R for removed, and I for intact, with the temperature of the postepi anneal, (5) Imp. is the implant type and relative dose with the implant energy in keV, (6) η is the ideality factor with sample standard deviation, (7) J_o is the reverse leakage current density in A/cm² taken at -3 volts, (8) and N is the sample size. Also, samples with T=450° C are Shottky diodes.

pancake reactor, and upgrades which are currently in progress, with generate equivalent results.

Current understanding of SEG sidewall leakages presumes that sidewall defects extend 0.5 to 1.5 microns from the SEG/insulator interface. Viewing CLSEG as SEG in a very small seed window of great depth, one would expect such defects to pervade the film, and that leakage currents would be very large. Thus, a negative dependence of material quality on the cavity height might be expected a priori (although in almost all cases the top layers were removed and thermal oxide grown on the CLSEG). This however, is not bourne out by the available data. Measurements of wafer 25/7 display the best average η value of all pancake-grown material, yet the cavity height was only 0.35 microns high, compared to a typical 1.0 micron height. Also, for the barrel reactor, the best results were achieved with slightly thinner films (0.86 microns). While much of these differences are certainly due to intentional and random process variations, it seems that at least, smaller cavity heights do not impair crystal quality in this range of heights. This agrees qualitatively with the growth results above, where growth in cavities of height down to 0.1 micron behaved very similarly.

It was seen in Chapter 2 that SEG sidewall defects are a strong function of sidewall material choice and surface roughness of the sidewall. In CLSEG processing, the top wall material is chosen appropriate to the sacrificial layer used; LP nitride is used on top of LTO, and thermal oxide (capped with LP nitride) is used on poly and amorphous silicon. While little difference in η values is seen between comparable poly and α -Si samples, there is a noticeable difference between poly and LTO. Comparing wafers 21/3 and 22B/7, the process variables are nearly identical except for the choice of sacrificial and top layer materials. Eta from the LTO devices is lower than from the poly devices. It was this difference that eventually led to the use of amorphous silicon as a sacrificial layer to form a smoother thermal oxide top layer, as compared to the roughness observed with oxidized polysilicon. Note that a-Si becomes polycrystalline at temperatures above 600° C, but the grain size is typically much smaller than as-deposited poly. The reverse leakage currents are approximately two orders of magnitude higher from the LTO devices than from the poly devices. This is to be expected from SEG studies which show that nitride sidewalls (top walls in this case) produce diodes with much higher leakage currents than oxide sidewalls. These results indicate that CLSEG diode performance is better with a smooth top cavity surface composed of thermallygrown silicon dioxide. These principles are exploited further in the One-mask step CLSEG process describe in Chapter 7.

Figure 4.14 shows a plot of ideality factor (η) versus post-epi anneal temperature $(T_{post-epi})$ for two cases: (1) bottom layer removed; and (2) bottom layer left intact, before post-epi anneal. This data was taken from devices implanted into pancake-grown CLSEG at low dose and 55 keV energy, all in the same wafer lot. There are several interesting phenomenon evident here. First, it is important to note that the values to 450° C are taken from non-annealed Shottky Al-Si diodes, and may not be comparable to the junction diode values at higher temperatures in Figure 4.14. At the low temperature end, removal of the bottom layer improves η values considerable. This was verified by nearly identical results from identical wafers 27S/5 and 27S/6 which were measured before and after bottom layer removed with no anneal other than microalloy of the metallization. As a result, each wafer has two lines in Table 4.4 This reduction in η value with bottom layer removal probably indicates the elimination of residual thermal stress in the CLSEG film. At elevated growth temperatures, the CLSEG silicon will partially bond to the oxide walls. When this structure is cooled, the different expansion coefficients of silicon and SiO_2 can then generate stress within the CLSEG. At 1200° C, the crystal quality of the CLSEG has degraded severely, and does not appear to depend on bottom layer treatment. At the more reasonable temperature of 900°, we see that η may be reduced if the bottom layer is left intact. The dependence of η values on bottom layer treatment in this range is more clearly seen in the data from lot 28.

A cursory look at the data from wafer lot 28 shows that removal of the bottom layer increases η values in this range of anneal temperatures. Comparing 28/11 to 28/7 and 28/12 to 28/9 shows an average increase of 0.07 in η with bottom layer removal. A more sophisticated analysis of this fractional factorial data (using lot 28 wafers 6,7,8,9,11, and 12) shows that, ignoring interactions between variables, bottom layer removal adds approximately 0.04 to η independent of T_{post-epi} and implant energy, within the ranges explored in lot 28. A proposed explanation of this phenomenon is discussed in Section 6.1.2.

So far, we have seen the effects of reactor type, cavity height, top layer material, and bottom layer treatment on CLSEG diodes. Now with each of these four variables held constant, we can assess the impact of post-epi anneal, natural logarithm of the implant dose (D_{ln}) , and the implant energy (E) on CLSEG diodes. This should provide direction for continued optimization of the CLSEG process. Wafers 5,6,7,8, and 9 from lot 28 vary only in these three process variables, and were fit in a least squares error manner to the following linear non-interactive model:



Figure 4.14 Ideality factor versus post-epi anneal temperature with the bottom layer removed and intact, for CLSEG grown in a pancake reactor at 950° C and 150 Torr.

$$\eta = \mathbf{b}_0 + \mathbf{b}_1 \times (\mathbf{T}_{\text{post-epi}} - \mathbf{T}_{o}) + \mathbf{b}_2 \times (\mathbf{E} - \mathbf{E}_{o}) + \mathbf{b}_3 \times (\mathbf{D}_{\ln} - \mathbf{D}_{o})$$
(6)

This analysis involved derivation of the least square error method to this model, and the solution of a 4×4 matrix. The reference values (T_o, E_o, D_o) were each chosen as the midpoint of the extreme values of each parameter; with the result: $\eta=1.142-.000555\times(T_{post-epi}-950)+.000948\times(E-77.5)-.00856\times(D_{ln}-33.07)$ (7)

A figure of merit for goodness-of-fit is the square root of the sum of the squares of error for each data point, divided by the number of data points; and was 0.0088 for this analysis. A more practical figure of merit is simply the average error of individual errors, which was calculated to be 0.020. This indicates that, on average, the model in equation 7 will have an error of this size in predicting η under the above range of conditions. This allows us to draw several insights into the nature of CLSEG diodes. Foremost is the negative dependence of η values on anneal temperature between 900 and 1000° C. Although this is at odds with the wide range of temperatures covered in Figure 4.14, it agrees well with published data on trench oxidation, where oxidation-induced defects decrease at higher oxidation temperatures. It may be that 1200° C is beyond some critical temperature at which CLSEG silicon degrades. This

The dependence on implant energy and (logarithm) dose agrees with a model in which η values are sensitive to implant damage. Higher implant energies impart more damage to the crystal, hence the positive coefficient on the \mathbf{E} term in equation (7). Higher implant doses (at the same energy, and receiving the same anneal), will have steeper concentration gradients, and so will experience more diffusion during the anneal. This will then drive the p-n junction deeper into the CLSEG, and further from the implant damage; resulting in improved η values. If one applies equation (7) to wafers 28/11 and 28/12, which have the bottom oxide intact, the measured values of η are smaller than predicted by 0.05 and 0.09 compared to the case with the bottom oxide removed. On the average, this indicates that bottom oxide removal increases η values by 0.07 within the specified ranges of post-epi anneal temperature, implant energy, and implant dose. Thus, for better CLSEG material quality in this middle temperature regime, one should leave the bottom oxide intact. Such a practice seems to prevent the oxidation-induced defects or mechanical stresses incurred when growing an oxide on the underside of a CLSEG slab.

In general, η values for CLSEG diodes were equal or slightly higher than for homoepitaxy or substrate diodes. A useful comparison is the η andJ_o values for

diodes in each of the three materials, taken from the wafer with the best overall CLSEG diodes. From wafer 28/8 η values for CLSEG, homoepitaxy, and substrate diodes are $1.05\pm.01$, $1.04\pm.01$, and $1.07\pm.01$ respectively, with sample sizes of 11, 12, and 12, respectively. The average values for J_0 were .0000555, .000840, and .000695 A/cm² for CLSEG, homoepitaxy, and substrate diodes, but the sample variances were much larger for the last two values. It appeared that these diode leakage currents were all near a common value, but that a few spurious data points increased the averages for homoepitaxy and substrate diodes significantly. The important point to note here is that η values are very similar between diodes in different silicon material on the same wafer. This implies that, to the limit of the process capability, each of these materials is roughly comparable in quality, as measured by ideality factor.

An important consideration in any practical implementation of a new process such as CLSEG is the yield and parameter variation of a large number of devices. Figure 4.15 (a) is a histogram of ideality factor for CLSEG diodes both with the bottom layer removed and with the bottom layer intact. These values come from wafers 28/6 and 28/11 which were grown in a barrel reactor at 1000° C and 50 Torr, received a P⁺ implant $(3.5 \times 10^{15} \text{ cm}^{-2})$ at 55 keV, and a post-epi anneal at 900°C. Figure 4.15 (b) is a histogram of reverse leakage currents for the same devices. For each wafer, data was taken from one diode per test pattern die in a 5×6 array of die, which covered approximately 5 cm². These data show both lower values and tighter clustering of those values for the CLSEG diodes with the bottom layer intact. This is a further indication that keeping the bottom layer intact after the CLSEG growth is essential to high-quality CLSEG crystal. However, as we will see in Chapter 5, there are important applications in which the bottom layer must be removed to take advantage of the special features of CLSEG.

4.2.4 MOSFETs in CLSEG

The value of a MOSFET as an analytic tool for evaluating silicon material quality is as a test of the silicon surface. Extracted carrier mobility (μ_p) is a barometer of surface roughness and interface defect states, while subthreshold slope (S) is indicative of surface properties. Because oxidation of silicon (i.e. CLSEG) tends to ameliorate surface defects, sample MOSFETs were prepared in the as-grown CLSEG using the intact polyoxide top layer as the gate dielectric (top layer nitride was removed), without any high temperature steps. For these



Figure 4.15 Histograms of ideality factor (a) and leakage current (b) with and without the bottom oxide layer removed for barrel- grown samples at 1000° C and 50 Torr, with nitride on oxide as the top layer, and a cavity height of 0.86 microns.

devices, with 100 nm thick gate oxide and bottom oxide intact, S=172 mV/decade which is very near the ideal for this structure. However, the unannealed P-N junctions with bottom oxide intact were very leaky and good data on μ_p was not obtainable. Still, this result suggests that reasonable material quality may exist at the as-grown CLSEG/top oxide interface. This in an interesting area of study, and further work could be very rewarding.

CLSEG MOSFETs were fabricated simultaneously with homoepitaxy and substrate devices, and their characteristics compared. Table 4.5 shows these results, where it is important to note the difference in background channel doping between the samples; which is 2×10^{16} atoms/cm² for the CLSEG and homoepitaxy devices and 7×10^{14} atoms/cm² for the substrate devices. The sample size is N=6 for all values, except for the leakage currents which exclude one die site (so that N=5) due to spuriously high readings. Comparing these measured values against published results shows that for both CLSEG and homoepitaxy islands, both $\mu_{\rm p}$ and S are very close to the published data for substrate silicon [105]. The standard deviations are also given for each data point, which are averages over six devices. CLSEG devices show slightly better values than homoepitaxy devices, but this difference is too small to be attributed much significance. It is also interesting to note that the leakage currents at $V_{DS} = -2.5$ volts divided by the channel width (29 microns) gives subpicoamp/micron of channel width leakage currents. This is considered in the literature to be an excellent result for this figure of merit for SOI devices. The much higher leakage currents for the substrate device is due to the lower channel doping as compared with the CLSEG and homoepitaxy devices. At the channel length for these devices, approximately 3.1 microns, the substrate devices are close to a short channel regime. Figure 4.16 shows output curves and plots of $ln(I_{DS})$ versus V_{GS} (for S measurements) for representative devices in CLSEG and homoepitaxy silicon; showing nearly identical behavior. The principal conclusion to be drawn here is that CLSEG MOSFETs perform at least as well as homoepitaxy devices.

4.2.5 Bipolar transistors in CLSEG

Among semiconductor devices, the bipolar junction transistor (BJT) is perhaps the most sensitive to material quality because of the critical nature of minority carrier lifetimes to current gains. Vertical BJTs have been reported in thin SOI films which achieve moderate current gains ($\beta \le 100$) but which have large Table 4.5 Measured parameters from MOSFETs in CLSEG, homoepitaxy, and substrate silicon material.

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SILICON MATRIX	MOBILITY cm ² /V-sec	SLOPE mV/dec.	LEAKAGE pA	$egin{array}{c} \mathbf{V}_{\mathrm{T}} \ \mathbf{volts} \end{array}$
CLSEG	283 ± 15	223 ± 5	$28\pm.5$	-4.63±.04
НОМО	257±24	254 ± 44	28±1.6	$-4.59 \pm .03$
SUB	455±11	120 ± 9	17486	$-1.60 \pm .03$

Note: All values are averages from 5 or more devices.



Figure 4.16 Transistor output curves (a) and plot of $ln(I_D)$ versus gate voltage (b) for MOSFETs in CLSEG (left) and homoepitaxy (right) material.

ideality factors for one or both junctions, and large leakage currents. There is a strong need for high quality vertical BJTs in thin films to provide current drive and analog functions in tomorrow's SOI technologies. The two main issues inhibiting this development are the inferior material quality (discussed in Section 2.2.2) and the high value of parasitic collector resistance due to the lack of a buried layer. Lowered collector resistance is addressed in the next chapter under Advanced Device Studies, while material quality and BJT performance are discussed in this subsection.

The road to high gain, low η value junctions in BJTs made in CLSEG is strewn with wildly varying results. Early measurements of high current gain derived from Gummel plots are worthless because punchthrough currents dominated the transistor action, precluding any output curves. The best results were achieved with the conditions described in Table 4.4 with bottom oxide removed. This produced BJTs with maximum dc current gains averaging 400 with ideality factors averaging $\eta_{\rm EB}$ =1.067. These are by far the best values ever reported for BJTs built in thin SOI films. Figure 4.17 (a) shows the Gummel plot, (b) the β versus I_C curve, and (c) output curves for a typical device in CLSEG. Of particular interest is the relatively flat value of β over five orders of magnitude change in collector current. This is an indirect indication that recombination currents are relatively small for these CLSEG devices.

Another interesting aspect of these curves is the change in slope of the I_C output curves in Figure 4.14 (c), in the saturation region. A PISCES [106] computer simulation was performed to see if this behavior is real. Figure 4.18 shows the I_C versus V_{CE} output curve trace for three slightly different CLSEG BJT structures, all at 0.6 volts base-emitter voltage. The two traces with CLSEG thickness (T) of 0.87 microns show that, independent of the interface state density (QF) of the underside oxide, the collector current will cease increasing at approximately 2.5 volts. This is in excellent agreement with the measured results of Figure 4.17 (c). However, if the CLSEG thickness is increased to 1.07 microns, this phenonemon is not observed out to at least 5.0 volts. Also, if the thickness is reduced to 0.7 microns, the slope change occurs at $V_{CE} = 0.7$ volts. A hand calculation shows based on this structure (taken from spreading resistance profile data) shows that the onset of this slope change occurs when the base-collector depletion region contacts the underside oxide at a base-collector voltage of approximately 1.8 volts. This condition is reached when the collector-emitter voltage is 2.4 volts with a base-emitter voltage of 0.6volts, again coinciding with measured results. These results indicate that Early voltages may be appreciably larger for thin film SOI vertical BJTs than for a comparable device in bulk silicon. Table 4.6 compares the extracted parameters for BJTs in CLSEG, homoepitaxy and substrate silicon. Again, the background collector doping and geometry must be accounted for when comparing r'_C and BV_{CEO} .

The values of $\eta_{\rm EB}$ among the different materials is not necessarily an indication of different material quality. As the comparison of diodes within lot XP28 shows, the substrate material is of slightly better quality than the CLSEG or homoepitaxy material. The $\eta_{\rm EB}$ value is more useful as an indicator of the processing quality. In this case, the lower value for CLSEG material may be due to an increase in oxidation-enhanced diffusion resulting from the underside of the CLSEG being oxidized at the same time as the topside. This is supported by the diode results showing that higher implant doses (and hence greater diffusion) have a beneficial effect on CLSEG diodes. Breakdown voltage (BV_{CEO}) occurs via punchthrough for BJTs in homoepitaxy and CLSEG, and is taken as that voltage at which $I_{\rm C} = 1.0 \ \mu A$. For the substrate device, breakdown occurs via avalanche multiplication, and probably defines an upper limit to transistor breakdown in the epitaxy material devices.

Not shown in Table 4.6 are analogous results for a sample differing only in that $T_{post-epi}=1000^{\circ}$ instead of 900°. The homoepitaxy and substrate devices on this wafer were virtually identical to the results of Table 4.6, but for the CLSEG device: $\beta_{max}=685$ and $\eta_{EB}=1.22$. The final anneal was identical to the samples represented in Table 4.6, so different thermal cycles are not able to explain the observed increase in β_{max} . It could be that the higher temperature oxidation after growth induced defects which raised η , and perhaps affected base and emitter diffusion coefficients. The diffusion effects could have helped to reduce the basewidth in these devices, accounting for the higher β_{max} .

The excellent performance demonstrated by BJTs in CLSEG gives clear indication that the cavity layout and fabrication, and the subsequent device processing are the best obtained to date. In the next section, the parameters used for this achievement are summarized with suggestions for further improvement.

4.3 Best Conditions for CLSEG Fabrication

In obtaining the best results for semiconductor devices built in CLSEG SOI material, the layout scheme of Figure 3.3 was used with the following process parameters and considerations.









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PARAMETER	CLSEG	HOMOEPITAXY	SUBSTRATE
$eta_{ t max}$	400±18	404±23	171±9
ND	2×10^{16}	2×10^{16}	2×10 ¹⁵
$\eta_{ m EB}$	$1.07 \pm .01$	$1.11 \pm .02$	1.13±.03
BV _{ECO}	$3.8 \pm .9$	$3.1 \pm .1$	13.8 ± 1.1
$\mathbf{r'_C}$ (k Ω)	$2.7 \pm .2$	$1.18 \pm .7$	$1.3 \pm .6$
No. of samples	7	5	3

Table 4.6 Measured parameters from bipolar junction transistors in CLSEG, homoepitaxy, and substrate silicon material.

- (a) substrate: <100> n- doped "standard" epi 5.0 microns at 2 Ω -cm.
- (b) bottom layer: thermal oxide of 0.13 to 0.25 microns thickness.
- (c) seed hole: RIE etched with regrown oxide, oriented along $\{001\}$.
- (d) sacrificial layer: CVD amorphous silicon roughly 1.0 microns thick.
- (e) top layer: LP CVD silicon nitride 0.11 to 0.15 microns thick over thermal oxidation of α -Si to 0.10 microns thickness.
- (f) sacrificial layer etch: ethylene diamine.
- (g) CLSEG pre-clean: 5 min. at 975°, 50 Torr in 80 SLPM hydrogen.
- (h) CLSEG growth: barrel reactor, 1000°, 50 Torr, growth rate=0.22 μ/min .
- (i) post-epi oxidation: 900° in dry oxygen with bottom oxide layer intact.
- (j) base and emitter: boron and arsenic implanted through oxide.
- (k) final anneal: 900° , 20 min. steam plus 20 min. N₂ anneal.
- (1) metallization: 1.0 microns thick sintered at 450°.

To further improve the quality of CLSEG silicon, the following considerations are suggested.

- (1) Wrap the cavity around the end of the seed hole, or leave the end of the cavity open to reduce end effects.
- (2) Planarize the sacrificial layer to avoid a perturbation in the top layer.
- (3) Make seed holes and via holes as small as possible to keep the distance that the top layer is unsupported to a minimum.
- (4) Keep deposition pressures as low as possible, prefer barrel reactor.
- (5) Keep post-epi oxidation temperatures to a minimum.

With the above parameters, high quality CLSEG has been prepared and evaluated. This demonstrates that CLSEG is suitable for individual devices. However, to be applicable to practical circuit operation, CLSEG BJTs should also possess low values of parasitic collector resistance. The next chapter presents a new BJT structure which both shows the potential for solving the collector resistance problem, and also demonstrates the applicability of the CLSEG process to advanced devices.

CHAPTER 5

ADVANCED DEVICE STUDIES

With active device regions for BJTs and MOSFETs approaching fundamental limits in scaling, more attention is being directed to alternate methods for realizing greater functionality and speed on a semiconductor chip. The two principal avenues currently available to achieve this are the use of nano-fabrication to make quantum devices, or three-dimensional integration i.e., the stacking of layers of devices. In broad scope, it is towards 3-D integration that this thesis endeavors; mainly through the fabrication of stackable SOI layers. So far, CLSEG has been used to make local-SOI (SOI regions suitable only for individual devices) with high aspect ratios, yielding devices with very good characteristics. In this and the next chapter, two more key steps towards the realization of a viable 3-D technology are presented.

The performance of MOSFETs built in SOI layers has been well-researched, and bulk quality (or better) characteristics have been reported [35]. But vertical bipolar transistors in SOI (using SIMOX, buried nitride, or recrystallized polysilicon) have met with only limited success due to inferior crystal quality and high parasitic collector resistance. The results of local-SOI vertical BJTs reported in section 4.2.5, have demonstrated the high material quality achievable with CLSEG. In this chapter, a SOI vertical BJT is fabricated with a highly-doped sub-collector on the underside of the CLSEG which can dramatically reduce collector resistance for this structure. Lowered collector resistance is vitally important to high-gain BJTs in SOI. With such devices, analog operation and high current drive capability can be integrated into CLSEG SOI technologies.

5.1 Fabrication of Under-diffused Local-SOI BJTs

One of the claims that will be made of CLSEG in chapter 7 is its suitability as a tool for advanced device construction. In this chapter, a novel fabrication technique using CLSEG is presented which allows a highly-doped layer to be formed on the underside of an SOI film. Underside doping is essential in reducing parasitic collector resistance in high-gain SOI BJTs. Although underside doping can be accomplished using other local-SOI techniques, it is most readily accomplished with CLSEG. This demonstration will serve as one example of the many uses for CLSEG in new device designs.

The key fabrication steps in underside doping are illustrated in Figure 5.1. The process leading up to Figure 5.1a begins with CLSEG growth 1.2 microns high and 8 microns wide with a background phosphorus doping of $2 \times 10^{15} \, \mathrm{cm}^{-3}$. All top and bottom layers were completely removed and a 96 nm post-epi oxide was grown at 900° C. Then a mask-less boron implant (for the BJT base region) was performed with a dose of 2.0×10^{13} atoms/cm² at 60 keV energy. This base implant covers the entire top of the CLSEG slab, and was driven-in at 1000° C for 175 minutes in nitrogen to yield a junction depth of approximately 0.65 microns. All oxides were again stripped to reach the structure shown in Figure 5.1.a. Figure 5.1.b shows the result of an anisotropic plasma-enhanced silicon oxide deposition. The key feature to note here is that the gap beneath the CLSEG is not filled with plasma oxide. In Figure 5.1.c a mask and etch step has been used to expose a region on top of the CLSEG slab for the emitter, and to unplug the opening of the gap beneath the slab. All the exposed silicon is now doped N⁺ with a solid source phosphorus deposition at 875° C in nitrogen for 10 minutes. As seen in Figure 5.1.c, this forms an underside N^+ region which serves as a sub-collector for the vertical SOI BJT. Following the underside diffusion step, the thin phosphosilicate glass formed on the silicon surfaces is etched away, and a low-temperature conformal CVD oxide is deposited. Contact windows and metallization were completed as described in section 4.2.1.

A layout-equivalent control transistor for the low-resistance device is not available with the current mask design. However, a bipolar transistor is formed simultaneously in the homoepitaxy material which has identical base and emitter doping profiles; but which has a much larger emitter area, and no nearby collector contact. This quasi-control device is included primarily as a check on the current gain and ideality factor of the low-resistance CLSEG device. Figure 5.2 shows a perspective drawing (with various oxide layers



Figure 5.1 Key CLSEG BJT process steps for the underside diffusion process (a) CLSEG with top and bottom dielectric layers removed, (b) plasma deposited masking oxide, and (c) after N^+ deposition and drive.

removed) which illustrates the under-diffused device layout as well as the cross section. Note that the N⁺ collector region wraps around the side (end) of the CLSEG slab making it accessible for topside contact. Note that the current design focuses primarily on reducing r'_C but the collector to substrate capacitance C_{CS} will be quite large due to the large area of the underdiffused N⁺ region. This latter problem can be reduced dramatically by electrically isolating the CLSEG slab with the device from the substrate. This can be achieved by a silicon etch or local oxidation of the CLSEG silicon directly over the seed hole.

5.2 Results of Under-diffused BJT

In Table 5.1, averaged values for the N⁺ under-diffused transistor in CLSEG and its quasi-control device are presented. Output curves for the low-resistance device are shown in Figure 5.3 which verify transistor action of this novel transistor structure. These results are meant to demonstrate the feasibility of the new technique used to dope the underside of the CLSEG, and have not been optimized either for transistor performance or device layout. The current gain is fairly high (β_{max} =158), but the ideality factors are not as low as for the devices reported in Section 4.2.5 where the bottom layer was left intact. The large value of $\eta_{\rm EB}$ is similar to both the CLSEG and the control devices, and may be due to the N⁺ diffusion process itself, which does not include a high temperature anneal after the diffusion. The higher $\eta_{\rm CB}$ in the low-resistance device is probably due in part to oxidation-induced stress at the inside corner of the gap underneath the CLSEG slab during the N⁺ deposition. Such an oxidation is similar to the oxidation of trench isolation sidewalls , and can generate defects in the surrounding material [9].

The measured r'_{C} values for the lowered-resistance under-diffused devices in CLSEG 1.2 microns thick ranged from 1.9 to 3.0 k Ω with an average of 2.24 k Ω . This is a rather large value for this parameter, and calls into question the use of "low-resistance" as a descriptor. Yet this r'_{C} value is lower (slightly) than that for the high-gain devices from Section 4.2.5, despite the much lower collector background doping. This suggests that the under-diffused N⁺ has served to lower the collector resistance of this particular structure, hence the use of "low-resistance". Although this in itself is good evidence for the presence of the underside diffusion, the layouts of either the high-gain or the quasi-control devices are too different to make a direct comparison, so further verification was sought.



Figure 5.2 Perspective drawing of under-diffused vertical bipolar transistor in CLSEG local-SOI material.

Table 5.1. Measured parameters from under-diffused bipolar junction transistors in CLSEG material compared to a non-under-diffused device in homoepitaxy material.

PARAMETER	CLSEG N ⁺ under-diffused	HOMOEPITAXY no underside N ⁺
$eta_{ extsf{max}}$	171 ± 9.5	72.3 ± 4.9
ND	2×10 ¹⁵	2×10 ¹⁵
underside N ⁺	3×10 ¹⁸	-
$\eta_{ m EB}$	$1.40 \pm .02$	1.35±.03
BV _{ECO}	$1.11 \pm .33$	9.2±.1
$\mathbf{r'_C}$ (k Ω)	$2.24 \pm .5$	15.3 ± 11.1
No. of samples	5	6



Figure 5.3 Transistor output curves for under-diffused vertical bipolar transistor in CLSEG local-SOI material.

Spreading resistance profiles or groove-and-stain measurements were not possible for this structure because the unsupported CLSEG cantilevers broke off during the grind steps. Instead, a spreading resistance profile was taken of the N^+ region in the substrate directly beneath the broken-off CLSEG (the bottom of the gap in Figure 5.1.c). The surface here should have received the same doping treatment as the underside of the CLSEG film. This analysis showed an N^+ region in the substrate 0.4 microns deep with a sheet resistance near 250 Ω /square. Additional evidence for underside doping is that under-diffused devices built in CLSEG only 0.9 microns high exhibited ohmic emitter to collector short circuits, indicating a joining of the topside and underside N^+

5.3 PISCES Computer Simulation

To study collector resistance further, the two-dimensional device simulation program PISCES [106] was used. Since the low-resistance device structure of Figure 5.2 has no axis of symmetry, it is not directly adaptable to a 2-D simulation. Instead, to model collector resistance, the N⁺ collector regions in the underside, side, and top of the CLSEG slab were laid out flat, and modeled as a 2-D resistor. This 2-D resistor was treated as a slab of silicon doped at 2×10^{18} cm⁻³ and 0.3 microns thick, while the actual N⁺ region follows an error function with peak doping of 3.2×10^{18} cm⁻³ and a junction depth of 0.4 microns. These should give nearly the same sheet resistance for this calculation. Corner effects were ignored, and contacts were placed in the 2-D resistor beneath where the emitter and collector contacts would be in the actual device. The collector region is 46 microns long and 10.7 microns wide except at the collector contact area where the width is 14.7 microns. The computed collector resistance for this structure is 2.56 k Ω which agrees quite well with the measured value of 2.24 k Ω . Then, using the error function doping approximated by a Gaussian profile, collector resistance was computed for a device with the cross section shown at the near end of Figure 5.2, but with a stripe geometry. For this optimized structure, the emitter and collector contacts are parallel and extend the entire length of the device. For such a transistor 46 microns long, the collector resistance was calculated as 74 Ω . This is a very acceptable value, and indicates that the under-diffused N^+ process is capable of producing vertical bipolar transistors in thin films with very low parasitic collector resistance. It is also interesting to note that the PISCES-computed punchthrough voltage at 1.0 μ A was 1.27 volts for this accurate cross section, which agrees well with the actual value of 1.11 volts.

CHAPTER 6

DISCUSSION

In this chapter, the results of the last two chapters are summarized and hypotheses are made to explain them. The second half of this chapter compares CLSEG to other SOI technologies in the light of these results, and discusses how CLSEG could be used in various applications.

6.1 Discussion of Results

6.1.1 Growth results

Observations of selective silicon growth within cavities has revealed interesting and unexpected new phenomenon. In this subsection, the implications of these discoveries on our understanding of selective growth mechanics is discussed.

When CLSEG fills a cavity, its crystal orientation follows that of the <100> substrate, even as it grows laterally through the cavity. ELO growth has this property also, implying that the top layer does not affect the crystallographic properties of the CLSEG silicon. The growing CLSEG does not alter the shape of the top layer; specifically the top layer is not (generally) pushed up as the growth front encounters it. This implies that epitaxy proceeds by deposition, not "growth". When the growth reaches the top wall, the process gasses are prevented from initiating further growth in the vertical direction. Then, CLSEG will conform to the shape of a cavity to the extent allowed by faceting and/or defects. This is a desireable property especially when using CLSEG over non-planar structures.

CLSEG growth rates are virtually equal to ELO growth rates, and are independent of both cavity height and cavity width (depth), for the ranges investigated. This suggests that the transport and deposition mechanisms are the same as for ELO, regardless of the presence of the cavity. This is surprising because it has long been assumed [100, 88, 84, 40, 81, 65] that gaseous diffusion accounts for silicon transport to the SEG growth fronts. If diffusion is the transport mechanism, one would expect reduced deposition in thinner and deeper cavities. The reasoning behind this rationale is explained below.

The inadequacy of gaseous diffusion due to concentration gradients to account entirely for silicon transport into a CLSEG cavity arises because of the smallness of cavity dimensions compared to the mean free path (MFP) of the gas. In a very large cavity (smallest dimension >> MFP), diffusion takes place freely, as it does for whole wafer epitaxy, for example. On the other hand, in a very minute cavity (largest dimension << MFP) any molecules entering the cavity are unlikely to encounter other such molecules (since the cavity dimensions are smaller than the average spacing between molecules), so diffusion is no longer an accurate treatment of this case. In the extreme, if the cavity dimensions approach the size of the gas molecule, the pressure inside the cavity will approach zero. Thus, as cavity dimensions (especially at the opening) go below the MFP of the gas molecules, the "pressure" in the cavity is reduced, and diffusive transport into the cavity is curtailed. More precisely, classical diffusion models are no longer adequate to represent species transport.

Table 6.1 lists the MFP of the SiCl₂ molecule in the epi reactor, believed to carry silicon atoms from the gas phase to the surface, under the range of conditions used for the results in Chapter 4. The MFP (λ) of an ideal gas is given by $\lambda = \frac{1}{(1.414\pi d^2n)}$ where d is the molecules diameter, and n is the number density of molecules in the gas, computed as $n = \frac{AN}{V} = \frac{AP}{BT}$ where A is Avagadro's number, R is the gas constant, P is pressure, and T is absolute temperature [107]. These values assume ideal gas behavior, a molecular diameter of 5 Angstroms, and do not account for partial pressures of the various gasses. Since cavity heights in the range [0.25, 1.2] microns are of the same order as the gas MFP, one would expect to see a noticeable dependence of CLSEG growth rates on cavity width and cavity height if diffusion accounts for all the silicon transport. Since no such dependence on cavity dimensions is observed, it is possible that some other transport mechanism is significant in CLSEG growth. As discussed in Chapter 2, many authors have noted the high surface mobility of silicon adatoms, and have cited surface diffusion distances up to 100 microns. This is based on the observation that, even in not-perfectly selective growth, a denuded zone free of polysilicon nucleates on the mask layer Table 6.1 Mean free path of $SiCl_2$ at various deposition conditions for selective epitaxial growth.

Temperature (C)	50 Torr	150 Torr
950°	$2.28~\mu{ m m}$	0.76 μm
1000°	$2.37~\mu{ m m}$	0.79 μm

exists surrounding the ELO to approximately these distances. It seems reasonable to hypothesize that silicon atoms adsorbed on the SEG mask surface can wander about for long distances, even into cavities too small for a gas molecule to enter. These mobile adatoms are then free to deposit within CLSEG cavities just as for ELO, thus accounting for the equality of growth rates and the independence of cavity dimensions. These conclusions are drawn from data which does not adequately rule out other possibilities, and should be considered with some caution. Clearly, more rigorous study in this area is needed to make a definitive case.

No facets are seen in lateral CLSEG from $\{001\}$ -oriented seed holes, which is in agreement with vertically-growing SEG in such seed holes. Thus, much of the understanding of SEG faceting can be applied to CLSEG. Interestingly, ELO faceting does not seem to follow the same rules as for SEG and CLSEG. This in in qualitative agreement with a faceting model [108] which states that the presence of a dielectric sidewall in $\{001\}$ seed holes affects the faceting by influencing the relative growth rates of different crystal planes. The end effect is probably caused by the same faceting mechanism that produces corner facets in $\{100\}$ SEG and makes octogonal ELO outlines. This phenomenon is a serious disadvantage to all three selective epitaxy techniques. However, CLSEG provides many designs for the placement of the cavity walls that are not possible with SEG or ELO. Although it is not clear how at this time, there may be a way to avoid the end effect/corner facet in CLSEG by appropriate cavity design.

6.1.2 Electrical results

CLSEG material quality, as evidenced by diode ideality factors (η), is very sensitive to process variations both in cavity construction and post-epi processing. The choice of silicon nitride over thermal polyoxide from a deposited α -Si sacrificial layer was found to yield the best results from the structures compared in this work. This arises from two main considerations. First, thermal oxide is far less likely to generate defects in the near-wall CLSEG (or SEG) than is nitride [69,72]. Second, when the inside surface of this oxide top layer is not microscopically parallel to the <100> plane (as with a polysilicon sacrificial layer), the likelyhood of generating defects increases, as discussed in section 2.3.3. Silicon nitride provides needed stiffness to the top layer which silicon oxide alone does not provide for the thicknesses investigated. This stiffness prevents sagging or deflection of the top layer, keeping it from being non-parallel to the $\langle 100 \rangle$ plane, and creating conditions favorable for defect formation during CLSEG growth. The combination of nitride and oxide as a top layer seems to provide the best results, as can be seen from Table 4.4.

Thermal and oxidation-induced stresses have strong influences on the final CLSEG material quality. In section 4.2.3, it was reported that in unannealed CLSEG, η values dropped dramatically after removal of the bottom oxide. Since no high temperatures were involved, and since defects are unlikely to disappear, one infers that residual thermal stress has a negative impact on η , which is released upon removal of the bottom oxide. In the above case the top layers were removed as well, but the bottom oxide seems a more likely site for stored thermal stress; since the top layers are free to deform plastically, while the bottom oxide is sandwiched between the substrate and CLSEG silicon, and must experience a shear stress upon cooling from the epitaxy temperature. Therefore if the CLSEG is never annealed at high temperatures, the bottom oxide should be removed for best film quality.

On the other hand, Table 4.4 shows that bottom oxide removal causes larger η values if moderate temperature (900 to 1000°) post-epi anneals and/or oxidations are performed. This effect is likely caused by oxidation-induced stress, especially at the inside corners of the gap under the CLSEG, as would be expected from studies of trench isolation oxidation. Another factor can be the hydrostatic forces generated by the growth of the oxide layer in the confined space beneath the CLSEG. This oxide can act to pry up the CLSEG canitlever, much as silicon nitride is pried up during a LOCOS oxidation. Studies of trench oxidation show that thermal oxides grown at higher temperatures (T $\geq 1000^{\circ}$ C) undergo viscous flow which can relieve stress due to oxidation. This model can explain the improvement in η values observed for the least square fit model in the temperature range of 900 to 1000° C. But the data at 1200° indicates that some other mechanism is at work in this regime. A possible cause for this may be that any defects already present in the CLSEG, especially at the top layer perturbation, will become more mobile at higher temperatures. These defects can grow or they can glide along slip planes until they extend into the lateral SOI portions of the CLSEG. In this case, an increase in defect density would cause the higher η values at the highest post-epi anneal temperatures. Further studies of this effect would benefit CLSEG technology, and could probably be applied to SEG and ELO as well.

For the SOI BJTs fabricated in CLSEG, a reduction in the slope of the collector current was observed at a collector-emitter voltage of approximately 2.5 volts. A PISCES computer simulation showed that this change in output

characteristics occurs when the base-collector depletion region reaches the underside oxide layer of the CLSEG SOI slab. This reduction in slope corresponds to an increase in the Early voltage for the device; implying that the effect of basewidth modulation is reduced in some way. To explain this, consider that, once the CLSEG collector region beneath the base is fully depleted, further increases in electric field will cause the base-collector depletion region to extend laterally down the CLSEG slab. Now, the change in the depletion layer width in the base is changing only in the lateral direction, where very little bipolar current is flowing. Since much of the current is still crossing the base where the presence of the emitter makes the basewidth very small, and since the base depletion layer is no longer changing much in this area, we would expect that basewidth modulation would be lessened. This principle can be used to artificially increase the output resistance of a SOI BJT for analog drive applications. However, by making the CLSEG slab thinner to increase Early voltage, collector resistance, and hence output current, will suffer. A second PISCES simulation (not shown) did indeed show that increasing the CLSEG slab height from 1.07 to 1.5 microns thickness resulted in an 11% increase in output current but with a corresponding 40% reduction in Early voltage. A design including a low resistance collector region, as described in chapter 5 could potentially be used to combine the benefits of high output resistance with high currents.

6.1.3 Advanced device results

The fabrication of the under-diffused BJT for lowering collector resistance was sufficient to demonstrate the concept. But to truly realize the high-gain, low-resistance device suggested in Chapter 5, several design and process improvements are needed. A stripe geometry layout was shown, by PISCES computer simulation, to greatly lower the parasitic collector resistance. This was not feasible with the current design rules (see section 4.2.1), but with more aggressive contact and metallization lithography, should be readily achievalbe. To reduce parasitic capacitances and avoid defect regions in the CLSEG, the base region should be masked, instead of being blanket-implanted as in the fabricated device. The emitter for the fabricated structure was diffused along with the collector for process simplicity. But for best control of the critical emitter doping profile, this region should be formed separately from the collector by using an ion implant. Better performance of the under-diffused device can be being non-parallel to the <100> plane, and creating conditions favorable for defect formation during CLSEG growth. The combination of nitride and oxide as a top layer seems to provide the best results, as can be seen from Table 4.4.

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On the other hand, Table 4.4 shows that bottom oxide removal causes larger η values if moderate temperature (900 to 1000°) post-epi anneals and/or oxidations are performed. This effect is likely caused by oxidation-induced stress, especially at the inside corners of the gap under the CLSEG, as would be expected from studies of trench isolation oxidation. Another factor can be the hydrostatic forces generated by the growth of the oxide layer in the confined space beneath the CLSEG. This oxide can act to pry up the CLSEG canitlever, much as silicon nitride is pried up during a LOCOS oxidation. Studies of trench oxidation show that thermal oxides grown at higher temperatures (T $\geq 1000^{\circ}$ C) undergo viscous flow which can relieve stress due to oxidation. This model can explain the improvement in η values observed for the least square fit model in the temperature range of 900 to 1000° C. But the data at 1200° indicates that some other mechanism is at work in this regime. A possible cause for this may be that any defects already present in the CLSEG, especially at the top layer perturbation, will become more mobile at higher temperatures. These defects can grow or they can glide along slip planes until they extend into the lateral SOI portions of the CLSEG. In this case, an increase in defect density would cause the higher η values at the highest post-epi anneal temperatures. Further studies of this effect would benefit CLSEG technology, and could probably be applied to SEG and ELO as well.

For the SOI BJTs fabricated in CLSEG, a reduction in the slope of the collector current was observed at a collector-emitter voltage of approximately 2.5 volts. A PISCES computer simulation showed that this change in output

characteristics occurs when the base-collector depletion region reaches the underside oxide layer of the CLSEG SOI slab. This reduction in slope corresponds to an increase in the Early voltage for the device; implying that the effect of basewidth modulation is reduced in some way. To explain this, consider that, once the CLSEG collector region beneath the base is fully depleted, further increases in electric field will cause the base-collector depletion region to extend laterally down the CLSEG slab. Now, the change in the depletion layer width in the base is changing only in the lateral direction, where very little bipolar current is flowing. Since much of the current is still crossing the base where the presence of the emitter makes the basewidth very small, and since the base depletion layer is no longer changing much in this area, we would expect that basewidth modulation would be lessened. This principle can be used to artificially increase the output resistance of a SOI BJT for analog drive applications. However, by making the CLSEG slab thinner to increase Early voltage, collector resistance, and hence output current, will suffer. A second PISCES simulation (not shown) did indeed show that increasing the CLSEG slab height from 1.07 to 1.5 microns thickness resulted in an 11% increase in output current but with a corresponding 40% reduction in Early voltage. A design including a low resistance collector region, as described in chapter 5 could potentially be used to combine the benefits of high output resistance with high currents.

6.1.3 Advanced device results

The fabrication of the under-diffused BJT for lowering collector resistance was sufficient to demonstrate the concept. But to truly realize the high-gain, low-resistance device suggested in Chapter 5, several design and process improvements are needed. A stripe geometry layout was shown, by PISCES computer simulation, to greatly lower the parasitic collector resistance. This was not feasible with the current design rules (see section 4.2.1), but with more aggressive contact and metallization lithography, should be readily achievalbe. To reduce parasitic capacitances and avoid defect regions in the CLSEG, the base region should be masked, instead of being blanket-implanted as in the fabricated device. The emitter for the fabricated structure was diffused along with the collector for process simplicity. But for best control of the critical emitter doping profile, this region should be formed separately from the collector by using an ion implant. Better performance of the under-diffused device can be attained if the CLSEG slab is made thicker. This allows an N^- intrinsic collector regions next to the base junction which will increase the punchthrough voltage and reduce the basewidth modulation.

The under-diffused region itself in the fabricated device is nearly as thin as can be produced with the phosphorus solid diffusion source used for this work. Part of the low collector resistance computed for the stripe geometry was due to the length of the device ($r'_C = 74 \Omega$ for 46 microns long). This value increases quickly for very small devices, so that a more highly doped under-diffused region will be needed. This can be done by further increasing the CLSEG slab thickness to accomodate a deeper under-diffused region; or by using an arsenic solid or gaseous diffusion source. Arsenic-doped spin-on glasses might be used for this purpose. Finally, for a very high performance device, the under-diffused collector process could be combined with concepts from advanced BJT structures (such as SST or SICOS) which optimize the base and emitter portions of the device.

To produce a reliable circuit using the under-diffused technique, the gap beneath the CLSEG would need to be filled with a non-conductive material. It is observed that the CVD low-temperature oxide deposited immediately after the N^+ diffusion step filled this gap to some extent. An optimized CVD oxide step could potentially fill this gap without voids. Alternatives are to close off the gap with a thermal oxide, or to use trench fill techniques currently used in trench isolation. Once, filled, the CLSEG should be mechanically stable and ready for 3D integration if desired.

6.2 Comparison to Current Technology

CLSEG, in its simplest context, is an extension of SEG, but as a technology in its own right can be evaluated from three fields of inquiry. As shown in Chapters 3,4, and 5, CLSEG can be used as an isolation technology, as a means of studying crystal growth and quality, and as a tool for the fabrication of new device structures. In each of the next three subsections, the utility of CLSEG for the application is discussed as a basis of comparison with other related technologies.

6.2.1 CLSEG as an isolation technology

In the previous chapters CLSEG has been used as a local-SOI technique where a separate SOI region is made for each individual device or set of devices. One of the advantages of this technique is that electrical connection to the substrate can be made while still benefitting from reduced parasitic capacitances. Alternatively, in local-SOI, this substrate connection can be eliminated by etching the silicon over the seed hole, or by consuming it in a local oxidation step. In this subsection, a method is presented for forming whole-wafer SOI using CLSEG. In whole-wafer SOI, the silicon slab extends across the entire wafer, and in general does not have a connection to the substrate. In addition to the SOI advantages listed in section 2.2.1, whole-wafer SOI has the further advantage of being transparent to circuit and layout designers. With whole-wafer SOI, isolation of a device is as simple as etching a hole or moat all around the device, whose dimensions are in no way limited by the SOI technology (as it is in local-SOI)

The local-SOI method shown in Figure 3.1 can be adapted to whole-wafer SOI using the two-step epitaxy process [50, 42] shown in Figure 6.1. CLSEG is first grown in back to back cavities, and merged with CLSEG growing from a facing cavity, as depicted in Figure 6.1(a). The dashed vertical line represents the plane along which the CLSEG growth fronts coalesce. Figure 4.10 is an SEM photograph of such a merged structure, and shows the ELO overgrowth visible in Figure 4.10 and indicated in Figure 6.1.

After the first CLSEG merge step, the silicon and the top layer material above the seed holes are etched down to the substrate. Silicon nitride (Si_3N_4) sidewall spacers are then formed on the exposed sides of the remaining CLSEG silicon, as shown in Figure 6.1(b). An oxidation step is now used to oxidize the substrate and the via hole overgrowth along the CLSEG merge plane; after which the nitride sidewalls are removed to form the structure of Figure 6.1(c) Now a second selective epitaxy step initiates growth from the exposed CLSEG sidewalls, which proceeds until it merges with the growth from a facing sidewall, as shown in Figure 6.1(d). The overgrowth protrusions above each merge plane can be readily removed by chemical-mechanical polishing or conventional plasma etch back. The result is continuous SOI film over an unlimited large area, or whole-wafer SOI.

This concept can be repeated indefinitely in principle, to produce 3D stacked layers of circuits. As research into very low temperature $(T_{epi} < 800^{\circ}C)$



Figure 6.1 Process for whole-wafer SOI using CLSEG

96

epi continues, it may soon be possible to grow selective epitaxy with almost no impact on existing dopant profiles. Since CLSEG allows a substrate (or previous SOI layer) connection even in whole-wafer SOI (by not etching over a given seed hole in Figure 6.1 (b)), this makes CLSEG a prime candidate for 3D integration of integrated circuits. The very low processing temperatures that are potentially achievable with CLSEG is a significant advantage over certain other SOI technologies. Buried insulator technologies and polysilicon recrystallization both require high temperatures and may involve large thermal gradients in the silicon wafer. These factors tend to preclude their use from 3D integration. The primary advantage of CLSEG as an isolation technology is the geometric freedom and dimensional control, coupled with design flexibility.

6.2.2 CLSEG as a device construction tool

CLSEG seems to encourage the creative process in device designers because of the variety of shapes and configurations it can provide. With appropriate microfabrication techniques applied to the CLSEG sacrificial layer, cavities of varying thicknesses, shapes, and widths are possible. These cavities can be stacked, merged, overlapped; or several layers can be grown at once. Access to the underside of CLSEG slabs opens us an entirely new range of devices.

Some of the devices that have been conceived using CLSEG are the following: novel DRAM concepts; buried drain DMOS structures; two-sided CCDs; buried channel MOSFETs; piezoresistive sensors; micromachined cantilevers; low resistance base and emitter contact for advanced BJTs; a doubly self-aligned shared-gate CMOS structure; and others. Most of these applications can be realized in one or another of the SOI techniques mentioned in Section 2.2.2. The advantage that CLSEG offers is the ease and flexibility of forming the silicon slab. Virtually any thickness of silicon can be formed; extremely thin layers by using oxidation to consume the CLSEG silicon, or thicker layers by growing homoepitaxy on top of the CLSEG slab. Control of thickness uniformity of CLSEG films can be very good since it follows the shape of the sacrificial layer, provided the top layer does not sag. Sagging might be avoided by more sophisticated designs of the top layer; certainly thicker materials would be helpful, and multi-layered structures might be made with negligible sag. The cavity can be made conformal to underlying structure, or by using planarization techniques, the cavity can be formed with a flat top surface. The substrate connection at the seed hole in CLSEG can be used as an electrical contact, as a mechanical support, or as a piezoresistive material. With CLSEG there is a wide choice of thicknesses possible for the bottom oxide layer, unlike buried insulator or OPS. Very thin bottom oxides can be used as a bottom side MOS gate insulator for 3D integration. CLSEG cavities can be stacked, with a common seed hole so that multiple layers can be formed in a single epi run. CLSEG can also be grown in cavities of different heights across a single wafer. For example, a 2 micron cavity for BJTs could be grown simultaneously with a 0.2 micron cavity for MOSFETs. These applications give a flavor of the wide range of uses for CLSEG. No other SOI technique offers so much variety and flexibility of design with such straightforward processing.

6.2.3 CLSEG for growth studies

The utility of CLSEG for growth studies has already been shown by the new insight into silicon transport in SEG discussed above. A number of experiments are possible with CLSEG and ELO which can further elucidate the behavior of silicon-containing species in an epitaxy reactor. Another field of study is into the defects formed at SEG sidewalls, which are (arguably) similar to CLSEG top and bottom walls. The sidewall gate-controlled diode of Figure 2.6 is very difficult to process, and may unduly influence the very properties it intended to examine. However, with CLSEG, the same goals can be easily accomplished by forming a gate-controlled diodes on top of a CLSEG slab which is identical in layout to a substrate gate-controlled diode. It was observed that, in many ways, the principles of SEG apply to CLSEG, so that it seems likely that data extracted from CLSEG gate-controlled diodes could be used to enhance or understanding of SEG sidewalls. Other possibilities for basic studies using CLSEG include: (1) effects of stress on device performance; (2) lateral diffusion characterization (by diffusing up from the CLSEG underside); (3) oxidation of shaped surface with perpendicular sides (not possible with trench etching); (4) and nucleation or growth of defects in low temperature and pressure silicon epitaxy.

CHAPTER 7

CONCLUSION

7.1 Significance of Results

CLSEG is a new epitaxy technique with many significant advantages when compared to current state-of-the-art in epitaxy, device isolation, and advance device construction. CLSEG can be used to form local-SOI or whole-wafer SOI silicon suitable for the fabrication of semiconductor devices. The aspect ratio of the as-grown single-crystal slabs can be at least 14:1 with a 10% or less local variation in thickness. No facets are observed in CLSEG growth fronts within the cavity (except for the end effects), which allows growth fronts to be merged, doubling the effective aspect ratio. The large variation in growth rates across a 5 inch diameter wafer is to be expected from epitaxy reactors optimized for homoepitaxy. However, CLSEG film heights are independent of growth rate, making this critical paramters more easily controlled than with other epitaxy techniques. Virtually no visible defects are found in the lateral SOI portions of CLSEG films; however, directly above the seed hole edge, a shallow defect region is formed. This defect region is presumably due to the perturbation in the top layer caused by the conformality of the α -Si sacrificial layer used, and may be avoided with appropriate planarization. The only serious drawback to CLSEG is the end effect at either end of the cavity. This is probably caused by the natural faceting which also detracts from SEG and ELO technologies. Yet, with CLSEG, there is hope to eliminate or at least minimize this faceting with clever cavity design.

Diodes, metal-gate MOSFETs, and vertical bipolar transistors have been formed in the lateral SOI regions of CLSEG films. Values of the parameters η , $\mu_{\rm p}$, S, and $\beta_{\rm max}$ are found to be equal in CLSEG and in homoepitaxy island silicon. Because of differences in background doping concentrations, these values could not be directly compared to substrate values. However, previous work in SEG [102] has demonstrated that homoepitaxy island material can be grown with values of η and β_{\max} which are equal to substrate values. By induction, it can be stated that device parameters in CLSEG can be made equal to devicequality substrate material. This implies that CLSEG crystal quality is on a par with manufacturer-prepared silicon device wafers. A new process using CLSEG has been introduced for doping the underside of a local-SOI film. This is the first report of such a method. This under-diffusion technique is very useful in reducing the collector resistance of vertical bipolar devices in thin silicon films. With the combination of high-quality material, and such fabrication techniques as under-diffusion, potentially very high performance devices and circuits can be realized using the CLSEG technology.

7.2 Further Investigation Possibilities

The CLSEG technology has many avenues open for further investigation. A breif list of further possibilities is: (1) achieving high aspect ratios; (2) study of radiation hardness; (3) study of latch-up resistance in local-SOI; (4) fabricating ultra-thin SOI layers for high-performance MOSFETs or quantum devices; (5) study of stress effects in silicon; (6) study of growth mechanisms in selective epitaxy; (7) study of CLSEG defects and sidewall phenomenon; (8) achieving whole-wafer SOI; (9) 3D integration, or stacking of devices; (10) study of end effects and their minimization; (11) improvement in top layer rigidity for better uniformity; (12) elimination of defects by planarizing the sacrificial layer; (13) study of oxidation-induced effects in silicon; (14) fabrication of highperformance (speed, gain, power) circuits in SOI using the under-diffused process; and (15) thin film silicon membranes for piezoresistive sensor elements.

The CLSEG process that has been described to this point uses three masking steps to benefit from all the advantages listed. Yet, by using three masks (or four for whole-wafer SOI), CLSEG becomes less attractive because of the added cost, time, and lower yield due to these lithography steps. To address this concern, a CLSEG technique was invented which uses only a single mask step, or two mask steps for whole-wafer SOI. This process is illustrated in Figure 7.1 and described below. Beginning with a P⁺ substrate, or a substrate with a P⁺ buried layer, an N⁻ epitaxy layer is grown on top. The thickness of this epilayer will approximately determine the CLSEG thickness. A thick oxide layer is thermally grown on the top surface, and optionally coated with silicon nitride (not shown) for added support. The mask step is then used to etch a hole through the thermal oxide (and nitride, if any) as shown in Figure 7.1(a).



Figure 7.1 One mask-step CLSEG process.

This forms the equivalent of the via hole in the three mask-step version. Now, using an preferential silicon etch, the N^- epilayer is etched down to the P^+ substrate. This etch is formulated and electrically biased to etch N-type silicon selectively over P-type silicon. By extending this etch, the top oxide layer is undercut by removing the N- epilayer beneath it. This is shown in Figure 7.1(b). Next, the structure is oxidized, which forms different oxide thicknesses over the exposed P^+ and N^- regions. The objective here is to form a thicker oxide on the P^+ substrate than on the N^- epilayer, while both are thinner than the top layer oxide, as illustrated in Figure 7.1(c). Note that N and P are interchangeable, and their choice will depend on the properties of the silicon etch and the relative oxidation rates of the layers for the conditions chosen. In Figure 7.1 (d), a breif (timed) oxide etch is used to remove all the oxide covering the N^- epilayer, while leaving oxide on the P^+ substrate and leaving the top layer intact. This step forms the CLSEG cavity, where the exposed N- epilayer acts as the seed hole in the three mask-step process. Now, during a selective growth step, this cavity will fill with silicon, forming the local-SOI slab.

The tradeoffs of three mask versus one mask CLSEG are that in this simpler process, the cavity is formed on all sides of the via hole. As a consequence, the CLSEG slab will grow towards the via hole from all four sides (assuming a rectangular hole). While this may be inconvenient for local-SOI, it is an advantage for whole-wafer SOI since the facing cavities are formed at the same time. Other possible disadvantages of the one mask-step process are that the silicon seed material may not be $\{100\}$ oriented due to the silicon etch. It is not clear whether this would adversely affect the crystal quality, since very little work has been done on SEG on non- $\{100\}$ material. The silicon etch itself is a non-standard process step, and obviates the three mask-step advantage of being performed with easily obtained equipment and materials. Other than these concerns, the one mask-step process bring CLSEG on a par with thinned ELO and polysilicon recrystallization in this important consideration.

7.3 Summary of Thesis

In this work, considerations needed to evaluate a new epitaxy technique were reviewed. CLSEG was compared to existing technologies used for scaling of device sizes, for device isolation, and for forming advanced epitaxy layers by SEG and ELO. This background provided a basis for the motivations which gave rise to the CLSEG process.

The methods for using CLSEG for either local-SOI or whole-wafer SOI have been described in detail using either the more-flexible three mask step technique, or the simpler one-mask step technique. The various issues related to material choices and epitaxy growth were covered in detail. An extensive characterization of the growth properties of CLSEG silicon was disclosed, covering all major areas of interest. A full report has been made of the method by which various semiconductor devices were fabricated in CLSEG material. These devices were tested to extract parameters which were used to assess the material quality of the grown material. The results of these studies showed very interesting behavior which might not have been expected prior to this undertaking. The final result was that CLSEG material quality can possibly be made equal to substrate silicon quality, ensuring that the full range of semiconductor devices can be formed in CLSEG silicon. To demonstrate this ability, a new device structure was created and fabricated using CLSEG. With the new technique of under-diffusion, high-performance bipolar junction transistors can at last be formed in thin SOI films.

Several new insights into the understanding of selective epitaxial growth have been revealed with the advent of the CLSEG technique. It has further revealed valuable insights into the effect of processing on thin silicon films, which will be useful as the semiconductor industry advances towards 3D integration. CLSEG has been compared to other SOI techniques, and been found to be superior in many ways to the current-state-of-the-art in device isolation. In the course of bringing these advantages, CLSEG has opened up new opportunities for valuable studies of the fascinating field of selective epitaxial growth.

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104

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APPENDIX

APPENDIX **CLSEG Process Flow**

PROCESS FLOW CLSEG MATERIAL CHARACTERIZATION

LOT XP28

· 11.4 · 11.2 · 11.4

REVISION DATE: 25 Sept 89 For YB3D/97M Test Chip

CLSEG PROCESS

LOT #_____ # wafers:_____Starting Date_

Starting Material: $N + \langle 100 \rangle$ with $\langle 100 \rangle$ flat.

1. N- Epitaxy - whole wafer. 5 μ 3-5 Ohm-cm. Hi temp. _____- resistivity=_____ Thickness =____

2. Initial oxide > = 2500 A 105' 900 C Wet=2280 A. For A1,7 950 DRYO2, 2.89 A/min (furnace ramp rates less than +/- 8 deg/min) Thickness=_____

SEED mask. Positive photoresist. Plasma etch for vertical sidewalls. 3. (Scribe wafer numbers in resist) THICKNESS=_ Measure (critical dimensions)CDs. Monitors need this for later alignment!

4. Seed hole oxidation. try 900 C DRYO2 for 20 minutes, about 200 A. THICKNESS=___

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5. AMORPHOUS silicon deposition (T=580 C). Smoothness of top layer is essential for low stacking fault density. Thickness = 10,000 for BJTs. Silicon thickness must exceed thickness of oxidation in step 9.

6. HMDS all wafers before resist coating.

7. BLCK mask, resist thickness = 2.2 microns.
(2-part etch, 135 C bake not needed with Tegal 801 Tegal 801 @ 90 watts. ER's: ox=500, poly=1500-2000, photoresist=1000 A/sec. Takes about 4 minutes for 10,000A.
Strip resist wet.

8. Strip backside poly in plasma etcher Tegal 701.

10. Deposit top layer nitride. 1100 to 1500 A. Use LPCVD stoichiometric nitride with low stress if possible. Thickness=_____

11. Strip backside nitride on 701. Wet strip backside oxide.

12. HMDS before resist application. very necessary!!!

13. VIAL mask. Bake 135 C for 30 minutes. Plasma etch nitride 901 or 701. Plasma etch oxide on LAM, g'head and overetch. Careful, tends to be non-uniform. Watch for dewet. Strip resist wet, do BHF dip quickly.

14. L O N G Poly etch Several choices...
R-52 (ethlyene diamine solution) USE NEW SOLUTION or get silicon precipitates. 86 C etches 11 um in 12 minutes.
OR - Nitric + Ammonium Floride 51:50ml NH4F controls ER, expect 2um/14 min. May let resist stick around.
* Si E.R. =.95u/1.1min. oxide E.R. =13A/13min.

WARNING - Hand Dry all wafers! DON'T use spin driers (top layers can be fragile at this point) "A" clean first - to get rid of slag and particles

15. Seed hole Oxide etch. See step 4. Be very careful. about 45 sec for 330 A in 10:1. Use thicker oxides in Nanometrics for endpoint detection.

"A" clean Many rinses, hand dry!!! ! May not be necessary to hand dry ADD MONITORS $P - \langle 100 \rangle$ for resistivity calculation and as etch dummies.

16. CLSEG	N- 8.0 μm la	teral growth in	clude P-,		
Do a checkou	t run with 2 v	wafers. expect E	LO growtl	n rate	
about 0.17 un	n/min for Pu	rdue reactor. ne	ear non-se	ective.	
Use N+<10)0> for G.	R., use P-<1	00> for	resistivity .	Parameter
PURDUE	DELCO				
Temp	950	1000			
Pressure	150 Torr	50 Torr			
H2 flow	60 LPM	80 LPM			
DCS flow	.22 LPM	.40 LPM			
HCl flow	1.26 LPM	2.05 LPM	н С.		
N-Dopant	N/A	1.5 LPM			

DO use HCl etch if at Purdue Continue with P- <100> wafer as substrate monitors. Thickness=______ Lateral=_____

17A. Nitride top layer strip.
Strip nitride in hot phosphoric acid. about 60 min.
17B. Oxide strip -- several choices
Definitely remove top layer oxide (from oxidized amorphous)
Probably remove field oxide so substrate devices see same oxide as CLSEG.
Maybe remove bottom oxide (1:1 BHF 10 min) for underside access.

18. Healing oxide 750 A. Try 26' Wet @ 900 THICKNESS=_____ Ramp up 5/min, down 7/min

HMDS all wafers.....

19. PBSE mask. KEEP RESIST for Implant include P-EXPOSE for 47 seconds. * Descum 3.5 minutes to remove residue. LINEWIDTH, ELO(T,C,B)=_____SUB=____

20. Boron Ion Implant thru healing oxideP-For MOSFETs P+ 5.0E15 @ 100 keV (or 55 kev for shallower junctions)For Bipolars P- 1.5E13 @ 55 keVStrip resist wet.

*. Hexamethyldisilazane (HMDS) all wafers

21. NEMT mask. ALIGNMENT IS CRITICAL P-Account for undercut of resist during oxide etch and heat shrink of resist during implant when choosing exposure doses. Use P- monitors for timing of etch

* Descum resist plasma, wet etch pattern. Etch time=P-

? Consider dry etch! Etch Back oxide to 360 A. HAND RINSE BEFORE QWUICK DUMP. KEEP RESIST! Be very careful with etch-back.... ETCH TIME=_____OXIDE THICKNESS=_____ LINEWIDTH ELO(T,C,B)=_____SUB=____

22. Arsenic Emitter II thru thin oxide 3.5E15 @ 100 keV. P-Strip resist plasma, then wet to remove residue....

23. HMDS before resist application, if doing plamsa etch.

24. CNTX mask. Use very thick resist to cover steps. P-Begin with plasma etch, then finish Wet etch. Be careful, since oxide thicknesses will be different ! Also, watchout for different window sizes, can be hazardous LINEWIDTH ELO(T,C,B)=_____SUB=____

25. Strip resist wet. "A" clean, 2-5 min "Q" etch to dewet.

26. METAL deposition. Use 10 kA w/heat to cover CLSEG steps.

27. METL mask. 200 bake for 30 ' first unless very fresh.
Expect significant undercut with wet etch. May choose liftoff process.
Need EBR for Tegal, use prog. 2,2 at 3.5 krpm or 3,2 resist.
Condition resist to plasma etch either (1) Prist, 200 C bake for
30 minutes or (2) Deep UV program H to 200 C.

Do hard overetch on FABII LAM. Tegal 1512e, 40 second overetch on 10k prog. NO passivation. Rinse wafers after etch to remove chlorine. Dry strip resist. USE A LONG EXPOSURE TIME..

28. Microally. Rinse first. 450 C for 45' in H2/N2.

END OF PROCESS Date finished_____

VITA