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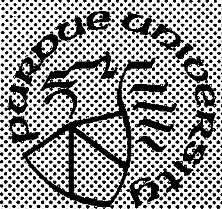

Evaluation of Silicon Selective Epitaxial Growth Defects using the Sidewall Gate Controlled Diode

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TR-EE 89-58
October, 1989

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This is dedicated to my wife, Alynn,
sitting beside our babbling brook,
waiting for her husband to come home.

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ABSTRACT

Klaasen,William A. Ph.D., Purdue University, December 1989. Evaluation of Silicon Selective Epitaxial Growth Defects Using the Sidewall Gate Controlled Diode. Major Professor: Gerold W. Neudeck.

Selective Epitaxial Growth (SEG) of silicon has shown great potential for advanced integrated circuit technologies. Before SEG can be fully utilized, sidewall defects must be reduced or at least controlled. The phenomena responsible for these defects were not understood, therefore more quantification of the sidewall defects is necessary. Walled diodes have been used to measure the sidewall leakage currents, but are susceptible to problems which make them poor devices for comparing different sidewall interfaces. A new device structure, the Sidewall Gate Controlled Diode (SGCD), is presented for the quantification of the defects near the SEG sidewall. The SGCD is shown to have advantages over the use of walled diodes despite the complex fabrication process required to build it. The development of the fabrication process for this device and the verification of its useful operation are presented. After the operation of the SGCD was verified, the device was used to evaluate the effects of various SEG deposition parameters on the sidewall defect density. This study determined that lower temperature, slower growth rate depositions followed with an in-situ hydrogen anneal generally reduced the defect density. Inconsistencies in the results also indicated that the profile of the sidewall may also influence the defect density at the SEG/oxide sidewall.

CHAPTER 1 - INTRODUCTION

1.1 Background

Silicon Selective Epitaxial Growth (SEG) and related technologies have demonstrated potential for use in producing cheaper, smaller, faster, more efficient integrated circuits. Before the SEG technologies can be used for many of the proposed applications, material quality issues must be addressed. The investigation of sidewall interface defects created with SEG is part of a research program for developing advanced bipolar applications of SEG.

This thesis addresses the quantification of the sidewall interface defect densities. After developing a measurement technique and structure for quantifying these defects, procedures designed to minimize the defect densities in and around the SEG material were studied. These procedures are applicable to the devices currently under development which include the Epitaxial Lateral Overgrowth Bipolar Junction Transistor (ELOBJT) [1] and the Quasi-Dielectrically Isolated Bipolar Junction Transistor (QDIBJT) [2].

1.2 Overview

A literature review is presented in the second chapter to provide background information on selective epitaxy technologies, selective epitaxial material quality, and applications of selective epitaxy technologies. The current knowledge of the sidewall defects is presented as well.

In the third chapter, the Sidewall Gate Controlled Diode (SGCD) is presented as a new device structure designed for investigating the SEG/oxide sidewall interface. The theory and a demonstration of the operation of a planar gate controlled diode is presented. The theory of operation of the SGCD is discussed, and the description of the test mask set is included.

The development of the fabrication process used to create the unique SGCD is discussed in Chapter 4. The creation of the SEG seed window with the oxidized polysilicon sidewalls is discussed in detail. Other fabrication techniques, which are necessary for the realization of the SGCD but not related to the SEG material quality, are also presented. Many of these techniques will be useful for constructing the ELOBJT and other devices such as a vertical gate MOSFET.

The electrical test data obtained from the SGCD on SEG material is presented in the fifth chapter. Data which verifies the intended operation of the SGCD is presented. After the successful operation of the SGCD has been verified, the evaluations of different sidewall interfaces produced with different process techniques are presented. These results are discussed, and conclusions are presented on the source of the sidewall defects.

Finally, a summary and recommendations of future work are presented in Chapter 6.

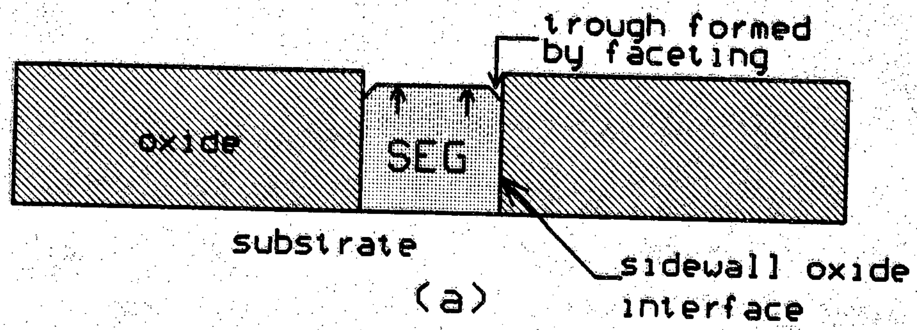
CHAPTER 2 - LITERATURE SURVEY

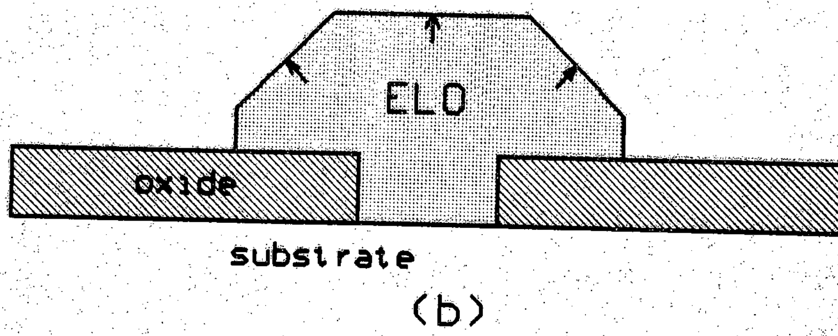
2.1 Selective Epitaxial Growth Technologies

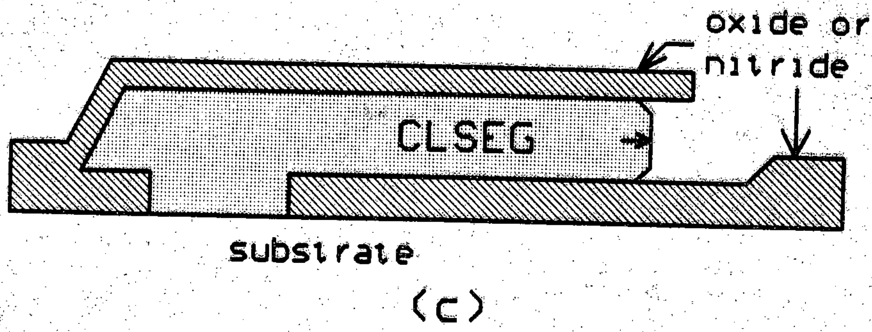
Silicon Selective Epitaxial Growth (SEG) is a technique which allows the epitaxial growth of silicon only at selected locations on a wafer. SEG evolved from full-wafer silicon epitaxy, and hence, the growth conditions are quite similar to those of full-wafer epitaxy. SEG has only recently overcome problems with defects, nonuniform growth rates, and selectivity with the utilization of purified hydrogen (H_2), hydrogen chloride (HCl), and dichlorosilane (SiH_2Cl_2 or DCS) gasses at low temperatures (<1000 $^\circ$C) and reduced pressures (10-200T) in cold wall epitaxial reactors [3-8].

Selective epitaxy is grown in seed holes, which are defined in a high temperature mask, usually oxide, on a silicon wafer as shown in Figure 2.1(a). The selective epitaxial deposition is performed under conditions which allow epitaxial growth only on the exposed silicon surfaces and not on the oxide surfaces. Epitaxial Lateral Overgrowth (ELO) is grown under identical conditions as SEG, but ELO is grown for longer periods of time so that the epitaxy grows out of the seed hole, spreading laterally over the oxide mask as depicted in Figure 2.1(b). Confined Lateral Selective Epitaxial Growth (CLSEG) [9] is grown using the same conditions as SEG, but the silicon grows vertically and then laterally in a cavity or tunnel in the oxide or nitride layer as shown in Figure 2.1(c).

The SEG deposition begins with a H_2 bake and an optional HCl etch, both at the deposition temperature, to clean the silicon growth surface in the seed


trough formed
by faceting
oxide
SEG
substrate
sidewall oxide
interface
(a)


ELO
oxide
substrate
(b)


oxide or
nitride
CLSEG
substrate
(c)

windows. During the H_2 bake, the reaction $Si + SiO_2 \longrightarrow 2SiO_{(g)}$ removes the native oxide [10]. This etch competes with the oxidation of silicon by water vapor and oxygen [11,12] and requires a very dry and oxygen free environment for removing the native oxide. H_2 is introduced into the reactor during this etch since it is easily cleaned and dried, will not react with the wafers or the epitaxial reactor, and because it will displace or carry out the residual H_2O and O_2. The H_2 gas becomes the principal source of H_2O and O_2 in the reactor, such that purifyers on the H_2 lines can significantly lower the H_2O and O_2 partial pressures in the reactor, as does the utilization of reduced pressure operation. Because of the dependence of the reaction rates on temperature, the H_2O and O_2 partial pressures in the reactor must be lowered as the deposition temperature is lowered.

The etching of the native oxide proceeds from defects or contamination on the oxide. Pinholes form at these points, and grow across the surface until they meet when all of the native oxide has been removed [10]. During the H_2 bake, the native oxide is not thinned because the oxide reacts with the silicon only at the exposed silicon/oxide interfaces. This reaction will undercut and lift-off portions of the oxide mask if it proceeds too quickly (at high temperatures) or is carried out for too long [13]. The dry, oxygen free environment must also be maintained during the deposition so that SiO_2 is not incorporated into the epitaxial silicon [14].

The HCl etch does not attack the native oxide but does etch the silicon surface. This etch is performed after the native oxide has been removed with the H_2 bake and is used to remove surface impurities or surface damage that may occur from a Reactive Ion Etch (RIE) step. The atomically clean surface required for low defect epitaxy is created.

Selective epitaxy depositions are performed in the same type of inductive or radiantly heated cold wall reactors as are used with full-wafer epitaxy, except that SEG is typically deposited in reactors capable of reduced pressure operation. The cold wall reactor is used to minimize contamination from the wall of the reactor and to help prevent gas phase nucleation of silicon. The lower temperature walls have a lower rate of desorption of adsorbed gasses, water vapor, and other impurities, resulting in a lower concentration of the impurities in the gas stream. Incorporation of these impurities into the epitaxial silicon growth results in higher defect densities, and the degradation of the performance of devices made in these areas. Gas phase nucleation is undesirable because it leads to non-epitaxial deposition (polysilicon). In a cold wall reactor, the gasses are much cooler than the substrate and attain decomposition temperatures only when near the substrate. As the deposition gas is heated near the surface, it partially decomposes and forms intermediate deposition compounds. Some of these compounds are adsorbed onto surface sites on the exposed silicon substrate where they further react to ultimately yield a new silicon atom bound in the crystal lattice of the substrate. DCS is typically used as the silicon source gas, but silicon tetrachloride ($SiCl_4$), trichlorosilane ($SiHCl_3$), and silane (SiH_4) can be used as well [3,15-17]. A carrier gas of hydrogen is used to improve the uniformity of the growth rates across a single wafer and from wafer to wafer without contaminating the chamber.

Nucleation on the oxide mask grows into polysilicon (poly) and produces nonselective growth. The prevention of nucleation is most easily achieved with the addition of HCl to the deposition gasses [3], but the selectivity is also affected by the DCS and H_2 flow rates, the deposition temperature, and the deposition pressure. When nucleation does occur, there is typically a denuded zone around

photolithography difficult and reduce the integrity of metal and polysilicon interconnect lines. One solution to this problem is to planarize the surface of the wafer after the SEG step. A typical planarization technique requires the conformal deposition and re-flow of an oxide, leaving a planar surface for interconnects. Another planarization technique which can be used begins with nitride islands on the oxide SEG mask. ELO material is grown between seed windows and the nitride islands. All of the epitaxy above the oxide is etched off using an chemical-mechanical polishing technique. The nitride islands act as an etch stop so that a uniform thickness of epitaxy can be defined above the masking oxide. An additional benefit with this technique is that it compensates for potential nonuniform growth rates of the epitaxy, either across the wafer, wafer to wafer, or from run to run.

Intra-wafer and inter-wafer uniformities have been reported as 2-5% [22,23]. In general, lower deposition temperatures and pressures will provide better uniformity was discussed above. Decreasing the ratio of oxide area to silicon area improves the uniformity within a run [24]. The fine tuning of the epitaxial parameters, which maximize uniformity, vary considerably between reactors and operating points. This is a complex problem which is currently being studied by others.

Early attempts at ELO focused on achieving large aspect ratios of lateral epitaxial growth across the oxide mask to vertical growth above the mask. The large aspect ratio was desired for application to a Silicon On Insulator (SOI) technology. For this technology, wide thin layers of silicon would be dielectrically isolated for use in building devices. Early reports of aspect ratios greater than one [17] have not been repeatable, and may have been exaggerated due to measurement errors caused by growth from pinholes formed in thin oxides.

Reproduceable aspect ratios are approximately 1:1. The recently introduced CLSEG technique can be used to achieve effective aspect ratio greater than 1:1 because it allows long thin fingers of epitaxial silicon to be grown exactly where they are desired and with a precise thickness.

The dopant level in the epitaxial layer is controlled by the amount of dopant introduced into the reactor, by the dopant concentration in the substrate, and by how far the epitaxial layer has grown above the substrate. The intrinsic doping with no intentional dopants introduced into the reactor and a lightly doped substrate is about 50Ω-cm and n-type. The gaseous dopants which are intentionally introduced include diborane (boron), phosphine (phosphorus), and arsine (arsenic). These dopants are introduced into the reactor along with the silicon source gas. Attempts to change the dopant concentration during the epitaxial growth may be affected by enhanced diffusion along the sidewall interface. The enhanced diffusion is a result of weak bonding at the interface created by the etching effect on the oxide from the $Si + SiO_2 \rightarrow 2SiO$ reaction.

Two phenomena, solid state diffusion and autodoping, are responsible for the interaction between the substrate dopant concentration and the doping of the epitaxial layer: solid state diffusion, and autodoping. Solid state diffusion is the diffusion of the dopant along its concentration gradient. Autodoping is a process where the dopant present at the surface of the wafer leaves the surface of the wafer, enters the gas phase, and is then reincorporated into the growing epitaxial region. Autodoping has a similar effect as solid state diffusion, but it produces a slightly different dopant profile. Both autodoping and solid state diffusion are minimized with the low temperature reduced pressure conditions utilized for selective epitaxy.

Low defect density in the bulk regions of SEG have been demonstrated by fabrication of bipolar and MOS transistors, and planar gate controlled diodes that have electrical characteristics similar to those made in substrate material [25-27]. The minority carrier lifetimes in the bulk SEG regions were within an order of magnitude of the lifetime in the silicon substrate [25,26].

The defect density associated with the SEG silicon/oxide sidewall interface, noted in Figure 2.1(a), is much greater than the density of defects at the silicon/oxide interface created by thermally oxidizing the silicon substrate. These SEG sidewall defects lead to larger p-n junction leakage currents and lower breakdown voltages in walled p-n junction diodes than in similar planar diodes fabricated in the same SEG material [20,27-30]. Walled junctions terminate at the silicon/oxide sidewall interface along the perimeter of the SEG seed hole as shown in Figure 2.3(a). Reverse bias leakage currents of walled diodes have been reported with a minimum mean ten times greater than those of the planar diodes of Figure 2.3(b) [27-29]. More importantly, it is reported that the leakage currents in walled devices are less consistent from device to device than in planar devices with identical bulk doping profiles [20]. This is an important performance criteria for typical integrated circuits that have thousands of transistors and must be designed to tolerate the average worst case performance of all the transistors on a die. Junction breakdown voltages are reported to be lower for walled junctions than for planar junctions. This may be due to enhanced diffusion at the sidewall defects which would produce a rough p-n junction.

In summary, the two most critical problems with SEG are faceting and the sidewall defects. The faceting can be overcome with additional conventional process techniques. The sidewall defects near walled junctions increase the reverse bias junction leakage currents across the junctions and lower the junction

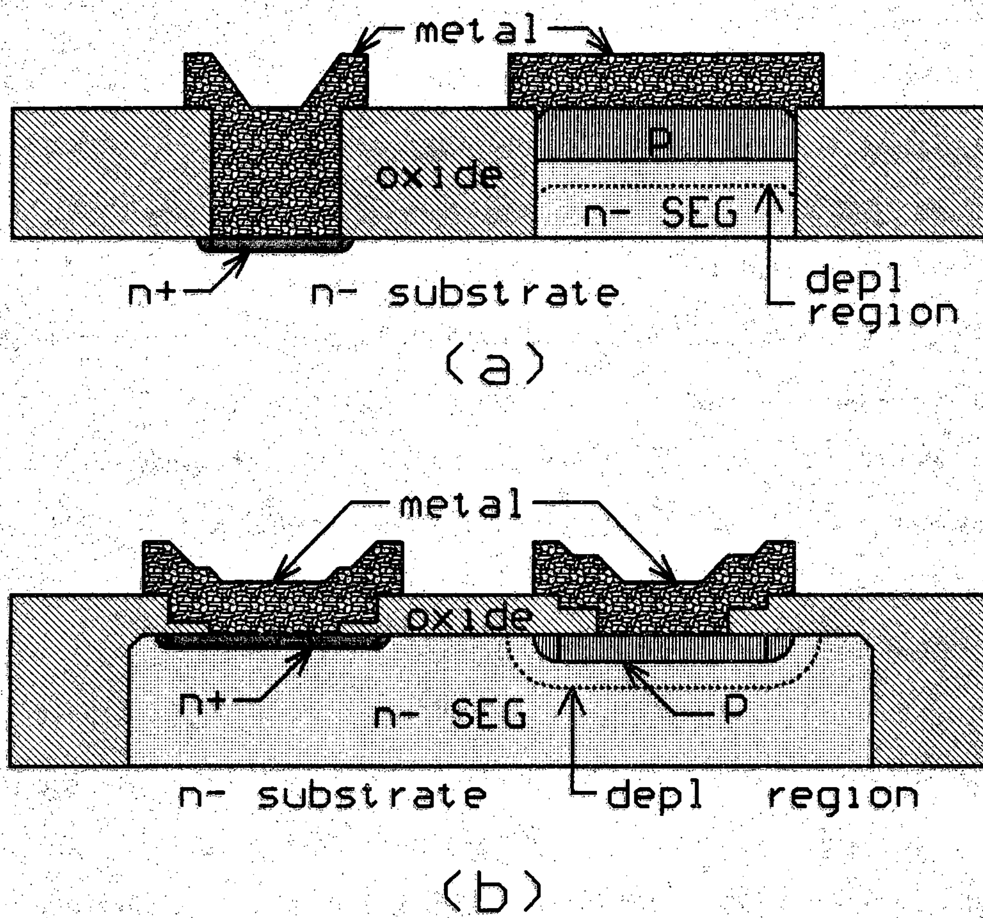


Figure 2.3. a) Walled and b) planar p-n junction diodes formed in SEG.

breakdown voltages. These effects degrade device performance, increase power consumption, and increase substrate currents which can lead to latchup. The sidewall defects need to be quantified and reduced by special techniques which is the subject of this thesis.

2.3 Sidewall Defects

2.3.1 Published Data

The published data on the SEG/oxide sidewall interface defects includes walled diode data, TEM evaluations, results from defect etching, and data from near sidewall planar diodes used to find and identify the defects. Early data [17] consisted of the recording of the defects that was enhanced by the Schimmel defect etch [31] on SEG grown from SiH_4. Dislocations and stacking faults were also reported.

The next report [7,20,27] included both TEM and walled diode data. SEG grown with DCS, HCl, and H_2 at 50T and 950°C produced walled diodes with larger leakage currents when the seed hole was aligned to the [110] direction compared to the [100] direction on a (100) wafer. Secondly, 1000Å of nitride on the sidewalls resulted in a larger spread of leakage currents than did oxide sidewalls. Defects that could be seen at the top surface of the SEG with an optical microscope were recorded per length of sidewall interface for SEG grown at different temperatures and HCl flow rates. SEG grown with higher HCl flows or lower deposition temperatures resulted in fewer sidewall defects at the surface. Finally, TEM analysis revealed stacking faults and dislocations near the sidewall interface.

Similar results to those discussed above were reported by another group [32]. Edge MOS transistor leakage leakage currents, equivalent to walled diode leakage currents, were reported as a function of deposition temperature, pressure, HCl concentration, and seed hole alignment. Lower temperature, reduced pressure depositions, lower HCl flow rates at 1050 °C, and alignment of the seed hole to the [100] direction all reduced the leakage currents. Walled diode leakage currents in SEG grown at 30T and 850 °C were 3-4 orders of magnitude lower than the leakage currents of walled diodes in SEG grown at 760T and 1050 °C. Optical defect counts were conducted, these counts support the leakage current data except for the HCl concentration results. Reduced temperature and pressure during the deposition lowered the visible defect density at the SEG surface along the sidewall interface. The visible defects decreased with increasing HCl flow rates when compared to the increased leakage currents with higher HCl flow rates reported in the same article. No explanation was offered for the discrepancy in the effects of HCl. Finally, TEM analysis revealed stacking faults and dislocations. These defects were reduced in number when the edges of the seed were aligned to the [100] direction instead of the [110] direction on (100) wafers. Twinning was looked for but not observed.

TEM analysis by a different group [21] revealed twinning, but no stacking faults or dislocations in SEG grown with DCS, HCl, and H_2 at 50-100T and 950-1000 °C.

Planar diodes built near the sidewall interface were tested [22] to find the dependence of defect density on distance from the interface and as a function of deposition temperature. The planar diodes were situated at a range of distances from the sidewall interface in 0.5μm increments. The sidewall leakage current dropped by an order of magnitude and became constant at a distance of 2μm

from the sidewall interface. The leakage also dropped by half an order of magnitude as the deposition temperature was dropped from 1000 ° C to 900 ° C.

In summary, lower deposition temperatures and pressures reduce the sidewall interface defect densities as does alignment of the seed hole to the [100] direction. It is not clear what affect the HCl flow rate has on the defect density, and it is not clear what defects are being created along the sidewall interface.

2.3.2 Theories on the Cause of the SEG/Oxide Sidewall Defects

Based on the data presented, three theories on the phenomena that may be responsible for the large junction leakage currents have been published: interface states due to weak bonding between the SEG silicon and the oxide wall; defects induced by thermal stress after the SEG growth; and defects nucleated as the silicon grows along the sidewall interface.

Excessive interface states resulting from weak bonding between the epitaxial silicon and the oxide mask can produce excessive sidewall leakage currents. Evidence for weak bonding include enhanced diffusion of impurities along the interface and an enhanced oxide etch rate along the sidewall interface [30,33]. Weak bonding is probably a result of the $SiO_2 + Si \longrightarrow 2SiO_{(g)}$ reaction at the silicon/oxide interface during the epitaxial growth [10,11]. This reaction etches away the silicon and oxide atoms at the interface and leaves a sheet of voids in their place. These voids result in dangling silicon bonds which are the source of interface states.

Recent results from poly/oxide/ELO capacitors, fabricated by growing ELO over the oxidized poly gate, have shown the bottom silicon/oxide interface of the ELO does not have an excess number of interface states after a 920 ° C anneal

[34]. This interface, beneath the ELO, is expected to be similar to the SEG sidewall interface. The capacitor study implies that interface states are probably not the major source of recombination-generation centers. Additionally, the enhanced oxide etch rates observed immediately after the epitaxial deposition are not present after a post-epitaxial oxidation [33]. The implication is the interface will be healed when it is re-oxidized during normal post-epitaxial processing. This would leave a thermally oxidized silicon surface with few interface states.

The second phenomenon which may be responsible for the large leakage is thermal stress induced by differences in the coefficient of thermal expansion for silicon and its oxide [35]. This stress may result in the formation of slip dislocations at or near the sidewall interface [36]. When patterns are aligned to the [110] direction, this stress is relieved along the (111) slip planes. This results in a large number of slip dislocations which propagate up the (111) slip planes. Patterns aligned to the [100] direction do not have stress lines aligned with slip planes and are not as likely to nucleate defects. The thermal stress induced during the cool down immediately after the SEG step may be concentrated at fewer points of bonding along the sidewall due to the weak bonding mentioned above. Increased stress at fewer points has a higher probability of producing dislocation defects near the epitaxial sidewall than the better silicon/oxide bonding present after a thermal oxidation.

Finally, it has been theorized that some defects are nucleated at the sidewall during the silicon epitaxial growth [21]. The influence of the oxide sidewall on the nucleation of the growth planes may create twinning, which has been observed with XTEM analysis. These defects propagate away from the interface during subsequent growth of the silicon. The slow growth planes along the sidewalls aligned to the [110] direction, are more likely to nucleate twins than the faster

growing {110} growth planes growing along the sidewalls aligned to the [100] direction. The presence of both the sidewall oxide and the twins may also explain the appearance of {113} growth facets near the sidewall aligned to the [110] pattern.

Although there is some evidence for each of the above phenomena, more information about the sidewall defects and the effects of changing process parameters are needed to fully comprehend the origin of these defects. Following the identification of the characteristics of these effects, procedures might be designed to eliminate or reduce them to an acceptable level.

2.3.3 Quantification of Electrical Defects at the SEG/Oxide Sidewall

To investigate the sidewall defects, the sidewall surface recombination velocity and near sidewall carrier lifetime need to be reliably measured. The devices used to measure these values on conventional planar surfaces include the junction diode, the MOS capacitor, and the gate controlled diode. The SEG/oxide sidewall interface has a unique location that makes the fabrication and operation of these devices more difficult, since planar devices cannot be used. In their place, similar, but more complex, device structures must be fabricated.

Walled diodes are the sidewall equivalent of planar p-n junction diodes and are the easiest sidewall devices to fabricate. They can be used to estimate the sidewall leakage current, but they will not yield the location of the defects with respect to the sidewall interface.

The walled diode requires a selective epitaxial step. This step includes a p-type diffusion into the selective epitaxy, an n^+ diffusion for the substrate contact, contact holes, and metallization. This process requires four mask steps and one

selective epitaxy.

The measurement of the reverse bias junction leakage current is sufficient for comparing the sidewall leakage currents of different walled diodes at low voltages. This is true because the bulk, or non-sidewall, leakage currents are insignificant. Evidence includes the data from planar diodes built in selective epitaxy that reveals reverse bias leakage currents of $1x10^{15}$–$1x10^{16}$ A/cm^2. These currents are two or more orders of magnitude less than the currents measured with walled diodes, and yet, the only difference between the two devices is that the junction of the walled diode terminates at the SEG/oxide sidewall interface instead of the surface of a typical thermal oxide interface. At high voltages, localized avalanche breakdown may occur as a result of geometric effects created by enhanced impurity diffusion. Enhanced impurity diffusion at defects may create diffusion spikes extending down from the p-n junction. The electric field will concentrate at these points, and this leads to localized early breakdown. The location of the junction depletion region is dependent upon the relationship to the sidewall interface, and it is dependent on both the height of the epitaxy and how fast the dopant impurities diffuse through the sidewall defects. This inconsistency with the location of the depletion region, in relation to the location of the sidewall interface, makes the walled diode a poor tool for the comparison of the effect of different SEG techniques on the sidewall defect density.

The MOS capacitor with a poly gate is very good for analyzing most interfaces. Unfortunately, it is more complex to fabricate than the walled diode, and it would suffer from too many parasitic capacitances and structural variations to be useful for evaluating the sidewall interface.

The fabrication of the sidewall capacitor, shown in Figure 2.4, begins with conventional fabrication techniques including a thermal oxidation, a poly deposition, a blanket implant to dope the poly, a photolithography step to define the poly, and a thermal oxidation of the poly. The second mask level is used to define the SEG seed with an RIE. The exposed poly is re-oxidized and a second RIE is used to re-open the seed hole while leaving the sidewall oxide intact before the SEG step. The SEG is protected with an oxidation, and the third mask is used to define diffused n^+ regions for low resistance contact to the SEG. Mask levels four and five are required for contacts and metallization. This process includes the added complexity of a masking step and two carefully monitored RIE steps when compared to the walled diode process.

The first problem with evaluating the sidewall interface is a range of flat band voltages will exist for the different locations along the interface. This will spread out the capacitor plots and make an analysis difficult and unreliable. The range of flat band voltages is partially due to the variation in the thickness from 1000Å to 2000Å of the sidewall oxide. This effect is caused by stresses on the poly during the sidewall oxidation, and the anisotropic etch is not ideal. These effects are discussed in greater detail in Section 4.2. The doping of the epitaxy will likely change along the sidewall due to the autodoping effects discussed earlier.

The second problem is a sidewall oxide of 2000Å is required to prevent the formation of pinholes in the oxide [37]. The oxide between the substrate and the poly gate can be at most 1μm, and the poly thickness may be at most 2μm due to anisotropic etch rates and the usable thickness of photoresist. Taking into account the generous alignment tolerances required because of the large step heights of more than a micron, approximately 10μm^2 of poly area would be needed for every 1μm of sidewall capacitor length. The result is the substrate

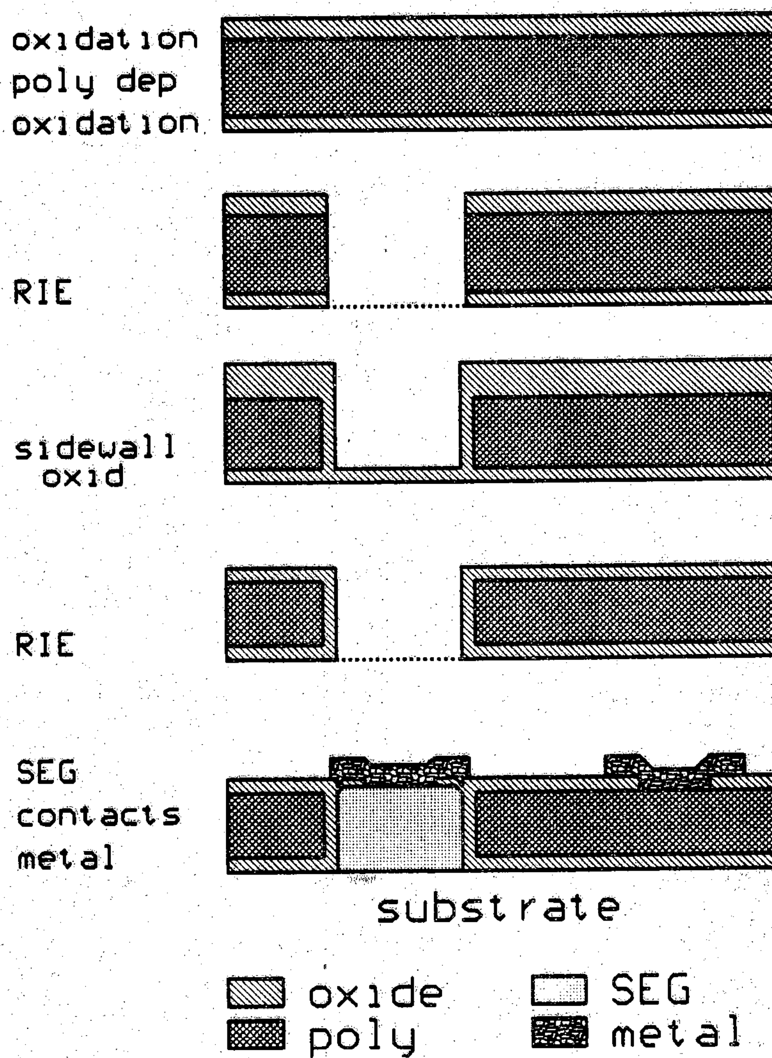


Figure 2.4. Sidewall MOS capacitor fabrication sequence with polysilicon gate and as-grown SEG sidewall.

accounts for one half of the total capacitance.

The third problem is to eliminate the effects of the depletion region extending into the substrate. Either the substrate can be doped or an additional poly layer can be fabricated between the gate poly and the substrate to act as a field plate. Doping the substrate will result in autodoping and will create a more severe vertical doping profile. This will extend the range of flat band voltages across the sidewall interface and further smooth out the capacitor plot. If a new poly layer is added under the gate, the capacitance from the gate to this poly layer will be even greater than the substrate-gate capacitance was, and the gate/SEG capacitance will account for approximately one third of the total capacitance. For these reasons, the sidewall MOS capacitor is not a good device for investigation of the sidewall interface related defects.

The Sidewall Gate Controlled Diode (SGCD) presented in this work is a new device structure and is the sidewall equivalent of the planar gate controlled diode. The SGCD is shown to be very useful for comparing the locations and densities of the defects in selective epitaxy grown under different fabrication conditions since the data produced will not be affected by the unique location of the structure. Enhanced impurity diffusion at defects will not affect the performance of the SGCD because the gated region is not diffused with any impurities. The device and its fabrication are complex and unique and are the subject of this thesis. The fabrication techniques developed for the SGCD have applications towards the fabrication of other device structures utilizing SEG technologies, such as the Epitaxial Lateral Overgrowth Bipolar Junction Transistor (ELOBJT) structure described below.

2.4 Applications of SEG

Silicon selective epitaxy technologies can be used for many different applications with both MOS and bipolar IC technologies. These applications include simple isolation techniques [8,19,20,27,38,39] as well as advanced device structures such as the ELOBJT [1,25], 3D-CMOS [40], compact DRAM [41,42], and SOI structures [18,26,36,43]. A simple isolation technique is first presented as an example of an immediate application of SEG. The ELOBJT structure follows, to show the potential of a more advanced application of the SEG technologies.

2.4.1 Isolation Techniques

Most current IC technologies rely on LOCal Oxidation of Silicon (LOCOS) isolation techniques. This technique requires 1-1.5 microns spacing between devices in addition to the minimum linewidth. This wasted space adds to interconnect parasitics and fabrication costs due to the larger die area required. Secondly, LOCOS isolation is relatively shallow and does not provide as much resistance to latch-up as does deeper isolation structures [44]. SEG technologies can provide isolation widths down to 1000Å with better latch-up resistance than LOCOS.

LOCOS isolation begins with a thin stress relief oxide layer followed by the deposition of a nitride layer shown in Figure 2.5. The nitride layer is defined, leaving nitride over the device regions. An oxidation is performed during which a thick oxide is grown in the field regions, but not under the nitride layer. The nitride and stress relief oxide are then removed to expose the silicon islands for the building of the devices. Very little oxide is grown under the nitride since oxygen diffuses very slowly through the nitride layer. The oxygen can diffuse laterally beneath the nitride film. At the edges of the nitride, oxygen diffuses to the silicon surface where it reacts with the silicon to form silicon dioxide. This produces the

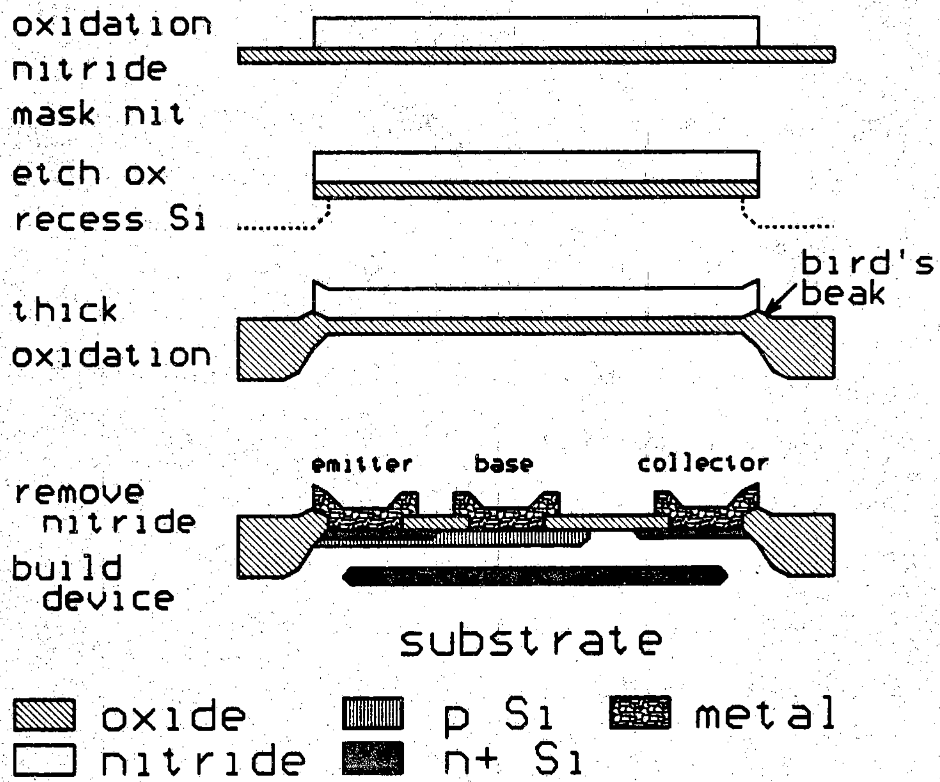


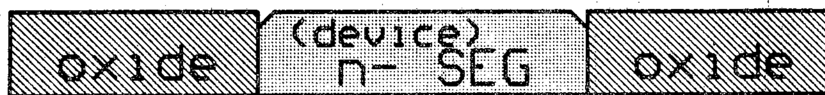
Figure 2.5. Typical LOCOS fabrication sequence with bipolar transistor.

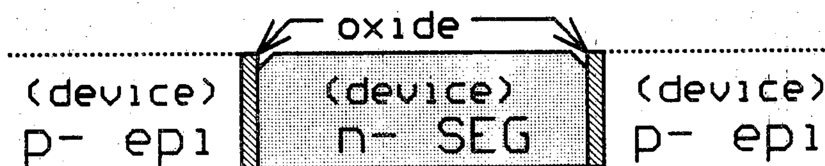
"bird's beak" phenomena seen in Figure 2.5. The "bird's beak" encroaches into the active device region, increasing the width of the isolation region by 1-2 microns.

Well isolation and tub isolation are used to refer to a number of different isolation techniques. In this thesis, the structure shown in Figure 2.6(b) is designated as well isolation and the structure shown in Figure 2.6(a) is designated as tub isolation. SEG well isolation can be used with bipolar, CMOS, or BiCMOS technologies. SEG silicon is used to fill wells etched into the substrate to form a planar surface. The wells of epitaxy are dielectrically isolated on the sides with oxide, and junction isolated from the substrate at the bottom of the well.

The complete well isolation process, shown in Figure 2.7, begins with the definition of wells into the substrate at a depth equal to the desired thickness. A 1000Å oxide is thermally grown to provide the sidewall isolation for the well. This thickness is the minimum required to prevent pinholes from forming in the oxide during the cleaning and deposition steps in the epitaxial reactor. The oxide on the bottom of the well is removed again before cleaning the wafer and performing the epitaxial deposition. The epitaxy only grows up from the bottom of the wells since all the other wafer surfaces are covered with the oxide mask. By doping the epitaxy as it is grown, the junction isolation to the substrate can be formed above the bottom of the oxide isolation wall of the well, and provides excellent isolation and latch-up resistance. The regions between wells can be used for dual well technologies.

The well isolation technique allows the epitaxy to be doped as it is grown. This provides wells with a highly versatile vertical doping profile. In the dual well process, this technique can be extended to give each set of wells its own doping profile, that is independent of the other set of wells. Currently, in





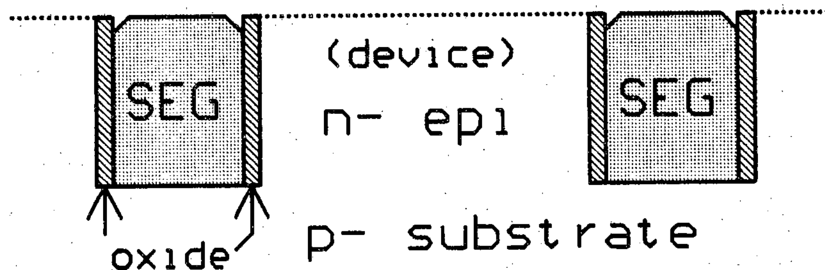


Figure 2.6. SEG isolation techniques: a) tub isolation, b) well isolation, c) trench isolation.

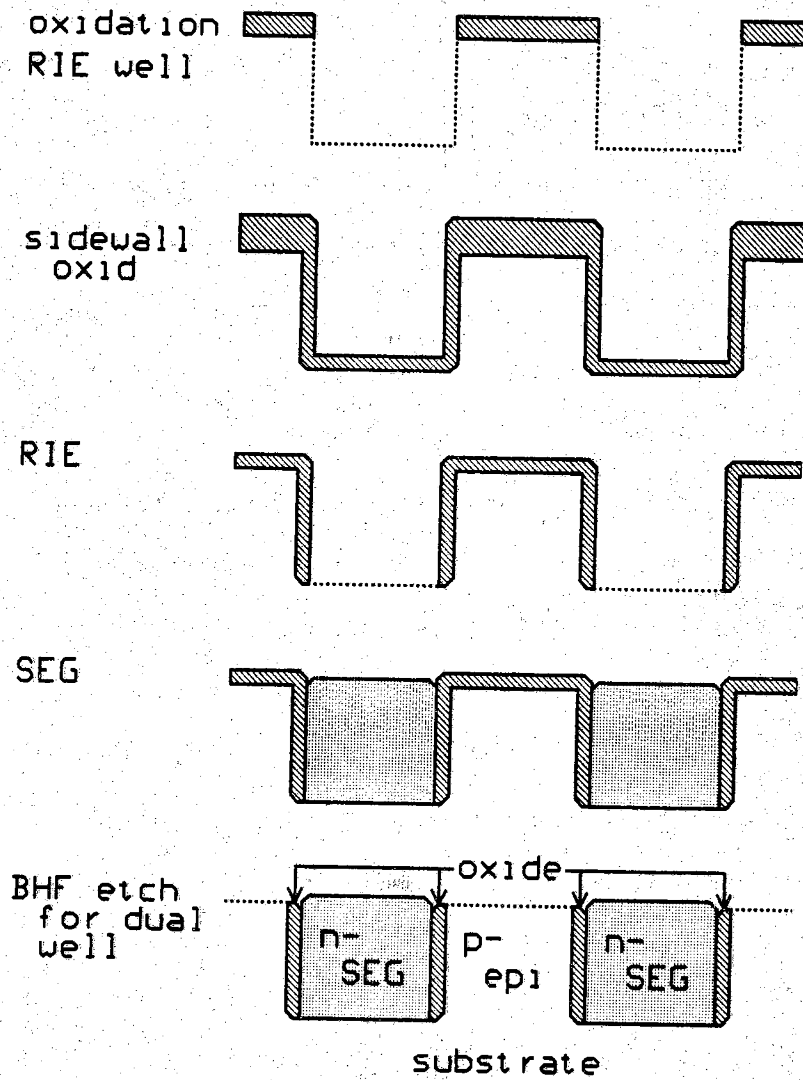


Figure 2.7. Well isolation fabrication sequence.

conventional CMOS, n-type wells are diffused into a p-type wafer. This produces a graded n-type well, and requires that some of the n-type impurities compensate for the p-type impurities present. Hence ionized impurities are created that do not add carriers to the silicon but do add scattering centers which lower the mobility. A light concentration of carriers in the p-type wells requires an exact knowledge of the n-type doping profile so that enough p-type impurities are present to compensate the n-type impurities as well as providing carriers. With the dual well SEG process, each well is grown independently, thus eliminating the compensated impurities.

Well isolation is also beneficial for bipolar technologies as an alternative to LOCOS isolation. In addition to the reduction in the amount of area used, well isolation provides a convenient vehicle for the creation of a buried layer. The buried layer can be incorporated in the growing of the SEG epitaxy. In this way the buried layer for each well is dielectrically isolated from the adjacent cell. It eliminates both the extra masking step required to define the buried layer, and the problems associated with alignment to the conventional buried layer. This alignment is difficult due to the tendency for the pattern to shift laterally during the epitaxial growth [45,46]. With well isolation, this pattern shift is overcome by aligning to the oxide sidewalls around the SEG wells.

Well isolation is a less complex technology than LOCOS. LOCOS isolation requires two mask steps; one for the buried layer, and one to define the nitride over the device regions. It requires the growth of doped epitaxy to form the n-type epitaxy layer that will become the device regions. A thermal oxidation and nitride deposition and removal are also required. Well isolation requires only one oxidation, one masking step to define the wells in the oxide, and the selective epitaxial growth. Reduced pressure epitaxial reactors are already used to grow

epitaxy for LOCOS to reduce autodoping and pattern shift. Selective epitaxy, therefore, requires only an adjustment of the growth conditions. SEG isolation eliminates a mask step and the nitride process, providing a less complex isolation technology. This type of SEG isolation has already been demonstrated with both CMOS and bipolar current mode logic circuits [8,20,38]. Because the devices are built in SEG material, the SEG material must have few defects so that device performance is not degraded.

Tub isolation, shown in Figure 2.6(a), [19,20,27,39] is similar to well isolation, but the seeds are etched to the bottom of a thick oxide. The SEG is grown in these oxide tubs to the top of the oxide layer. Contact to the substrate is difficult and extra process steps are required for a twin well technology (requiring devices in both n-type and p-type material). In addition, the minimum spacing between devices becomes the minimum linewidth which is much larger than the 1000Å separation which is attainable with well isolation. The advantage of tub isolation is that it is simple, using only one RIE, and because the substrate/interconnect capacitance is reduced due to the thick oxide under the poly and metal interconnects.

SEG is also useful for trench refill with trench isolation, [47] shown in Figure 2.6(c), because it can be used to refill trenches without forming voids [48]. This technique eliminates the need for low defect SEG because no devices are built in the SEG material. However trench isolation doesn't share many of the advantages of well isolation. First, the isolation spacing for trench isolation is the minimum linewidth instead of 1000Å of oxide. Second, for most applications, trench isolation requires an additional full-wafer epitaxial step to grow the device material on the substrate. Third, for bipolar technologies, trench isolation does not overcome the problems with pattern shift associated with aligning patterns to the buried

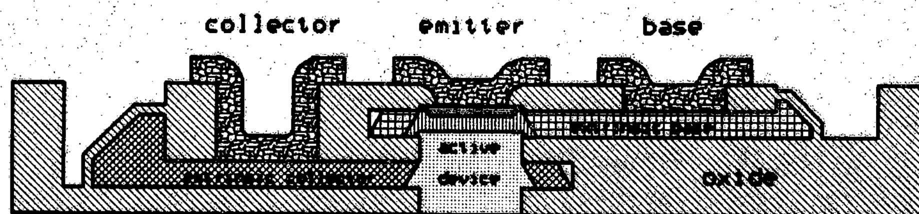
layer. Finally, trench isolation does not eliminate compensation with twin well processes.

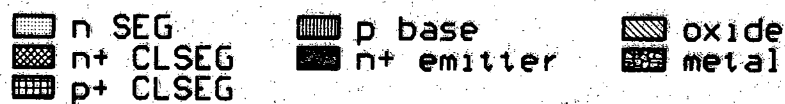
2.4.2 Epitaxial Lateral Overgrowth Bipolar Junction Transistor

The Epitaxial Lateral Overgrowth Bipolar Junction Transistor (ELO-BJT) had been proposed [5] to eliminate the standard buried layer and thereby decrease C_{cs}, R_c, and even C_{cb}. That structure and its fabrication have been revised to incorporate the advantages of the CLSEG technology.

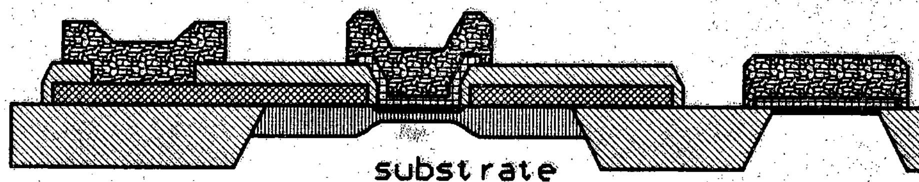
The revised ELOBJT, shown in Figure 2.8(a), is a self isolating high performance bipolar transistor structure fabricated with one SEG and two CLSEG steps. Along with self-isolation, the structure has other advantages such as reduced parasitic capacitances, reduced parasitic resistances, a flexible process technology, and potential application to BiCMOS. The SEG forms the intrinsic or active regions of the device and the emitter contact. The two CLSEG steps create the dielectrically isolated low resistance monocrystalline extrinsic regions between the intrinsic base and collector regions and their metal contacts. The emitter/base, base/collector, and collector/substrate junction dimensions are all minimum linewidths, and are all self aligned. Hence, the parasitic (extrinsic) junctions have been virtually eliminated.

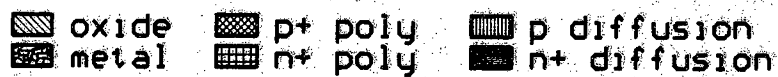
The ELOBJT fabrication process starts with a thermally oxidized (100) p-type silicon wafer. Polysilicon (poly) is deposited, defined, and oxidized to form the mold for the extrinsic collector CLSEG. Another poly layer is deposited, defined, and oxidized as a mold for the extrinsic base CLSEG. Next, the SEG seed hole (emitter) is masked with photoresist and anisotropically etched to the lower, or extrinsic collector, poly layer. A highly selective isotropic etch is used to remove all of the poly silicon from the wafer, leaving the oxide structures intact





(a)





(b)

Figure 2.8. a) Revised epitaxial lateral overgrowth bipolar junction transistor (ELOBJT) structure, b) Super self aligned bipolar transistor (SST) structure.

to form the cavities for the CLSEG of the extrinsic regions. The SEG seed hole is again anisotropically etched to the substrate. Cleaning the wafer precedes growing enough SEG to almost fill the seed hole. A thin oxide is deposited on top of the SEG, and a protective nitride is grown over the entire wafer. This nitride prevents further oxidation of the SEG and it can be removed with a wash etch later in the process.

A via hole is opened to the extrinsic collector cavity, and n^+ CLSEG is grown out to the via hole and then oxidized. Another via hole is next opened to the extrinsic base cavity, p^+ CLSEG is grown out to this via hole and also oxidized. The protective nitride and the thin oxide over the SEG are both removed before boron and arsenic are implanted into the SEG and annealed to form the intrinsic base and emitter regions respectively. Finally, contacts are opened to the extrinsic collector and base regions followed by metal deposition and definition steps.

There are many potential advantages of this structure, including very low parasitic capacitances and resistances, good inverted operation characteristics, and self isolation.

Switching speed and unity gain frequency (f_T) are limited by the transit times of the carriers through the device and by intrinsic and parasitic charging associated with specific device geometries. The dielectric isolation around the extrinsic base and collector regions provides lower base/collector and collector/substrate capacitances with the revised ELOBJT than with conventional structures. Virtually all bipolar transistors, including recent advanced structures, have used an n^+ buried layer or sub-collector to reduce collector resistance. Although a buried layer accomplishes its goal of reducing collector resistance, it inherently provides a large collector to substrate area and therefore capacitance

(C_{cs}). LOCOS [49], SICOS [50], and SST (shown in Figure 2.8(b)) [51-53], regardless of their advanced upper structures, have the same buried layer, with similar collector-substrate capacitance (C_{cs}) per unit area. The collector-substrate capacitance is normally the largest of all parasitic capacitances. For example, in the SST structure, C_{cs} is roughly a multiple of three greater than the collector-base capacitance (C_{cb}). Although C_{cs} does not enter into the unity gain frequency equation (defined with collector shorted to ground), it is frequently a significant parasitic in many circuit applications (digital and analog). Therefore, it is clearly desirable to eliminate the standard buried layer without increasing the collector resistance, as has been done with the ELOBJT.

Just as with the buried layer, all of the conventional bipolar transistor structures (except the SICOS structure) have parasitic extrinsic base/collector junctions, with a large associated capacitance (C_{cb}). The revised ELOBJT utilizes a sidewall extrinsic base to intrinsic (active) base region contact similar to that of the SICOS transistor. Device speeds are even more sensitive to C_{cb} than they are to C_{cs}, thus it is even more important to minimize this capacitance. As with the extrinsic collector, the dielectric isolation around the extrinsic base provides the minimal capacitance desired without increasing the base resistance.

The extrinsic base and collector resistances of the ELOBJT are minimized because they are highly doped monocrystalline silicon regions. In LOCOS devices, there is frequently no extrinsic base region, using an extension of the lightly doped intrinsic region instead. In SST devices, the extrinsic base region is poly crystalline, and therefore it suffers from the increase in resistivity associated with the poly grain boundaries. The extrinsic collector region is typically a buried layer which can not be heavily doped because a high quality epitaxial layer must be grown over it. The extrinsic regions of the ELOBJT can be highly doped

because their quality does not matter, they are only low resistance contacts to the active device. In addition, making a low resistance metal contact to the conventional buried layer requires additional process complexity and cost, which is eliminated with the ELOBJT. The dielectric isolation around the extrinsic regions also eliminates doping profile limitations imposed by the possibility of junction breakdown at the junctions between extrinsic regions in conventional devices.

The self aligned junctions are all the same size, and are defined at the minimum geometry of the photolithography and etching processes. These dimensions can be scaled down as lithography improves. This creates emitter/base and base/collector junctions which are both almost completely active. As a result, this device should also have good gain when operated in the inverted mode, with the emitter at the bottom and the collector at the top.

Device isolation is provided by the dielectric isolation on the sides and junction isolation between the active collector region and the substrate. Neither side of the collector/substrate junction is heavily doped, which minimizes the collector to substrate capacitance. In addition, the substrate junction is small and located under the center of the transistor. This means that although the isolation spacing between devices is small, the spacing between substrate junctions will be large and will help to reduce the possibility of latch-up.

As with the SEG well isolation and other applications of SEG technologies, the ELOBJT requires low defect SEG material to prevent device degradation, such as high reverse bias junction leakage currents and low junction breakdown voltages. For this reason, the sidewall defect density must be reduced especially with small dimension (high frequency) devices. The SGCD described in Chapter 3 was designed for the quantification of these defects so that techniques to reduce the defect density could be evaluated.

CHAPTER 3 - SIDEWALL GATE CONTROLLED DIODE DESIGN

The Sidewall Gate Controlled Diode (SGCD) was developed from the planar Gate Controlled Diode (GCD). Because of the 3-dimensional nature of the SGCD, the planar GCD is much easier to comprehend. Therefore, the planar GCD structure and its operation are presented first, followed by the design and the operation of the SGCD.

3.1 Planar Gate Controlled Diode

The planar GCD [54] can be fabricated as a three terminal device consisting of a diode and a MOS capacitor for the gate. The gate and the diode are located such that diode surrounds the gate, and the diode and gate slightly overlap as shown in Figure 3.1. The common terminal of the diode and the MOS capacitor is the ground contact. The other two terminals are labeled the diode and gate contacts.

To operate the GCD, the diode bias is fixed at a few volts reverse bias while the gate voltage is slowly ramped such that the region under the gate is swept from accumulation to depletion and finally into inversion, as shown in Figure 3.2. These changes in bias represent changes in carrier densities under the gate which result in changes in the surface and bulk generation currents flowing through the diode as described below. To see these changes, the diode current is plotted with respect to the gate voltage, as in Figure 3.3. This data is typical of planar GCD fabricated and measured at Purdue University. From this plot, the minority

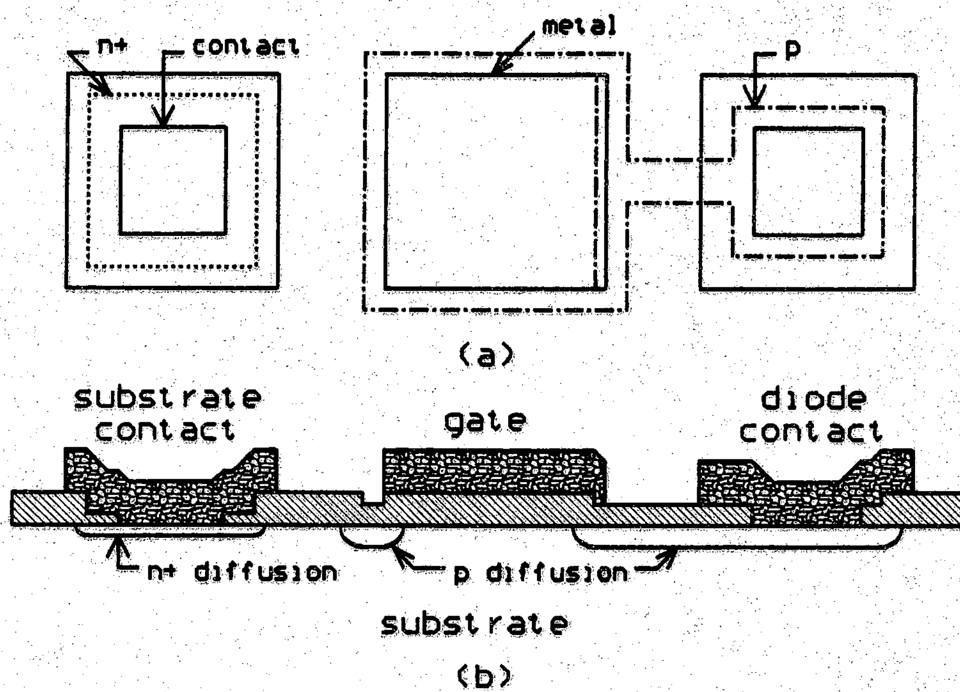


Figure 3.1. Planar Gate Controlled Diode (GCD); a) plan view of layout and b) cross section.

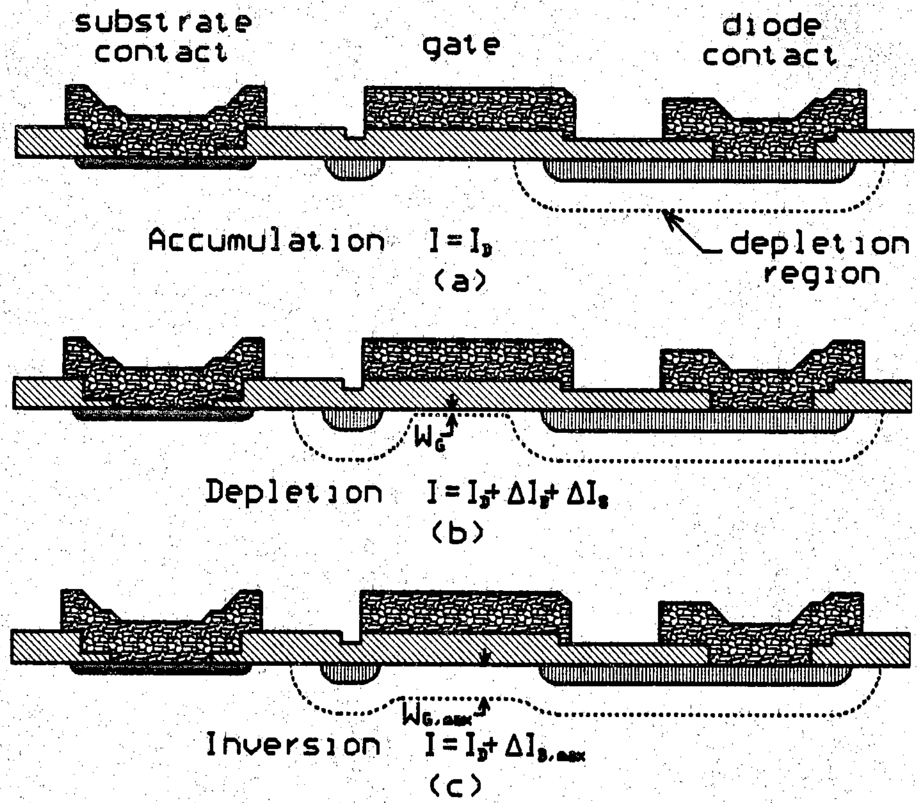


Figure 3.2. Generation currents and depleted regions of GCD for different modes of operation.

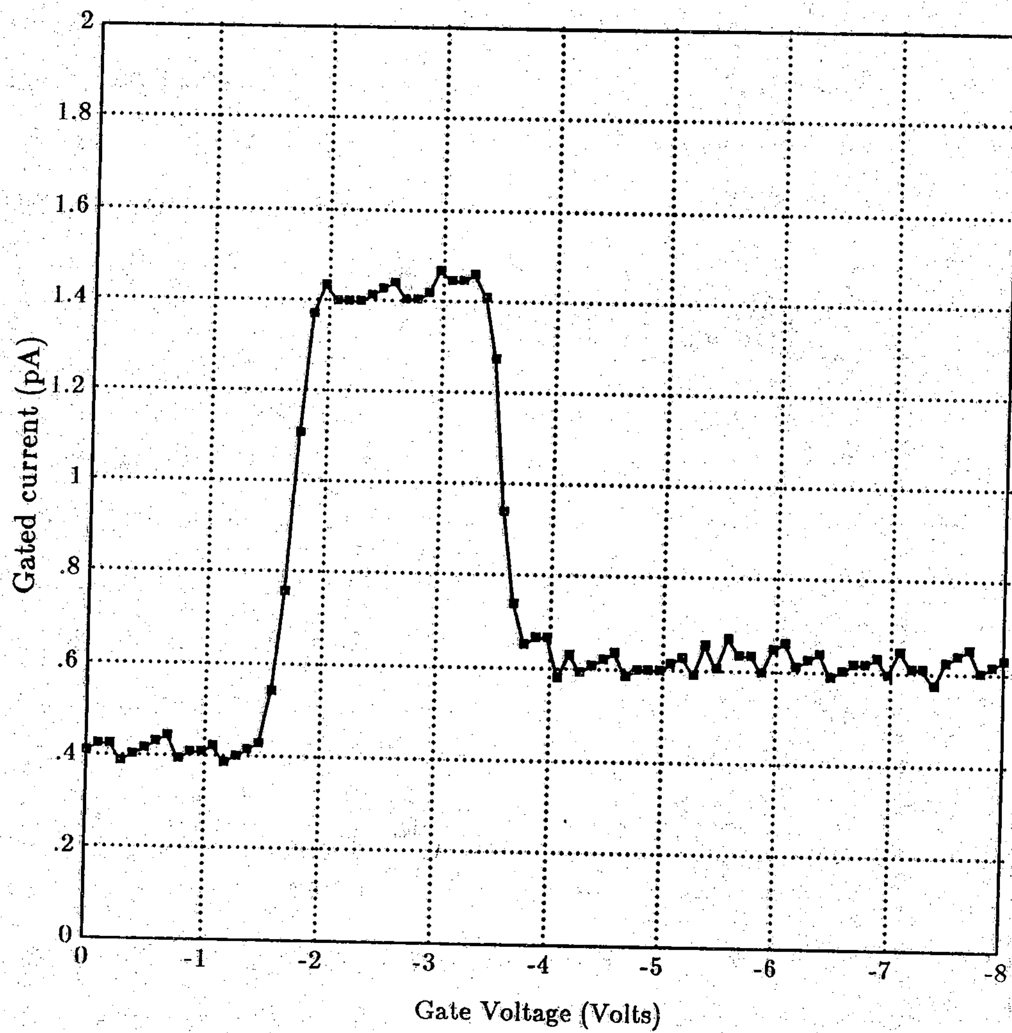


Figure 3.3. Typical planar GCD data from SEG: diode current (I_D) versus gate voltage (V_G).

carrier lifetime, τ_0, and surface recombination velocity, S_0 can be estimated.

In this mode of operation, the diode current will have three primary components. The first component is the reverse bias junction leakage current (due to both surface and bulk generation) along the physical diode junction, I_R. The other two components are generation currents generated under the gate region. One of these is due to bulk generation, I_B, and the other is due to surface generation, I_S. Because the diode bias is constant, the current component along the physical junction is constant. For this reason, the exact value of this current component is unimportant.

The gated bulk and surface generation currents are dominated by the Shockley-Read-Hall (S-R-H) generation current when the device is not biased into breakdown. The Shockley-Read-Hall process is the dominant recombination-generation (R-G) process in non-degenerately doped silicon. This is the process of recombination or generation of electrons in the conduction band and holes in the valence band through Recombination-Generation centers (R-G centers) located within the energy gap between these two bands. These R-G centers are defects in the otherwise perfect silicon crystal. The defects may be physical defects, such as a missing silicon atom or the interface between the silicon and the oxide; or impurity atoms, which might either replace a silicon atom at a lattice site (substitutional) or be located between lattice sites (interstitial).

The gated bulk generation current is proportional to the bulk generation rate, U_B, and can be calculated by integrating over the volume which is depleted of carriers, $I_B = qA_G \int U_B dz$. Similarly, the gated surface generation current is proportional to the surface generation rate, U_S, and can also be calculated by integrating over the surface area which is depleted of carriers, $I_S = qL_X \int U_S dy$.

Where q is the charge of an electron, A_G is the area of the gate, and L_X is the length of the gate on one side, the integral $\int dz$ is taken through the depletion width under the gate, and the integral $\int dy$ is taken over the length of the gate on the other side for a square gate.

The generation rates are determined from the S-R-H generation equation. After redefining the density of traps, N_t, as the density of traps within $3k_BT$ of the middle of the energy gap, replacing the exponents with 1.0, and assuming $\sigma_p = \sigma_n = \sigma$, the bulk generation rate can be approximated as:

$$U_B = \frac{\sigma V_T N_t (pn - n_i^2)}{n + p + 2n_i} \tag{3.1}$$

Similarly, the surface generation rate can be approximated as:

$$U_S = \frac{\sigma V_T N_{st} (p_s n_s - n_i^2)}{n_s + p_s + 2n_i} \tag{3.2}$$

where n_s and p_s are the carrier densities at the surface, and N_{st} is the trap density per unit area at the surface. In the depleted regions which are being integrated over, n, p, n_s, and p_s are all less than n_i, therefore the generation rates can be further simplified as: $U_B = \frac{\sigma V_T N_t n_i}{2}$, and $U_S = \frac{\sigma V_T N_{st} n_i}{2}$. Defining the minority carrier lifetime, τ_0 as $\frac{1}{\sigma V_T N_t}$, and the surface recombination velocity, S_0 as $\frac{\sigma V_T N_{st}}{2}$, then $U_B = \frac{n_i}{2\tau_0}$, and $U_S = n_i S_0$.

The gated surface generation current component, I_S, can now be integrated: $I_S = qL_XL_YU_S = qn_iS_0A_G$. This component is due to S-R-H generation at interface states along the silicon/oxide interface when it is depleted of carriers. When the region under the gate is in accumulation or inversion, $I_S = 0$. The surface recombination velocity is determined from the current I_S and the area of the gate,

A_G:

$$S_0 = \frac{I_S}{qn_iA_G}. \tag{3.3}$$

From the data plotted in Figure 3.3, $S_0 = 4\text{cm/sec}$ with $I_S = 1.0\text{pA}$ and $A_G = 1\text{x}10^{-4}\text{cm}^2$.

The gated bulk generation current component, I_B, can now be integrated: $I_B = qA_GW_{D,gate}U_B = \frac{qn_iA_GW_{D,gate}}{2\tau_0}$. This component is due to bulk S-R-H generation in the depleted part of the bulk region under the gate. As this region becomes more depleted, I_B increases. With the onset of inversion, the depletion width reaches a maximum, and I_B becomes constant at its maximum value, $I_{B,max}$. The average bulk lifetime can be estimated as:

$$\tau_0 = \frac{qn_iA_GW_{D,gate}}{2I_{B,max}}. \tag{3.4}$$

The depletion width can be calculated as a function of V_G using: $V_G{}' = V_G - V_{FB} = V_O + \psi_{Si}$. Substituting in $V_O = \frac{qN_DW_Dt_{ox}}{\epsilon_{ox}}$ and $\psi_{Si} = \frac{qN_DW_D{}^2}{2\epsilon_s}$,

$$W_D = \frac{qN_DW_Dt_{ox}}{\epsilon_{ox}} + \frac{qN_DW_D{}^2}{2\epsilon_{Si}}. \tag{3.5}$$

Equation 3.5 is set up as a quadratic for W_D and easily solved using the quadratic equation to get W_D as a function of V_G:

$$W_D = -\frac{\epsilon_{Si}}{\epsilon_{ox}} t_{ox} + \sqrt{\frac{\epsilon_{Si}^2}{\epsilon_{ox}^2} t_{ox}^2 + \frac{2V_G \epsilon_{Si}}{qN_D}} \tag{3.6}$$

As before, q is the electron charge, N_D is the dopant concentration in the semiconductor, t_{ox} is the oxide thickness under the gate, ϵ_{ox} and ϵ_{Si} are the oxide and silicon permeabilities respectively. The flat-band voltage (V_{FB}) is the gate voltage of the transition between depletion and accumulation (where the diode current first jumps up at approximately -1.0v), V_G' is the ideal gate voltage, V_O is the voltage across the oxide under the gate, and ψ_{Si} is the potential induced in the silicon by the charge in the depletion region (from the ionized impurities).

With equation 3.6, W_D is estimated at about $3\mu m$. using the data in Figure 3.3, τ_0 can now be estimated as $90\mu sec$.

Unfortunately, $W_{D,gate}$ is not constant under the gate because of the change in surface potential under the gate. This change in potential is due to the lateral current flowing through the depleted region to the diode [55] as shown in Figure 3.4. This effect makes the GCD a poor tool for measuring the actual lifetime when the defect densities are high, but it is a good device for comparing lifetimes when identical GCD structures are used. The GCD is also a good tool for separating surface and bulk effects.

3.2 Planar GCD Example

As an example of the use of a GCD, planar GCD were used to compare the quality of epitaxial silicon layers grown with and without residual oxide at the epitaxy/substrate interface. Two samples, A and B, both started with SEG seed holes defined in an 8000Å oxide. Sample B received a 500°C dry oxidation to form a thin oxide which was not removed with a buffered HF etch prior to the

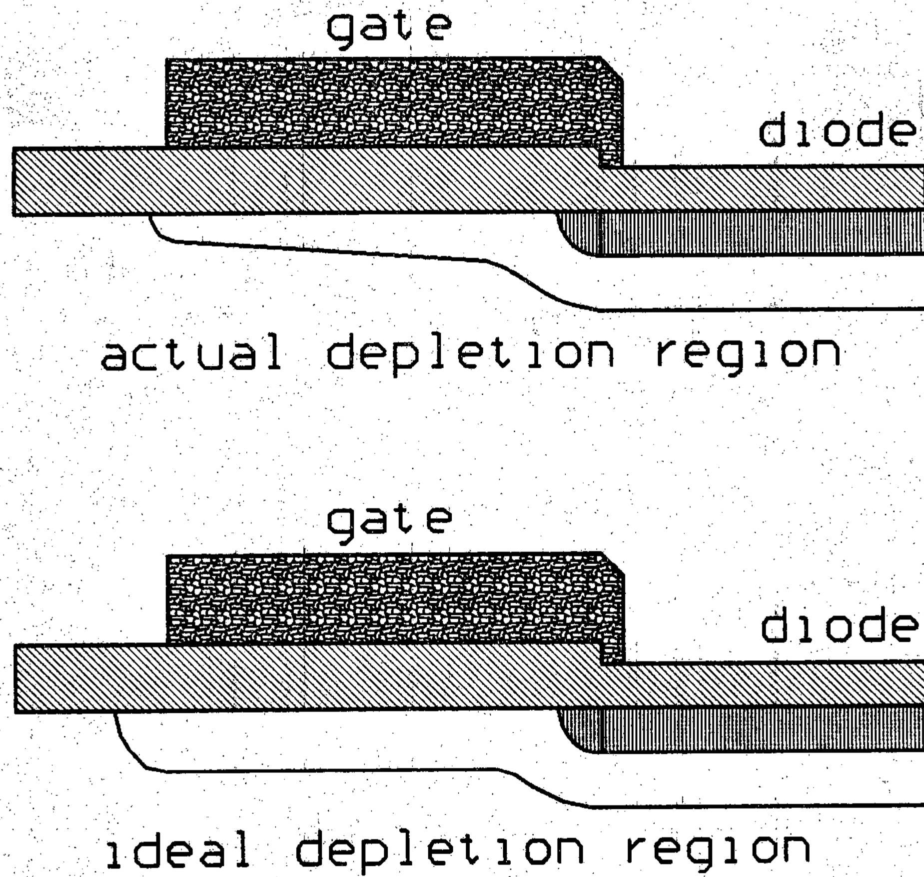


Figure 3.4. Change in depletion region due to lateral current flow under gate.

epitaxial deposition. The thicker oxide was not totally removed during the $950\,^{\circ}C$ H_2 bake before the epitaxial deposition. The samples did not receive an in-situ HCl etch prior to deposition. Using this cleaning procedure, islands of oxide were left at the substrate/epitaxy interface of sample B. Both samples received selective epitaxial depositions at $920\,^{\circ}C$, 150T, and with 1.76 slpm HCl and 0.44 slpm DCS. They were then processed as part of the same wafer set for the remainder of the processing steps required to fabricate the planar GCD.

The planar GCD were built in large Selective Epitaxial Growth (SEG) islands, away from the sidewall interfaces, and the structures were identical to the one shown in Figure 3.1. The gate was $100\mu m$ x $100\mu m$, with a total gate area of $10^{-4} cm^2$.

The GCD data from each of these two samples is shown in Figure 3.5. Sample A exhibits a well behaved I_B component, although the response was almost an order of magnitude higher than typical. The effects of surface generation are seen at 0.9v and 2.8v. Between these points, the rate of increase of I_B decreases as the gate voltage becomes more negative. This was expected for a region of constant carrier lifetime (no change with depth) because of the relationship between V_G and the depletion width under the gate (W_D). The bulk generation current becomes constant when the region under the gate becomes strongly inverted.

I_B of sample B is well-behaved for small gate voltages, but starts to increase rapidly at about $V_G = -2V$. As the gate voltage decreases, the depletion width increases, extending deeper below the surface of the silicon. When the depletion region reaches the substrate/epitaxy interface, the current suddenly increases due to a drop in the carrier lifetime caused by a high density of defects. These defects result from the residual oxide left at the substrate/epitaxy interface. Checking the depth with equation 3.6; $W_D = -.8\mu m + 2.0\mu m = 1.2\mu m$ using $V_G{}' = 0.9v$,

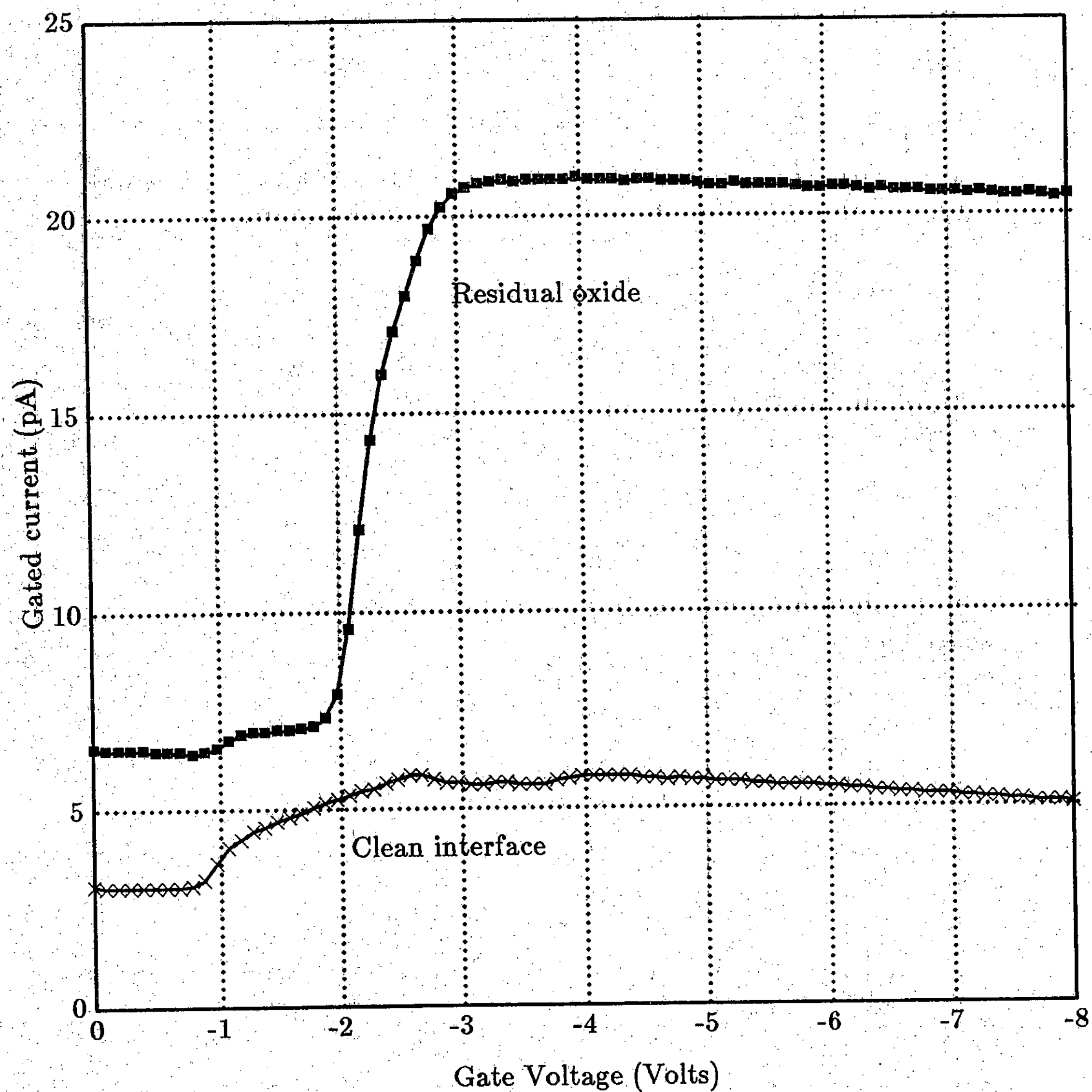


Figure 3.5. Planar GCD data: a) SEG grown with clean substrate interface, b) SEG grown with residual oxide at the substrate/SEG interface.

$t_{ox} = 0.25\mu m$, and $N_D = 1x10^{14}/cm^3$. This calculation is an approximation because the values of N_D, t_{ox}, and $V_G{}'$ are estimated values. This example is an excellent demonstration of the value of the GCD for investigating the defect density variations under the surface of the silicon. These results also show that most of the defects at the substrate/epitaxy interface, generated by the residual oxide at the interface before the deposition, do not propagate up through the epitaxial layer grown above this interface.

3.3 Sidewall Gate Controlled Diode Structure

The Sidewall Gate Controlled Diode (SGCD) is similar to the planar GCD, but is designed to evaluate the electron-hole generation rates at the SEG silicon/oxide sidewall interface and in the bulk epitaxial region near this interface. The device operation is similar to that of a planar gate controlled diode. The SGCD is built with a vertical gate instead of the horizontal gate of a planar GCD. This allows testing of the SEG/mask sidewall interface and the near sidewall electrical characteristics. SEG is grown up past the oxide isolated gate from the SEG seed hole. The complete SGCD layout and cross section are illustrated in Figures 3.6(a) and (b). Detailed cross sections of two parts of the main device fingers are shown in Figures 3.7(a) and (b) respectively. Note that the vertical dimensions in these figures are not to scale. The five SEG fingers under the field plate are 110μm long by 10μm wide, and 2μm thick.

The SGCD consists of a diode, an SEG region, two oxide isolated polysilicon (poly) regions, and an oxide isolated metal field plate. The diode in Figure 3.7(b) is a diffused p-n junction formed at the top surface of the SEG. The contact to the n-type SEG region is made through the n-type substrate. The second, or upper, level of poly forms the gate along the sidewalls. The first level of poly,

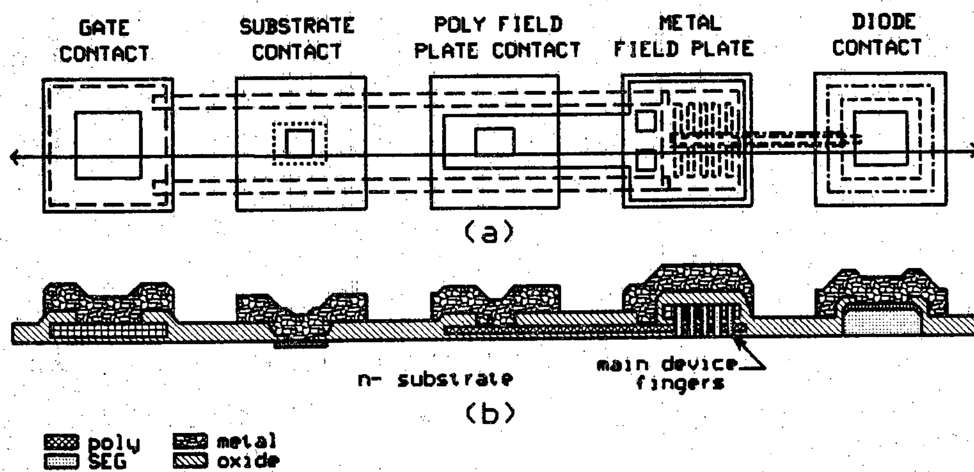


Figure 3.6. Sidewall Gate Controlled Diode (SGCD): a) plan view of layout and b) cross section.

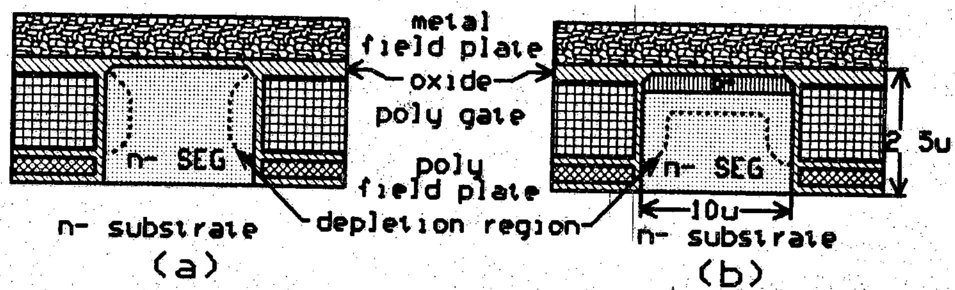


Figure 3.7. SGCD main device finger cross section: a) without diode and b) with diode.

closest to the substrate, and the metal over the fingers act as field plates to confine the depletion region.

The upper, or gate, poly is doped p-type to minimize the magnitude of the gate voltage required to bias the SEG into inversion, which minimizes the stress on the sidewall poly oxide. The gate "width" is actually the thickness of the gate poly, approximately 1.3μm, and is limited by the process technology available. The finger pattern is used to maximize the gate "area", which is a product of the gate poly thickness and the SEG seed hole perimeter within the gate poly region. The gated depletion regions extend laterally from the diode, along the SEG silicon/oxide interface at the sides of the fingers, until they meet at the end of the fingers [see Figure 3.7(b)]. At this point, the depletion region stabilizes at a maximum width. With a good quality interface, such as that formed with a thermal oxide, a gate area of 10,000μm^2 will produce a signal current of less than a picoampere. This is near the limit of reliable measurement, before the signal is lost in noise. If the defect density of the SEG sidewall is an order of magnitude worse than that of the planar thermal oxide as reported with walled diode data, a gate area of 1000μm^2 is required to produce a measurable signal. This requires a perimeter of approximately 1000 microns, which is the perimeter of the SGCD.

As described above, the GCD is most accurate when the length of the gate (from the diode to the point farthest from the diode) is minimized. This is easily done by forming the diode over the entire region of the SEG seed located in the gate poly region, but is impractical for two reasons. First, the SEG is lightly doped, such that the deletion region will extend down along most of the gate even when the gate is biased into the accumulation mode. This produces a surface potential gradient next to the gate. The gradient results in a more gradual transition between regions of operation, making the measurements difficult. The

second problem with the full region diode is that the diode current would be large, masking the change in the gated current components because the measurement resolution is a percentage of the total current.

The poly field plate prevents the depletion region from extending into the substrate under the gate poly. This poly is doped n-type so that it is conductive and has a negative flat-band voltage, V_{FB}. The negative V_{FB} allows the poly field plate to be tied to the substrate potential and bias the adjacent SEG into accumulation during normal operation. This accumulated region includes the substrate underneath the gate poly, and thus the poly field plate prevents generation in the substrate underneath the gate. The metal field plate above the SEG prevents the depletion region from extending across the top of the SEG finger. It also has a negative V_{FB}, and prevents generation at the top surface of the SEG when this field plate is tied to the substrate potential. The combination of these two field plates confines the gated depletion region to the sidewall interface.

The depleted region of the SEG is plotted in Figure 3.8 as simulated using the PISCES device simulator [56]. This shows that there is no depletion region when the region adjacent to the gate is in accumulation (for $V_G > 2V$), and how it grows as the gate voltage is dropped to the point of inversion. The confinement by the field plates was also simulated using PISCES, giving the depletion region shown in Figure 3.9. The three depletion regions shown resulted from simulations with 0, 2, and 4 volts applied to the field plates to show that the exact bias on the field plates is not critical. These simulations did not take into account the various oxide charges which would have shifted the flat-band voltages. Instead, the flat-band voltages were measured from the fabricated devices to insure that the regions adjacent to the field plates are not depleted with the field plates fixed at the substrate potential.

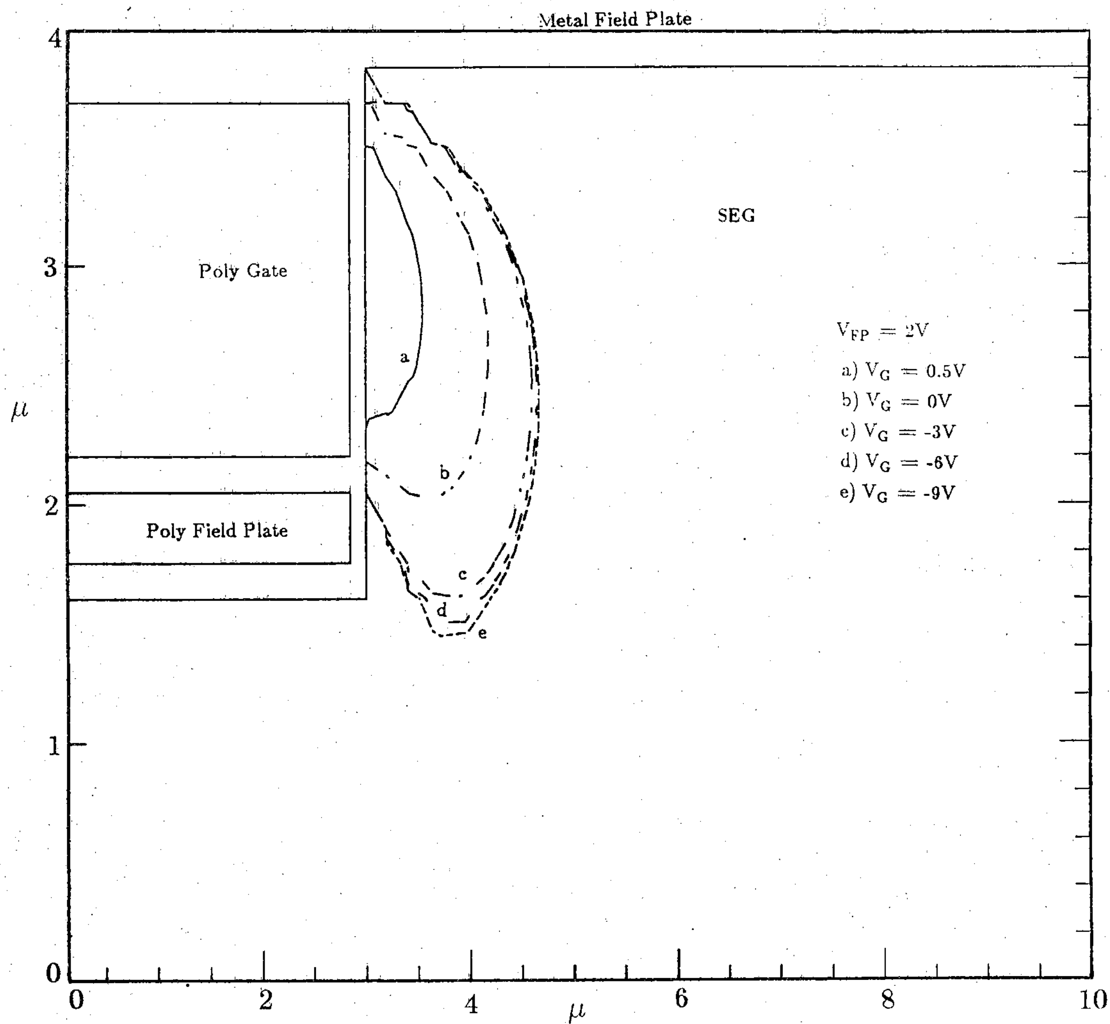


Figure 3.8. Depletion regions created with different gate biases simulated with PISCES.

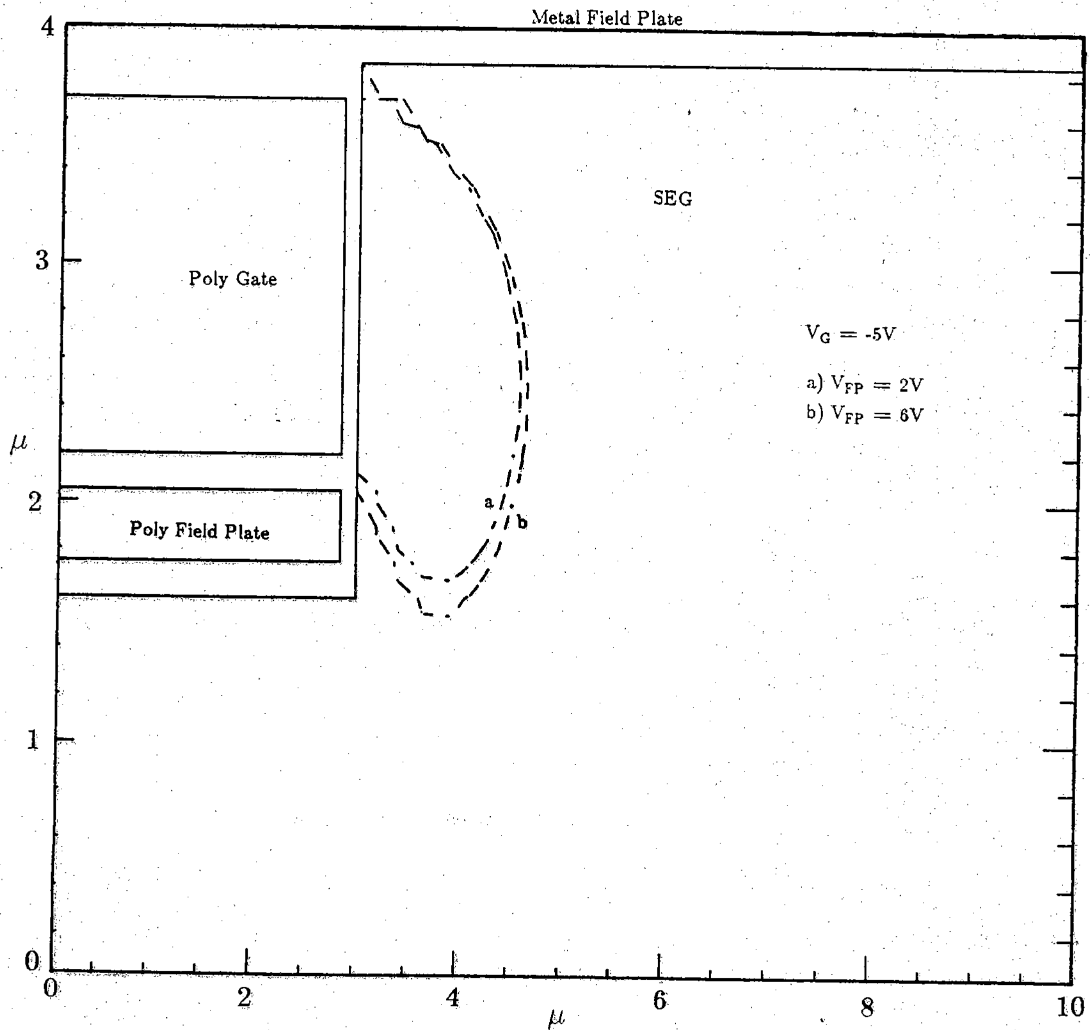


Figure 3.9. **Confinement of depletion region by field plates simulated with PISCES.**

3.4 SGCD Test Mask Layout

The initial design of the SGCD is shown in Figure 3.6(a). Seven mask levels are required to define the SGCD structure as listed in Table 3.1. These process steps will be discussed in greater detail in Chapter 4. A Reactive Ion Etch (RIE) well definition mask could have been added to the step before the SEG seed mask to define the wells, and then the SEG seed mask (slightly smaller) could be used to re-open the seed hole after the sidewall oxidation. This approach was avoided to insure that the sidewall angles and conditions in the SGCD would resemble typical SEG seed holes as much as possible. Most SEG seed holes are defined with RIE to achieve maximum packing density and minimum feature size. The layout was designed with 10μm design rules to minimize the fabrication and yield problems associated with the alignments and lithography steps. Smaller geometries and tighter alignments would not improve the performance of the SGCD, but would significantly reduce the yield of working devices.

The contacts for the gate, diode, and substrate are necessary for the operation of the SGCD. Two additional contacts were provided for the two field plates to allow separate biasing of each of them. This option allows the measurement of all their leakage currents independently of each other. The additional contacts also allow separate biasing of the monocrystalline silicon regions adjacent to the field plates to investigate the effectiveness of the field plates.

A second generation of SGCD were designed in attempt to improve the gated current to reverse bias junction current ratio, and to test various aspects of the sidewall defect densities. First, the ratio of the walled portion of the diode to the gated interface was minimized by locating the diode contact within the gated interface boundary. Second, devices were designed with four outside corners or no gated corners to investigate the defect density near SEG sidewall corners.

Table 3.1.
Mask levels of SGCD test mask set.

Mask Number	Region Defined
1	Field plate poly
2	Gate poly
3	SEG seed hole
4	Boron implant
5	Arsenic implant
6	Contacts
7	Metal

Finally, various sidewall alignments were incorporated into the same mask set to compare the defect densities associated with different sidewall alignments.

Other test devices in the mask set include bipolar transistors, planar GCD, MOS capacitors, resistors, and planar and walled diodes, all built in SEG islands. The bipolar transistors and planar GCD were used to investigate the bulk quality (defects) of the SEG as described in sections 4.3.1 and 4.3.2. The planar and walled diodes were used to investigate the sidewall defects where the SGCD could not be used, as described in section 4.2.3, and to verify the operation of the SGCD in Chapter 5. The MOS capacitors were included as process monitor devices. The MOS capacitors can be used to verify surface oxide thicknesses, doping densities, and carrier lifetimes. The resistors can be used to evaluate resistivities for modelling purposes, and to check some of the dopant profiles.

Alignment and resolution diagnostic structures are included with a large window for coarse alignments. Long SEG wells through the field oxide and combinations of the two poly layers are located across the dicing borders to provide cross sections, after dicing, for SEM analysis. Blank 6mm x 6mm windows with various combinations of poly, SEG, and doping are provided around the test devices for process monitoring. Finally, unused space between devices was filled with SEG seed windows to improve the SEG thickness uniformity across the wafer [24]. The layout of a complete die from the test mask is illustrated in Figure 3.10.

3.5 SGCD Operation

As with the planar GCD, the SGCD is operated by sweeping the gate voltage with the p-n junction diode held at a fixed reverse bias voltage. The bias of the two field plates is fixed at the potential which minimizes the diode current. Tying

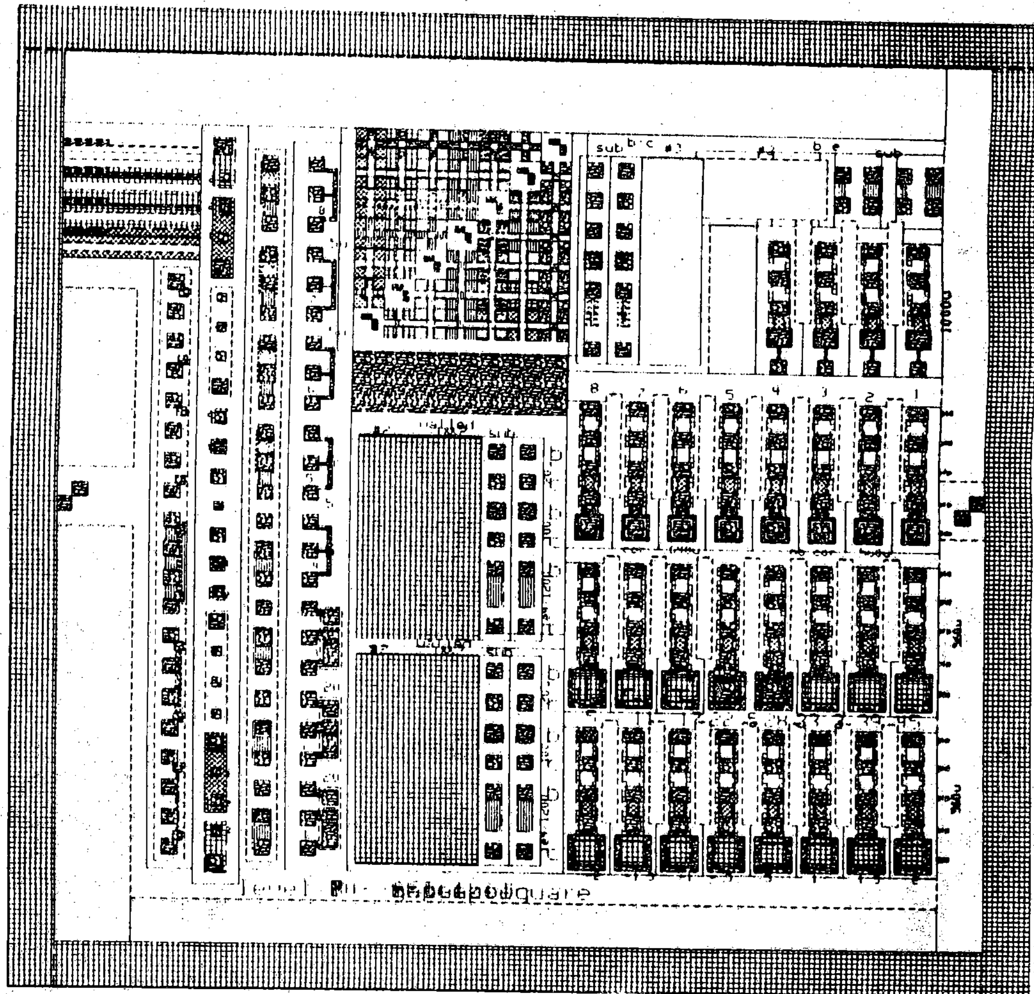


Figure 3.10. Complete die from SGCD test mask.

them to the substrate potential was sufficient for this work. The change in diode current, I_D, is recorded as the SEG sidewall region bias is changed from accumulation, through depletion, and into inversion. When the gate is biased into accumulation, the diode current measured is simply the reverse bias current, I_R, resulting from generation in the depletion region around the p-n junction. As the gate is biased from accumulation into depletion, two additional current components contribute to I_D. These include the interface generation current from depleted interface states at the SEG silicon/oxide interface, I_S, and the bulk generation current from the gated depletion region next to the gate, I_B. I_S rapidly approaches a constant value, while I_B starts at zero and increases as the gate bias is ramped towards inversion. At the onset of inversion, the interface becomes inverted, and I_S drops to zero. The depletion width reaches a nearly constant maximum value, and thus I_B also reaches a constant maximum value.

The surface recombination velocity at the sidewall interface, S_0, and lifetime, τ_0, can be estimated from I_S and I_B respectively, which are measured from the plot of diode current versus gate voltage. Knowing the area of the gate, A_G, and the width of the depletion region under the gate, W_D, the surface recombination velocity is estimated with the formula $S_0 = \frac{I_S}{qn_iA_G}$, and the carrier lifetime in the bulk is estimated as $\tau_0 = \frac{qn_iA_GW_{D,max}}{2I_{B,max}}$. Similarly, an approximation of the lifetime as a function of depth, or distance from the sidewall, can be made using

$$\tau_0(W_D(V_G),W_D(V_G+\Delta V_G)) = \frac{qn_iA_G}{2}\left(\frac{W_D(V_G+\Delta V_G)-W_D(V_G)}{I_B(V_G+\Delta V_G)-I_B(V_G)}\right), \quad (3.7)$$

where $\tau_0(W_D(V_G),W_D(V_G+\Delta V_G))$ is the average lifetime between $W_D(V_G)$ and $W_D(V_G+\Delta V_G)$, V_G is the gate voltage, and ΔV_G is the change in gate voltage.

Only one GCD or SGCD is required to estimate S_0 and τ_0.

The gated currents measured with the SGCD will be affected by vertical variations in both the doping density (autodoping in the epitaxy) and the sidewall oxide thickness within each device. These two phenomena will produce a very gradual gated response, such that the estimation of the location of defects and of the surface recombination velocity more difficult. The oxide thickness variation occurs during the second RIE, resulting from the fact that the sidewalls are not perfectly vertical. The variations in the vertical dopant profile results from a mismatch between the substrate dopant concentrations and the background dopant concentration of the epitaxy, leading to autodoping effects and a graded dopant profile. These variations result in a gradient in both the flat-band and threshold voltages along the vertical face of the poly gate, which spreads out the gated response for that device.

Planar GCD results from SEG with different dopant concentrations are shown in Figure 3.11. The data in the lower curve was taken from a planar GCD fabricated in epitaxy which was not intentionally doped. The data in the upper curve was taken from a planar GCD fabricated in epitaxy which was intentionally doped by placing heavily doped phosphorus wafers in the epitaxial reactor at the time of the deposition. The difference between the threshold voltage and the flat-band voltage for the autodoped SEG is about 2.6 volts versus approximately 1.4 to 1.8 volts (depending on the DCS flow rate) for the undoped SEG.

The threshold voltage (V_T) is the voltage where the diode current drops as the region under the gate becomes inverted. This occurs at a voltage equal to the sum of the diode voltage (V_D), the flatband voltage (V_{FB}), the built-in potential of the semiconductor (ψ_B), and the voltage across the oxide insulator (V_O). The diode voltage is externally applied, and thus is independent of the doping

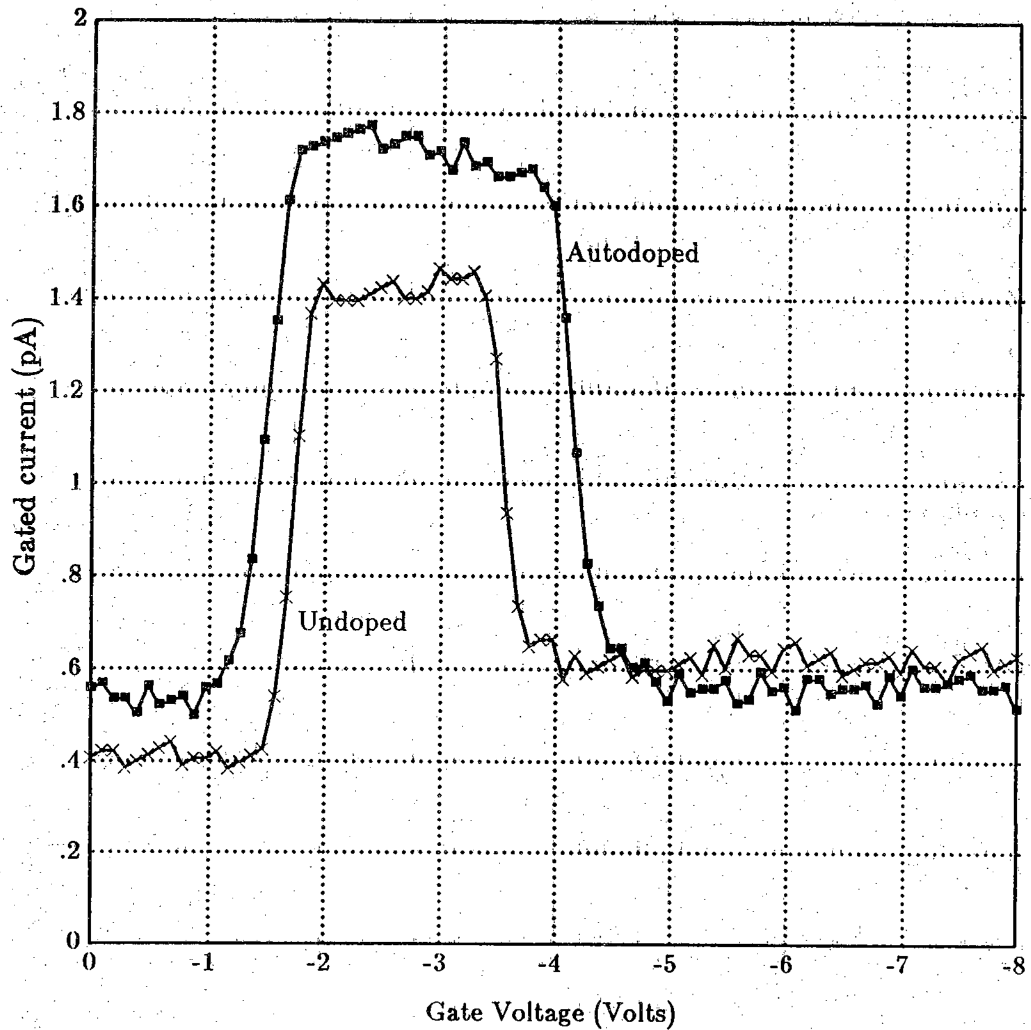


Figure 3.11. Diode current versus gate voltage data from planar GCD showing change in the threshold voltage (V_T) resulting from different epitaxial dopant concentrations.

concentration and oxide thickness of the GCD. The flatband voltage is equal to the poly-semiconductor workfunction difference plus any charges in the oxide or at the silicon/oxide interface. The charges at the silicon/oxide interface include charges resulting from lateral currents flowing along the gate to the diode. The lateral currents will produce different charges at different locations along the gate. These charges will increase near the diode as the current increases, thus the gated region farthest away from the diode will reach inversion before the region near the diode. This effect will spread out the gated response curve of the GCD if the generation rate in the silicon is high as shown in Figure 3.5. This can be used as an indicator as to when equation 3.6 is usefull because a sharp gated response will indicate low interfacial charges, and therefore little change in the depletion width. The built-in potential is a slowly increasing function of the doping density in the depleted region. The change in V_T due to ψ_B is negligible compared to the change in the oxide voltage. The oxide voltage is $V_O = \frac{qN_D W_D t_{ox}}{\epsilon_{ox}}$, and is proportional to the silicon doping density and the oxide thickness. The depletion width (W_D) is also a function of the doping density and the oxide thickness, such that a simple expression of the shift in V_T as a function of dopant concentration or oxide thickness is not obtainable.

When different parts of the gated regions have different doping densities, then the gated response is spread out as inversion is attained at a different gate voltage for each part of the gated region. Typical SGCD data from an intentionally autodoped epitaxial run (with phosphorus doped source wafers) is shown in Figure 3.12. The dielectric leakage current through the sidewall oxide contributes significantly to the diode current before the threshold voltage is reached. This is evident because the gate current increases rapidly with gate voltages less than

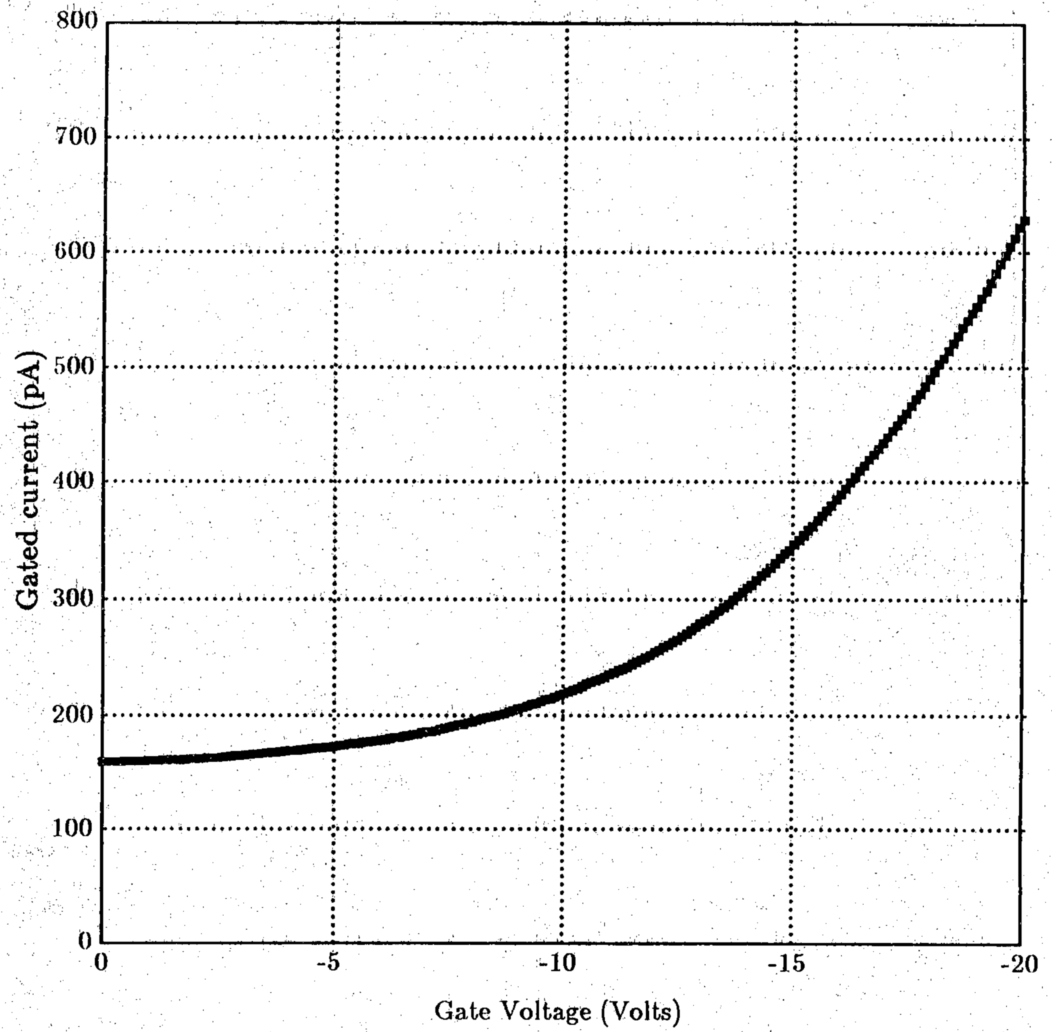


Figure 3.12 Diode current vs. gate voltage data from SGCD fabricated in intentionally autodoped SEG.

-20V. The SGCD data discussed in Chapter 5 is taken from SGCD which were not intentionally doped, and thus exhibit very small autodoping effects.

As with the planar GCD, the SGCD is affected by the lateral currents flowing along the gate to the diode at higher levels of current flow [55]. Again, this phenomena results in the underestimation of S_0 and an overestimation of τ_0, but does not affect comparisons of the S_0 and τ_0 from different interfaces as long as the SGCD structures are identical. Therefore, the SGCD is still an excellent device for comparing different interfaces, which is its intended purpose.

CHAPTER 4 - SGCD FABRICATION

The SGCD fabrication process can be separated into the following four process sequences; the conventional creation of the oxide/poly/oxide/poly/oxide structure, a new process sequence for the creation of the SEG seed hole, an SEG step, and a standard bipolar transistor process. The first sequence includes standard techniques of thermal oxidation, poly deposition, poly definition, and implantation. The next sequence, defining the SEG seed hole with the sidewall oxide covering the poly layers, creates a novel structure which required the design and development of a new fabrication process. An initial SEG technique, developed during previous work, was shown to be sufficient for fabricating the SGCD structure. This initial SEG technique was used to verify that the SGCD structure performed as intended, after which development of the SEG technique continued in an attempt to produce better quality SEG sidewall material as called for in the objective for this research. The final sequence was a bipolar process which, although adopted from a previous research project, proved to be sufficient for the requirements of this project.

An initial SGCD process design, based on SUPREM simulations and previous work, is presented first. The development of the seed hole is next described, including sections on plasma etching with CF_4 gas mixtures, plasma etching with Freon 115 and SF_6, and other aspects of the seed hole development. The third section includes an evaluation of the initial SEG technique as well as results from other SEG evaluations which do not utilize the SGCD. At the end of this

chapter, the final SGCD fabrication process is described. The final SGCD fabrication process run sheet is listed in the Appendix B.

4.1 Initial SGCD Process Design

The initial fabrication process was designed from SUPREM simulations to create the SGCD structure which was described in Chapter 3. Some of the structure requirements include a poly field plate which has to be electrically conductive and must form an MOS type structure with the selective epitaxy with a negative flat band voltage (V_{FB}). The poly gate has to be electrically conductive, about 1μm thick after processing, and has to form an MOS type structure with a positive V_{FB}. In addition, all areas other than the seed holes should be covered with at least 1000Å of oxide before the SEG to prevent the creation of pinholes during the SEG process [37].

The SGCD fabrication process, depicted in Figure 4.1, starts with an oxidation to isolate the field plate poly from the substrate. A 20 minute 1000°C H_2 burn oxidation produced 1400Å of oxide, which was sufficient. Next, the field plate poly was deposited. This poly required a final minimum thickness of at least 0.1μm to be electrically conductive, while minimizing step heights which degrade the photolithography capabilities throughout the rest of the process. The deposited thickness was determined by simulating all of the subsequent oxidations which the poly was exposed to, multiplying the simulated oxide thickness by 0.44 to calculate the silicon thickness consumed by these oxidations, and adding to this 0.1μm. After the oxidations were simulated, the required poly thickness was estimated to be approximately 4000Å. The negative V_{FB} and low resistivity was achieved with an n-type implant of phosphorus at $3x10^{14}/cm^2$ and 35keV, for a doping density of approximately $7x10^{18}/cm^3$. The field plate poly was defined

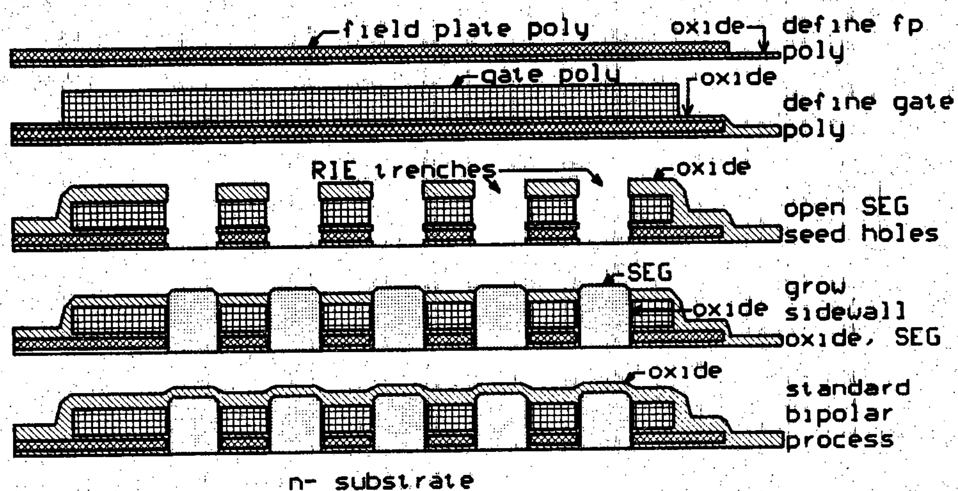


Figure 4.1. Fabrication sequence of SGCD main device area.

with mask level 1, and oxidized to provide isolation from the gate poly. A 20 minute 1000 °C H_2 burn oxidation produced about 1400Å of oxide.

The second poly deposition, for the poly gate, was next performed. The thickness of this poly was again calculated as above, except that the final desired thickness was 1.0μm. The required deposition thickness of the poly was estimated at about 1.3μm. A positive V_{FB} and low resistivity required a p-type implant of boron at 1x10^{15}/cm^2 and 35keV, which again produced a doping density of about 1x10^{19}/cm^3. The outdiffusion of the boron from the gate poly to the SEG sidewall was simulated using the SUPREM4 process simulation program [57]. The resultant dopant profile is shown in Figure 4.2, Due to limitations in the simulation program, many approximations had to be made. These included modeling the poly as single crystalline silicon, neglecting autodoping effects, modeling the epitaxial deposition as an instantaneous deposition, and substituting nitrogen for hydrogen during the epitaxial deposition. The effect of a surface channel at the sidewall interface would be to suppress the surface generation. The bulk generation rate would be unaffected, although variations in the sidewall oxide thickness produced during the RIE steps and the sidewall oxidation would produce variations in the boron concentration in a surface channel if it did exist. This effect would spread the gated response, making analysis of the defect densities difficult.

The gate poly was defined with mask level 2, and oxidized to prevent growth of the poly during the SEG step. A thick oxide of 1000Å or more was necessary to prevent pinholes from forming during the selective epitaxy [37]. A 2000Å oxide was specified to take into account local thinning which might occur during the RIE step. The as-grown oxide had to be thicker because it was be etched during the second RIE, which was used to remove the oxide, grown during the sidewall

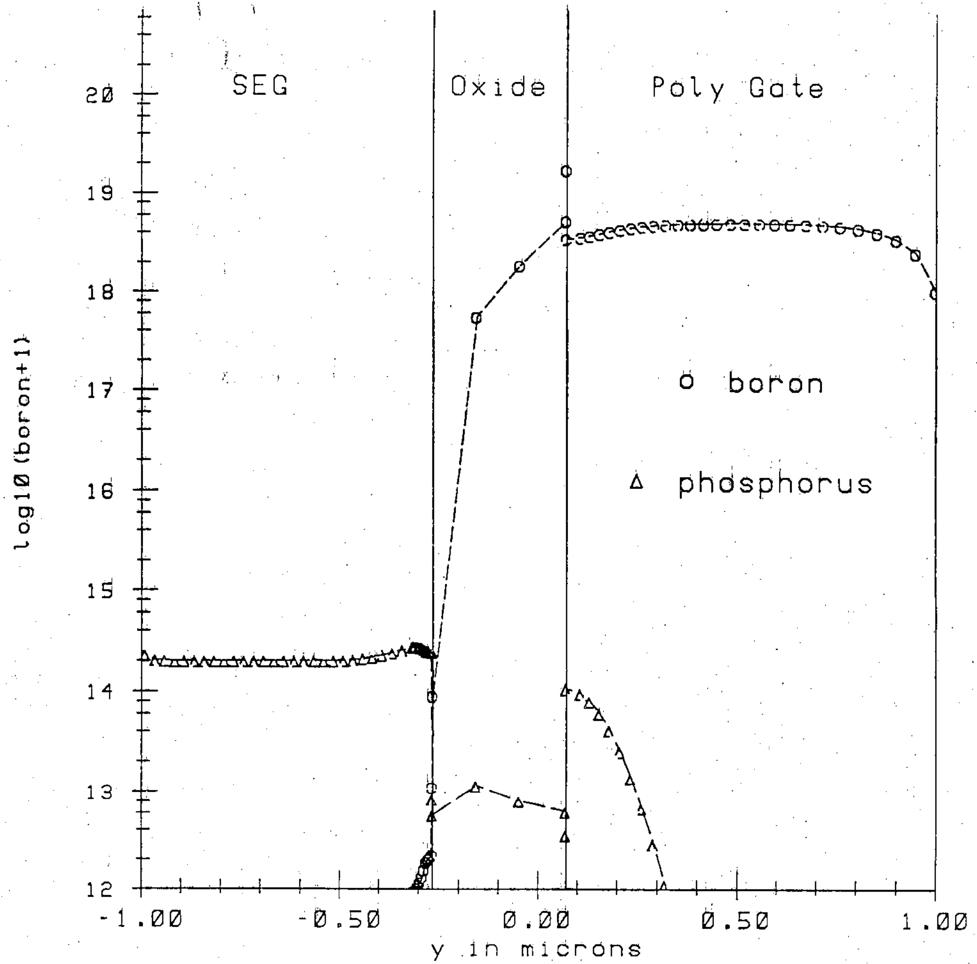


Figure 4.2. Boron diffusion into SEG through the sidewall from the gate poly simulated with SUPREM4.

oxidation, from the bottom of the seed hole. The sidewall oxide was specified as 2000Å, the same as the oxide on top of the gate poly, thus a 2500Å oxide etch is required for the second RIE to include a 500Å overetch. The 2000Å added to 2500Å sums up to a total oxide of 4500Å to be grown from the gate poly, which was accomplished with a 75 minute 1100°C H_2 burn oxidation.

The SEG seed holes were next defined with mask level 3 in photoresist, which was used as a mask for the RIE. The etch through the three oxide and two poly layers to the substrate must be an anisotropic etch, thus it was carried out in a parallel plate plasma etching system. After the etch, the resist mask was removed, and the exposed poly sidewalls in the SEG seed holes were oxidized with a 40 minute 1000°C H_2 burn oxidation to grow a 2000Å oxide. This oxide was intentionally grown twice as thick as the 1000Å required for pinhole prevention to take into account some sidewall oxide thinning during the second RIE. The second RIE was used to remove the oxide from the bottom of the SEG seed holes. The process to create the seed holes and the sidewall oxide is discussed in detail in section 4.2.

The SEG step consisted of a cleaning procedure and the deposition. The cleaning procedure taken from previous work began with a 1:1 H_2O_2:H_2SO_4 clean followed by a 10 second buffered HF etch to remove excess oxide from the seed hole. The clean continued in the epitaxial reactor with a 5 minute 60 slpm H_2 bake at 950° C and atmospheric pressure to remove the native oxide and a 30 second 1.5 slpm HCl etch in the H_2 carrier gas also at 950°C and atmospheric pressure to remove any damage or contamination from the top layer of the silicon in the seed holes. This cleaning procedure was used with buffered HF etched wafers but had not been tried with plasma etched wafers, so some development of the cleaning procedure was expected. The deposition was performed at 950°C

and 150T with 1.24 slpm HCl, 0.22 slpm SiH_2Cl_2 (DCS), and 60 slpm of H_2 as the carrier gas. These conditions yielded selective growth at approximately 0.2μm/minute. Although these conditions were sufficient for fabricating the SGCD, the accomplishment of the objective for this project required the evaluation of other SEG deposition parameters as well.

The rest of the process was a simple bipolar transistor process which was used to create the p-type diffusion for the junction diode and the n^+ diffusion needed to form a low resistance substrate contact. The process sequence started with a 20 minute 950 °C H_2 burn oxidation. Mask level 4 was used to define the photoresist mask for the p-type boron implant of $5x10^{13}/cm^2$ at 25 keV. The boron was driven and a thicker oxide was grown to mask the n-type implant with a 40 minute 950 °C H_2 burn oxidation. Mask level 5 was then used to define the oxide mask for the arsenic implant of $3x10^{15}/cm^2$ at 25keV. The arsenic was activated with a 40 minute 950 °C H_2 burn oxidation before contacts are defined with mask level 6 and the Al-1% Si metal was lifted off using photoresist defined with mask level 7. The metal was annealed at 400 °C in dry nitrogen before the wafer was diced and tested.

4.2 Process Development

4.2.1 CF_4 Plasma Etching

The preparation of a completely intact sidewall oxide was the most difficult element of the fabrication process. Initially, CF_4 gas mixtures [58,59] were used for both of the RIE steps. These mixtures did not produce highly anisotropic etches, and as a result portions of the poly layers were exposed before the SEG and therefore shorted to the SEG.

An attempt was made to find etches with the highest selectivity of both silicon over oxide and oxide over silicon, with the intention of switching between the two gas mixtures as the different layers were being etched. Etch trials were performed in a Technics PDIIA 40kHz parallel plate plasma etch/deposition system. The etch rate variation from run to run resulted from inconsistent gas flow control, nonuniform gas distribution, poor wafer temperature control, loading factors, and because the length of the etch was manually timed. The temperature control problem resulted from insufficient wafer cooling, which allowed the wafer temperature to increase as the etch proceeded, and also limited the power density which could be applied without baking the resist onto the wafer.

Various gas mixtures of CF_4, H_2, and N_2O were evaluated at various pressures and flow rates, giving the etch rates in Table 4.1. The etch rates were linearly proportional to power density. The rates also increased with increasing pressure, but not linearly. The selectivities approached 1:1 as the pressure was dropped, but no significant change in anisotropy was observed. The most selective silicon etch was $CF_4 + 15\%\ N_2O$ at 400mT and 150W with a silicon/oxide selectivity of 11:1, but the combination of $CF_4 + 12\%\ N_2O$ was used because of the lower resist etch rate. Many of the CF_4 and H_2 mixtures deposited a halocarbon film onto the wafer. The most selective oxide etch was $CF_4 + 25\%\ H_2$ at 400mT and 150W with an oxide/silicon selectivity of about 1:1. This combination frequently resulted in a halocarbon deposition in later trials, so the combination of $CF_4 + 90\%\ H_2$ was utilized with approximately the same etch rates.

Using $CF_4 + N_2O$ to etch the poly layers and $CF_4 + H_2$ to etch the oxide layers, with an intentional silicon overetch to undercut the oxide, the structure shown in Figure 4.3 was fabricated. This SGCD structure did not work because the oxide over the poly field plate was thinned during the second RIE, and ended

Table 4.1.
Plasma etch rates with CF_4 based gas mixtures in a parallel plate etching system.

Power (Watts)	Pressure (mTorr)	Gas flow rates (sccm)			Etch rates (Å/min)			
		CF_4	N_2O	H_2	Si	SiO_2	Si_3N_4	AZ 1350 Resist
250	400	50			500	125	475	325
150	100	7			325	100	325	600
150	400	55			320	80	340	240
50	400	60			100	40	200	133
250	400	48	4		1670	240	1300	730
250	400	45	6		2130	260	2270	1070
250	400	43	8		2600	290	2850	900
250	400	41	10		3300	290	3450	1300
150	400	47	8		770	no loading		
					250	loading=4 3" Si wafers		
					600	load=4 3" SiO_2 wafers		
150	400	55		5	110	57	210	400
150	400	50		10	100	48	170	100
250	400	50		15	120	73	260	130
250	400	47		25	73	94	350	0
250	400	38		35	dep	dep	100	dep
150	400	48		20	80	50	dep	dep
150	400	0		90	20	30	57	<30
250	400	56		10	125	105	180	75

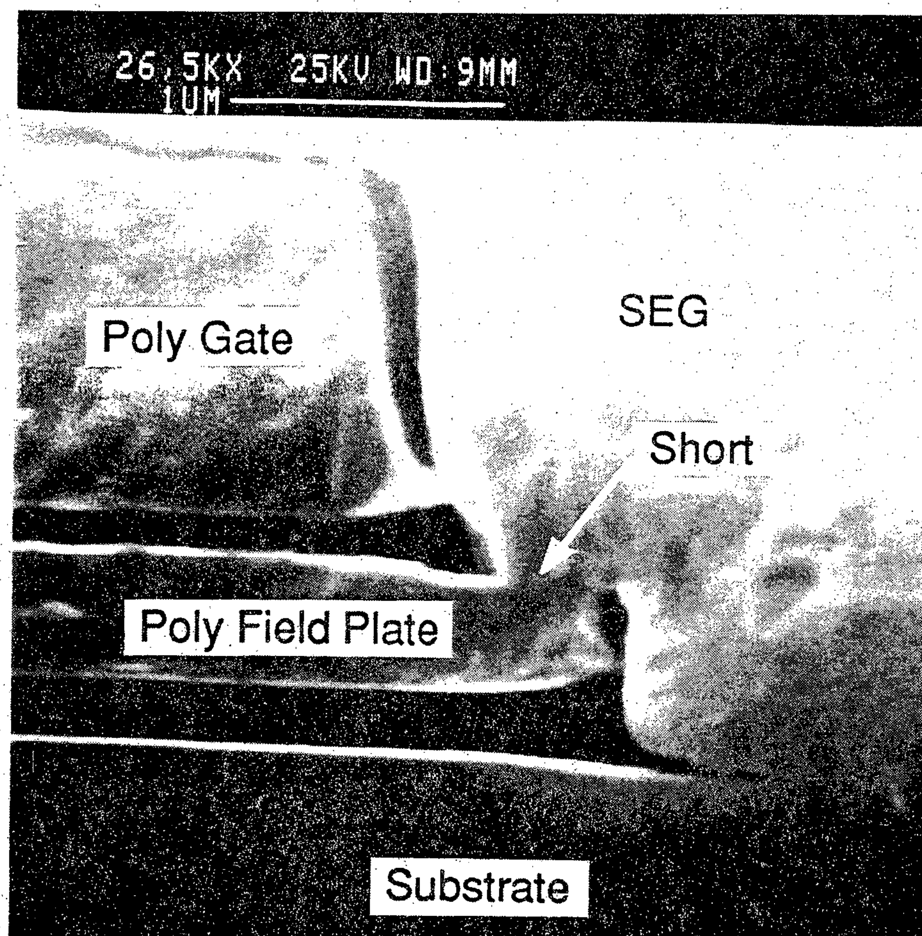


Figure 4.3. SEM of cross sectioned and HF etched SGCD structure produced with plasma etching using CF_4 gas mixtures.

up shorted to the SEG.

An attempt was also made to replace the oxide isolation around the poly with plasma deposited nitride to investigate the different plasma etch characteristics of the plasma nitride. These experiments were abandoned because the low strength and adhesion, and high thermal stresses in these films caused them to flake off while cooling down to room temperature from the deposition temperature of 250-300 ° C.

4.2.2 SF_6 and Freon 115 Plasma Etching

It was apparent that the CF_4 gas mixtures would not work, so new gasses were tried. The etching characteristics of Freon 115 (C_2ClF_5) and Sulfur Hexafluoride (SF_6) were next evaluated in a Drytek DRIE-100 13.56MHz parallel plate plasma etcher [60]. This system is equipped with six individual etch platforms, each with its own tuning network and gas distribution so that all six wafers can be etched at close to the same rate. The gas flows, system pressure, and etch times are all electronically controlled to provide better uniformity than the Technics system could provide. The wafers are also water cooled in this system and are kept at lower temperatures even with higher power densities.

The Freon 115 and SF_6 etch rates are given in Table 4.2. The Freon 115 provides a highly anisotropic etch with a vertical to lateral etch ratio of about 10:1 when etching monocrystalline silicon. It has a silicon/oxide selectivity of about 3.5:1, which is reasonably low compared to most etchants. A low selectivity is desirable when etching through the multiple poly and oxide layers so that a straight sidewall, with no steps, is created. The etch rates are slow, requiring a couple of hours to etch the seed hole, but the resist etch rate is also slow. Hence, the only problem with the etch rate is the time required. Depletion effects were

Table 4.2.
Plasma etch rates of SF_6 and Freon 115 in Drytek DRIE-100 parallel plate etch system.

Gas	Flow (sccm)	Pressure (mTorr)	Power (Watts)	Etch rates (Å/min)		
				Si	SiO_2	AZ 1350 Resist
SF_6	40	150	500	2000		400
C_2ClF_5	40	160	500	100	16	30
C_2ClF_5	40	160	800	160	25	65
C_2ClF_5	95	250	650	160	30	25
C_2ClF_5	95	250	750	320	90	60

observed with this etch, with the small seed holes and the edges of large (6mm x 6mm) seed windows etching faster than the central portions of the large seed windows. The etch rate across each wafer was consistent, with a total variation across a wafer of less than 1 percent. There was no noticeable correlation between the angular position of the wafer in relation to the gas flow and the etch uniformity.

The SF_6 etch is very different from the Freon 115 etch, with the SF_6 etch being isotropic, fast, and highly selective. The isotropy was demonstrated by overetching a 0.5μm poly film back 3μm under the photoresist mask. The selectivity of silicon over oxide and silicon over photoresist are both between 10:1 and 100:1, depending on the etch conditions and loading factors. These selectivities are more than sufficient for the etches used in this work. This etch exhibited different depletion effects than the Freon 115 etch, with the outside of the wafer etching faster than the inside of the wafer almost independent of the seed hole dimensions. As with the Freon 115 etching, the etch rate variation across a wafer was less than 1 percent.

The SF_6 and Freon 115 etches were immediately and successfully incorporated into the SGCD fabrication process. The SF_6 was used to define the poly layers with masks levels 1 and 2, and the Freon 115 was used for the two seed holes etches. Development of a useful anisotropic etch had been the major barrier to fabricating the SGCD.

The SF_6 etch was used for the poly etches because it was a dry etch. Previously, a wet etch was used which resulted in the lifting off of small geometries of photoresist due to poor adhesion. The dry SF_6 etch eliminated this problem.

The Freon 115 was used to etch seed holes in the oxide/poly/oxide/poly/oxide structure, and again to remove the oxide from the bottom of the seed hole which was grown during the sidewall oxidation. Although this structure looked much better (closer to vertical) when etched with the anisotropic Freon 115 etch, the slight etch selectivity still created a small step between the field plate poly and the gate poly. The oxide on this step would then get etched during the second RIE, exposing the field plate poly which shorted to the SEG during the epitaxial growth. In addition, the top seed edge of the gate poly was also exposed during the second RIE as shown in Figure 4.4, because the as developed resist was too thin at the edges. To alleviate these problems, an SF_6 etch was added near the end of the first RIE to etch back the poly layers $0.5\mu m$ from the edge of the seed hole. This finally eliminated the poly-SEG shorts, but created a small void at the top of the gate as is shown in Figure 4.5. Attempts to eliminate this void with shorter SF_6 etches and subsequently shorter etch back distances have resulted in shorts, apparently because of slight variations in etch rates and morphologies across the wafer.

The added SF_6 etch also resulted in a smoother surface if it was started while the Freon 115 was etching the field plate poly layer. Because the SF_6 has such a high selectivity, it leaves the original flat oxide surface at the bottom of the seed. The Freon 115 transfers the surface roughness of the poly layers down to the the etching surface as it etches. The roughness itself is not a problem when growing the epitaxy, but it does make removing all of the oxide from the surface difficult after it has been re-oxidized during the sidewall oxidation. The roughness creates some thicker regions of oxide which require too long to etch (because the oxide on the gate poly is also thinned) and forms defects when the epitaxy is grown. To help insure the removal of all of the oxide from the seed, the overetch

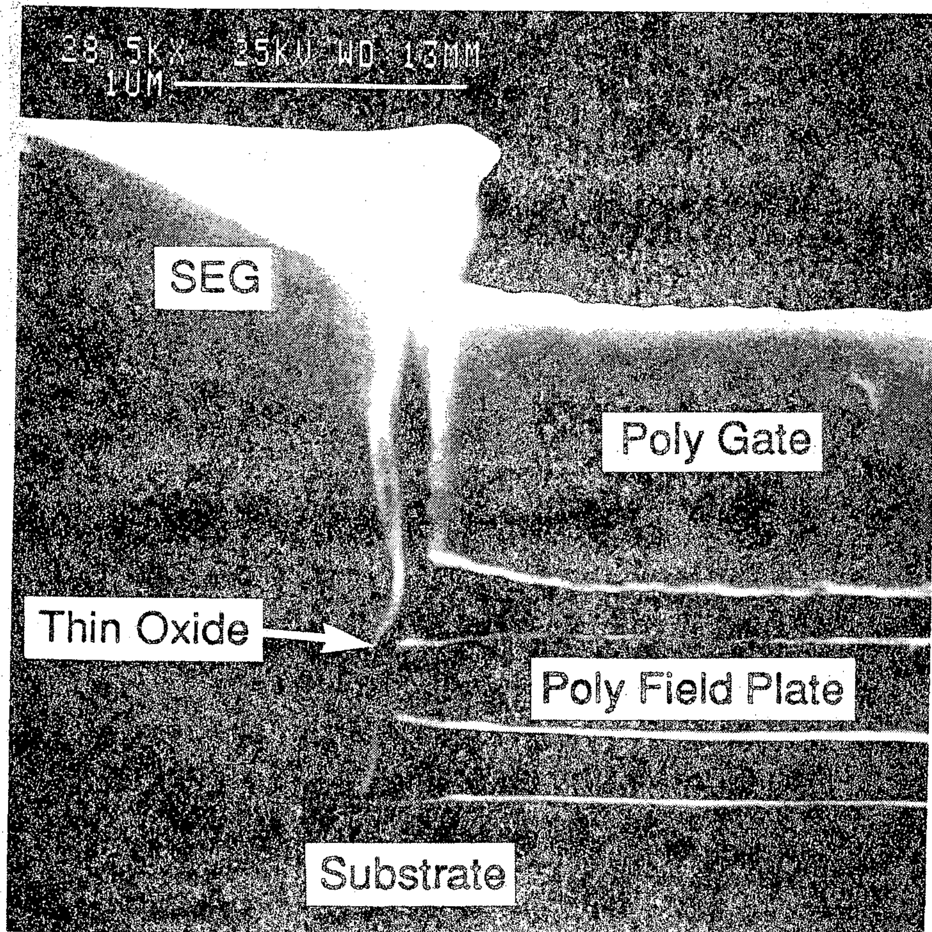


Figure 4.4. SEM of cross sectioned and HF etched SGCD structure showing field plate to SEG short resulting from fabrication of SGCD with no etch-back of the poly layers during the first RIE step.

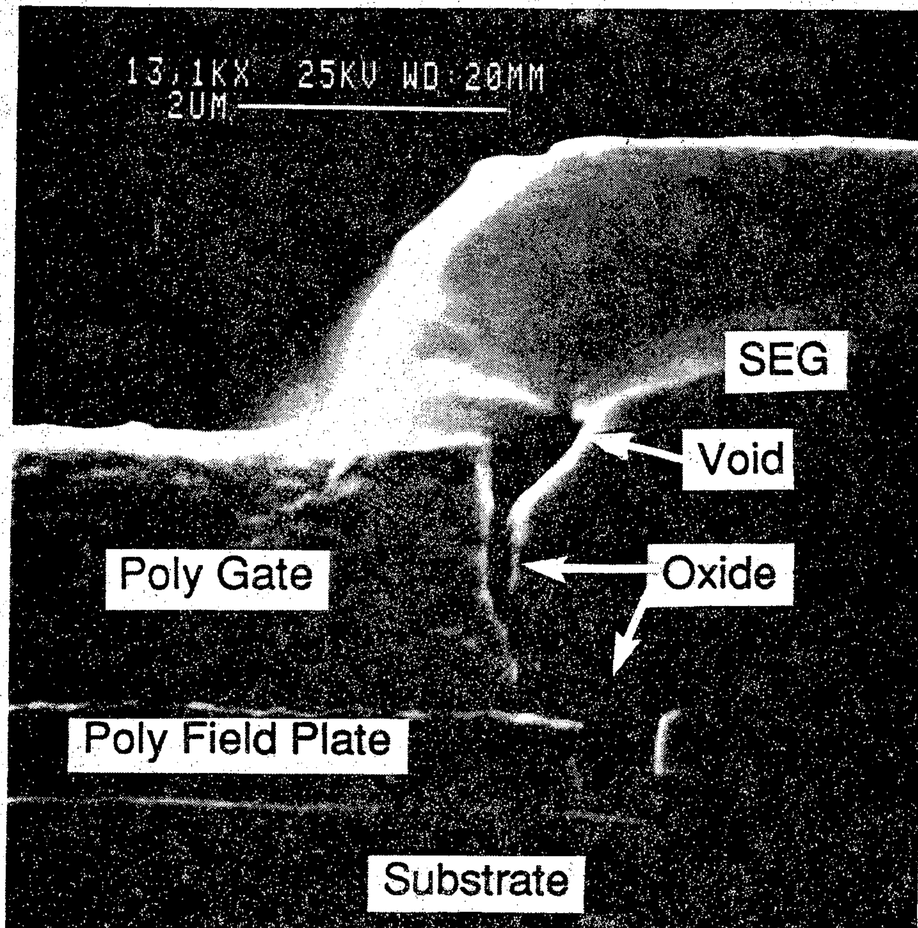


Figure 4.5. SEM of cross sectioned and HF etched SGCD structure showing void created with SF_6 poly etch-back technique.

on the second RIE was extended to 1500Å.

4.2.3 Seed Hole Development

The SEG grown in seed holes formed by Freon 115 RIE was compared to SEG grown in seed holes created with buffered HF etching in an 8000Å oxide layer. This evaluation was necessary because the SGCD would not be a viable tool for the quantification of the sidewall defect density if the defects it measured resulted from the fabrication process. Defects inherent to the SGCD fabrication would mask defects created by the SEG technique. The SEG used for these tests was grown for 20 minutes at 920 °C with 1.76slpm HCl and 0.44slpm DCS, resulting in 1.2μm of growth. The seed holes were etched with a 100 minute 750W Freon 115 RIE on wafer A, and a combination of a 50 minute Freon 115 etch and a 5 minute buffered HF etch on wafer B. The wafers were processed together for the rest of the walled diode fabrication process after the SEG step.

Reverse bias junction leakage currents (I_R) from walled diodes were measured at a bias of 3v, as shown in Table 4.3. It can be seen that the diodes in RIE etched seed holes exhibit slightly higher leakage currents than do the diodes in buffered HF etched seed holes. This difference is very small compared to the difference between walled diodes and planar diodes, thus the RIE etch was sufficient for fabrication of the SGCD. The reason for the higher leakage currents from the walled diodes with the RIE may be that etch residue is left on the sidewalls, or the higher leakage currents may result from the different oxide sidewall angles. Both of these wafers contained defects at the substrate interface, probably due residual oxide left after the epitaxial pre-clean (the BHF dip prior to the epitaxial deposition was omitted to preserve the sidewall conditions created by the RIE).

Table 4.3.
Median reverse bias junction leakage currents (I_R) from walled diodes fabricated in wells etched with Freon 115 RIE and buffered HF.

Wafer	Etch	I_R at -3v (nA)
A	Freon 115	1.65
B	Buffered HF	0.85

The SGCD seed hole sidewall oxide, formed after the initial RIE, was originally grown from the gate and field plate poly layers. This procedure resulted in a severe stress on the edges of these poly layers which deformed them in such a way that regions of thin oxide were created, as shown in Figure 4.6. To eliminate this problem, a new 750Å poly layer was conformally deposited on the wafers after the first RIE and oxidized entirely to form the sidewall oxide. This procedure also thickened the oxide on top of the gate poly, minimizing the probability of the second RIE thinning this oxide too much and resulting in the creation of pinholes during the epitaxial growth. The thickness of this poly layer was constrained by the fact that a thin layer would result in more stress on the poly and a thick layer might not get fully oxidized, thus forming shorts between the dielectrically isolated regions. A deposited oxide was avoided because the oxidized poly was thought to result in a higher breakdown voltage for the sidewall oxide. A low temperature (580 °C) poly deposition was used to minimize the leakage current through the oxide grown from this poly [61].

The 0.5μm field plate and 1.5μm gate poly layers created large steps on the wafer surface, which resulted in resist thinning at the edges of the steps. This thinned resist was etched through during the first RIE, and the underlying poly was exposed during the second RIE. The exposed poly then grew during the SEG step, forming shorts to the SEG at the edge of the seed hole. The use of a thicker resist (AZ1375) resolved this problem.

Another problem resulted from a poor edge profile of the resist. The gradual profile was slowly etched back during the first RIE, exposed the edge oxide to the plasma etch, and lead to the growth and shorting of the gate poly to the SEG during the epitaxial deposition. This problem was in part due to the fact that emulsion photoplate masks were being used. These emulsion plates did not have

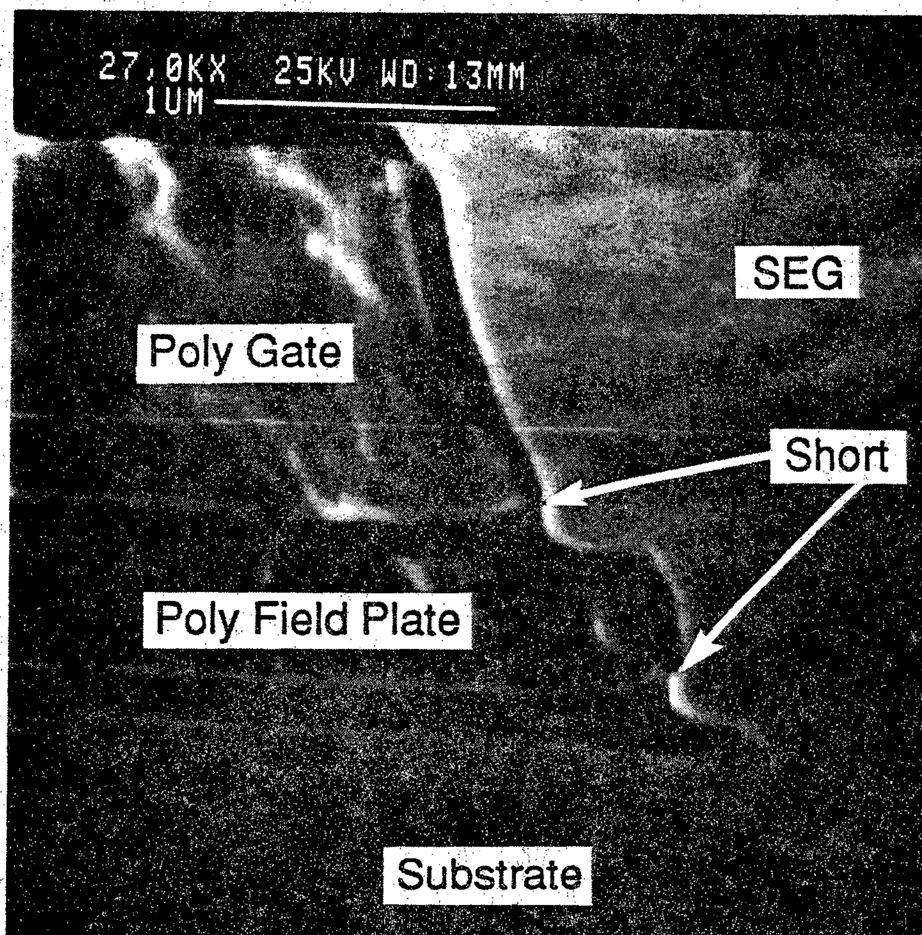


Figure 4.6. SEM of cross sectioned and HF etched SGCD showing oxide thinning resulting from stress created by growth (expansion) of the oxide under the poly layers.

a sharp light/dark transition, and thus resulted in a gradual slope at the edge of the resist. This problem was partially fixed by switching to chrome photoplate masks, which have a sharper light/dark transition and yield a better edge profile.

Finally, surface preparation was a problem on some of the seed holes etched through the oxide/poly/oxide/poly/oxide layers. Visual inspection of this surface after the RIE revealed a very rough surface. This was initially thought to be the source of the bulk defects, but a more careful process run revealed that the roughness in itself was not a problem during the epitaxial growth. However, if the surface was rough after the first RIE, then the oxide grown during the sidewall oxidation would also be rough. On the sides of the hillocks, the vertical oxide thickness, which had to be etched through, was much larger than the growth thickness of 2000Å. These locally thick regions of oxide required an excessive overetch to remove it, which resulted in excessive thinning of the oxide over the gate poly. The solution to this problem was underetching the initial RIE so that the original smooth thermal oxide substrate interface was left intact for the sidewall oxidation. This resulted in the growth of a much smoother oxide on the bottom of the seed hole, which could be removed entirely during the second RIE without excessively thinning the oxide over the gate poly. Additional preventative measures included changing the 500Å overetch during the second RIE to a 1500Å overetch. Also, the poly deposition pressures were lowered to deposit smoother poly layers. Lastly, the timing of the SF_6 undercut etch during the first RIE was adjusted to start before the Freon 115 etch reached the bottom of the field plate poly. The high selectivity of the SF_6 etch allowed the rough poly to be removed without etching the top of the smooth thermal substrate oxide under it, leaving a smooth surface for the start of the second Freon 115 etch of the first RIE sequence.

4.3 SEG Development

4.3.1 Epitaxy Pre-clean

The last step that the seed holes are exposed to before the SEG is the RIE step. The RIE process produces a dirty and damaged surface, which has to be cleaned and etched before the SEG so that low defect density material can be grown. A common procedure is to thermally oxidize the damaged layer and etch off the oxide with a buffered HF etch. However, this procedure thins the sidewall oxide too much because the buffered HF etch is too difficult to control. Thin regions in the oxide result in pinholes through the sidewall oxide as described earlier. Instead, a combination of a low temperature (400 ° C) oxidation to burn off the contaminants (halocarbon residues) [62], a 5 sec buffered HF etch to remove the thin oxide, and a 950 ° C in situ HCl vapor etch to remove the damaged layer was attempted.

Planar GCD (described in section 3.1) were built in large islands of SEG material grown with the HCl pre-clean etch to evaluate the effectiveness of this etch for removing the damaged layer. Carrier lifetimes estimated from the gated currents of these planar GCD were about 100μsec, which were the same as the lifetimes estimated from planar GCD fabricated in the substrate. The oxide grown at 400 ° C is only about 25Å, thus the damaged layer must be very thin, or the damage is annealed out during the high temperature 950 ° C H_2 bake before the epitaxial deposition.

4.3.2 SEG Bulk Quality

Bipolar transistors and planar GCD were fabricated in different materials to evaluate the bulk SEG quality. These tests were used to insure that the bulk qualities of the SEG would not affect the operation of the SGCD.

Bipolar transistors were fabricated simultaneously in substrate, single SEG, and double (interrupted growth) SEG material. The fabricated structures were designed to investigate the quality of SEG material up and beyond the level of its seed hole, as well as the quality of material grown on top of an already existing SEG. Since these devices were all made in the same wafer and die, with the same processing, they are used to compare the electrical quality of the SEG materials to that of the substrate. A test mask set was used to fabricate a set of three comparative transistors, all with similar dimensions and doping profiles, but all existing in different materials on the same wafer in the same die as illustrated in Figure 4.7.

The first device is a typical planar BJT fabricated in substrate material with no epitaxial layer or buried sub-collector. The second device is identical to the substrate device in all dimensions, except that its active base and emitter regions are located in an SEG island. Finally, the double SEG device is closest to the proposed ELO-BJT structure. After the first SEG is grown, it is oxidized and a seed window opened for growth of the second SEG. After the second growth, the active device regions are placed in the top (second) SEG island, and collector contact made to the first SEG layer.

Device structures were oriented along [100] directions on the <100> plane as this reduced perimeter defects and thereby increased material quality. Dimensions of the devices were made large ($60\times60\ \mu m^2$ emitter areas) so that bulk

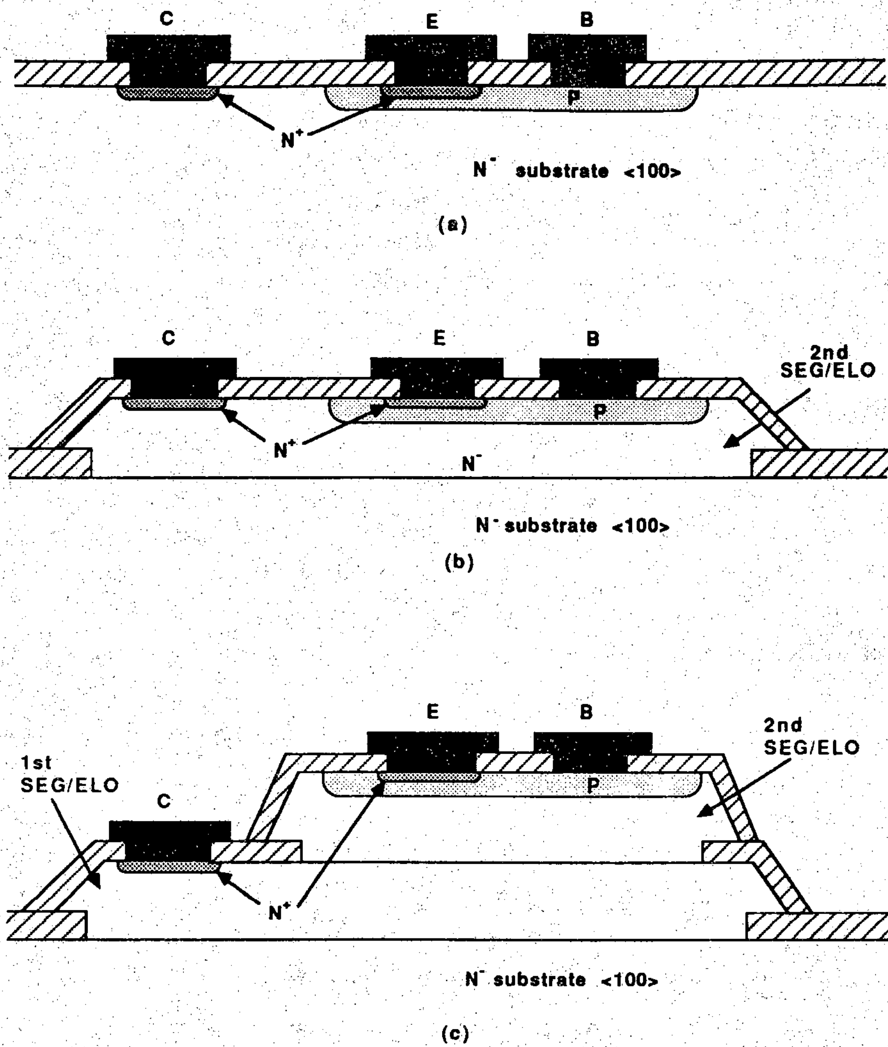


Figure 4.7. Cross sections of the three fabricated bipolar devices: (a) Substrate, (b) Single SEG, and (c) Double SEG.

effects could be studied without the complications of surface and perimeter effects. High speed devices were not an objective of this work.

N-type, 50-100 Ω-cm, <100>, silicon wafers were used as the starting material. The process began with 3100Å of thermal field oxide, into which seed holes were wet-etched for the first layer of the double SEG devices. A standard reduced pressure, pancake-type, RF heated epitaxial reactor was used. A cleaning cycle of five minutes of hydrogen bake and 30 seconds of HCL etch, both at 950 °C and atmospheric pressure, prepared the silicon for growth. SEG was then grown up from the substrate in the seed holes at 950 °C and 150 Torr, using dichlorosilane (DCS) as the silicon source, hydrogen chloride (HCL) to prevent nucleation, and hydrogen (H_2) as the carrier gas. Growth of 0.54 μm of ELO was obtained beyond the oxide seed window, both vertically and laterally, for a total height above the substrate interface of 0.85 μm. The small amount of ELO (0.54 μm) relative to the seed window size ($140 \times 280\ \mu m^2$) was the major difference between the fabricated and the proposed ELO-BJT devices [1].

After the first SEG growth, approximately 1800Å of thermal oxide was grown. Again, seed holes were wet-etched for the second layer of the double SEG devices and for the first layer of the single SEG devices, as shown in Figure 4.7. The second SEG was grown with the same parameters as the first. The nominal growth rate of approximately 0.1 μm per minute yielded 1.13 μm of total height above the second seed interface. All three types of devices simultaneously received the same base and emitter implants and drives. The base was implanted with boron at 25 keV and a dose of 3.0×10^{13} cm^{-2}, and wet-oxidized for 15 minutes at 1000 °C. The emitter was implanted with arsenic at 25 keV and a dose of 3.0×10^{15} cm^{-2}, with a final wet oxidation/drive of 20 minutes at 1000 °C. Finally, approximately 3000Å of aluminum-1% silicon alloy was sputter

deposited, defined, and annealed at 400 °C in dry nitrogen for 20 minutes.

The NPN doping profiles for the devices were obtained by spreading resistance profile (SRP), and determined to be nearly identical. The emitter doping, 10^{20} cm^{-3}, and junction depth, 0.12 μm, were similar to the values produced by simulating this process with SUPREM II. Base doping, 10^{17} cm^{-3}, and junction depth, 0.31 μm, as well as collector doping (4.5×10^{13} for substrate and single SEG, 2×10^{14} cm^{-3} for double SEG) were also determined from SRP data. The slight increase in collector doping of the double SEG device was probably due to the background intrinsic doping of the epitaxial reactor.

Following fabrication, the wafers were diced, mounted in packages, and bonded for testing. The packaged devices were mounted in a dark box test fixture, and tested using an HP 4145 Semiconductor Parameter Analyzer. Sixteen of each of the three types of devices were tested from each of two wafers in order to obtain an adequate sample size. Although yields were excellent from both wafers, the values reported here are from one single wafer to insure process similarity.

Base-collector and base-emitter junctions were tested separately for reverse and forward bias characteristics. It is important to note that initially neither junction was biased to breakdown, since breakdown has been shown to adversely affect junction/oxide interface quality [63]. Junction reverse bias leakage currents were measured at -3 volts, while a data analysis computer program extracted the forward bias junction ideality factor, η. The transistor was tested by measuring the forward DC current gain, β, over a range of collector currents with $V_{BC} = 0$ volts, while incrementing V_{BE} from 0 to 1 volt. The Early-voltage, V_A, was measured by extrapolation from the common emitter collector curves. After all other measurements were taken, the junction breakdown voltages were measured

on a few select devices. In addition, an HP 4140B pico-ammeter was used to verify the recombination region and reverse leakage currents.

Plots of the emitter-base junction current versus applied forward bias voltage are shown for all three devices in Figure 4.8. The slope of the forward bias curve determines the junction ideality factor, η, by the relationship,

$$I_{BE} = I_o \, e^{\frac{q V_{BE}}{\eta k T}} \tag{4.1}$$

where I_o is the saturation current, q is the electron charge, V_{BE} is the applied voltage, k is Boltzmann's constant, and T is temperature. An ideality factor, η equal to one indicates diffusion current domination over recombination current and exemplifies excellent material quality with low defect density. However, an ideality factor near two would indicate recombination current domination over diffusion current and would signal poor material quality with high defect density. At moderate forward bias voltages, average emitter-base junction ideality factors for all three devices were between 1.00 and 1.02 as listed in Table 4.4. The similarity between SEG and substrate values indicates excellent quality in the double SEG, single SEG, and substrate materials.

In order to determine material quality farther from the surface than the emitter-base junctions, the collector-base junctions were tested for forward bias characteristics as shown in Figure 4.9. Again, ideal regions (where $\eta \simeq 1.00$) were measured over four to five decades of diode current, with ideality factors ranging from 1.00 to 1.03 as listed in Table 4.4. Note that once again the three materials have very similar results.

In addition to junction ideality factors, minority carrier lifetimes in the three different materials were estimated using collector-base junction data [64]. Although the ideal region ($\eta \simeq 1.00$) was very clearly defined, the recombination

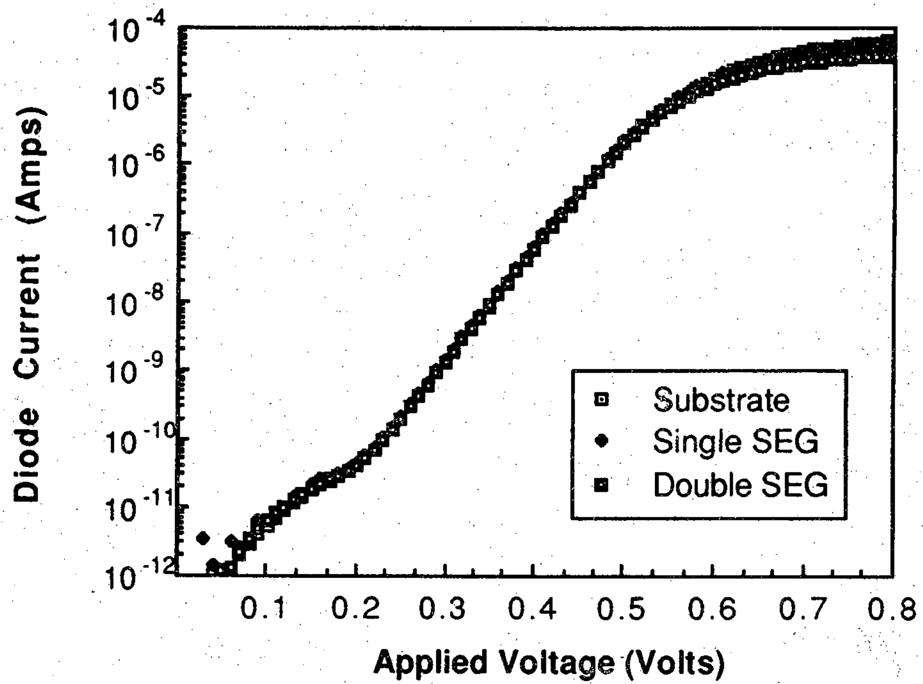


Figure 4.8. Forward bias base-emitter diode characteristics for three representative devices (area $= 3.6\times10^{-5}$ cm^2).

Table 4.4.
Summary of emitter-base and collector-base junction data averaged over approximately 16 fabricated devices in each group.

Type of Device	Emitter-Base Junction		Collector-Base Junction		
	η	Leakage Current ($\times 10^{-8}$ A/cm^2)	η	Leakage Current ($\times 10^{-8}$ A/cm^2)	τ (μsec)
Substrate	1.02	6.75	1.00	2.63	222
Single SEG	1.00	7.06	1.03	2.66	203
Double SEG	1.00	12.2	1.01	2.91	83.6

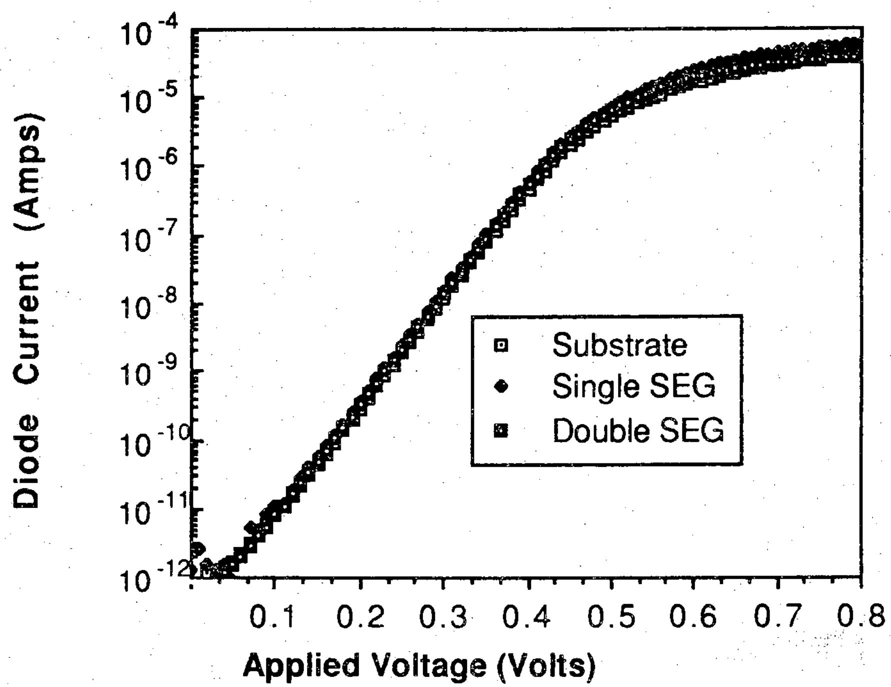


Figure 4.9. Forward bias base-collector diode characteristics for three representative devices (area $= 1.6\times10^{-4}$ cm^2).

current region ($\eta \simeq$ 2.00) predicted at small forward bias was very small. Because recombination current never became dominant in the total diode current, recombination region ideality factors were in the 1.08 to 1.12 range. However, recombination current density proportionality constants, J_{rec}, were still a useful means of comparing minority carrier lifetimes for similar devices.

Total diode current density in a non-ideal diode containing both diffusion current as well as recombination current is given by

$$J_{BC} = J_{diff}\, e^{\frac{q V_{BC}}{k T}} + J_{rec}\, e^{\frac{q V_{BC}}{2 k T}}, \tag{4.2}$$

where the first term on the right side represents the diffusion current component, and the second term is the recombination component. Typically, at small values of forward junction bias, recombination currents tend to dominate the diffusion currents in the total current density relationship, so that

$$J_{BC} \simeq J_{rec}\, e^{\frac{q V_{BC}}{2 k T}} \tag{4.3}$$

From space charge region considerations, the recombination current density can be approximated as,

$$J_{rec} = \frac{q\, n_i\, W}{2\, \tau} \tag{4.4}$$

so that the minority carrier lifetime can be calculated as,

$$\tau = \frac{q\, n_i\, W}{2\, J_{rec}} \tag{4.5}$$

Doping profiles determined by SRP were used to calculate the zero bias junction depletion widths. These values were combined with the experimentally determined recombination current density proportionality constants, J_{rec}, in equation 4.5 to produce effective carrier lifetimes in each of the three devices as listed in

Table 4.4. Substrate and single SEG lifetimes were similar and very high (222 and 203 μsec respectively). The lower lifetime of the double SEG (82.6 μsec) indicates slightly lower quality material, perhaps from defects generated at the growth interface. However, values from all devices were similar within a multiple of three, indicating relatively similar lifetimes in each of the materials.

The reverse leakage current densities, J_o, for the emitter-base junctions (measured at -3 volts) are listed in Table 4.4. Because of the difference in doping from base to emitter (10^{20} vs 10^{17} cm^{-3}), the base-emitter depletion region exists almost entirely in the base region ($W = 0.11$ μm calculated at zero bias). Although this region is near the emitter and its accompanying implant damage, current leakages for all devices were similar in magnitude, indicating similar material quality in all three devices.

Reverse leakage current densities for the base-collector junctions (also measured at -3 volts) were similar in all three devices, and smaller overall than base-emitter values as seen in Table 4.4. This is presumably because the base-collector depletion regions were farther from the emitter implant damage. Because of the extremely lightly doped collector (4.5×10^{13} to 2.0×10^{14} cm^{-3}), the depletion region extended entirely into the collector ($W = 4.29$ μm calculated at zero bias voltage). Although both device junctions were shallow ($x_{BE} = 0.12$ μm and $x_{BC} = 0.31$ μm), because of the depth of the collector-base depletion region, reverse leakage current densities indicate excellent material quality entirely through one or both SEG and into the substrate.

The three comparative bipolar transistors were fabricated on the same wafer, and designed as test structures with no lateral device isolation. The collectors of the devices were electrically connected through the n-type substrate.

As expected, large collector resistance due to low collector doping was found in all of the devices tested. However, as stated previously, these devices were designed to compare material and device quality, not for high frequency operation. Due to the relative doping of base to collector regions, average early voltages for all three devices ranged from 250 to 350 volts, indicating very little base width modulation. Junction breakdown voltages were also large as expected with $BV_{EB0} = -11.5$ volts and $BV_{CB0} = -90.0$ volts. In addition, collector to emitter breakdown was caused by avalanche and not punch-through. No evidence of piping, caused by increased diffusion of impurities near crystal dislocations, was observed in any of the devices.

The forward DC current gain, β, versus collector current, I_c, is plotted for three representative devices in Figure 4.10. The maximum gain of all three transistor types was very high (between 446 and 482), and are a final indication of the quality of the single and double SEG material relative to the substrate. It is important to note that, of all integrated circuit devices, the bipolar transistor is perhaps the most sensitive to material quality (defects, impurities, etc.). Differences in current gain between the devices were partly due to slight differences in impurity concentrations in the SEG and the substrate material, as well as the averaging of devices tested across the wafer. The quality of the devices is further seen in Figure 4.10 by the flatness of the gain curve over at least five decades of collector current. The sharp decrease in current gain near 10^{-4} Amps is a result of the large collector resistance of these test devices driving the device into saturation.

Finally, planar GCD data was evaluated to find the carrier lifetime in epitaxy grown with HCl and without HCl. This test was used to insure that the HCl gas was not introducing impurities into the SEG. Wafer A received SEG grown

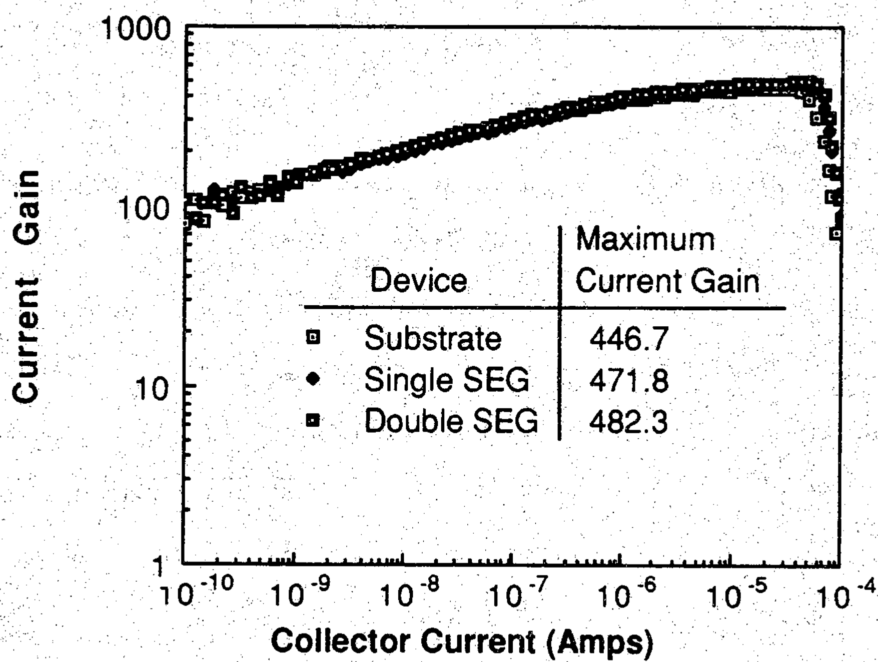


Figure 4.10. Comparison of current gain, β, versus collector current for three representative devices. The inset table lists averages of the maximum current gains of the fabricated devices.

at 920 ° C with 1.76slpm HCl and 0.44slpm DCS. Wafer B received epitaxy grown at 950 ° C with 0.06slpm DCS and no HCl. The wafers both received the same bipolar process after their epitaxial growths.

The lifetimes calculated from the planar GCD data are shown in Table 4.5. The HCl had no influence on the carrier lifetime, and thus is quite clean. Although the HCl was not thought to be the cause of the sidewall defects, this test insures that the SEG bulk material has the lowest defect density possible.

4.3.3 LPCVD Hot Wall Selective Epitaxy

Development work on LPCVD hot wall tube selective epitaxy was carried out with the intent of comparing the quality of the epitaxy from this system with the quality of the epitaxy from the cold wall reactor. The LPCVD hot wall epitaxy tube was modified from a LPCVD poly deposition tube to accommodate the higher temperatures required for epitaxy. The LPCVD system operates at low pressures of 0.1 - 10Torr, much lower than the cold wall epitaxy reactor. Secondly, the LPCVD system can be used to control the wafer temperature down to 400 ° C for slow cooling of the wafers as compared to only 650 ° C with the cold wall reactor. Finally, the LPCVD reactor can provide in situ oxidations to heal the SEG/oxide interface at the deposition temperature before cooling the wafers. An oxidation in the cold wall reactor would result in the burning of the graphite susceptor and would require extensive new plumbing. An additional benefit of the LPCVD system is that it can hold up to 50 wafers per run, many more than the cold wall reactors.

Results of test runs using mixtures of H_2, HCl, and DCS at 950 ° C are given in Table 4.6. Selectivity was achieved in some of the runs, but most of the runs resulted in rough bulk epitaxy with high defect densities. The low quality was

Table 4.5.
Carrier lifetimes calculated using planar GCD data from devices built in epitaxy (away from the sidewall region) grown with and without HCl introduced during the deposition.

		τ_0
Wafer A	No HCl	**90μsec**
Wafer B	HCl	**90μsec**

Table 4.6.
Results from 20 minute, 950 ° C LPCVD hot wall tube selective epitaxial depositions.

Flow rates (sccm)			Pressure	Growth Rate	Selective (at location)	
H_2	DCS	HCl	(mTorr)	(Å/min)	2'	3'
0	100	250	1000	-150		
0	100	50	385	0		
0	200	100	720	0		
0	200	50	600	0		
0	200	0	420	50		Yes
0	50	0	140	20	No	Yes
200	100	50	805	0		
200	100	10	700	20	No	Yes
200	200	0	810	100		No
400	50	10	985	20	Yes	Yes
400	40	5	950	40	Yes	Yes
400	40	0	870	60	No	Yes
400	20	0	835	40	No	Yes
600	60	0	1400	70	No	Yes
1000	100	30	2790	80	No	Yes
1000	100	20	2750	130*		Yes
1000	100	0	2570	100	No	Yes
1000	40	0	2370	30	No	Yes
* 60 minute deposition						

probably due to air leaks in the system, which resulted in excessive amounts of H_2O and O_2 in the system. This project was abandonded due to lack of time and money. Continued development of this system would be required to produce usable epitaxy.

4.4 Final Process Design

The final fabrication process starts with 50-100Ω—cm phosphorus doped (100) wafers which are oxidized (1400Å) before the first layer of poly (0.5μm) is deposited and doped n^+ with a $3x10^{14}/cm^2$ phosphorus ion implantation. This is the field plate poly and is defined with mask level 1. A second oxide of 1400Å is thermally grown on the field plate poly, after which the second (gate) poly layer of 1.5μm is deposited and doped p^+ with a $1x10^{15}/cm^2$ boron ion implantation. The gate poly is then defined with mask level 2, and a 5000Å thermal oxide grown on it. The initial seed hole is opened to the field plate poly through photoresist defined with mask level 3 using an anisotropic Freon 115 plasma etch in a 13.56 MHz parallel plate RIE system. This etch creates the vertical sidewalls required to prevent etching of the sidewall oxide during the next anisotropic RIE. The two poly layers are then purposely recessed approximately 0.5μm under the edges of the seed holes with an isotropic SF_6 plasma etch in the same system. This recess creates an oxide overhang which prevents the upper corners of the poly from being exposed during the sidewall oxide RIE. The seed hole etch is finished with a second Freon 115 etch to within 200Å of the substrate. A 750Å poly layer is next conformally deposited and completely oxidized to form the sidewall oxide without stressing the gate and field plate poly layers. A thick 2200Å oxide layer is grown, on the sidewalls and the bottom of the seed hole, and another anisotropic etch with Freon 115 is performed to remove this oxide from

the bottom of the seed holes, while leaving it intact on the sidewalls. The pre-epitaxy cleaning starts with a 400 ° C oxidation to remove any halocarbon residue left by the RIE, which is followed by an H_2O_2 and H_2SO_4 clean. In the epitaxial reactor, the pre-clean continues with a 5 minute 950 ° C, 150T, H_2 bake to remove the native oxide over the seed holes followed by a one minute 950 ° C, 150T, HCl silicon etch to remove any damaged silicon left by the RIE. SEG is grown n^- to 3.0μm, and the standard bipolar transistor process sequence to form the p-n junction and contacts is completed. Mask level 4 is used to define the photoresist implant mask for a 25keV 5x10^{13}/cm^2 boron base implant which is activated with a 20 minute 950 ° C wet oxidation to form the diode regions. Mask level 5 is used to define the oxide mask for the 25keV 3x10^{15}/cm^2 arsenic emitter implant, which is activated with another 20 minute 950 ° C wet oxidation to form low resistance substrate contacts. Mask level 6 is used to open the contact holes, and mask level 7 is used to define the photoresist for the metal lift-off. An SEM of a cross section of the finished SGCD is shown in Figure 4.5.

This process is much more complex than that required for planar diodes, walled SEG diodes, or planar GCD. It requires three additional photolithography steps, three poly depositions, and two anisotropic etches in addition to the SEG step. This complex design is justified because it will provide a good estimate of both the sidewall interface surface recombination velocity, S_0, and the lifetime, τ_0, near the sidewall for comparison with the bulk lifetime as estimated from an adjacent planar GCD also built in SEG.

CHAPTER 5 - RESULTS

We reported the first SGCD devices as fabricated using the above process [65]. In this chapter the successful operation of the SGCD is verified, and the SGCD is used to investigate the SEG/oxide sidewall interface. The tests used to verify the intended operation of the SGCD include an analysis of the structure, investigation of the gated response with normal operation of the SGCD, and an analysis of the field plates. The range of the SGCD data was compared to walled diode data. To demonstrate the use of the SGCD, the results of an evaluation of the effects of changing process parameters on the SEG/oxide sidewall interface defect density are presented in section 5.2. The effects of changing the deposition conditions of temperature, growth rate (HCl flow rate), and DCS flow rate are presented and discussed. An evaluation of post-deposition thermal cycles is included with the discussion of the effects of the process parameters. Finally, the consistency of the results is discussed, and the physical profile of the vertical sidewall interface is suggested as a mechanism responsible for many of the defects observed.

5.1 Verification

The SGCD consisted of a p-n junction diode and three dielectrically isolated conductors: the metal field plate, the poly gate, and the poly field plate. An SEM picture shown in Figure 4.4 revealed that the gate and the two field plates were located as designed. The oxide leakage currents through the SiO_2 dielectric

were measured at 15V with the other four terminals grounded. Typical oxide leakage currents are listed in Table 5.1. The poly-oxides exhibited the expected higher leakage currents and lower breakdown voltages than good thermal oxides grown from monocrystalline material. The sidewall poly-oxide next to the poly field plate and gate started to break down at approximately 20V. An observation of the beginning of this breakdown was used to verify that electrical contact had been made to the poly regions around the SEG.

The leakage currents are consistent from device to device and from run to run, indicating the oxides are of consistent quality. Of more importance, the leakage currents are low enough to not interfere with the operation of the SGCD. They also verify that shorts do not exist across the oxide regions. The existence of shorts (especially in the early devices) between the poly regions and the SEG was the leading cause of failure in the SGCD structure. These shorts interfered with the operation of the SGCD by changing the electric field distribution and current flows. They also indicated grain boundaries existed in the SEG near the sidewall. A short implies that holes existed in the poly-oxide before or during the SEG, and the poly grains thus grew epitaxially from these holes. Grain boundaries occur where the epitaxial and poly grain growths join. The existence of the diode was confirmed by observation of the I-V plot, and the breakdown voltage was measured to be approximately 10V.

An output plot from a typical SGCD device is shown in Figure 5.1, and a definite gated response was observed. This current was significantly larger than the gate dielectric leakage current and confirmed a gated response resulting from an extension of the depletion region from the diode along the length of the gate. The gradual gated response resulted from variations of the sidewall oxide thickness in the vertical direction and variations in the SEG doping resulting from

Table 5.1
Leakage currents of dielectrically isolated electrodes with bias of 15V to all other regions.

Electrode	Oxide Leakage
Metal Field Plate	20pA
Poly Field Plate	50pA
Poly Gate	45pA

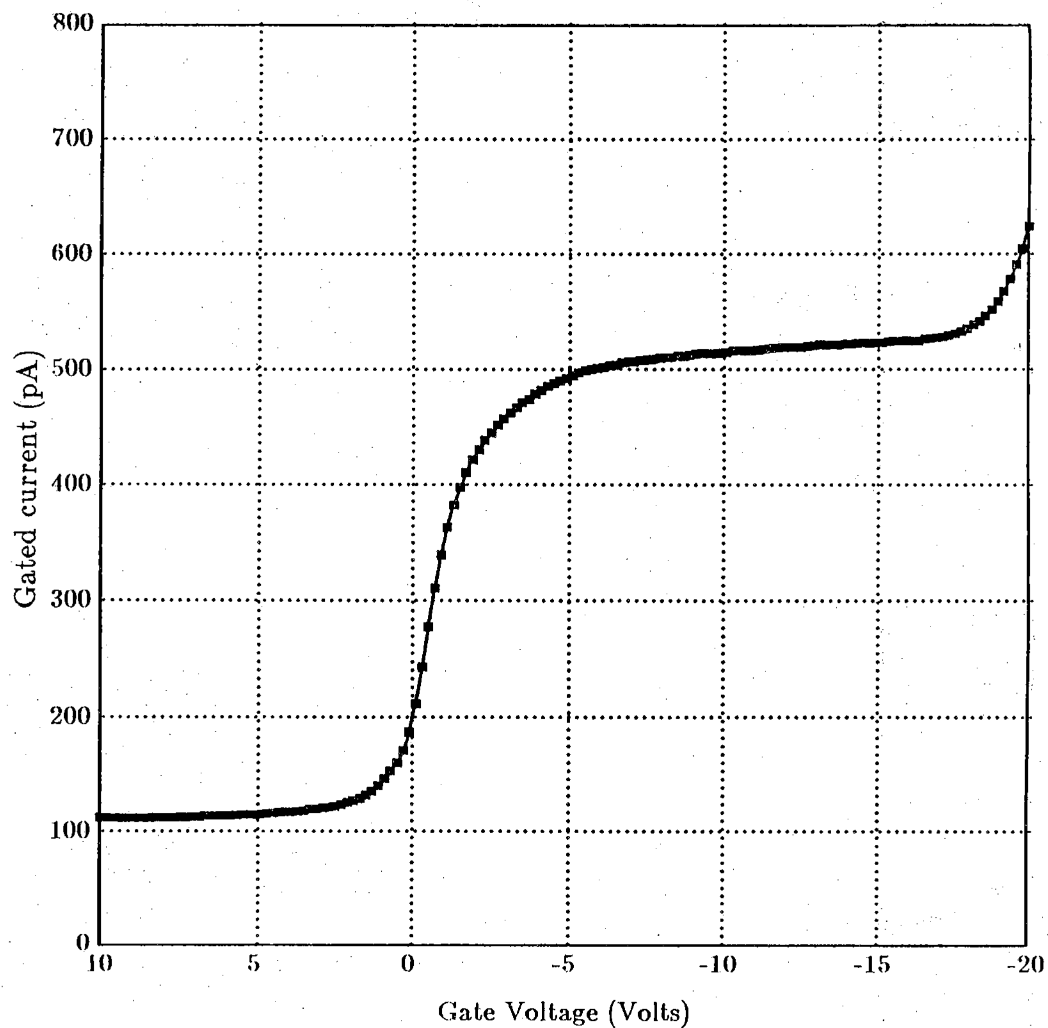


Figure 5.1. Data demonstrating the successful operation of the SGCD: diode current (I_D) versus gate voltage (V_g).

slight autodoping effects. The sidewall oxide thickness variation is inherent to the fabrication process resulting from different etch rates for silicon and SiO_2 during the initial RIE through the poly layers. The selectivity of this etch creates steps in the sidewall which are etched at different rates during the second RIE. These variations result in a range of flat-band and threshold voltages along the interface, and the spreading of the gated response.

Finally, the flat-band voltages of the metal and poly field plates were measured to insure that the surfaces adjacent to the field plates were not depleted. The flat-band voltage was recorded as the gate voltage at which the diode current begins to increase due to the transition from accumulation to depletion. For these tests, the gate and one of the field plate leads were interchanged before operating the SGCD as described above. The flat-band voltages were -4V for the metal field plate and -1V for the poly field plate. Both field plates biased the adjacent SEG regions into accumulation when they were grounded.

5.2 Initial Evaluation of SGCD Data

The SGCD data of Figure 5.1 was used to provide estimates of the surface recombination velocity and carrier lifetime near the SEG/oxide sidewall interface. The diode current did not fall off as the gated region changed from depletion to inversion indicating there was very little gated surface generation current. The surface recombination velocity, which is proportional to this gated current, is negligible compared to both the reverse bias junction leakage current and the gated bulk generation current. The recombination-generation rate at the interface is therefore insignificant when compared to the recombination-generation rate in the bulk epitaxy near the interface. If a poor interface is created during the epitaxial deposition, it is apparently healed during the oxidation steps after

the deposition. This result is consistent with the data previously published for the ELO/oxide interface [24], which was expected to be similar to the SEG silicon/oxide sidewall interface.

It is possible that a surface channel formed by boron atoms diffused from the gate poly into the SEG prevented the surface from being depleted as the gate bias relative to the substrate was decreased. The surface region would instead be depleted with positive gate voltages. Although positive gate voltages were evaluated, the gated response associated with surface depletion was never observed in the SGCD data. In addition, a surface channel of boron atoms would shift the flat-band voltage of the poly gate. This flat band voltage was nearly equal to zero volts. The difference between the flat-band voltage of the gate and the poly field plate results from the different doping densities in each of these poly layers.

To estimate the carrier lifetime near the sidewall, the gated area was calculated as $1000\mu m \times 1.3\mu m = 1300\mu m^2$. The resistivity was measured at approximately $50\Omega cm$ with a spreading resistance profile, corresponding to a dopant concentration of about $2 \times 10^{14}/cm^3$. With a potential of 0.1 volts applied across the diode, the depletion width extends about $3\mu m$ into the epitaxy. The near sidewall lifetime was estimated as 90ns from a gated bulk current component of 50pA. This was significantly lower than the bulk lifetime of close to $100\mu s$ for the same selective epitaxy as estimated from planar GCD data. The low near sidewall lifetime can account for the high perimeter junction leakage current observed in walled diodes.

5.3 Evaluation of the Effects of Varying Deposition Parameters on the Sidewall Interface Defect Density

The average (mean) gated currents of SGCD from individual wafers are plotted versus temperature, growth rate, HCl flow rate, DCS flow rate, and the HCl/DCS flow ratio in Figures 5.2-5.6 respectively. These results are from the wafers processed with the SEG depositions described in Table 5.2.

The mean gated current for the wafers with SEG grown at 920 °C is lower than the mean for the wafers with SEG grown at 950 °C. This result agrees with previously published results [7,20,22,27,32]. The implication from this result is either cooling from the lower temperature results in lower thermal stress, or the growth mechanism is temperature sensitive such that fewer defects are nucleated at lower growth temperatures.

The gated current plotted as a function of growth rate generally reveals lower gated currents are measured from lower growth rate SEG devices. This data might also explain the relationship with temperature observed in Figure 5.2 since the growth rate at the 950 °C SEG was higher than the growth rate of the 920 °C depositions. This is the first report of a correlation between the growth rate and the sidewall defect density. Such a correlation would imply the primary cause of the sidewall defects is related to a growth mechanism. The growth rate may also affect the sidewall bonding resulting in a change in the distribution of thermal stress as the wafer is cooled after the deposition.

There is no evidence of a correlation between the gated current and the HCl flow rate, DCS flow rate, or HCl/DCS flow ratio, as seen in Figures 5.4, 5.5, and 5.6 respectively. A correlation between the defect density and these parameters would indicate the defects are created by a growth induced mechanism. The

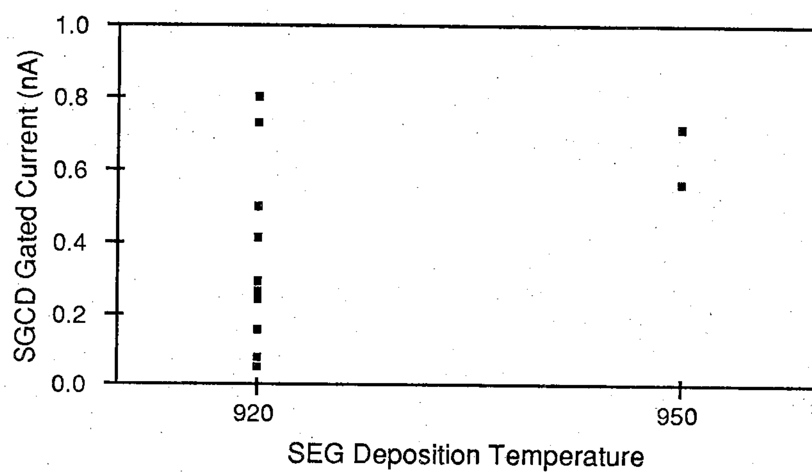


Figure 5.2. Mean gated bulk generation current of SGCD for each wafer versus deposition temperature.

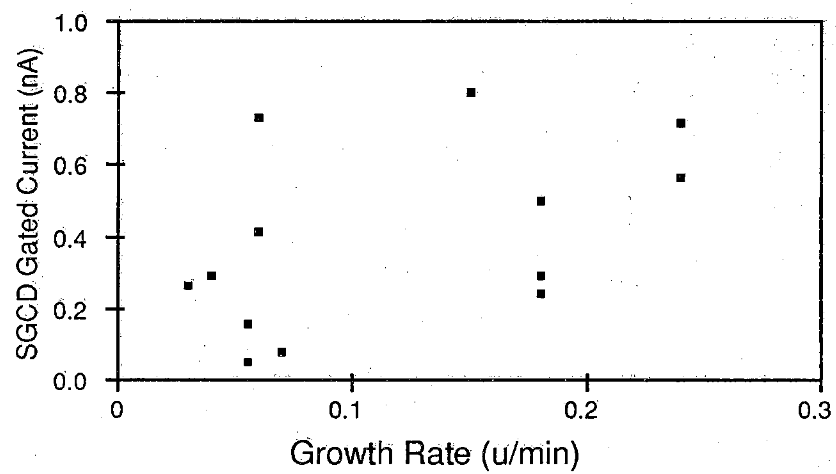


Figure 5.3. **Mean gated bulk generation current of SGCD for each wafer versus epitaxial growth rate.**

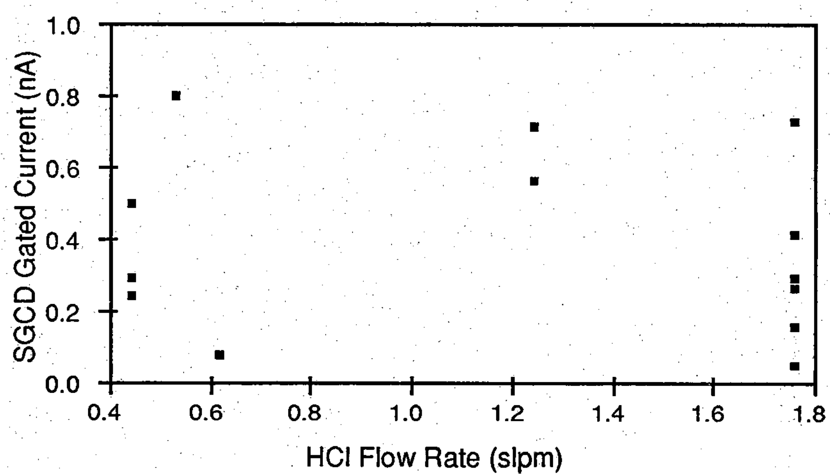


Figure 5.4. Mean gated bulk generation current of SGCD for each wafer versus HCl flow rate.

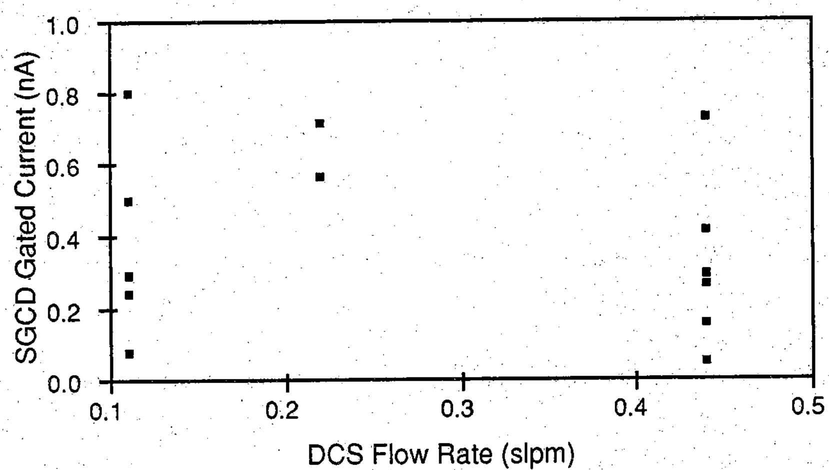


Figure 5.5. Mean gated bulk generation current of SGCD for each wafer versus DCS flow rate.

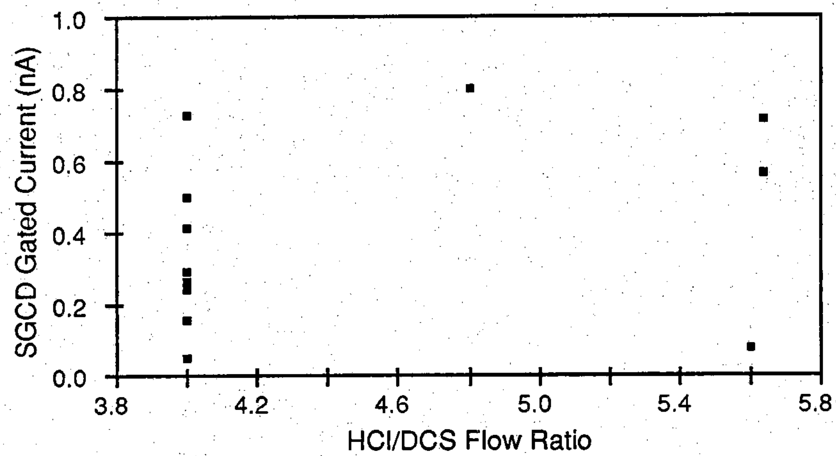


Figure 5.6. Mean gated bulk generation current of SGCD for each wafer versus HCl/DCS ratio.

Table 5.2
Mean gated bulk generation currents from SGCD and planar GCD and reverse bias leakage currents of planar diodes in SEG with the SEG deposition parameters.

Run #	Wafer ID	Time (min)	Pres (T)	Temp (°C)	Gas Flow Rate (slpm) H_2	HCl	DCS	Growth Rate (μ/min)	SGCD I_G (pA)	PGCD I_G (pA)	Planar Diode (pA)
247	16-14	4	150	950	60				565	0.2	1.0
	18-1	1	150	950	60	1.5			712	0.2	1.2
		30	150	950	60	1.24	0.22	0.19			
248	16-16	5	150	920	60				240	0.2	5.0
	18-2	1	150	920	60	1.5			500	0.2	20
	18-8	30	150	920	60	0.44	0.11	0.13	292	0.25	5.5
281	19-14	5	150	950	60				802	0.9	2.0
		1	150	950	60	1.5					
		60	150	920	60	0.528	0.11	0.148			
288	19-18	5	150	950	60				80	1.35	2.0
		1	150	950	60	1.5					
		45	150	920	60	0.616	0.11	0.068			
284	18-12	5	150	950	60						
	19-16	1	150	950	60	1.5			725	0.5	16
		60	150	920	60	1.76	0.44	0.057			
285	18-12	10	760	900	60				295	0.5	5.8
250	18-4	5	150	920	60				51	0.2	6.2
	18-10	1	150	920	60	1.5			156	0.2	17
		60	150	920	60	1.76	0.44	0.06			
		10	760	900	60						
282	19-15	5	150	950	60				265	0.5	1.7
		1	150	950	60	1.5					
		60	150	920	60	1.76	0.44	0.04			
		10	760	900	60						
		slow cool - 10 °C/min to 700 °C									

absence of a correlation should not be considered proof against a growth induced mechanism without further knowledge about the growth mechanism.

Both post deposition hydrogen annealing and slow cooling rates seem to reduce the gated current as shown in Figure 5.7. The lowest gated current was measured from a SGCD treated with an in-situ 10 minute atmospheric pressure hydrogen anneal at 900 ° C. This correlation was not found in any previous publication.

The intention of the in-situ anneal was to create an environment so that the SEG/oxide interface would either re-oxide or possibly heal itself by diffusion of atoms to the interface. The thermal stress would be then distributed over the entire surface and not confined to a few silicon-oxide bonds. Lowering the maximum stress seen by the silicon-oxide bonds was hoped to reduce the number of sidewall defects. By increasing the pressure from 150T to one atmosphere (740T), the H_2O and O_2 partial pressures are increased by a factor of 5. The maximum H_2O and O_2 partial pressures are desired to accommodate a higher temperature oxidizing anneal. The result would be a faster annealing rate for the interface due to higher diffusion rates. Previous experiments indicated 900 ° C and atmospheric pressure are close to the highest temperature oxidizing environment achievable in the epitaxial reactor at Purdue University. The slow cooling of the wafers was an attempt to reduce the effects of thermal stress by allowing the materials time to flow while cooling.

5.4. Vertical Sidewall Profile

There was a large variation in the gated currents measured from SGCD between wafers processed similarly, and this anomaly prompted further investigation into the cause of this variation. The variation is evident in the SGCD from

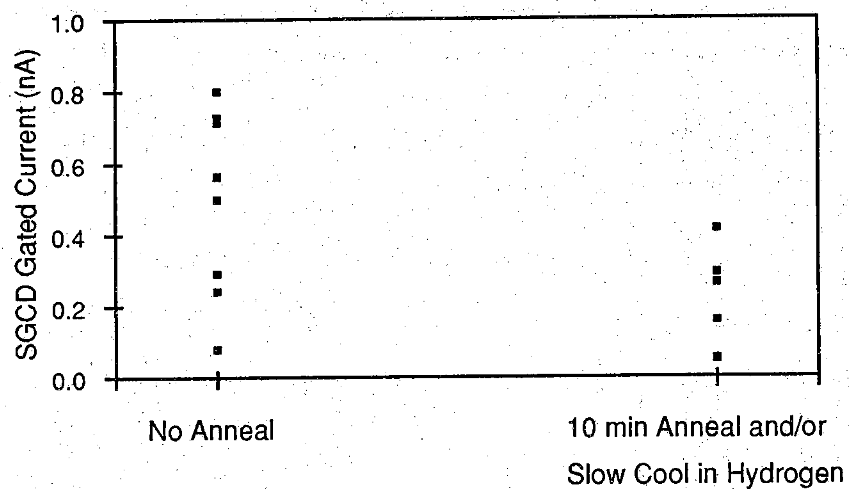


Figure 5.7. Mean gated bulk generation current of SGCD for each wafer with and without post-deposition anneals.

deposition runs 248, 281, and 288. In these particular runs, the gated current increased from the 250-500pA range to about 800pA and dropped to 80pA as the HCl flow rate increased from 0.44 slpm to 0.528 slpm to 0.616 slpm. All other deposition parameters were identical. There is also no direct relationship between the gated current values and the different deposition parameters as detected by observation of the plots in the Figures 5.2 through 5.7.

Additionally, different wafers receiving the same SEG deposition and processed together, with the exception of the RIE steps, showed a significant variation of gated currents from the SGCD. This was true with the group of wafers 18-2,8 and 16-16, with the results given in Table 5.3. These wafers were the largest group to receive selective epitaxy at the same time and had SGCD fabricated on them. This data eliminated the possibility of the defects being caused by a deposition parameter not measurable such as the water vapor partial pressure since these wafers received identical epitaxial depositions.

A large variation appeared between wafers processed in the same SEG deposition. Walled diode data was next studied to ascertain whether or not this phenomenon was unique to the SGCD. The walled diode data from wafers 18-2,8 and 16-16 are listed in Table 5.3. The substrate/oxide walled diode leakage currents were in the range of one to three times the leakage currents of the poly/oxide walled diodes. The oxides exposed on the sidewalls of the two types of walled diodes were grown from the deposited sidewall poly, and both were exposed to the second RIE step. The difference between the SGCD results and the poly/oxide walled diode results may be from the sensitivity of the walled diodes to enhanced dopant diffusion effects along the sidewall interface defects and the variations in the SEG height.

Table 5.3
Mean gated currents of SGCD and leakage currents of walled diode from wafers from run 248.

Wafer	SGCD (pA)	Walled Diode Poly/Poly-ox (nA)	Walled Diode Sub/Poly-ox (nA)
18-2	500	1.85	3.35
18-8	292	1.4	1.5
16-16	240	1.65	4.0

The leakage current variation and the higher leakage current (higher defect density) of the substrate/oxide walled diode compared to the poly/oxide walled diodes implies the sidewall defect density is a function of the physical sidewall profile. The SEM cross sections, shown in Figure 5.8, reveal considerable variation of the sidewall profile in structures located next to each other. This variation occurs during the sequence of defining the SEG seed hole.

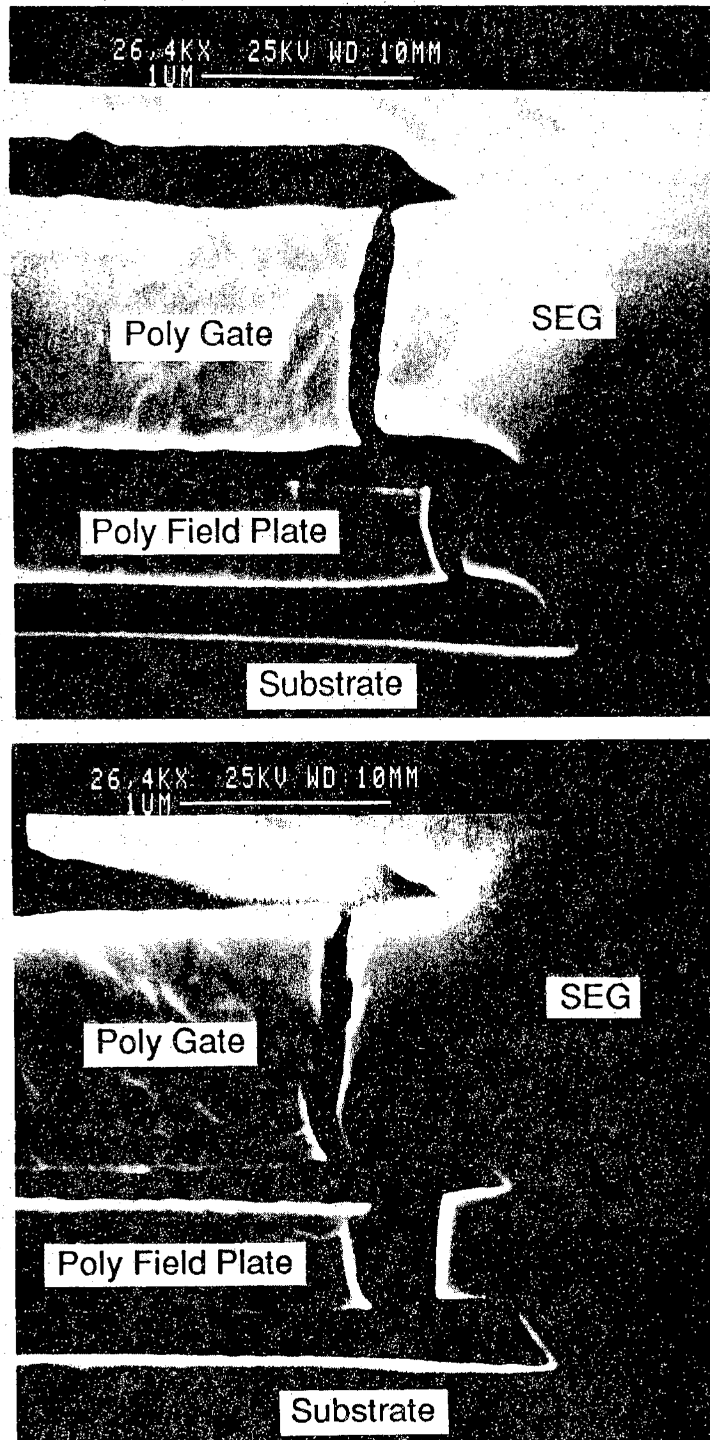


Figure 5.8. SEM of HF etched cross sectioned SGCD structures on same wafer.

CHAPTER 6 - SUMMARY AND RECOMMENDATIONS

It was shown that the SEG/oxide sidewall interface suffers from a high density of electrically active defects. These defects are generation-recombination centers which lead to high junction leakage currents in diodes located at or near the sidewall interface. The sidewall defects need to be reduced before many possible applications of SEG and its related technologies can be considered practical.

Walled diodes suffer from potential problems with enhanced dopant diffusion and variation in the height of the SEG from deposition to deposition. These problems make the walled diode a poor tool for comparing SEG/oxide sidewall interfaces produced under different conditions. In addition, walled diode data does not reveal the location of the defects. Two new devices, the sidewall capacitor and the Sidewall Gate Controlled Diode (SGCD), were presented as new tools for evaluating and comparing the sidewall defect densities of different SEG/oxide interfaces. The SGCD was shown to to be a better tool for the evaluation of this interface than either the walled diode or the sidewall capacitor.

The design and operation of the SGCD was presented in addition to the development of the fabrication process used to create this unique device structure. The fabrication process required the development of a new procedure to create a sidewall oxide for use as a dielectric between the gate and field plate electrodes and the SEG. This new procedure consisted of an anisotropic RIE and a thermal oxidation of a deposited poly layer. These steps were followed by a second an isotropic RIE.

SEM photographs and an evaluation of the oxides used to isolate the different electrodes revealed the SGCD structure was fabricated as designed. The change in diode current as the gate voltage was ramped indicated a clear gated response. With the addition of the field plate flat-band voltage analysis, the intended operation of the first reported SGCD was verified.

An analysis of the gated currents measured with the SGCD revealed the sidewall junction currents result from bulk defects in the silicon near the sidewall interface and not just from interfacial defects (dangling bonds) at the interface. Carrier lifetimes were estimated at 90ns near the sidewall in the SEG and were much shorter than the 100μs lifetime in the central region of the same SEG. The SGCD data had a significantly smaller range of values than walled diodes.

The usefulness of the SGCD was also demonstrated by distinguishing between different defect densities in different SEG. A study of the effects of various SEG deposition parameters determined that lower temperature, slower growth rate depositions, and in-situ hydrogen anneals produced the the lowest density of electrically active defects near the sidewall interface.

The effect of deposition temperature is confirmed in the published literature. However, the apparent effects of growth rate and post deposition anneals are new and were previously unpublished. Poor correlation between deposition parameters and the defect densities, and the variation of the defect densities of different wafers that had received the same SEG deposition, suggests many of the defects are not influenced by the deposition conditions. Instead, it is suggested the density of these defects is controlled by the vertical sidewall profile. Variations in the sidewall profile were observed by use of a SEM.

Continued work is necessary to investigate the effects of the sidewall profile and the sidewall surface on the sidewall defect density. The sidewall profile may be modified by reducing the pressure during the RIE steps or by the elimination of the SF_6 etch in the first RIE step. The sidewall surface may be modified by either using a deposited oxide or by coating the sidewall oxide with a polysilicon layer before the second RIE step. These steps are followed by the removal of this protective poly layer before the SEG deposition with a SF_6 etch. After an acceptable sidewall (one which is able to provide consistently low gated currents with the SGCD) has been found, the investigation of the effects of varying the growth parameters should continue.

Other promising areas of continued research include development of the hot-wall LPCVD selective epitaxial procedure, and an investigation into utilizing the SGCD structure for a side-gated vertical channel MOSFET.

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APPENDICES

Appendix A. PISCES Device Simulation Information.

```
file: in.init
Title Simulation of SGCD
$
$  Generate the mesh
$
option  plotdev=tekc
mesh rect nx=21 ny=21
x.mesh n=1 l=0.0
x.m n=3 l=2.85 r=.9
x.m n=5 l=3
x.m n=21 l=10 r=1.1
y.mesh n=1 l=0.0
y.mesh n=3 l=.15
y.mesh n=4 l=.3
y.mesh n=12 l=1.8
y.mesh n=14 l=1.95
y.mesh n=16 l=2.25
y.mesh n=18 l=2.4
y.m n=21 l=4
$
$ Define electrode and oxide regions
$
region num=1 ix.l=1 ix.h=3 iy.l=16 iy.h=18 oxide
region num=1 ix.l=1 ix.h=3 iy.l=12 iy.h=14 oxide
region num=1 ix.l=1 ix.h=3 iy.l=1 iy.h=4 oxide
region num=1 ix.l=3 ix.h=5 iy.l=1 iy.h=18 oxide
region num=1 ix.l=5 ix.h=21 iy.l=1 iy.h=3 oxide
region num=2 ix.l=5 ix.h=21 iy.l=3 iy.h=21 silicon
region num=2 ix.l=1 ix.h=5 iy.l=18 iy.h=21 silicon
region num=3 ix.l=1 ix.h=3 iy.l=14 iy.h=16 silicon
region num=4 ix.l=1 ix.h=3 iy.l=4 iy.h=12 silicon
$
$ Define electrodes:
$      1-pfp 2-gate     3-mfp     4-gnd
$
elec num=1 ix.l=1 ix.h=1 iy.l=14 iy.h=16
elec num=2 ix.l=1 ix.h=1 iy.l=4 iy.h=12
elec num=3 ix.l=1 ix.h=21 iy.l=1 iy.h=1
elec num=4 ix.l=21 ix.h=21 iy.l=3 iy.h=21
$
$ define the doping in the different regions
$
doping reg=2 n.type conc=2e14 uniform
doping reg=3 n.type conc=1e19 uniform
doping reg=4 p.type conc=1e19 uniform
$
contact num=3 aluminum
$
$ solve initial condition
```

```
$
symb newton.carr=2
method xnorm autonr
models temp=300 cons print
solve init
$
regrid potential step=.25
$
symb newton carr=2
method xnorm autonr
models temp=300 cons print
solve prev v1=0 v2=-.1 v3=0 v4=0
$
regrid potential step=.25 outf=msh.init
$
$ now perform the real solution:
$
symb newton carr=2
method xnorm autonr
models temp=300 cons print
solve prev v1=0 v2=-1 v3=0 v4=0 outf=slv.init
$
end
```

file: in.fp-gate-fp

```
Title Simulation of SGCD
$
$  Generate and plot the mesh
$
option  plotdev=ei3
mesh inf=msh.init
$
$ define the doping in the different regions
$
doping reg=2 n.type conc=1e14 uniform
doping reg=3 n.type conc=1e19 uniform
doping reg=4 p.type conc=1e19 uniform
$
contact num=3 aluminum
models temp=300 cons print
$
load inf=slv.init
$
$      1-pfp 2-gate       3-mfp        4-sub
$
symb newton carr=2
method xnorm autonr itlimit=20
solve prev v1=0 v2=-5 v3=0 v4=0 outf=slv.fp-gate-fp
$
end
```

Appendix B. SGCD Fabrication Process Run Sheet.

ELO BJT - Process Flow Sheet
Mask Set EBD.1; Process EBD.1
Wafer Set WAK19: SGCD
P. Schubert
Revised: W. Klaasen & J. Siekkinen
Latest: W. Klaasen 8/13/89

Date Step Completed

1) STARTING MATERIAL
* 3 inch n-type (phos) 50-100 Ohm-cm <100> with flat on <110>
\# Date process flow started: ____________
\# Lot ID #: ____________ #wafers: ______

2) FIELD OXIDE
* Oxidation in Tube #4 x__________
- 40 min H2 burn oxidation @ 1000 C
- H2 @ 90, O2 @ 60
\# Oxide color/thickness
Field: ______/______ (2300)

3) FIELD PLATE POLY
* Poly dep - 5000A x__________
- 2 hr, 50sccm SiH4, 200mT, 580C
\# Thickness: ____________

4) FIELD PLATE POLY IMPLANT
* Implant Phos @ 35keV, dose=3e14/cm2 x__________
- Implant with beamline pressure below 1e-6T
\# Beam Current:__________uA

5) FIELD PLATE POLY LITHOGRAPHY (EBD-1,lightfield)
- Lightfield! Flipped!
* Mask #1: x__________
\# AZ 1350 resist: 25sec @ 5k rpm; 20min @ 90C
\# Expose: 79sec, 300Watts; dev ___ sec, 4:1 DI:351
\# Bake 5 min @ 120C
* Etch poly with SF6 in DRIE-100 x__________
\# ___ min (1.5) #3; 500W (8.5), 40sccm SF6, 160mT
* Strip resist x__________
- Include piranha clean (2:1 H2SO4:H2O2) 10 min

6) FIELD PLATE POLY OXIDE
* Oxidation in Tube #4 x__________
- 20 min H2 burn oxidation @ 1000 C
- H2 @ 90, O2 @ 60
\# Oxide color/thickness
Field: ______/______ (3000)
Field plate: ______/______ (1400)

7) POLY GATE
 * Poly dep - 13000A (1.3u) x__________
 - 6 hour, 50sccm SiH_4, 200mT, 580C
 # Thickness: __________

8) GATE POLY IMPLANT
 * Implant Boron @ 35keV, dose=1e15/cm2 x__________
 - Implant with beamline pressure below 1e-6T
 # Beam Current:__________uA

9) GATE POLY LITHOGRAPHY (EBD-2,lightfield)
 - Lightfield! Flipped!
 * Mask #2 x__________
 # AZ 1350 resist: 25sec @ 5k rpm; 20min @ 90C
 # Expose: 79sec, 300Watts; dev ___ sec, 4:1 DI:351
 # Bake 5 min @ 120C
 * Etch poly with SF_6 in DRIE-100 x__________
 # ___ min (3) #3; 500W, 40sccm SF_6, 160mT
 * Strip resist x__________
 - Include piranha clean (2:1 H_2SO_4:H_2O_2) 10 min

10) GATE POLY OXIDE
 * Oxidation in Tube #4 x__________
 - 75 min H_2 burn oxidation @ 1100 C
 - H_2 @ 90, O_2 @ 60
 # Oxide color/thickness
 Field: ________/________ ()
 Field Plate: ________/________ ()
 Gate: ________/________ (6000A)

11) EPI SEED LITHOGRAPHY (EBD-3)
 * Mask #3: x__________
 # AZ 4620 resist: 40 sec @ 5k rpm; 30min @ 90C
 # Expose: 3min, 375Watts; overdev 50% ___(90) sec, 4:1 DI:351
 # Bake 5 min @ 120C

12) RIE - TRENCH
 * Drytek DRIE-100 system x__________
 # ___ min (125) #1; 750W (9.2), 95sccm 115, 260mT
 # ___ min (2:15) #3; 500W (8.5), 40sccm SF_6, 160mT
 # ___ min (23) #1; 750W, 95sccm 115, 260mT
 * remove resist with piranha clean (3:1) x__________

13A) SIDEWALL POLY DEP
 * Dry oxidation in Tube #2 x__________
 - 10 min @ 400 C
 * Poly dep: 12min 50sccm SiH_4 580C 190mT (600A) x__________

13) OXIDATION - SIDEWALL
 * Oxidation in Tube #4 x__________
 - 40 min H_2 burn oxidation @ 1000 C

- H2 @ 90, O2 @ 60
  # Oxide color/thickness
  Field: ________/________ (6167A)
  Field Plate: ________/________ (5860A)
  Gate: ________/________ (4896A)
  Seed holes: ________/________ (2100)

14) RIE - BOTTOM OXIDE
 * Drytek DRIE-100 system x__________
  # ____ min (45) #1; 750W (9.2), 95sccm 115, 260mT
 * Dry oxidation in Tube #2 x__________
  - 10 min oxidation @ 500 C

15) SELECTIVE EPITAXY
 * Submitted with monitor x__________
  - EPI PARAMETERS Target thickness: 3u
  # Date:______ Run:________ Program:________
  # Bake:____min ____H2, ____DCS, ____HCl; ____C; ____T
  # Etch:____min ____H2, ____DCS, ____HCl; ____C; ____T
  # Grow:____min ____H2, ____DCS, ____HCl; ____C; ____T
  # Epi Height:____________________ Oxide:________A

16) EPI OXIDE
 * Oxidation in Tube #4 x__________
  - 20 min H2 burn oxidation @ 950 C
  - H2 @ 90, O2 @ 60
  # Oxide color/thickness
  Field: ________/________ (3920A)
  Field Plate: ________/________ (3600A)
  Gate: ________/________ (2670A)
  Epi: ________/________ (860A)

17) BASE LITHOGRAPHY (EBD-4)
 * Mask #4: x__________
  # AZ 1350 resist: 25sec, 5k rpm; 20min @ 90C
  # Expose: 99sec, 300Watts; overdev 100% ____ sec, 5:1 DI:351
  # Bake 20 min @ 120C
 * Etch oxide in BHF until dewet x__________
  - Etch through field oxide ->or<- only 900A
  # Etch time: (50sec) ________________

18) BASE IMPLANT
 * Implant Boron @ 25 keV, dose=5.0E13 cm**-2 x__________
  - Implant with beamline pressure below 2e-6
  - Implant through resist - use beam current of 6uA
 * Strip resist x__________

19) BASE OXIDE
 * Piranha clean (1:1) x__________
 * Oxidation in Tube #4 x__________
  - 40 min H2 burn oxidation @ 950 C

- H2 @ 90, O2 @ 60
  # Oxide color/thickness
  Field: ________/________ (4770A)
  Field Plate: ________/________ (4600A)
  Gate: ________/________ (3670A)
  Epi: ________/________ (2205A)
  Base: ________/________ (1580A)

20) EMITTER LITHOGRAPHY (EBD-5)
* Mask #5: x__________
  # AZ 1350 resist: 25sec, 5k rpm; 20min @ 90C
  # Expose: 99sec, 300Watts; overdev 100% ___ sec, 5:1 DI:351
  # Bake 20 min @ 120C
* Etch oxide in BHF until dewet x__________
- Etch through field oxide
  # Etch time until dewet: (5 min) ________________
* Strip resist x__________
- Include piranha clean (2:1 H2SO4:H2O2) 10 min

21) EMITTER IMPLANT
* Implant Arsenic @ 25 keV, dose=3.0E15 cm**-2 x__________
- Implant with beamline pressure below 2e-6
  # Beam current:__________

22) EMITTER OXIDE
* Piranha clean (1:1) x__________
* Oxidation in Tube #4 x__________
- 40 min H2 burn oxidation @ 950 C
- H2 @ 90, O2 @ 60
  # Oxide color/thickness
  Field: ________/________ (5550A)
  Field Plate: ________/________ (5470A)
  Gate: ________/________ (4550A)
  Epi: ________/________ (3280A)
  Base: ________/________ (2770A)
  Emitter: ________/________ (2220A)

23) CONTACT LITHOGRAPHY (EBD-6)
* Mask #6: x__________
  # AZ 1350 resist: 25sec, 5k rpm; 20min @ 90C
  # Expose: 99sec, 300Watts; overdev 100% ___ sec, 5:1 DI:351
  # Bake 20 min @ 120C
* Etch oxide in BHF until dewet x__________
- Etch through base and emitter oxides
  # Etch time until dewet: (5 min) ________________
* Strip resist x__________
- Include piranha clean (1:1 H2SO4:H2O2) 10 min

24) METAL LITHOGRAPHY - LIFTOFF (EBD-7,Darkfield)
* Prebake 20 min @ 120C x__________
* Mask #7: x__________

AZ 1350 resist: 30sec, 3k rpm; 30min @ 90C
Expose: 99sec, 300Watts; overdev 50% 12 sec, 4:1 DI:351
Bake 20 min @ 120C

* BHF dip 5sec x____________
- Do not look for dewet
- Do not remove photoresist

25) METAL DEPOSITION
* Sputter deposit Al-1%Si x____________
- 20min, 100watts, 7mTorr
Metal thickness:____________________

26) LIFT-OFF
* Lift off metal with ace in ultrasonic cleaner x____________
- Rinse with ace, meth, di, and N2

27) METAL ANNEAL
* Anneal in Tube #8 x____________
- 20 min N2 @ 400C !
- Make sure furnace is down to 400C !

DATE PROCESS FLOW COMPLETED:____

Appendix C. SUPREM4 Process Simulation Information.

```
# SGCD Process Simulation
#
# Grid definition
#

line x loc=0 spacing=0.2 tag=left
line x loc=2 spacing=0.2 tag=right

line y loc=0 spac=0.02  tag=top
line y loc=1.0 spac=0.05 tag=bottom

region silicon xlo=left xhi=right ylo=top yhi=bottom

bound exposed xlo=left xhi=right ylo=top yhi=top
bound backside xlo=left xhi=right ylo=bottom yhi=bottom

initial orient=100 boron conc=5e18

# gate oxide
deposit silicon phosphor conc=2e14 thick=0.08 div=8
diffuse time=40 temp=1000 weto2

# Save the structure to a file
structure outf=2a.str

# SEG
diffuse time=10 temp=950 argon
deposit silicon thick=0.05 divisions=10 phos conc=2e14
deposit silicon thick=0.95 divisions=19 phos conc=2e14
diffuse time=10 temp=950 argon

# Save the structure to a file
structure outf=2b.str

# finish GCD
diffuse time=20 temp=950 weto2
diffuse time=40 temp=950 weto2
diffuse time=40 temp=950 weto2

# Save the structure to a file
structure outf=2c.str
```

VITA

William A. Klaasen was born August 19, 1962 in Grand Rapids, MI. He graduated from grade school, junior high school, and high school in Mount Prospect, IL. He received an award for excellence in mathematics while attending high school. He was married to Alynn Gentry on September 6, 1986.

He started college in 1980 at Purdue University, and graduated with a BSEE in December, 1983. As an undergraduate, he was active in the Eta Kappa Nu Honor Society, Phi Eta Sigma Freshman Honorary, Purdue Marching Band, and the Volleyball Pep Band.

He was accepted into the graduate program at Purdue University, and received the MSEE in December, 1985. His Masters' Thesis title was "Development of a tactile sensor." He integrated, into silicon, part of a tactile sensor for use with robotics. He also worked on poly-Si emitter bipolar transistors using recrystallized amorphous silicon. This work gave him experience with process design, as well as fabrication experience with: ion implanter; ion mill; diffusion furnaces; evaporators; r-f sputtering; LPCVD; mask aligners; and mask generation

In the fall of 1985, he was the teaching assistant for a graduate level IC fabrication laboratory course. The next year, he investigated poly-silicon emitter bipolar transistors fabricated with various types of recrystallized amorphous silicon emitters. While earning the PhD degree at Purdue University, he has worked with a group developing advanced bipolar transistor applications of SEG technologies.

His publications include:

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