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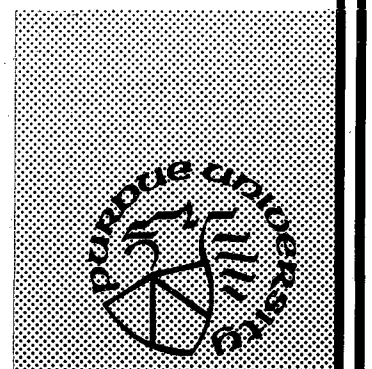

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ABSTRACT

Chen, Kai. MSEE, Purdue University, December 1989. Development of GaAs MODFET DCFL circuits and Process Technology. Major Professor: James A. Cooper, Jr.

The GaAs MODFET device is one of the prominent candidates for very high speed circuit applications. This thesis presents the MODFET DCFL inverter and other logic circuit design and process development. Working circuits of E/D type inverters, three-input NAND and NOR logic gates and ring oscillators are reported.

CHAPTER 1

INTRODUCTION

For more than three decades, silicon has been the dominant material for the semiconductor industry. But since the late 1950s, gallium arsenide (GaAs) has been considered a semiconductor with the potential to replace silicon because of the following properties of GaAs:

(1) the very high low-field electron mobility (six times that of Si [1]) which give GaAs the possible high-frequency performance;

(2) the large bandgap coupled with a short minority carrier lifetime which gives GaAs an advantage over Si in high-radiation environment;

(3) GaAs substrates grown with very high resistivities can be used as a dielectric medium for high-frequency microwave and millimeter-wave IC.

Since the early 1980's, a new promising transistor made of GaAs has been developed. This device is now known as the MOdulation-Doped Field Effect Transistor (MODFET), which held the record as the fastest logic switching device[2] since 1984 until a recently reported faster result made by a GaAs Heterojunction Bipolar Transistor (HBT).[3] Several other names such as the Selectively-Doped Heterojunction Transistor (SDHT), the High Electron Mobility Transistor (HEMT), the Two-Dimensional Electron Gas FET (TEGFET), have also been used for MODFET by different groups who have developed MODFET's. Excellent performance has been demonstrated by AlGaAs/GaAs MODFET's.

On the basis of the baseline of MODFET process fabrication technology developed by Mark Whiteside at Purdue, the purpose of this thesis is to present one way to build MODFET Enhancement-mode driver/Depletion-mode load (E/D type) inverters and other simple logic circuits such as three input NAND and NOR gates as well as ring oscillators. More complex MODFET circuits can be built by the design and process technology developed from this research.

1.1 MODFET Review

The MODFET device evolved from the work on AlGaAs/GaAs superlattices (thin alternating layers of differing materials sharing the same crystalline lattice) pioneered by Esaki and Tsu at IBM in the late 1960's.(4) It was predicted that high mobilities in GaAs could be accomplished if electrons were translated from the highly doped AlGaAs to an adjacent undoped GaAs layer, because of less Coulomb scattering, a process now known as modulation doping. The mobility enhancement behavior was first demonstrated by a single modulation doping heterojunction structure shown in Figure 1.1 in 1978, by Dingle, et al, of AT&T Bell Labs.(5) The electron layer confined on the GaAs side of the interface was proven to have a quasi two-dimensional character(6) and is referred to as a two-dimensional electron gas (2DEG). In 1980, the first MODFET device, shown in Fig. 1.2, was successfully fabricated by Fujitsu.(7) In 1986, the state-of-the-art devices with gate lengths of 0.1μm demonstrated transconductance (g_m) of 500ms/mm (77K), propagation delay (t_{pd}) of 12ps (300K), and maximum current density (J_{max}) of 500mA/mm.(8)

1.2 MODFET Overview

From Fig. 1.2, it is clear that because of the higher electron affinity of GaAs, the free electrons ionized from the donors in the wider band gap AlGaAs are transferred and confined in the undoped GaAs layer, forming the 2DEG conducting layer across the whole wafer. The advantage of this 2DEG layer is that the mobility of electrons in this layer is obviously higher than that of the bulk GaAs doped to a comparable level, as illustrated by Figure 1.3.(9)

Fig. 1.4 shows a typical cross sectional diagram of a MODFET, which is similar to a Si MOSFET in drain/gate/source structure. The gate, which modulates the 2DEG channel that is normally hundreds of angstroms below the gate, is a metal-semiconductor Schottky barrier junction. The channel is modulated by the gate voltage, which changes the depth of the depletion region of the Schottky barrier into the semiconductor. The device will be shut off when the gate voltage is negative enough so that the depletion region extends into the 2DEG, eliminating the conducting channel between the drain and the source.

Similar to the Si MOSFET, there are two types of MODFET, enhancement-mode and depletion-mode devices. The enhancement-mode is a normally-off device, which means the conducting channel is cut off when the gate is zero biased. This mode is built with a smaller gate-to-channel separation than the zero-bias depletion width of the gate Schottky

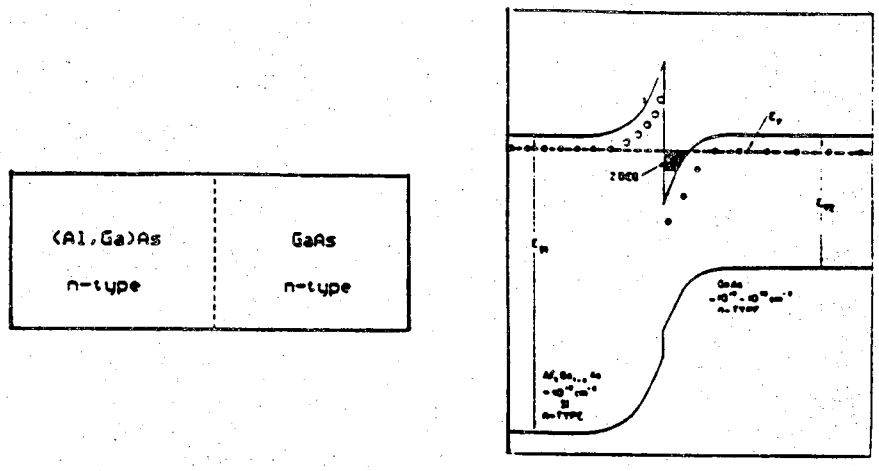


Figure 1.1 The heterostructure and its energy band diagram.(5)

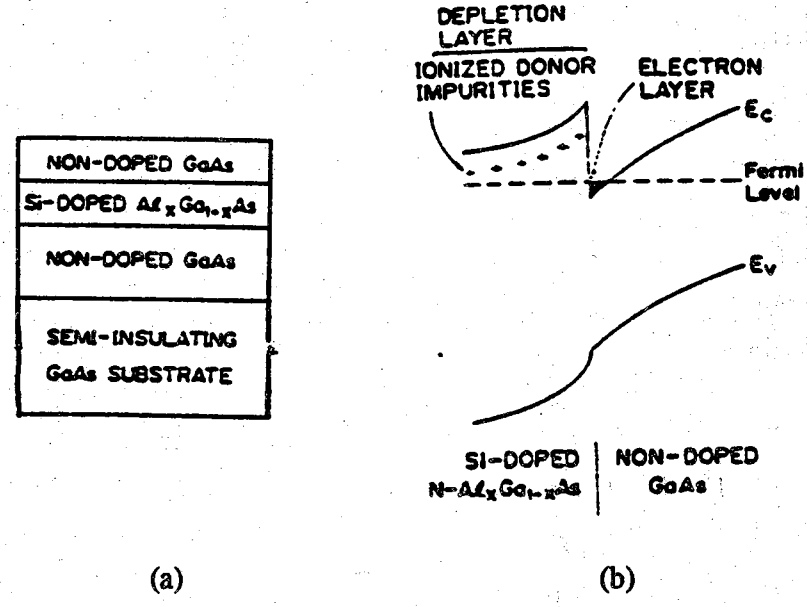


Figure 1.2. (a) The MODFET heterojunction and, (b) its energy band diagram .(7)

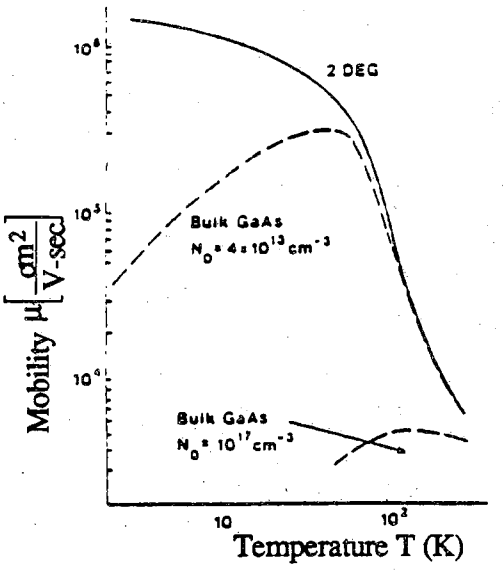


Figure 1.3 The 2DEG and bulk GaAs carrier mobilities vs. temperatures.(9)

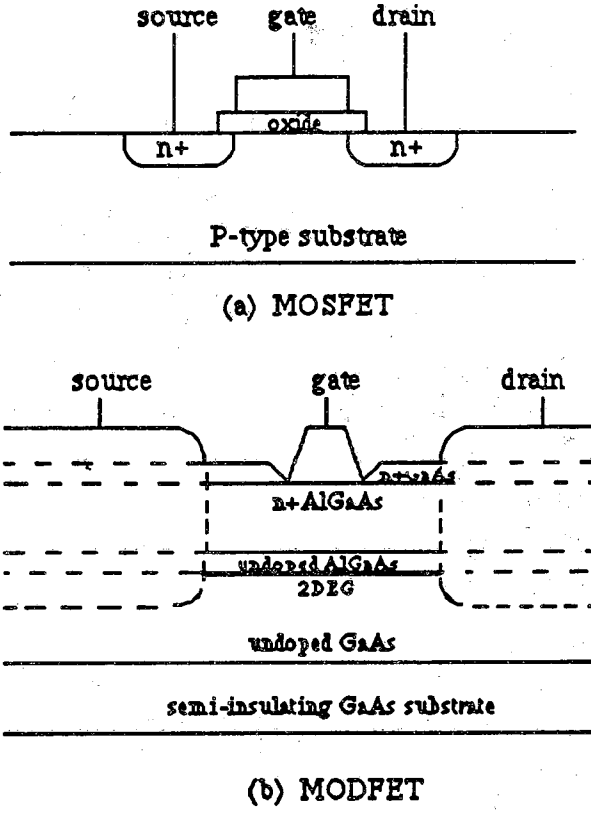


Figure 1.4 (a) Si MOSFET and, (b) GaAs MODFET.

barrier. The other type is the depletion-mode, which is a normally-on device. It is built with a larger gate-to-channel separation than the zero-bias depletion width of the gate Schottky barrier.

Similar to CMOS in silicon, a complementary MODFET technology, that is a p-MODFET coupled with an n-MODFET can be of interest at temperatures below 77K[10]. Below this temperature, the mobility of holes in the two-dimensional hole gas (2DHG), formed in undoped GaAs when the AlGaAs is p-doped, is on the same order as the electron mobility in bulk GaAs.

Recently, new interest has arisen in pseudomorphic MODFET's, in which a mismatched lattice layer of (In,Ga)As is grown between the (Al,Ga)As spacer and the undoped GaAs layer. The 2DEG is thus formed in this newly included (In,Ga)As layer. In 1989, the devices of this structure with 0.2μm gate length exhibited a maximum channel current (I_{max}) of 550mA/mm, peak transconductance (g_m) of 550ms/mm, and peak current gain cutoff frequency (f_T) of 122 GHZ[11]. Transconductance as high as 930ms/mm at 300K was also reported[12].

1.3 MODFET Circuit Implementation

The universally used MODFET circuit type is the direct coupled FET logic (DCFL, Fig. 1.5 (a)). Its prominent advantages are:

(1) the basic DCFL circuit has the simpler (minimal number of two transistors) inverter gate than the buffered FET logic (BFL, Figure 1.5 (b));

(2) E/D type DCFL circuit consumes less power than the depletion driver circuit;

(3) from circuit design point of view, DCFL is very attractive since its enhancement-mode driver (E-driver) results in a direct-coupled scheme identical to that employed in silicon MOS circuitry.

A big disadvantage of DCFL is that it is very sensitive to the threshold voltage. The control of the threshold voltage across the wafer is a major challenge to build a working MODFET circuit with DCFL. A control of threshold voltage better than 30mV across the wafer is equivalent to a control of gate recess etching of better than 10Å --- a very difficult prescription to fill.[13] This will be discussed later in the chapter on process development.

The first circuit manifestations of high speed, low power capabilities of MODFET applications, a ring oscillator with 27-stages and DCFL configuration, was reported in 1981 by Fujitsu.[14] Since then, impressive improvements have been achieved.[15] In 1986, a switching time of 5.8 ps/stage at 77K was achieved with 0.35μm gate length

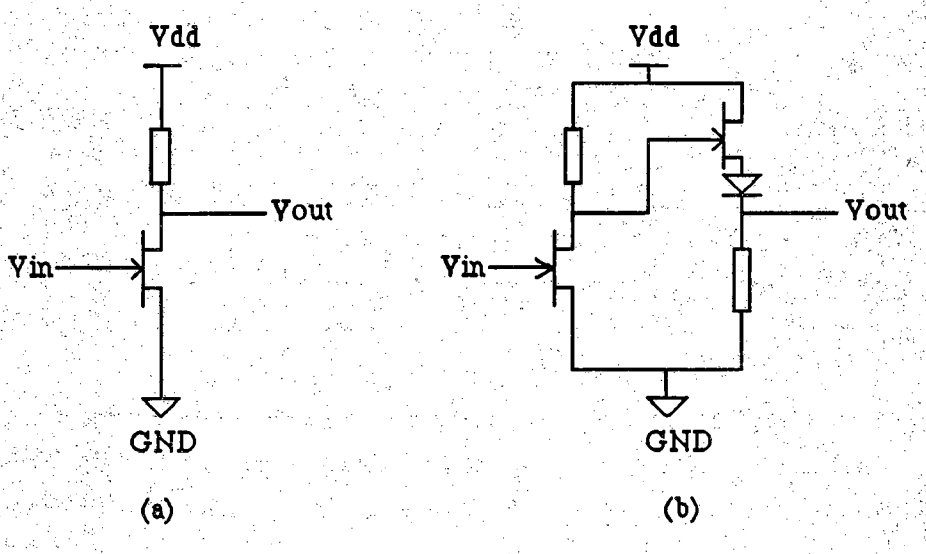


Figure 1.5 (a) Direct-coupled FET logic and, (b) buffered FET logic.

devices[16]. This is the fastest FET ring oscillator switching speed ever reported.

With the use of MODFET NOR logic gates, a high-frequency divider, another application of DCFL circuits, can be built using D flip-flops. The results of such a circuit with device gate length of 1 μm were first reported by Kiehl et al [17] in 1983. A maximum operating frequency of 3.7 GHz at 300 K (30 mW total power with 1.3V bias) and 5.9 GHz at 77K (19mW total power with 1.4V bias) were demonstrated.

The first MODFET static RAM (4-bit) with 1-μm gate lengths was built in 1984[18]. In the same year, a 4-kbit MODFET SRAM with a typical access time of 2ns was successfully built[19]. This was also the fastest access time ever reported for a 4-kbit SRAM up to then. In 1987, a 1-kbit MODFET SRAM with access time of 0.6ns was achieved[20].

In 1986, a self-aligned gate superlattice AlGaAs/n+ GaAs MODFET 5x5-bit parallel multiplier with multiplication times of 1.80ns at 300K (power dissipation of 0.43mW/gate) and 1.08ns at 77K (power dissipation of 0.75mW/gate), using DCFL circuits, was reported[21].

In microwave applications, extremely impressive results have been shown by MODFETs as compared to GaAs MESFETs. Table 1.1 [8] shows some data for this

Table 1.1. Comparison of MODFET and MESFET microwave figures.[8]

PARAMETERS	MODFET			MESFET
Gate length L (μm)	0.35	0.50	1.0	1.0
Transconductances g_m (ms/mm)	230	235	140	100
Current-gain cutoff frequency f_T(GHz)	47	35	18	14
Power-gain cutoff frequency f_{max}(GHz)	75	96	38	30

comparison. Contrary to the digital application, the uniformity requirement of threshold voltage is more relaxed since only discrete FET devices are involved in microwave applications. This makes the MODFET a more favorable candidate for microwave circuits.

1.4 Feasibility of MODFET Technology

When evaluating a new device technology, four key factors need to be considered. They are speed and energy consumption, complexity of the process, yield, and the scaling potential into the submicron range.

The intrinsic speed and energy requirements are related to the drift velocity of the electrons in the channel, therefore the MODFET is expected to be the best among the existing FET technologies because of its mobility advantage of the 2DEG (even though this mobility advantage disappears for drift fields above a few hundred V/cm[22][23]), as proven by the actual measurements shown in Fig. 1.6[8] and Table 1.2.[2]

The complexity of the process and yield of the MODFET technology are still far from mature. Two major problems, quality of the epitaxial layer and threshold voltage uniformity, need to be solved. Some progresses have been made. Defect density below 100 cm^{-2} [24] and threshold voltage standard deviation of only 4mV at I_d=10μA [25] have been reported. At present, the recess etching problem is solved at the expense of increasing process complexity. The method that is widely used is to introduce a self-terminating-layer during MBE growth. Dry ion reactive etch (RIE) is then used to do the etch quite uniformly. More details of this method will be discussed in Chapter 6. Further efforts in these techniques are needed for the economically feasible MODFET technology.

Table 1.2 Device technology comparison graded 1 (best) through 5.(2)

	GaAs				Si	
	MODFET	MESFET	Vertical FET	HBT	CMOSFET	BJT
Speed	1	3	1	2	5	4
Power delay product	1	2	2	4	5	4
Lithographic requirement	2	3	5	1	1	4
Doping control	4	4	4	1	2	1
Processing complexity	2	1	4	5	3	5
Materials problems	4	3	5	4	1	2

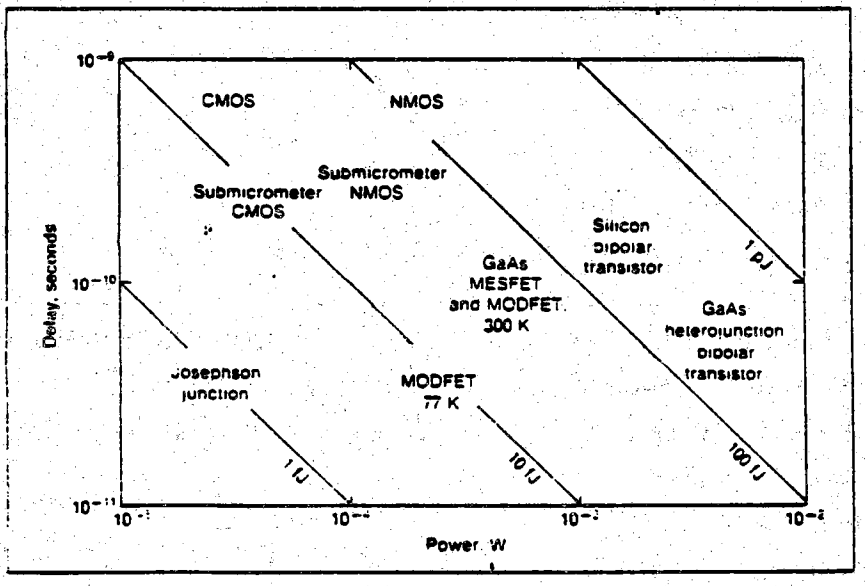


Figure 1.6 A comparison of various device technologies.(8)

Both vertical and lateral dimensions limit the ultimate extent to which a FET can be scaled down. Vertically, similar to Si MOSFETs whose minimum oxide thicknesses are limited to about 40Å by electron tunneling, the minimum thickness of AlGaAs in the MODFET is approximately 200Å by the same token. Another limit to decreasing the n+AlGaAs layer comes from the requirement that enough donors in the n+AlGaAs, i.e., N_2 (doping density in AlGaAs) x t_2 (n+AlGaAs thickness), are needed to provide the carrier concentration in the 2DEG, n_s, as high as possible (usually $\approx 10^{12} cm^{-2}$). The third limit is due to the necessity of the spacer layer (≈50Å to 200Å) between the n+AlGaAs and the undoped GaAs to ensure the high electron mobility in the 2DEG. The lateral scaling of the MODFET depends physically somehow on the vertical dimension. This can be explained by fringing effects as follows: One of the primary reasons to reduce the gate length is to reduce the gate capacitance. As the gate length is decreased to the order of the gate-to-channel separation, the fringing effects become dominant. There will be no further gate capacitance reduction, nor further speed improvement by squeezing the gate length. Another factor to limit the lateral dimension for III-V compound channels is the ballastic transport effect. This comes into play when the gate length is below 0.5μm.

MODFETs, on the basis of the above discussion, clearly indicate a superiority over other FET technologies in terms of achieving operation of ultrafast transistors, lower power dissipation, and lower noise. The continuous improvement in MODFET technology is expected to make it a very bright candidate for superfast circuit applications.

1.5 The Organization of Thesis

In Chapter 2, theory and equations describing MODFETs will be discussed. Chapter 3 will present the circuit and mask design of the MODFET logic gates and circuits. A detailed discussion on development of fabrication process and related experimental results will be given in Chapter 4. Chapter 5 will present the electrical characterizations of all circuits (inverters, three-input NAND, NOR logic gates, and ring oscillators) fabricated. Some recommendations for future work will be suggested in Chapter 6.

CHAPTER 2

THEORY OF MODFET

This chapter discusses theories of MODFETs. The model of calculations presented here is basically developed by Delagebeaudeuf and Linh.[25] In this model, the subband splitting and the existence of an undoped AlGaAs spacer layer between the doped AlGaAs and undoped GaAs are considered.

Section 2.1 will discuss the electrostatics of a normal heterojunction. Section 2.2 will consider the 2DEG which is isolated from the effect of the Schottky gate on top of the doped AlGaAs layer, refered to as the isolated regime. Section 2.3 will present a discussion on the charge control regime, where the effect of the Schottky gate on the 2DEG will be considered. Section 2.4 will present the analytical formula of current-voltage relationship of the MODFET. Finally, the modifications of the model under some conditions, such as second order effects, and the correspondence between the MOSFET and MODFET will be discussed in Section 2.5.

2.1 Heterojunction Electrostatics

The depletion approximation shown by the solid line in Fig. 2.1 (b) (the actual case is shown by the dashed line) is used to find the relationship between the doping densities, N_1 and N_2, and depletion widths, x_1 and x_2, of the heterojunction formed by AlGaAs and GaAs. (Note: subscripts 1 and 2 refer to the quantities in GaAs and AlGaAs, respectively).

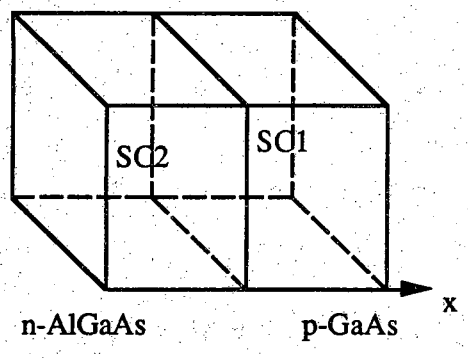
The charge neutrality relationship gives

$$qN_1x_1=qN_2x_2 \tag{2.1}$$

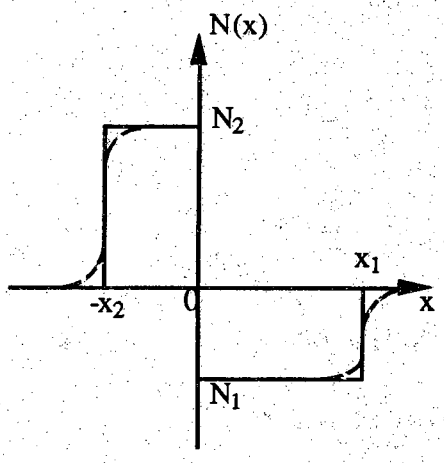
The Poisson equations of both sides are

$$\frac{\partial E_1(x)}{\partial x} = -\frac{qN_1}{\varepsilon_1} \tag{2.2}$$

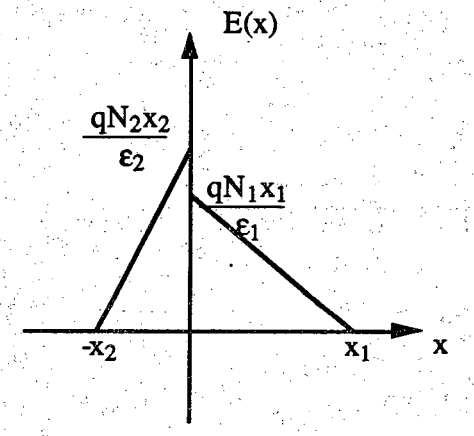
$$\frac{\partial E_2(x)}{\partial x} = \frac{qN_2}{\varepsilon_2} \tag{2.3}$$



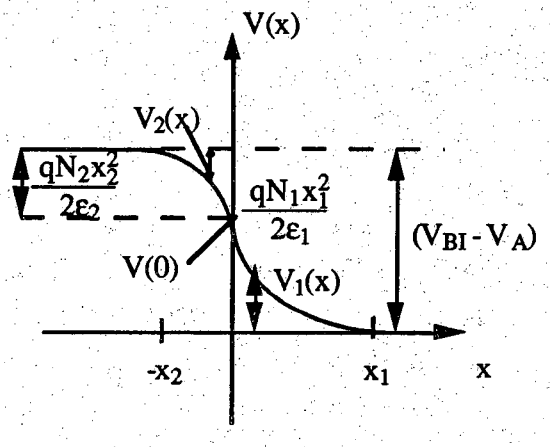
(a) AlGaAs/GaAs contact



(b) space charge distribution



(c) electric field



(d) potential

Figure 2.1 Heterojunction electrostatics.

Integrating these two equations and using the depletion approximation, we obtain:

$$E_1(x) = \frac{qN_1(x_1-x)}{\varepsilon_1} \tag{2.4}$$

$$E_2(x) = \frac{qN_2(x_2+x)}{\varepsilon_2} \tag{2.5}$$

as shown in Fig. 2.1 (c). Integrating the following equations:

$$V_1(x) = \int_x^{+\infty} E_1(x)dx \tag{2.6}$$

$$V_2(x) = \int_{-\infty}^{x} E_2(x)dx \tag{2.7}$$

where V_1, V_2, the built-in potential, V_{bi}, and the applied voltage across the heterojunction, V_A, are defined in Fig. 2.1 (d). These quantities are related as:

$$V(0) = \frac{qN_1x_1^2}{2\varepsilon_1} = (V_{bi}-V_A) - \frac{qN_2x_2^2}{2\varepsilon_2} \tag{2.8}$$

Solving (2.8) and (2.1) for x_1 and x_2, we obtain:

$$x_1 = \left[\frac{2\varepsilon_1\varepsilon_2N_2(V_{bi}-V_A)}{qN_1(\varepsilon_1N_1+\varepsilon_2N_2)}\right]^{\frac{1}{2}} \tag{2.9}$$

$$x_2 = \left[\frac{2\varepsilon_1\varepsilon_2N_1(V_{bi}-V_A)}{qN_2(\varepsilon_1N_1+\varepsilon_2N_2)}\right]^{\frac{1}{2}} \tag{2.10}$$

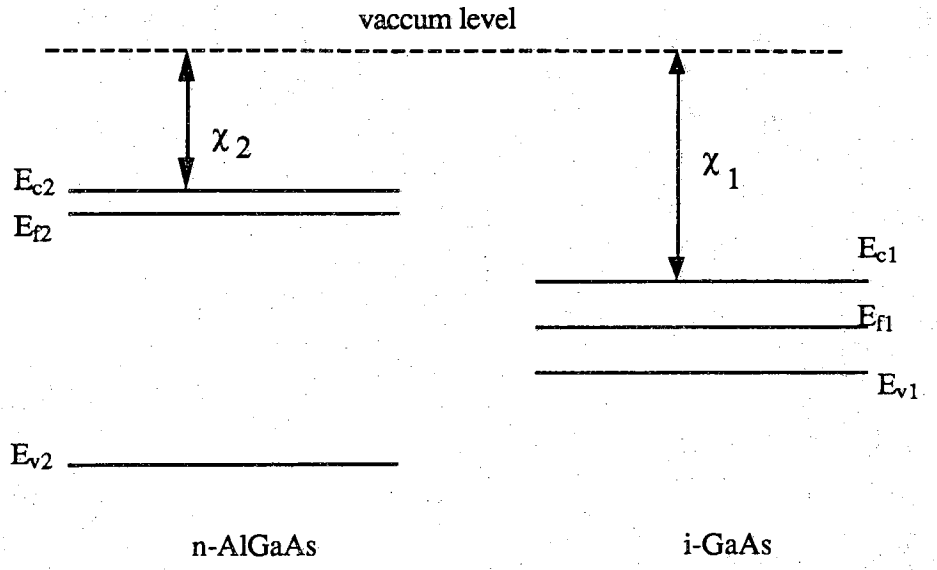
The energy band diagram of AlGaAs and GaAs before and after contact are shown in Fig. 2.2.

The MODFET heterojunction is much more complicated than what we have discussed above. The appropriate space charge distribution for a MODFET AlGaAs/GaAs heterojunction is illustrated by Fig. 2.3. An extra layer of electrons (the 2DEG) as well as an electrically neutral spacer layer are added to Fig. 2.1 (b).

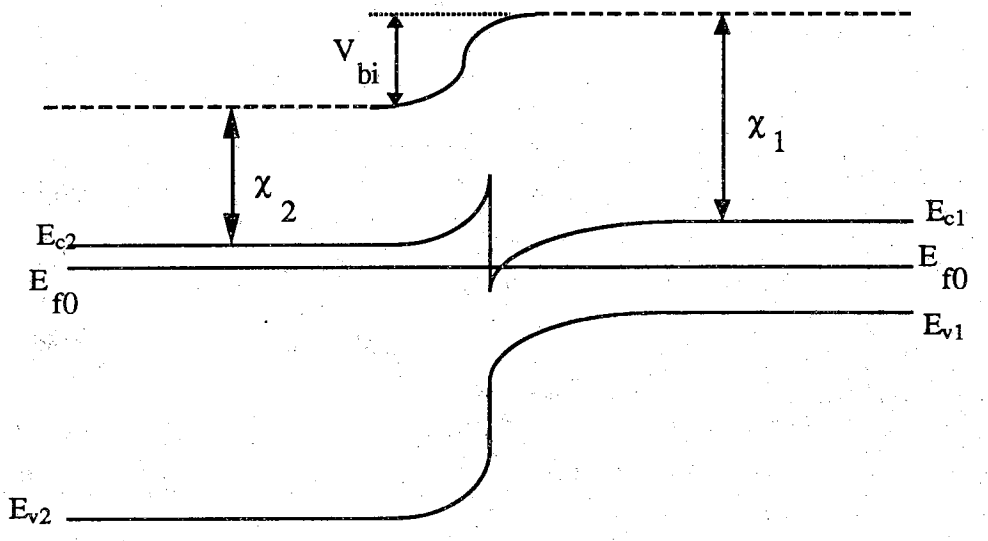
The very thin 2DEG layer (approximately 100Å) implies the electrons are confined in a potential well with a dimension comparable to the carrier's effective Bohr radius, therefore quantum mechanics must be used to describe the 2DEG's behavior.

2.2 The 2DEG

To solve the Schrodinger equation of an electron in the 2DEG, the potential energy must consist of the contributions from both ionized donors in AlGaAs and other electrons in the 2DEG. A very important assumption is the so-called quasi-constant electric



(a) Energy levels of AlGaAs and GaAs before contact.



(b) Energy band diagram of AlGaAs/GaAs heterojunction.

Figure 2.2 Energy band diagrams of AlGaAs/GaAs before and after contact.

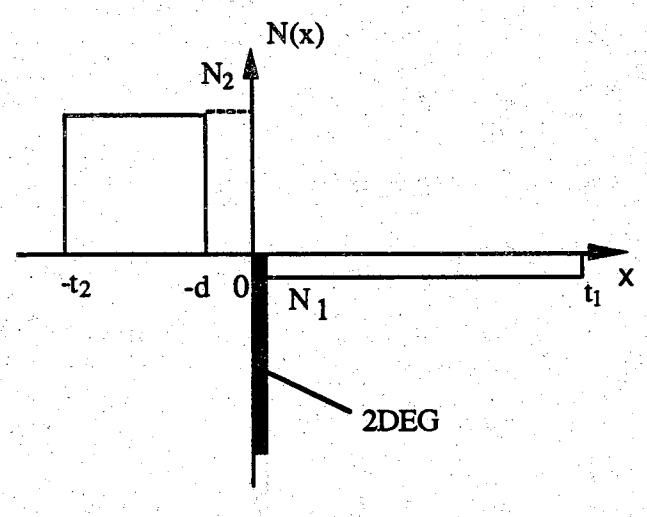


Figure 2.3 Space charge distribution of MODFET.

field E in the potential well or triangular potential. It is deduced from the fact that the electric field E contributed by the other electrons in the 2DEG can be introduced as an average constant value while the linear electric field due to ionized donors can be approximated by a constant when the extremely small segment (which is the thickness of the 2DEG ≈100Å, as compared to the whole depletion width of ≈5000Å in GaAs) is considered. With this assumption, the self-consistent Schrodinger-Poisson equations can be solved[27][28][29] and the longitudinal quantized energy is obtained:

$$E_n(eV) = \left[\frac{h^2}{8\pi^2 m_l^*}\right]^{\frac{1}{3}}\left[3\pi qE\right]^{\frac{2}{3}}\left[n+\frac{3}{4}\right]^{\frac{2}{3}} \qquad (2.11)$$

where m_l^* is the longitudinal effective mass, h is the Planck's constant, E is the electric field and n is the quantum number of the energy level.

The 2DEG is characterized by three physical parameters for the equilibrium state: The Fermi-level position in the 2DEG E_{f0}, the sheet density of 2DEG carriers n_s, and the electric field at the interface in GaAs E_{1i}. The relationship between them will be established. The notations are defined by Fig. 2.4 and Fig. 2.5.

2.2.1 n_s versus E_{1i}

The Poisson equation of the GaAs depletion region is

$$\frac{dE}{dx} = \left(\frac{q}{\varepsilon_1}\right)(n(x)-N_1) \qquad (2.12)$$

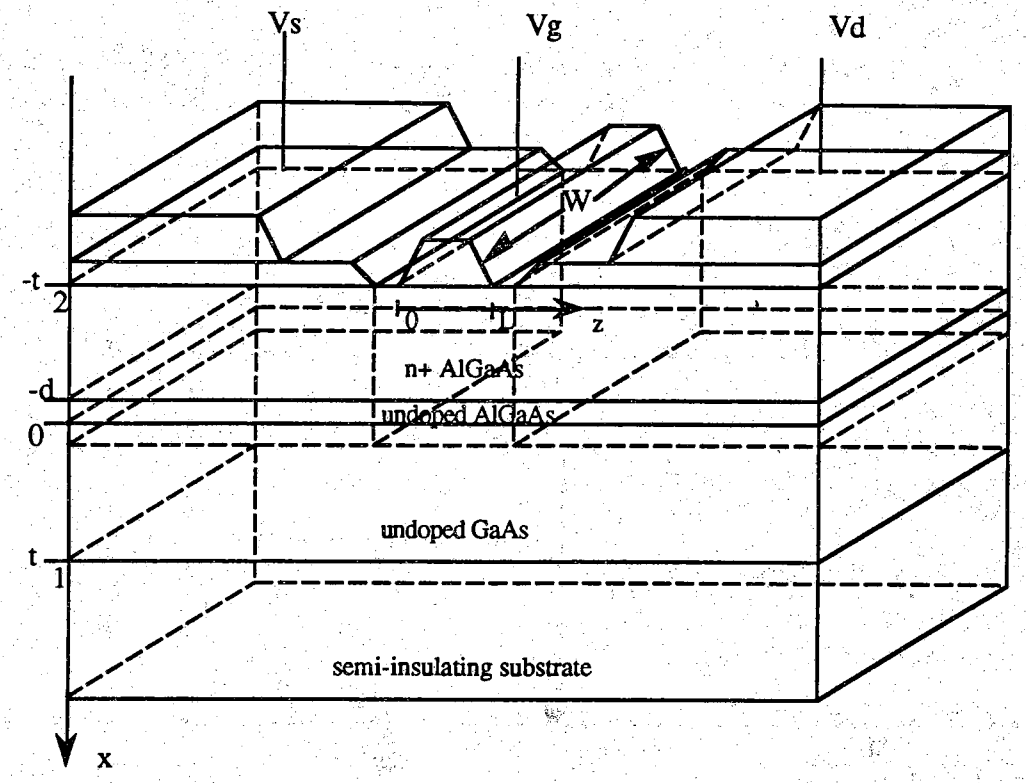


Figure 2.4 MODFET structure with defined notations and coordinates.

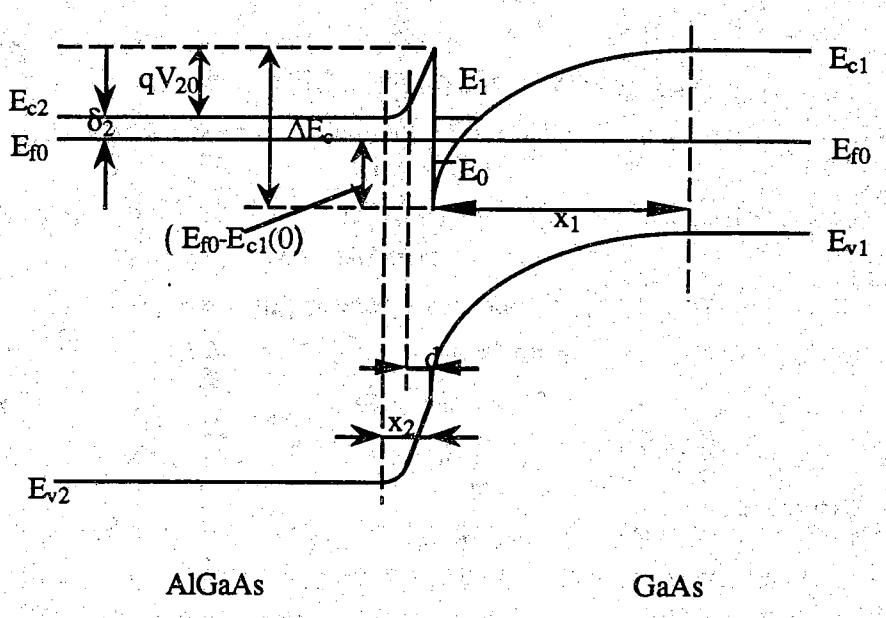


Figure 2.5 MODFET energy band diagram for isolated regime.

where N_1 is ionized donor density in GaAs and n(z) is bulk free electron concentration. Integration across the depletion region (between $E(x=x_1)=0$ and $E(x=0)=E_{1i}$) of GaAs layer gives

$$\varepsilon_1 E_{1i}=q(n_s+N_1 x_1) \tag{2.13}$$

Typically, $N_1x_1\approx10^{14}cm^{-3}x0.5\mu m = 10^{10}cm^{-2} << n_s\approx10^{12}cm^{-2}$, thus

$$\varepsilon_1 E_{1i}\approx qn_s \tag{2.14}$$

Likewise, we have the similar relationship for the undoped AlGaAs:

$$\varepsilon_2 E_{2i}\approx qn_s \tag{2.15}$$

Substituting (2.14) into (2.11) for GaAs, we have the first two energy levels:

$$E_0(eV)\approx\gamma_0(n_s)^{2/3}$$
$$E_1(eV)\approx\gamma_1(n_s)^{2/3} \tag{2.16}$$

The two constants obtained here:

$\gamma_0 = 2.26x10^{-12}$
$\gamma_1 = 4.0x10^{-12}$ (SI)

are adjustable. They are experimentally estimated as:(6)(30)(31)

$\gamma_0 = 2.50x10^{-12}$
$\gamma_1 = 3.20x10^{-12}$ (SI)

2.2.2 n_s vs. E_f

The density of states $\Delta n(E)$ for a two dimensional system is

$$\Delta n(E) = \frac{4\pi q m^*}{h^2} \tag{2.17}$$

The density-of-states function is shown by Fig. 2.6. Using Fermi-Dirac statistics, we get:

$$n_s = \Delta n(E)\int_{E_0}^{E_1}\frac{dE}{1+e^{\frac{(E-E_f)}{kT}}} + 2\Delta n(E)\int_{E_1}^{+\infty}\frac{dE}{1+e^{\frac{(E-E_f)}{kT}}}$$
$$= \frac{\Delta n(E)kT}{q}\ln(1+e^{\frac{(E_f-E_0)}{kT}})(1+e^{\frac{(E_f-E_1)}{kT}}) \tag{2.18}$$

This expression applies to a two-level system. It is also a valid approximation to the N-level system because typically only the first 2 levels are significantly filled.

More practically, we desire to establish a function in terms of donor density in the AlGaAs N_2 and the thickness of the undoped AlGaAs spacer layer d.

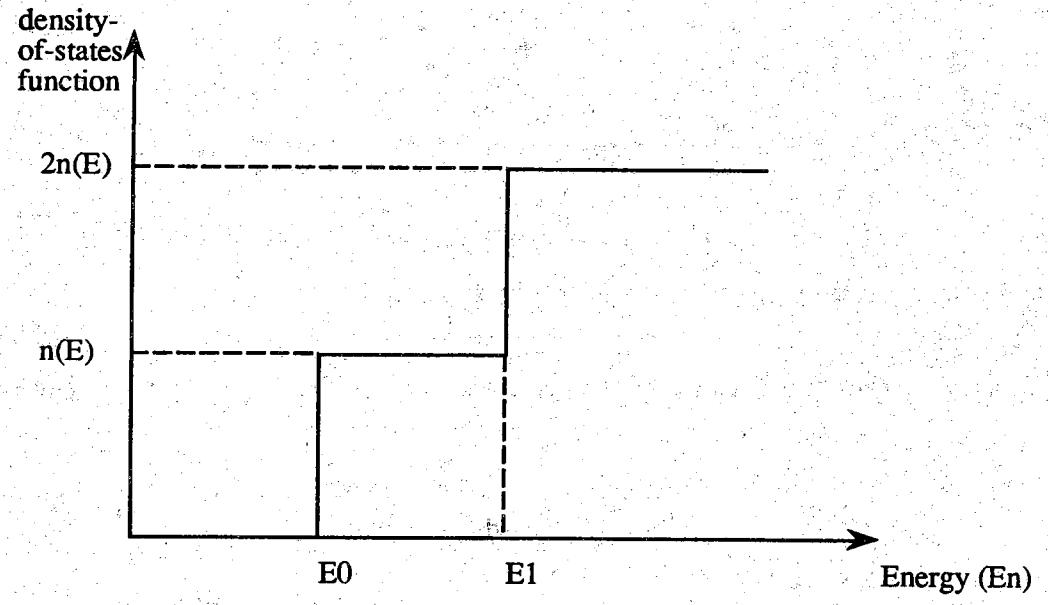


Figure 2.6 Density-of-states function vs. energy En.

2.2.3 $n_s=f(d, N_2)$

The Poisson equation for the depletion region in AlGaAs is

$$\frac{d^2 V_2}{dx^2} = -\frac{qN_2(x)}{\varepsilon_2} \tag{2.19}$$

where V_2 is the potential drop in AlGaAs from the AlGaAs/GaAs interface and N_2 is the donor density in AlGaAs, with the boundary conditions:

$$V_2(x=0) = 0$$
$$\left[\frac{dV_2}{dx}\right]_{x=-x_2} = -E_2(x=-x_2) = 0$$
$$\left(\frac{dV_2}{dx}\right)_{x=0} = -E_{2i} \tag{2.20}$$

and

$$N_2(x)=0, \quad -d < x < 0$$
$$N_2(x)=N_2, \quad -x_2 < x < -d \tag{2.21}$$

where x_2 is the depletion width of doped n+ AlGaAs plus the thickness of the spacer layer and is determined by (2.10). Solving these equations, we find the band bending in AlGaAs, V_{20}, as defined in Fig. 2.5:

$$\varepsilon_2 E_{i2} = qN_2(x_2 - d) \tag{2.22}$$

$$V_{20} = \frac{qN_2(x_2^2 - d^2)}{2\varepsilon_2} \tag{2.23}$$

Combining (2.22) and (2.23) gives:

$$\varepsilon_2 E_{2i} = \sqrt{2q\varepsilon_2 N_2 V_{20} + q^2 N_2^2 d^2} - qN_2 d \tag{2.24}$$

From the energy band diagram of Fig. 2.5 we have:

$$qV_{20} = \Delta E_c - E_{f0} + E_{c1}(0) - \delta_2 \tag{2.25}$$

Additionally, with the interface states neglected, Gauss's Law can be applied to get

$$\varepsilon_2 E_{2i} \approx \varepsilon_1 E_{1i} = qn_s \tag{2.26}$$

The final expression is then obtained from (2.18), (2.24) and (2.26):

$$\sqrt{2q\varepsilon_2 N_2 V_{20} + q^2 N_2^2 d^2} - qN_2 d = qn_s$$

$$= \Delta n(E) kT \ln\left(1 + e^{\frac{(E_{f0} - E_{c1}(0) - E_0)}{kT}}\right)\left(1 + e^{\frac{(E_{f0} - E_{c2}(0) - E_1)}{kT}}\right) \tag{2.27}$$

Here, E_0 (or E_1) are energy difference between the ground level (or the first level) and the valence energy band at x=0, i.e., $E_{c1}(0)$. This equation can only be solved numerically. The procedure is to pick an arbitrary low value for $E_{f0}-E_{c1}(0)$ to determine n_s by (2.24), (2.25) and (2.26). E_0 and E_1 are computed by (2.16) and are then substituted back to (2.18) to calculate a new n_s. Iterate this procedure until the two n_s's calculated above are equal.

Given some basic constants:

$N_c = 2(2\pi m_n^* kT/h^2)^{3/2} = 9.15 \times 10^{17} cm^{-3}$,

$\delta_2 = (E_c - E_f)_{AlGaAs} = kT \times \ln(N_c/N_d)$ (eV),

$\Delta E_c = 1.06x$ (V) $= 0.32$eV

where the mole fraction of Al, x, is assumped to be 0.3, and

kT=0.0259eV (300K),

$m_n^* = 0.11 m_0$,

$\varepsilon_2 = 1.08 \times 10^{-12}$F/cm,

$\Delta n(E) = 2.75 \times 10^{13}\ V^{-1} cm^{-2}$,

the carrier concentration can be calculated in terms of spacer thickness d and doping density in AlGaAs, N_2, as shown in Table 2.1[33] and Fig. 2.7.[33]

2.3 Schottky Gate Charge Control Regime

In this section, the effects of the Schottky gate on the 2DEG will be investigated. Suppose the AlGaAs layer is thin enough or the gate voltage is negative enough that the AlGaAs layer is completely depleted. The band diagram of the influence of the Schottky

Table 2.1 The 2DEG carrier concentration n_s (cm^{-2}).(33)

d (Å)	AlGaAs doping density N_2 (cm^{-3})		
	$1x10^{17}$	$5x10^{17}$	$1x10^{18}$
50	$4.79x10^{11}$	$9.00x10^{11}$	$1.13x10^{12}$
100	$4.44x10^{11}$	$7.73x10^{11}$	$9.27x10^{11}$
150	$4.12x10^{11}$	$6.73x10^{11}$	$7.84x10^{11}$
200	$3.83x10^{11}$	$5.95x10^{11}$	$6.77x10^{11}$

gate is shown in Fig. 2.8. The Poisson equation is then:

$$\frac{d^2V}{dx^2} = -\frac{qN_2(x)}{\varepsilon_2} \tag{2.28}$$

with the conditions

$$N_2(x)=0, \quad -d < x < 0$$
$$N_2(x)=N_2, \quad -t_2 < x < -d \tag{2.29}$$

and the potential reference point is taken at the interface: $V_2(x=0)=0$, then

$$V_2(-t_2) = \frac{qN_2(t_2-d)^2}{2\varepsilon_2} - E_{2i}t_2 = V_{p2} - E_{2i}t_2 \tag{2.30}$$

where t_2 is the thickness of the entire doped and undoped AlGaAs layer and

$$V_{p2} = \frac{qN_2(t_2-d)^2}{2\varepsilon_2} \tag{2.31}$$

From Fig. 2.8, we also have the relationship

$$qV_2(-t_2) = \Phi_{BN} - qV_g + E_f - E_{c1}(0) - \Delta E_c \tag{2.32}$$

where Φ_{BN} is the metal-semiconductor work function difference. Substituting (2.32) into (2.30), we get

$$\varepsilon_2 E_{2i} = \frac{\varepsilon_2\left(V_{p2}+V_g+\frac{-E_f-\Phi_{BN}+E_{c1}(0)+\Delta E_c}{q}\right)}{t_2} \tag{2.33}$$

From (2.26) and (2.33), we have:

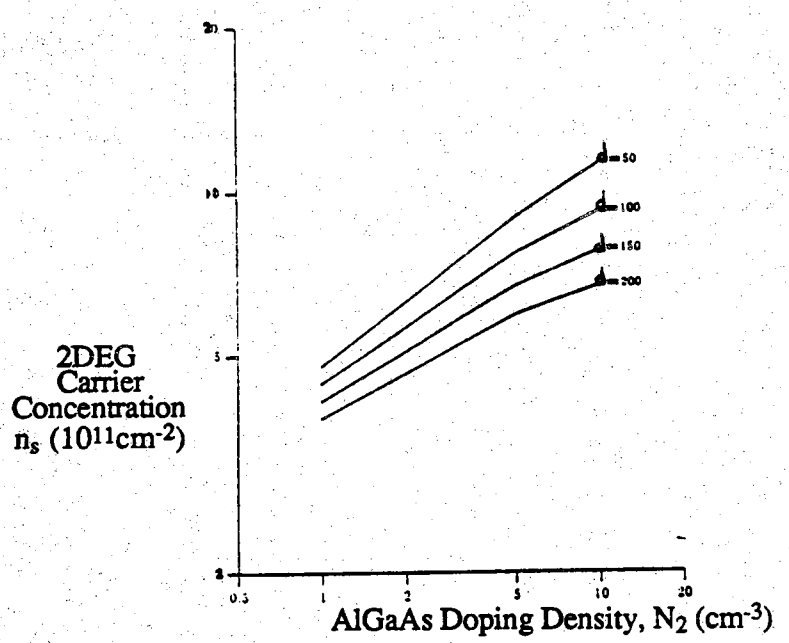


Figure 2.7 2DEG carrier concentration vs. AlGaAs doping density for various d.(33)

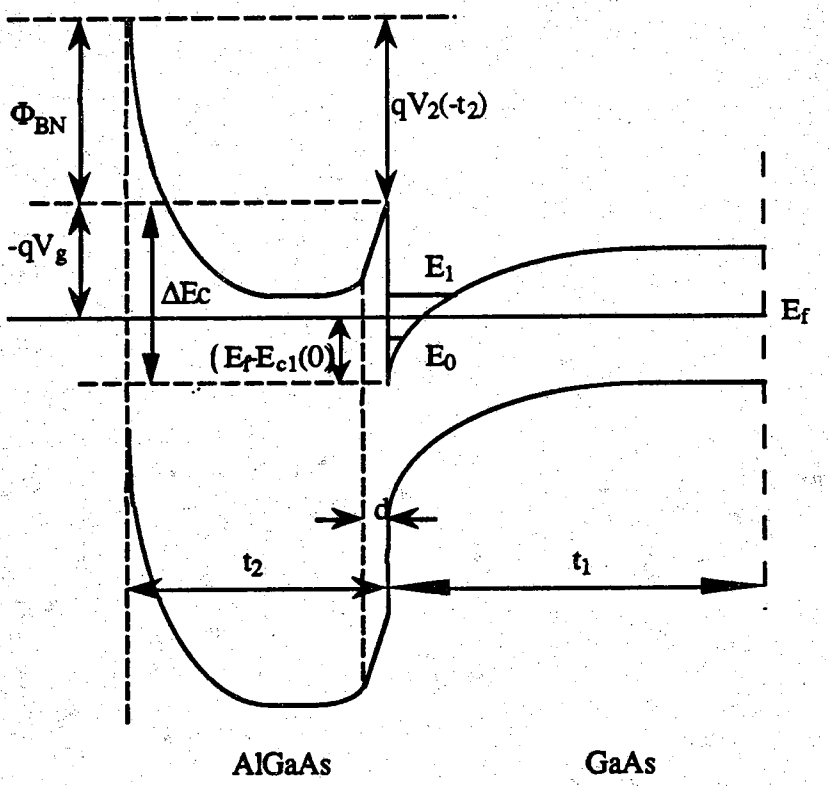


Figure 2.8 The energy band diagram for the charge control regime.

$$Q_s = -qn_s = -C_2(V_{p2}+V_g + \frac{-\Phi_{BN}-E_f+E_{c1}(0)+\Delta E_c}{q}) \quad (2.34)$$

where $C_2= \varepsilon_2/t_2$ can be considered as the capacitance of AlGaAs. Since E_f-$E_c(0)$ is always very small compared with the other terms (its dependence on the gate voltage will be discussed later), (2.34) can be reduced to

$$Q_S \approx - C_2(V_g-V_{th}) \quad (2.35)$$

$$V_{th} = \frac{\Phi_{BN} - \Delta E_c}{q} - V_{p2} \quad (2.36)$$

Obviously Q_S=0, i.e., the 2DEG is eliminated when V_g=V_{th}, therefore the V_{th} is defined as the threshold voltage.

By examination of above equations, several comments or conclusions can be made here.

2.3.1 The effect of interface states

If the interface states Q_i are taken into account, the threshold voltage V_{th} of (2.35) would be shifted as

$$V_{th} = \frac{\Phi_{BN} - \Delta E_c}{q} - V_{p2} - \frac{Q_i}{C_2} \quad (2.37)$$

2.3.2 Control of V_{th}

For a given device the terms Φ_{BN} and ΔE_c in (2.36) are fixed, therefore the threshold voltage V_{th} is controlled by the term $V_{p2}=qN_2(t_2-d)^2/2\varepsilon_2$. V_{p2} can be changed by changing either the doping of AlGaAs, N_2, or the thickness of the doped AlGaAs layer, t_2-d. A higher doping N_2 is usually used to provide a high carrier concentration (Note through (2.27) that the maximum 2DEG density depends on N_2). Thus, the thickness of the AlGaAs is most often used to control the V_{th}.

If the thickness of the doped AlGaAs layer, t_2, is large enough so V_{th} is a large negative number (see (2.31) and (2.37)), then the Q_s of the 2DEG is not zero, and a reverse bias voltage on the Schottky gate is needed to shut off the channel of the device. The device is then "depletion-mode". When the thickness t_2 is decreased, V_{p2} is decreased and V_{th} becomes less negative. At a point where t_2 is decreased to such a value that V_{th}=0, from (2.35) a forward bias gate voltage is now needed to create a 2DEG channel to turn on the device. After this point the device becomes "enhancement-mode".

Physically the transition that from the isolated regime to the charge control regime occurs when the gate-to-channel separation is equal to the depletion region width

contributed by both Schottky gate and AlGaAs/GaAs heterojunction. Alternatively, for a given thickness t_2, the transition gate voltage V_{gtr} between the two regimes can be found by equating (2.24) to (2.33),

$$V_{gtr} = \frac{\Phi_{BN}-\delta_2}{q} - \left[\sqrt{\frac{qN_2t_2^2}{2\varepsilon_2}} - \sqrt{\frac{\Delta E_c-\delta_2- E_{f0}+E_{c1}(0)}{q} + \frac{qN_2d^2}{2\varepsilon_2}}\right]^2 \tag{2.38}$$

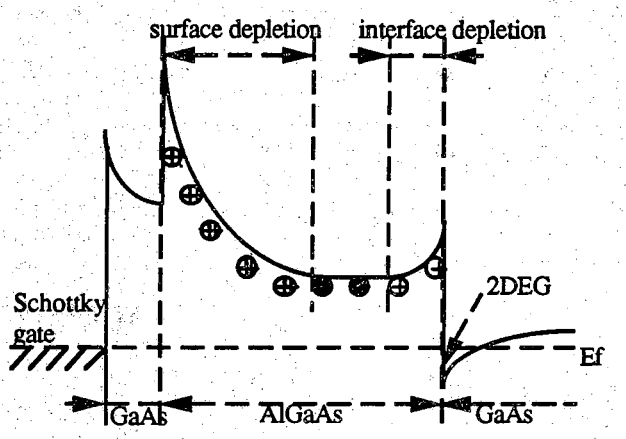
A decreased thickness of the doped AlGaAs layer will lead to an increased threshold voltage. This also makes sense from the band diagram point of view. Fig. 2.9 (a) shows that before etch, the n+AlGaAs layer is partially depleted by surface (the outside face for metal contact) and interface (between AlGaAs and undoped GaAs) depletion. The device now is depletion-mode, $V_{th} < 0$, because it is conducting when $V_g=0$. After some of n+AlGaAs layer is etched away, the total number of donors is decreased so that more neutral donors are ionized. After all donors are ionized when the etch continues, the density of carriers in the 2DEG will begin to decrease. The interface bands of GaAs will become more flat (in Fig. 2.9 (b)) than in Fig. 2.9 (a). The device now is still depletion-mode because a 2DEG is still there, but V_{th} has become less negative. As the etch is continued further, the band bending in the GaAs becomes more and more flat until it touches the interface Fermi level (Fig. 2.9 (c)). At this point, any small change in gate bias will turn the transistor on or off, by positive or negative gate voltage, respectively, therefore $V_{th}=0$ now. The transistor becomes enhancement-mode from this point on. Further etch after this will cause the space charge region in the AlGaAs to extend into the GaAs layer until the 2DEG disappears, as shown in Fig. 2.9 (d). $V_{th} > 0$ now because the transistor will be turned on only when a positive V_{gs} ($> V_{th}$) is applied, as shown by the dashed line in Fig. 2.9 (d).

2.3.3 Depletion-mode and enhancement-mode Device

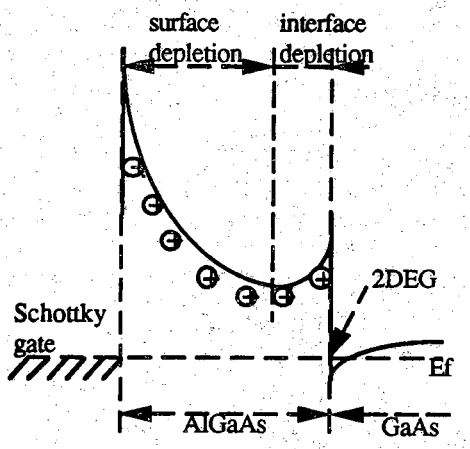
For the depletion-mode device, the optimal AlGaAs thickness t_2 is chosen such that $V_{gtr}=0$:

$$t_{2op} = \sqrt{\frac{2\varepsilon_2(\Phi_{BN}-\delta_2)}{q^2N_2}} + \sqrt{\frac{2\varepsilon_2}{q^2N_2}(\Delta E_c-\delta_2-E_{f0}+E_{c1}(0))+d^2} \tag{2.39}$$

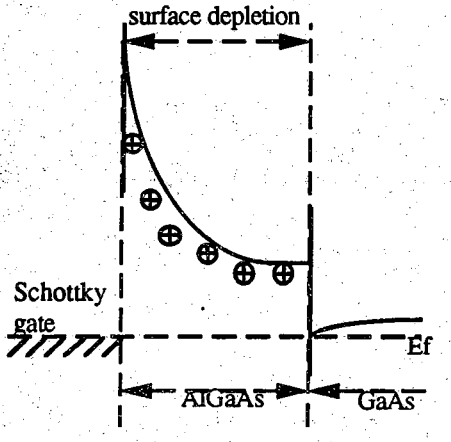
This t_{2op} enables the 2DEG be affected by any negative gate voltage. Given the Schottky barrier height $\Phi_{BN}=1.106eV$[34] and typical AlGaAs doping $N_2=1x10^{18}cm^{-3}$, for various spacer layer thickness d, the t_{2op} and corresponding threshold voltage V_{th} for the depletion-mode device can be calculated by (2.39) and (2.36), respectively, as shown



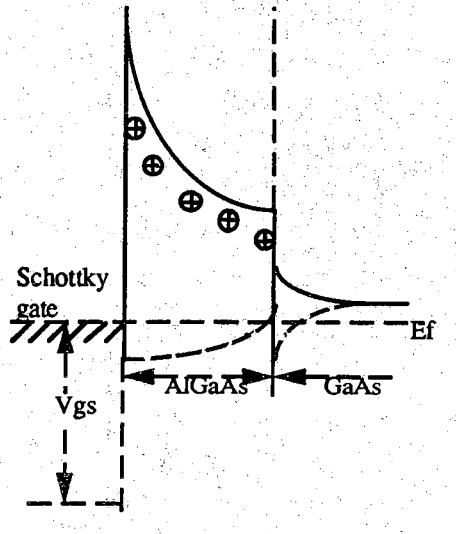
(a) before etch: Vth0 <0.



(b) after some etch: Vth0 < Vth1<0.

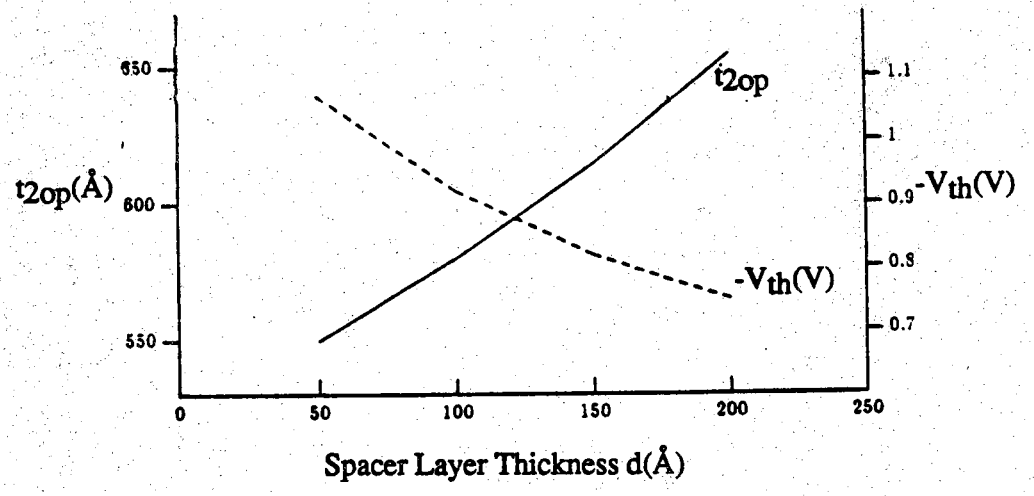


(c) more etch: the 2DEG is about to dissappear, Vth2 = 0.

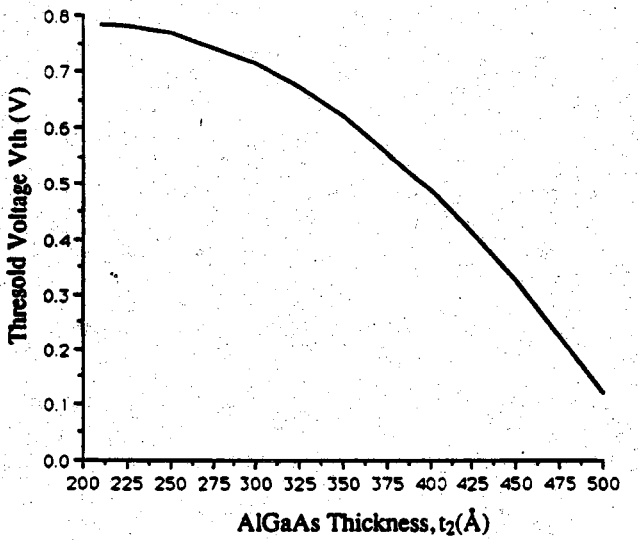


(d) more etch than (c): E-mode device formed, Vth3 > 0.

Figure 2.9 The energy-band diagrams with regard to etching.



(a) t_{2op} and V_{th} for optimal D-mode MODFET with $N_2=10^{18}cm^{-3}$.(33)



(b) t_2 vs. V_{th} for E-mode MODFET with $N_2=10^{18}cm^{-3}$, d=200Å.

Figure 2.10 N_2 vs. threshold voltages for (a) optimal D-mode and, (b) E-mode MODFET's.

in Fig. 2.10 (a). A thicker t_2 will produce a more negative V_{th} because part of the gate voltage must be used to deplete the extra thickness of AlGaAs, t_2-t_{2op}.

Similarly, for the enhancement-mode device, given spacer layer thickness d and AlGaAs doping N_2, a series of V_{th} vs. the various t_2 can be calculated from (2.31) and (2.36). The result is illustrated in Fig. 2.10 (b).

A final comment is about the choice of the spacer layer thickness, d. The trade-off is that a thinner d will lead to a higher 2DEG carrier concentration n_s but a lower mobility μ because of closer physical separation between the ionized impurity centers in AlGaAs and the carriers in 2DEG.

2.4 DC Current-Voltage Model of MODFET

The coordinate system used for this analysis is illustrated by Fig. 2.4. When a voltage V_d is applied between the grounded source and the positive drain, the effective voltage for charge control by the gate at any point of the channel, $V_{eff}(z)$, can be expressed in terms of the gate voltage V_g and the potential at the corresponding point in the channel $V_c(z)$:

$$V_{eff}(z) = V_g - V_c(z) \tag{2.40}$$

so (2.35) becomes

$$Q_s(z) \approx - C_2(V_g - V_c(z) - V_{th}) \tag{2.41}$$

The current in the channel at any point x is given by

$$I(z) = Q_s(z)v(z)W \tag{2.42}$$

where W is the gate width and v(z) is the electron velocity. Only the drift component is considered here because the diffusion component is small enough to be ignored for the first order analysis.

The electron velocity will be saturated by the scattering limitation after the effective electric field E in the channel exceeds a critical value E_c. Thus,

$$\begin{aligned} v &= \mu E, \quad E < E_c \\ v &= v_{sat}, \quad E > E_c \end{aligned} \tag{2.43}$$

(Note: unlike the Si MOSFET case, the saturation velocity v_{sat} is field dependant for GaAs MODFETs). Similar to the case in Si MOSFETs, there are also three operation regions for the MODFET. The first region is the linear region for small drain voltage V_d and $V_g > V_{th}$, where the drain current I_d is increased proportionally with V_d, corresponding to the electron velocity before saturation. The second region, $V_g > V_{th}$, but $V_{ds} \geq V_g - V_{th}$, is the saturation region where I_d is basically a constant for certain V_g, corresponding to the electron velocity saturation or the channel pinch-off in the drain end. The third region is

the triode region, $V_g > V_{th}$ but $V_{ds} \leq V_g - V_{th}$, which is an interim state between the linear and the saturation regions. Physically, this region corresponds to the state in which the 2DEG channel starts narrowing for the increased V_d to the channel pinch-off in the drain end. Once pinch-off occurs, I_d remains constant and the device enters the saturation region.

2.4.1 The linear region

In this region, the effective channel voltage drop $V_d'=V_c(L)-V_c(0)$ (where L is the gate length) is small as compared to V_g. We thus have:

$$V_{eff}(z) \approx V_g$$

$$v(z) = \mu E = \mu \frac{V_d'}{L}$$

Then (2.42) becomes:

$$I_d = \mu C_2 (\frac{W}{L})(V_g - V_{th})V_d' \tag{2.44}$$

If the source/drain access resistances R_s/R_d are considered, then

$$V_d' = V_c(L) - V_c(0) = V_d - I_d(R_s+R_d) \tag{2.45}$$

Substituting this into (2.44), we obtain

$$I_d = \mu C_2 (\frac{W}{L})(V_g - V_{th})[V_d - I_d(R_s+R_d)] \tag{2.46}$$

or

$$\frac{V_d}{I_d} = R_s + R_d + \frac{L}{\mu C_2 (V_g - V_{th})} \tag{2.47}$$

As mentioned earlier, in this linear region the MODFET acts as a pure controllable resistor. For small $I_d(R_s+R_d)$, (2.46) can be reduced to:

$$I_d = \mu C_2 (\frac{W}{L})(V_g - V_{th})V_d \tag{2.48}$$

2.4.2 Triode region

In this region, V_d is increased from the linear region so that the channel voltage drop can not be neglected. But the electric field in the channel does not reach E_c yet.

Substituting (2.40) into (2.42), yields:

$$I(z) = WC_2[V_g - V_{th} - V_c(z)]\mu \frac{dV_c(z)}{dz} \tag{2.49}$$

Integrating this equation from zero to L and assuming I(z) is a constant throughout the channel, we obtain:

$$I_d L = \mu C_2 W[(V_g - V_{th})(V_c(L) - V_c(0)) - \frac{1}{2}(V_c(L) - V_c(0))^2] \tag{2.50}$$

Substituting (2.45) into this equation and rearranging the result, we have:

$$I_d = \mu C_2 \left(\frac{W}{L}\right)\left((V_g - V_{th})[V_d - I_d(R_s+R_d)] - \frac{1}{2}[V_d - I_d(R_s+R_d)]^2\right) \quad (2.51)$$

Again, if $I_d(R_s+R_d)$ can be neglected as compared to the drain voltage V_d, (2.51) then becomes:

$$I_d = \mu C_2 \left(\frac{W}{L}\right)\left((V_g - V_{th})V_d - \frac{1}{2}V_d^2\right) \quad (2.52)$$

2.4.3 Saturation region

When V_d is increased, $V_d > V_g - V_{th}$, the channel will be pinched-off near the drain end first. The electric field at this end is larger than anywhere else in the channel because a portion of the drain voltage, $V_d-(V_g-V_{th})$, will be applied to the depletion region at the drain end of the channel. Integrating (2.49) from zero to x and rearranging the result, we have:

$$I_d z = \mu C_2 W[(V_g - V_{th})(V_c(z) - V_c(0)) - \frac{V_c^2(z) - V_c^2(0)}{2}] \quad (2.53)$$

$$V_c(z) = V_g - V_{th} - \sqrt{(V_g - V_{th} - V_c(0))^2 - \frac{2I_d z}{\mu W C_2}} \quad (2.54)$$

Applying $E(z)=dV_c(z)/dz$, $E(L)=E_c$, and $\mu = v_{sat}/E_c$ to (2.47) and (2.48), we get:

$$I_{dsat} = C_2 W v_{sat}(\sqrt{E_c^2 L^2 + (V_g - V_{th} - R_s I_{dsat})^2} - E_c L) \quad (2.55)$$

2.5 Discussion of Model

Under certain conditions, the model we have developed can be simplified while under some other circumstances, the model is modified by taking into account the effects we have ignored. A few simple cases will be discussed in this section. The correspondence between the MOSFET and MODFET will also be discussed.

2.5.1 Application of Model

For large gate length, $E_c L >> (V_g - V_{th} - R_s I_{dsat})$, (2.55) can be approximated as

$$I_{dsat} = \frac{\mu C_2}{2}\left(\frac{W}{L}\right)(V_g - V_{th} - R_s I_{dsat})^2 \quad (2.56)$$

If $R_s I_{dsat}$ can be neglected as compared to the $(V_g - V_{th})$, (2.56) becomes:

$$I_{dsat} = \frac{\mu C_2}{2}\left(\frac{W}{L}\right)(V_g - V_{th})^2 \quad (2.57)$$

This familiar square law can also be found in the MOSFET. Equating (2.52) to (2.57), the transition drain voltage V_{dsat} between the triode region and the saturation region can be found:

$$V_{dsat} = V_g - V_{th} \tag{2.58}$$

Clearly this point corresponds to the drain end channel pinch-off, as we mentioned earlier.

For short gate length, $E_cL << (V_g - V_{th} - R_sI_{dsat})$, (2.55) becomes

$$I_{dsat} = C_2 W v_{sat} (V_g - V_{th} - R_sI_{dsat}) \tag{2.59}$$

This linear dependence of I_{dsat} vs. V_g for the short gate case makes a constant saturation transconductance

$$G_m = \left(\frac{\Delta I_{dsat}}{\Delta V_g} \right)_{V_d=const} \tag{2.60}$$

an important figure for the merit of FETs, while the square dependence of (2.56) for large gate leads to an increased G_m proportional to V_g.

Also for short gate, the transition drain voltage V_{dsat} between the triode and the saturation regions can be found by equating (2.52) and (2.55), with some assumptions and simplifications,

$$V_{dsat} = (V_g - V_{th})\left(1 - \sqrt{1 - \frac{2E_cL}{(V_g - V_{th})}}\right) \tag{2.61}$$

For very small gate length L, this equation will be reduced to

$V_{dsat} \approx E_cL$

by first order Taylor expansion. This physically corresponds to the case of electron velocity saturation.

2.5.2 Modification of model

The first correction comes from our earlier assumption of small and constant Fermi level. In reality, the change in E_f with V_g changes the effective gate-to-channel separation by about Δt_2=80Å.[35] Thus

$$C_2 = \frac{\varepsilon_2}{t_2 + \Delta t_2} \tag{2.62}$$

Recall (2.35), the decreased C_2 will also decrease the carrier concentration of the 2DEG, especially when the doped AlGaAs layer is relatively thin.

The second obvious correction is to add the diffusion term which we did not consider in the previous model. An improved model including the mobility degradation effect, has been developed by Park et al.[36]

2.5.3 Correspondence between MOSFET and MODFET

From the previous discussion, the external current-voltage similarity between the MODFET and MOSFET has been mentioned. A physical correspondence can also be well

established. The AlGaAs layer can be treated as "insulator", similar to the gate oxide in the MOSFET because the reverse bias current through the Schottky gate is negligible. The band bending in the "insulator" (i.e., in the AlGaAs) in the MODFET can be thought of as due to a significant volume charge, such as ionized sodium, distributed throughout the insulator (oxide) in the MOSFET. The ΔE_c conduction band discontinuity replaces the semiconductor-to-insulator barrier height in the usual MOSFET. Such a correspondence allows the direct use of MOSFET formalism to model the MODFET.(37)

As we have derived in these two sections, the DC current-voltage relationships of the MODFET in the three regions, i.e., (2.48), (2.52) and (2.57) for the linear, the triode, and the saturation regions, respectively, have forms completely similar to that of Si MOSFETs for the corresponding operation regions. Since both external and physical correspondence exists between the MODFET and MOSFET, it is very profitable to make use of the knowledge of NMOS circuit design to design the MODFET circuit, which will be the subject of the next chapter.

CHAPTER 3

TEST CHIP DESIGN

With the model developed in the last chapter, we are able to design depletion-mode and enhancement-mode MODFET devices, inverters and other logic gates as well as some circuits like ring oscillators. This chapter will discuss the considerations for MODFET device and circuit design.

Design of discrete depletion-mode and enhancement-mode devices will be discussed in Section 3.1. Section 3.2 will discuss the design of logic gates and ring oscillators. Section 3.3 will present a MODFET process overview. Finally, Section 3.4 will discuss considerations for design of mask layout.

3.1 MODFET Device Design

The goal of this section is to find out the saturation current at zero gate bias I_{dsat} for the ungated device, and, for the device with a gate, to find the drain current Id for the given gate length L and gate voltage V_g. Fig. 3.1 shows the layout of a MODFET device with the defined dimension notations. The key formula used to design the device is equation (2.55).

First, consider the depletion-mode MODFET. Remembering the trade-off of undoped AlGaAs thickness d discussed earlier, usually the reasonable values of d and N_2 are 200Å and $1x10^{18}cm^{-3}$, respectively. Thus for the depletion-mode MODFET, Table 2.1 gives $n_s=6.77x10^{11}cm^{-3}$ and Fig. 2.10 (a) gives

t_2=660Å

V_{th}= - 0.75V.

$$C_2 = \frac{\varepsilon_2}{d_2} = 1.634x10^{-7}\frac{F}{cm^2}$$

Further, assume

$\mu=5000cm^2/V\text{-}sec.$

$v_{sat}=1x10^7cm/sec.$

$E_c=3x10^3V/cm$

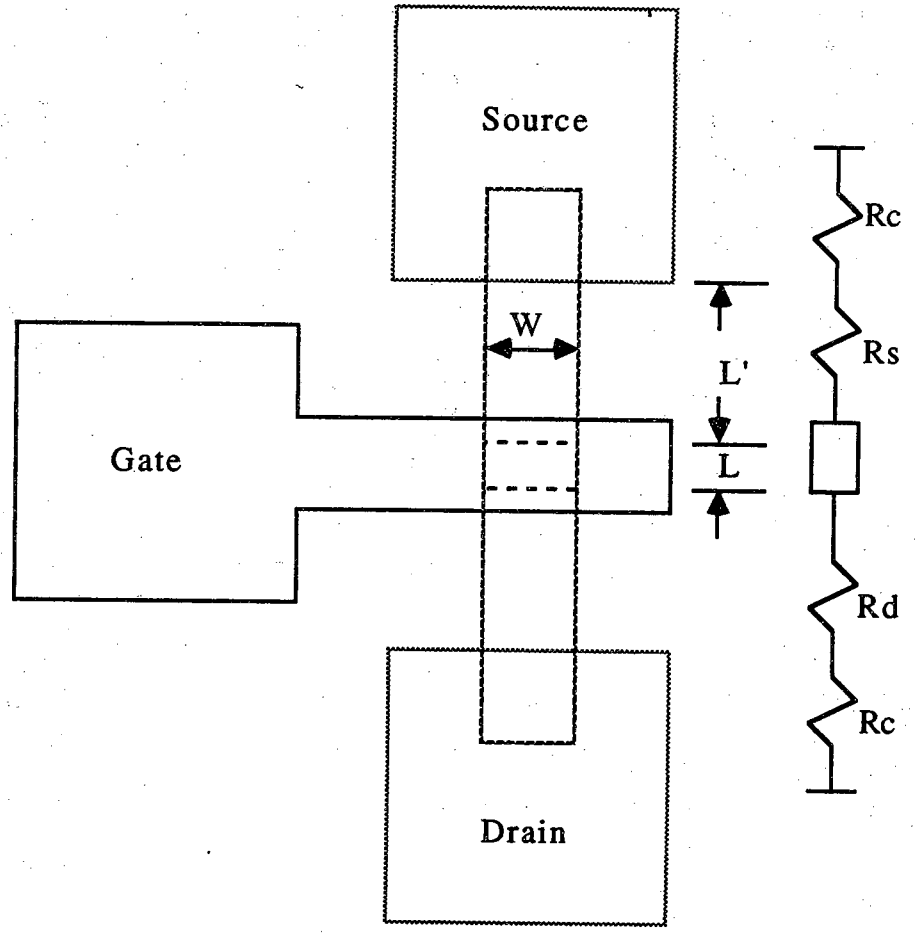


Figure 3.1 The layout of a MODFET device with dimension parameters defined.

The source or drain resistance

$$R_s = R_d = \rho_s \frac{L'}{W} + R_c \tag{3.1}$$

where

$$\rho_s = \frac{1}{q\mu n_s} \tag{3.2}$$

is the sheet resistance and R_c is the contact resistance (their measurements will be discussed in Chapter 5). Here ρ_s=1.84kΩ (as will be discussed in Chapter 5). Choosing L'=2μm, W=40μm and R_c=150Ω, we thus get R_d=R_s=242Ω. Substituting these values into (2.55), the numerical solution for I_{dsat} (Vg=0) versus gate length L for a depletion-mode MODFET is calculated and shown in Fig. 3.2 (a).

For the enhancement-mode device, the same procedure and parameters are taken except that

V_{th}=0.2V

d_2=380Å (from Fig. 2.10 (b)),

$C_2=\frac{\varepsilon_2}{d_2} = 2.83\text{x}10^{-7}\frac{F}{cm^2}$.

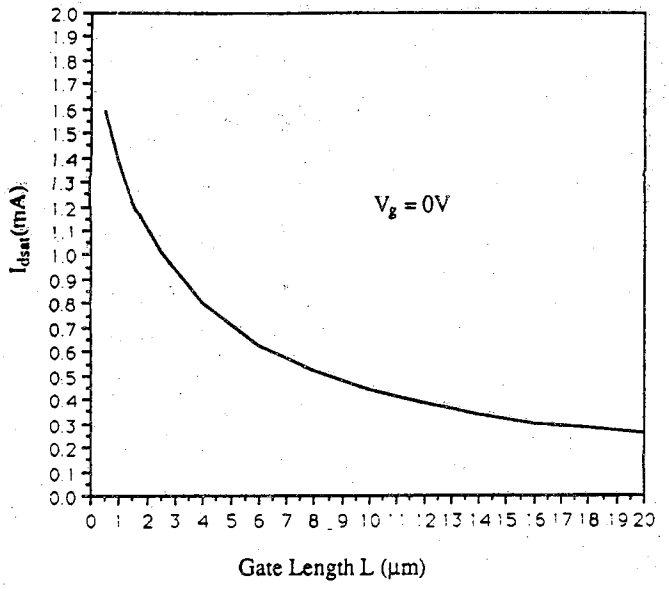
The numerical calculation results of $I_{dsat}(V_g=1V)$ vs. L are shown in Fig. 3.2 (b). For gate length L=2μm, I_{dsat} (V_g=1V) = 2.2mA.

3.2 Circuit Design

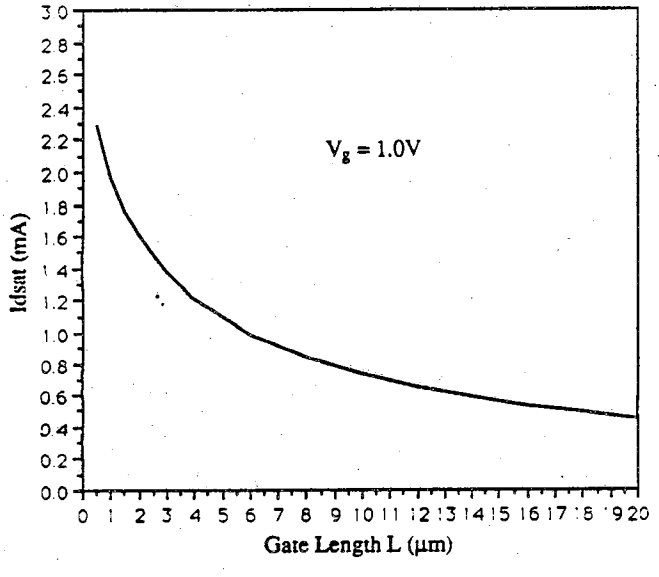
The inverter (NOT gate) is the basic element of all digital logic families and more complicated digital circuits. The design of the inverter, three-input NAND and NOR gates, and ring oscillator will be discussed in each of the following subsections. The DCFL circuit has been used for these circuits.

3.2.1 Inverter

As in the MOSFET case, the MODFET inverter can be created by several different ways, as shown in Fig. 3.3. They all have an enhancement-mode driver in common. Only the loads are changed. Either resistive load (resistor) or active load (transistor) can be used. Among them, the depletion load in Fig. 3.3 (b) is most usually used. One of the reasons is that when V_{in}=0, inverter's output high voltage V_{oH} can be pulled up to V_{dd} while the one in Fig. 3.3 (c) can not. This is due to the fact that the depletion-mode FET in Fig. 3.3 (b) is hooked-up in such a way that it acts as a non-linear resistor. V_{oH}=V_{dd} is also true for the ohmic load inverter in Fig. 3.3 (d). The load transistor is ohmic since it is forced to operate in its linear region. For these two cases, the loads are always conductive



(a) I_{dsat} vs. L for depletion-mode MODFET (V_g=0V).



(b) I_{dsat} vs. L for enhancement-mode MODFET (V_g=1V).

Figure 3.2 I_{dsat} vs. gate length L for (a) D-mode and, (b) E-mode MODFET's.

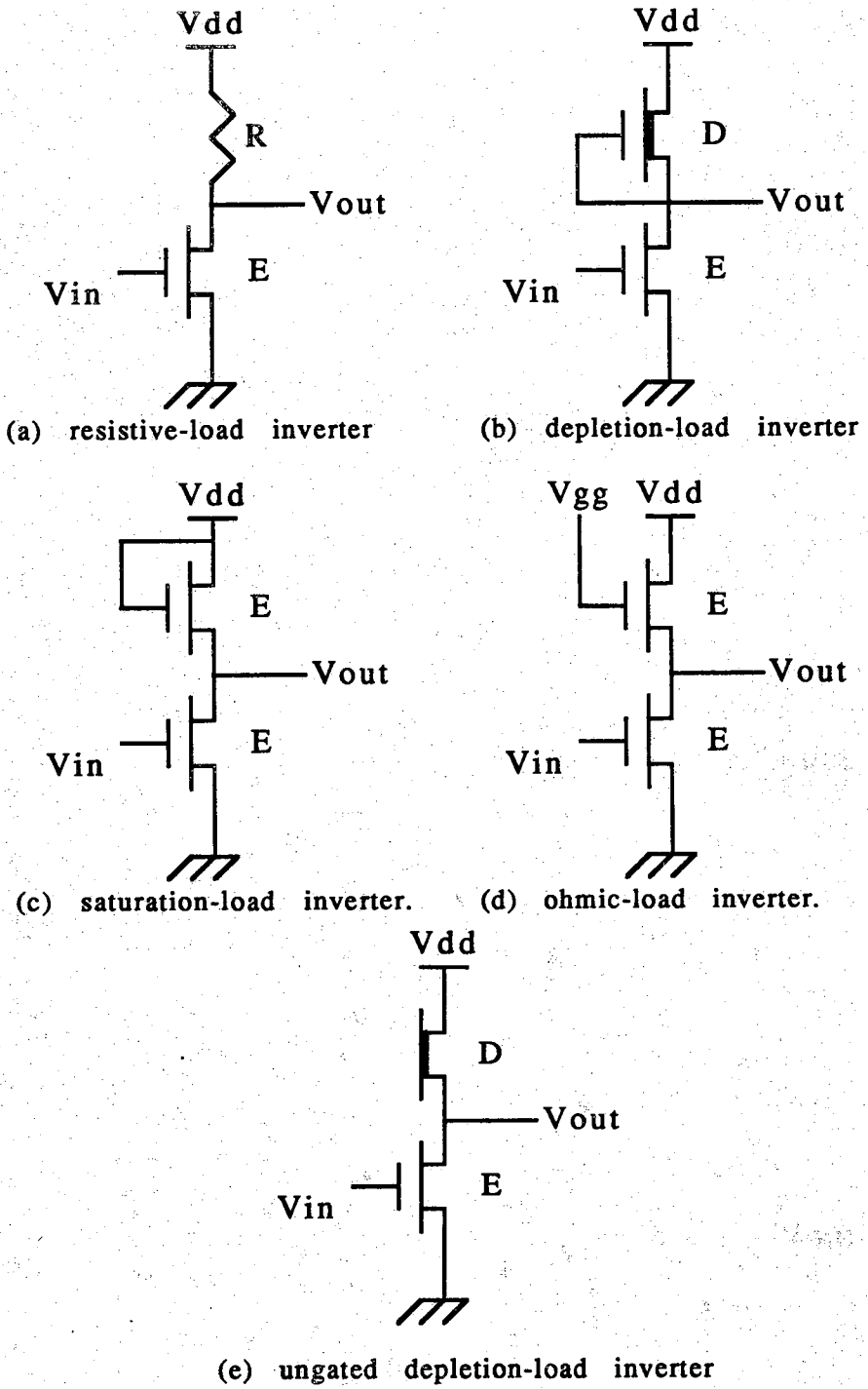


Figure 3.3 Inverter elements with various types of loads.

so that the output V_{out} is pulled up to $V_{OH}=V_{dd}$. In contrast, the saturated load in Fig. 3.3 (c) can not pull V_{out} all the way up to Vdd, but $V_{OH}=V_{dd}-V_{th}$ instead. This is because when the source of the load transistor has been pulled up to $V_{OH}=V_{dd}-V_{th}$, the gate-to-source voltage is $V_{dd}-(V_{dd}-V_{th})=V_{th}$, and the transistor turns off.

The type of inverter we have designed is shown in Fig. 3.3 (e). It is a depletion-load/enhancement-driver (E/D type) inverter. The load is an ungated device. Its "floating gate" can be thought of as $V_{gl}=0$ (subscripts l and d stand for load and driver, respectively) for the design calculation of the inverter.

Given V_{thl}=-3.5V, V_{dd}=1.0V, and V_{in}=0, we can construct the following table:

V_{out}	V_{dsl}	V_{gsl}	Vgsl-Vthl
V_{out}	$V_{dd}-V_{out}$	0V	$-V_{thl}$
0V	1V	0V	3.5V
1V	0V	0V	3.5V

Since $V_{dsl} < V_{gsl}-V_{thl}$ for all values of V_{out}, the load is always ohmic as the one shown in Fig. 3.3 (d).

Now the (W/L) ratio must be determined for both enhancement-mode driver and depletion-mode load. In addition, to make an inverter work properly, a very important parameter,

$$\beta_r = \frac{\beta_d}{\beta_l} \tag{3.2}$$

is yet to be determined, where

$$\beta_d = \mu_d C_{2d} \left(\frac{W}{L}\right)_d$$

$$\beta_l = \mu_l C_{2l} \left(\frac{W}{L}\right)_l$$

Considering the process technology available at Purdue (such as the minimum linewidth defined by the optical aligner) and the discussion of the last section, the following values for the dimension of the enhancement-mode driver (E-driver) were chosen:

$W_{driver}=W_d=40\mu m$

$L_{driver}=L_d=2\mu m$

$SD_{driver}=SD_d=6\mu m$

$L_d'=2\mu m$

where SD is the source-drain spacing and L' is defined in Fig. 3.1.

For the sake of symmetry and simplicity, W_{load} can take the same value as that of the driver, that is

$W_{load}=W_l=40\mu m$

What value of SD_{load} (or SD_l), which is also the "gate length" L_{load} (or L_l) for the ungated D-load, should be taken?

Supposing $V_{dd}=1.0V$, $V_{thd}=0.3V$ and $V_{thl}=-3.5V$, we will next calculate the output high and output low voltage of the inverter, V_{OH} and V_{OL}, respectively for input voltages of zero and V_{dd}. (Strictly speaking, V_{OH} is the output when the input is equal to the V_{OL}, not zero. Here zero and V_{dd} for input low and high, rather than the V_{OL} and V_{OH}, respectively, are chosen for simplicity).

For $V_{in}=0V$, $V_o=V_{OH}=V_{dd}$ since

$V_{gsd}=0 < V_{thd}=0.3V$,

the driver is shut off, therefore the drain current for E-driver $I_{dd}=0$.

$V_{dsl}=V_{dd}-V_{OH}\approx 0 < V_{gsl}-V_{thl}=+3.5V$

The load is in the ohmic operation region. V_{out} will be pulled all the way up to V_{dd} since the drain current of the load $I_{dl}= I_{dd}$ (because they are in series), is zero, therefore there is no voltage drop across the load, nor between the V_{dd} and V_{out}.

For $V_{in}=1.0V$, $V_o=V_{OL}$, which will be calculated as follows.

First, let's see what regions the driver and the load are eventually in.

$V_{gsd}=1.0V > V_{thd}=0.3V$

$V_{dsd}=V_{OL} < V_{gsd}-V_{thd}=1.0-0.3=0.7V$

The driver is in its ohmic or triode region. From (2.52), the current-voltage relationship of the E-driver is thus:

$$I_{dd} = \beta_d[(V_{gsd} - V_{thd})V_{dsd} - \frac{V_{dsd}^2}{2}] \tag{3.3}$$

The load is also ohmic because

$V_{gsl} = 0 > V_{thl}=-3.5V$

$V_{dsl}=V_{dd}-V_{OL}\approx 1.0V < V_{gsl}-V_{thl}=+3.5V$

therefore the current-voltage relationship of the load is:

$$I_{dl} = \beta_l[(V_{gsl} - V_{thl}) - \frac{V_{dsl}^2}{2}] \tag{3.4}$$

Equating (3.3) to (3.4) and rearranging the result, we obtain:

$$(1+\beta_r)V_{OL}^2+2V_{OL}[V_{thl} - \beta_r(V_{dd} - V_{thd})]-2(V_{thl} + \frac{V_{dd}}{2})V_{dd} = 0 \tag{3.5}$$

Substituting the assumed values of V_{dd}, V_{thd} and V_{thl}, we then have

$$(1+\beta_r)V_{OL}^2-(7+1.4\beta_r)V_{OL}+6 = 0 \tag{3.6}$$

or

$$V_{OL} = \frac{7+1.4\beta_r-\sqrt{25-4.4\beta_r+1.96\beta_r^2}}{2(1+\beta_r)} \tag{3.7}$$

To see the dependence of V_{OL} on β_r, we may neglect the second order term V_{OL}^2 in (3.6) when V_{OL} is much smaller than V_{dd}=1V, thus

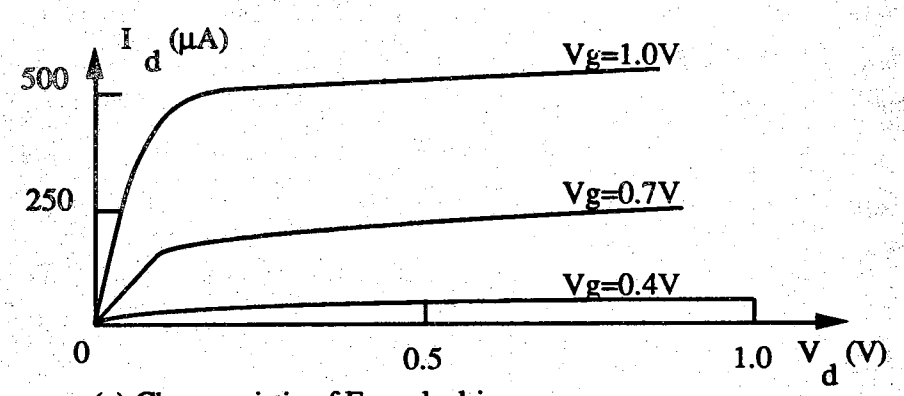
$$V_{OL} = \frac{6}{7(1+0.2\beta_r)} \tag{3.8}$$

This expression clearly shows that a bigger β_r will lead to a lower V_{OL}. Given V_{OL}=0.1V, a typical value of $\beta_r \approx 40$ can be calculated by (3.6). Thus a variety of β_r values from 25 to 50 were chosen for the test chip.

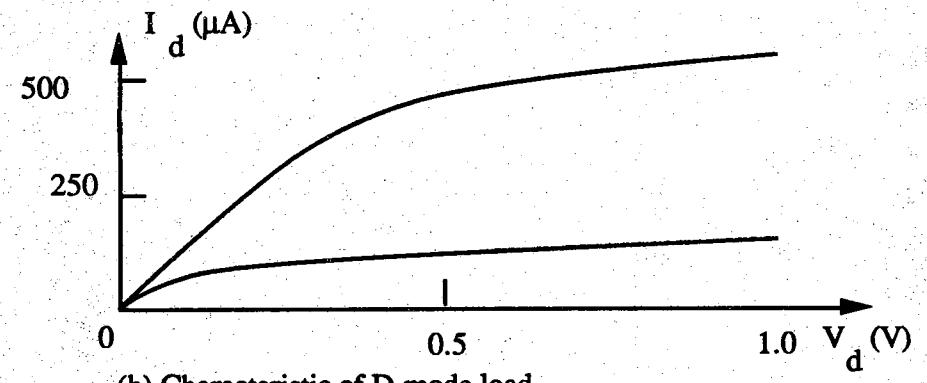
When we calculate β_r, we assumed $C_{2d}=C_{2l}$, i.e., the capacitances of the E-mode and D-mode devices were supposed equal. Strictly speaking, this is not true. The gate regions of the E-driver is recessed more than that of the D-loads. This results in a different AlGaAs thicknesses, or different C_2 between the E-driver and D-load. Typical values for the AlGaAs thicknesses of the E-driver and unetched D-load are 400Å and 600Å, respectively, therefore $C_{2d}/C_{2l} \approx 3/2$. The real value of β_r should be about fifty percent larger than what we have calculated. For the etched D-load, this factor of difference between the real β_r and the calculated one would be smaller.

The DC transfer characteristic of an inverter can be analyzed graphically if both characteristics of the driver and the load are given. This is realized by superimposing the two I-V characteristic curves with the same current and voltage scale, as shown in Fig.3.4 (c). Note that the curve of the load from Fig. 3.4 (b) is flipped to the load line shown in Fig. 3.4 (c). By this way, it is very easy to determine if the inverter is properly designed. If the load is not resistive enough, as the dashed line in Fig. 3.4 (c), the left cross point of two curves for a given V_{gd} of E-driver will be too large, indicated by V'_{OL} in Fig. 3.4 (c). In other words, the output low voltage of the inverter formed by these two transistors will be too high. If a circuit is built using these inverters, it will not work since no operating points can be found for the inverters, as shown in Fig. 3.5 (a). A well designed inverter, as far as the DC characteristic is concerned, should have good operating points shown in Fig. 3.5 (b).

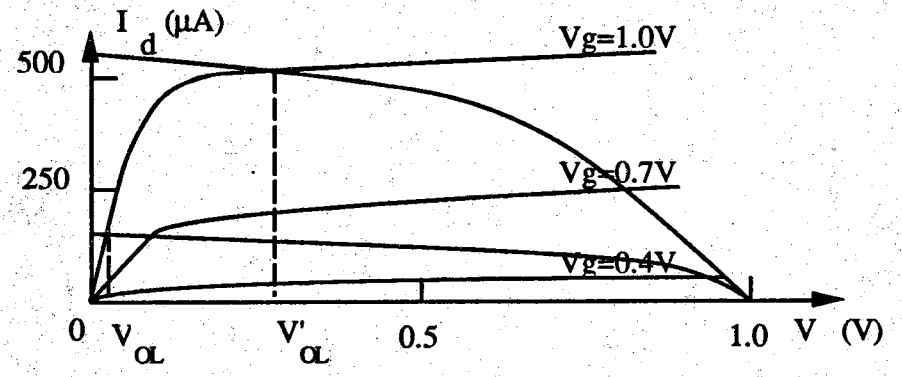
To make the load more resistive, two approaches can be taken. One is to increase the gate length of the load by choosing the large value of L_l (or βr), in case the W_d, L_d and W_l are fixed. The other way is to change the threshold voltage of the load, V_{thl} while L_l is kept relatively short. This can be explained by looking at the relationship between the V_{OL}



(a) Characteristic of E-mode driver.

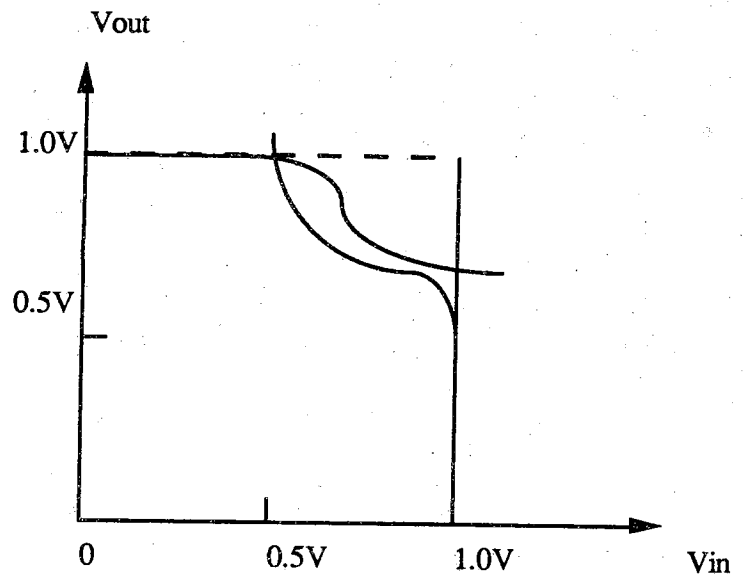


(b) Characteristic of D-mode load.

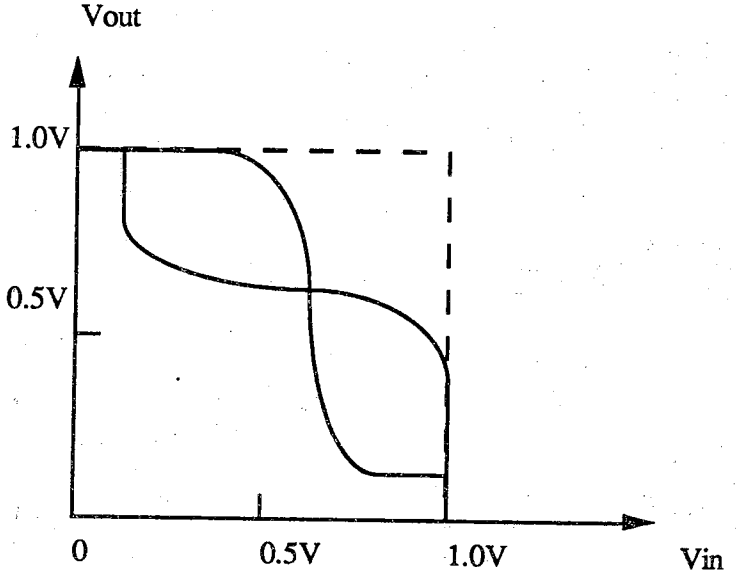


(c) Overlap of the two transistors of an inverter to find out the logic swing.

Figure 3.4 Characteristics of E-driver and D-load for an inverter.



(a) transfer characteristics of an inverter without operating points.



(b) transfer characteristics of an inverter with operating points.

Figure 3.5 Transfer characteristics of (a) without and (b) with operating points.

and V_{thl}. Differentiating (3.5), we have:

$$\frac{dV_{OL}}{dV_{thl}} = \frac{V_{dd}-V_{OL}}{V_{OL}+V_{thl}+\beta_r(V_{OL}+V_{thd}-V_{dd})} \qquad (3.9)$$

From the typical values given previously, $(V_{dd}-V_{OL}) > 0$ while both $(V_{OL}+V_{thl})$ and $(V_{OL}+V_{thd}-V_{dd})$ are negative. Thus

$$\frac{dV_{OL}}{dV_{thl}} < 0 \qquad (3.10)$$

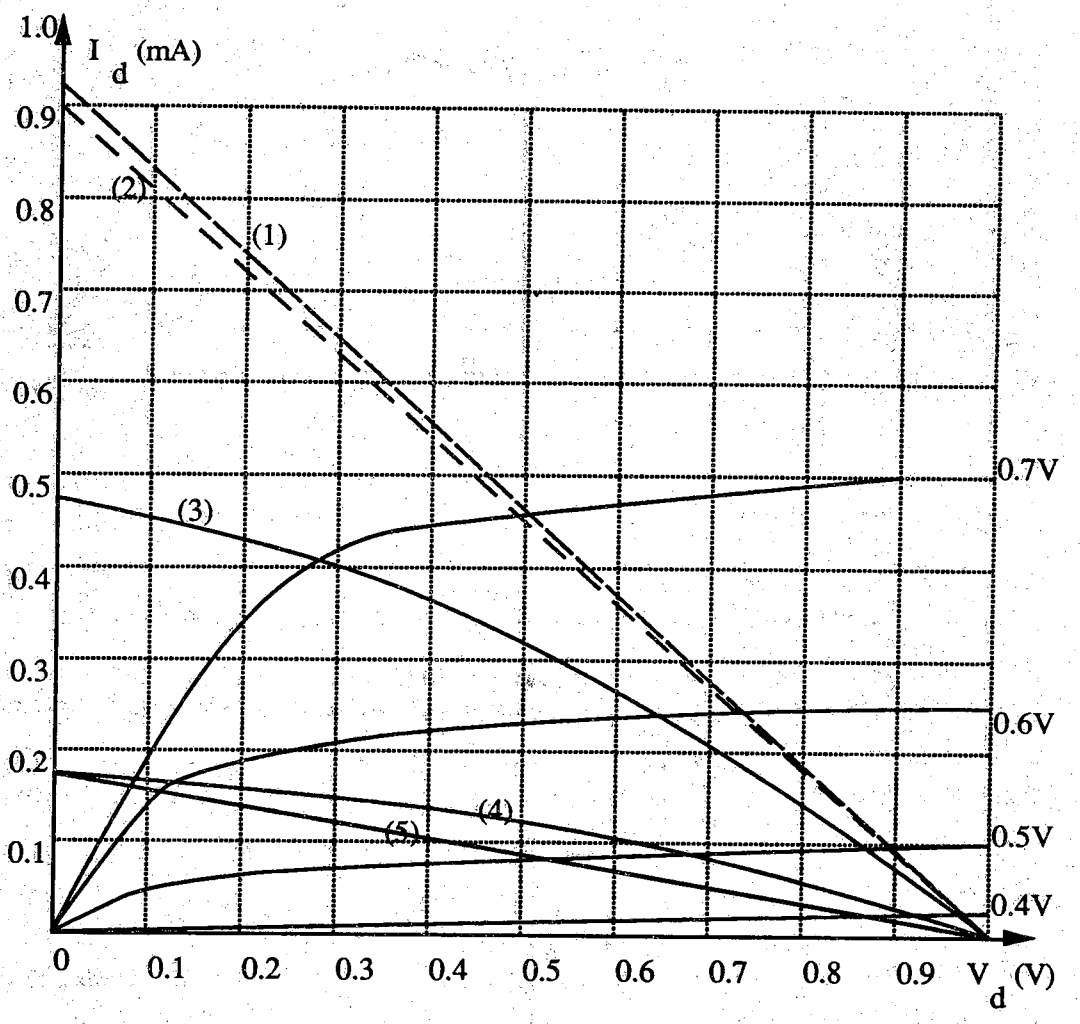
This means a less negative V_{thl} will cause a lower V_{OL}. Recalling the discussion of Chapter 2, V_{thl} can be increased by decreasing the thicknesses of the AlGaAs layer, t_2. Fig. 3.6 shows the experimental measurements of the change of load lines for various times of load recess etch, or equivalently, the various thicknesses of the AlGaAs layer.

It should be noted that to compare the two ways to determine the load for the inverter, the advantage of one is the disadvantage of the other. The long load is simple to process because a threshold adjust etch for the D-load is not required, and therefore one major process step, D-load recess etch, may be skipped. But this choice is poor in device area. The method of increasing threshold voltage of the load is good in saving area but bad in increasing the process complexity. An extra etching step, relative to the long load choice, must be added. It is especially bad if accurate control of V_{thl} is required by the design, remembering the trouble in control of threshold voltage across the wafer mentioned in Chapter 1.

Both types of load--etched and unetched loads were designed on the test chips. It is not difficult to calculate how much V_{thl} should be increased, or equivalently how much etching time should be taken, by equation (3.5) with β_r given. But a very simple and quick way is to look at the experimental results shown in Fig. 3.6. The line (1) shows the load line before any etch. The line (4) shows the load line after 26 second etch. The current of the load is reduced approximately five times after this etch. If the line (4) is accepted as a good load line for the driver shown in this figure, then the unetched load must be designed as the line (5) shown on Fig. 3.6 to have an equivalent logic swing. This implies that for the same V_{OL}, the current I_{dl} and the gate length L_l (or β_r) of the unetched load should be roughly five times that of the etched load I_{dl}^* and L_l^* (or β_r^*), respectively. This factor of 5 has been used to design the inverters with the etched loads for the test chip fabricated.

3.2.2 NAND and NOR logic gates

The circuits and logic symbols of three-input NAND and NOR gates are shown in Fig. 3.7 and 3.8, respectively. The truth table of NAND logic is shown by column Z_1 in



E-driver:
W/L=40/2, SD=5μm
D-load:
W/L=40/4, SD=10μm

Etch time:
line (1)..... <10 sec.
line (2)..... ≈18 sec.
line (3)..... ≈23 sec.
line (4)..... ≈26 sec.
line (5)..... unetched load

Figure 3.6 characteristics with load lines corresponding to different etching times.

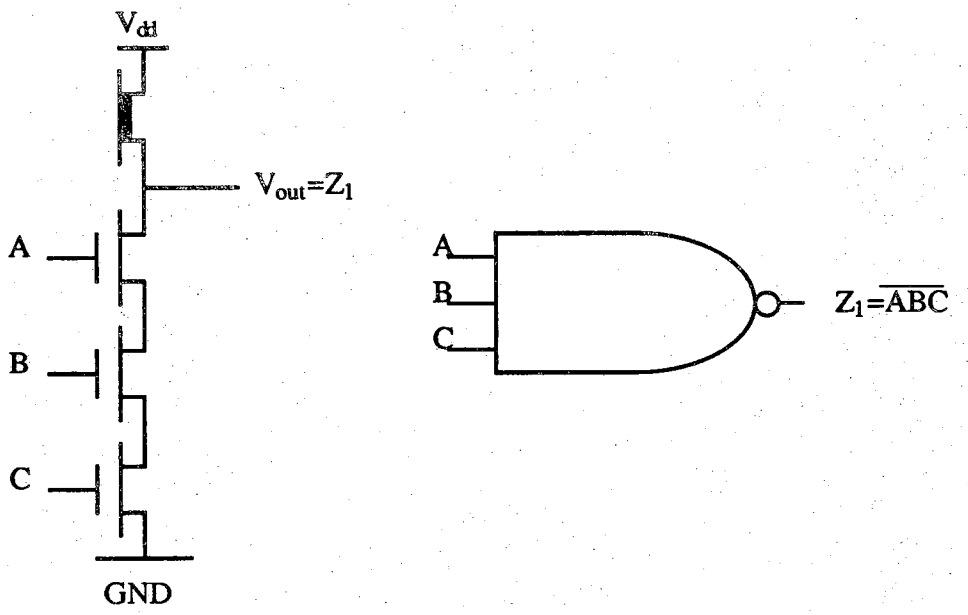


Figure 3.7 Circuit and logic symbol of three-input NAND logic gate.

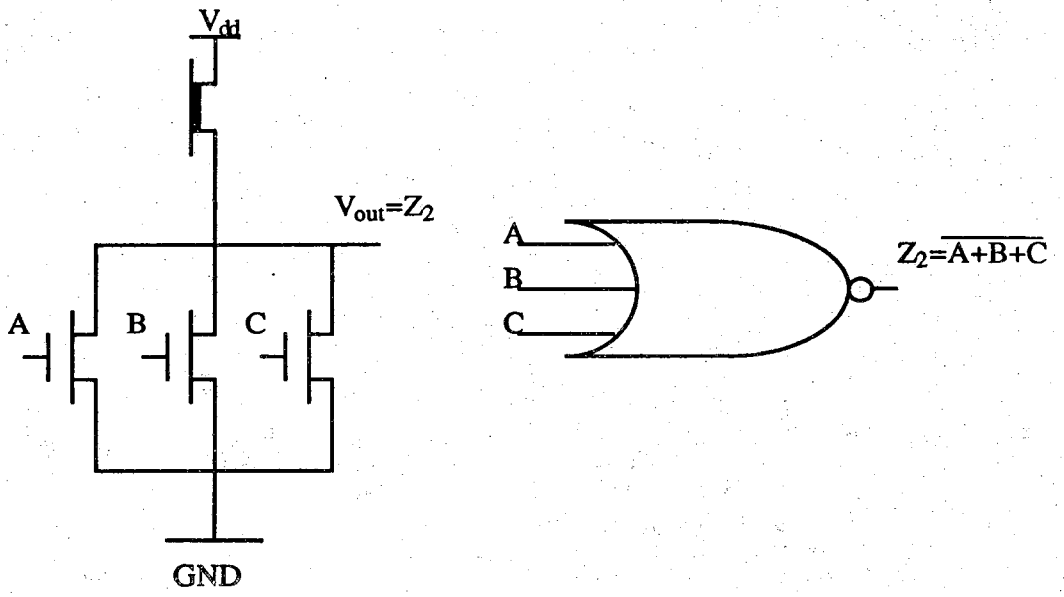


Figure 3.8 Circuit and logic symbol of three-input NOR logic gate.

Table 3.1 The truth table of 3-input NAND (Z_1) and NOR (Z_2) logic.

state No.	A	B	C	$Z_1=\overline{ABC}$	$Z_2=\overline{A+B+C}$
1	0	0	0	1	1
2	0	0	1	1	0
3	0	1	0	1	0
4	0	1	1	1	0
5	1	0	0	1	0
6	1	0	1	1	0
7	1	1	0	1	0
8	1	1	1	0	0

Table 3.1.

To analyze the DC characteristics of the NAND circuit, first note that $V_{OH}=V_{dd}$ is a good approximation. This is due to the use of a depletion-mode load, as discussed in the previous subsection. $V_O=V_{OH}$ occurs when any one or more inputs are low because the drivers are in series. If any one of the drivers is shut off, no current can pass from the supply V_{dd} to ground. Only when all inputs are high will the output V_O be pulled down to V_{OL} because the circuit is acting as an inverter. Three drivers with identical W over L ratio of 40/2, for example, can be treated as a single enhancement-mode driver with an equivalent $(W'/L')_d=40/3x2=40/6$. Suppose a β_r of 25 for the inverter with an unetched load or 5^* for the etched load is chosen, then $(L_l^*/L_d)=5^*$ or $L_l^*=30$ is chosen.

Similarly, the same procedure can also be applied to the analysis of the NOR gate. But three different cases must be considered for the calculation of V_{OL} this time: (a) one of the drivers is on, (b) two of the drivers are on, and (c) all three drivers are on. For each of these cases there exists a current path from the supply through the ground. Parallel drivers for the later two cases can be treated as a single driver with two or three times larger channel width equivalently. The details of the calculation of V_{OL} are skipped here. The results are summarized in Table 3.2. The function of the NOR gate is presented by the truth table of Table 3.1, column Z_2.

3.2.3 Ring oscillator

It is always important to know the speed of devices and the circuits. The propagation delay time t_p, the time spent to pass each inverter stage of the circuit, can be characterized

Table 3.2 Summary of design results for various circuits built on the test chip.

Circuit	I/O	E-driver (W/L)	D-load (w/L)			$\beta_r = \frac{\beta_d}{\beta_l}$
			Unetched	Etched	Gated	
Inverter	1/1	40/2 SD=6	40/50 SD=50		no	25
	1/1	40/2 SD=6		40/10 SD=10	no	5*
	1/1	40/2 SD=8	40/100 SD=100		no	50
	1/1	40/2 SD=8		40/20 SD=20	no	10*
	1/1	40/4 SD=8	40/120 SD=120		no	30
	1/1	40/4 SD=8		40/24 SD=24	no	6*
	1/1	40/6 SD=10	40/150 SD=150		yes	25
	1/1	40/6 SD=10		40/30 SD=30	yes	5*
NAND	3/1	40/2 SD=6		40/30 SD=30	no	5*(all three drivers "on")
NOR	3/1	40/2 SD=6		40/6 SD=6	no	3*(one "on") 6*(two "on") 9*(three "on")
	0/1	40/2 SD=6	40/40 SD=40		no	20(11 stages)
Ring Oscillators		40/2 SD=6 40/2 SD=6		40/8 SD=8 40/8 SD=8	no no	4*(11 stages) 4*(19 stages)

by testing the oscillation frequency of the ring oscillator. For this purpose, also for testing the yield of the MODFET process technology developed at Purdue, several ring oscillators with both etched and unetched loads have been designed.

A ring oscillator is constructed by cascading an odd number of identical inverter stages to induce oscillations, which may be measured at any input or output node. The oscillatory behavior of the circuit is achieved by the feedback provided in connecting the output of the final stage to the input of the first stage, as shown in Fig. 3.9. Two output stages are added for this MODFET ring oscillator design. The primary function of the output stage is to buffer the output signal without introducing a large capacitive load on the internal nodes. Thus the E-driver of the last inverter in the output stage is designed to have a doubled $(W/L)_d$ ratio, 80/2, than that of the rest of the inverters to increase the drive ability of the circuit.

The design of MODFET inverters, three-input NAND and NOR logic gates and ring oscillators with 11 and 17 stages have been done on the basis of the above discussion. The results are summarized in Table 3.2.

3.3 Process Overview

In this section we present a brief overview of the fabrication procedure, in order to explain the mask sequence. A detailed description of the processing steps will be given in the next chapter.

The bare wafer to start the MODFET fabrication process is shown in Fig. 3.10 (a). It is a single heterojunction (AlGaAs/GaAs), modulation-doped heterostructure grown by a Perkin Elmer molecular beam epitaxy (MBE) machine.

The first layer, undoped GaAs with thickness of 1 to 1.5 μm, is grown on a semi-insulating substrate. The 2DEG layer will be formed in this GaAs layer. Then a 100Å undoped AlGaAs is grown. This layer is named spacer layer because it is used to physically separate the 2DEG from the ionized impurity centers in the doped AlGaAs layer. There is a trade-off to choose the thickness d of the spacer layer, as mentioned in Section 2.3. A heavily doped n+AlGaAs is grown next. The doping density of this layer directly determines the carrier concentration of 2DEG, as shown in Fig. 2.5 in Chapter 2, therefore it is expected to be doped as heavy as possible, typically $10^{18}cm^{-3}$, by Si donors. The thickness of this layer depends on the device type. Usually 200Å and 600Å for enhancement- and depletion-mode devices, respectively, are chosen. The same thickness of AlGaAs are grown for all the devices on the same wafer and later recess etch

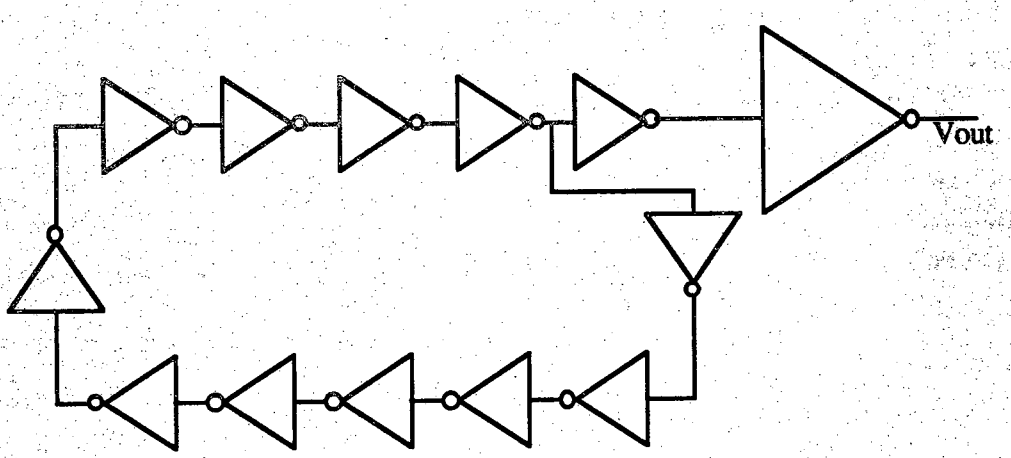
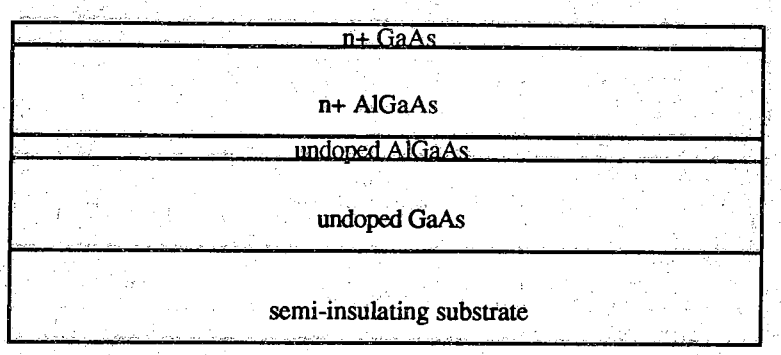


Figure 3.9 Logic diagram of an eleven-stage ring oscillator with two output stages.

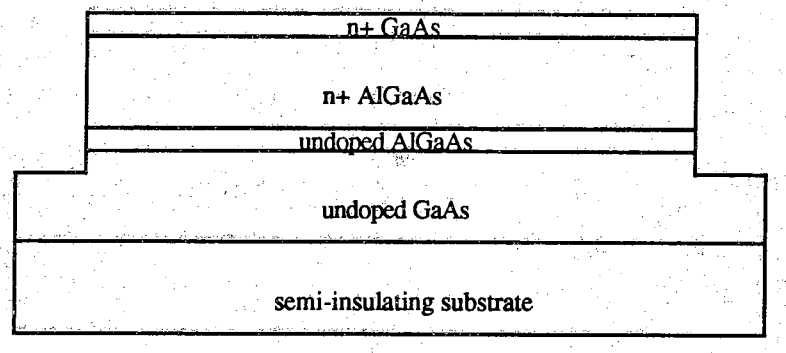
is performed for the E-mode devices. Finally, a very thin n+GaAs layer, normally from 50Å to 400Å, is grown on the top. This cap layer is used to protect the AlGaAs surface from being oxidized. The other purpose of this layer is to help the alloy contact to make a lower ohmic contact resistance in the source/drain areas.

Given the bare wafer described above, the first process step is device isolation. Since the 2DEG layer exists across the whole wafer, all of the devices built on the same chip must be isolated electrically from each other. This is done by a wet chemical etch, a process known as the mesa etch, as shown in Fig. 3.10 (b). The 2DEG channel is removed in the isolation areas when the etch passes all the way through the doped AlGaAs layer. The active areas, or mesas, on which the devices will be built, are defined by the mask and under the protection of the photoresist when the etch is performed.

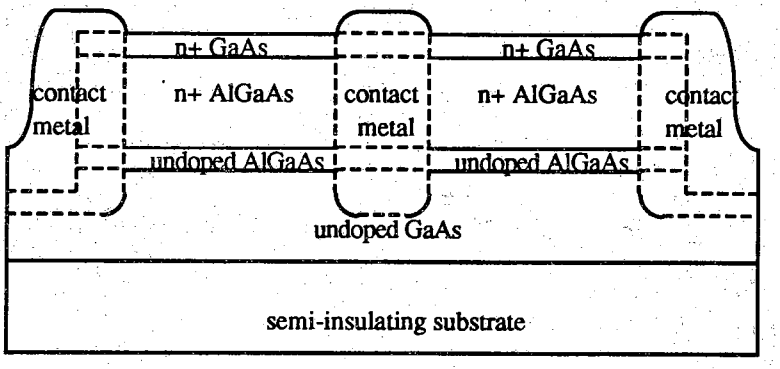
The Next process step is to form the source/drain of the device. The second mask is used to define the source/drain pattern. Metals are evaporated on the wafer surface in contact areas, with all other areas covered by photoresist. Then the photoresist is stripped, lifting off the metal and leaving metal in source/drain areas, as shown in Fig. 3.10 (c). This process is known as lift-off. The wafer is then annealed at a certain temperature (typically 450C-550C) to allow the metals to interact with the surface of the wafer. Thus a highly doped n+ region in contact with metals forms an ohmic contact to the 2DEG by electrons tunneling through the narrow barrier.(34)(38)(39)(40) There are two important requirements for this step. One is to minimize the source/drain access resistances, by



(a) MODFET film.

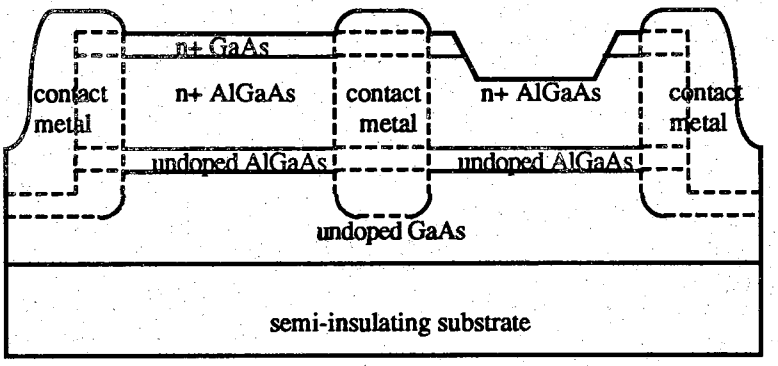


(b) mesa etch

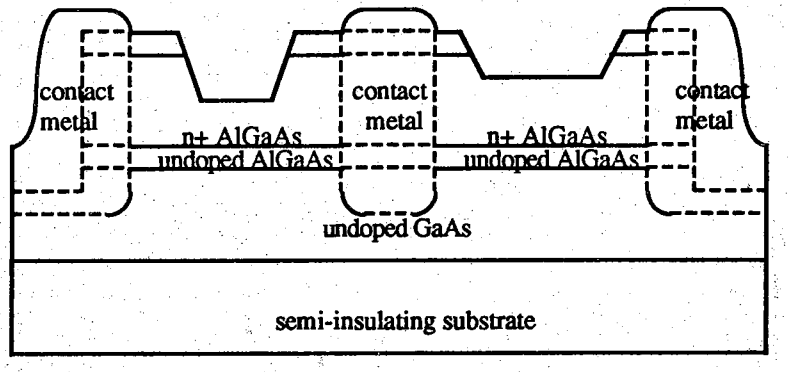


(c) source/drain formation

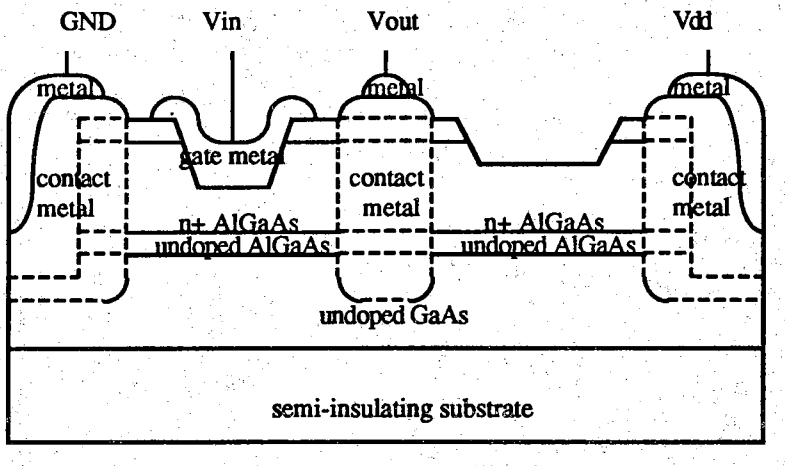
Figure 3.10 Cross section schemes of MODFET inverter process.



(d) D-load recess etch



(e) E-driver recess etch.



(f) gate and interconnect metallization.

Figure 3.10 (continued).

making the source/drain-to-gate spacing as close as possible. This spacing is limited by lithography of the gate pattern. A self-aligned gate process by ion implantation has been developed for this purpose.(15)(41) The other requirement is to minimize the ohmic contact resistance. The high contact resistance is the primary reason for low transconductance or poor device performance in MODFETs. The details of ohmic contacts will be discussed in Section 4.3 later.

Mask three and four are used to define the recess etch patterns, through which the etches are performed to control the threshold voltages of depletion and enhancement-mode devices, respectively, as shown in Fig. 3.10 (d) and (e). Both dry etch and wet chemical etch can be applied to fulfill this process. For the selective reactive-ion etch (RIE), a pre-calculated thickness of AlGaAs for both the enhancement- and depletion-mode devices are grown precisely including etch stopping layers. The etch will stop automatically at the specified layer. The wet etch is controlled by electrical monitoring of the drain current I_d. The uniformity control problem associated with the wet chemical etch will be addressed in the next chapter.

Finally, the metallization, mask level 5, is done by metal evaporation and lift-off. The gates, interconnects, and pads are formed by this step. The Schottky barrier heights of various metals making good Schottky contacts, such as Al, Au/Ge and pure Au, are almost the same, as will be discussed in Section 4.4. The metal must be thick enough to cover the mesa depth as well as for the purpose of bonding and testing afterwards. The finished cross section of an MODFET inverter with an etched ungated D-load is shown in Fig. 3.10 (e).

3.4 Mask Design

From the above discussion, five mask levels are needed for the MODFET test chip fabrication at Purdue. They are:

Mask #1 mesa etch

In contrast to all the other mask levels, this mask is designed to be light field, i.e., the background (isolation regions) is transparent while the features (active areas or mesas) are opaque. Therefore most areas of mask are clear. This allows the operator of the aligner to see the wafer below the mask easily. Since the MODFET wafer is usually small in area, this light field design makes it easier to adjust the wafer's position relative to the mask in order to make full use of the wafer's area. The AZ type positive photoresist is used for this MODFET fabrication. One alignment mark is designed on this mask so that the

patterns formed in the first level can be aligned to by the second mask through the mask aligner.

Mask #2 ohmic contact

The source and drain areas are defined by this mask. Three alignment marks are designed for all subsequent mask alignment.

Mask #3 recess etch for the depletion-mode device

This level is aligned to the ohmic contact pattern. Some windows on the source and drain regions must be opened to allow the probing for electrical monitoring during etch.

Mask #4 recess etch for the enhancement-mode device

This level is also aligned to the ohmic contact mask in order to define the recess notch right in the middle of source and drain. Windows similar to the mask #3 must also be designed on the mask for convenience of probing and monitoring.

Mask #5 Metallization

Alignment is an essential step for this mask. Spacing between the gate and source/drain area to tolerate the misalignment must be considered. Otherwise the gate will short to the source/drain areas by misalignment or other errors.

The dark field design of mask #2 to #5 makes alignment easy for the type of marks used, as shown in Fig. 3.11 (b).

The bonding pads are 100μmx100μm. The overall size of each of the two chips is 1395μmx1395μm. The pads of logic circuits are designed to be along the die boundaries for easier bonding and testing afterwards.

Several testing structures such as Greek-cross structure for carrier concentration measurement, Cross Bridge Kelvin Resistor (CBKR) for contact resistance measurement and MODFET capacitor for C-V measurement have also been designed on the test chip.

The overall layout of two chips, logic circuits and ring oscillators, are shown in Fig. 3.11 (a) and (b), respectively.

The layout file was created by CMASK graphics. The masks were made by a Cambridge Electron Beam Mask Fabrication system (EBMF system).

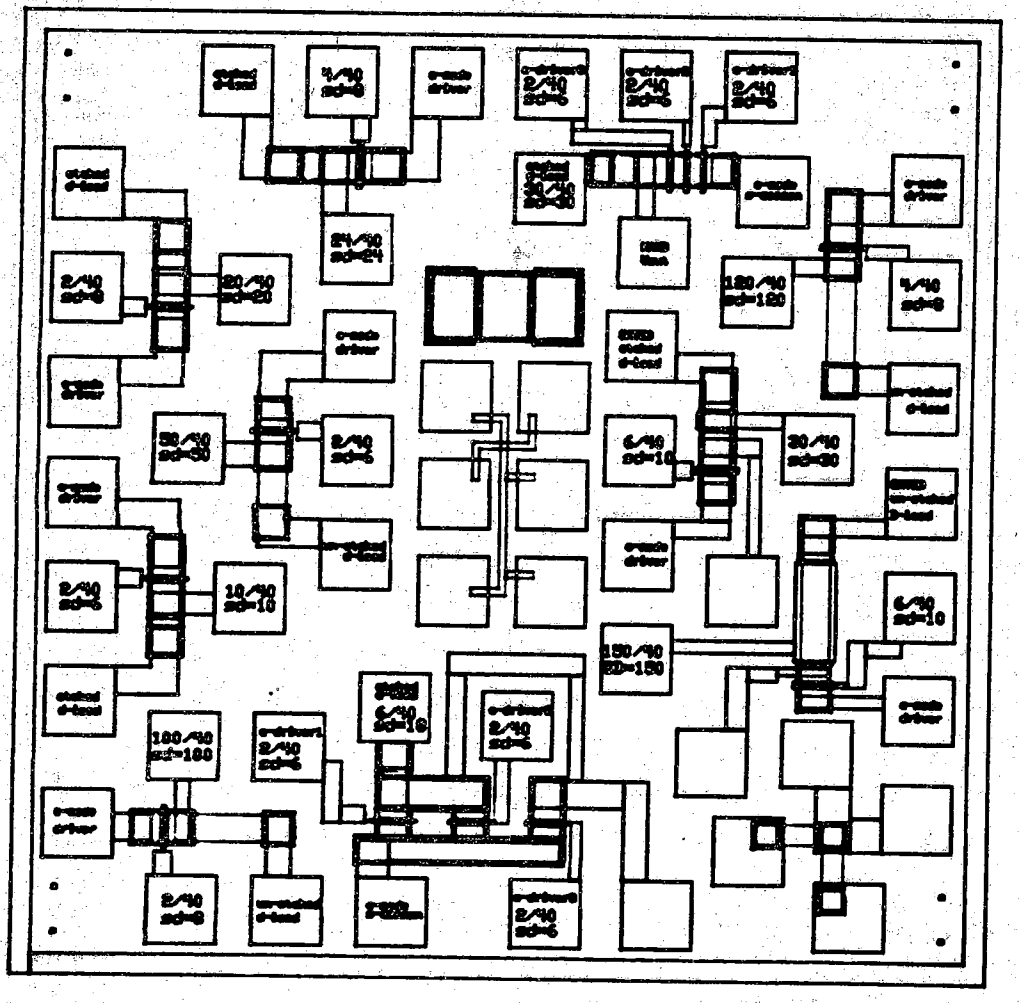


Figure 3.11 Layout of (a) logic circuit chip and, (b) ring oscillator chip.

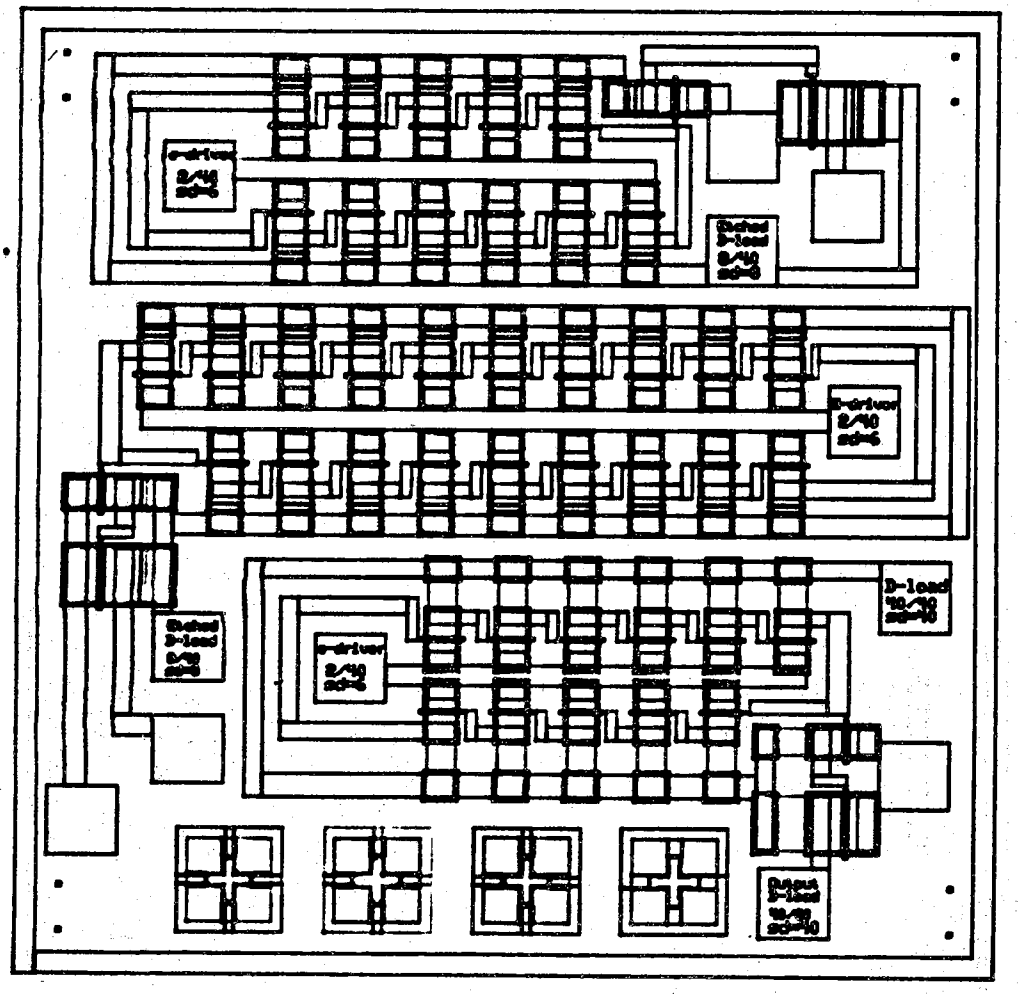


Figure 3.11 (continued).

CHAPTER 4

PROCESS DEVELOPMENT AND FABRICATION

The discussion of Chapter 3 gave an overview of the basic semiconductor processing steps employed in this MODFET fabrication. This chapter will give a full discussion on each of these fabrication techniques. The baseline of the MODFET process technology at Purdue has been primarily developed by Mark Whiteside.(33) Photolithography and lift-off will be discussed in Section 4.1. Section 4.2 will deal with the wet chemical etch and related threshold voltage control problem. A study of alloy contacts and some experimental results will be presented in Section 4.3. Metallization will be discussed in Section 4.4. Finally, a summary of the process developed at Purdue will be presented in Section 4.5.

4.1 Photolithography and Lift-off

As mentioned in the end of the last chapter, five mask levels are used for this fabrication process. For levels #1, 3 and 4, that is mesa and recess etches, several basic steps, such as wafer cleaning, resist application, soft baking, mask alignment, ultraviolet (UV) light exposure and photoresist development, hard baking, and resist removal, are involved. For levels #2 and #5, however, a special technique, known as lift-off, is used to define metal patterns on the wafer surface without metal etch.

The device dimensions are primarily limited by optical lithography. The minimum linewidth reliably produced by optical lithography is $\approx 2\mu m$, therefore the minimum "gate length" (the length of the recess notch) for the MODFET test chip is designed as $2\mu m$. The actual metal gate length is $3\mu m$. The minimum source/drain distance is chosen to be $6\mu m$, with $1.5\mu m$ spacing between the gate and source/drain area for tolerance of possible misalignment and other errors. If a much smaller device size is desired, a new lithography method must be developed. One prominent candidate for MODFET lithography is electron beam (E-beam) lithography, which is able to produce a gate length as small as $0.1\mu m$. With this gate length, the device size will be reduced dramatically.

As mentioned in Chapter 3, the lift-off technique allows metallization after resist exposure and development. The key requirement for this technique is to form an undercut profile after resist development. Metals can then be evaporated over the entire surface, and a discontinuity is maintained between the metal on the wafer surface and the metal over the photoresist. Upon removal of resist, the metal over the resist is removed and a faithful reproduction of the metallization pattern is obtained.

The optical AZ-1350J positive photoresist is used for all lithography steps of this process. To create the required undercut profile on the single layer of the UV-light exposed AZ photoresist, a chlorobenzene-soak process[42][43][44][45] is used.The steps of this process are almost the same as the normal lithography except that to make the resist thicker and softer, a lower spin speed, shorter spin time and lower soft baking temperature are intentionally used. Also instead of hard baking, the resist is soaked in chlorobenzene for 14 minutes. This soak is believed to remove residual solvent and low-molecular-weight resin and thereby create a dense surface layer less susceptible to developer's attack. Then the development of the soaked resist goes fast laterally below the hardened surface layer, therefore the desired profile is produced. The process should be optimized by choosing the proper times of resist spin, soft bake, exposure, chlorobenzene soak, and development as well as the spin speed and bake temperature. These data developed at Purdue for the Suss aligner are summarized in section 4.5 and the Runsheet in Appendix.

4.2 Wet Chemical Etch

In this MODFET fabrication, three different types of etches are to be performed for different purposes or requirements. These etches are:

(a) mesa etch, which is used to isolate all of the devices electrically on the same wafer from each other. The barrier materials are both AlGaAs and GaAs.

(b) oxide etch, which is used to guarantee good contact between the metal and wafer surface before evaporation. The barrier material is AlGaAs oxide.

(c) recess etch, which is used to control the threshold voltage for both enhancement mode and depletion-mode devices. The barrier material is AlGaAs only.

The solution for mesa etch is $1H_2SO_4$:$1H_2O_2$:24D.I. H_2O. For the purpose of electrical isolation, at least the layers of n+ GaAs, and n+ AlGaAs must be removed, as shown in Fig. 3.10 (b). The thickness of these layers add up to about 2000Å for the film used at Purdue. But for ease of subsequent mask alignment, a mesa depth of around 4,000Å is required. Otherwise it would be difficult to see the defined pattern and alignment mark through the mask aligner.

The etch depth is controlled by the etch time, knowing the etch rate, which is about 50Å/second for the etch solution mentioned above. This rate may vary from time to time since it depends on several factors such as the temperature and the age of the solution after it is prepared. A calibration on an expendable wafer is recommended before etching. However, there is no substantial requirement for mesa depth, as long as it is deep enough to isolate the devices and make it easy to see the patterns and alignment marks under aligner. Thus it is not essential to calibrate the mesa etch every time. After the etch and photoresist removal, the depth is measured by the Tencor Alpha-step profilometer.

Obviously, the disadvantage of a mesa etch is that it is not a planar process. To achieve a planar surface, ion implantation can be used to replace the wet etch.(2) The 2DEG is eliminated when the crystal lattice is destroyed by ion implant. But ion implantation introduces additional complexity to the process.

The solution for oxide etch is $1NH_4OH$:40DI H_2O. One of the two oxide etches for the MODFET is used to remove the oxide layer before the contact alloy metals are evaporated. As we have discussed earlier, lowering contact resistivity is very important for the improvement of the device performance. The insulating oxide layer must be removed to insure a solid contact between the metals and the wafer. The other oxide etch is performed before the gate metal is evaporated. Immediately after oxide etch, the wafer must be loaded into the evaporation chamber which is pumped down promptly. If the wafer is left in air for more than half hour or so without being loaded into the chamber, the oxide etch should be redone before loading because a new oxide layer may have been grown.

Finally, the threshold voltage control through recess etch is a critical consideration for the MODFET process. As discussed earlier, the recess etch is done by monitoring the drain current. The etch is stopped when the target current is met. For example, to build an enhancement-mode device of (W/L)=40/2, distance between source and drain SD=6μm, and threshold voltage V_{th}=0.4V, the proper current (assuming drain voltage V_d=1.0V) is about 5μA. This value is found by trial and error in the process of previous runs. The task is tough since, as shown in Fig. 4.1(46) the sensitivity of V_{th} on the AlGaAs thickness t_2 for a typical AlGaAs doping of $2x10^{18}$ cm^2 is 6mV/Å. To achieve a very modest uniformity of 300mV in the lab, the equivalent depth of recess etch must be controlled better than 50Å! From the calculation of (2.27) and (2.34) in Chapter 2, a relationship of n_s vs. t_2 can be plotted, as shown in Fig. 4.2.(47) The 50Å change in t_2 corresponds to a seven times change in n_s, or equivalently in I_d (assuming mobility μ is a constant). The actual situation was even worse because of the unstable property of the

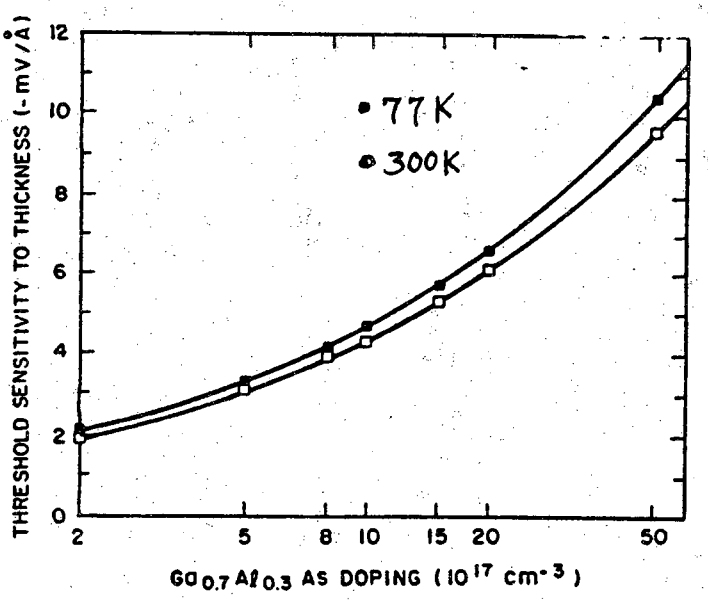


Figure 4.1 Sensitivity of threshold voltage V_{th} versus thickness of AlGaAs, t_2.(46)

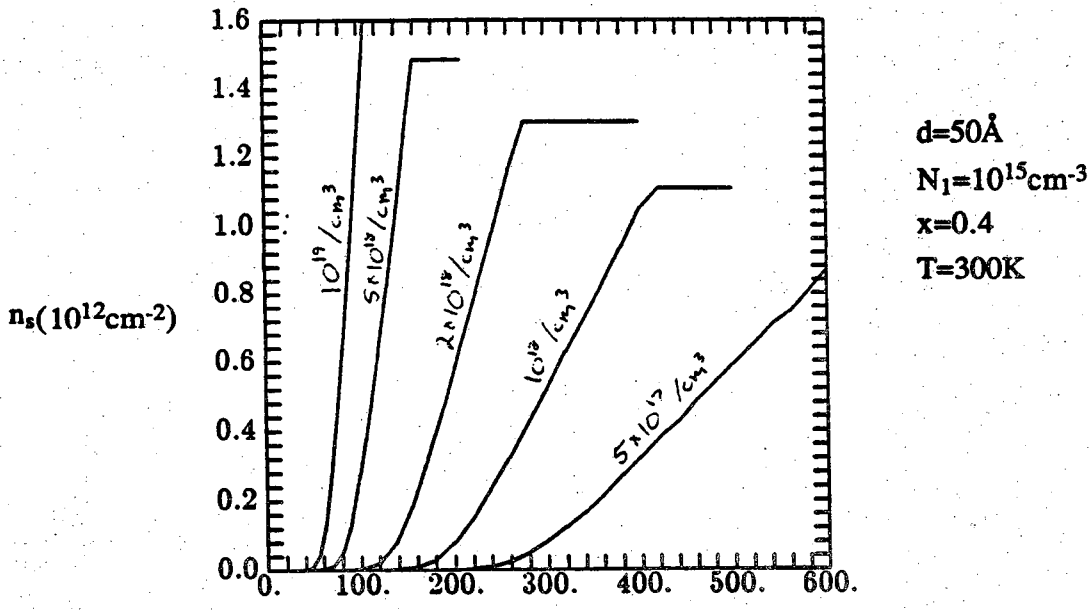


Figure 4.2 Sensitivity of 2DEG carrier concentration n_s vs. thickness of AlGaAs, t_2.(47)

etch solution. The original etch solution used was $3NH_4OH:1H_2O_2$:1500DI H_2O whose etch rate was about 4Å/second. With the solution agitated by hand, two orders of magnitude difference in drain current I_d were found for different devices across the wafer with same sizes. This large deviation of uniformity makes it extreme difficult to control the threshold voltage by electrical monitoring. This poor result is believed due to the instability of the solution made of NH_3 and H_2O_2. Both are volatile and the latter is very unstable at room temperature. In addition, the etchants are not dissolved and distributed uniformly throughout the whole solution when it is agitated by human hand.

Definitely, a more reliable etch recipe and tighter etch operation procedure had to be developed. The new solution is just to dilute the mesa etch solution to $2H_2SO_4:1H_2O_2$:500D.I. H_2O because both etches have the same barrier material: AlGaAs. The etch rate of this new solution is measured as 2.2Å/second. The H_2O_2 is still used as the active agent to oxidize the AlGaAs. The volatile NH_3 is replaced by H_2SO_4. Additionally, the solution is agitated smoothly and uniformly by magnetic agitating machine. The new etch solution and mechanical agitation reduce the spread of I_d and brings the recess etch under control. Besides, the slower etch rate of the new solution than that of the previous one enhances the former's advantage to avoid overetch. The current drops dramatically when the etch for the enhancement-mode device is nearly done, as shown in Fig. 4.3. Hence a slower etch rate will make control of the etch easier.

The curve in Fig. 4.3 makes sense physically. The current I_d in that figure is actually the zero-gate-bias drain current $I_d(Vg=0)$ for a fixed drain voltage V_d=1.0V. Figure 4.4 (a) shows the entire curve of I_d vs. various gate voltage Vg. Before the device is totally turned on, $(I_d)^{1/2}$ starts from zero (neglect the subthreshold current) and increase slowly when Vg is increased. After the device is completely turned on, $(I_d)^{1/2}$ becomes linear with Vg for most of the region because the square law of I_d vs. (Vg-Vth) takes over. After Vg is increased further, the gate leakage current and source/drain access resistance in series will come into play, therefore the drain current I_d is limited and its increase rate comes down again. Physically, this corresponds to a situation where the 2DEG contains the maximum electron density which the AlGaAs barrier can contain, and any additional electrons leak to the gate.

Before any etch, suppose the AlGaAs layer is thick enough (as the actual film processed at Purdue) so that the threshold voltage is quite negative, as shown in Fig. 4.4 (a). After the etch is started, the thickness of AlGaAs t_2 is decreased continuously. Consequently the threshold voltage becomes less and less negative. The curve will be gradually shifted from (a) to (b), neglecting the effect of t_2 in drain current. During this

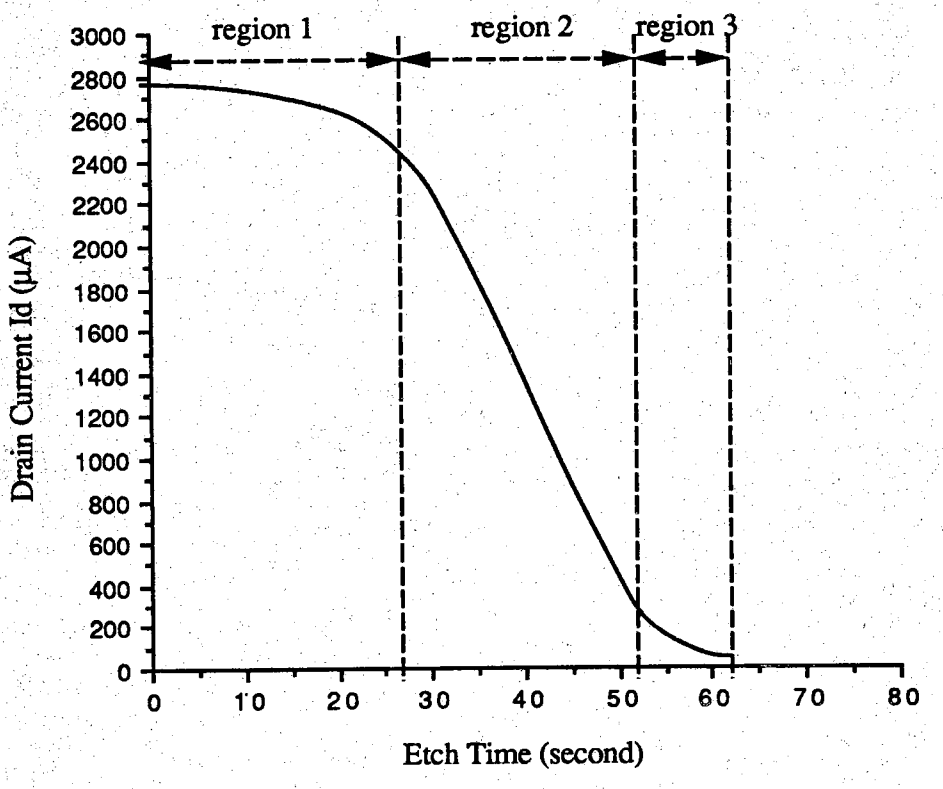


Figure 4.3 Measurement of drain current I_d vs. etch times (ungated D-mode device: W/L=40/8, V_d=4V).

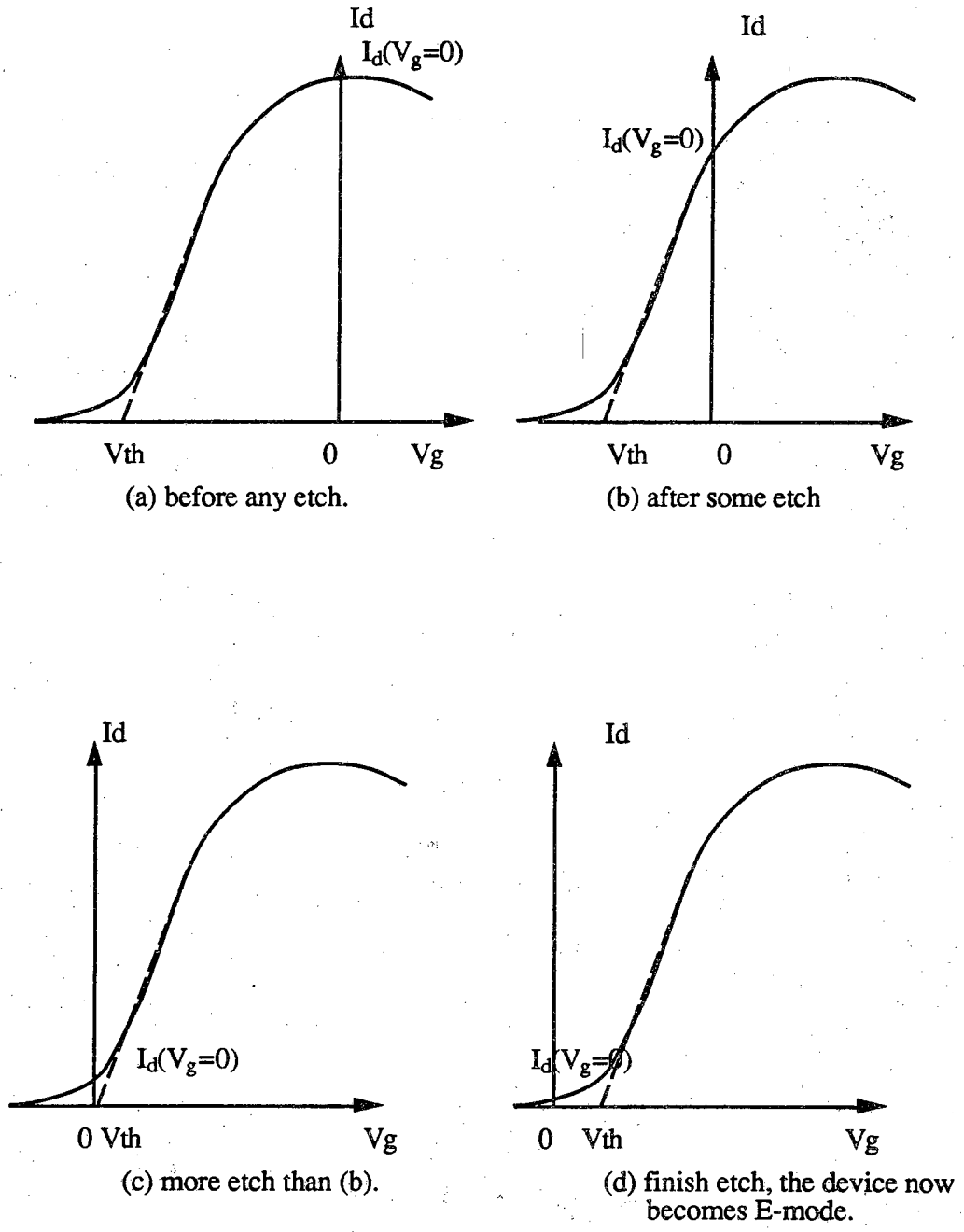


Figure 4.4 Curve of I_d vs.Vg changes with different recess etch times.

period, the current I_d(Vg=0) (the cross point between the I_d-Vg curve and the vertical axis Vg=0) is changed little, since the I_d for large Vg in Fig. 4.4 (a) is almost saturated. This corresponds to region 1 in Fig. 4.3. When further etching is performed, the linear region in Fig. 4.4 (b) will take over and a huge drop will occur from (b) to (c) in Fig. 4.4. This period is represented by region 2 in Fig. 4.3. Finally, when the etch is performed further from Fig. 4.4 (c) to (d), the drop of I_d in Fig. 4.3 will naturally slow down again because now the tail of the curve in Fig. 4.4 (c) is passing across the vertical axis Vg=0. Around this region, the device will be changed from depletion-mode into enhancement-mode.

Even though the new recipe for etch seems better than the old one, it is still desirable to look for a better technology. Recently, a pH controlled wet etch has been reported.(11) It was suggested that the pH monitoring of the solution is a very helpful way to control the wet etch. The other method that is also widely used is the selective reactive ion etch (RIE), which offers a very sophisticated way to control the etch accurately and uniformly. More details of this method and related calculations will be discussed in Chapter 6.

4.3 Ohmic Contact

Ohmic contact is another critical stage of fabrication. Unlike the situation in the MOSFET, whose contact is made to the channel at the semiconductor's surface, the contact of the MODFET must be made to the 2DEG channel through a few hundred angstroms of AlGaAs layer.

Before the contact is made, the band diagram is as shown in Fig. 4.5. The electron transport from the surface to the 2DEG is limited by three series components: the two-heterojunction barriers which are formed by (n+ GaAs)/(n+ AlGaAs) and (n+ AlGaAs)/(undoped-GaAs) on the two sides, respectively, and the depleted AlGaAs layer in the middle. Calculation shows that such a structure does not meet the requirement of linear characteristic and small resistivity.(2)(39)

One way to achieve the low-resistivity-contact is to fabricate a contact area which is very highly doped from the surface through the 2DEG by metallic material. The 2DEG will be destroyed both in the contact area and a zone extending approximately one Debye length around the periphery. However, an accumulation layer of excess electrons, parallel to the surface, will be formed right in this area. Thus an unbroken conductive path, vertically downward by tunneling through both n+ - n+ heterointerfaces mentioned above and horizontally via the accumulated zone to the undisturbed 2DEG, is formed from surface contacts to the 2DEG. The contact resistance will then consist of four parts: the metal-semiconductor contact to the cap layer, tunneling through the two n+-n+

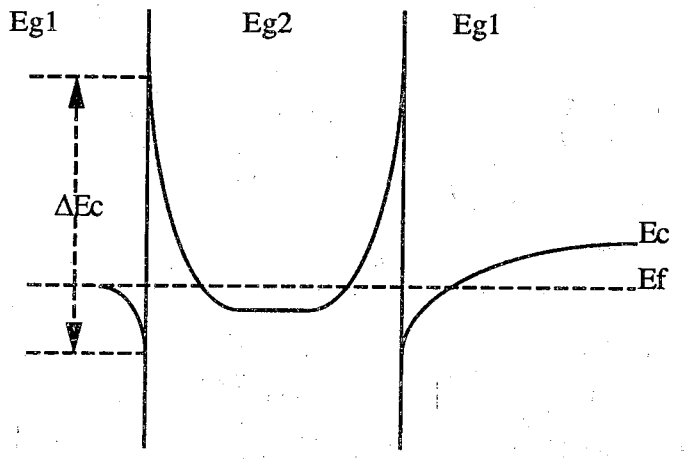


Figure 4.5 Heterostructure energy band diagram.

heterojunction interfaces, and ohmic conduction through the accumulated region. Usually only the first term contributes primarily to the contact resistance. This is due to the facts that the accumulation has a high carrier concentration and the heights of the two heterojunction barriers are about half that of a typical Schottky barrier formed by the first term. Thus the contact of metal to the MODFET 2DEG becomes similar to the conventional ohmic contact to a bulk n+ material.

To realize the above ohmic contact, either ion implantation or metal alloy may be used. The later is chosen for our process for simplicity. First, the metal pattern on the wafer surface is defined by evaporation and lift-off. The oxide on the surface of the contact area must be removed before evaporation, as discussed in Section 4.2. After lift-off, the wafer is heated to a high temperature for a few minutes to allow the metals to interact with the heterostructure system.

The metallization materials chosen for alloying are important. The chemical reaction occuring during the heat treatment of the contact is very complicated and not totally understood yet. Most of the ohmic contacts are made on the basis of the Au/Ge eutectic system with some additional materials like nickel (Ni) and titanium (Ti). A simplified model to explain the alloy process for the Au/Ge eutectic is as follows. The Au/Ge deposited on the wafer surface in the contact area melts when the wafer is annealed above the lowest melting point of the Au/Ge combination (≈360C for 12% Ge:88% Au). The GaAs then dissolves in this eutectic system. Upon cooling, the GaAs will come out of host semiconductor atoms, Ga, and their lattice sites.

Ni is found to lower the surface free energy of the molten metal alloy and therefore enhance the spread of molten Au on the surface. Ni is also found to increase the solubility of Ga in the melt during alloying. This results in an increase in Ga vacancies and hence a higher Ge doping density in the semiconductor. Ni is also a fast diffuser in GaAs. This directly enhances the n+ doping of the alloy area and lowers the resistance.(38)

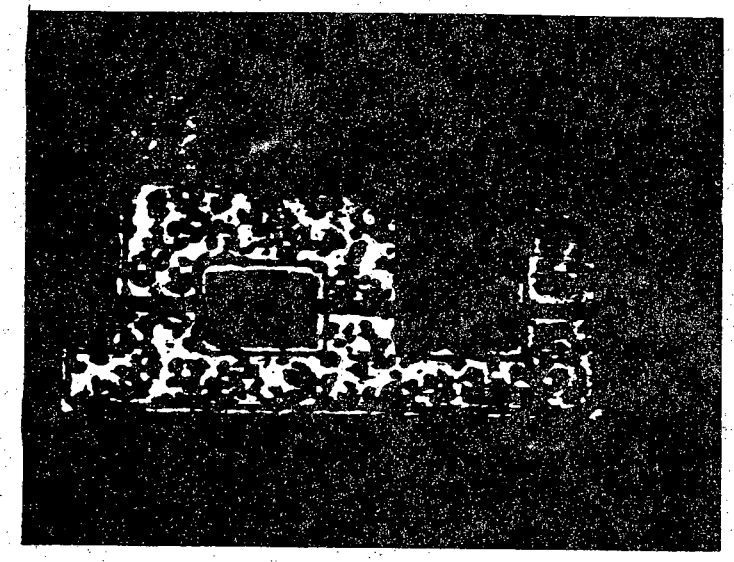
The alloy cycle is another important factor to achieve good contact. For the MODFET process, an alloying temperature of 400C or higher is necessary.(48) But temperature higher than 650C is usually not desired for conventional alloy because of two recognized problems: formation of metal globules on the surface, and formation of a AuGa intermetallic compound, which will lead to a poor contact interface and excessive strain at the contact region.(49) Temperatures as high as 850C have been reported for transient alloy.(49) The desired alloying temperature for the Au/Ge based system is in the range of 450C to 600C.

The alloy temperature with its associated time must be optimized for good device performance. A "sequential alloying" technique for this purpose has been proposed by Eastman et al.(40) In this method, an expendable sample with the metal evaporated and defined is alloyed at a starting temperature (450C) for about 100 seconds. After measuring the contact resistance, the temperature for alloy is increased and the wafer is realloyed. This sequence is repeated until a maximum temperature, 580C for their case, is reached. The temperature at which the minimum contact resistance occurs is the optimum temperature for subsequent device ohmic contact.

Two different types of evaporators have been used for MODFET ohmic contacts at Purdue. Using a Varian e-beam evaporator, a multilayer structure chosen according to the results of O'Connor et al.(39) has been developed. The structure is listed below.

Ni	50Å
Ge	500Å
Au	1000Å
Ni	300Å
Au	300Å
Ti	1000Å
Au	2000Å

The Ni is added to achieve a nice and smooth contact surface. A comparison of two surfaces alloyed with and without Ni is shown in Fig. 4. 6. The final Au layer is used to



(a) rough surface with Au/Ge alloy.

(b) smooth surface with multilayer structure.

Figure 4.6 Comparison of surfaces alloyed (a) with and, (b) without Ni.

get better conductivity and a smooth surface to be covered by interconnect and pad metallization.

The other machine used at Purdue is the NRC filament evaporator. Au/Ge is evaporated for the alloy contact but the thickness of metal evaporated is not well controllable except a rough estimation by the number of Au/Ge pellets used.

To compare the effects of different metallization systems deposited by different evaporators, using different alloy temperatures with and without a thermal quench, a simple and interesting experiment has been conducted in the lab. Five pieces cut from the same wafer were prepared. Their contact resistances were measured after they were alloyed through different cycles. The results are listed in Table 4.1.

It has been reported that rapid cooling is felt to be important for the production of contacts with low resistivity and high reliability.(50)(51) To investigate this, two pairs of samples were prepared. One of each pair was quenched on a cool metal block immediately after it was annealed at high temperature while the other was not quenched but allowed to cool down to room temperature slowly. The two pairs were alloyed at two different temperatures, 450C and 600C, respectively. Several observations can be obtained from Table 4.1.

For both temperatures, the contact resistances of the quenched samples, #7 and #5, in each pair, #6/#7 for 450C and #3/#5 for 600C, are clearly smaller than that of its counterpart, the nonquenched samples, #6 and #3, respectively. The rapid cooling procedure is thought to reduce the factors, such as irregular alloying and dislocation formation which is caused by the stress at the interface between reactants and substrate semiconductor, that lead to poor ohmic contact.(52)

As for the comparison of different metal structures, samples #4 and #7 are alloyed by NRC filament evaporator and Varian e-beam evaporator, respectively, while other conditions are kept the same. A better result is obtained from the Varian than the NRC. This is partly due to the Ni layers added to the multilayer structure of sample #7. This conclusion agrees with the previous discussion about the positive role played by Ni in alloying.

As far as the alloy temperature is concerned, unfortunately no consistent conclusion can be drawn. For the quenched pair of samples, #5 and #7, the results seem to favor 600C as alloying temperature, wheres the opposite conclusion can be seen from the nonquenched pair, #3 and #6, which suggests that the better temperature should be 450C. This fact implies again that the quench, or rapid cooling procedure, plays an important role during the formation of ohmic contact by alloy.

Table 4.1 Comparison of alloy contact through different alloy cycles.

Cycle	#3	#4	#5	#6	#7
Evaporator	Varian	NRC	Varian	Varian	Varian
Temperature	600C	450C	600C	450C	450C
Quench ?	No	Yes	Yes	No	Yes
Alloy time	1 min.	4.4 min.	1 min.	4.4 min.	4.4 min.
ρcmin. ($x10^{-5}\Omega$-cm^2)	55.0	20.3	5.5	52.04	26.59
ρcave. ($x10^{-5}\Omega$-cm^2)	372.1	82.9	12.3	144.6	64.4
ρcmax. ($x10^{-5}\Omega$-cm^2)	670.0	273.6	19.0	320	120.5

Comparing the results of all samples, the lowest contact resistivity is found with sample #5. This suggests that the optimum alloy cycle should include a combination of several techniques, such as an optimized multilayer metal structure, quench procedure together with appropriate alloying temperature and time, etc.

4.4 Gate Metallization

In contrast to the ohmic (linear and low resistivity) contact discussed in the last section, a Schottky (rectifying) type contact must be made between the metal gate and AlGaAs.

The primary object to choose a "good gate" is to choose a metal with a high Schottky barrier height. But for the majority of metals, this height is almost a constant with respect to the semiconductor AlGaAs due to Fermi level pinning[32]. Thus some other criteria, such as stability and resistance to interdiffusion during device operation, reasonable ductility to allow wire bonding, and adherence to the GaAs surface, must be considered. In reality, it is difficult to find a metallization that satisfies all these conditions. Thus multilayer metallizations have been widely used to seek the optimum metal system to meet the above demands.

Both Al and Ti/Au have been used for MODFET gates at Purdue. The NRC filament evaporator is used for deposition of Al gates. The disadvantage of this method, as mentioned in the last section, is that the thickness of the gate can not be controlled accurately. This is a more serious problem for metallization here than for the contact

deposition because of the existence of a mesa step. If the thickness of Al film evaporated is not enough to cover the mesa depth of 4000Å to 5000Å, open circuits between pads or interconnects and the gates or contacts will occur. Unlike the situation in metal defined by etch techniques, where at least a precaution against possible open circuits can be taken by depositing thicker metal, the lift-off technique requires a relatively thin metal layer to make sure the discontinuity does occur between the metal that will be maintained on the wafer surface and the metal that will be lifted off.

The thickness of each layer of the Ti/Au double layer system evaporated by the Varian e-beam evaporator, on the other hand, can be controlled quite precisely by a crystal monitoring system. The total thickness of Ti and Au is designed to be 4500Å, which is thick enough to cover the mesa height.

A relatively thin layer (500Å) of Ti is used below the Au layer because, on the one hand, the Au/GaAs interface would interdiffuse and degrade at a relatively low temperature, 250C, if only Au is used. Considering that the devices have to operate at elevated temperatures, this could be a big problem. In addition, Au in GaAs would produce deep levels which would degrade device performance. However, on the other hand, Au is an ideal choice from considerations of rectification, bonding, thermal heat sinking, and resistance to chemical attack. To eliminate the disadvantages of the Au/GaAs interface and while making use of the advantage of Au as metal, a layer of Ti is included between the Au and GaAs.

4.5 Summary

With all the information and experimental results discussed in the previous four sections, the final process steps of MODFET circuits at Purdue have been developed and summarized as follows. The process runsheet is attached in Appendix B. SEM photographs of the MODFET after major process steps are shown in Fig. 4.7.

First, a bare modulation-doped heterojunction MODFET film grown by MBE, as shown in Fig. 3.10 (a), is obtained. The n+ AlGaAs layer of the wafer is thick enough (600Å) so that those devices fabricated without any gate recess etch would be depletion-mode with threshold voltage of ≈-3.1V. For convenience of handling during process, the film is mounted on a larger piece of silicon wafer soldered by indium. The soldering is done on a heated hotplate. The MODFET film should be mounted as parallel as possible to the Si surface; otherwise it will cause difficulties for subsequential alignment under the microscope of the aligner. Another caution is that neither indium spots on the surface of the MODFET film nor spare indium higher than the surface of the film around the

MODFET wafer is allowed. The former will lead to low circuit yield. Both will damage the masks which are tightly contacted to the film during alignment with the Karl Suss model 123 mask aligner used at Purdue.

Next, a standard lithography procedure is followed. The sample is prebaked at 120C for 15 minutes to dry the surface for a better adhesion between the wafer and the photoresist that will be applied next. After the wafer surface is blown by N_2 gun to remove any particles, AZ-1350J positive photoresist is applied. The wafer is spun at 4400 rpm for 40 seconds. Then the resist is softbaked at 90C for 15 minutes to make it dry and hard enough to stand the contact of mask. The first mask level, mesa pattern, is then defined by UV-light exposure with the Suss aligner and resist development. The resist is then solidified by hardbake at 120C for 20 minutes to endure the wet chemical etch next.

The mesa etch is then performed in an etch solution of $1H_2SO_4$:$1H_2O_2$:24 D.I. H_2O for about 90 seconds. After thorough rinse in fresh D.I. water and N_2 blow dry, the photoresist is removed by acetone (ACE) soak. Then the wafer is soaked in methanol, rinsed in D.I. H_2O and blown dry by N_2. The mesa depth is measured by a Tencor Alpha Step profilometer to make sure the mesas are isolated (i.e., the mesa depth > 3000Å).

Then the ohmic contact pattern, the second mask level, is defined. The lithography step is almost the same as that of mesa etch except that the resist is softbaked at 65C and spun at 4000 rpm for 30 seconds. A thicker and softer resist will ease the lift-off, as mentioned earlier. Then the wafer is aligned and exposed to the ohmic contact mask with the Suss aligner. The photoresist is then developed after soaking in chlorobenzene for 14 minutes to produce an undercut profile. The hardbake is skipped here to make lift-off easier.

The wafer is loaded into the evaporation chamber immediately after etching the oxide etch with $1NH_4$:40 D.I. H_2O for 30 seconds. After evaporation, the metal is lifted off by acetone (ACE). If lift-off can not be completed by soak, a squirt bottle filled with ACE can be used. In the extreme situation, if the squirt bottle still does not work, a cotton tipped applicator may also be used with extreme caution. The mesas and ohmic contact patterns may be damaged easily by scrubbing. After the ACE soak, a methanol rinse, fresh D.I. H_2O rinse, and N_2 blow dry are performed.

Soon after lift-off, the alloy in Marshall furnace in N_2 environment should be performed. A long time wait (days) may lead poor contact resistivity. The alloy should follow the optimized procedure discussed in Section 4.3.

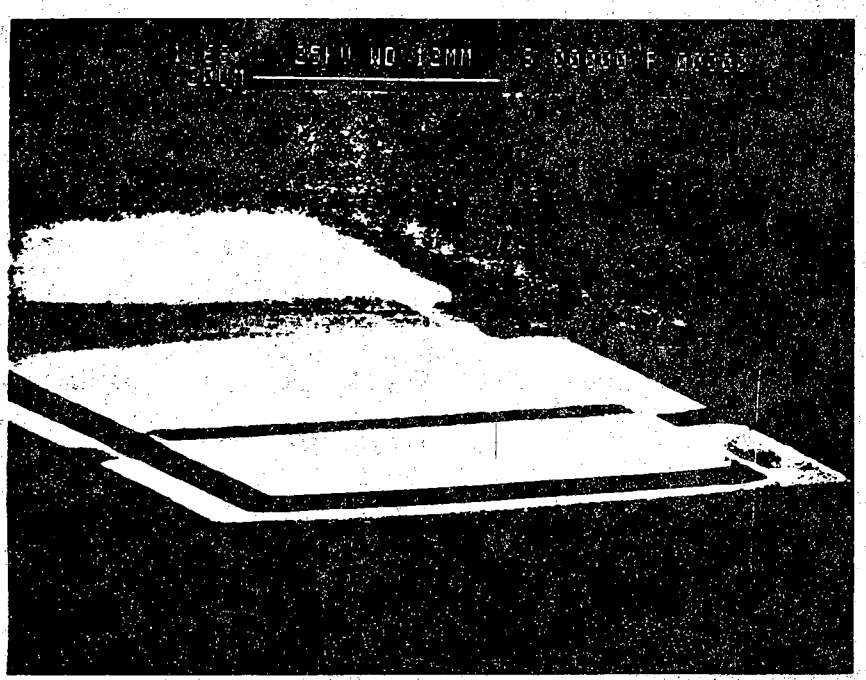
Next, the depletion-mode recess etch pattern, the third mask level, is defined. The lithography procedure is completely the same as that of the mesa etch. The etch is

performed with $2H_2SO_4$:$1H_2O_2$:500D.I.H_2O. The etch is monitored by drain current I_d. According to the discussion of circuit design in subsection 3.2.1, the etch for the depletion-mode device should be stopped when the drain current of the monitored device is decreased to one fifth of its original value (roughly corresponds to a 20 to 30 second etch). After the etch is complete, the wafer is flushed with fresh D.I. H_2O followed by N_2 blow dry.

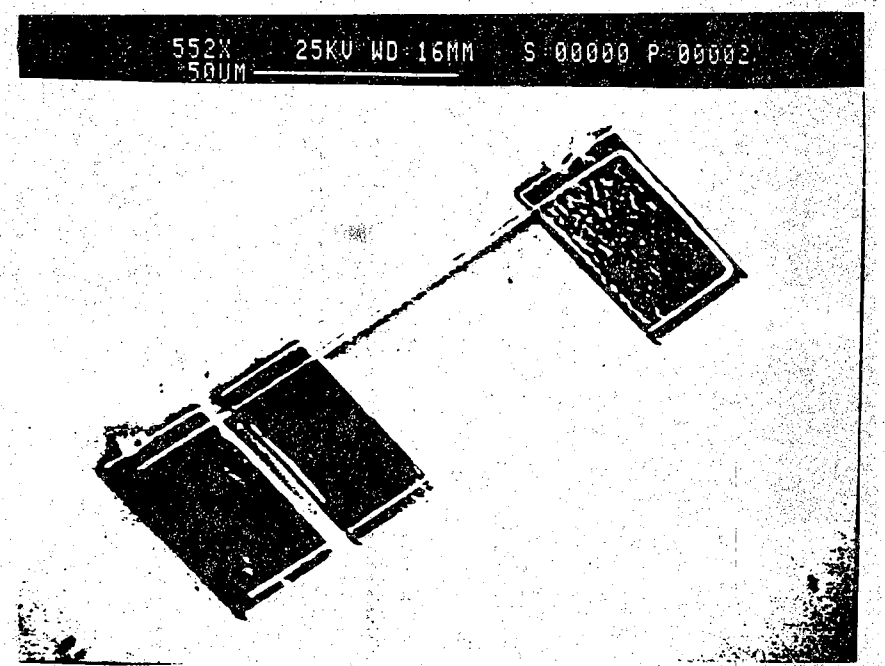
Similarly, the recess etch for the enhancement-mode device, fourth mask level, is performed in the same way as the depletion-mode device with the exception of a much smaller drain current. Extreme attention should be paid to prevent overetch. When the etch is nearly finished, a few seconds may make a big difference, remembering the sensitivity of n_s to thickness discussed in Section 4.4. Typically, for the device of (W/L)=40/2, SD=6μm and Vd=1V, the target drain current I_d is around 5μA for V_{th}≈0.4V. The etch time from experience is approximately 60 to 75 seconds by the recipe of $2H_2SO_4$: $1H_2O_2$: 500 D.I. H_2O. To prevent overetch, smaller time intervals and more devices belong to different die taken for monitoring are strongly recommended.

The final mask level, gate and interconnect metallization pattern is defined. The lithography and lift-off procedure is totally identical to that of the ohmic contact level. Alignment must be done with great caution. After resist development, the wafer must be inspected under a microscope carefully. Otherwise, misalignment with too large an error may cause gate-to-drain/source shorts, a fatal disaster for the device. This alignment becomes tougher as a more complex circuit composed of more devices, such as a ring oscillator, is fabricated. At this case, even if only one transistor out of 26 (for a eleven-stage ring oscillator, including two output stages) is shorted, then the entire circuit will fail.

Photographs of each major process steps are taken by a Cambridge Stereoscan 90 Scanning Electron Microscope (SEM), as shown in Fig. 4.7.

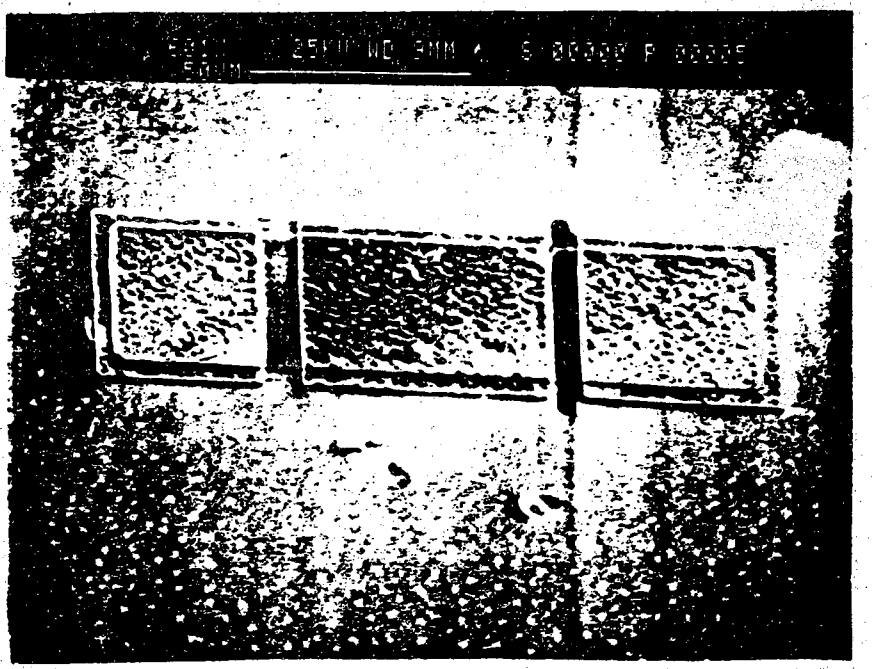


(a) mesa etch

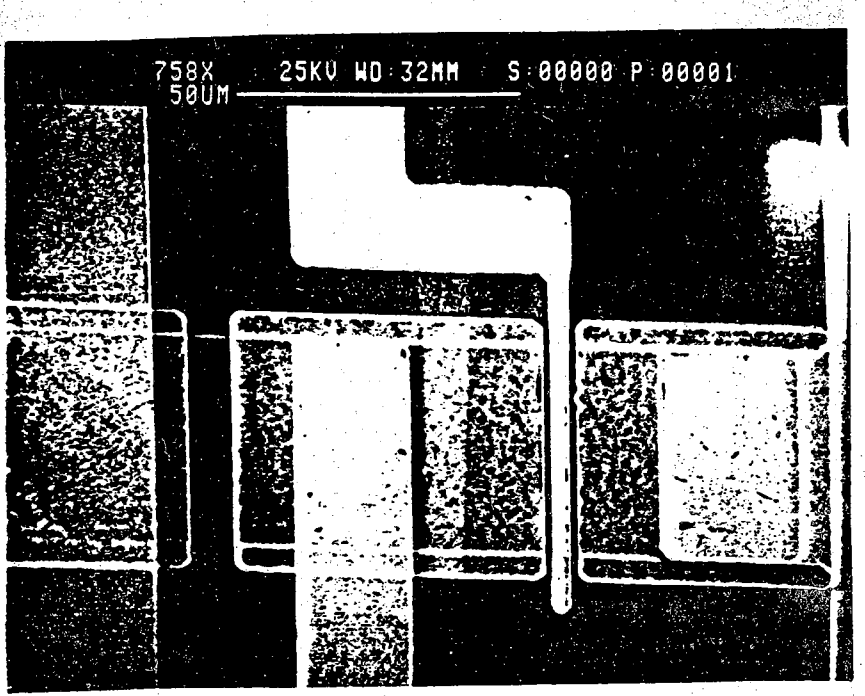


(b) ohmic contact

Figure 4.7 SEM photographs of E/D type inverter process steps.



(c) recess etches



(d) gate metallization

Figure 4.7 (continued).

CHAPTER 5

ELECTRICAL CHARACTERIZATION

This chapter will present the electrical testing results and discussions of the test chips. The specific devices and circuits that have been designed and fabricated for testing are:

(1) diagnostic devices
   (a) Greek-cross test structure, and
   (b) cross bridge Kelvin resistor (CBKR);
(2) D-mode and E-mode transistors
   (a) gated and unetched depletion-mode load,
   (b) ungated and unetched depletion-mode load,
   (c) ungated and etched depletion-mode load, and
   (d) enhancement-mode driver;
(3) DCFL E/D type inverters
   (a) inverter with the gated and unetched D-load,
   (b) inverter with the ungated and unetched D-load, and
   (c) inverter with the ungated and etched D-load;
(4) three-input NAND and NOR logic gates;
(5) ring oscillators.

These devices and circuits are built on an MBE MODFET film grown by Perkin Elmer. The thicknesses of various layers of the film are listed in the begining of the runsheet in the Appendix. A quite thick spacer layer of d=200Å implies that the film is optimized for high mobility rather than device transconductance, as will be explained in Section 5.2.

The measurements of Hall effect at room temperature on the film shows a Hall mobility of μ_H=7300cm^2/V-second and a sheet carrier concentration of the 2DEG n_s=4.88x10^{11}cm^{-2}.(61)

In section 5.1, the testing results on the diagnostic devices will be presented. Transistor measurements will be discussed in Section 5.2. Section 5.3 will present the results of E/D type MODFET inverters. Section 5.4 will present the characterization of all other DCFL circuits that have been fabricated, including three-input NAND and NOR

logic gates as well as an eleven-stage ring oscillator. Finally, a discussion about the testing results will be given in Section 5.5.

5.1 Diagnostic Devices

One of the two testing structures built and characterized is the Greek-cross test structure. The pattern is defined by etching a mesa to which the ohmic contacts are made, as shown in Fig. 5.1. The sheet resistance of the 2DEG, ρ_S, can be obtained by testing the van der Pauw structure formed by pads 1, 2, 3 and 4. A current I_{13} is forced from pad 1 to pad 3 and the voltage drop between pad 2 and pad 4, ΔV_{24}, is measured. The sheet resistance of the 2DEG is then given by the formula:

$$\rho_s = \left[\frac{\pi}{\ln 2}\right]\left[\frac{\Delta V_{24}}{I_{13}}\right] \tag{5.1}$$

The average of the measured sheet resistance is

ρ_S=1.84 KΩ/square

Recalling the equation of ρ_S used in Chapter 2:

$$\rho_s = \frac{1}{q\mu n_s} \tag{5.2}$$

the actual electron drift mobility in the 2DEG is then calculated by

$$\mu_d = \frac{1}{q\rho_s n_s} = 6951.84 \frac{cm^2}{V\text{-}sec} \tag{5.3}$$

where n_S=4.88x10^{11}cm^2 was used. This drift mobility is smaller than the measured Hall mobility. This is expected because these two physical parameters are related by

$$\mu_H = r_H \mu_d \tag{5.4}$$

where r_H is called the Hall factor. For both electrons and holes in GaAs, $r_H \geq 1$, (54) which implies $\mu_H \geq \mu_d$.

The other two pads of this structure, pads 5 and 6, are used to find out the actual line-width of the pattern. A current I_{35} is forced from pad 3 to pad 5 and the resultant voltage drop between pads 4 and 6, ΔV_{46}, is measured. Then the resistance is determined by

$$R = \frac{\Delta V_{46}}{I_{35}} \tag{5.5}$$

Also, according to the defination of sheet resistance,

$$R = \rho_s\left(\frac{L}{W}\right) \tag{5.6}$$

where L and W are length and width of the 2DEG channel. Substituting (5.5) into (5.6) and rearranging the result, we obtain the real line-width defined by the process:

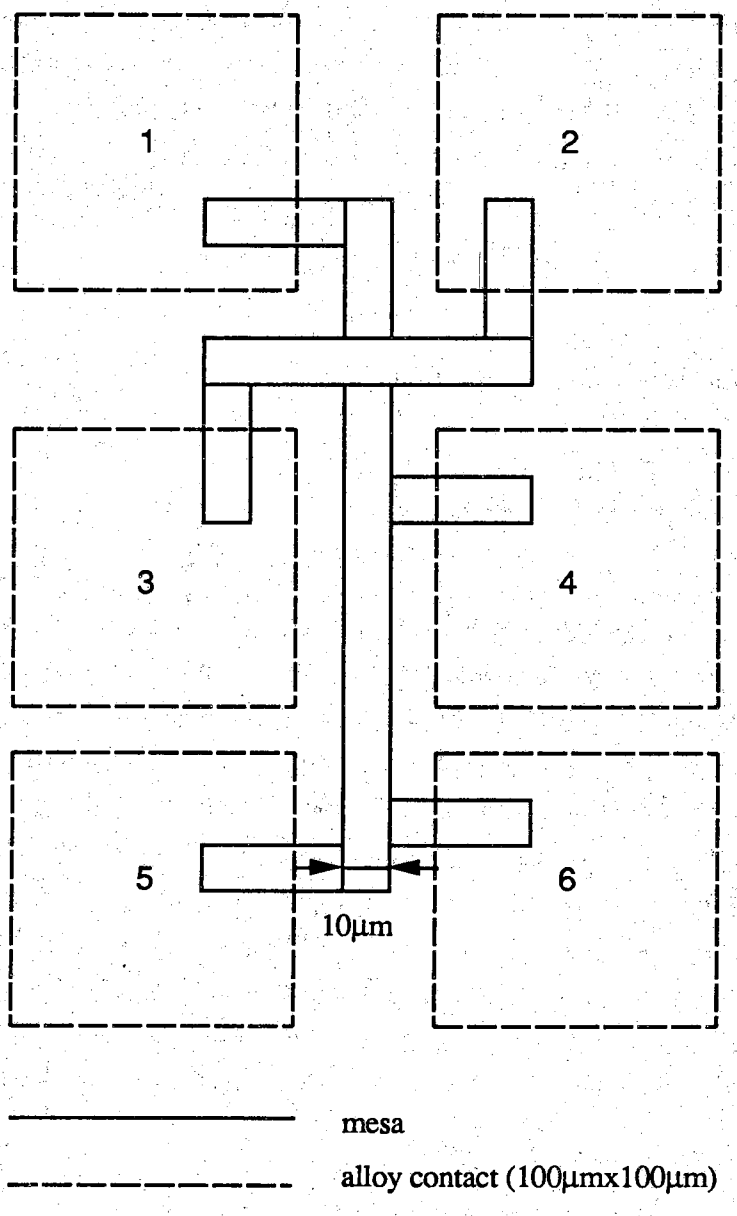


Figure 5.1 Greek-cross test structure.

$$W' = \rho_s \frac{L}{R} = \rho_s L \left(\frac{I_{35}}{\Delta V_{46}} \right) \tag{5.7}$$

where the sheet resistance ρ_S is obtained from the previous measurement on the van der Pauw structure. The average line-width of 9.72μm is found, as compared to the designed line-width of 10μm. Several factors may account for this deviation. The mask pattern may be a little bit off from its original layout file during mask production. Lithography and lateral etch are major factors responsible for the change.

Another important parameter which needs to be known well is the contact resistance, as we have discussed in Section 4.2. The widely used definition of specific contact resistivity is:

$$\rho_c = \left(\frac{dV}{dJ} \right)_{V=0} (\Omega\text{-cm}^2) \tag{5.8}$$

where J and V are the current density per unit area and the voltage drop of the contact, respectively. Another measure of the contact resistance is the width normalized contact resistance R_C (Ω-mm). According to the transmission line model (TLM),(39)(54) the above two figures are related as:

$$R_c = \sqrt{\rho_c \rho_s} \coth \left(\sqrt{\frac{\rho_s}{\rho_d}}\, d \right) \tag{5.9}$$

where d is the length of the contact along the 2DEG channel.

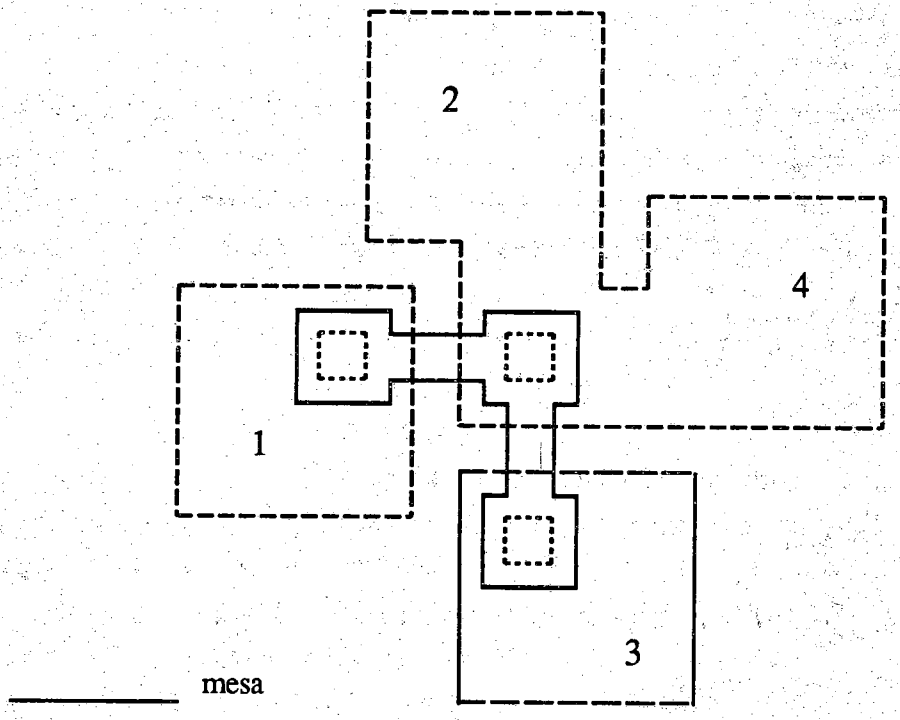
To directly measure the contact resistivity ρ_C, the CBKR four-terminal microelectronic testing structure is used. This is the second diagnostic device defined on the test chip. Its pattern is shown in Fig. 5.2 (a). Three contacts are made to the 2DEG channel which is defined by mesa. A current I_{23} is forced vertically through pads 2 and 3. The corresponding voltage drop across the contact is measured between pad 1 and pad 4. Since no current flows through pad 1 and pad 4, the voltage drop between them, ΔV_{14}, is exactly equal to the voltage drop across the contact resistance R_C, as shown by the equivalent circuit in Fig. 5. 2 (b), therefore this four point method eliminates any effect of series resistance introduced by the testing probes in the two-probe method.

The specific contact resistivity ρ_C determined by the CBKR structure is

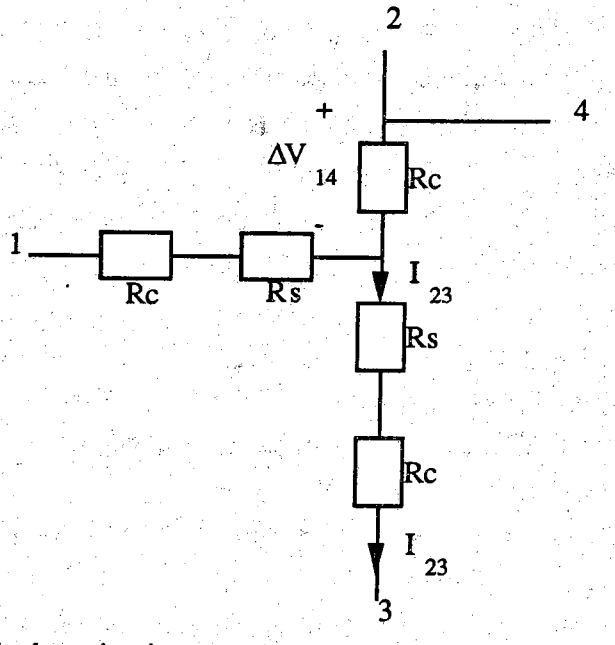
$$\rho_c = \left(\frac{\Delta V_{14}}{I_{23}} \right) A \ (\Omega\text{-cm}^2) \tag{5.10}$$

where A is the area of the contact measured. In our case, A=15μmx15μm.

The data obtained from the CBKR measurement have been given in Table 4.1 and have been fully discussed in the previous chapter. The average specific contact resistivity of sample #5 ρ_C=12.3x10^{-5} Ω-cm^2 can be converted into a width-normalized contact



(a) CKBR structure.



(b) equivalent circuit.

Figure 5.2 CBKR and its equivalent circuit.

resistance of Rc=4.76 Ω-mm by (5.9) and the value of ρ_s=1.84 KΩ/square, as measured from the Greek-cross structure before. For a typical ohmic contact of 40μmx40μm, a contact resistance of Rc=119 Ω is obtained for each contact. As will be discussed in the next section, the contact resistance accounts for a large portion of the total serial access resistance of the MODFET devices on the test chips. A further reduction of contact resistance is very necessary for better device performance. A specific contact resistivity as small as $5x10^{-8}$ Ω-cm^2 has been reported by Morkoc, et al.(49) A value below $1x10^{-6}$ Ω-cm^2 should be targeted for the Purdue MODFET process, as will be discussed in Section 5.2.

5.2 D-mode and E-mode Transistors

The characteristic that gives most information for the analysis of FET performance is the drain current I_d versus drain voltage V_d for various gate voltages V_g. Such two curves of a D-mode and an E-mode devices are shown in Fig. 5.3 (a) and (b), respectively. As expected, the D-mode device is on from V_g=0 to its negative threshold voltage V_{th}≈-3.4V is reached. At this point the 2DEG channel is eliminated. Oppositely, the E-mode device is off at V_g=0. When V_g is increased to V_{th}≈0.4V, a 2DEG channel is formed and a drain current is produced. For both modes, increased gate voltages V_g will cause increased 2DEG carrier concentrations, and therefore increased drain currents.

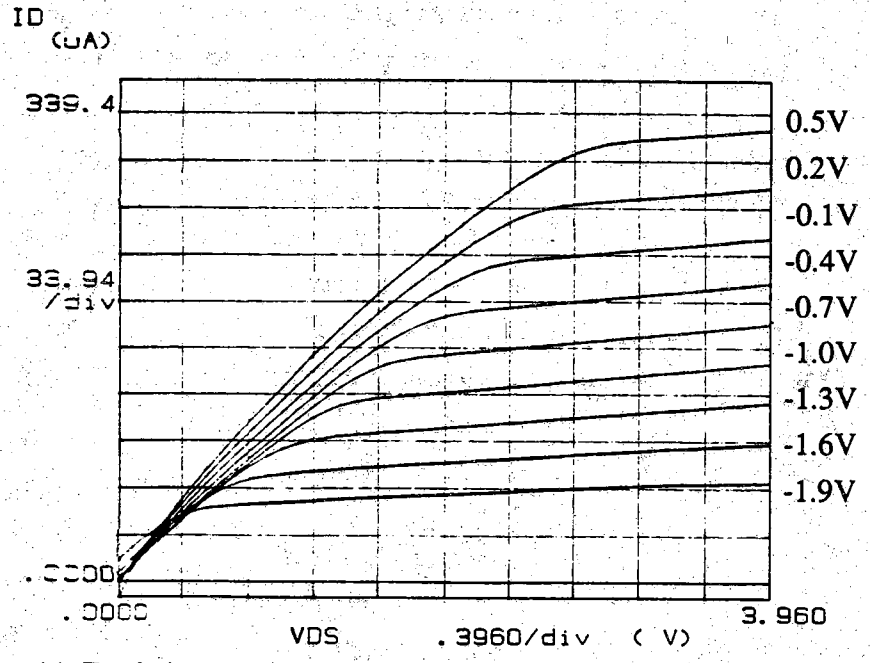
Slight discontinuities occur in the small V_d regions for both curves. This is due to gate leakage. The forward bias voltage across the gate-to-drain Schottky diode is approximately V_g-V_d. If V_g is relatively large and V_d is small, a current will flow from the gate to the drain, therefore a negative drain current occurs. When V_d is increased, the voltage across the diode is decreased and at a certain point the gate diode is turned off. Beyond this point, the I_d versus V_d curve comes back to the normal characteristic as expected.

The threshold voltage of a MODFET device can be found by the curve I_d vs. Vg for very small V_d, as shown in Fig. 5.4 (a). Small V_d=0.05V is used to guarantee the device is in its linear region of operation. Recalling the equation of the linear region:

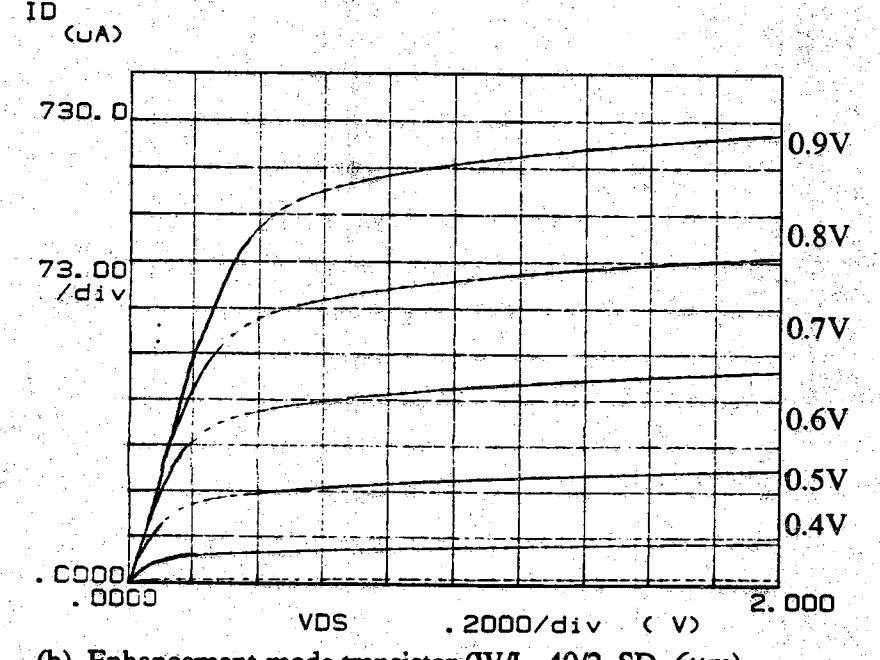
$$I_d = \beta(V_g - V_{th})V_d \qquad (2.48)$$

Hence the linear portion of the curve in Fig. 5.4 (a) can be extrapolated to I_d=0. The intercept is the threshold voltage of the device.

The above method may not be realistic if the gate leakage is too serious. In this case, the saturation region of the device will be used. Recalling the equation of the saturation region for relatively large gate length:

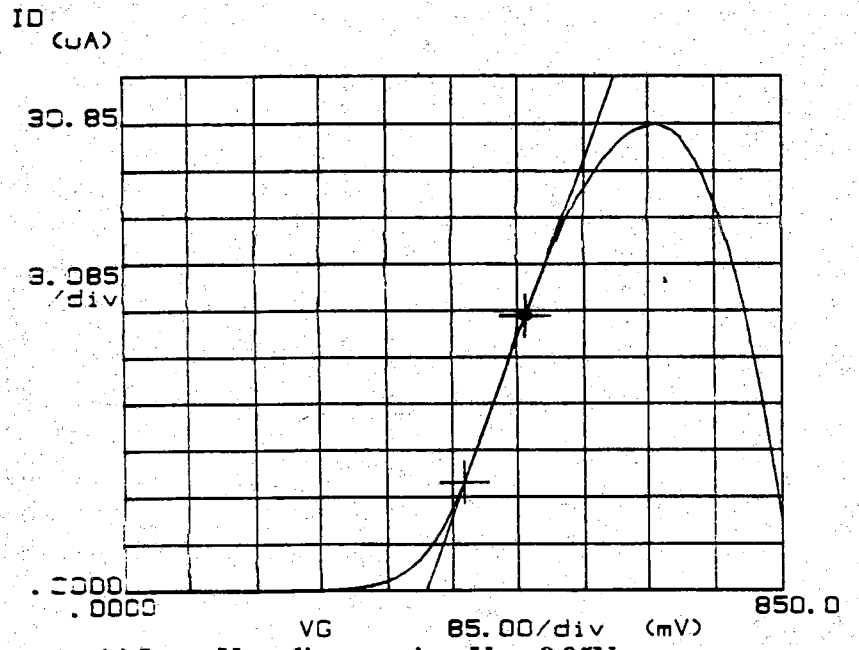


(a) Depletion-mode transistors (W/L=40/150, SD=150).

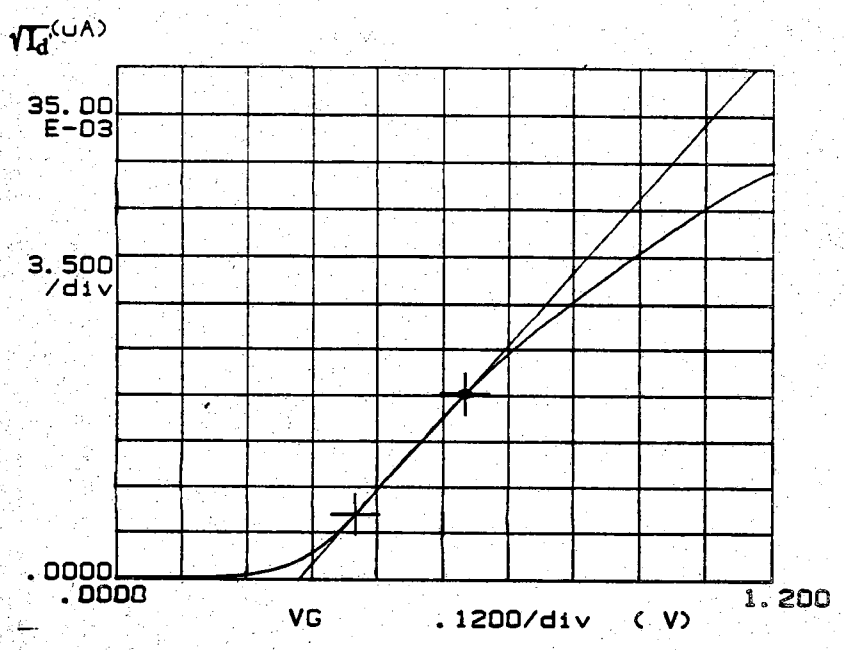


(b) Enhancement-mode transistor (W/L=40/2, SD=6μm).

Figure 5.3 Characteristic curves of (a) D-mode and, (b) E-mode MODFET's.



(a) I_d vs. V_g at linear region, V_{ds}=0.05V.



(b) $I_d^{1/2}$ (=I) vs. V_g at saturation region, V_{ds}=2.5V.

Figure 5.4 I_d vs. V_g at two operation regions of an E-mode transistor (W/L=40/2, SD=6μm).

$$I_d = \beta \frac{(V_g - V_{th})^2}{2} \tag{2.57}$$

Here, the current saturation due to the channel pinch-off is assumed since all of the gate lengths on the test chips are greater than 2 micrometers. This equation can be rewritten as

$$\sqrt{I_d} = \sqrt{\frac{\beta}{2}}\,(V_g - V_{th}) \tag{5.11}$$

Thus the linear region of the curve $I_d^{1/2}$ vs. V_g can be extrapolated to I_d=0. A constant but relatively large drain voltage, $V_d > V_g - V_{th}$, must be used to make the device operate in its saturation region. The intercept point is the threshold voltage of the device, as shown in Fig. 5.4 (b) and Fig. 5.5 for E-mode and D-mode transistors, respectively.

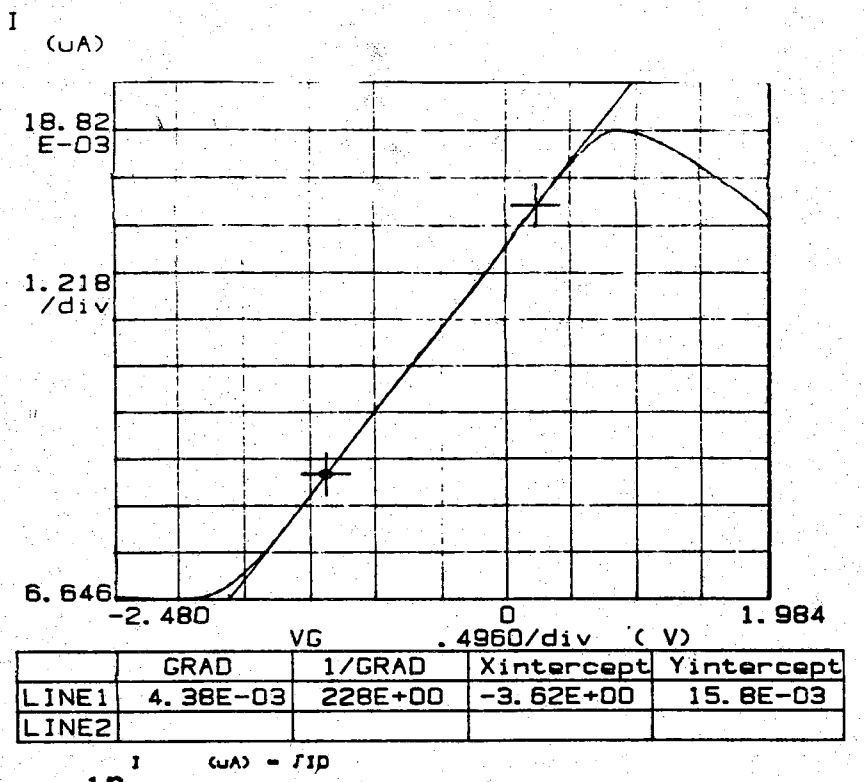
The above two curves of linear and saturation regions should give same value of threshold voltage V_{th} if no gate-to-drain leakage occurs. If the gate leakage is not negligible, the threshold voltages obtained from the two curves in Fig. 5.4 will be slightly different.

To eliminate the effect of this leakage, the data measured and used later on will be obtained from that of the saturation region, or $I_d^{1/2}$ vs. V_g.

The threshold voltages of both D-mode and E-mode transistors measured across the 24 die in a 6mmx9mm wafer are shown in Fig. 5.6 and Table 5.1. The control of the E-mode threshold voltage has been achieved by the process discussed in Chapter 4. A further improvement is necessary for better device and circuit performances.

Another important figure of merit is the transconductance, G_m (s) or width-normalized transconductance, g_m (ms/mm), as discussed in Section 2.5. The test results of G_m's for both D-mode and E-mode MODFET's are shown in Fig. 5.7 For each of the two cases, G_m is zero when V_g is below threshold voltage since the device is off. Beyond the threshold voltage, G_m increases rapidly. A maximum is reached where the 2DEG carrier concentration reaches it's maximum value, i.e., the potential well at the AlGaAs/GaAs interface is full. At this point, the depletion region from the gate and the depletion region from the heterojunction just touch. Beyond this point, G_m goes down because the depletion width of the Schottky gate is smaller than AlGaAs thickness so that a parallel channel in the doped n+AlGaAs will appear. Thus the charge in the AlGaAs isolates the 2DEG from changes in V_g, i.e., a change in V_g mainly changes the charge in the AlGaAs, so dn_s/dV_g goes to zero.

The transconductance G_m defined by (2.60) and measured in Fig. 5.7 is the so called extrinsic transconductance, which includes the series resistance of source. An intrinsic transconductance, G_{mo}, is defined as:



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	4.38E-03	228E+00	-3.62E+00	15.8E-03
LINE2				

I (uA) - VIp

Figure 5.5 $I_d^{1/2}$ vs. V_g for the D-mode transistor.

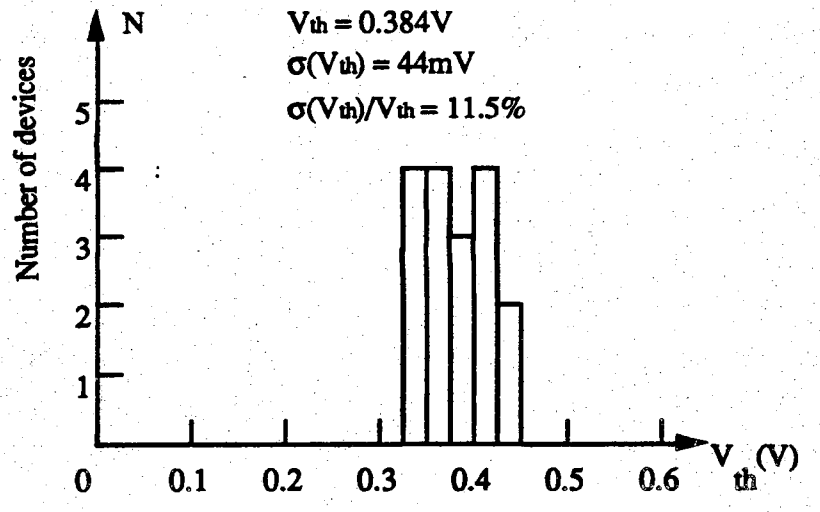


Figure 5.6 Histogram of V_{th} of E-mode transistors across the wafer.

Table 5.1 Threshold voltages V_{th} (V) of E-mode MODFET's across the entire wafer.

Mode	Enhancement-mode	Depletion-mode
No. of transistors measured	17	8
Average value $\overline{V_{th}}$	0.384V	-3.42V
Standard deviation σ	44.0mV	155.0 mV
$\frac{\sigma}{\overline{V_{th}}}$ x 100%	11.5%	4.52%
Gate recess controlled by	wet etch	MBE (unetched)

$$G_{mo} = C_2 W V_{sat} \tag{5.12}$$

Opposite to G_m, G_{mo} considers the 2DEG channel conductance only. The two transconductances are related by

$$G_m = \frac{G_{mo}}{1+G_{mo}R_s} = \frac{1}{R_s+\frac{1}{G_{mo}}} \tag{5.13}$$

Another important parameter is the drain conductance, which is:

$$G_d = \left(\frac{\Delta I_d}{\Delta V_d}\right)_{V_g} \tag{5.14}$$

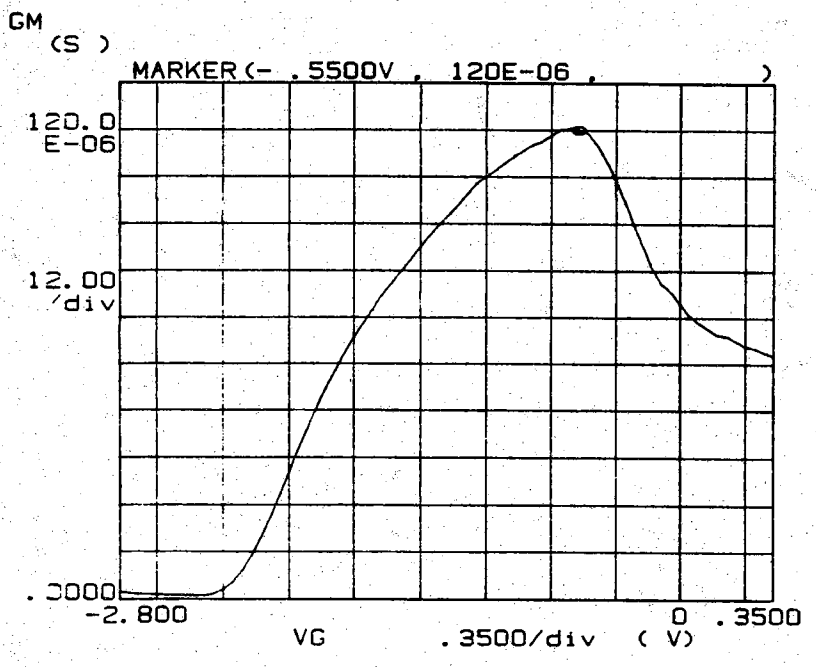
The open circuit gain of a FET is determined by the drain and extrinsic transconductances as

$$\text{gain} = \frac{G_m}{G_d} \tag{5.15}$$

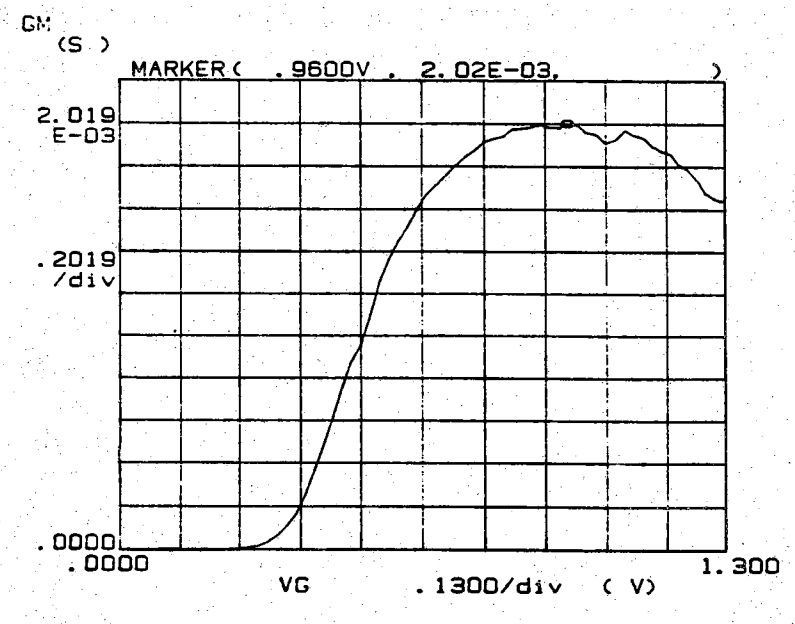
Both G_m and G_d depend on the gate voltage V_g. To obtain a maximum gain, an operating point at V_g should be found. Since G_d is almost a constant in saturation region, V_g is picked where G_m reaches it's maximum value. For the device in Fig. 5.3 (b) and Fig. 5.7 (b), G_d=0.057ms at V_g=0.9V, the maximum open circuit dc gain of this FET is then:

gain=2.019/0.057=35.42

Now it is easy to understand why this film with a thick spacer layer of t_2=200Å is said



(a) D-mode transistor (W/L=40/150, SD=150μm).



(b) E-mode transistor (W/L=40/2, SD=6μm).

Figure 5.7 Transconductances at V_{dd} = 2.0V.

not to be optimized for transconductance. A thick spacer layer leads to a smaller capacitance $C_2 = \varepsilon_2/t_2$. This turns into a smaller G_{mo} and G_m by (5.12) and (5.13), respectively.

It is understood that a shorter gate length MODFET will result in a smaller channel resistance, therefore a larger transconductance. In other words, $g_m=\mu_n C_2 W(V_g-V_{th})/L$ so long as $n_s=C_2(V_g-V_{th})/q$. If g_m is expressed in mS per unit width, then g_m goes as 1/L. This is proven by the measurements illustrated in Table 5.2.

Table 5.2 Transconductances versus gate lengths L and source-to-drain spacing SD.

No.	mode	(W/L) ratio	SD (μm)	Gm (mS)	g_m(mS/mm)
1	E	80/2	6	3.53	44.06
2	E	40/2	6	2.02	50.50
3	E	40/2	8	1.63	40.75
4	E	40/4	8	1.362	34.05
5	E	40/6	10	1.199	29.975
6	D	40/150	150	0.955	6.37

Comparing the results listed in Table 5.2 with the values obtained at Purdue one year ago[33], moderate improvements have been made. This progress is believed primarily due to the efforts of improving ohmic contact and threshold voltage control on the E-mode MODFET's. Better control of the recess etch allows the threshold voltage V_{th} of the E-mode devices to be decreased from about 0.85V one year ago to 0.38V now. Recalling equation (2.57) for the large gate case (where saturation is due to channel pinch-off, rather than carrier velocity saturation), the transconductance in the saturation region is then

$$G_m = \mu C_2\left(\frac{W}{L}\right)(V_g-V_{th})=\frac{q\mu n_s W}{L} \tag{5.16}$$

where

$$n_s = \left(\frac{C_2}{q}\right)(V_g-V_{th}) \tag{5.17}$$

This means a reduced threshold voltage Vth will lead to a larger Gm because other quantities in (5.16) are constants.

Even when V_g is below the threshold voltage V_{th}, the drain current is not absolute zero as long as V_d is not zero. This leakage current is called the subthreshold current. Its magnitude is about 500nA for the MODFET's processed at Purdue, as shown in Fig. 5.8.

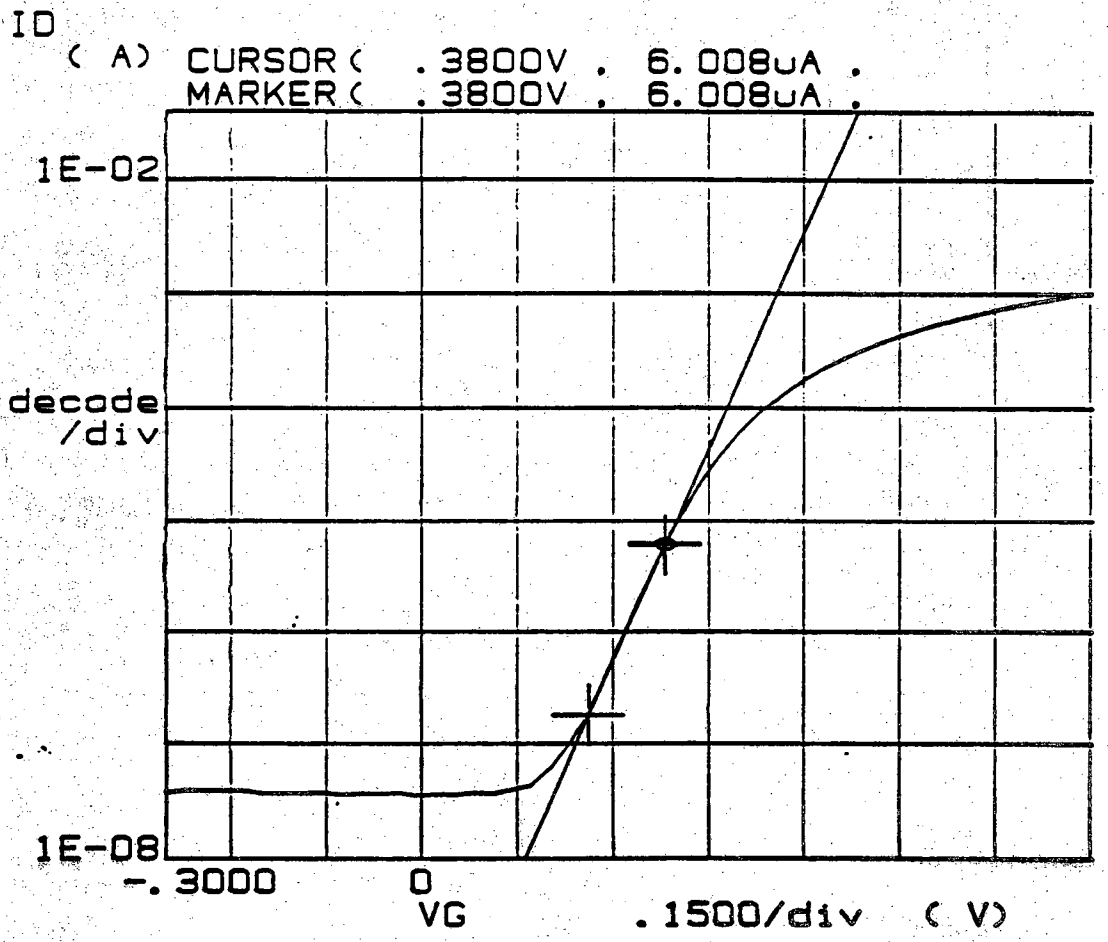


Figure 5.8 Subthreshold current at V_d=2.0V (E-mode device:W/L=40/2, SD=6μm).

The leakage path is believed to be through the undoped GaAs and the semi-insulating substrate. Currents from 50nA to 180nA between the isolated mesas were found when a voltage of V=3V was applied. Similar to Si MOSFETs[58], an exponential relationship in the region below the threshold voltage, as shown in Fig. 5.8, is found. The typical value of MODFET's fabricated at Purdue is about 80mV/decade.

The final important figure of merit measured for the single FET is the drain/source resistance. From (2.46), for any two points (V_{g1}, I_{d1}) and (V_{g2}, I_{d2}) chosen for large (V_g-V_{th}) but small V_d, we can obtain the following equation through some simple derivation:

$$R_s+R_d = \left(\frac{V_d}{I_{d1}}\right)\left(\frac{1-\left(\frac{I_{d1}}{I_{d2}}\right)\left(\frac{V_{g2}-V_{th}}{V_{g1}-V_{th}}\right)}{1-\left(\frac{V_{g2}-V_{th}}{V_{g1}-V_{th}}\right)}\right) \tag{5.18}$$

The difference of the source and drain access resistances Rs-Rd, is determined by end resistance measurements proposed by K. W. Lee, et al.[59] A current is forced between the gate and the grounded source. The voltage drop between the drain and the source is measured. This voltage divided by the current gives the source access resistance together with some portion of the channel resistance. The same procedure is repeated after the drain and source are switched. The difference between the two resistances obtained above is reasonably thought to be (Rs-Rd). For a quick estimation, especially when source and drain are physically symmetric, it is reasonable to assume $R_s \approx R_d$. Then for the device illustrated in Fig. 5.4 (a) with V_{th}=0.334V, choosing the two points at Vd=0.05V:

I_{d1}= 18.51μA , V_{g1} = 0.527 V

I_{d2} = 30.85μA, V_{g2}= 0.69V

Calculation of (5.18) gives

R_s+R_d= 495Ω

and

$R_s \approx R_d$=247.5Ω

The total resistance Rs+Rd is:

$R_s+R_d = R_{channel} + 2R_c$

where $R_{channel}$ is the resistance due to the 2DEG under the ungated portions of the device. Recalling the contact resistance obtained from last section, R_c=119Ω, the total contact resistance is then about 48.1% of the total resistance. To reduce its percentile to 10% or below, a contact resistance of Rc=14.3Ω or a specific contact resistivity $\rho_c < 1.8\times10^{-6}$ Ω-cm^2 must be achieved, as claimed earlier.

Finally, the characteristic curves of ungated D-mode MODFET's are shown in Fig. 5.9. Only a small portion, the linear region of operation, is used for the E/D type inverter built at Purdue, as discussed in Section 3.2.

5.3 DCFL E/D Type Inverters

As discussed in Chapter 3, the operating points V_{OL}, V_{OH} of an inverter can be found by connecting two identical inverters in cascade, as shown in Fig. 3.5 (b).

In addition to the above two values, several other critical voltages and concepts are commonly used in characterizing and evaluating the inverter performance. These concepts are input low and high voltages, V_{IL} and V_{IH}, inverter threshold voltage V_t, noise margin NM, voltage noise sensitivity NS, the input transition width TW, the logic swing V_l, and the circuit noise immunity levels NI. Some of them are shown in Fig. 5.10. They will be explained and defined next in the order they are listed above.

V_{IL} is defined by the point where

$$\frac{dV_{out}}{dV_{in}} = -1 \tag{5.19}$$

V_{IL} represents the maximum value that a logic "0" input may have and still guarantee a logic "1" at the output. Similarly, V_{IH} is defined by the same equation mentioned above and represents the minimum logic "1" input voltage that will guarantee a logic "0" at the output. V_t is defined as the intersection of the transfer characteristic with the unity gain line Vout = Vin. The rest of the concepts mentioned above are defined in terms of V_{OL}, V_{OH}, V_{IL}, V_{IH}, and V_t.

The noise margin NM's are expressed as

$$NM_H = V_{OH} - V_{IH} \tag{5.20}$$

$$NM_L = V_{IL} - V_{OL} \tag{5.21}$$

as shown in Fig. 5. 10. Here and later on the subscripts "H" and "L" are for high and low states, respectively. Physically, noise margin NM is the range of variation of an input voltage for which no output transition will occur. It can be interpreted by Fig. 5.11.

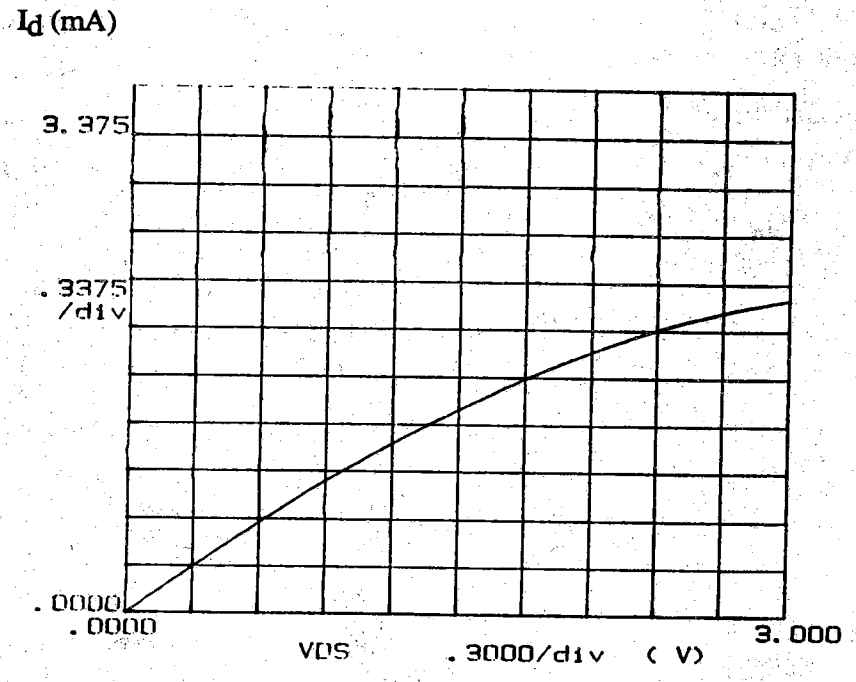
The voltage noise sensitivities NS's are defined as

$$NS_L = V_{th} - V_{OL} \tag{5.22}$$

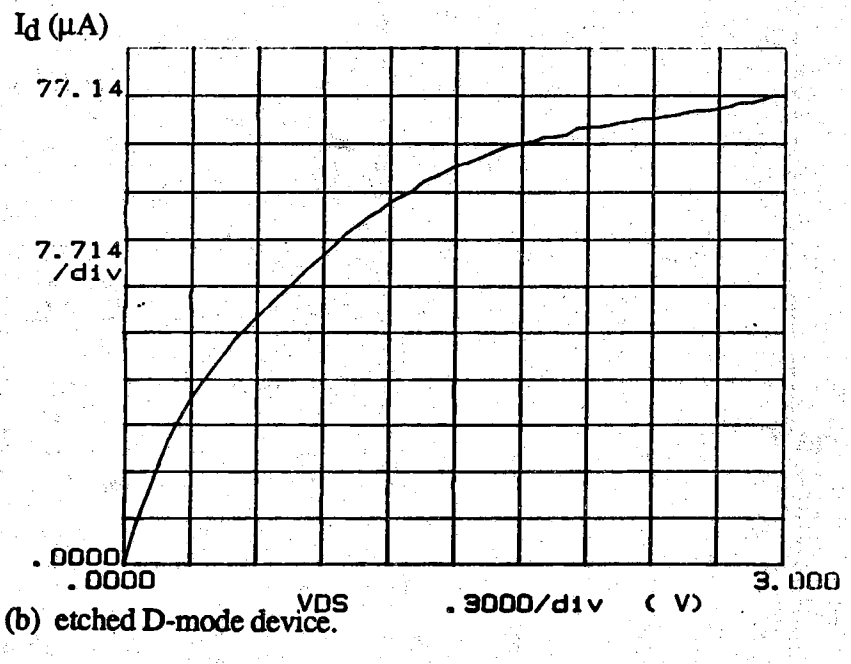
$$NS_H = V_{OH} - V_t \tag{5.23}$$

as shown in Fig. 5.10 also. For an ideal inverter, $NS_H = NS_L = V_{dd}/2$. The interpretation of NS is the amount of voltage necessary at the input to cause a definite output transition, as defined in Fig. 5.10.

The input transition width TW is defined as



(a) unetched D-mode device.



(b) etched D-mode device.

Figure 5.9 Characteristic curves of ungated D-mode transistors (W/L=40/8, SD=14).

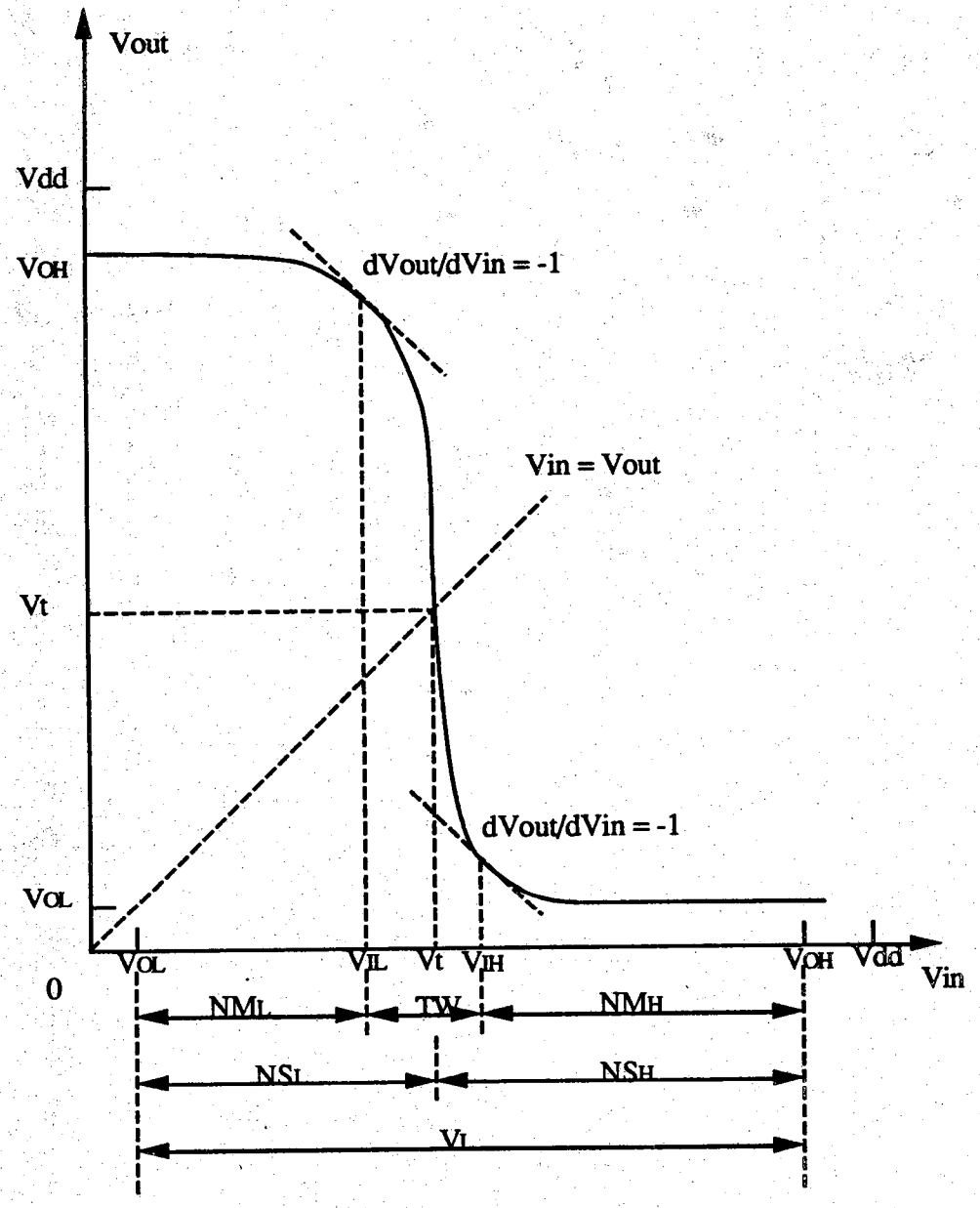


Figure 5.10 Inverter transfer characteristic with notations defined.

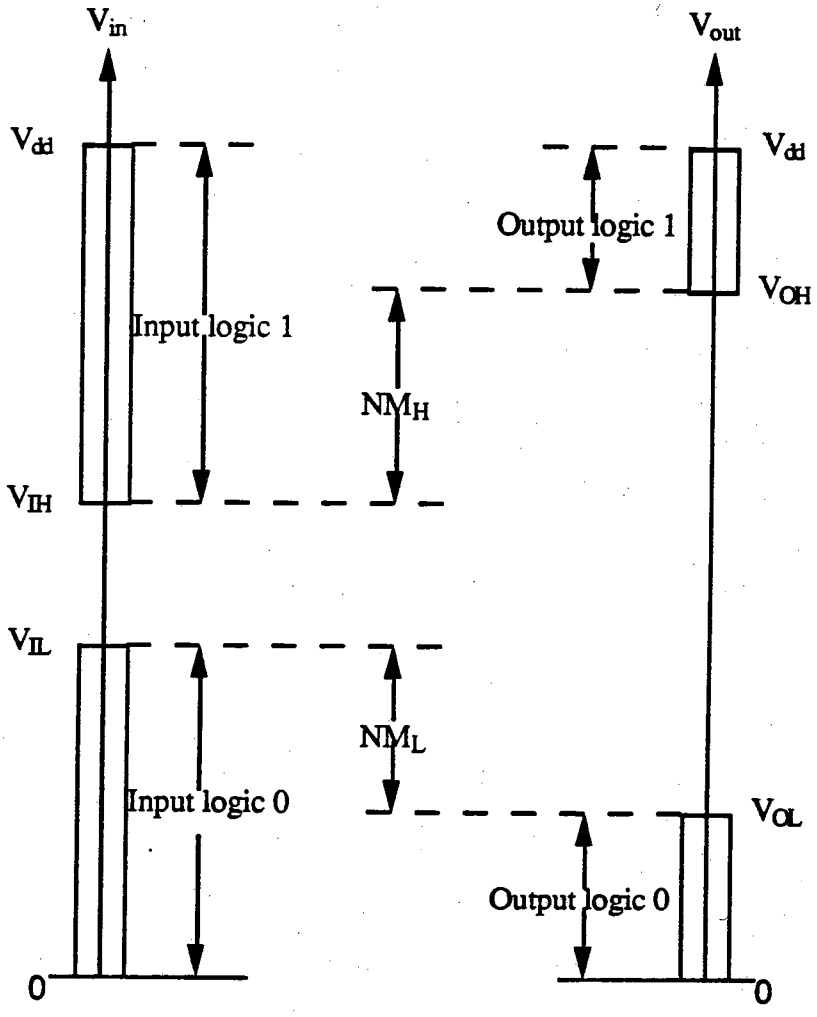


Figure 5.11 Interpretation of noise margin.

$$TW = V_{IH} - V_{IL} \tag{5.24}$$

This quantity is a measure of the separation between input logic low and input logic high values.

The logic swing V_l, which is simply the separation of output high and output low values, or be expressed as

$$V_l = V_{OH} - V_{OL} \tag{5.25}$$

Finally, the circuit noise immunity levels are defined as:

$$NI_H = \frac{NS_H}{V_l} = \frac{V_{OH}-V_{th}}{V_{OH}-V_{OL}} \tag{5.26}$$

$$NI_L = \frac{NS_L}{V_l} = \frac{V_{th}-V_{OL}}{V_{OH}-V_{OL}} \tag{5.27}$$

which are the measure of the ability of the circuit to resist noise.

With the concepts and their values defined above, the DC properties of the inverter circuit can be evaluated. Two typical transfer characteristic curves of inverters with unetched and etched loads fabricated on the test chip are shown in Fig. 5.12 and 5. 13, respectively. The characterization results are listed in Table 5.3.

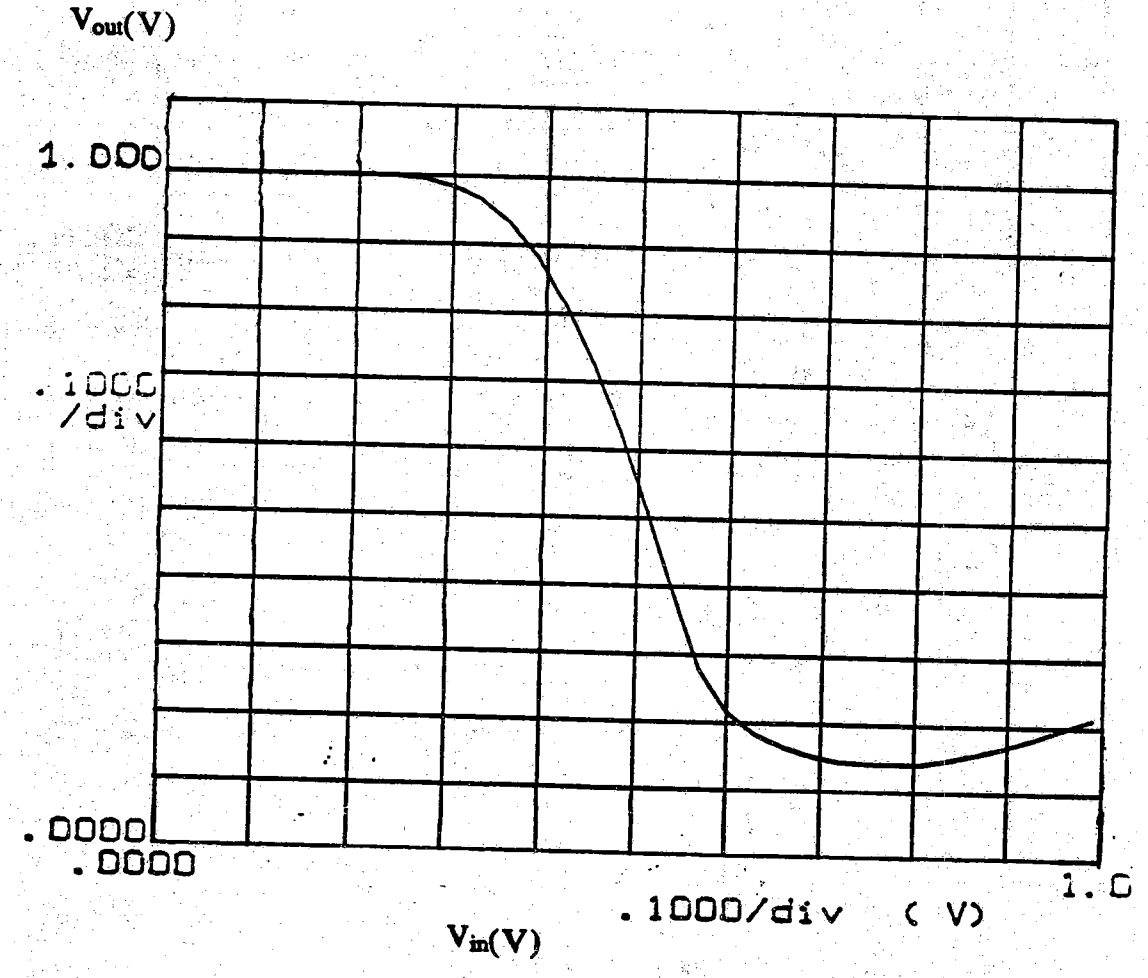
The inverter with etched load has a good shape. The one with unetched load does not. But the etched D-load is overetched. This overetched load possesses a very high resistance or a threshold voltage which is almost positive. Its behavior is similar to an E-mode load such that the output high of the inverter can not be pulled all the way up to V_{dd}.

5.4 Other MODFET DCFL Circuits

In this section, three-input NAND and NOR logic gates and ring oscillators will be characterized.

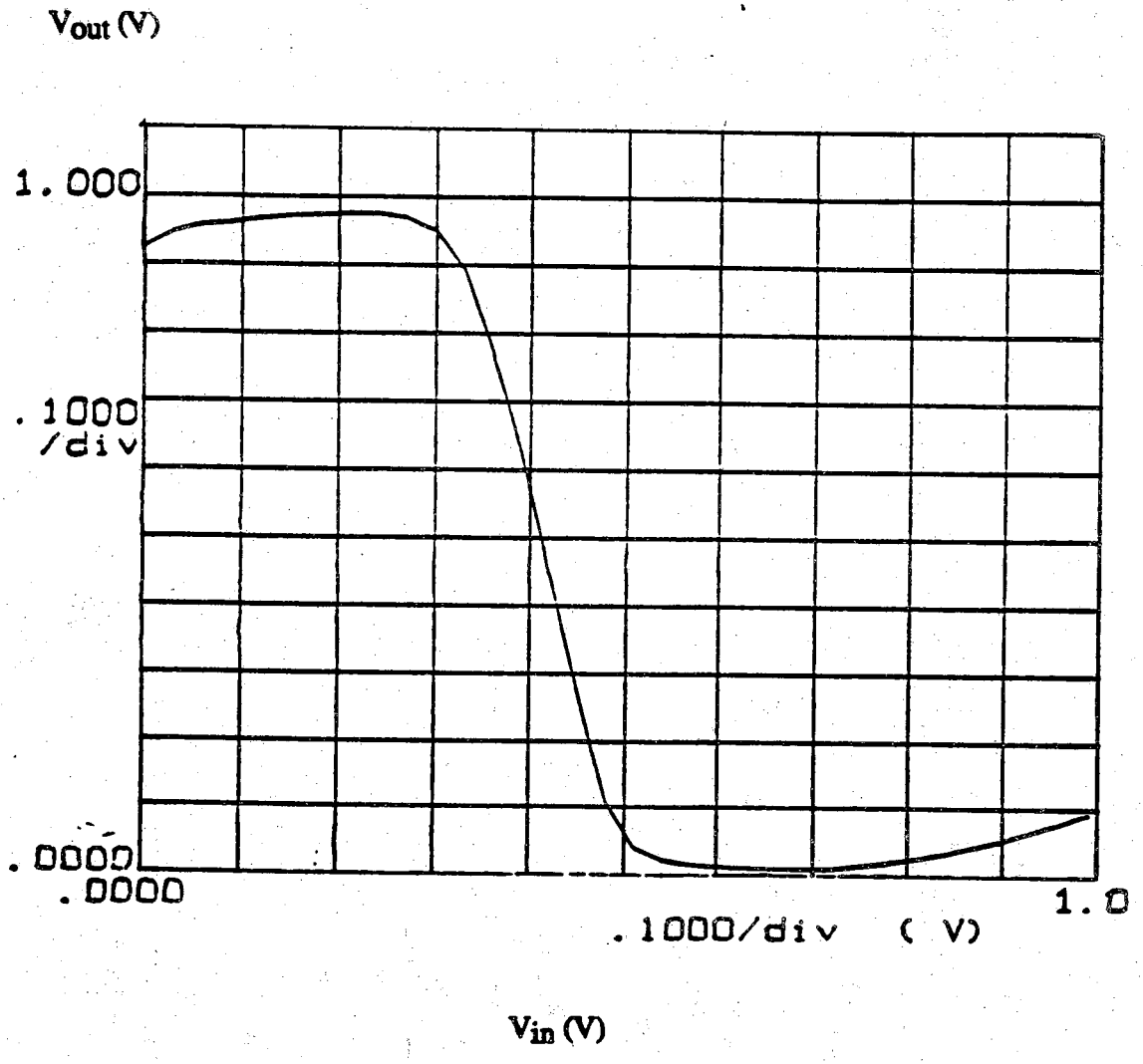
5.4.1 Three-input NAND and NOR logic gates

To characterize these two gates, input sequential signals representing the truth tables Table 3.1 and Table 3.2 must be generated. Since no multioutput sequential generator is available at present, a square periodic wave form generator (IEC F51 function generator) and a TTL dual D-type edge-triggered flip-flops (SN7474N) as well as a hex buffer/driver with open collector high voltage outputs (SD7407) are connected as shown in Fig. 5.14 (a). The timing sequence generated by this circuit is illustrated in Fig. 5.14 (b). Totally six probes, three inputs A, B, and C, one voltage supply V_{dd}=1.0V, one ground and one output, are needed.



E-driver: W/L=40/4, SD=8μm
D-load: W/L=40/120, SD=120μm

Figure 5.12 Transfer characteristic of E/D inverter with unetched load.



E-driver: W/L=40/2, SD=8μm
D-load: W/L=40/20, SD=20μm

Figure 5.13 Transfer characteristic of E/D inverter with etched load.

Table 5.3 Characterization of E/D inverters with etched and unetched loads.

No.	Characterized values	Inverter with unetched load	Inverter with etched load
1	V_{OH}	1.0	0.96
2	V_{OL}	0.21	0.08
3	V_{IH}	0.62	0.51
4	V_{IL}	0.34	0.30
5	Vt	0.52	0.42
6	NM_H	0.38	0.45
7	NM_L	0.13	0.22
8	NS_H	0.49	0.54
9	NS_L	0.31	0.34
10	TW	0.28	0.21
11	V_I	0.79	0.88
12	NI_H	0.61	0.61
13	NI_L	0.39	0.39

The two logic gates are tested with a Tektronix 5440 oscilloscope. Their inputs and outputs are pictured in Fig. 5.15 and Fig. 5.16, respectively. The correct logic functions are created by the two gates.

5.4.2 Ring Oscillators

As shown by the layout of the ring oscillator chip on page 52, totally four probes are needed to characterize a ring oscillator. One is for voltage supply V_{dd}, one is for output Vout, and two for the ground.

A Micromanipulator FET PS4 probe, a HP54501A Digitizing oscilloscope and a Tektronix 5440 oscilloscope are used to characterize the ring oscillators. The oscillation waveform of an eleven-stage MODFET ring oscillator with E/D type inverters and two output stages is shown in Fig. 5.17 (a). The load of each of 13 inverters in this circuit is unetched. The shortest propagation time delay of each stage is tpd=477.3ps/stage (when Vdd=1.94V). A supply voltage Vdd dependence of oscillation frequency is shown in Fig. 17(b).

5.5 Discussion and Summary

The two transfer characteristics of the test inverters shown in Fig. 5.12 and 5.13 show that their output low tail near Vin=1.0V is bent up a little, rather than level out or decay continuously. This is due to the gate leakage of the E-driver. A typical characteristic of E-driver coupled with a typical load line is shown in Fig. 5.18. For Vg larger than 0.8V, more and more gate leakage currents for larger gate voltages in the small portion of drain voltage appear. The intersections between the load line and that of E-driver for the increased Vg's become more and more positive. This results in a slightly high output voltages of the inverter.

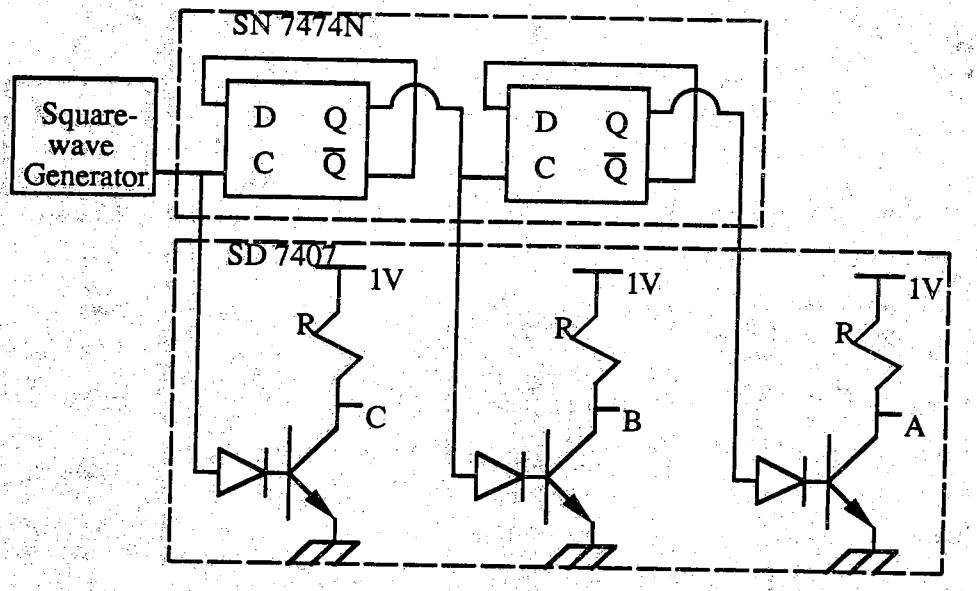
For the inverter performance consideration, in addition to the DC voltage values we have characterized in Section 5.2, another important criterion is the power dissipation. For the unetched load case, the load is always in its linear region of operation as we have discussed in Chapter 3. For the ungated D-load, the current before saturation can be calculated by:

$$I_{dl} = qn_s Wv = qn_s\left(\frac{W}{L}\right)\mu V_{dsl} \tag{5.28}$$

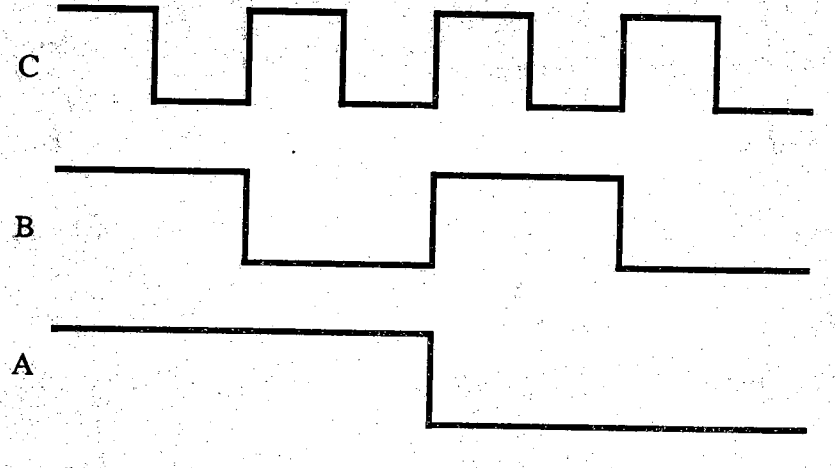
From previous discussion, the following parameters are known or calculated as

μ=6951.84 cm^2/V-sec.

n_S=4.88x$10^{11}$$cm^{-3}$

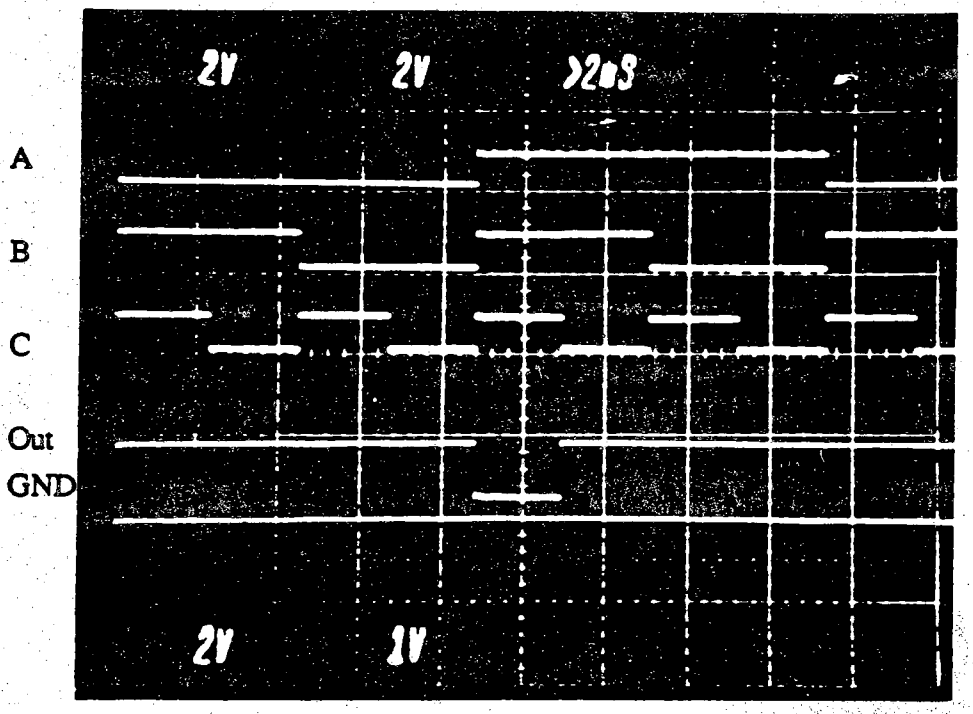


(a) waveform generator circuit.



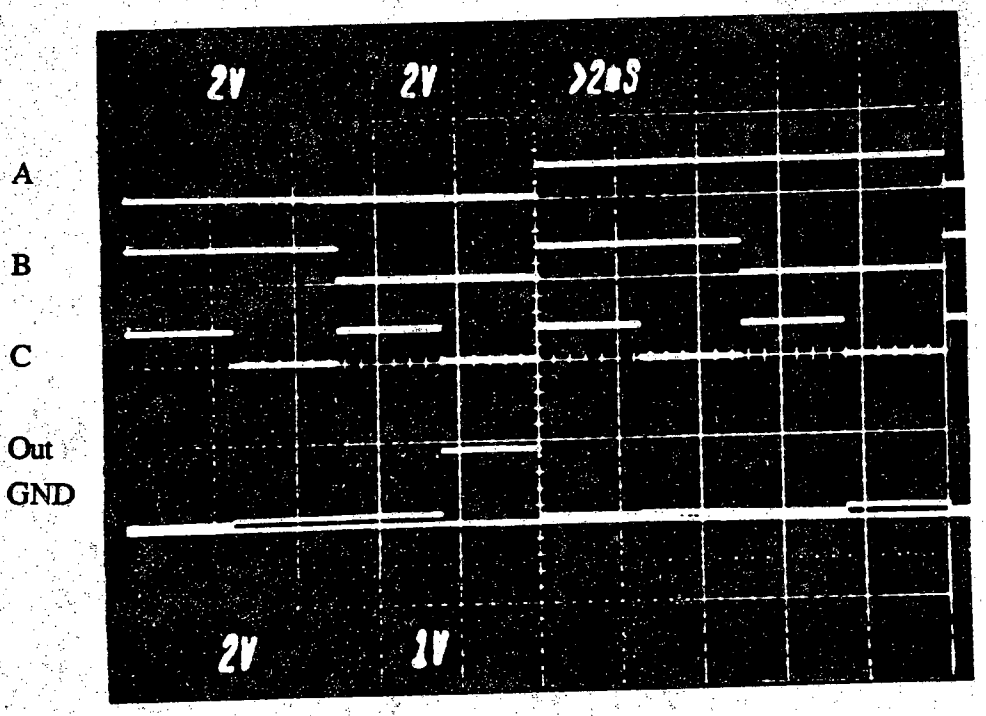
(b) output timing sequence of the generator.

Figure 5.14 Waveform generator and its output timing sequences.



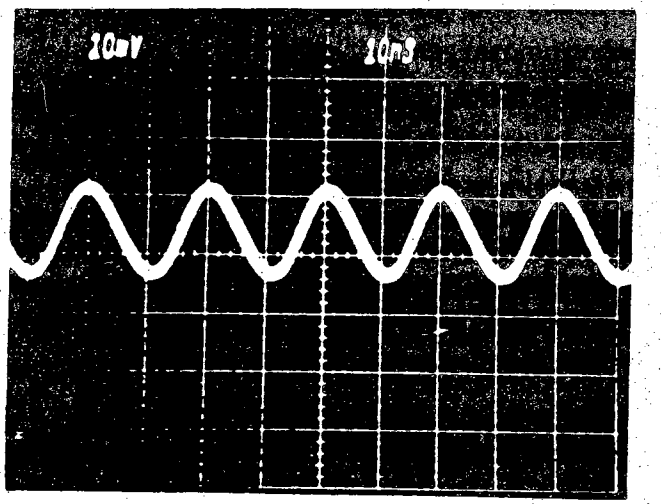
Three E-drivers: W/L=40/2, SD=6μm
Etched D-load: W/L=40/30, SD=30μm

Figure 5.15 Input and output of a 3-input MODFET NAND logic gate.

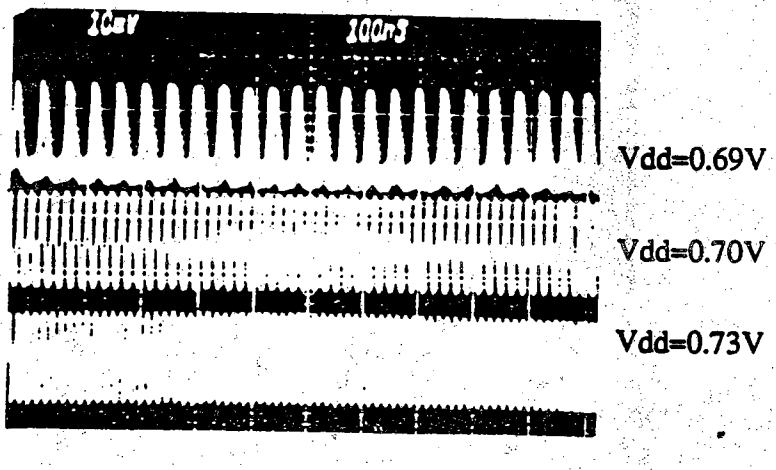


Three E-drivers: W/L=40/2, SD=6μm
Etched D-load: W/L=40/6, SD=6μm

Figure 5.16 Input and output of a 3-input MODFET NOR logic gate.

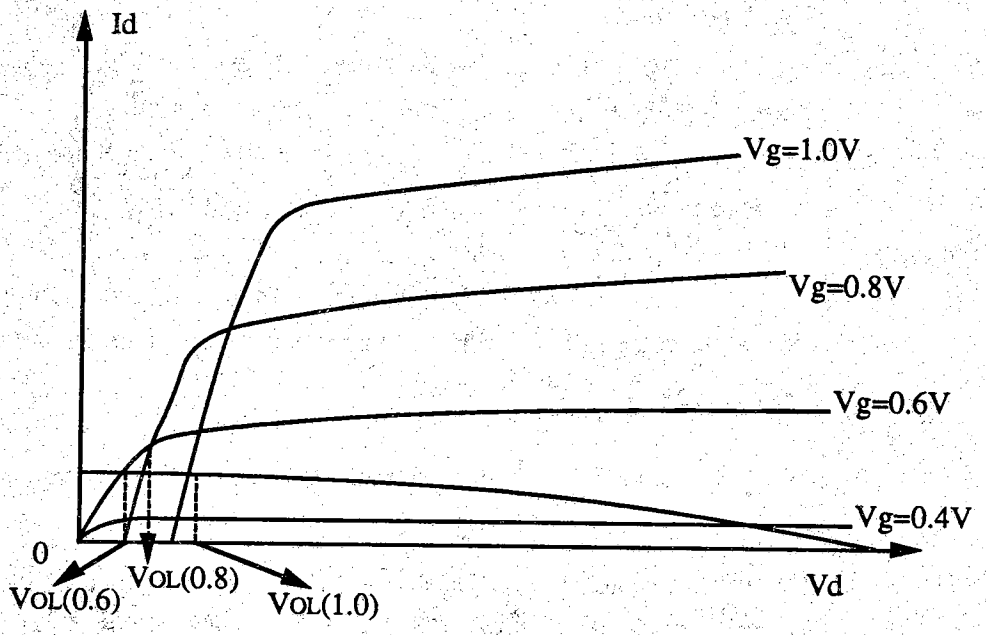


(a) oscillation waveform of an eleven-stage MODFET ring oscillator at Vdd=0.70V.



(b) oscillations of ring oscillator for three different supply voltages.

Figure 5.17 Oscillation waveforms of MODFET ring oscillator (E-drivers: W/L=40/2, SD=6μm, unetched D-loads: W/L=40/40, SD=40μm).



Vin=Vgsd	0.6V	0.8V	1.0V
Vout (Vin)	VOL(0.6)	VOL(0.8)	VOL(1.0)

$V_{OL}(0.6) > V_{OL}(0.8) > V_{OL}(1.0)$

Figure 5.18 Effect of E-driver's gate leakage on inverter's output low region.

$(W/L)_1=40/50=0.8$

$V_{dsl}=V_{dd}-V_{OL}=0.75V$

Hence

$I_{dl} = 326\mu A$

as compared to the measurement result (which will be used for the later calculation):

$I_{dl}=350\mu A$

The power of the inverter Pinv is approximated as:

$P_{inv}=I_{dl}xV_{dd}= 350\mu W$

This inverter consumes a lot of power because of its relatively large $|V_{tl}|$. Usually reduced $|V_{tl}|$ and β_1 are desired to reduce the power dissipation. The physical interpretation for this reduction is that a reduced $|V_{tl}|$ or β_1 means a more resistive load. This will results in a smaller static current from voltage supply to the ground, but a lower speed.

Likewise, the power dissipation of a ring oscillator can be calculated in the same way. For each inverter of the test ring oscillator, all parameters are the same as in the above list with the exception of $(W/L)_1=40/40=1$. Thus

$I_{dl}=437.5\mu A$

and the power P_{osc} consumed by each stage of the ring oscillator is given by

$$P_{osc}=437.5V_{dd}\ (\mu W) \qquad (5.29)$$

This expression shows a linear relationship between the power dissipation of the ring oscillator P_{osc} (mW/stage) and the voltage supply V_{dd} (V). Thus on the one hand, smaller V_{dd} is prefered to reduce the power dissipation of the circuit. However, on the other hand, an increased V_{dd} will cause a less propagation delay t_{pd}. Transient response analysis shows that the propagation delay of an inverter is primarily determined by how fast the output voltage of the inverter is pulled up from low to high by the load current, rather than pulled down from high to low by the driver. As a larger V_{dd} leads to a larger load current I_{dl}, it is apparent that this increased V_{dd} will cause a smaller time delay, as proven by the measurements shown in Fig. 5.19. The P_{osc}. vs. V_{dd} is calculated by (5.19) and is also shown in the same figure.

The choice of V_{dd} is a trade-off between the power dissipation and the propagation delay. A very important figure of merit, the product

t_{pd} (propagation delay) x P_{osc}. (power dissipation)

is usually considered to compare the performance of different ring oscillators. The curve of product $t_{pd}xP_{osc}$ vs. V_{dd} of the test MODFET ring oscillator is shown in Fig. 5.20. From this figure, the optimum figure of merit for this ring oscillator is

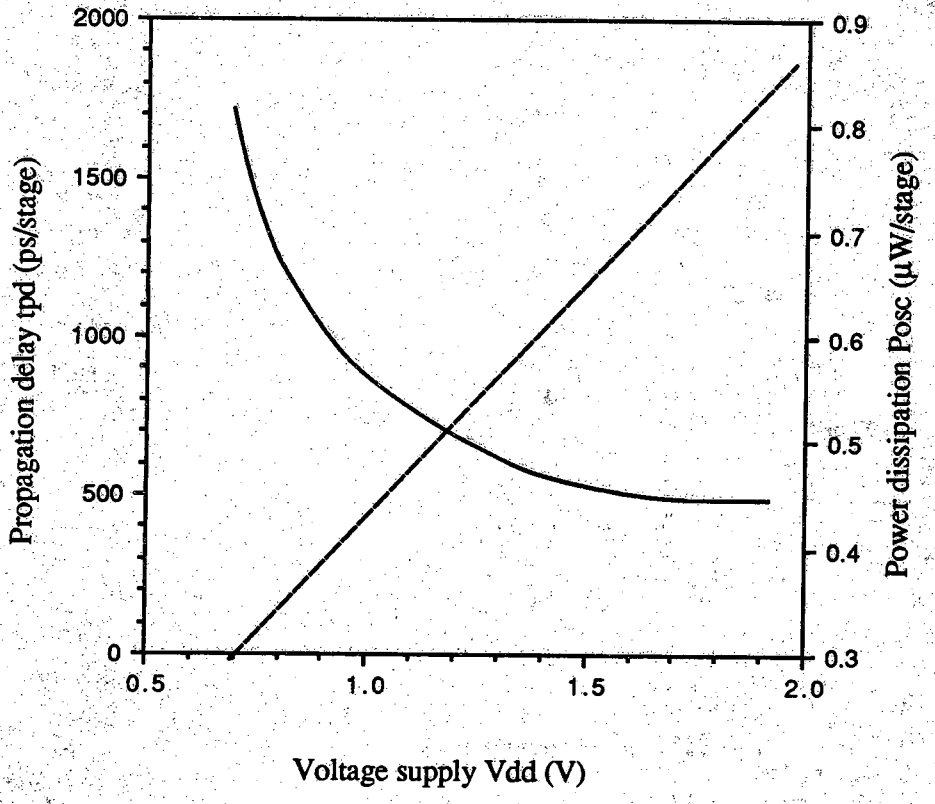


Figure 5.19 t_{pd}, P_{osc} versus V_{dd}.

$t_{pd}xP_{osc}$=372.2 fj/stage

and corresponding t_{pd}, P_{osc} and V_{dd} are:

t_{pd}=650 ps/stage

P_{osc}=573.13 μW/stage

V_{dd}= 1.31V.

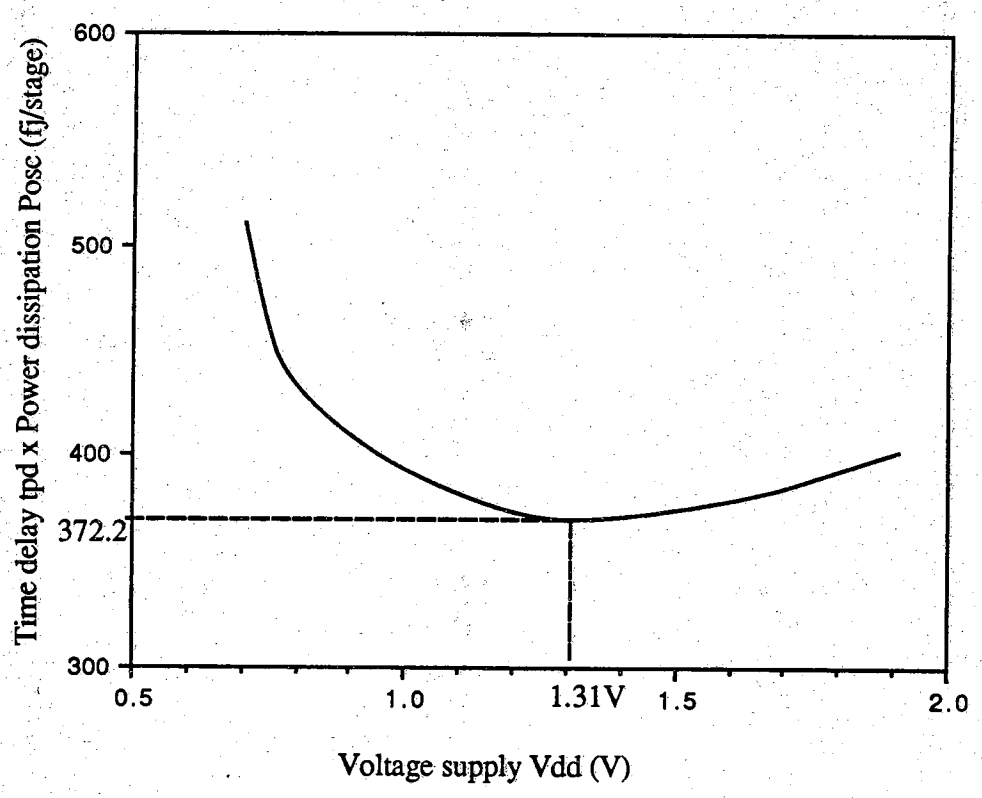


Figure 5.20 Time-power product ($t_{pd}xP_{osc}$) versus V_{dd}.

CHAPTER 6

CONCLUSIONS AND RECOMMENDATION FOR FUTURE WORK

GaAs MODFET DCFL E/D type circuits and fabrication technology have been developed by this work. Several goals have been achieved.

The enhancement-mode MODFET's with 2μm gate lengths defined by totally optical lithography have demonstrated the transconductance as high as 50.50 ms/mm. A series of experiments on the contact alloy cycle have been conducted. The specific contact resistivity and width-normalized contact resistance as low as 4.95×10^{-5} Ω-cm^2 and 3.02 Ω-mm, respectively, have been accomplished. Research on the gate recess etch has led to an acceptable threshold voltage uniformity. The threshold voltages of enhancement-mode devices across the 6mmx9mm wafer ranged from 0.319V to 0.466V with a mean value of 0.38V and standard deviation of 44mV for the 17 transistors measured.

All types of DCFL circuits designed and fabricated on the test chip are working well. The E/D type inverters have demonstrated noise margin of $NM_L = 0.22V$, $NM_H = 0.45V$ and logic swing of $V_I = 0.88V$. The three-input NAND and NOR logic gates have exhibited correct logic functions. MODFET ring oscillators with E/D type inverters have been successfully built. The shortest propagation time delay of 477.3 ps/stage, the optimum time-power product of 372.2fj/stage at $V_{dd} = 1.31V$ and power dissipation of 573.1μW/stage (at 300K) have been demonstrated by an eleven-stage ring oscillator with two additional output inverter stages.

After progress has been made in basic MODFET circuits as presented in the previous chapters, larger and better circuit applications are goals for future work. For this purpose, better control of the process and improved device performance are necessary. Two primary recommendations are made for these concerns.

First, for further transconductance improvement, both MBE film structure and device geometrical dimensions need to be improved. As mentioned in Chapter 5, the thick spacer layer of the Perkin Elmer MODFET film used at Purdure is optimized for carrier mobility, rather than transconductance. A thinner spacer layer may be used for better transconductance performance. Also, a relatively large source-to-drain spacing,

6μm, has been used for the process runs up to now. A spacing reduction is necessary to reduce the source to drain serial resistance. But this reduction is limited by the optical lithography. Much smaller spacings can be achieved by e-beam direct-write. Gate lengths of 0.5μm and source-to-drain spacing of 3.5μm can be easily achieved by this technique. Additionally, large source and drain resistance is primarily attributed to the large contact resistance, which causes the poor transconductance as mentioned in Section 5.5. Despite some work which has been done on this so far, more effort is necessary. The specific contact resistivity as low as $5x10^{-8}\Omega$-cm^2 or width-normalized resistance of 0.035Ω-mm has been reported.(49) Further study and experiments on the contact and it's alloy cycle as discussed in Chapter 3 are needed.

Second, a better control on the threshold voltage or gate recess etch is desired. A pH controlled etch is worth trying for its simplicity. By controlling the pH value of the recess etch solution at the value of 7.1 with a high-resolution pH meter, a good uniformity of threshold voltage with small variation of 70mV for several runs has been accomplished.(11) Much better results can be achieved by dry reactive ion etch (RIE). This technique is strongly recommended in spite of its complexity. Threshold voltage variation as small as 4mV across the 10mmx10mm wafer has been reported using this method.(20) This impressive result shows the necessity of this technique for high quality MODFET DCFL circuits. The RIE and self-stopping-layer technique makes use of former's high selectivity between GaAs and AlGaAs. A very thin stop layer, GaAs, is included to the doped AlGaAs during MBE growth of film. The AlGaAs thickness below the stop GaAs layer which is required for the threshold voltage of the enhancement-mode device is calculated and controlled precisely during MBE growth. Then, on top of the thin GaAs stop layer, another AlGaAs layer is grown to produce the desired thickness for the threshold voltage of depletion-mode MODFET. RIE is then applied to remove the cap n+ GaAs layer on the depletion-mode gate areas and recess through the GaAs stop layer on the enhancement-mode gate regions. Accurate threshold voltages for both E-mode and D-mode MODFET's will be achieved. The details of the RIE dry etch for the MODFET 's are discussed in Reference (19), (20), (24), (26) and (60).

Better mask layout can contribute a lot to the improvements of circuits. For the example of the ring oscillator, the propagation delay is primarily due to the pull-up procedure and the value of the load capacitance has a dramatic impact on the speed. The major portion of the load capacitance is the gate capacitance of the next stage. So the area of the gate and interconnect metal between the output of one stage to the gate of the next

stage must be reduced as small as possible. To reduce this area and capacitance, one layout example is illustrated in Fig. 6.1. This design aligns the gate of each stage straight to the output of the previous stage, rather than to the gate as we did. The area of the interconnect metal or load capacitance is thus reduced greatly.

Finally, a planar process realized by implant isolation is recommended for the more complicated circuit implementations. As mentioned earlier, the mesa etch may cause open circuits if the gate and interconnect metal is not deposited thick enough to cover the mesa step. For the relatively simple circuits we have built on the test chips, mesa etch is an acceptable method for simplicity. However, for large scale integrated circuits, the probability of open circuits due to the mesa depth will be increased.

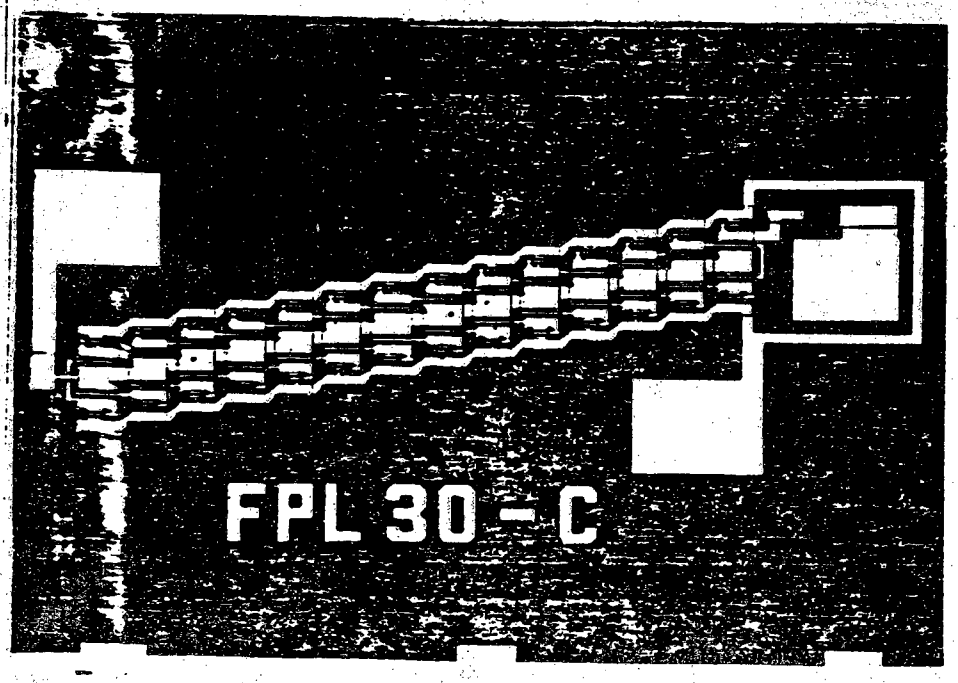


Figure 6.1 A ring oscillator designed with the reduced load capacitances.(59)

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APPENDIX

APPENDIX

MODFET Runsheet (Optical Process)

1) Obtain film

Film cross-section:

Semi-insulating GaAs substrate
1.0 micron undoped GaAs
200 Å undoped (Al,Ga)As
600 Å n+(Al,Ga)As
50 Å n+ GaAs

2) Mount sample on Si wafer

Solder with Indium

MASK 1:

3) Define mesa pattern

Prebake sample @ 120^0C for 15 minutes
Deposit AZ-1350J-SF positive photoresist
Spin @4400 rpm for 40 seconds
Softbake resist @ 90^oC for 15 minutes
Align and expose mesa mask (Suss Aligner)
Exposure time: 6 seconds
Exposure units: 275w
Exposure Mode: HP
Develop resist
Developer: 1 AZ Developer : 1 DI
Develop time: 30 seconds
Rinse time: 40 seconds (DI)

Inspect pattern

Hardbake resist @ 120° C for 20 minutes

4) Mesa Etch

Wet Etch

Solution: 1 H_2SO_4 : 1 H_2O_2 : 24 DI

Depth: 5000Å

Rate: approximately 50 Å/second

Time: 100 seconds

NOTE:

Add H_2SO_4 to DI

Wait for temperature to fall to 35 °C.

Add H_2O_2, wait 30 seconds.

Perform etch.

DI rinse

N_2 blow dry

Strip resist with Aceton

Methanol rinse

DI rinse

N_2 blow dry

Record depth and each rate (Tencor Alpha Step)

NOTE: Perform etch on GaAs sample first to calibrate etch rate. Use identical DI temperature and time delay for both.

MASK 2:

5) Define Ohmic Contact Pattern

Prebake @ 120°C for 15 minutes

Deposit AZ-1350J-SF positive photoresist

Spin @ 4000 rpm for 30 seconds

Softbake resist @ 65°C for 15 minutes

Align and expose contact mask

Exposure time: 6 seconds

Exposure units(power): 275w

Exposure Mode: HP

Aid liftoff with 14 minute soak in Chlorobenzene

Develop resist

Develop solution: 1 AZ Developer : 1 DI

Develop time: 70 seconds

Rinse time: 40 seconds (DI)

Inspect pattern

6) Ohmic Contact Evaporation

Oxide Etch

Etch solution: 1 NH_4OH : 40 DI

Etch time: 30 seconds

DI rinse

N_2 blow dry

E-beam Evaporation (Varian system)

Ni	50 Å	262 Hz
Ge	500 Å	1,565 Hz
Au	1000 Å	11,353 Hz
Ni	300 Å	1,571 Hz
Au	300 Å	3,406 Hz
Ti	1000 Å	2,653 Hz
Au	2000 Å	22,706 Hz

7) Liftoff Pattern

Aceton soak

(Use Aceton filled squirt bottle)

Methanol rinse

DI rinse

N_2 blow dry

Inspect pattern

8) Alloy Ohmic Contacts

Open tube N_2 furnace (Marshall furnace)

Alloy @ 450°C for 5 minutes

Inspect contacts (should be brownish and bubbly for Au/Ge)

MASK 3:

9) Define Gate Recess Pattern for D-mode Load
   Prebake @120°C for 15 minutes
   Deposit AZ-1350J-SF positive photoresist
      Spin @ 4400 rpm for 40 seconds
   Softbake resist @ 70° C for 15 minutes
   Align and expose gate recess mask
      Exposure time: 5.75 seconds
      Exposyre units (power): 275w
      Exposure Mode: HP
   Develop resist
      Develop solution: 1 AZ Developer : 1 DI
      Develop time: 85 seconds
      Rinse time: 40 seconds (DI)
   Inspect pattern

10) D-mode Load Recess Etch:
   Wet Etch
      Solution: 2 H_2SO_4 : 1 H_2O_2 : 500 DI
      Time: (determined by electrical monitoring) 30-45 seconds
      Rate: 2.25 Å / second
         Depth: (determined by electrical monitoring) the current should be about five times smaller than its initial magnitude.
   DI rinse
   N_2 blow dry
   Strip resist with Aceton
      Methanol Rinse
      DI Rinse
      N_2 blow dry

MASK 4:

11) Define Gate Recess Pattern for E-mode Driver
   Prebake @ 120°C for 15 minutes

Deposit AZ-1350J-SF positive photoresist
Spin @4400 rpm for 40 seconds
Softbake resist @70°C for 15 minutes
Align and expose gate recess mask
Exposure time: 5.75 seconds
Exposure units (power): 275w
Exposure Mode: HP
Develop resist
Develop solution: 1 AZ Developer : 1 DI
Develop time: 85 seconds
Rinse time: 40 seconds (DI)
Inspect pattern

12) Gate Recess Etch
Wet Etch
Solution: 2 H_2SO_4 : 1 H_2O_2 : 500 DI
Time: (determined by electrical monitoring) 60-75 seconds
Rate: 2.25 Å / second
Depth: (determined by electrical monitoring) about 160-180Å
DI rinse
N_2 blow dry
Strip ressit with Aceton
Methanol Rinse
DI Rinse
N_2 blow dry

MASK 5:

13) Define Gate Metal Pattern
Prebake @ 120° C for 15 minutes
Deposit AZ-1350J-SF positive photoresist
Spin @ 4000 rpm for 30 seconds
Softbake resist @ 65 °C for 15 minutes
Align and expose metal mask
Expoaure time: 5.5 seconds

Exposure power: 275w

Exposure Mode: HP

Aid liftoff with 14 minute soak in Chlorobenzene

Develop resist

Develop solution: 1 AZ Developer : 1 DI

Develop time: 85 seconds

Rinse time: 40 seconds

Inspect pattern

14) Gate Metal Evaporation

Oxide etch

Etch solution : 1 NH_4OH : 40 DI

Etch time: 30 seconds

DI rinse

N_2 blow dry

E-beam Evaporation (Varian System)

Ti	500 Å	1326 Hz
Au	4000 Å	45,412 Hz

15) Liftoff Pattern

Aceton soak

(Use Aceton filled squirt bottle)

Methanol rinse

DI rinse

N_2 blow dry

16) Inspect MODFETS