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# Measurements of Carrier Generation- Recombination Parameters in Silicon Solar Cell Material Using MOS Techniques

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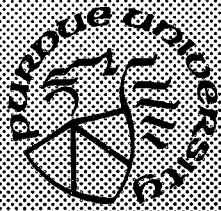
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# **Measurements of Carrier Generation-Recombination Parameters in Silicon Solar Cell Material Using MOS Techniques**

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**MEASUREMENTS OF CARRIER GENERATION-RECOMBINATION  
PARAMETERS IN SILICON SOLAR CELL MATERIAL  
USING MOS TECHNIQUES**

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## ABSTRACT

Modified and new measurement techniques were developed for determining the carrier generation-recombination (G-R) parameters in silicon solar cell material under carrier deficit and low-level carrier excess conditions using MOS-based test structures. The structures mainly consisted of ring-dot MOS-Capacitors (MOS-C) and Schottky-Drained Gate-Controlled Diodes (SGCD). Sample G-R parameters were extracted from n-type high quality silicon solar cell material. Additional measurements were also performed on low-quality n-type silicon substrates for comparison purposes.

The photoaccelerated MOS-C Capacitance-time (C-t) transient measurement technique, modified from the standard C-t method, allows one to drastically reduce the observation time in deducing the carrier generation lifetime ( $\tau_g$ ) by simply illuminating the test structure during the transient. In applying the technique to MOS-C's (which exhibited generation lifetime on the order of 1 msec) the observation time was reduced by approximately an order of magnitude. This is important in dealing with solar cell material because of typically long generation lifetimes.

The SGCD structure, which consisted of an extended Schottky diode located next to an MOS-C, was developed and utilized for extracting the

surface generation velocity ( $s_g$ ). The measurement is based on recording two C-t transients at  $V_D = 0$  and at  $V_D = V_T$ , respectively. The structure has a distinct advantage over the conventional PN junction GCD in that it is only slightly more complicated to fabricate and interrogate than a simple MOS-C. It was also demonstrated that steady-state deep-depletion C-V characteristics can be obtained using the SGCD structure.

An MOS-C photo/forward-sweep measurement technique was primarily developed to extract the recombination lifetime ( $\tau_p$  for n-type substrates) under low-level carrier excess conditions. The new technique is based on the change in inversion capacitance in response to a set of illumination and forward-sweep voltages applied to the MOS-C. The technique conveniently allows one to extract the recombination lifetime under room temperature conditions and was successfully applied to MOS-C's fabricated on high quality silicon solar cell substrates.



## CHAPTER 1 INTRODUCTION

Carrier generation-recombination (G-R) is one of the major fundamental processes which influences the characteristics and eventually dictates the performance of semiconductor devices. In the area of silicon solar cell design, one of the criteria for achieving high energy conversion efficiency is to minimize carrier generation-recombination rates throughout the device, i.e., in the bulk and at the surfaces [1-4]. A proper characterization of carrier generation-recombination is, therefore, a key requirement prior to further cell improvements.

While today's silicon substrates used in solar cell fabrication are of high quality, it is the subsequent wafer processing which inevitably introduces unintended impurities into the substrates [5,6], hence increases undesirable generation-recombination rates and ultimately degrades the cell performance. Consequently and logistically, test structures built on processed solar cell substrates should be employed for the characterization of carrier generation and recombination. In this work, Metal-Oxide-Semiconductor (MOS)-based test structures were utilized for the generation-recombination measurements. As will be detailed in the Research Overview, the work described in this writing is in fact a portion of a larger research program; cited MOS-based measurements were developed as a correlation technique for characterizing carrier generation-recombination in processed silicon solar cell material.

The two parameters used to characterize carrier generation are generation lifetime ( $\tau_g$ ) and surface generation velocity ( $s_g$ ), which describe the bulk and surface generation respectively. Similarly, recombination lifetime ( $\tau_r$ ) and surface recombination velocity ( $s_r$ ) are the corresponding parameters for characterizing carrier recombination.  $\tau_g$  and  $\tau_r$  are different from, but related to, each other under certain conditions [7]. A similar statement can be made for  $s_g$  and  $s_r$ . For silicon solar cell material with minimal carrier generation-recombination rates, both  $\tau_g$  and  $\tau_r$  are expected to be large in magnitude

whereas  $s_g$  and  $s_r$  are projected to be small. Ideally, one would like to determine all four parameters using the same test structure. In reality, however, one or two of the mentioned parameters are typically determined with a given device. Herein, we describe and illustrate modified or new techniques developed for the determination of  $\tau_g$ ,  $s_g$  and  $\tau_r$  in processed solar cell material using MOS-based test structures.

## 1.1 Literature Review

### 1.1.1 General Overview

A survey of lifetime measurement techniques in 1968 yielded 300 papers published during the period from 1949-1967 [8]; and it is undoubtedly safe to speculate that an equivalent or greater number of papers have been published since 1967. There are at least forty lifetime measurement techniques available today [9,10], and additional techniques are under continuous development. Understandably, it would be difficult, if not impossible, to give a thorough and direct comparison of the techniques. The measurements, however, can be grouped into two general categories. The first category includes those techniques which are performed on bulk substrates (and which are therefore of limited interest herein). Major approaches include photoconductivity decay [11], surface photovoltage [12], and the photoelectromagnetic method [13].

The second category involves measurements which require the use of test structures such as PN junctions, gate-controlled diodes and MOS-Capacitors (MOS-C). In particular, PN junctions with different configurations have been extensively employed for extracting  $\tau_r$  and  $s_r$ . Major measurement techniques such as spectral response [14,15], open-circuit voltage decay and short-circuit current decay [16-20] are frequently used for extracting  $\tau_r$ . While the use of a PN junction is an apparently logical choice for measuring  $\tau_r$  in solar cell work, difficulties are often encountered in interpreting results. For example, the carrier recombination process may be influenced by band-gap narrowing and Auger recombination [21-23] associated with heavy doping effects.

The gate-controlled diode (GCD) [24,25], which consists of a PN junction surrounded by an MOS-C, is another popular test structure. It has been widely used for both  $s_g$  and  $\tau_g$  measurements. Unfortunately, Pierret and Pierret et al [26,27] have shown that in order to deduce the true  $s_g$  parameter,

the dimension of the MOS-C gate must be less than or approximately equal to the carrier's effective diffusion length in the silicon surface channel. This tends to complicate the configuration and fabrication of the GCD [28].

Because of its fabrication and interpretational simplicity, the MOS-Capacitor is perhaps the most frequently employed carrier generation-recombination test structure. The majority of experimental results presented herein are derived from standard or modified MOS-Cs. A more detailed review of published MOS-C-based measurement techniques is given in the next two subsections.

### 1.1.2 MOS-C Carrier Generation Studies

Various methods have been developed for the determination of generation lifetime and/or surface generation velocity using the MOS-C test structure. These methods, when classified according to the type of perturbation applied to the MOS-C, can be grouped into pulsed gate voltage techniques and voltage sweep techniques. All measurement techniques, nevertheless, are commonly based on the response (mostly capacitance response) of the MOS-C after it is driven into deep depletion. The pulsed MOS-C Capacitance-time (C-t) transient method was first introduced by Jund and Poirier [29] to extract  $\tau_g$ . In the Jund and Poirier measurement, the MOS-C was initially biased under accumulation conditions. It was then suddenly switched from accumulation to deep depletion by application of a large inverting gate voltage step (commonly referred to as pulsed voltage). The capacitance response was then recorded as a function of time as carriers were thermally generated, relaxing the MOS-C to equilibrium inversion. The original analysis of the C-t transient performed by Jund and Poirier was incorrect; the minority carrier generation rate was assumed to be proportional to the rate of change in depletion width. Consequently,  $\tau_g$  was incorrectly deduced.

A more detailed analysis of the C-t transient was later given by Zerbst [30]. Two major modifications were introduced. First, an additional generation component associated with the gated surface was included. The surface generation rate was assumed to be constant throughout the transient. Second, carriers were noted to be generated in only a portion of the depletion region. The second modification was important because of a rapidly decreasing generation rate near the edge of the depletion region. With the above changes, a plot of  $-d(C_O/C)^2/dt$  versus  $C_F/C-1$  (commonly referred to

as Zerbst plot) was constructed from the measured C-t transient;  $C_0$  is the oxide capacitance and C is the instantaneous capacitance at time t during the transient. The generation lifetime and the gated surface generation velocity were then derived, respectively, from the linear slope of the plot and the extrapolated  $-d(C_0/C)^2/dt$  axis.

Heiman [31] simplified Zerbst's analysis by neglecting the gated surface generation component. He pointed out that Zerbst's assumption of a constant gated surface generation rate throughout the transient was incorrect: once an inversion layer was formed, the surface states were filled by minority carriers and subsequently the gated surface generation rate should be reduced. The simplification meant that  $\tau_g$  could be obtained by measuring C and  $dC/dt$  at any point on the C-t curve. While the method allows one to determine  $\tau_g$  rapidly, the value obtained is sensitive to point chosen on the C-t curve and is typically inaccurate.

Huang [32] published an analysis similar to that performed by Heiman. He also assumed that the capacitance change was caused solely by carrier generation inside the depletion region, and hence repeated the Heiman mistake in extracting  $\tau_g$ .

Schroder et al [33,34] first noted the importance of lateral surface generation, a carrier generation component which was previously ignored, on the general behavior of the C-t transient and the corresponding Zerbst plot. The lateral surface region, which is depleted of carriers and hence gives rise to lateral surface generation, is an extension of the depletion region beyond the gate periphery. Assuming that the width of the laterally depleted surface was the same as the width of the depletion region, they showed that the generation parameter deduced from the Zerbst plot was not the true lifetime, but an effective generation lifetime ( $\tau'_g$ ).  $\tau'_g$  is a function of  $\tau_g$ ,  $s_g$  and the P/A ratio; P and A are respectively the perimeter and area of the MOS-C gate. For a given  $s_g$  (which is typically small for a properly processed MOS-C), it is important to employ MOS-Cs of large dimension so as to minimize the error in deducing the true generation lifetime. In addition, since the gated surface generation is reduced once an inversion layer is formed, the extrapolated intercept of the Zerbst plot should not be interpreted as the surface generation velocity.

Noticing the dependence of the lateral surface generation on the perimeter to area ratio, Kano et al [35] proposed to measure  $\tau_g$  and  $s_g$  using MOS-Cs of different radii. However, since both  $\tau_g$  and  $s_g$  vary from device to device across the wafer surface, the proposed method is in general

inapplicable.

A similar approach was given by Rabbani et al [36]. Capacitors of varying perimeter to area ratio were used. They considered not only the lateral surface generation but also accounted for the lateral volume generation of the extended depletion region. Since their method also relies on several capacitors (each with its own  $\tau_g$  and  $s_g$ ) to extract a single value of  $\tau_g$  and  $s_g$ , the technique has the same disadvantage as that of Kano.

Calzolari et al [37,38] showed that by measuring both the C-t and I-t transients, where I is the external current,  $\tau_g$  and  $s_g$  could be determined from the plot of I versus  $(1/C - 1/C_F)$ . The measurement procedures are slightly complicated because two correlated measurements are required.

A pulsed I-t transient method was implemented by Trullemans et al [39];  $\tau_g$  was evaluated from the I-t data at  $t=0$ . Since  $\tau_g$  was determined from only one point, namely the data point at  $t=0$ , the response time of the measurement system has to be taken into account. Moreover, the extraction of  $\tau_g$  is expected to be inaccurate because the surface generation rate is highest at  $t=0$ .

A graphical scheme was developed by Pierret [40] for the rapid determination of  $\tau_g$  using three points on the C-t curve. The merit of the approach is no lengthy data manipulation is required. The C-t curve, however, must be "well-behaved".

Yue et al [41] also developed a fast extrapolation technique for determining  $\tau_g$ . Instead of waiting for the complete recovery of the capacitance, a time  $t_0$  is arbitrarily chosen to end the measurement. The total recovery (transient) time,  $t_s$ , is then extrapolated from a  $\ln W$  vs  $t$  plot;  $W$  is the depletion width computed from the capacitance. One then calculates  $\tau_g$  using the extrapolated  $t_s$  value and an additional capacitance-time information obtained at any point on the C-t curve. The extracted  $\tau_g$ , however, can be quite inaccurate if the measurement time,  $t_0$ , is not properly chosen (which, unfortunately, is an arbitrary parameter). One may have to repeat several measurements using different  $t_0$  values in order to achieve a greater degree of confidence in  $\tau_g$  results.

Keller [42] instituted a major modification of measurement procedures. Instead of recording a complete C-t curve, he sampled various portions of the C-t transient by periodically pulsing the MOS-C with different voltage magnitudes. Before each pulse was applied, the nonequilibrated MOS-C was

rapidly restored to the equilibrium inversion by illuminating the device. In this way the measurement time is reduced. The instrumentation setup is, however, quite complicated.

As mentioned before, a second group of  $\tau_g$  measurement methods can be generally classified as voltage sweep techniques. Historically, Pierret [43] was the first to introduce the linear voltage sweep technique for determining  $\tau_g$ . This nonpulse method is based upon the C-V characteristics of the MOS-C in response to a linear voltage sweep creating deep depletion conditions. For a given sweep rate R, the deeply-depleted capacitance will eventually saturate at some point ( $C_{sat}$ ) after application of the sweep. A set of linear-sweep curves are recorded and a plot of R versus  $(C_F/C_{sat} - 1)$  is constructed. This plot is identical, in information content, to the Zerbst plot. For long lifetime devices, the experimental observation time can be quite lengthy and there may also be some question as to whether the capacitance has truly saturated. Subsequently a modified linear sweep technique was proposed by Pierret and Small [44]. In the modified method, a preselected deep-depletion capacitance was maintained at a constant value by adjusting the sweep rate. This is accomplished using a bias supply circuit.

Using a dot-dual ring MOS-C structure, Small and Pierret [45] developed a "subtraction" method based on the modified linear sweep technique. In the subtraction method one can separate the depletion region generation and the lateral surface generation. Their method allows one to accurately determine  $\tau_g$  and estimate  $s_g$ .

Using the modified linear sweep method, both Eades et al [46] and Hof et al [47] performed measurements on single-dot capacitors of different perimeter to area ratio in an attempt to separate  $\tau_g$  and  $s_g$ . Their methods are of limited application since  $\tau_g$  and  $s_g$  vary from device to device across the wafer surface.

Gorban et al [48] modified the analysis of the linear sweep method by accounting for the dependence of  $s_g$  on the inversion charge density. The technique was based upon non-equilibrium C and dC/dV measurements at a given sweep rate. However, such dependence is typically negligible.

A triangular voltage sweep technique was later developed by Taniguchi et al [49]. It utilized both reverse sweep (from inversion towards deeper depletion) and forward sweep. While the measurement time for acquiring experimental data is reduced, the time to extract  $\tau_g$  and  $s_g$  is lengthened

because a family of graphical curves has to be generated prior to data analysis.

Lin [50] also used the triangular voltage sweep method and related  $\tau_g$  to the slopes of the forward and reverse swept C-V curves evaluated at a chosen deep-depleted capacitance. The measurement is simple but the inaccuracy in determining the slopes typically introduces unacceptable error in  $\tau_g$ .

As a final observation: of the many available measurement methods, the pulsed C-t transient technique has remained as one of the most widely-used methods for extracting  $\tau_g$ . The technique is well established not only because of its simplicity in measurement, but also due to the emergence of automated data acquisition and computer analysis. The pulsed C-t technique (either in standard or modified form) constitutes the major analytical tool employed in this work.

### 1.1.3 MOS-C Carrier Recombination Studies

The measurement of the carrier recombination lifetime using the MOS-C was first performed by Tomanek [51] in 1969. In his method, the MOS-C was initially biased into inversion. Under this condition, an inversion layer of minority carriers was formed underneath the interface. The MOS-C was then momentarily pulsed from inversion to accumulation. Consequently, the minority carriers became excess carriers and gradually recombined in the bulk of the MOS-C. Right after the termination of the pulse, the MOS-C was deeply depleted, and the remaining excess minority carriers — those that did not recombine during the pulse time — were drawn back to the interface. The amount of recombined carriers,  $\delta Q$ , was computed from the capacitances recorded before and after the pulse. Assuming a simple decreasing-exponential relationship between carrier concentration and time, Tomanek constructed a semilog plot of  $\delta Q$  versus  $\delta t$ , where  $\delta t$  is the pulse duration, and deduced  $\tau_r$  from the slope of the plot. One problem with the method was the assumption that there was no variation of surface state charge during the pulsing period. This assumption is incorrect; surface states do introduce an error in the  $\delta Q$  measurements. Another disadvantage is that the measurement time is comparable to  $\tau_r$ , which is typically on the order of microseconds.

Calzolari et al [52] later extended and modified Tomanek's method. Additional factors which might affect the measurements were evaluated;

namely, high level carrier injection, lateral diffusion of minority carriers and the surface state effect. Modifications of the measurement included pulsing the MOS-C from inversion to flatband conditions (hence reducing the surface state effect), and monitoring the change in minority carrier concentration directly with an electrometer. Their experimental semilog  $\eta$  versus  $\delta t$  plots, where  $\eta$  is the normalized residual minority charge, always deviated from the theoretical unity intercept on the  $\eta$ -axis. They concluded that the deviation was caused by surface states.

Hillen et al [53,54] re-examined the analysis given by Calzolari et al and suggested that both surface states and the incomplete return of minority carriers accounted for the non-ideal  $\eta$ - $\delta t$  observation.

Tomanek's carrier injection scheme was also adopted and modified by Wei et al [55] for determining  $\tau_r$ . To minimize the surface state effect, the MOS-C was again never pulsed into accumulation. An approximate diffusion model, which included the incomplete return of minority carriers, was developed. The resultant analysis showed that the remaining (not-recombined) minority carriers did not follow the simple decreasing-exponential dependence on the pulse width. Experimentally, device lags (the fraction of injected minority carriers) were measured for a set of pulse widths.  $\tau_r$  was then varied to fit the measured data and was subsequently determined when a best fit was obtained. The lag measurements, however, are very complicated as a correction must be made for each measured data point during the data analysis.

An alternate scheme to create excess carriers inside the MOS-C, as suggested by C. St. L. Rhodes et al [56], was to illuminate the back side of the MOS-C. In the cited measurement, the pulsed C-t transient response of the illuminated MOS-C was mainly due to the photogenerated minority carriers. The requirement of incorporating an aperture in the back metallization, however, greatly complicates the proposed measurement.

A different approach was introduced by D. K. Schroder et al [57,58] for determining  $\tau_r$ . The technique involved measuring the pulsed C-t transient at elevated temperatures. The underlying principle is based on the dominance of the quasi-neutral bulk generation over the depletion region generation at high temperatures. When the dominance occurs, a plot of  $1-(C_i/C)^2$  versus  $t$  should reveal a linear characteristic;  $C_i$  is the initial capacitance at  $t=0$ .  $\tau_r$  is then deduced from the constant slope of the plot. M. Aminzadeh et al [59] extended Schroder's method and showed that, as the area of the MOS-C



decreases, lateral quasi-neutral bulk generation must be accounted for to obtain an accurate  $\tau_r$  determination. While Schroder's method is convenient for extracting  $\tau_r$ , the method is of limited utility since  $\tau_r$  is often a function of temperature [60,61].

## 1.2 Research Overview And Thesis Organization

As pointed out in the preceding introduction, one of the design criteria for improving the silicon solar cell performance is to minimize carrier generation-recombination rates. The generation-recombination rates, in turn, are closely related to processing. As a result, appropriate test structures, together with a systematic measurement approach, must be employed to characterize carrier generation-recombination.

The goal of the overall research program was to develop reliable diagnostic measurement techniques which were capable of extracting the desired generation-recombination parameters systematically and unambiguously over a broad range of excitation conditions. Two complimentary measurement approaches were adopted, and pursued in parallel, for achieving the cited goal. The first approach (under development by the author's colleague, Fati Sani) was to employ infra-red free carrier absorption for determining  $\tau_r$  and  $s_r$  under various carrier excess conditions. The second approach, which is the author's research domain, was to establish MOS-based measurement techniques for providing generation-recombination information under carrier deficit and low-level carrier excess conditions. It should be noted that the MOS-based measurement methods pursued by the author were envisioned in part as a means of checking, or at least correlating, the results derived from the highly-novel infra-red free carrier absorption measurement method.

The remainder of the thesis is organized as follows. In Chapter 2, background information are provided which include a brief review of carrier G-R statistics, the establishment of expressions for the four carrier G-R parameters ( $\tau_g$ ,  $s_g$ ,  $\tau_r$  and  $s_r$ ) and their relationships to the G-R rates. In addition, the measurement concepts for extracting the carrier G-R parameters is also qualitatively introduced, followed by a concise review of the standard pulsed MOS-C C-t transient analysis. Next, the general wafer processing steps, test structure fabrication procedures and three measurement set-ups are described and summarized in Chapter 3. In Chapter 4, the determination of

generation parameters using modified C-t techniques are explained and illustrated. Chapter 5 is entirely devoted to the presentation of a new technique for extracting the recombination lifetime. Lastly, a summary and conclusion are given in Chapter 6.

## CHAPTER 2

### CARRIER G-R PARAMETERS AND MEASUREMENT CONCEPTS

There are different kinds of carrier G-R processes. For silicon, which is an indirect bandgap material, the dominant G-R process is that which proceeds via G-R centers located within the silicon bandgap. These G-R centers can be envisioned as stepping stones for the carriers. For a nondegenerate semiconductor, the indirect carrier G-R is best described by Shockley-Read-Hall (SRH) statistics [62,63].

According to the spatial origins, carrier G-R can be respectively classified as bulk and surface G-R. In particular, the surface that we are interested in is the  $\text{SiO}_2$ -Si interface, since it is the basic surface constituent of MOS-based test structures. The two parameters used to characterize carrier generation are generation lifetime ( $\tau_g$ ) and surface generation velocity ( $s_g$ ). In a like manner, the corresponding parameters for characterizing carrier recombination are the recombination lifetime ( $\tau_r$ ) and surface recombination velocity ( $s_r$ ).

In this chapter, the SRH formalism of the bulk carrier G-R statistics is briefly reviewed. Next, expressions are established for  $\tau_g$  and  $\tau_r$  corresponding to carrier deficit and low-level carrier excess conditions, respectively. A similar analysis for the surface G-R statistics is then examined. This eventually leads to general expressions for  $s_g$  and  $s_r$ . Following the establishment of carrier G-R relationships, we present a qualitative overview of the measurement concepts for obtaining  $\tau_g$  and  $\tau_r$  using an MOS-Capacitor. This preview lays the groundwork for comprehending a more detailed analysis of measurement techniques presented later on in Chapter 4 and 5. Finally, we review the analysis of the standard C-t transient technique, a review which serves as a basis for subsequent modifications.

## 2.1 Bulk And Surface G-R Relationships

### General Bulk Relationships

For an n-bulk silicon substrate the electron is the majority carrier whereas the hole is the minority carrier. The carrier concentrations in the substrate are given by

$$n = n_o + \delta n \quad (2.1a)$$

and

$$p = p_o + \delta p \quad (2.1b)$$

where  $n_o(p_o)$  is the equilibrium electron (hole) concentration [ $\text{cm}^{-3}$ ],  $\delta n(\delta p)$  is the excess or deficit electron (hole) carrier concentration [ $\text{cm}^{-3}$ ] relative to equilibrium, and  $n(p)$  is the total electron (hole) concentration [ $\text{cm}^{-3}$ ].

The four basic transitions of electrons and holes via single level G-R centers of energy  $E_T$  are illustrated in Fig. 2.1. Transition (a) and (b) represent the electron capture and emission from  $E_T$ , respectively. Similarly, transition (c) and (d) describe the capture and emission of holes from  $E_T$ . The generation-recombination of an electron-hole (e-h) pair can be depicted as a combination of these transitions. Transition (b) and (d) result in an e-h pair generation, whereas (a) and (c) produce an e-h pair recombination.

A detailed discussion of the SRH formalism is given in [64], and is summarized as follows. Intuitively, one can readily argue that the net change in electron concentration ( $dn/dt$ ) and hole concentration ( $dp/dt$ ) are respectively given by

$$\frac{dn}{dt} = e_n n_T - c_n p_T n \quad (2.2a)$$

and

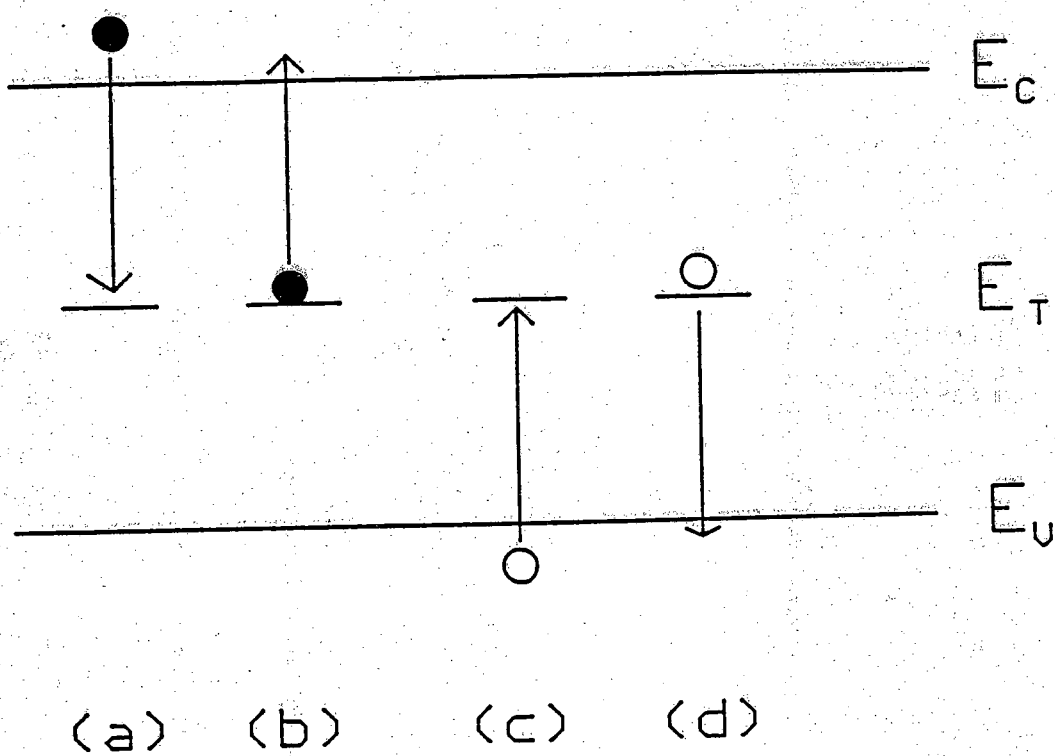


Fig. 2.1 Carrier generation-recombination via bulk G-R centers: (a) electron capture (b) electron emission (c) hole capture (d) hole emission.

$$\frac{dp}{dt} = e_p p_T - c_p n_T p \quad (2.2b)$$

where  $e_n$  ( $e_p$ ) is the electron (hole) emission coefficients,  $c_n$  ( $c_p$ ) is the electron (hole) capture coefficient,  $n_T$  is the number of filled G-R centers,  $p_T$  is the number of empty G-R centers.

Under steady-state conditions, we have

$$\frac{dn}{dt} = \frac{dp}{dt} = G = -R \quad (2.3)$$

or

$$G = -R = \frac{\frac{e_n e_p}{c_n c_p} - np}{\frac{1}{c_n N_T} (p + e_p/c_p) + \frac{1}{c_p N_T} (n + e_n/c_n)} \quad (2.4)$$

where  $G$  ( $R$ ) is designated as the net generation (recombination) rate under steady-state conditions.  $N_T$  is the total number of G-R centers ( $N_T = n_T + p_T$ ).

The capture and emission coefficients can be related to each other by considering the semiconductor under equilibrium conditions. In equilibrium, the principle of detailed balance states that each fundamental process and its reverse must self-balance, i.e.,  $dn/dt = dp/dt = 0$ . Setting Eqs. (2.2a) and (2.2b) to zero, and assuming that the capture and emission coefficients are the same in equilibrium and nonequilibrium, one obtains

$$e_n = c_n n_1 \quad (2.5a)$$

$$e_p = c_p p_1 \quad (2.5b)$$

where

$$n_1 = n_i e^{(E'_T - E_i)/kT} \quad (2.6a)$$

$$p_1 = n_i e^{(E_i - E'_T)/kT} \quad (2.6b)$$

and

$$E'_T \equiv E_T \pm kT \ln(g) \quad (2.7)$$

$E'_T$  is interpreted as the effective energy level of the G-R centers including the degeneracy factor  $g$  associated with the centers [64].  $T$  is the temperature in Kelvin and  $k$  is Boltzman's constant.

Substituting Eqs. (2.5a) and (2.5b) into Eq. (2.4) gives

$$G = -R = \frac{n_i^2 - np}{\tau_n(p+p_1) + \tau_p(n+n_1)} \quad (2.8)$$

where  $\tau_n = 1/N_T c_n$  and  $\tau_p = 1/N_T c_p$  are respectively the minority carrier lifetime of electrons and holes [sec].

By inspecting Eq. (2.8), one can readily confirm that carriers will be generated when  $n_i^2 > np$ . Recombination dominates if  $n_i^2 < np$ . In what follows we will establish expressions for  $\tau_g$  and  $\tau_r$  under carrier deficit and low-level carrier excess conditions, respectively.

### Generation Lifetime

Under steady-state carrier deficit conditions ( $n \ll n_1, p \ll p_1$ ), Eq. (2.8) simplifies to

$$G = \frac{n_i}{\tau_g} \quad (2.9)$$

where

$$\tau_g \equiv \tau_n(p_1/n_i) + \tau_p(n_1/n_i) \quad (2.10)$$

$\tau_g$  is interpreted as the generation lifetime [sec] which characterizes the carrier generation rate,  $G$ , under the cited steady-state conditions.

### Recombination Lifetime

Under low-level carrier excess conditions ( $\delta n, \delta p \ll n_o, n \simeq n_o$ ), the majority electron concentration remains essentially unchanged. In addition, we assume the dominant G-R centers have an energy level  $E_T$  located near midgap. Letting  $\delta n = \delta p$ , one can then simplify Eq. (2.8) to obtain [64]

$$R = \frac{\delta p}{\tau_p} \quad (2.11)$$

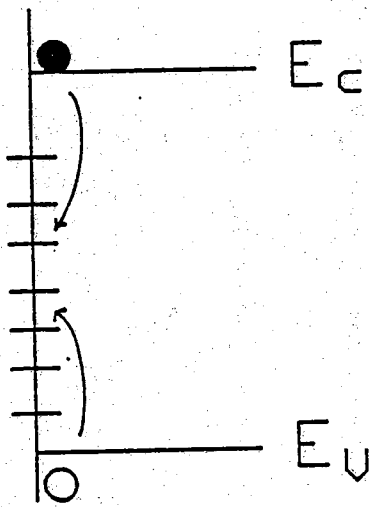
Clearly, the minority carrier hole lifetime,  $\tau_p$ , specifies the recombination rate  $R$ , and is equal to the recombination lifetime  $\tau_r$  under low-level carrier excess conditions.

### General Surface Relationships

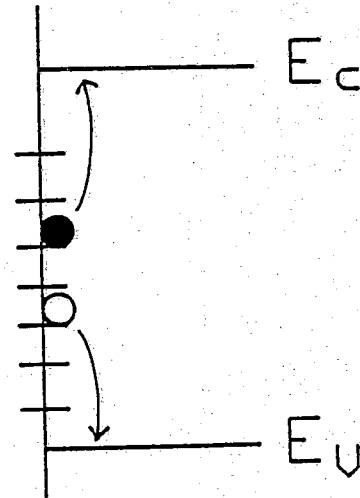
Having established expressions for  $\tau_g$  and  $\tau_r$ , one can follow a similar approach in analyzing the surface G-R via interfacial traps (also referred to as surface states). The major differences in the surface and bulk analyses are that the interfacial traps are typically distributed throughout the bandgap, as illustrated in Fig. 2.2, and the change in carrier concentration is expressed as per unit area instead of per unit volume.

If we first assume that the bandgap at the interface contains surface states of a single energy level  $E_{IT}$ , then by analogy with the bulk analysis





(a) electron and hole capture



(b) electron and hole emission

Fig. 2.2 (a) Carrier capture and (b) emission via interfacial traps.

$$G_s = -R_s = \frac{n_i^2 - n_s p_s}{\frac{1}{c_{ps} N_{Ts}} (n_s + n_{1s}) + \frac{1}{c_{ns} N_{Ts}} (p_s + p_{1s})} \quad (2.12)$$

The quantities in Eq. (2.12) are the same as those employed in the bulk analysis except the added subscript "s" denotes surface values.

In order to include the effect of multi-levels on the net rate of change in carrier concentrations, we introduce  $D_{IT}(E)$  as the density of interfacial traps as a function of energy within the bandgap at the interface. Replacing  $N_{Ts}$  in Eq. (2.12) by  $D_{IT}(E)dE$  and integrating over the bandgap yields

$$G_s = -R_s = \int_{E_V}^{E_C} \frac{(n_i^2 - n_s p_s) D_{IT}(E)}{(n_s + n_{1s})/c_{ps} + (p_s + p_{1s})/c_{ns}} dE \quad (2.13)$$

### Surface Generation Velocity

When the surface is depleted of carriers ( $n_s \rightarrow 0$ ,  $p_s \rightarrow 0$ ), Eq. (2.13) simplifies to

$$G_s = s_g n_i \quad (2.14)$$

where

$$s_g = \int_{E_V}^{E_C} \frac{c_{ns} c_{ps} D_{IT}(E)}{c_{ns} e^{(E-E_i)/kT} + c_{ps} e^{(E_i-E)/kT}} dE \quad (2.15)$$

$s_g$  is interpreted as the depleted surface generation velocity [cm/sec]. Using the experimental information that the capture coefficients and the surface state density in the Si/SiO<sub>2</sub> system are approximately constant near midgap [65-67], one can further simplify Eq. (2.15) to obtain

$$s_g = \frac{\pi}{2} \left( c_{ns} c_{ps} \right)^{1/2} D_{IT} kT \quad (2.16)$$

where it is understood that  $c_{ns}$ ,  $c_{ps}$ , and  $D_{IT}$  are to be evaluated at midgap.

### Surface Recombination Velocity

Under low-level carrier excess conditions ( $\delta n_s = \delta p_s \ll n_{so}$ ), we can simplify Eq. (2.13) to read

$$R_s = s_r \delta p_s \quad (2.17)$$

where

$$s_r = \int_{E_V}^{E_C} \frac{c_{ps} D_{IT}(E)}{1 + \frac{n_{1s}}{n_{so}} + \frac{c_{ps} p_{1s}}{c_{ns} n_{so}}} dE \quad (2.18)$$

$s_r$  defined by Eq. (2.18) is the surface recombination velocity [cm/sec] under low-level carrier excess conditions.  $n_{so}$  is the surface electron concentration under equilibrium conditions.

Comparing Eq. (2.15) with Eq. (2.18), one concludes that the evaluation of  $s_r$  is more complicated than  $s_g$  since  $n_{so}$  depends on the degree of energy band-bending at the surface.

## 2.2 MOS Lifetime Measurement Concepts

Assuming an n-bulk device, we herein introduce the basic MOS measurement concepts involved in determining  $\tau_g$  and  $\tau_r$  under carrier deficit and low-level carrier excess conditions. Fig. 2.3 depicts a typical high frequency C-V characteristic of an MOS-C maintained under equilibrium conditions. The C-V curve includes three basic segments: accumulation, depletion and inversion.  $C_0$  is the oxide capacitance observed under

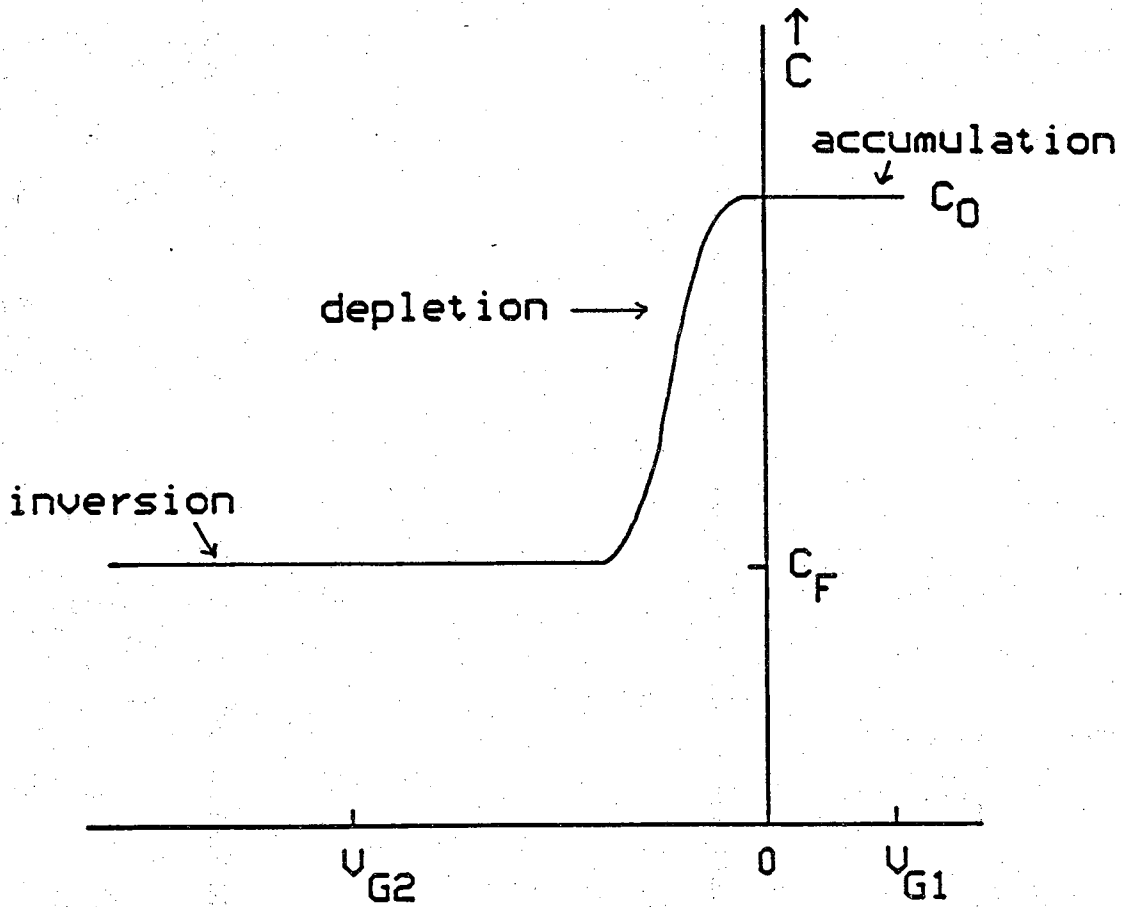


Fig. 2.3 Typical C-V characteristics of an n-bulk MOS-C under equilibrium conditions.

accumulation conditions and  $C_F$  is the equilibrium inversion capacitance. Corresponding to the inversion situation there exists an inversion layer and an equilibrium depletion region,  $W_F$ , as depicted in Fig. 2.4. The inversion layer and the depletion region consist of positive hole charges and positive ionized impurity donors, respectively. Given an ideal device, the combined positive charges within the semiconductor balance the negative charges on the metal gate.

### 2.2.1 "Reverse-Bias" Measurements

If the gate voltage of the MOS-C (originally set at  $V_{G1}$  in Fig. 2.3) is momentarily pulsed or swept rapidly to  $V_{G2}$ , no inversion layer can be formed due to a lack of minority carrier holes inside the semiconductor. Instead, the depletion region  $W$  expands to a larger value ( $W > W_F$ ) so that the charge placed on the metal gate is balanced solely by the resultant exposed ionized donors. The MOS-C is said to be deeply-depleted. Recall that if a PN junction diode is reverse-biased, its depletion width also increases. Thus, by analogy, one can state that pulsing or sweeping the MOS-C into deep-depletion is equivalent to "reverse-biasing" the structure. The consequence of reverse-biasing is that there exists a carrier deficit condition inside the deep-depletion region. Consequently, carrier generation takes place. This is pictured in Fig. 2.5. The generation current  $I_{GEN}$  is related to  $\tau_g$  and the effective generation width  $W_G$  by

$$I_{GEN} \propto \frac{W_G}{\tau_g} \quad (2.19)$$

As generation continues, the generated holes are swept to the interface and an inversion layer is gradually formed. Correspondingly, the depletion region decreases. Hence by monitoring  $I_{GEN}$  or  $W_G$ ,  $\tau_g$  can readily be deduced. As will be detailed in Section 2.3, one typically monitors the capacitance;  $W_G$  is a capacitance-related quantity.

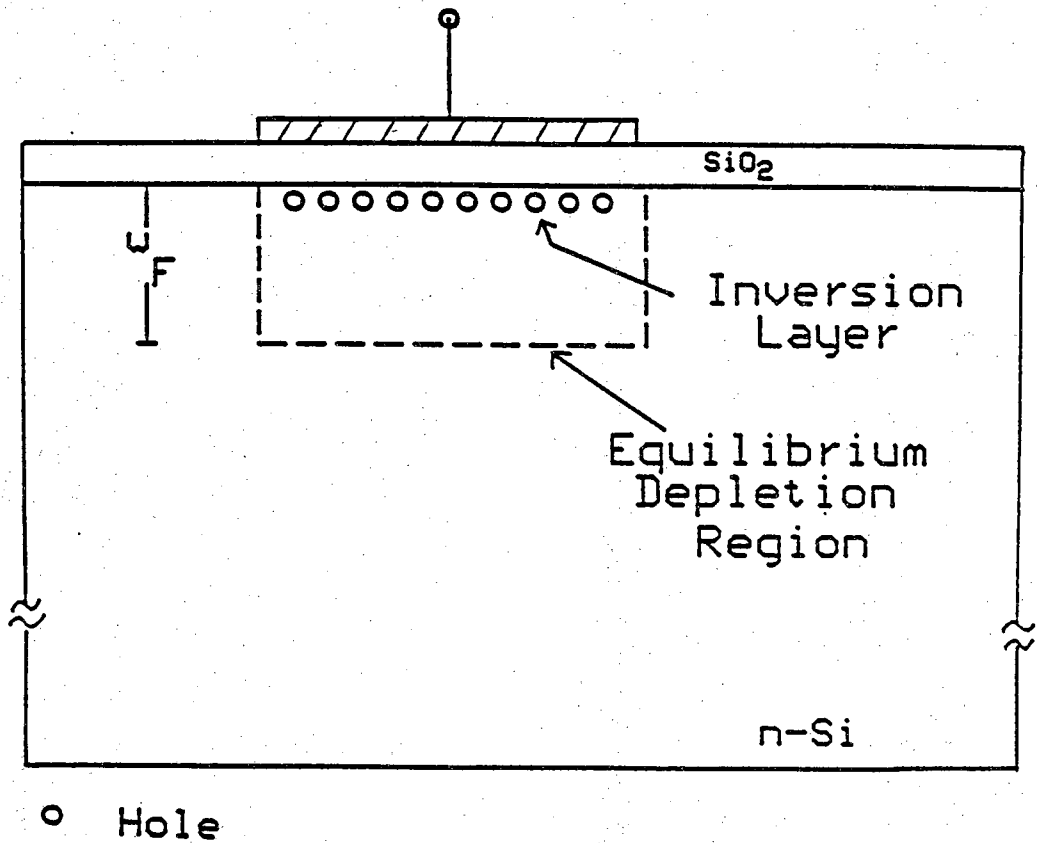


Fig. 2.4 Cross-sectional view of an equilibrium n-bulk MOS-C illustrating the inversion layer and the depletion region. The MOS-C is biased under inversion conditions.

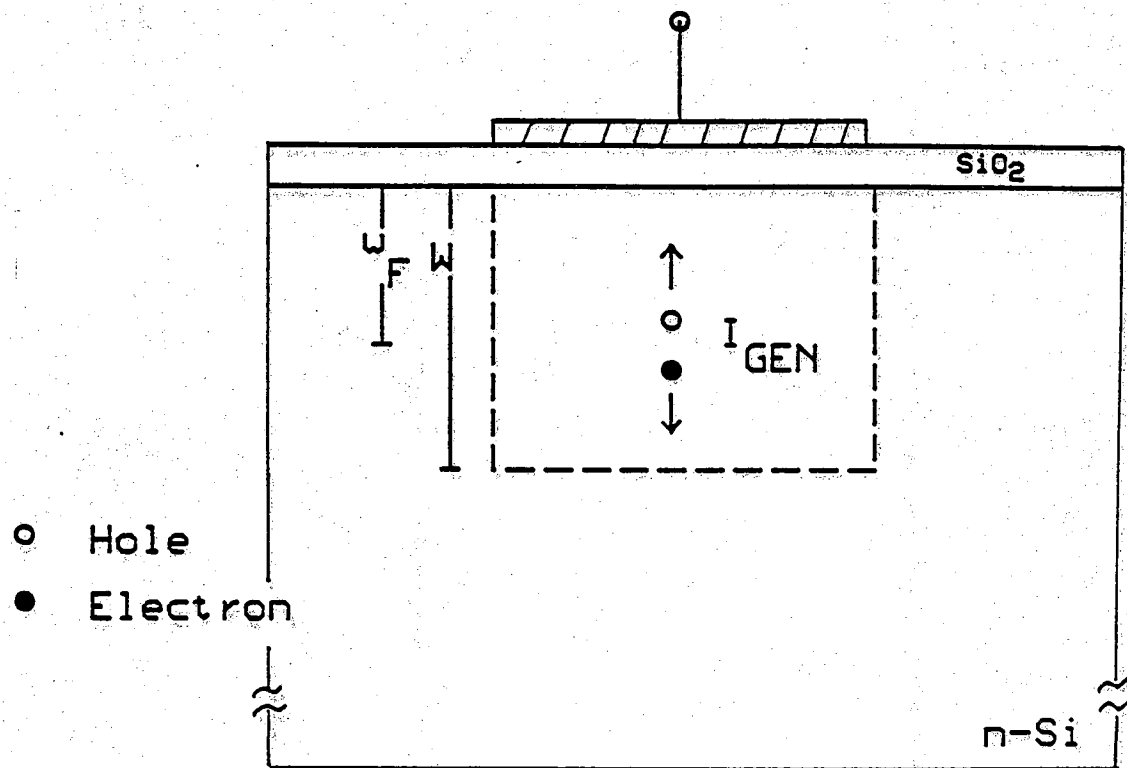


Fig. 2.5 Major bulk carrier generation component inside a "reverse-biased" MOS-C.

### 2.2.2 "Forward-Bias" Measurements

If carrier deficit conditions are created by reverse-biasing an MOS-C, then it is reasonable that carrier excess conditions can be initiated by simply "forward-biasing" an MOS-C. The action of forward-biasing can be induced, for example, by sweeping the gate voltage from inversion toward less inversion. As depicted in Fig. 2.6, holes are injected into the quasi-neutral bulk and depletion regions where they recombine with the majority electron carriers. Paralleling the analysis of a forward-biased PN junction diode, recombination arising from the quasi-neutral region, commonly referred to as the diffusion current  $I_{\text{DIFF}}$ , should dominate at large forward-biases. The diffusion current is related to  $\tau_p$  by

$$I_{\text{DIFF}} \propto \frac{1}{\sqrt{\tau_p}} (e^{qV_e/kT} - 1) \quad (2.20)$$

where  $V_e$  is the effective forward-bias voltage inside the MOS-C. Recall that the minority carrier hole lifetime is equivalent to the recombination lifetime ( $\tau_r = \tau_p$ ) under low-level carrier excess conditions. As will be shown in Chapter 5,  $I_{\text{DIFF}}$  and  $V_e$  can be related to the voltage sweep and capacitance, respectively; thus  $\tau_r$  can be deduced from "forward-bias" MOS-C measurements.

### 2.3 Standard MOS-C C-t Transient Analysis

As detailed in Chapter 4, modifications of the standard C-t technique are introduced for extracting  $\tau_g$  and  $s_g$ . The techniques build on the standard MOS-C C-t transient measurement. Understandably, when a given technique is being modified, the mathematical expressions which describe the original technique are accordingly altered. It is therefore logical to present a condensed formalism of the standard C-t transient analysis.

The standard C-t measurement is basically performed by pulsing an MOS-C into deep-depletion, and recording its subsequent C-t transient response. Fig. 2.7 depicts a typical C-t transient characteristic; assuming that the MOS-C is initially biased into accumulation. The deep-depletion capacitance  $C$  and the inversion hole charges  $Q_p$  are related by [68]



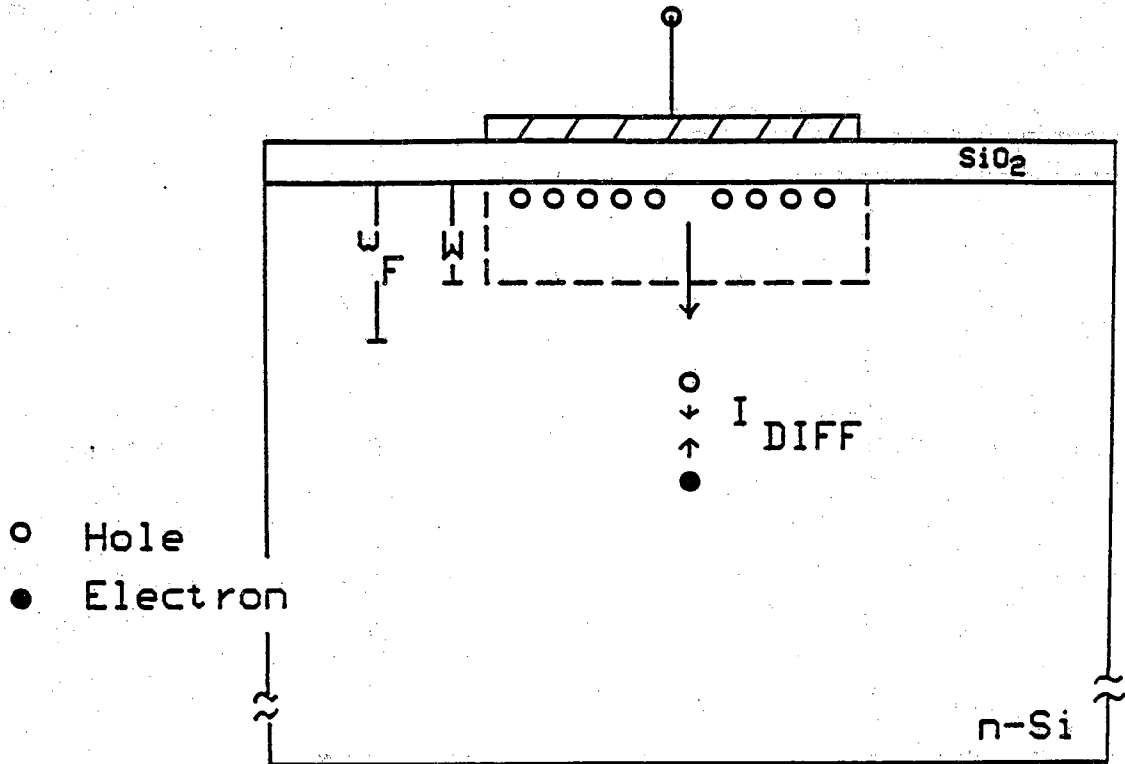


Fig. 2.6 Major carrier recombination component inside a "forward-biased" MOS-C.

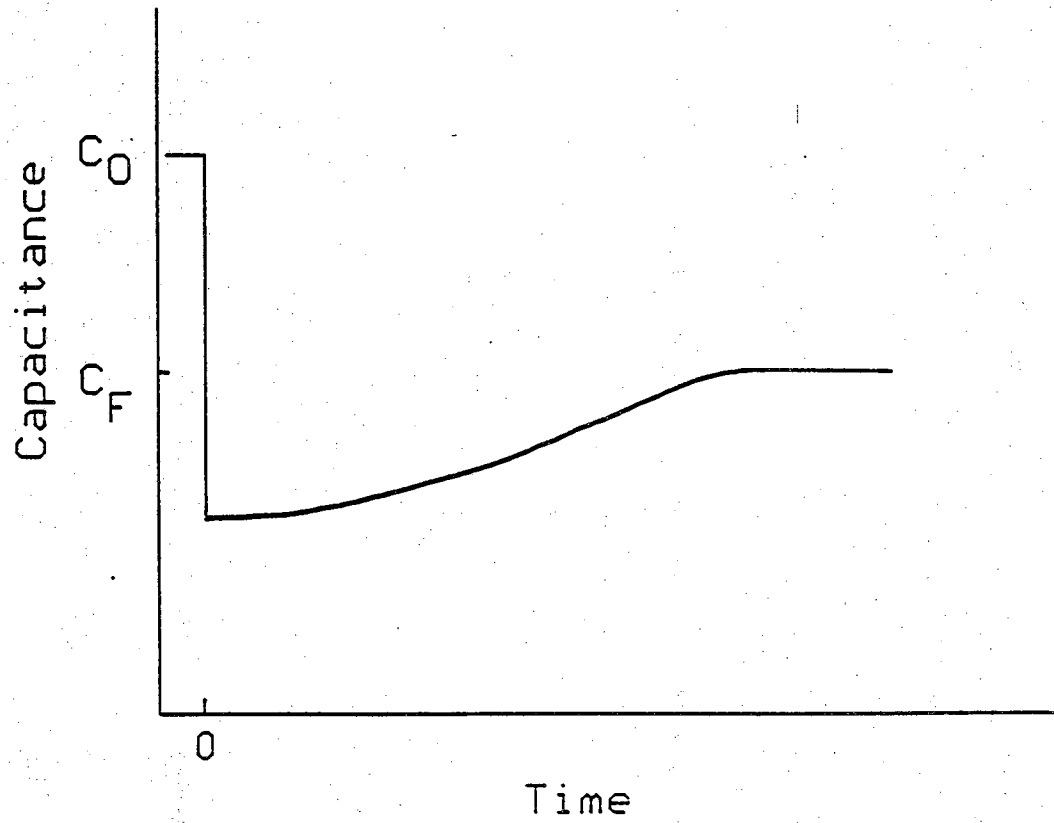


Fig. 2.7 Typical pulsed C-t transient characteristics of an MOS-C.

$$\left(\frac{C_O}{C}\right)^2 = 1 + \frac{V_G - V_{FB}}{V_o} + \frac{Q_p}{C_o V_o} \quad (2.21)$$

where  $C_o$  is the oxide capacitance per unit area ( $C_o = C_O/A_G$ ),  $V_{FB}$  is the flat band voltage,  $V_G$  is the applied inverting voltage, and  $V_o$  is a defined constant given by

$$V_o \equiv \frac{qK_S x_o^2 N_D}{2K_O^2 \epsilon_o} \quad (2.22)$$

$K_O$  is the dielectric constant of silicon dioxide,  $K_S$  is the dielectric constant of silicon,  $x_o$  is the oxide thickness and  $N_D$  is the net doping concentration.

Taking  $-d/dt$  of both sides of Eq. (2.21), and since  $dV_G/dt = 0$  after  $t=0^+$  ( $V_G$  is a constant right after the the step voltage is applied), one obtains

$$\frac{-d}{dt} \left(\frac{C_O}{C}\right)^2 = -\frac{1}{C_o V_o} \frac{dQ_p}{dt} \quad (2.23)$$

Fig. 2.8 identifies different carrier generation components within the deeply-depleted MOS-C. Component 1 is the bulk generation inside the depletion region, and is characterized by  $\tau_g$ . Component 2 is the lateral surface generation around the gate periphery, and is characterized by  $s_g$ . Both components 1 and 2 are  $W$ -dependent quantities. Components 3 and 4 are respectively the gated surface generation and quasi-neutral bulk generation. These latter components are  $W$ -independent quantities, are typically negligible at room temperature conditions, and are usually combined and characterized by  $s_{eff}$  — an effective surface generation velocity. The minority hole carrier generation rate,  $dQ_p/dt$ , is related to the cited generation components by [33,34,68]

$$\frac{dQ_p}{dt} = q \frac{n_i}{\tau_g} W_G + q n_i s_g \frac{P}{A_G} W_G + q n_i s_{eff} \quad (2.24)$$

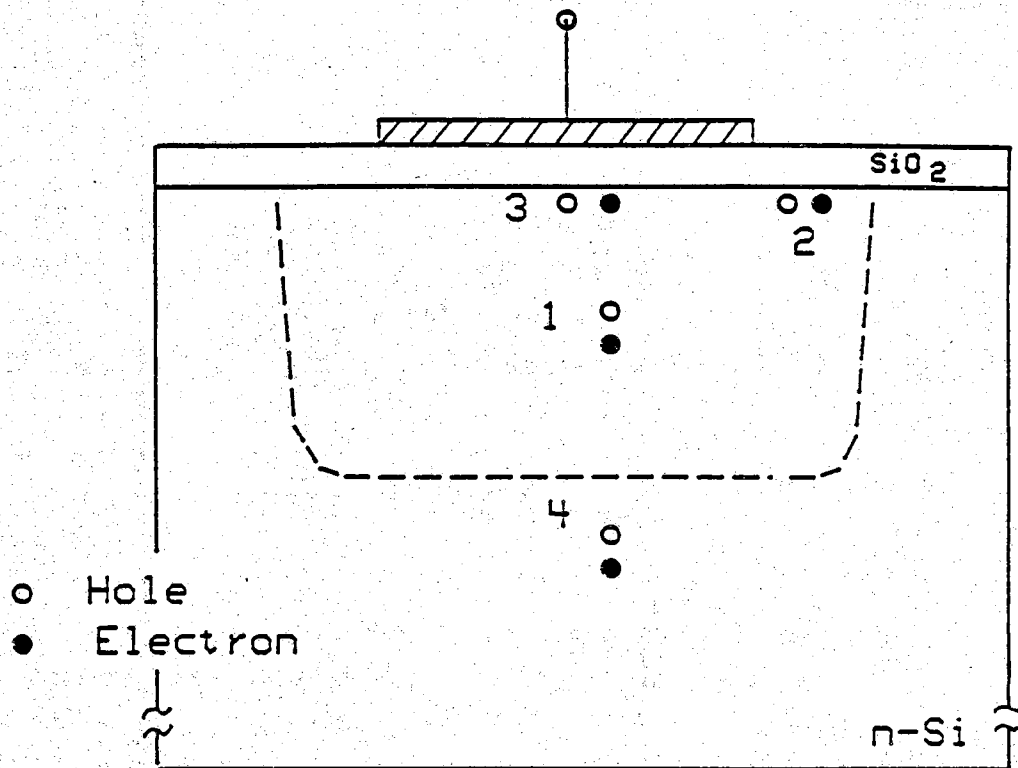


Fig. 2.8 Different carrier generation components inside a deeply-depleted MOS-C. Component 1 is the bulk generation inside the depletion region, component 2 is the lateral depleted surface generation, component 3 is the gated surface generation and component 4 is the quasi-neutral bulk generation.

The first two terms on the right hand side of Eq. (2.24) are the generation contributed by components 1 and 2, respectively; the last term represents the combined contribution by components 3 and 4.  $P/A_G$  is the perimeter to gate area ratio and  $W_G$  is the effective bulk generation width.

Substituting Eq. (2.23) into Eq. (2.24) and reorganizing the result, one obtains

$$-\frac{d}{dt} \left( \frac{C_O}{C} \right)^2 = 2 \frac{K_O}{K_S} \frac{1}{x_o N_D} \left( \frac{n_i}{\tau_g'} W_G + n_i s_{\text{eff}} \right) \quad (2.25)$$

where

$$\tau_g' \equiv \frac{\tau_g}{1 + \tau_g s_g P/A_G} \quad (2.26)$$

$\tau_g'$  is known as the effective generation lifetime.

The effective generation width,  $W_G$ , is usually approximated by  $W - W_F$  (as first suggested by Zerbst [30]). Moreover,  $W$  is related to  $C$  by [68]

$$W = \frac{K_O}{K_S} x_o \left( \frac{C_O}{C} - 1 \right) \quad (2.27a)$$

and

$$W_F = \frac{K_O}{K_S} x_o \left( \frac{C_O}{C_F} - 1 \right) \quad (2.27b)$$

Thus setting  $W_G = W - W_F$  and substituting Eqs. (2.27a) and (2.27b) into Eq. (2.25) yields

$$-\frac{d}{dt} \left( \frac{C_O}{C} \right)^2 = 2 \frac{n_i}{N_D} \frac{C_O}{C_F} \frac{1}{\tau_g'} \left( \frac{C_F}{C} - 1 \right) + 2 \frac{n_i K_O}{K_S x_o N_D} s_{\text{eff}} \quad (2.28)$$

Clearly, if one appropriately manipulates the C-t data and plots  $-d(C_O/C)^2/dt$  versus  $C_F/C - 1$ , one can readily extract the lifetime from the slope of the plot. This widely-employed plot is commonly referred to as the Zerbst plot.

Finally, it should be emphasized that the lifetime parameter extracted from the Zerbst plot is typically an *effective* generation lifetime ( $\tau_g'$ ). The true generation lifetime  $\tau_g$  is obtained only when  $\tau_g s_g P/A_G \ll 1$  (see Eq. (2.26)). As a result, well-annealed MOS-C's with large dimensions (making  $s_g$  and  $P/A_G$  small, respectively) should be used for measurements in order to extract the true  $\tau_g$ .

## 2.4 Summary

In this chapter, the SRH theory of generation-recombination has been briefly reviewed. Expressions for the generation lifetime, the surface generation velocity, the recombination lifetime, the surface recombination velocity, and their relationships to the G-R rates have been established. Also included in this chapter are the basic MOS-C measurement concepts for determining  $\tau_g$  and  $\tau_r$ . We likewise reviewed the standard C-t transient analysis, thereby forming a base for future modifications. Finally, it should be mentioned again that the research work focuses on the experimental determination of generation lifetime and surface generation velocity under carrier deficit conditions, and recombination lifetime under low-level carrier excess conditions.

### CHAPTER 3

## TEST STRUCTURE FABRICATION AND MEASUREMENT SET-UPS

The MOS-based test structures employed for G-R parameter measurements consisted of MOS-Capacitors (MOS-C) and Schottky-Drained Gate Controlled Diodes (SGCD). In this chapter the general processing techniques for producing the test structures are first reviewed. These include wafer clean-up, oxidation, phosphorus gettering, metallization, post-metallization anneal, pattern definition, sawing and bonding. It should be mentioned that, although the techniques employed in this work are common processing routines, appropriate modifications had been made over the course of the research work in an effort to fabricate test structure with a long generation lifetime. The fabrication procedures, processing history and pertinent physical characteristics of the test structures are summarized following the general overview of processing techniques. The presentation includes information on an infra-red (IR) multibounce test structure which was developed for free carrier infra-red absorption measurements. Finally, three basic measurement set-ups, which were utilized for obtaining the capacitance-voltage (C-V) characteristics, the capacitance-time (C-t) characteristics, and the voltage sweep-capacitance characteristics, are described.

### 3.1 General Processing Techniques

All test structures were fabricated on n-type silicon substrates using the following processing techniques.

*Initial wafer clean-up:* All wafers were cleaned with either cleaning procedure #1 or #2, as listed in Appendix A.1, to remove organic and inorganic contaminants which might possibly adhere to the wafer surfaces. Improper cleaning will inevitably lead to a disastrous leaky oxide that is

grown on the substrates during subsequent oxidation. As a rule of thumb to ensure proper cleaning, the wafers should be completely pulled dry from the DI (deionized) water in the last step of the cleaning procedures.

*Oxidation:* Following the initial clean-up step, the wafers were immediately subjected to oxidation to avoid further contamination. Oxidation was performed in a Tempress 4" furnace tube maintained at 1100 °C. The wafers were first loaded and pushed to the center of the tube in flowing N<sub>2</sub>, and were allowed to temperature stabilize for 5 minutes. The N<sub>2</sub> gas flow was terminated, and the O<sub>2</sub> source gas was admitted. The wafers were then dry oxidized at 1100 °C for various periods of time to achieve an oxide thickness of either 0.1 or 0.2 μm. Following the oxide growth, an in situ 10 minute N<sub>2</sub> anneal was performed at the same temperature so as to reduce the number of fixed oxide charges (Q<sub>f</sub>) associated with the oxidation [69]. Upon completion, there should be no observable spotted oxide on the wafer surfaces if they were properly cleaned prior to oxidation. Procedural details of the oxidation step is given in Appendix A.2.

*Phosphorus Gettering:* All gettering steps were performed at 850 °C using a Tempress 4" furnace tube. After the wafers were loaded and pushed to the center of the tube in N<sub>2</sub>, they were allowed to warm up for 3 minutes with both N<sub>2</sub> and O<sub>2</sub> gases flowing. The phosphorus oxychloride (POCl<sub>3</sub>) source gas was admitted for a total of either 4 or 20 minutes during which the actual phosphorus deposition, and gettering action, took place. The phosphorus entering the backside or the unpolished side of the wafers (with the back oxide removed in advance) formed an n<sup>+</sup>/n region for ohmic contact, and also gettered metallic impurities from the bulk substrates [70] — thus increasing the generation lifetime. In addition, phosphorus deposited on the frontside of the wafers diffused into the silicon dioxide to form a layer of phosphosilicate glass (PSG) which, in turn, gettered the sodium ions (Na<sup>+</sup>) from the remaining oxide layer — thus stabilizing the SiO<sub>2</sub> [71,72]. Since the test structures were not to be subjected to bias-temperature tests, the polarization problem associated with the PSG was of no concern [73]. Consequently, the PSG in the gate oxide was left in place for all wafers. Details of the gettering procedures are outlined in Appendix A.2.

*Metallization:* Aluminum was used exclusively for metallization. All wafers described herein, except one, were metallized using the Perkin-Elmer 2400 sputtering system. The system consists of mainly an aluminum target (together with some other material targets) and a movable substrate platform,



all enclosed in an vacuum chamber. The detailed procedural aspects of the sputtering system are given in Appendix A.3, and are summarized as follows: After the vacuum chamber of the system was unsealed, the wafers were placed onto the center of the platform. The chamber was then resealed and was pumped down into the low  $10^{-7}$  torr range. The time for pumping down the system typically lasted for at least 4 to 5 hours. Following the pump down period, argon (Ar) source gas was admitted until a steady pressure of about 6-7 mtorr was attained. The substrate platform was then rotated away from the aluminum target, and the surface of the target was pre-cleaned using a procedure known as pre-sputtering. This involved bombarding the target with Ar ions originating from an excited plasma. The input power to the plasma was 300 watts, and the pre-sputtering time was 10 minutes. Following pre-sputtering, the power was reduced to 100 watts and the wafers were then exposed to the plasma for 30 minutes during which aluminum was sputtered onto the substrates. Typical thickness of the aluminum layer was on the order of 3000 Å.

As indicated previously, the metal on one wafer (wafer J24) was deposited using a second system, the NRC-3114 vacuum system. In this system, aluminum is evaporated from a resistance heated, low-alkali tungsten filament after the system attains a base pressure in the low to mid  $10^{-7}$  torr range.

A final note: the sputtering scheme is a much cleaner deposition process than the evaporation method. For this reason it was chosen as the major metallization procedure for wafer processing. Although an increased amount of interfacial traps were created due to the radiation associated with sputtering, the interfacial traps were usually annealed out by a subsequent procedure known as post-metallization annealing, which will be described next.

*Post-Metallization Anneal (PMA):* PMA was performed for metallized wafers using a Tempress 4" furnace tube. All wafers were annealed in  $N_2$  at 450 °C for 30 minutes. With regard to the MOS-C, the PMA can effectively reduce interfacial traps located at the Si-SiO<sub>2</sub> interface [74-76]. For the SGCD test structure, it also ensured the formation of a good Schottky contact between the aluminum and the n-type substrate [77].

*Pattern Definition:* Patterns were defined using photolithographic techniques. Specifically, AZ-1350J positive photoresist and KTI 747 negative photoresist were respectively utilized for the MOS-C and SGCD test structures. The procedures of applying the positive photoresist (henceforth

simply referred to as resist) included, first of all, spinning a layer of resist on the frontside of the wafers at 4400 rpm for 40 seconds. A 10 minute, 90 °C soft-bake was then performed so as to harden the resist. The wafers were next transferred to the Kasper 2" mask aligner and were exposed to UV illumination for 1.5 minutes, followed by developing in AZ Developer for 60 seconds. After a subsequent 60 second rinse in DI water, the wafers were blown dry in N<sub>2</sub> and again hard-baked at 110 °C for 10 minutes prior to aluminum etching.

Using positive resist as a protective mask, the actual MOS-C gate patterns (i.e., the aluminum patterns) were defined through the use of an aluminum etch solution. The solution consisted of 760 : 30 : 15 : 50, H<sub>3</sub>PO<sub>4</sub> : HNO<sub>3</sub> : CH<sub>3</sub>COOH : H<sub>2</sub>O. Excess aluminum etching solution was removed by rinsing in DI water, and the resist was removed with acetone.

The application of negative resist was similar to that of positive resist. The negative resist was spun on the wafers at 300 rpm for 40 seconds, followed by a 10 minute, 85 °C soft-bake. However, the UV exposure time was merely 30 seconds. The wafers were then developed in KTI Developer II solution for 90 seconds, and rinsed in KTI Rinse I solution for another 30 seconds. The wafers were then hard-baked at 110 °C for 10 minutes. Schottky contacts of the SGCD were defined using the buffered HF SiO<sub>2</sub> etch whereas aluminum patterns were defined using the aluminum etch previously described. It should be noted that negative resist requires more attention to detail than the positive resist. A careless prolonged baking, or a change in baking temperature, for example, may later result in an incomplete removal of the resist.

*Sawing and Bonding:* Upon the completion of fabrication, all test structures were separated by sawing the wafers with the Tempress dicing saw 602 system. All wafers were first coated with a layer of positive resist (spin but no baking) prior to sawing, which protected the test structures from flying debris during the sawing process. With regard to the actual sawing, the wafers were sawed in such a way that the depth of the sawing was about half the wafer thickness. After removing the resist, the wafers were rinsed in DI water, blown dry in N<sub>2</sub>, and then carefully broken into individual devices. Depending on structural sizes, each test structure was then either mounted on a TO-5, TO-6, or TO-8 header with silver epoxy heated at 110 °C for at least 1 hour and 15 minutes. Finally, contact wires made of aluminum were ultrasonically bonded from the test structure to the header posts.

### 3.2 Test Structure Summary

MOS-based test structures were fabricated on wafers which included 4" 3-5 ohm-cm (100)-oriented, 2" 2-3 ohm-cm (100)-oriented, and 2" 3-5 ohm-cm (111)-oriented, one-sided polished n-type silicon substrates. The thickness of the 4" and 2" wafers were about 550 and 255  $\mu\text{m}$ , respectively. The 4" wafers were high quality float zone solar cell substrates and they were scribed into quadrants prior to processing. The 2" Czochralski-pulled wafers were used for comparison purposes and were processed as a whole substrate. The wafers used in fabricating the IR multibounce structures were 3", 200 ohm-cm, (100)-oriented, two-sided polished n-type silicon substrates with a thickness of 350  $\mu\text{m}$  and a primary flat in the  $\langle 110 \rangle$  direction. Relevant processing history and pertinent characteristics of all wafers are summarized in Table 3.1.

#### 3.2.1 MOS-Capacitor (MOS-C)

The configuration of the MOS-C is shown in Fig. 3.1. Different pattern sizes of the ring-dot structures were used for generation-recombination measurements. In all measurements, the ring was connected to the electrical ground to suppress lateral surface effects while the dot was subjected to various biases.

In fabricating the MOS-C, the wafers were first cleaned and oxidized using the procedures described in Subsection 3.1 and Appendix A. The backside oxide was then removed with buffered HF and the wafers were recleaned using cleaning procedure #3, as outlined in Appendix A.1. The wafers were then subjected to the gettering step which was previously described and detailed in Appendix A.2. Next aluminum was deposited on both sides of the wafers, followed by a PMA. After the PMA, the metallized wafers were pre-baked at 110 °C for 10 minutes. A layer of positive resist was spun on the backside of the wafer, followed by a hard-bake at 110 °C for 10 minutes. This extra photoresist step was utilized for protecting the backside metallization from the subsequent aluminum etch. One then defined the MOS-C gates using the aforementioned positive photolithographic process. Finally, both the frontside and backside resists were removed with acetone. After several rinses in DI water and blow drying in  $\text{N}_2$ , the wafers were sawed, mounted and tested.

**Table 3.1 Summary Of Wafer Characteristics And Relevant Processing History.**

Wafer Number	Size(")	Wafer Specs		Test Structure	Oxide Thickness( $\mu\text{m}$ )	Gate Area ( $\text{cm}^2$ )	Drain <sup>†</sup> Area ( $\times 10^{-3} \text{cm}^2$ )
		Orient-ation	Nom. Doping ( $\times 10^{15} \text{cm}^{-3}$ )				
D5	4"	100	2	MOS-C	0.2	$2.970 \times 10^{-3}$	-
J24	4"	100	2	SGCD	0.1	$2.500 \times 10^{-3}$	2.50
O5	2"	100	2	SGCD	0.2	$2.500 \times 10^{-3}$	1.25 or 2.50
M14	4"	100	2	MOS-C	0.2	$3.675 \times 10^{-2}$	-
D2	4"	100	2	MOS-C	0.2	$3.675 \times 10^{-2}$	-
D514	2"	111	1	MOS-C	0.2	$3.675 \times 10^{-2}$	-
IR1	3"	100	0.1	IR	0.1	*	-

Wafer Number	Relevant Processing History		
	Cleaning Procedure #	Gettering Time (min)	Metallization Method
D5	1	20	sputter
J24	1	4	evaporate
O5	1	20	sputter
M14	1	20	sputter
D2	2	4	sputter
D514	1	20	sputter
IR1	1,2	-	sputter

<sup>†</sup> Drain area is defined as one-half of the Schottky-related MOS-C area.

\* Refer to subsection 3.2.3.

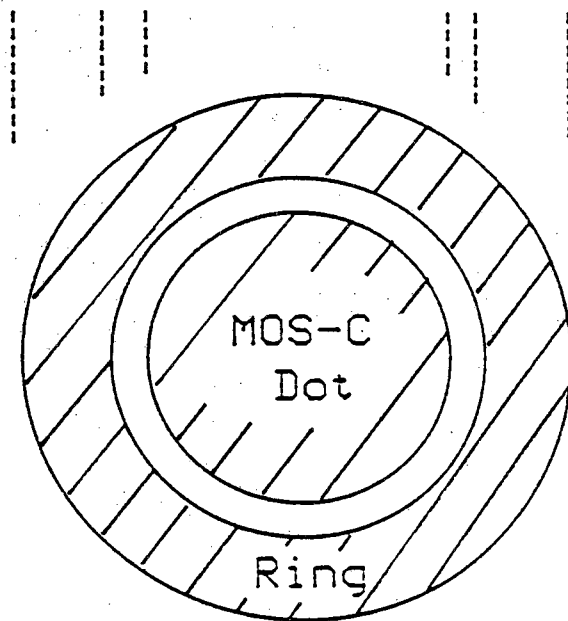
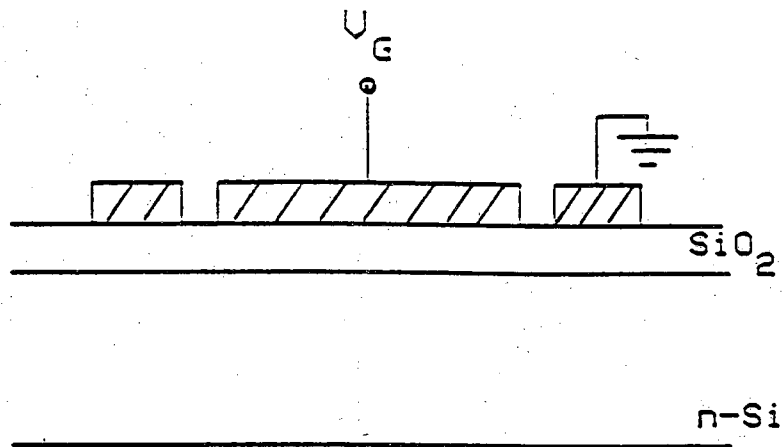


Fig. 3.1 (a) Cross-sectional view and (b) top view of a ring-dot MOS-C.

### 3.2.2 Schottky-Drained Gate-Controlled Diode (SGCD)

The general configuration of the SGCD test structure is pictured in Fig. 3.2. The structure actually consisted of a standard MOS-C located next to a Schottky diode which had an extended MOS-region. The separation between the diode and the MOS-C was 10  $\mu\text{m}$ . Its operational principle will be detailed in Chapter 4.

The fabrication of SGCD test structures were exactly the same as that of MOS-C's up to and including the gettering step. After gettering, however, the Schottky contact openings were defined using the negative photoresist procedures listed in Appendix A.4. As part of this step the wafers must be inspected with a microscope to ensure that the  $\text{SiO}_2$  windows were properly etched down to the Si substrates. With the negative resist removed by nophenol, aluminum was deposited on both surfaces of the wafers and the wafers were annealed using PMA procedures. After defining the SGCD negative resist patterns on the frontside, an additional layer of resist was spun on the backside of the wafers prior to the hard-bake. The hard-bake was then carried out at 110 °C for 10 minutes. With the backside properly protected, the SGCD aluminum patterns were next defined using the aluminum etch. The negative resist was subsequently removed with nophenol, and the test structures were separated by sawing.

### 3.2.3 Infra-red Multibounce Test Structure

The cross-sectional view of an IR multibounce structure, together with an IR probe beam and an excitation beam, is depicted in Fig. 3.3 (a). The top view of a complete test structure pattern is illustrated in Fig. 3.3 (b). The most distinguishing feature of the test structure is the paired V-groove openings (windows) which facilitate the introduction and extraction of infra-red probe light into and from the substrate. Free carrier concentrations in the substrate are modulated either by the gate voltage or the excitation light incident on the back of the wafer. The rectangular V-groove windows are patterned perpendicular (or parallel) to the  $\langle 110 \rangle$  flat of the substrate. Separation between the windows varies from 0.5 to 5.0 cm. The six-paired rectangular MOS-Cs have a large area of 0.5x0.135, 1.0x0.135, 1.5x0.135, 2.0x0.135, 4.0x0.135 and 5.0x0.135  $\text{cm}^2$ . A large metallization area is provided for electrical grounding purposes. 2x2  $\text{mm}^2$  MOS-Cs were also fabricated on the same substrate for supplemental measurements.

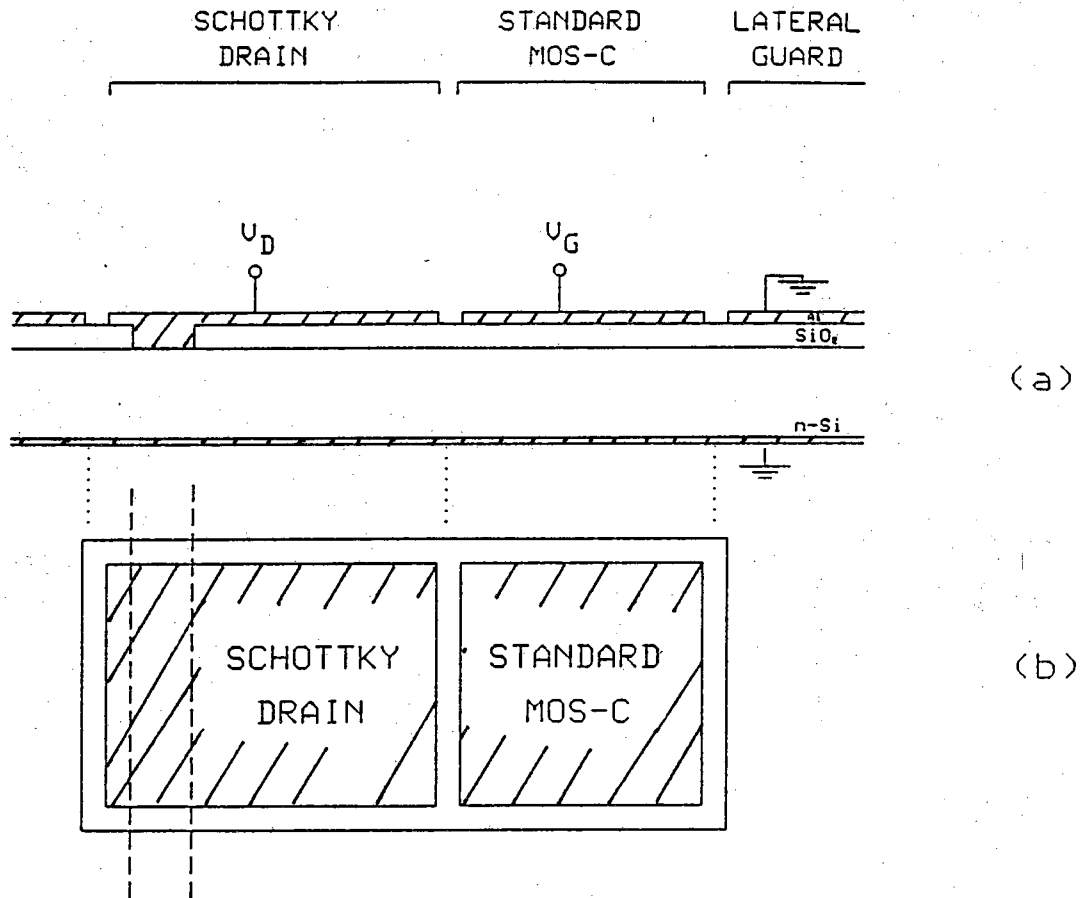


Fig. 3.2 (a) Cross-sectional view and (b) top view of a SGCD structure. The interspacing between the diode and the standard MOS-C is  $10 \mu\text{m}$ .

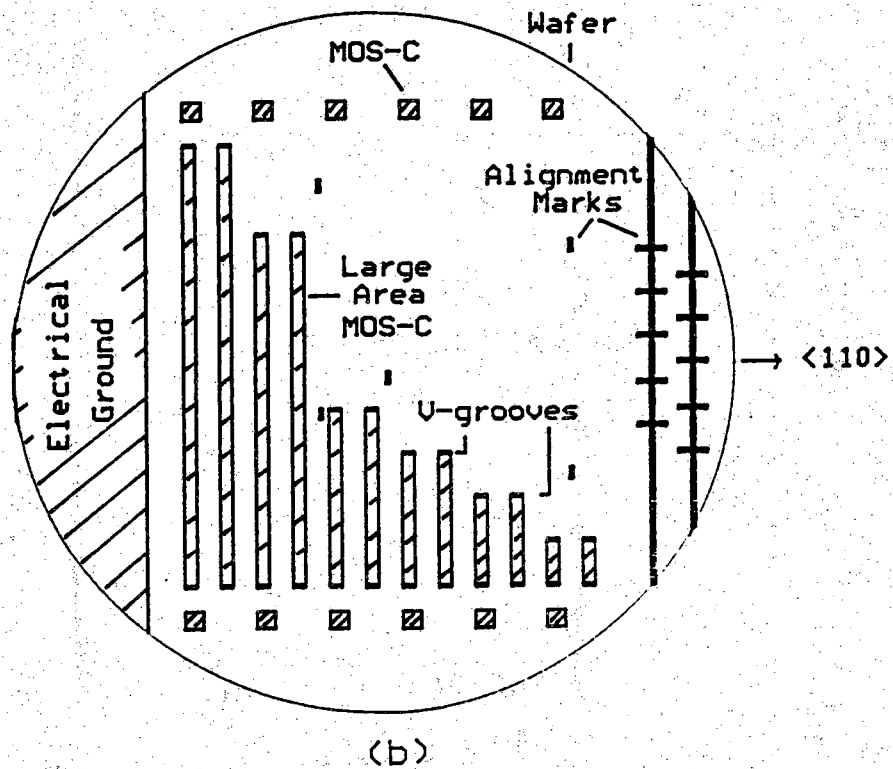
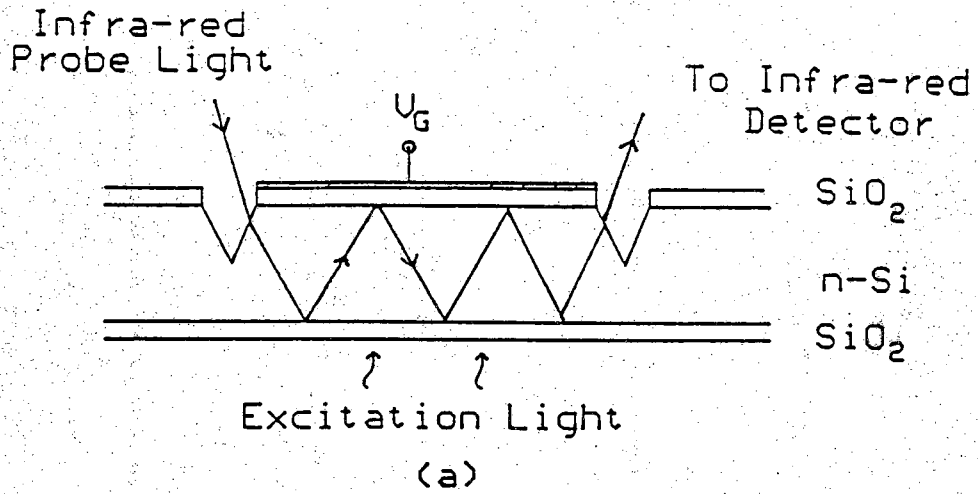


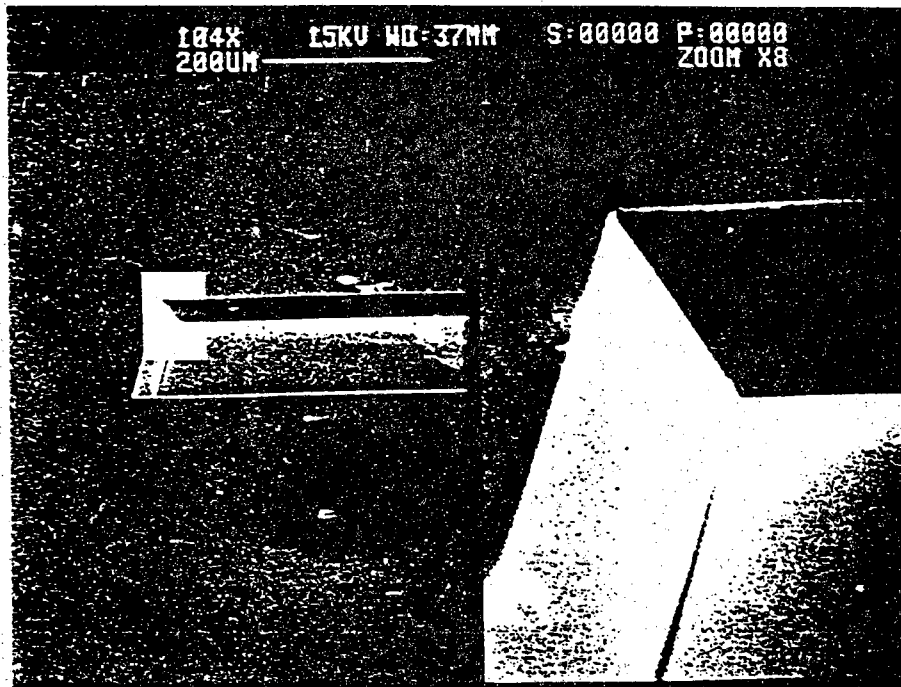
Fig. 3.3 (a) Cross-sectional view of an IR multibounce structure and (b) top view of the complete test structure pattern showing six-paired IR multibounce structures.



IR multibounce structures were fabricated (wafer IR1) using the following processing techniques, which were similar to those described in Section 3.1 except for the anisotropic V-groove etching. The wafer was first cleaned using procedure #2, and was wet oxidized in a Tempress 4 " furnace tube at 1100 °C to achieve an oxide thickness of about 0.4  $\mu\text{m}$ . This oxide layer was later used as a protective mask during the V-groove etching. One of the two polished surfaces was chosen as the front-side on which V-groove windows were defined. After patterning a negative resist on the front-side, the back-side was protected with another layer of negative resist. The wafer was then subjected to buffered HF etch in order to open the  $\text{SiO}_2$  windows. With the resist removed, the V-groove etching was subsequently performed. The anisotropic etching solution consisted of 8 ml : 17 ml : 3 g of DI : ethylenediamine : pyrocatechol and must be freshly prepared each time prior to the beginning of the etching process. The etchants were first agitatedly mixed and then poured into a beaker containing the wafer with the  $\text{SiO}_2$  patterns facing upward. The beaker was next covered with a teflon petri-dish so as to retain the composition of the highly volatile solution. The solution was gradually heated up to 95 °C, which was monitored with a teflon-coated thermometer. The etch rate of the (100) Si :  $\text{SiO}_2$  was about 50  $\mu\text{m/hr}$  : 200  $\text{\AA/hr}$  [78]. A sample of a partially etched V-groove window is pictured in Fig. 3.4. Following the V-groove etching, the  $\text{SiO}_2$  layer was removed; and a new high quality  $\text{SiO}_2$  was grown using dry oxidation. After the oxide growth, the wafer was held with a tweezer and the bottom part of the wafer was dipped into buffered HF. This procedure exposed a large Si surface which was later to serve as an electrical ground. Following the HF dip, the wafer was subjected to phosphorus deposition during which an  $n^+/n$  ohmic contact was formed and the  $\text{SiO}_2$  was stabilized. It should be noted, however, that the bulk substrate was not and could not be properly gettered without affecting the back-side surface. Finally, the front side test patterns were then defined photolithographically.

### 3.3 Measurement Set-ups

Three types of measurements were conducted on MOS-based test structures yielding either the capacitance-voltage (C-V) characteristics, the capacitance-time (C-t) characteristics, or the voltage sweep-capacitance data under dark or illumination conditions. In order to facilitate the measurements



**Fig. 3.4** An SEM photograph of a partially etched V-groove window with different magnifications.

and to eliminate possible surface damage associated with frequent direct probing, all of the test structures were mounted and bonded on TO-headers prior to testing. During measurements, the header was inserted and enclosed in a "light-tube" test fixture pictured in Fig. 3.5. The fixture was made of brass tubing equipped with BNC connectors and a  $N_2$  line. An adaptor, equipped with an adjustable slit and a filter holder, was specially built for the fixture. This arrangement thus allowed one to perform electrical measurements on a given test structure surrounded by a moist or dry  $N_2$  atmosphere and under dark or front-side illuminated conditions. With regard to the illumination sources, either an incandescent lamp or a high intensity Dolan-Jenner 170-D illuminator was used for the measurements. The incandescent lamp and the illuminator was driven by a 118V constant voltage transformer and a Sorensen QB18-12 dc power supply.

All electrical data were obtained through the use of three basic measurement set-ups. Specifically, we employed an Helwett-Packard automated system for most of the C-V and C-t measurements. The system, which is illustrated schematically in Fig. 3.6, consisted of an HP-98035A real time clock for providing a time base reference, two LCR bridges (4274A/4275A) for biasing the test structure and measuring the capacitance, and a HP-9845B desktop computer. The utilized measurement signal of the 4274A and 4275A bridges were respectively 100 kHz and 1MHz at 15 mV rms. (Historically, the 4274A bridge was installed first and provided a maximum test frequency of 100 kHz. The 4275A bridge, on the other hand, has a maximum test frequency of 10 MHz.) Two BASIC programs, CVPLOT<sup>†</sup> and CTDATA, were used for computer collection of the C-V and C-t data. The data were then downloaded, using UNIX6<sup>†</sup>, to the Engineering Computer Network for convenient data manipulation.

Additional C-V and C-t data were also obtained from another self-contained measurement set-up -- the MSI system, which is pictured in Fig. 3.7. This system includes several units, two of which were employed in this work; namely, the model 868 capacitance bridge/sweep generator and the HP-7015A XY recorder. Originally, the sweep (or ramp) generator had a continually adjustable sweep rate of 2.5 mV/sec to 2.5 V/sec. It was subsequently modified by this author so that sweep rates as high as 25 V/sec could be

<sup>†</sup> The CVPLOT and UNIX6 software were written by J. A. Shields [88]; CTDATA was written by the author using Shields's software formats.

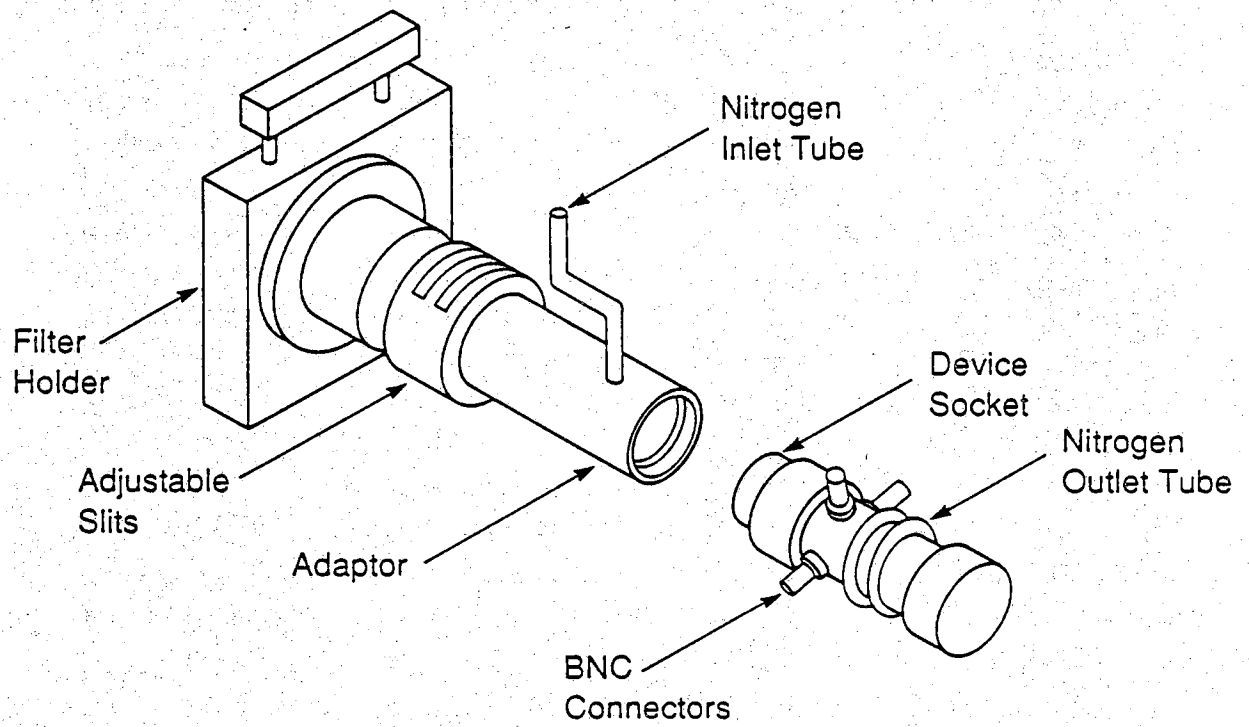


Fig. 3.5 Light tube test fixture.

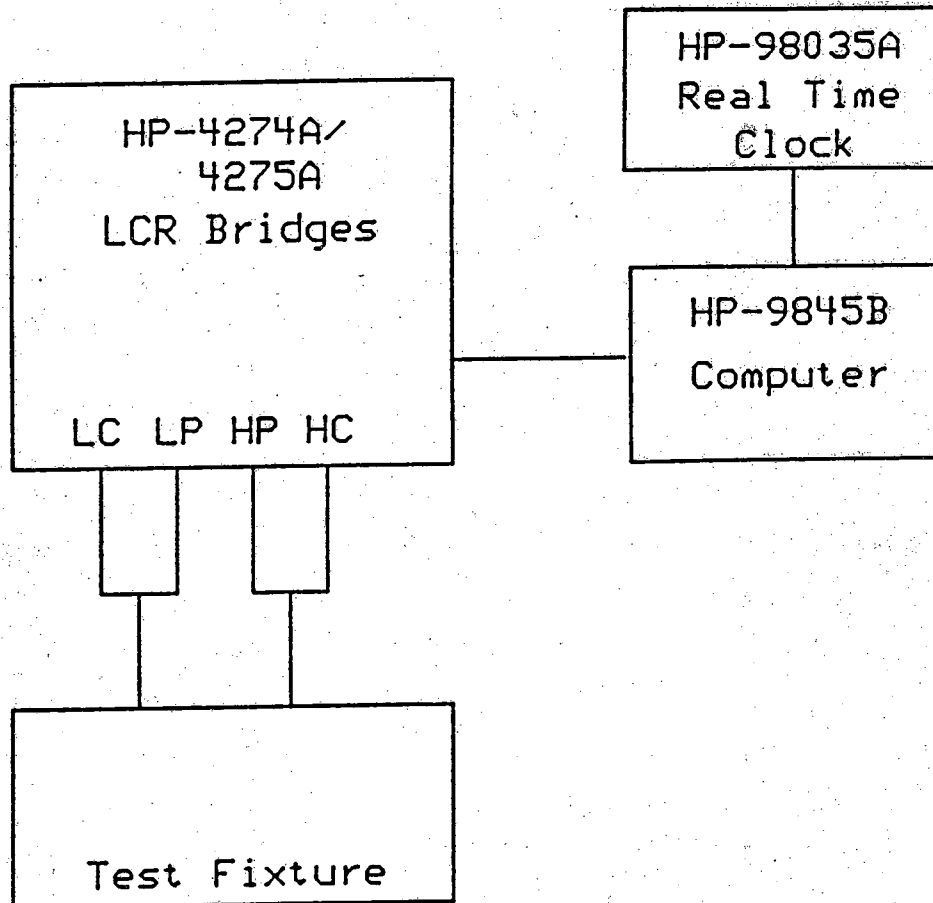


Fig. 3.6 The set-up of the HP automated system for C-V and C-t measurements.

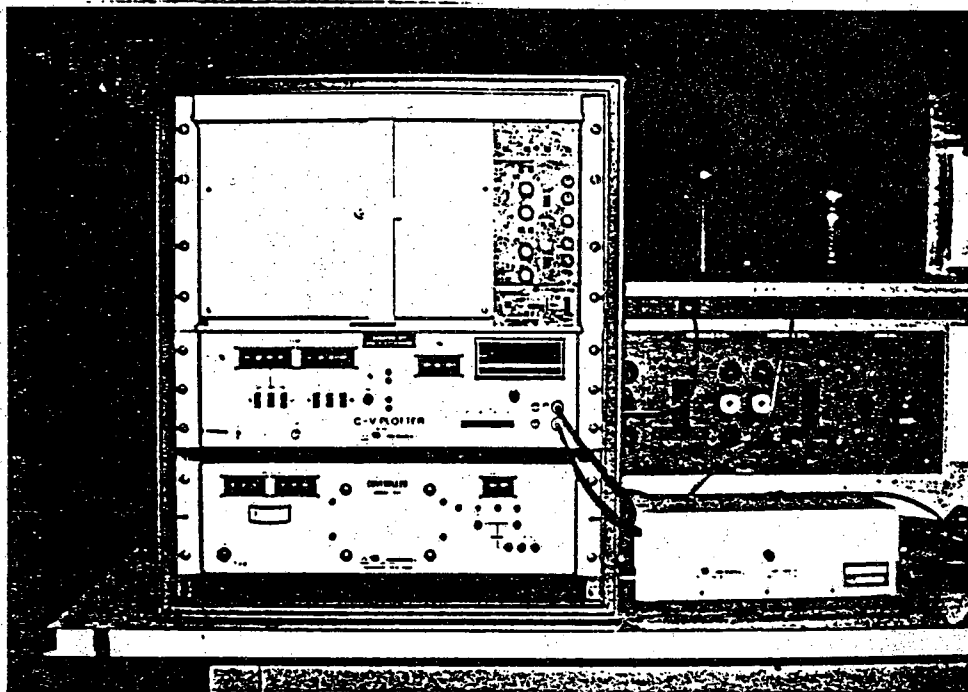


Fig. 3.7 MSI model 868 C-V system. The instrument contains an X-Y recorder (top), a 1 MHz C-V bridge (middle) and a temperature controller (bottom).

attained by simply using an added-on external switch, thereby keeping the original sweep rates unchanged. The capacitance bridge supplied a 1 MHz, 15 mV rms, ac measurement signal which was superimposed on the dc voltage provided by the sweep generator. C-V measurements were either conducted manually, in a point-by-point manner, or automatically using the sweep generator. One can also record C-t measurements using the built-in x-axis time base of the xy recorder. The MSI system was, however, mainly employed for obtaining the voltage sweep-capacitance data under dark conditions. In this application, the sweep voltage was sampled periodically as a function of time with a Keithley 175 DVM. The sweep rate,  $R=dV/dt$ , was calculated from the sampled values. The capacitance, in response to the sweeping action, was read directly from an LED capacitance display. The accuracy of the capacitance, which greatly influenced the subsequent analysis of the sweep-capacitance data, was improved by employing a user-supplied capacitance box connected to the capacitance offset of the MSI system.

A more sophisticated set-up, which was utilized solely for the sweep-capacitance measurements under illumination conditions, is illustrated schematically in Fig. 3.8. Basically, the set-up utilized the existing BIO-RAD Polaron S4600 DLTS system to achieve an accurate capacitance measurement. As shown in Fig. 3.8, a trigger signal was used for synchronous purposes; the saw-tooth sweep voltage and dc biases was supplied by a Wavetek waveform generator and a Heathkit IP-27 dc source, respectively. The capacitance response, measured by a Boonton 72B capacitance meter with a key-in capacitance offset capability, was fed to a DLTS signal processor. The processor then measured the capacitances specified by the two corresponding time windows, and outputted a voltage which was proportional to the capacitance difference. The basic idea of the measurement will be explained in Chapter 5.

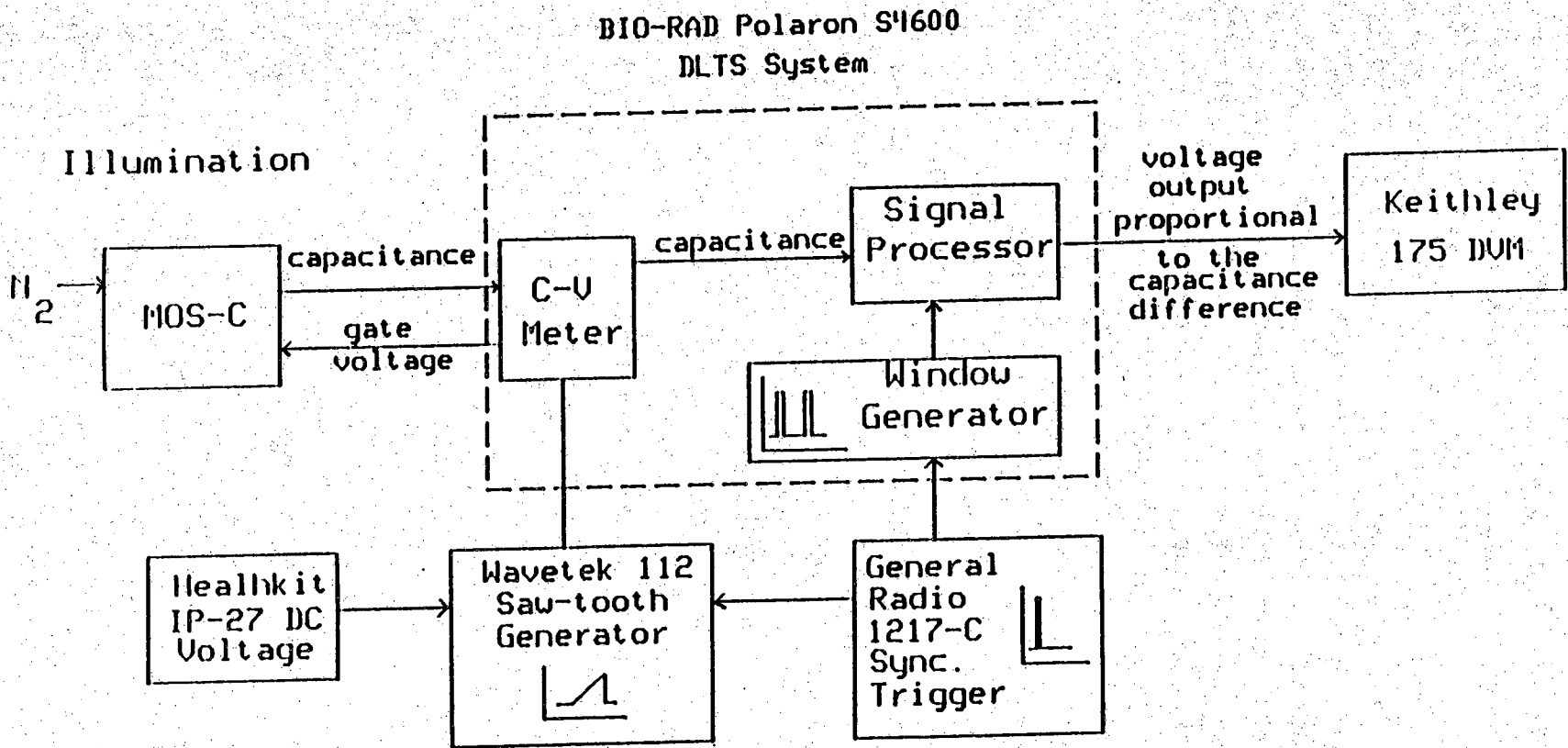


Fig. 3.8 The set-up for the sweep-capacitance measurements.



## CHAPTER 4

### MODIFIED TECHNIQUES FOR DETERMINING $\tau_g$ AND $s_g$

One of the research objectives was to determine the carrier generation parameters in silicon solar cell material using MOS-based test structures. The parameters included the carrier generation lifetime ( $\tau_g$ ) and surface generation velocity ( $s_g$ ); which respectively characterize carrier generation within the carrier-depleted bulk substrate and at the  $\text{SiO}_2/\text{Si}$  interface. In this chapter, we describe and illustrate a photoaccelerated MOS-C C-t transient measurement technique [79] for determining  $\tau_g$ . As the name implies, the method is actually a modification of the conventional "standard" C-t technique which had been introduced and reviewed in Chapter 2. However, the photoaccelerated technique allows one to drastically reduce the transient time through the use of illumination, and hence rapidly deduce  $\tau_g$ . This is important in dealing with solar cell material because of the typically long carrier lifetimes. Following the  $\tau_g$  measurements, we explain and demonstrate the utilization of a new test structure — the Schottky-drained gate-controlled diode (SGCD) [80], which enables one to easily determine  $s_g$  by simply measuring two C-t transients. Finally, the chapter concludes with a summary.

#### 4.1 Photoaccelerated MOS-C C-t Transient Technique [79]

As noted in Chapter 1, the standard C-t transient technique is one of the most widely-used techniques for extracting  $\tau_g$ , and was employed as a major measurement method in this work. Its data acquisition scheme is computer-automated, and its measurement procedures are straightforward — after enclosing the MOS-C in a dark environment, one then simply applies a depleting step voltage to the MOS-C and records the subsequent C-t transient response. The time response depends directly on how rapidly the carriers are thermally generated via generation centers. Consequently, a major problem with this technique is that, as the generation lifetime approaches the

millisecond range (i.e., the thermal generation rate is slow), the transient can be quite lengthy in duration. To circumvent the long transient problem, and to retain the advantage of the C-t automation, the measurement is slightly modified by introducing photogenerated carriers inside the MOS-C through the use of illumination. The measurement theory is detailed as follows.

#### 4.1.1 Measurement Theory

The effect of front-side lateral illumination on the carrier generation in an n-bulk MOS-C is depicted in Fig. 4.1. Under the illustrated situation, the photogenerated minority hole carriers located within one diffusion length of the depletion region are collected under the gate of the MOS-C. The corresponding C-t transient response is, therefore, not only due to the thermal-generated carriers but also due to the photo-generated carriers. As a result, the light-on C-t transient is expected to be short compared to the light-off (dark) C-t transient; hence the name "photoaccelerated" C-t transient.

Paralleling the Zerbst analysis of the C-t data reviewed in Chapter 2, with the MOS-C illuminated and assuming the lateral surface effects have been minimized, one must modify Eq. (2.25) to read

$$-\frac{d}{dt} \left( \frac{C_0}{C} \right)^2 = 2 \frac{K_0}{K_S X_0 N_D} \left( \frac{n_i}{\tau_g} W_G + s_{\text{eff}} n_i + G^* \right) \quad (4.1)$$

where  $G^*$  is the photogeneration rate, and the other symbols have their usual meanings as defined in Chapter 2.

The lateral front-side illumination may possibly give rise to a  $G^*$  exhibiting a time dependence related to  $W_G(t)$ . Taking  $G^*$  to be a general function of  $W_G$  and expanding  $G^*(W_G)$  in a power series, one then obtains

$$G^* = G_0^*(1 + \gamma W_G + \dots) \quad (4.2)$$

For a given experimental condition,  $G_0^*$  and  $\gamma$  are constants. Specifically,  $G_0^*$  is a function of the incident light intensity. " + .... " indicates the possibility of higher-order  $W_G$  terms in the expansion. Substituting Eq. (4.2) into Eq. (4.1) yields

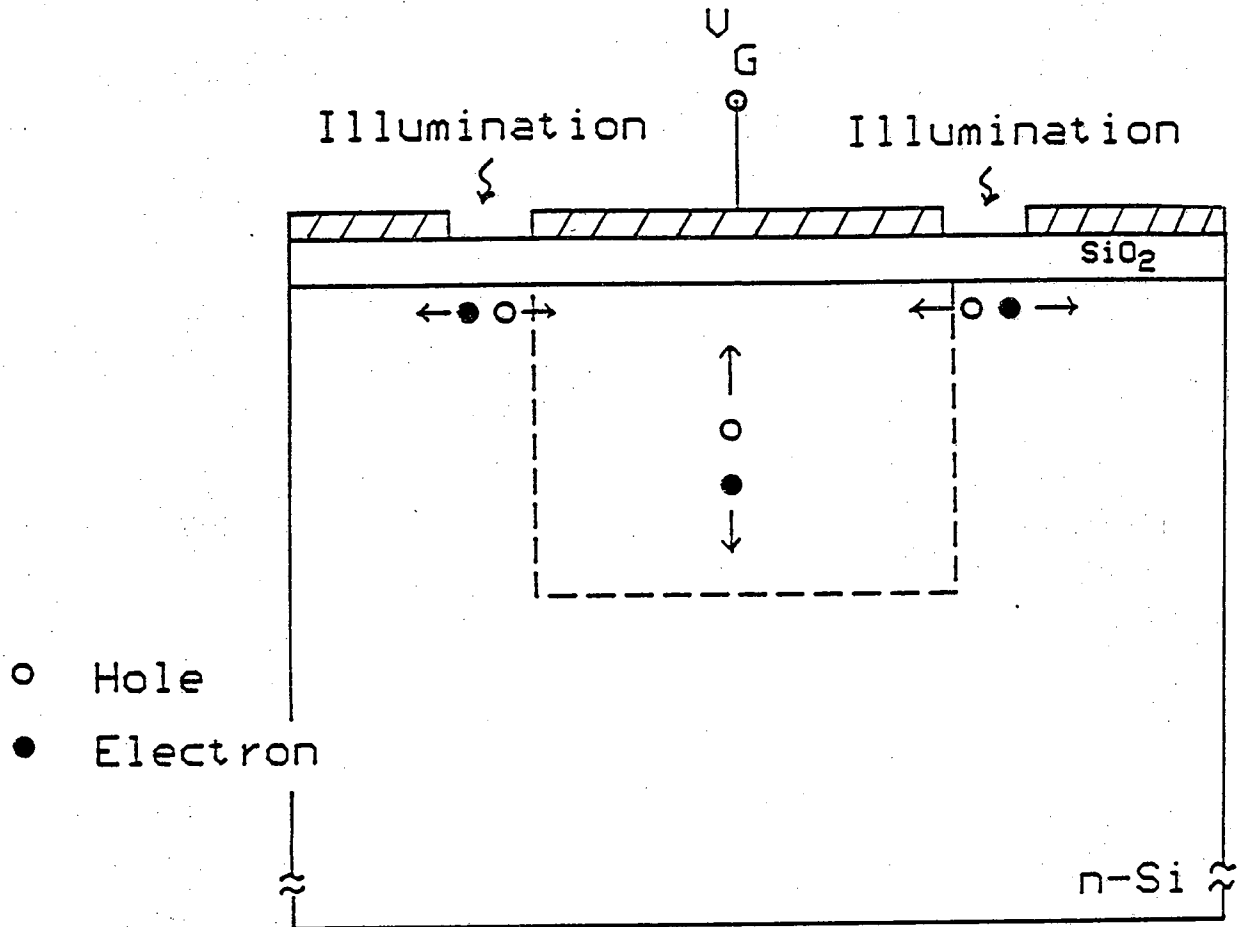


Fig. 4.1 Major carrier generation inside a deeply-depleted MOS-C under illumination conditions.

$$-\frac{d}{dt} \left( \frac{C_O}{C} \right)^2 = 2 \frac{K_O}{K_S x_o N_D} \left[ \left( s_{\text{eff}} n_i + G_o^* \right) + \left( \frac{n_i}{\tau_g} + \gamma G_o^* \right) W_G + \dots \right] \quad (4.3)$$

Eq. (4.3) is the equation used to construct the Zerbst plot with  $W_G \propto C_F/C - 1$ , as reviewed in Chapter 2. As deduced from Eq. (4.3), photogeneration will always increase the extrapolated Y-axis intercept on a Zerbst plot. It could also increase the linear region slope and even give rise to a totally non-linear plot. If, however, higher  $W_G$  terms are negligible and  $n_i/\tau_g \gg \gamma G_o^*$ , only the extrapolated Y-axis intercept will be affected. This latter situation has been the rule in measurements performed on MOS-C's in our laboratory. Assuming that  $n_i/\tau_g \gg \gamma G_o^*$  and the higher-order  $W_G$  terms are negligible, we can simplify Eq. (4.3) to

$$-\frac{d}{dt} \left( \frac{C_O}{C} \right)^2 = 2 \left( \frac{n_i}{N_D} \right) \left( \frac{C_O}{C_F} \right) \frac{1}{\tau_g} \left( \frac{C_F}{C} - 1 \right) + 2 \frac{K_O}{K_S x_o N_D} \left( s_{\text{eff}} n_i + G_o^* \right) \quad (4.4)$$

In rewriting Eq. (4.4) we have expressed  $W_G$  in terms of capacitances for the purpose of constructing the Zerbst plot. Comparing Eq. (4.4) with Eq. (2.28), one notes that the only difference between the light-on and light-off Zerbst plot will be an increase in the extrapolated Y-axis intercept due to  $G_o^*$ . Consequently, if the assumptions leading to Eq. (4.4) are met,  $\tau_g$  can be extracted from a Zerbst plot constructed from the photoaccelerated C-t transient. Finally, it should be noted that the inversion capacitance,  $C_F$ , in Eq. (4.4) is the value obtained under light-off conditions. The effective generation width,  $W_G$ , is simply  $W - W_F$  (which is proportional to  $C_F/C - 1$ ) whether the light is on or off.

### 4.1.2 Experimental Results

To demonstrate the feasibility of the photoaccelerated C-t technique, ring-dot MOS-C's (wafer D5) were fabricated and tested under various illumination conditions. The relevant processing history of wafer D5 was given in Chapter 3. The MOS-C under test was enclosed in the light-tube fixture with a dry  $N_2$  gas flowing in and out of the fixture for all measurements. This precaution was taken to reduce the possible influence of lateral surface effects [81-83] on the  $\tau_g$  measurements. An incandescent lamp, driven by a constant voltage transformer, was employed as the light source. Different light intensities were attained through the use of neutral density filters. In addition, a violet filter was used to ensure that the photogeneration took place as close as possible to the MOS surface, and thereby reduce the risk of perturbing the bulk minority carrier concentration.

Fig. 4.2(a) shows the C-t transient measurements of test structure D5-1 recorded in the dark and under two illumination conditions. Notice from the figure that the transient time was reduced by a factor of 7 at the higher level of illumination. The corresponding Zerbst plots are shown in Fig. 4.2(b). The plots exhibit the same linear slope to within experimental errors. Additional measurements on another structure (D5-2) are displayed in Fig. 4.3, which confirms the reproducibility of the photoaccelerated C-t technique. More detailed analysis and deduced  $\tau_g$  values are summarized in Table 4.1. It should be mentioned that a further reduction in the transient time could readily be achieved using even higher levels of illumination. However, the accuracy of the lifetime deduced from the Zerbst plot understandably decreases — the Zerbst plots become unacceptably "noisy" — with increasing levels of illumination.

### 4.2 Measurements of $s_g$ Using the SGCD Structure [80]

The SGCD test structure consists of a standard MOS-C and an extended Schottky diode (refer to Fig. 3.2). It is actually a form of gate-controlled diode (GCD) [25] except that the PN junction of the GCD is replaced by a Schottky contact. A special feature of the Schottky diode is that it has an extended MOS-area ( $A_D$ ) located inbetween the standard MOS-C and the diode itself. The threshold voltages ( $V_T$ ) are assumed to be the same for the standard MOS-C and the Schottky-related MOS-C. However, no inversion

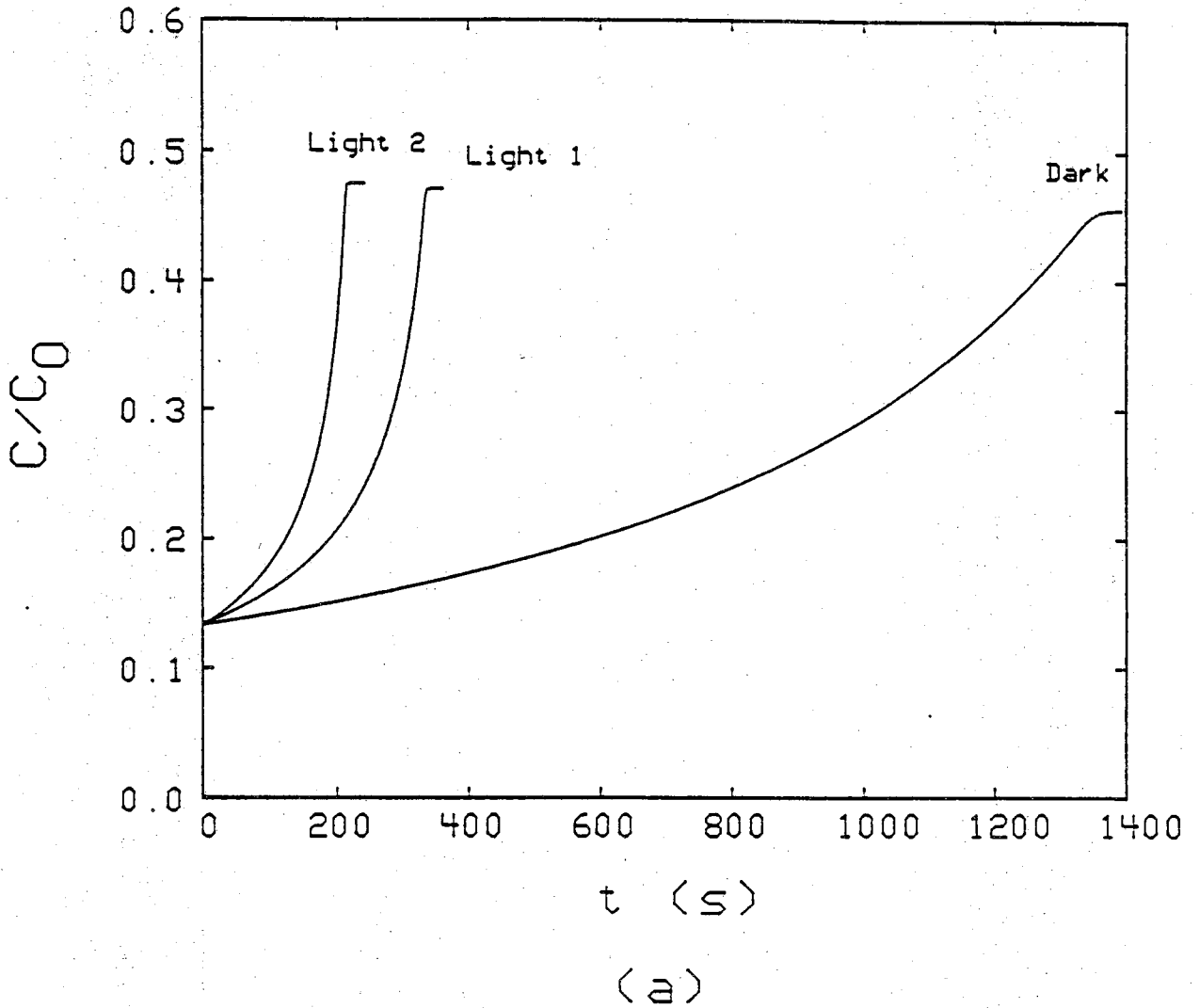


Fig. 4.2 (a) The C-t transients under dark and various illumination conditions. (b) The corresponding Zerbst plots (device D5-1).

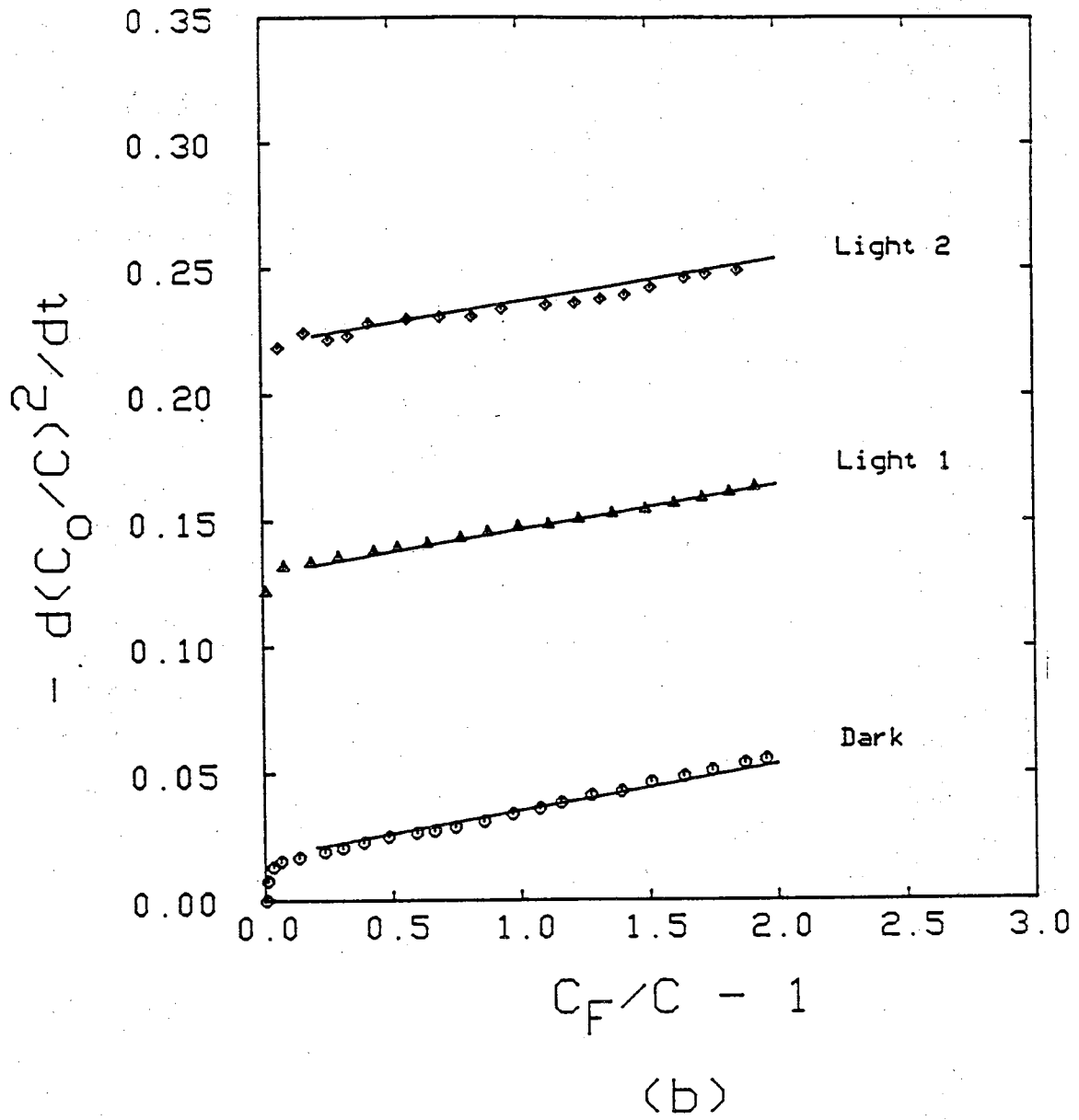


Fig. 4.2 Continued.

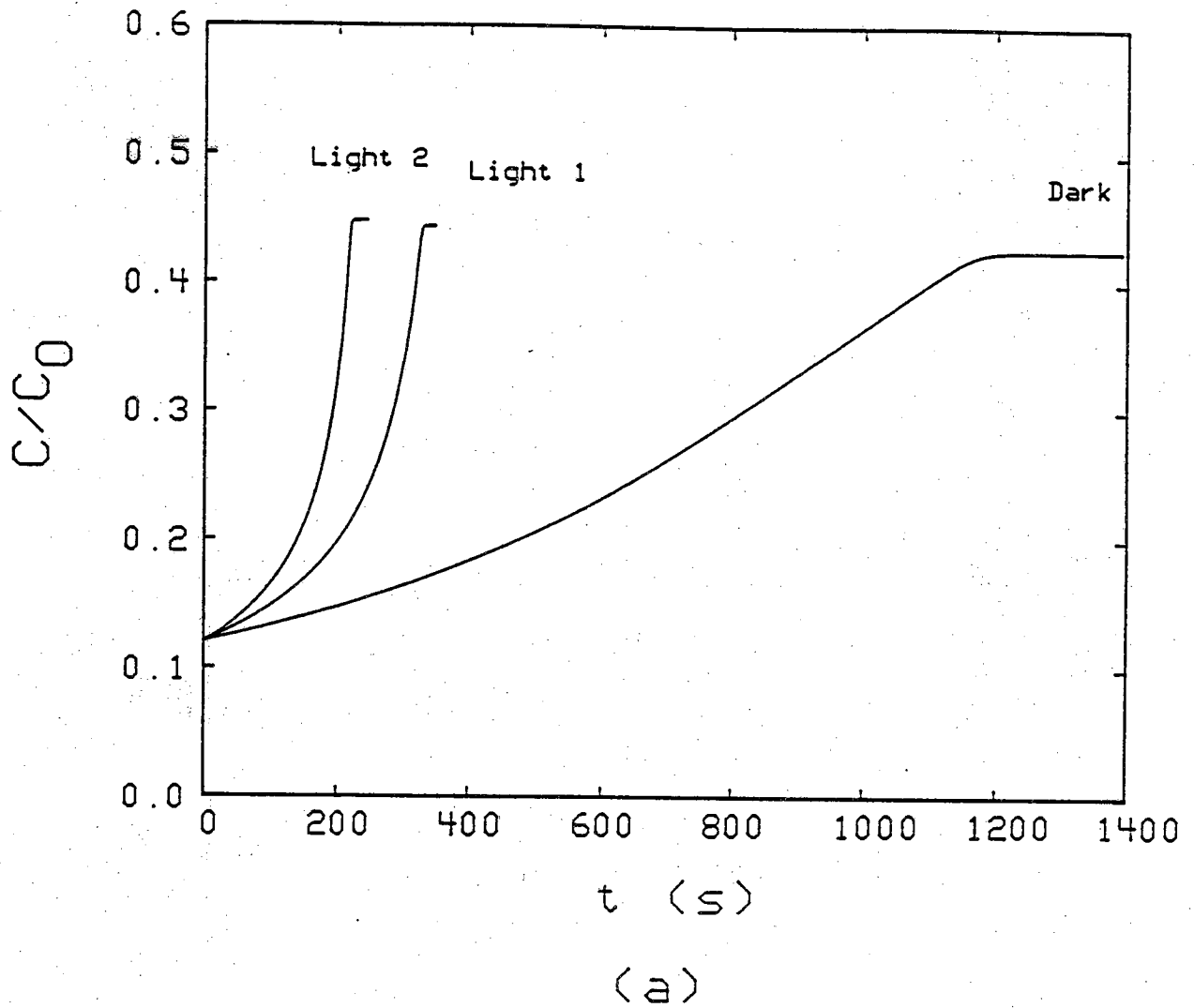


Fig. 4.3 (a) The C-t transients under dark and various illumination conditions. (b) The corresponding Zerbst plots (device D5-2).



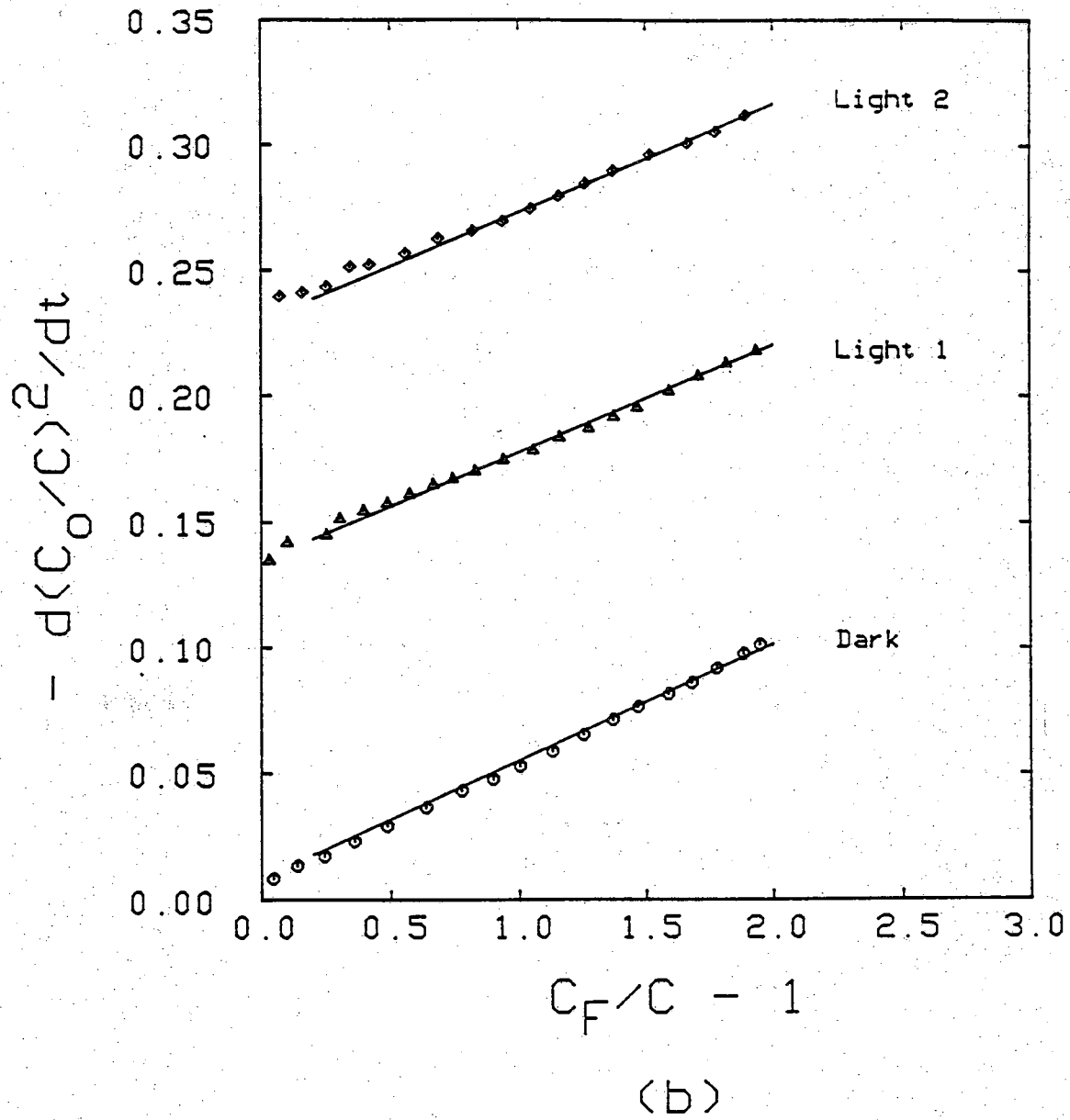


Fig. 4.3 Continued.

**Table 4.1** Summary of  $\tau_g$  Measurements Using Standard and Photoaccelerated C-t Techniques.

D5-1	$C_0=53.67$ pF $C_F=24.29$ pF $N_D=1.90 \times 10^{15} \text{ cm}^{-3}$	
	slope	$\tau_g$ ( $\mu\text{sec}$ )
Dark	0.0170	1176.6
Light 1	0.0176	1136.5
Light 2	0.0168	1190.6

D5-2	$C_0=53.21$ pF $C_F=22.56$ pF $N_D=1.37 \times 10^{15} \text{ cm}^{-3}$	
	slope	$\tau_g$ ( $\mu\text{sec}$ )
Dark	0.0461	642.3
Light 1	0.0424	698.4
Light 2	0.0430	688.6

charge layer could be formed underneath the Schottky-related MOS-C, since the Schottky diode is also reverse-biased at the same time and therefore acts as a minority carrier drain. The diode is herein referred to as the Schottky drain for illustrating its special effects on the lateral inversion charges of the MOS-area. In contrast with the conventional GCD where one monitors the I-V characteristics of the PN junction diode for determining  $s_g$ , the measurement approach in using the SGCD is based on C-t transient measurements applied to the standard MOS-C while the Schottky drain is biased at  $V_D = 0$  and  $V_D = V_T$ . The following subsection details the measurement principle for determining  $s_g$  using the SGCD structure.

#### 4.2.1 Measurement Theory

Fig. 4.4 (a) and (b) illustrate the major carrier generation components contributing to the relaxation of the deeply-depleted standard MOS-C when the Schottky drain is zero and  $V_D = V_T$  biased, respectively. With  $V_D = 0$ , the standard MOS-C and the Schottky drain are totally decoupled. The C-t characteristics derived from the standard MOS-C is then of the usual form. With  $V_D = V_T$ , the interface beneath the Schottky-related MOS-C is deeply-depleted (because of the Schottky-drain action), and carriers are therefore generated through the interfacial states located at the depleted surface. Due to the symmetry of the test structure, and also since both the deeply-depleted standard MOS-C and Schottky-drain act as an infinite minority carrier sink, exactly one-half of the generated carriers flow into the depletion region of the standard MOS-C, as visualized in Fig. 4.4 (b). Obviously, the length of the C-t transient exhibited by the standard MOS-C decreases. In addition, since the Schottky-related MOS-C is already deep-depleted, pulsing the standard MOS-C has no effect on the depletion-width beneath the Schottky-related MOS-C.

It should be mentioned that with  $V_D > V_T$  (both are negative quantities for n-bulk substrates), the surface is only partially depleted and the surface generation rate is not at its maximum. On the other hand, with  $V_D < V_T$ , the depletion width beneath the Schottky-related MOS-C extends beyond  $W_F$ . The extra bulk generation from the expanded depletion region contributes a large lateral current to the standard MOS-C, thereby adversely affecting the  $s_g$  measurement. At  $V_D = V_T$ , however, the surface is completely depleted and the depletion width is relatively small; hence the lateral bulk generation is at a

Schottky-related  
MOS-C

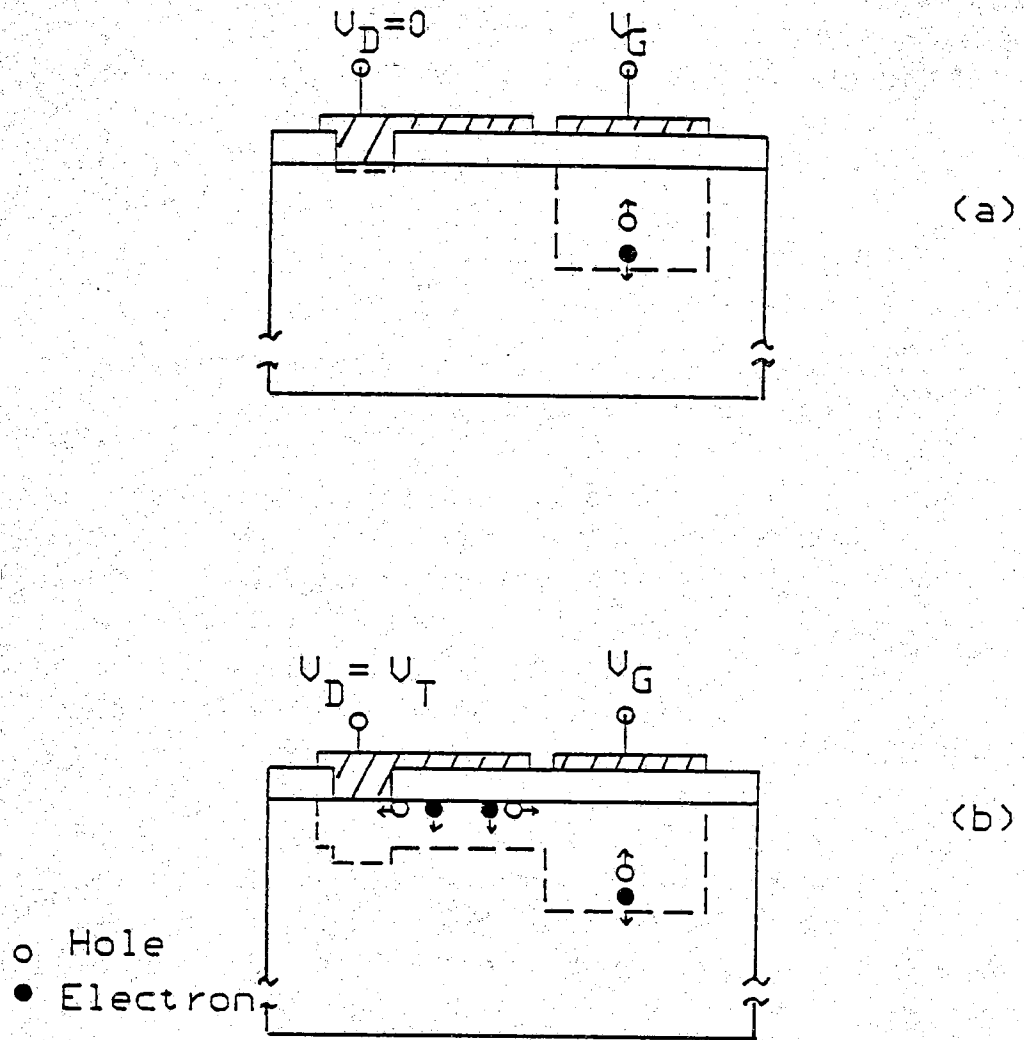


Fig. 4.4 Major carrier generation inside the SGCD structure at (a)  $V_D = 0$  and (b)  $V_D = V_T$ .

minimum.

Assuming the bulk generation under the Schottky-related MOS-C is negligible (which will be elaborated on later), one can rewrite Eq. (2.28) as

$$\begin{aligned}
 -\frac{d}{dt} \left( \frac{C_O}{C} \right)^2 &= 2 \left( \frac{n_i}{N_D} \right) \left( \frac{C_O}{C_F} \right) \frac{1}{\tau_g} \left( \frac{C_F}{C} - 1 \right) \\
 &+ 2 \frac{n_i K_O}{K_S x_o N_D} s_{\text{eff}} \\
 &+ 2 \frac{n_i K_O}{K_S x_o N_D} \left( \frac{A'_D}{A_G} \right) s_g
 \end{aligned} \tag{4.5}$$

where  $A'_D$  is equal to half of the Schottky-related MOS-C area, since only one-half of the generated carriers beneath the Schottky-related MOS-C flow to the standard MOS-C. As is obvious from Eq. (4.5), Zerbst plots constructed from C-t transient data corresponding to  $V_D = 0$  and  $V_D = V_T$  should therefore have the same linear slope but different Y-axis intercepts. One can equate the  $\delta$ -intercept (i.e., the difference obtained from the two extrapolated y-intercepts) to the third term of Eq. (4.5) and thereby readily deduce  $s_g$ .

$$s_g = \frac{1}{2} \frac{N_D}{n_i} \frac{K_S x_o}{K_O} \frac{A_G}{A'_D} \left( \delta\text{-intercept} \right) \tag{4.6}$$

As previously suggested, there is in reality a nonzero bulk component from the Schottky-related MOS-C which should be accounted for in order to extract a more accurate  $s_g$ . To quantify the bulk component, we utilize the energy band diagram and the corresponding effective generation plot pictured in Fig. 4.5. Pierret [84] argued that, when  $V_D = V_T$ , the effective generation width underneath the Schottky-related MOS-C is approximately  $W_F - W_I$  as depicted in Fig. 4.5b.  $W_F$  is the maximum equilibrium depletion width and is doping dependent;  $W_I$  is the depletion width when  $E_I = E_F$  at the Si/SiO<sub>2</sub> interface. Notice that from  $x=0$  to  $x=W_F - W_I$  the generation rate is approximately constant and is equal to  $\frac{n_i}{\tau_g}$ . The bulk generation component

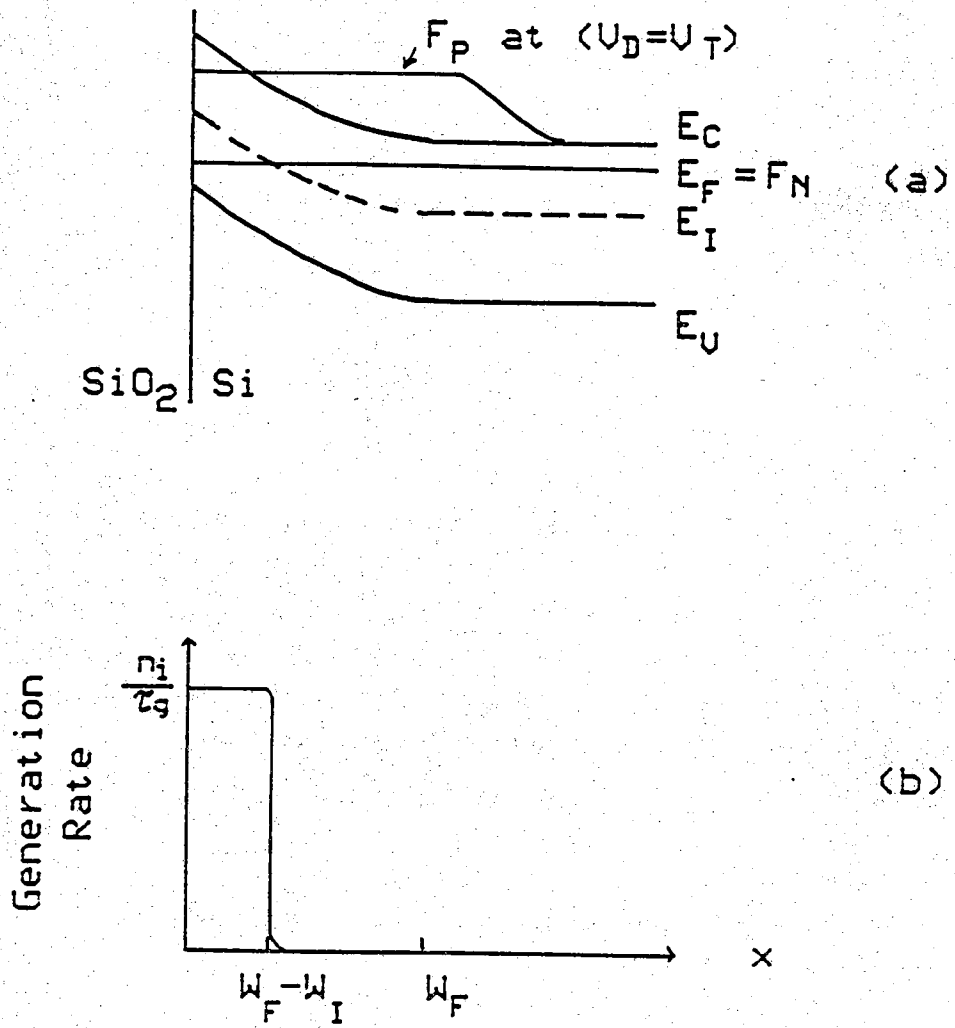


Fig. 4.5 (a) Energy band diagram and (b) the effective generation width beneath the Schottky-related MOS-C area when  $V_D = V_T$ .

$G'_D$ , which is proportional to  $-d(C_O/C)^2/dt$ , is approximately given by

$$\begin{aligned} G'_D &= A'_D \frac{n_i}{\tau_g} (W_F - W_I) \\ &= A'_D \frac{n_i}{\tau_g} W_F \left( 1 - \frac{W_I}{W_F} \right) \end{aligned} \quad (4.7)$$

$W_F$  and  $W_I$  are respectively expressed as [69]

$$W_F = \left[ (kT/q) \frac{4K_S \epsilon_o}{qN_D} (2U_F) \right]^{1/2} \quad (4.8a)$$

$$W_I = \left[ (kT/q) \frac{4K_S \epsilon_o}{qN_D} (U_F) \right]^{1/2} \quad (4.8b)$$

Thus

$$G'_D = 0.293 \frac{n_i}{\tau_g} W_F A'_D \quad (4.9)$$

We note that the bulk generation component,  $G_G$ , of the standard MOS-C in the SGCD structure is

$$G_G = \frac{n_i}{\tau_g} (W - W_F) A_G \quad (4.10)$$

Let us perform a sample computation to gauge the relative size of  $G'_D$ . Let  $W_F = 0.6 \mu\text{m}$ ,  $x_o = 0.2 \mu\text{m}$  and  $A'_D = A_G/2$ . If we select  $C_F/C - 1 = 1$ , which corresponds to  $W - W_F = W_F + \frac{K_S}{K_O} x_o = 1.2 \mu\text{m}$ , then

$$\frac{G_D'}{G_G} = 7.33\% \quad (4.11)$$

Although not large, the lateral bulk component cannot be neglected.

The foregoing sample computation understandably yields a percentage error which depends on  $W_F$ ,  $x_0$  and  $A_D'$ . Consequently the percentage error differs from device to device with different physical characteristics. When calculating the  $s_g$  parameter, one has first to compute the percentage error for a given device (say,  $x\%$ ). Next, the  $\delta$ -intercept is determined from the difference in Y-axis intercepts of the two Zerbst plots. From the Zerbst plot with  $V_D = 0$ , one then computes  $x\%$  of the  $-d(C_O/C)^2/dt$  value at the  $C_F/C-1 = 1$  point. A corrected  $\delta$ -intercept is obtained by subtracting the evaluated error from the original  $\delta$ -intercept.

#### 4.2.2 Experimental Results

SGCD test structures were fabricated on (100) 3-5 ohm-cm silicon solar cell substrates (wafer J24) and also on (100) 2-3 ohm-cm n-bulk substrates (wafer O5) for comparison purposes. Wet  $N_2$  gas and appropriate gate biasing were used to couple the Schottky drain and the standard MOS-C by creating an inversion charge layer inbetween the two structures. (The separation between the drain and the MOS-C was 10  $\mu\text{m}$ .) The  $V_D$  biases were obtained through the use of a dry cell connected to a variable resistance, thereby minimizing possible electrical noise interference on the C-t measurements.

Typical I-V characteristics of a fabricated Schottky diode is shown in Fig. 4.6. Fig. 4.7 to 4.9 illustrate the C-t transients and corresponding relevant Zerbst plots of different test structures under various  $V_D$  biases. The deduced  $s_g$  values and other pertinent parameters are summarized in Table 4.2. Prior to accounting for the bulk generation correction, the deduced  $s_g$  varied from 1.1 to 2.7 cm/sec. The subsequent correction gave  $s_g$  values from 1.02 to 2.4 cm/sec, illustrating that the bulk generation beneath the Schottky-related MOS-C indeed introduces a relative small correction. The  $s_g$  values obtained from the SGCD structures were typical parameters for well-annealed structures [68].



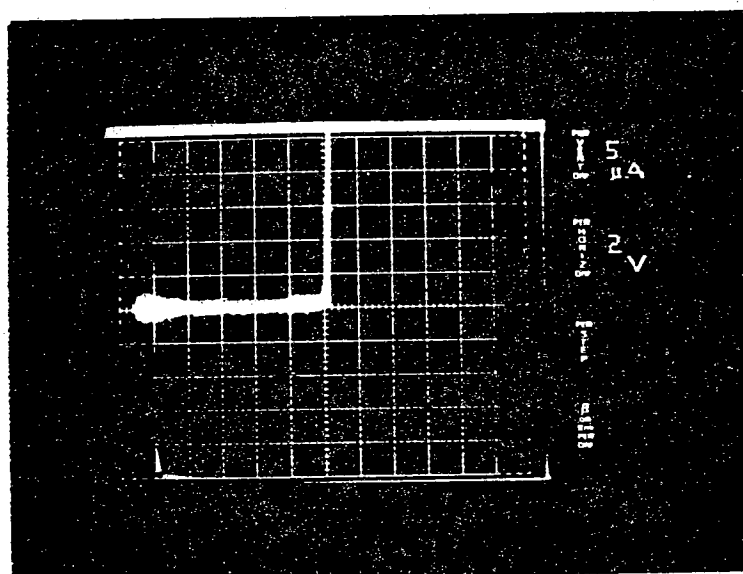


Fig. 4.6 Sample I-V characteristics of an Al/n Schottky diode.

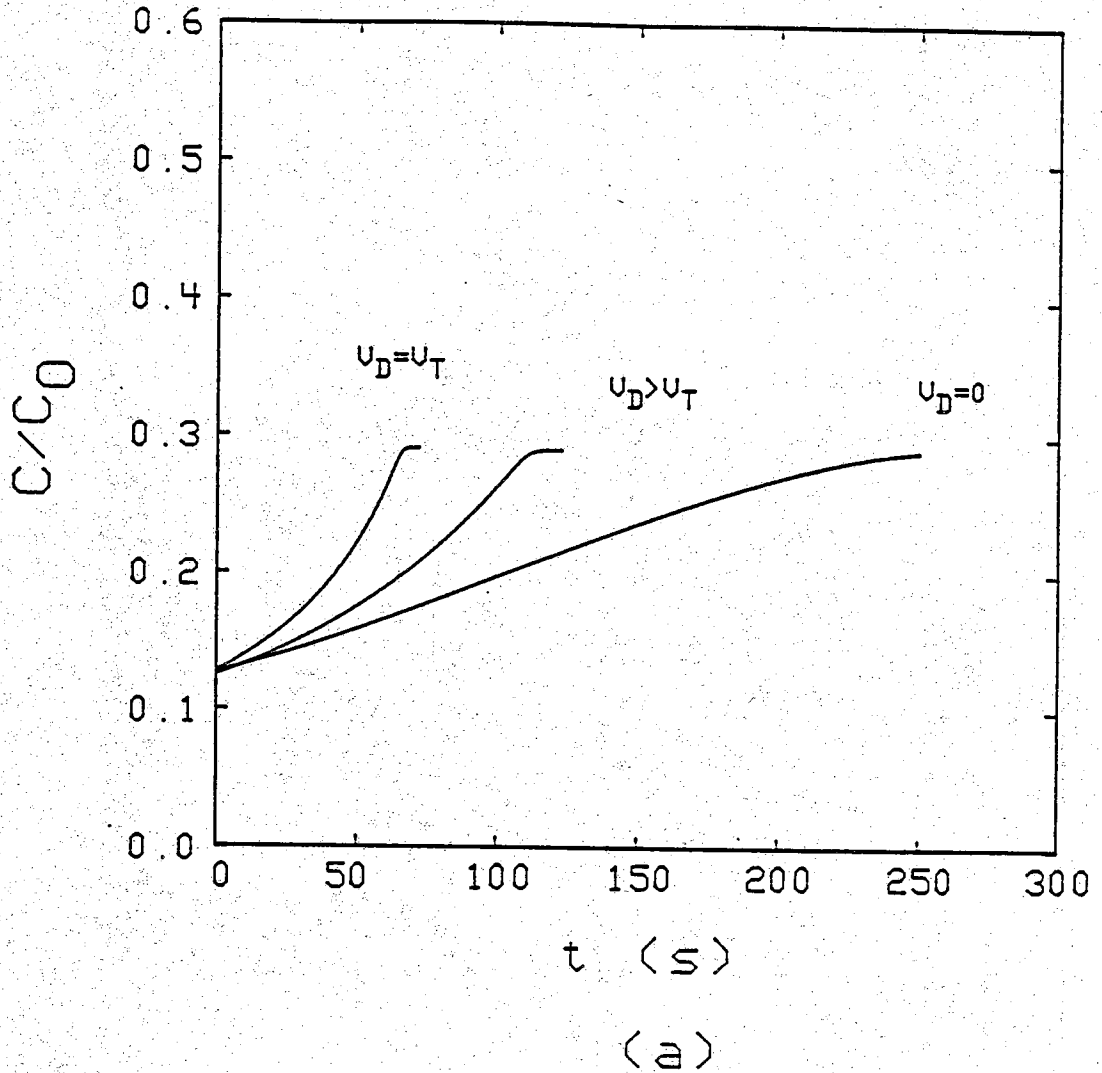


Fig. 4.7 (a) C-t transients and (b) relevant Zerbst plots at various  $V_D$  biases for device J24-1. ( $C_O = 95.3$  pF;  $C_F = 26.4$  pF;  $x_o = 0.096$   $\mu\text{m}$ ;  $N_D = 1.8 \times 10^{15}$   $\text{cm}^{-3}$ ;  $\tau_g = 90.8$   $\mu\text{sec}$ ; slope = 0.38.)

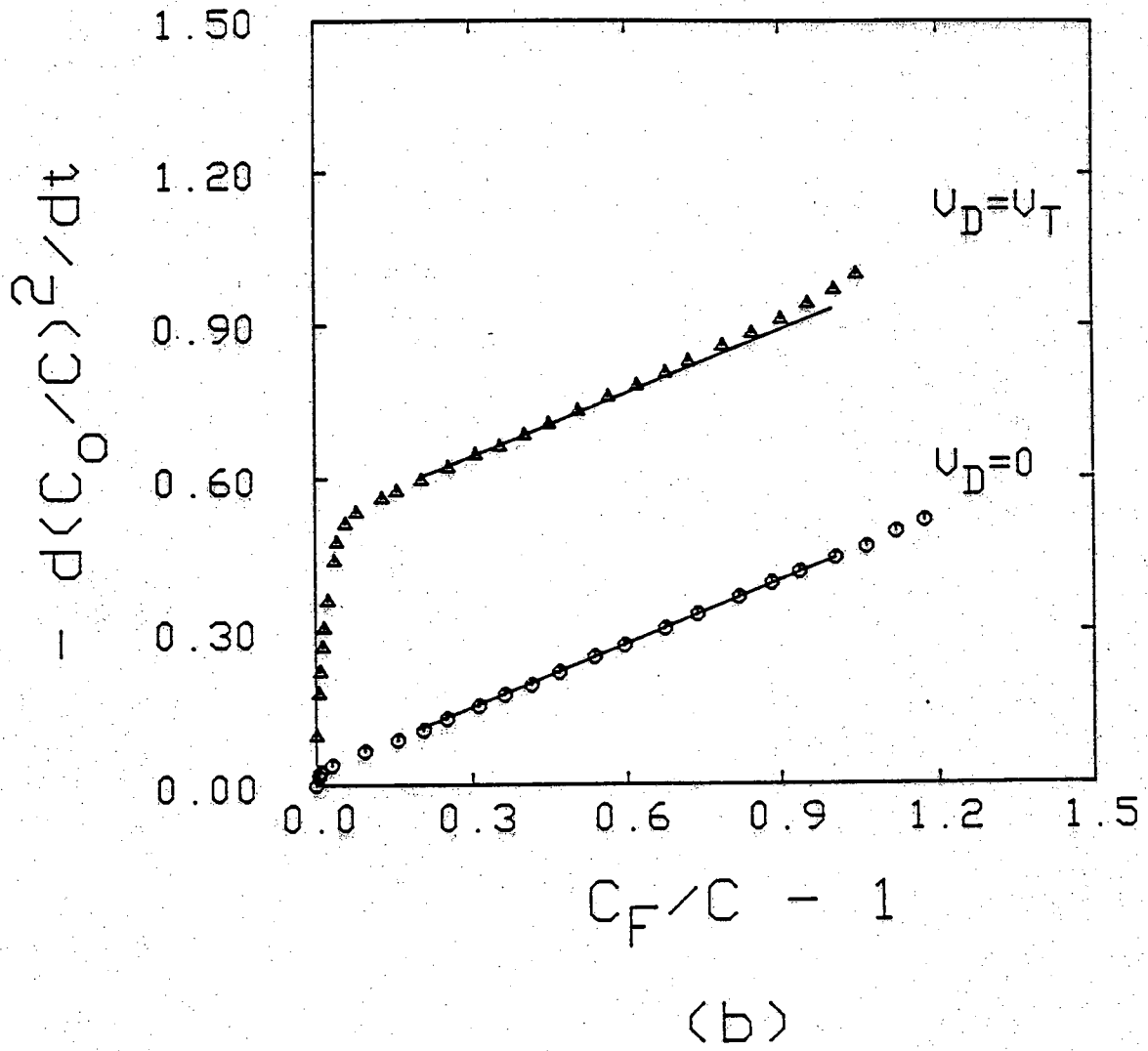


Fig. 4.7 Continued.

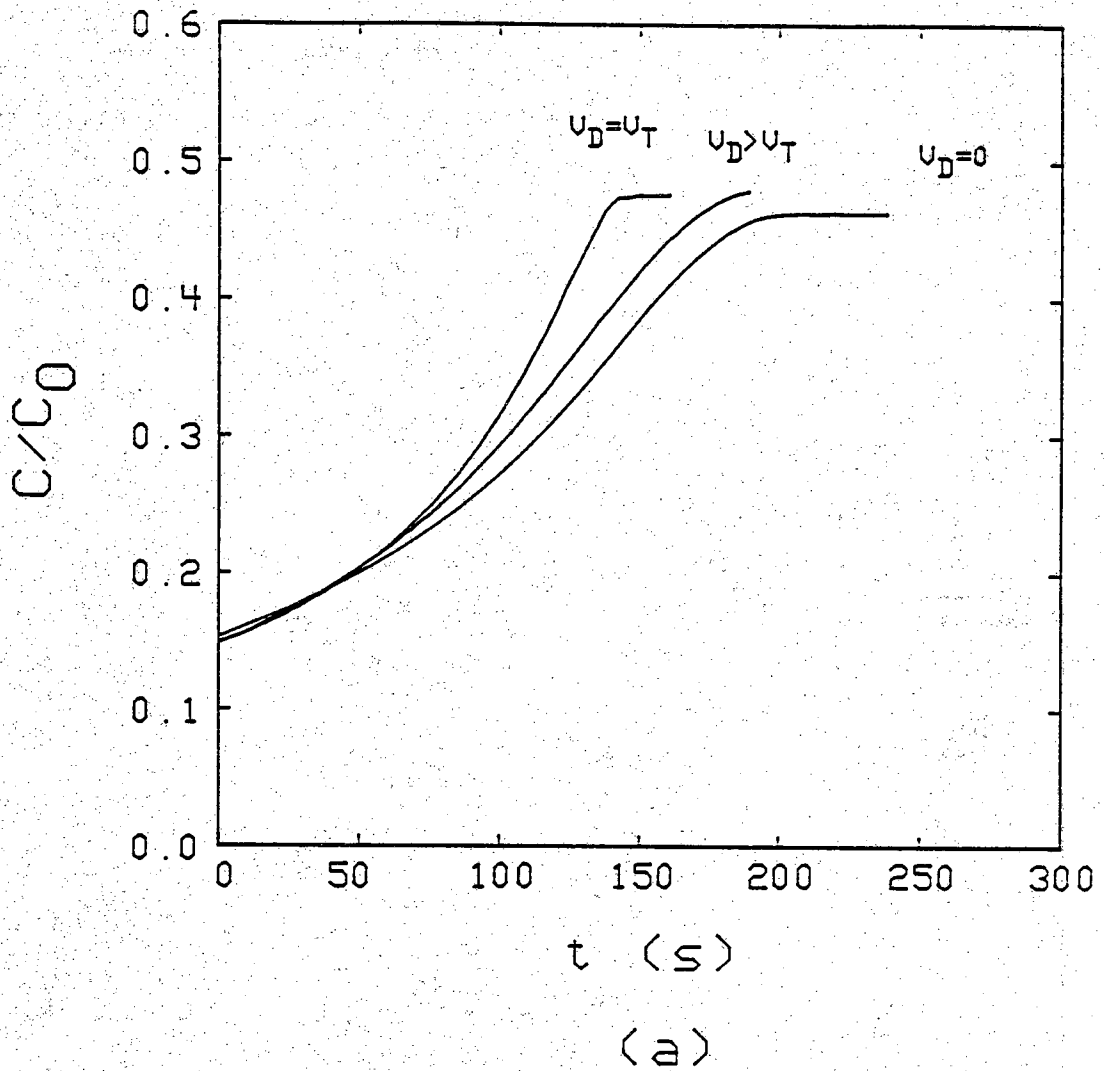


Fig. 4.8 (a) C-t transients and (b) relevant Zerbst plots at various  $V_D$  biases for device O5-L. ( $C_O = 41.6$  pF;  $C_F = 21.3$  pF;  $x_o = 0.194$   $\mu\text{m}$ ;  $N_D = 2.17 \times 10^{15}$   $\text{cm}^{-3}$ ;  $\tau_g = 90.8$   $\mu\text{sec}$ ; slope = 0.17.)

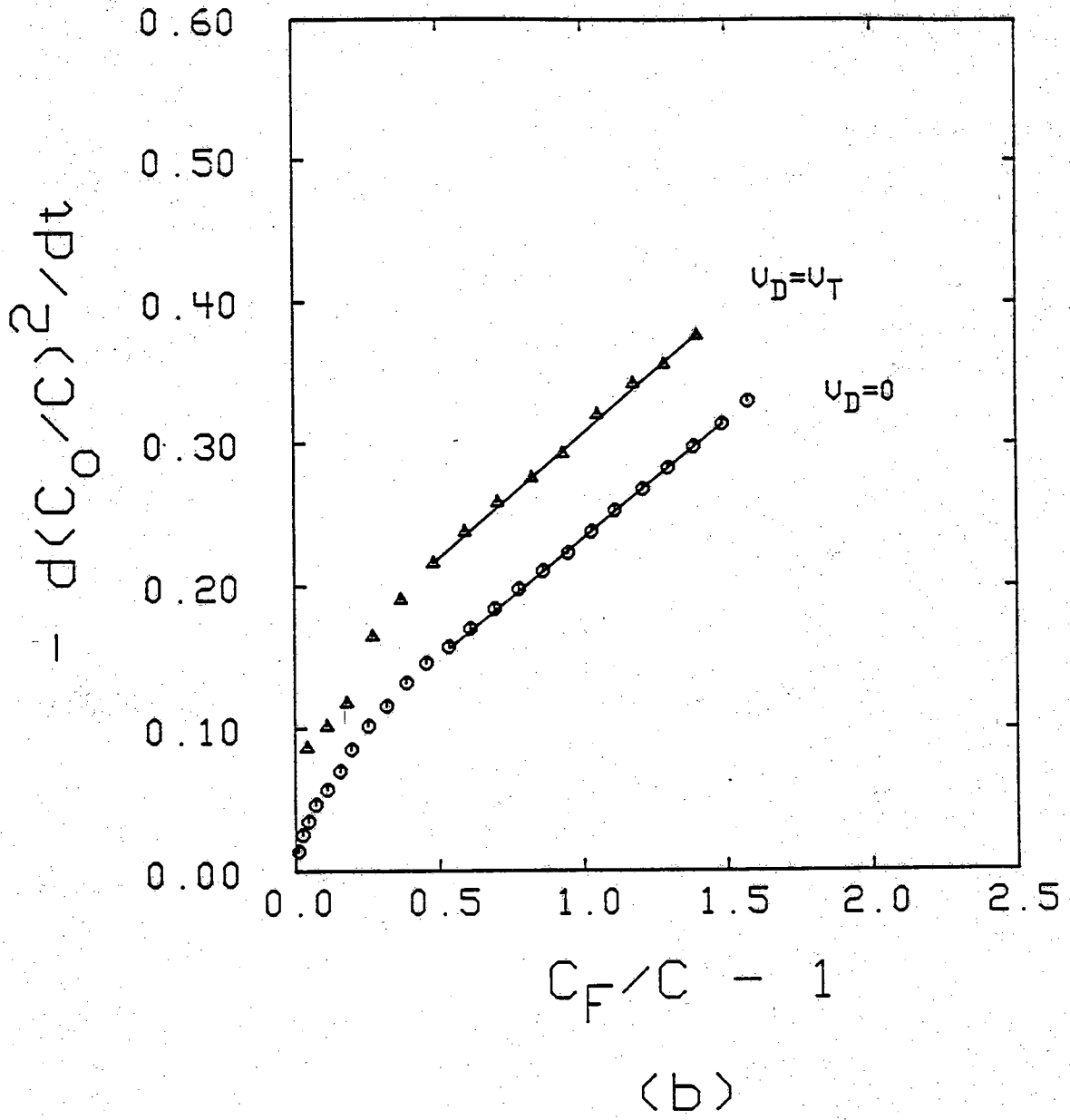


Fig. 4.8 Continued.

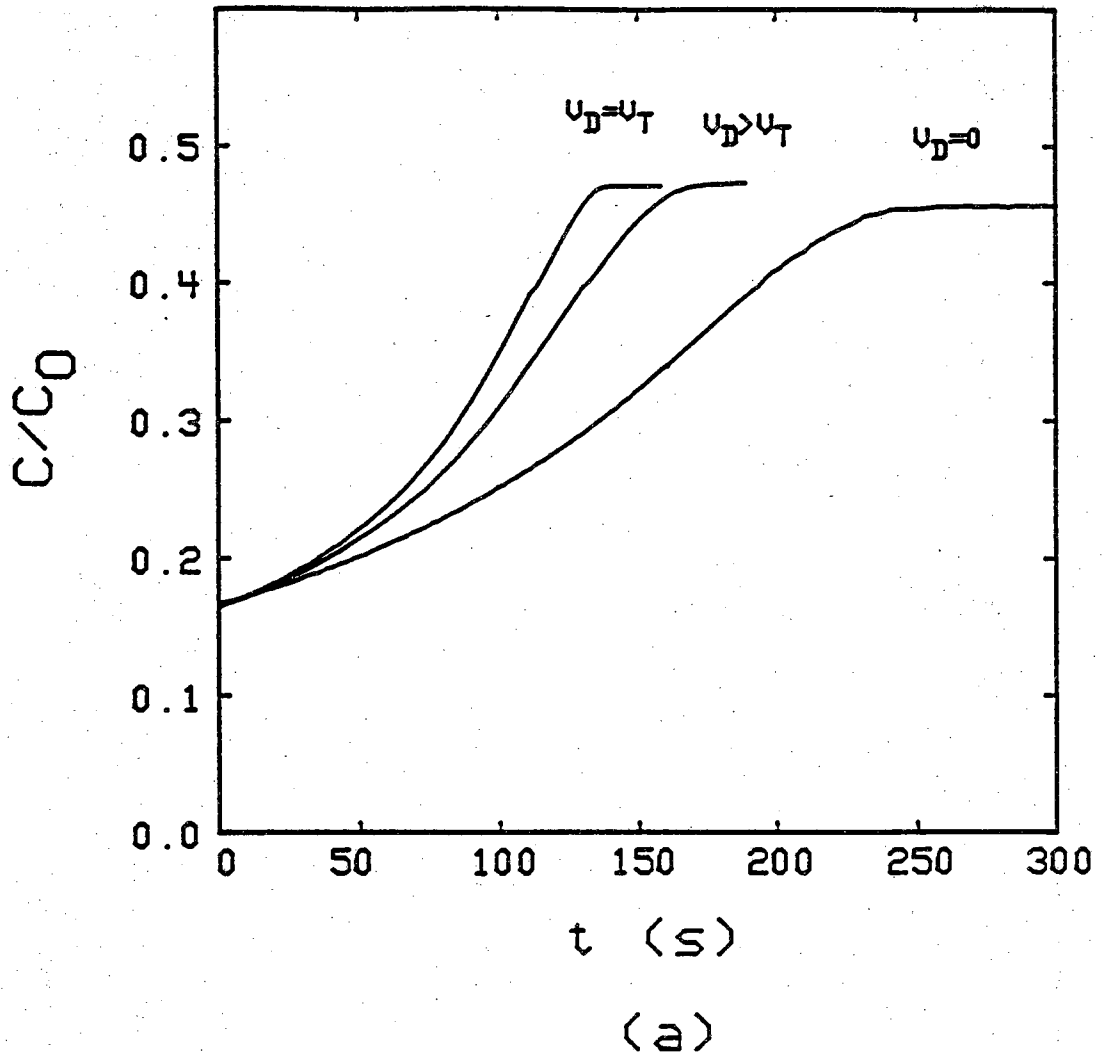


Fig. 4.9 (a) C-t transients and (b) relevant Zerbst plots at various  $V_D$  biases for device O5-S. ( $C_O = 44.9$  pF;  $C_F = 20.5$  pF;  $x_o = 0.192$   $\mu\text{m}$ ;  $N_D = 1.82 \times 10^{15}$   $\text{cm}^{-3}$ ;  $\tau_g = 173.1$   $\mu\text{sec}$ ; slope = 0.12.)

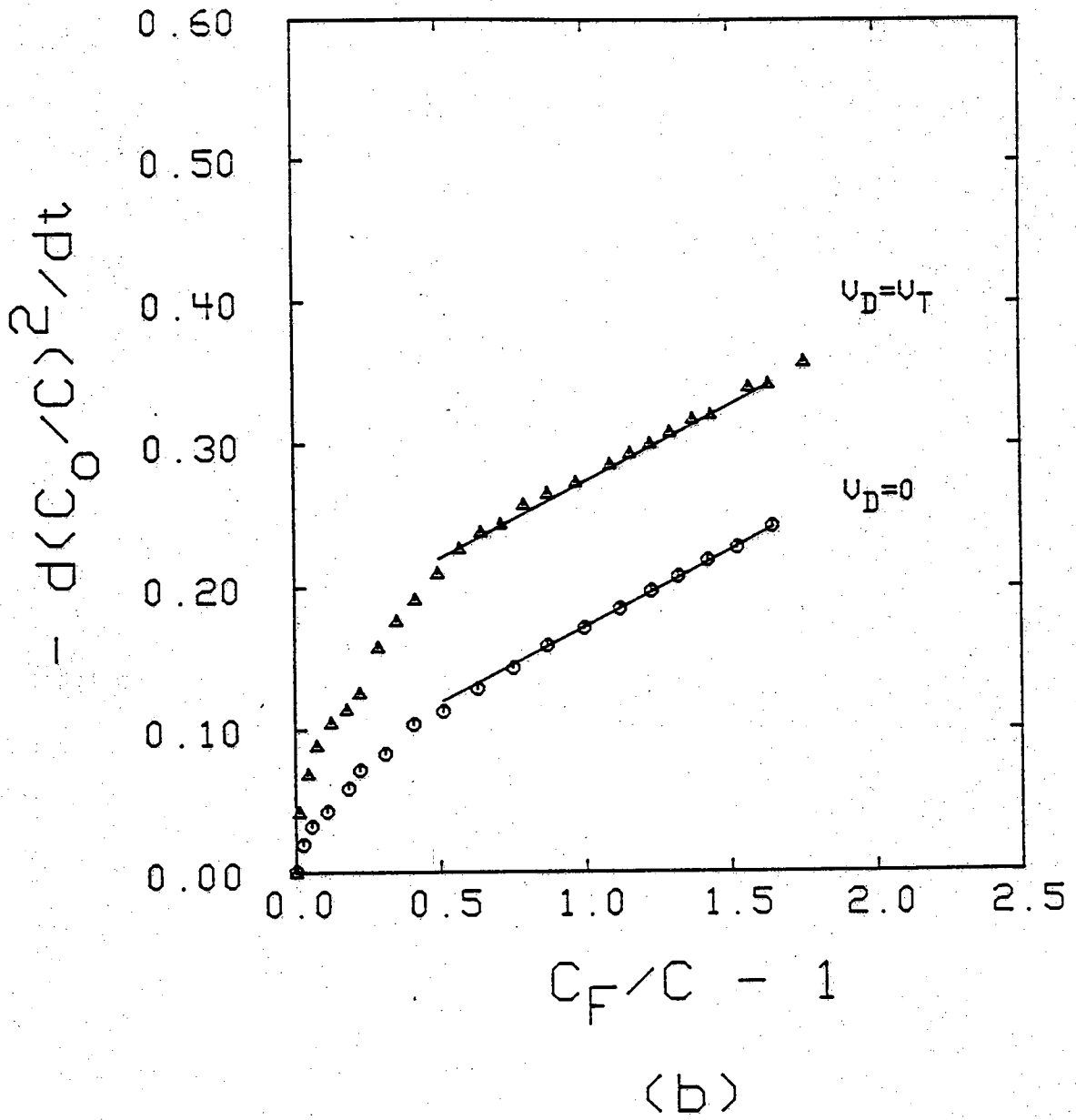


Fig. 4.9 Continued.

Table 4.2 Summary of  $s_g$  Measurements Using the SGCD Test Structure.

Device #	$A_D'$ ( $\times 10^{-3} \text{ cm}^2$ )	$\delta$ -intercept	$s_g$ (cm/s)	Corrected $\delta$ -intercept	Corrected $s_g$ (cm/s)
J24-1	1.250	0.410	2.6	0.370	2.4
O5-L	1.250	0.074	1.1	0.069	1.02
O5-S	0.625	0.110	2.7	0.090	2.20



For the PN junction GCD, Pierret [26] has shown that the measured  $s_g$  is smaller than the true  $s_g$  because weak inversion typically forms along a portion of the MOS-surface as a result of the lateral current flow. Inevitably, the SGCD has the same problem. However, as with PN junction GCD measurements, the  $s_g$  value deduced is still of value for comparative purposes. Concerning the measured  $\tau_g$ , it is interesting to point out that, because of different fabrication processes, the generation lifetime of wafer J24 was only in the 100  $\mu\text{sec}$  range, which was much smaller in magnitude as compared to that presented in the photoaccelerated C-t measurements. Finally, as a potentially useful aside, we note that steady-state deep-depletion C-V characteristics can be obtained using the SGCD structure. This is illustrated in Fig. 4.10. Unlike the PN junction diode, the Schottky diode cannot supply minority carriers. Thus when  $V_D < V_G < V_T$  (n-bulk structure), the standard MOS-C deep depletes. If  $V_G < V_D$  the depletion width beneath the standard MOS-C pegs at the depletion width beneath the Schottky-related MOS-C and the observed capacitance becomes constant.

### 4.3 Summary

In this chapter we have described a photoaccelerated C-t transient technique for reducing measurement time and hence rapidly deducing  $\tau_g$ . The method is of particular interest in solar cell work where  $\tau_g$  is in the 1 msec range. The technique was subsequently demonstrated with MOS-C structures fabricated on silicon solar cell material. We also introduced a new test structure — the Schottky-drained gate controlled diode. The SGCD allows one to deduce  $s_g$  based on C-t type measurements. Experimental results were presented to illustrate use and application of the structure. Extracted  $s_g$  values were in the range of 1-3 cm/sec. The structure has a distinct advantage over the PN junction GCD in that it is only slightly more complicated to fabricate and interrogate than a simple MOS-C. In addition, the structure may be of special interest in probing semiconductor systems where PN junctions are difficult to fabricate or possibly in establishing steady-state deep-depletion C-V characteristics.

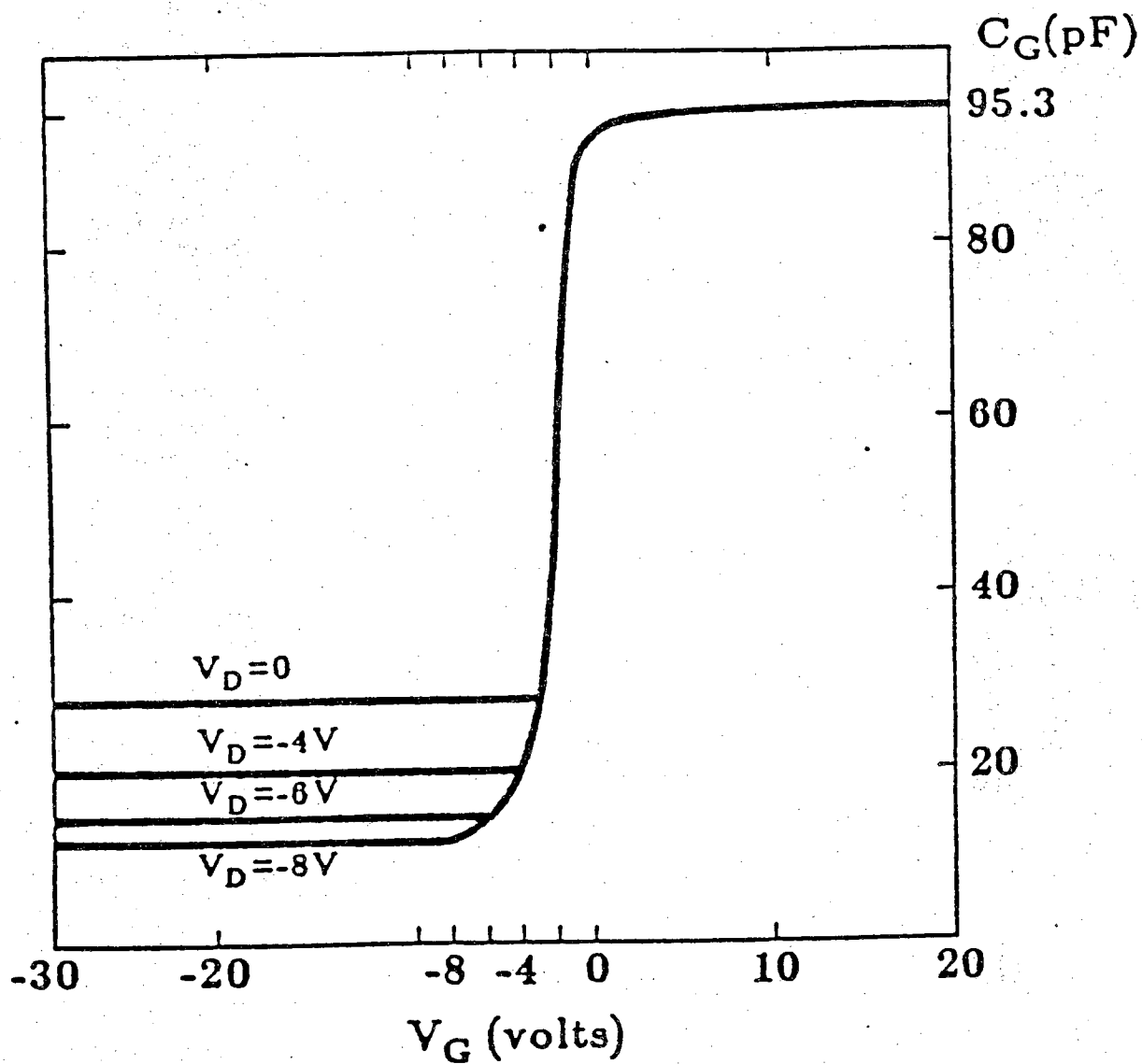


Fig. 4.10 Sample equilibrium and steady-state deep depletion C-V characteristics.

## CHAPTER 5

### AN MOS-C PHOTO/SWEEP TECHNIQUE FOR DETERMINING $\tau_r$

One of the prime objectives of the research work was to determine the carrier recombination lifetime  $\tau_r$  in silicon solar cell substrates. In this chapter we describe and demonstrate a new measurement method — an MOS-C photo/sweep technique — for extracting the cited parameter. The measurement procedures are based on the increase in inversion capacitance  $C_F'$  in response to a set of illumination and linear sweep voltages. Relative to other MOS techniques, the measurement method is simple, accurate, and allows one to determine  $\tau_r$  under room temperature conditions. Basically, the MOS-C is operated under "forward-biased" conditions —  $C_F'$  is related to the applied voltage; illumination and voltage sweep are related to the current. As discussed in Chapter 2, the recombination lifetime can be deduced from the diffusion-dominated current at large forward biases.

In what follows we consider the effects of a linear voltage sweep, illumination, and a combination of photo/sweep on the MOS-C. The description of the voltage sweep and illumination effects serve as intermediate steps in understanding ultimately the adopted photo/sweep technique. A quantitative analysis of the measurement for determining  $\tau_r$  is then detailed. In the analysis we establish how  $C_F'$  is related to  $V_e$ ;  $V_e$  is the effective voltage developed across the MOS-C (which is equivalent to the forward-biased voltage across a PN junction diode) and is a central variable in computing  $\tau_r$ . Finally, experimental results are presented to demonstrate use of the technique.

To avoid confusion in the subsequent discussion we would like to emphasize the following points:

1. For an n-bulk substrate (on which measurements were performed), holes are of course the minority carriers whereas electron are the majority carriers. As established in Chapter 2, the recombination lifetime  $\tau_r$  in an n-type material is equivalent

to the minority carrier hole lifetime  $\tau_p$ ; hence the terms  $\tau_r$  and  $\tau_p$  are used interchangeably.

2. To simplify theoretical relationships, we have adopted the usage of  $U_e$ , where  $U_e \equiv \frac{V_e}{kT/q}$ .  $U_e$  is simply the effective voltage developed across the semiconductor component of the MOS-C normalized to  $kT/q$ .  $U_e$  is of course dimensionless.

## 5.1 Measurement Theory

### 5.1.1 The Forward-Sweep Method

We herein define *forward sweep* to be an applied voltage ramp which linearly varies the gate voltage from inversion toward accumulation conditions. Accordingly, when the gate voltage is swept from accumulation to inversion conditions, it is referred to as a reverse sweep. The following qualitative description of the MOS-C response to an applied forward voltage sweep closely parallels the well-established "linear sweep" response [43] where a reverse sweep is employed.

Picture an n-bulk MOS-C which is initially biased under equilibrium inversion conditions. The inversion capacitance is  $C_F$ . Next, suppose the MOS-C is forward-swept by varying the gate voltage  $V_G$  at a constant ramp rate  $R$  ( $R = dV_G/dt$ ). During the initial stages of the sweep, the depletion region progressively shortens as the semiconductor reacts to offset the charges being removed from the MOS-C gate. As depicted in Fig. 5.1(a), a decrease in the depletion region in turn increases the inversion capacitance. At the same time, an excess of minority carrier holes is created inside the near-Si-surface inversion layer. Responding to the excess, these carriers are injected into the depletion region and the adjacent quasi-neutral region where they subsequently recombine (see Fig. 5.1(b)). After a short period of time the recombination rate within the semiconductor becomes sufficiently large so as to precisely balance the rate at which charge is being removed from the gate. Under this dynamic steady-state condition the new observed inversion capacitance is  $C'_F$ . The charge removed from the gate per unit area per second is  $C_o R$ , which is equal to the magnitude of the injected current  $J_{\text{SWEEP}}$  inside the semiconductor;  $C_o$  is the oxide capacitance per unit area. The injection

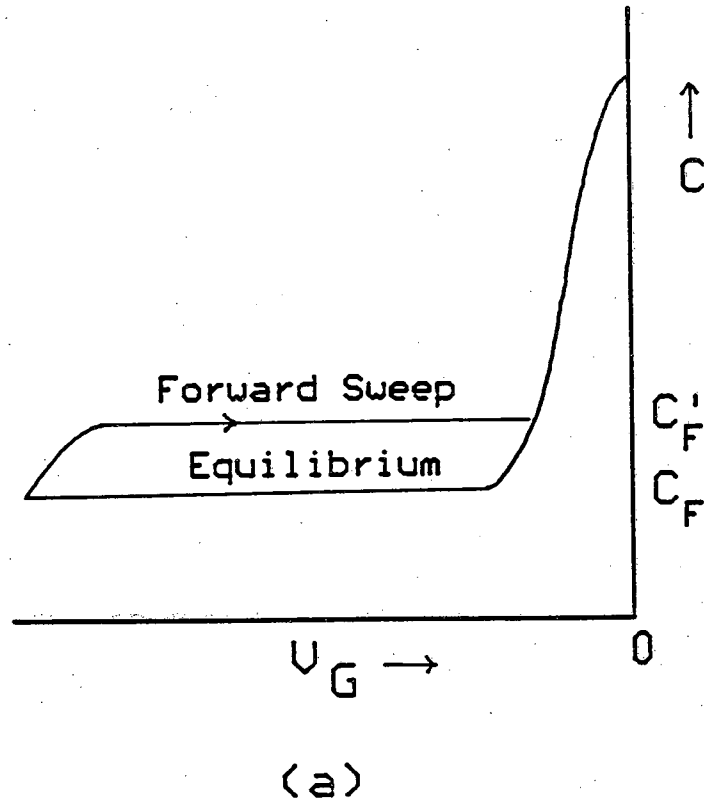


Fig. 5.1 (a) Effect of forward-sweeping on the inversion capacitance. The applied voltage sweep causes the equilibrium inversion capacitance  $C_F$  increase to a dynamic steady-state value,  $C'_F$ . (b) Carrier injection due to forward-sweeping and subsequent carrier recombination inside the MOS-C.

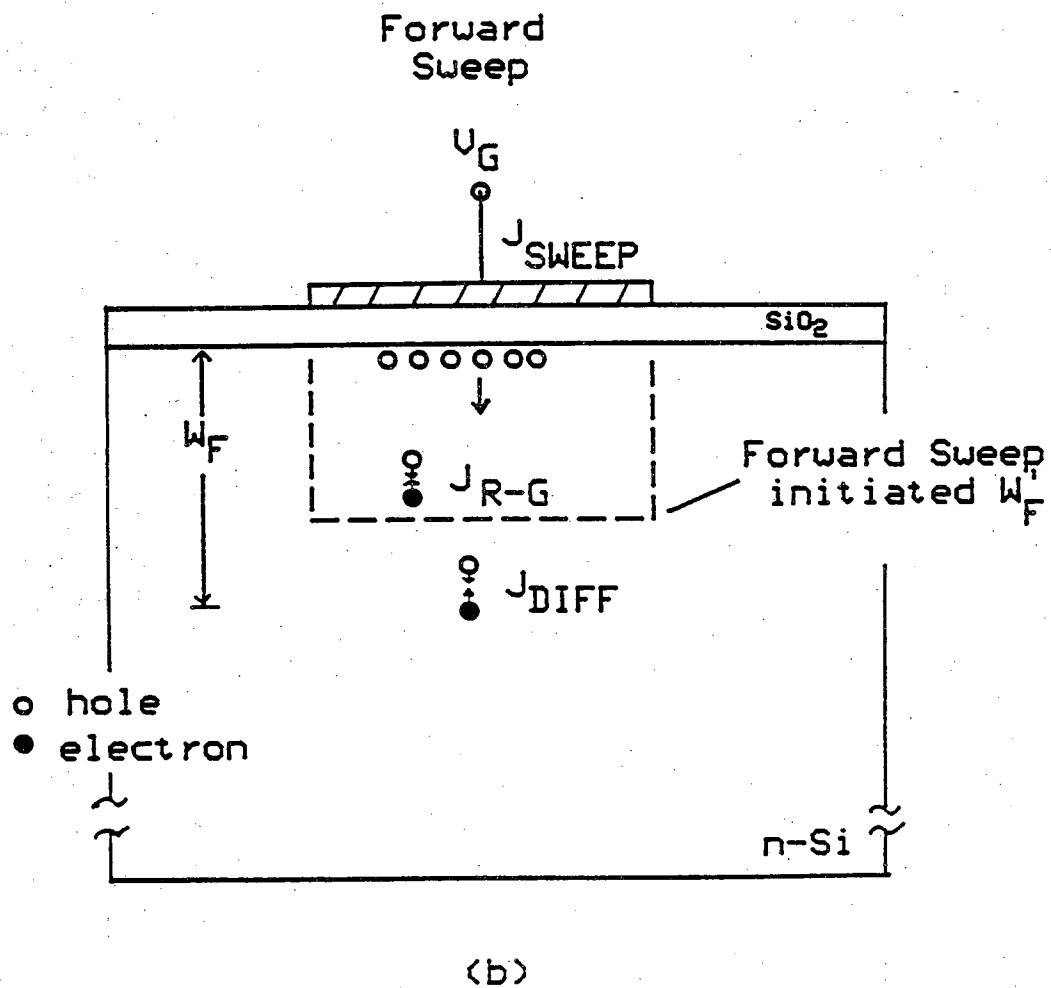


Fig. 5.1 Continued.

current is in turn balanced by the recombination currents in the depletion region,  $J_{R-G}$ , and also in the quasi-neutral region,  $J_{DIFF}$ .

The energy band diagrams under equilibrium and dynamic steady-state conditions are depicted in Figs. 5.2(a) and 5.2(b), respectively. Note from Fig. 5.2(b) that there is a separation of quasi-Fermi levels ( $F_N$  for electrons and  $F_P$  for holes) near the interface. Under low-level injection conditions  $F_N = E_F$ , where  $E_F$  is the equilibrium Fermi-level for the majority carrier electrons. The difference between the two quasi-Fermi levels divided by  $kT$  is identified as the normalized effective voltage  $U_e$ , which is functionally equivalent to the applied voltage  $V_A$  across a PN junction diode. As will be summarized in Subsection 5.1.5, and as detailed in Appendix C, the  $U_e$  value is readily deduced from the observed steady-state capacitance  $C_F'$ .

From the foregoing qualitative analysis it should be obvious that a plot of  $R$  vs  $U_e$  should display an "I-V" characteristic which is similar to that of a forward-biased PN junction diode. In principle, one could systematically increase the sweep rate  $R$ , until the  $R$  vs  $U_e$  plot enters a diffusion-current-dominated regime. From the slope of the plot in this regime one could then extract the minority carrier lifetime. Practically speaking, however, one can only perform ramp-type forward-sweep measurements for a limited range of sweep rates (typically,  $< 30$  V/sec). High sweep rates cannot be conveniently utilized for the measurement. For instance, if an n-bulk MOS-C initially biased at  $-30$  V and exhibiting a negative flat band voltage is forward-swept at  $R=30$  V/sec, the allowable time for measuring  $C_F'$  is less than 1 second. Note that the forward sweep measurement is one-shot in nature — the MOS-C has to be biased back to the initial inversion conditions and allowed to equilibrate before additional forward sweep measurements can be performed. Depending on the value of the carrier lifetime for a given MOS-C, the  $R-U_e$  plot constructed from forward sweep data (where  $R < 30$  V/sec) may or may not display a strong diffusion-dominated regime. Typically, higher sweep rates are required for achieving the desired plot. This led to the use of illumination to achieve the required forward-biased ( $U_e$ ) values.

### 5.1.2 The Illumination Method

Compared to the forward sweep approach, illumination can readily induce a larger effective voltage. Consequently, illumination can be used as a

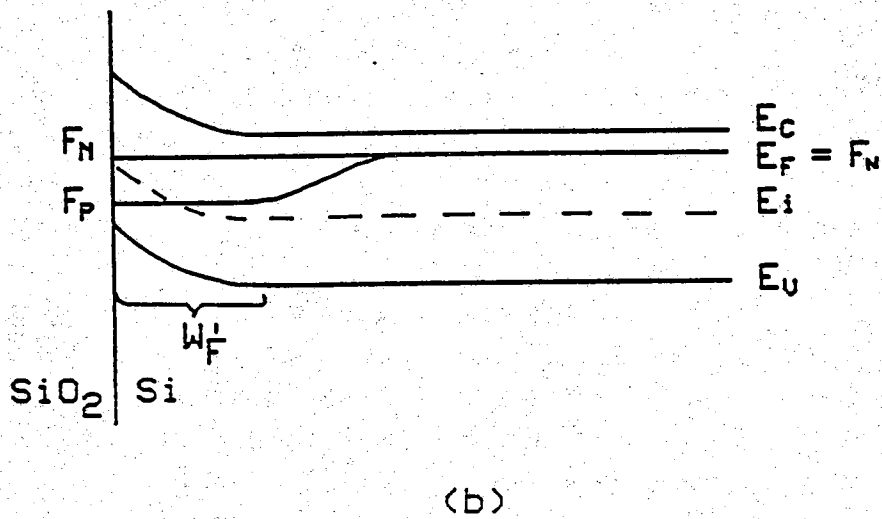
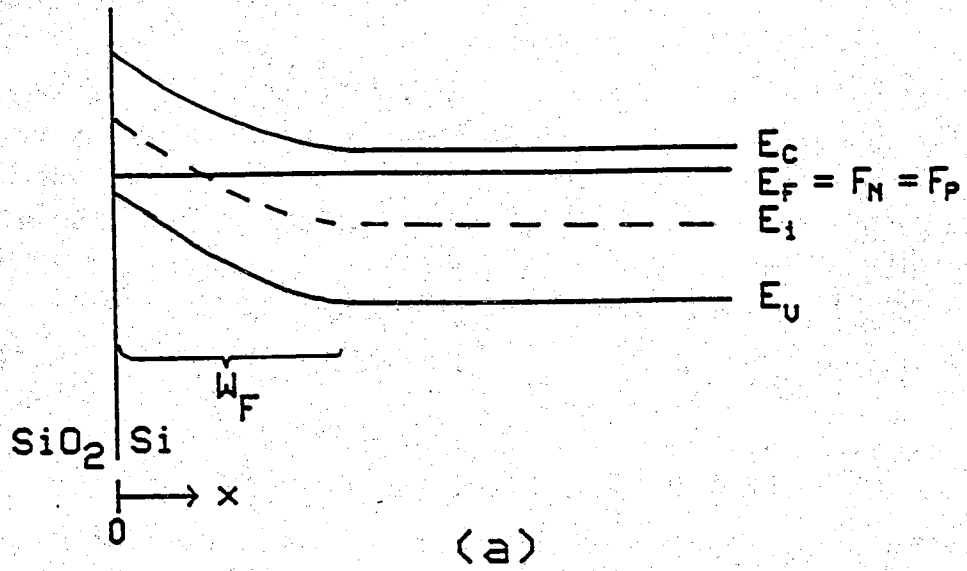


Fig. 5.2

(a) Equilibrium and (b) steady-state energy band diagrams under inversion conditions. Note that  $W_F > W'_F$ ;  $W_F$  and  $W'_F$  are the depletion widths corresponding to  $C_F$  and  $C'_F$ , respectively;  $F_P$  and  $F_N$  are the quasi-Fermi levels for holes and electrons, respectively.



tool to simulate large sweep rates.

When the MOS-C is exposed to illumination, the photogenerated minority carrier holes are first collected under the gate and then injected into the bulk of the MOS-C. Once the carrier injection is initiated, the subsequent response of the depletion region and the corresponding inversion capacitance are the same as that described in the forward sweep method. The resulting injection current is denoted as  $J_{\text{PHOTO}}$ , indicating that the current is initiated by illumination alone.  $J_{\text{PHOTO}}$ , in general, is very difficult to accurately relate to first principle parameters such as light intensity and the absorption coefficient. However, since it has the same effect as a forward sweep, it is logical to introduce an effective sweep rate  $R^*$ , where  $J_{\text{PHOTO}} \equiv C_o R^*$ .  $R^*$ , of course, has to be calibrated for a given illumination intensity.

One calibration method would be to compare  $C'_F$  produced by known forward-sweep rates and by known levels of low-intensity illumination. The same value of  $C'_F$  obtained independently by the forward-sweep and the illumination implies  $R^* = R$ . A plot of the illumination levels versus  $R^*$  (hopefully linear) could then be constructed. For values beyond that accessible to forward sweeping,  $R^*$  could be deduced from an extrapolation of the linear calibration plot. The cited calibration approach was indeed implemented and sample results will be discussed in Section 5.2. The calibration, however, proved quite difficult and inconvenient;  $R^*$  depends on parameters such as the distance between the source and the device. Practically speaking, one must obtain a calibration plot prior to each lifetime measurement. The photo/sweep method, described next, was developed to circumvent the uncertainty associated with the photo-calibration while still providing the advantages of illumination.

### 5.1.3 The Photo/Sweep Method

Having established the conceptual foundations for the forward sweep and illumination methods, it is not difficult to understand the underlying measurement concept of the photo/sweep approach. As the name implied, the measurement involves a combination of illumination and forward sweep. The basic idea is to strongly illuminate the MOS-C so that the recombination current is diffusion-dominated. Let the corresponding illumination-only injection current, capacitance, and effective voltage be  $C_o R^*$ ,  $C'_{F1}$ , and  $U_{e1}$  respectively. The subscript 1 denotes that the response is due only to the

illumination. Since the photocurrent is diffusion-dominated one can write  $J_{\text{INJECTION}} = J_{\text{PHOTO}} = C_0 R^* \propto \exp(U_{e1})$ . As discussed previously, the carrier lifetime parameter is contained in the proportionality constant. Next a forward sweep of sweep rate  $R$  is applied to the MOS-C under the same illumination conditions. This will cause an additional, though small, increase in capacitance. Assuming  $R$  does not perturb  $R^*$ , one can express the total injection current, capacitance, and effective voltage as  $C_0(R+R^*)$ ,  $C'_{F2}$  and  $U_{e2}$ , respectively. The subscript 2 denotes that the response is caused by both the forward sweep and illumination. Here  $J_{\text{INJECTION}} = C_0(R+R^*) \propto \exp(U_{e2})$ . Subtracting the corresponding injection currents yields  $C_0 R \propto \exp(U_{e2}) - \exp(U_{e1})$ . Hence the minority carrier lifetime can readily be extracted without determining  $R^*$ . It should be pointed out that the method does require an accurate determination of the small increase in capacitance resulting from  $R$ . The implementation of the photo/sweep method is detailed in Section 5.2.

#### 5.1.4 Quantitative Analysis

There are a number of basic assumptions underlying the analysis : (1) We assume a spatially uniform distribution of R-G centers in the MOS-C depletion region and in the adjacent quasi-neutral bulk. (2) The same R-G center is assumed to dominate in both the depletion region and in the quasi-neutral bulk under all experimental conditions. (3) Recombination at the interfacial traps under the gated MOS-C surface is taken to be negligible under inversion conditions. (4) It is assumed the periphery to gate area ratio has been made sufficiently small so that lateral surface effects are negligible. (5) The quasi-neutral bulk width,  $d$ , is taken to be greater than the minority carrier diffusion length  $L_p$ . (To first order,  $d$  is the same as the wafer thickness.)

Under experimental conditions where a steady-state or dynamic steady-state condition has been established, one can write

$$J_{\text{INJECTION}} = J_{\text{RECOMBINATION}} \quad (5.1)$$

or

$$J_{\text{SWEEP}} + J_{\text{PHOTO}} = J_{\text{R-G}} + J_{\text{DIFF}} \quad (5.2)$$

where

$$J_{\text{SWEEP}} = C_o R \quad (5.3)$$

and

$$J_{\text{PHOTO}} = C_o R^* \quad (5.4)$$

The recombination current  $J_{\text{R-G}}$  in the depletion region is related to the lifetime by (refer to Appendix B)

$$J_{\text{R-G}} = q \left( \frac{n_i}{\tau_g} \right) W_R \quad (5.5)$$

where

$$W_R = \gamma L_D \left( e^{U_c} - 1 \right) \quad (5.6)$$

$$\gamma = \hat{U}_S \int_0^{U_S} \frac{dU}{\left[ 1 + \frac{\tau_p}{\tau_g} e^{U-U_F} + \frac{\tau_n}{\tau_g} e^{U_F+U_c-U} \right] F(U, U_F, U_c)} \quad (5.7)$$

$$F(U, U_F, U_c) = \left[ e^{U_F+U_c} \left( e^{-U+U-1} \right) + e^{-U_c} \left( e^{U-U-1} \right) \right]^{\frac{1}{2}} \quad (5.8)$$

$$L_D = \left[ \frac{K_S \epsilon_o kT}{2q^2 n_i} \right]^{\frac{1}{2}} \quad (5.9)$$

$$U_F = -\ln \left( \frac{N_D}{n_i} \right) \quad (5.10)$$

$$\begin{aligned} U_e &\equiv (F_N - F_P)/kT \\ &\equiv \frac{V_e}{kT/q} \end{aligned} \quad (5.11)$$

$W_R$  is the effective recombination width inside the electrostatic depletion region,  $F$  is the normalized dimensionless electric field,  $L_D$  is the intrinsic Debye length,  $U_F$  is the normalized doping parameter,  $U$  is the normalized potential, and  $U_S$  is the normalized surface potential at the interface;  $\hat{U}_S = \pm 1$  if  $U_S \gtrless 0$ .

Analogous to the diffusion current in the PN junction analysis, one can write  $J_{DIFF}$  as [85]

$$J_{DIFF} = q \frac{D_P}{L_P'} \frac{n_i^2}{N_D} \left( e^{U_e} - 1 \right) \quad (5.12)$$

where

$$L_P' = L_P \left( \frac{1 + \beta e^{-2d/L_P}}{1 - \beta e^{-2d/L_P}} \right) \quad (5.13)$$

$$\beta = \frac{1 - s_B L_P / D_P}{1 + s_B L_P / D_P} \quad (5.14)$$

$$L_P = \sqrt{D_P \tau_p} \quad (5.15)$$

$s_B$  is the surface recombination velocity at the back of the MOS-C.  $L_P'$  is an effective diffusion length and  $D_P$  is the hole diffusion constant.

One can readily deduce from Eq. (5.12) that it is  $L_P'$  (not  $L_P$ ) which one actually determines from the diffusion current characteristics. However, if  $d \geq L_P'$ , then  $L_P$  is approximately equal to  $L_P'$ , and  $\tau_p$  can readily be determined using Eq. (5.15). The foregoing assertion is confirmed in Fig. 5.3 employing Eq. (5.13). On the other hand, if  $L_P' > d$ , one cannot determine the true  $\tau_p$  parameter without knowing  $s_B$ .

Invoking assumption #5, i.e., assuming  $d \gg L_P$ , the bracket in Eq. (5.13) approaches unity and Eq. (5.12) becomes

$$J_{\text{DIFF}} \simeq q \frac{D_P}{L_P} \frac{n_i^2}{N_D} \left( e^{U_e} - 1 \right) \quad (5.16)$$

Eq. (5.16) is of course the textbook result for the diffusion current flowing through a PN junction diode. As noted previously,  $\tau_p$  enters the  $J_{\text{DIFF}}$  term through  $L_P$  (see Eq. (5.15)).

Substituting Eqs. (5.3), (5.4), (5.5) and (5.16) into Eq. (5.2) yields

$$C_o(R+R^*) = \underbrace{\frac{qn_i}{\tau_g} W_R}_{J_{R-G}} + q \underbrace{\left( \frac{D_P}{\tau_p} \right)^{\frac{1}{2}} \frac{n_i^2}{N_D} \left( e^{U_e} - 1 \right)}_{J_{\text{DIFF}}} \quad (5.17)$$

Eq. (5.17) is the general "current-voltage" relationship describing the response of the MOS-C under forward sweep and illumination conditions. A sample theoretical  $R+R^*$  versus  $U_e$  plot based on Eq. (5.17) is shown in Fig. 5.4.

In applying the photo/sweep method to extract  $\tau_p$ , one creates experimental conditions such that  $J_{R-G}$  is negligible compared to  $J_{\text{DIFF}}$ . With  $J_{\text{DIFF}} \gg J_{R-G}$  it follows from the discussion in Subsection 5.1.3 and Eq. (5.17) that

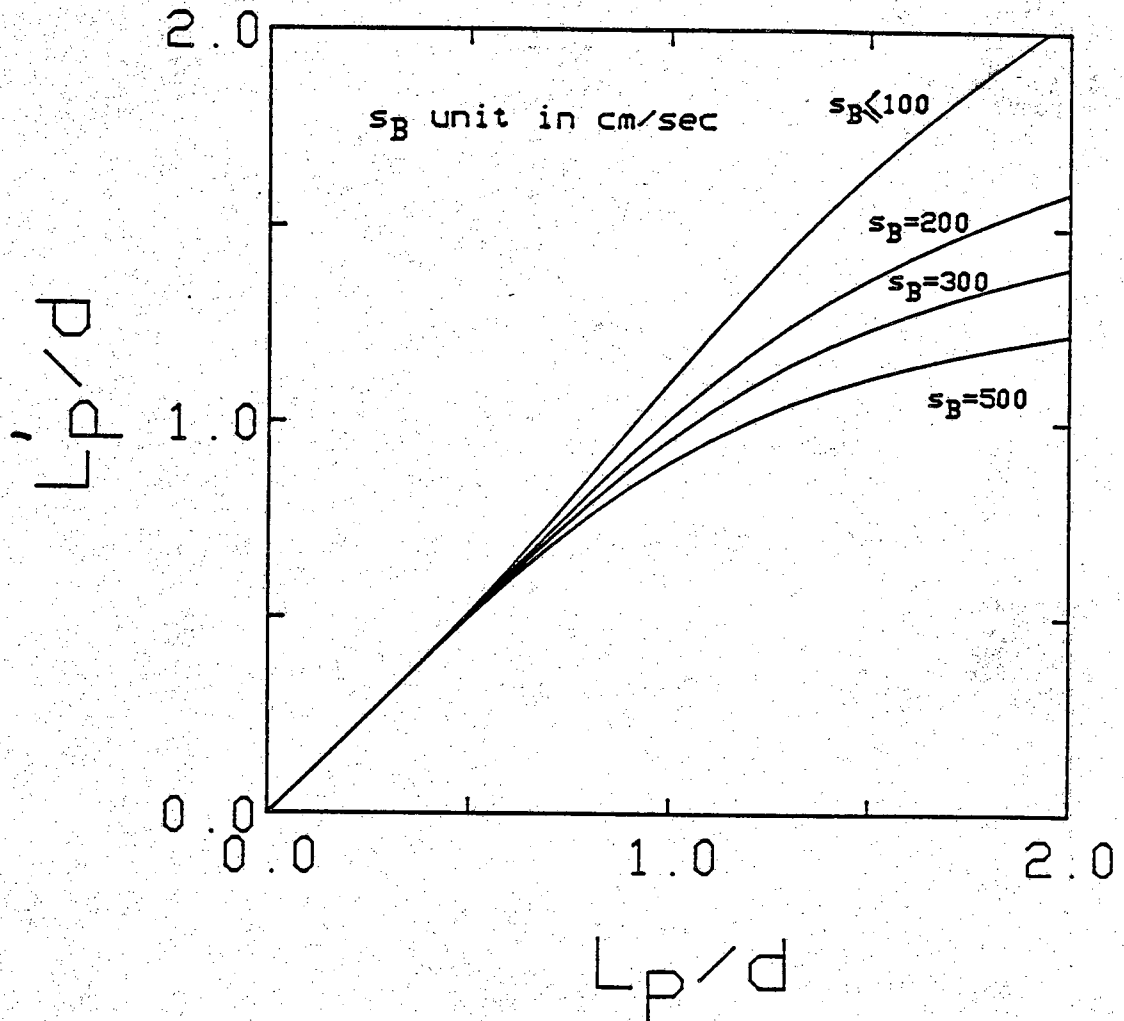


Fig. 5.3 Plot of  $L'_P/d$  versus  $L_P/d$  for various  $s_B$ . ( $d = 0.055$  cm;  $T = 296$  K;  $N_D = 2 \times 10^{15}$  cm $^{-3}$ ;  $D_P = 11.6$  cm $^2$ /sec.)

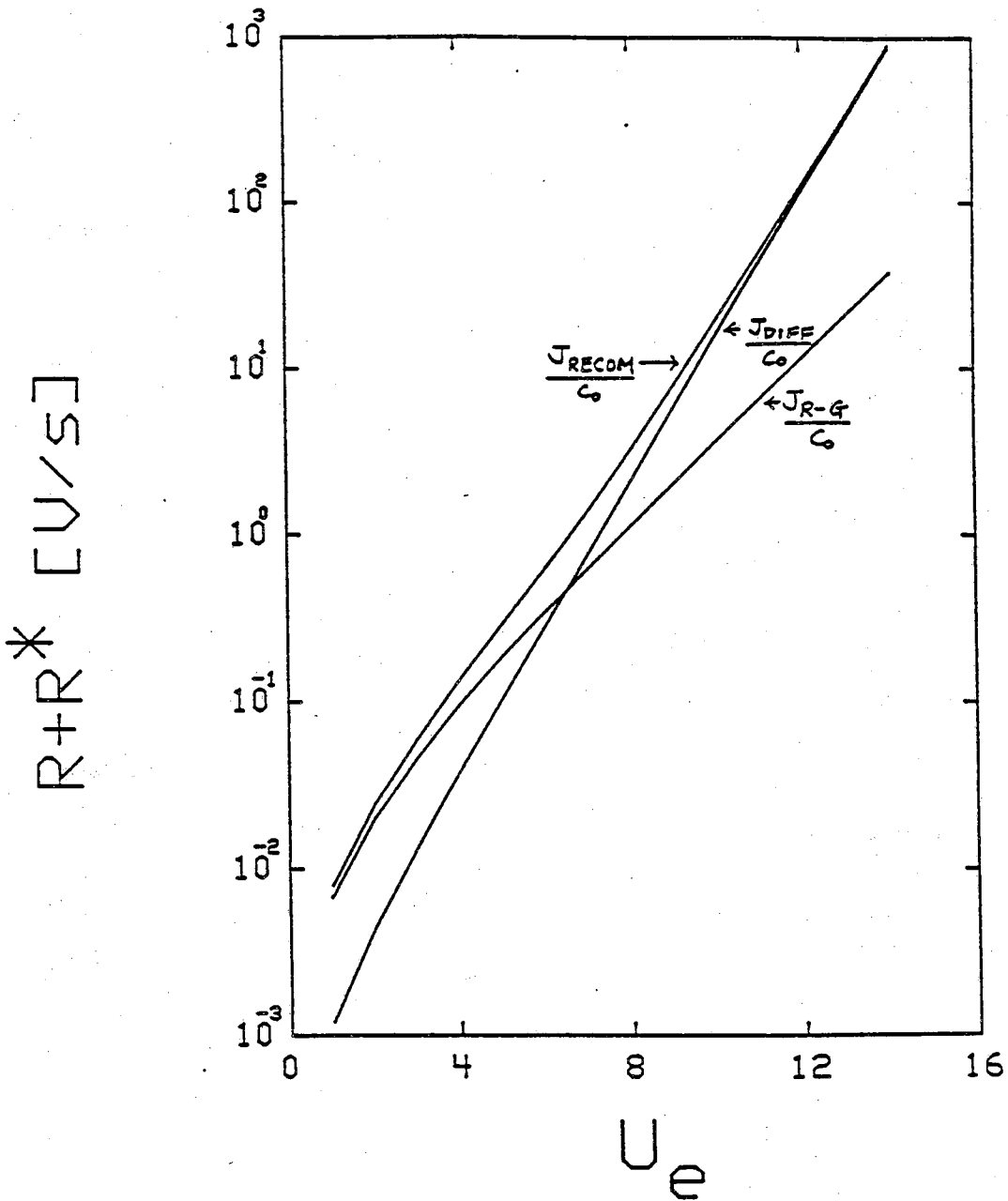


Fig. 5.4

Sample  $R+R^*$  versus  $U_e$  plot using

$C_O = 86$  pF,  $C_F = 25$  pF,  $x_o = 0.1$   $\mu\text{m}$ ,

$N_D = 1.68 \times 10^{15}$   $\text{cm}^{-3}$ ,  $A_G = 2.5 \times 10^{-3}$   $\text{cm}^2$ ,  $T = 295\text{K}$ ,

$\tau_g = 100$   $\mu\text{sec}$ ,  $\tau_p = 1$   $\mu\text{sec}$  and  $\tau_n = 99$   $\mu\text{sec}$ .

$$C_o R = q \left( \frac{D_p}{\tau_p} \right)^{\frac{1}{2}} \frac{n_i^2}{N_D} \left( e^{U_{e2}} - e^{U_{e1}} \right) \quad (5.18)$$

Both  $U_{e2}$  and  $U_{e1}$  are deduced from the corresponding inversion capacitance  $C'_{F2}$  (due to photo/sweep) and  $C'_{F1}$  (due to photo-only). Since  $R$  is also a known quantity,  $\tau_p$  can be readily deduced from Eq. (5.18).

### 5.1.5 Relating $C'_F$ And $U_e$

To compute the lifetime parameter from the sweep-capacitance data, one must first deduce the effective normalized voltage  $U_e$  from the capacitance  $C'_F$ . As detailed in Appendix C, the  $C'_F - U_e$  relationship is essentially derived from extending the high frequency exact C-V analysis [86] from equilibrium to steady-state conditions. Referring back to Fig. 5.2, one notes that the quasi-Fermi level for holes ( $F_p$ ) and the quasi-Fermi level for electrons ( $F_n$ ) are the same under equilibrium conditions, i.e.,  $F_p = F_n = E_F$ . Under steady-state conditions, the quasi-Fermi level for the minority carrier holes is displaced from  $E_F$  across the depletion region. In addition, since the minority carrier hole concentration in the quasi-neutral bulk is negligible compared to the majority carrier electron concentration under low-level injection conditions, one can further assume  $F_p$  in the quasi-neutral bulk to be the same as that in the depletion region in the exact C-V analysis without introducing a significant error. In doing so, we obtain the following set of control equations relating  $C'_F$  and  $U_e$ .

$$C'_F = \frac{C_o}{1 + (W'_F/x_o)} \quad (5.19)$$

$$W'_F = -L_D \left[ \frac{2F(U_s, U_F, U_p)}{e^{U_F}(1 - e^{-U_s})/(1 + \Delta) + e^{-U_F}(e^{U_s} - 1)} \right] \quad (5.20)$$



$$\Delta = \frac{(e^{-U_s} + U_s - 1)/F(U_s, U_F, U_P)}{\int_0^{U_s} \frac{e^{-U_F}(e^U - 1)(e^{-U} + U - 1)}{2F^3(U, U_F, U_P)} dU} \quad (5.21)$$

$$V_G' = \frac{kT}{q} U_s + \hat{U}_s \frac{x_o'}{L_D} F(U_s, U_F, U_P) \quad (5.22)$$

$$U_P = \ln \left[ \frac{\left[ \frac{[V_G'/(kT/q)] - U_s}{x_o'/L_D} \right]^2 - e^{-U_F}(e^{U_s} - U_s - 1)}{e^{-U_s} + U_s - 1} \right] \quad (5.23)$$

with

$$U_P = U_F + U_e \quad (5.24)$$

$U_F$  is the normalized doping parameter,  $U_P$  is the normalized quasi-Fermi level for holes,  $U_s$  is the normalized dc surface potential. Using iteration methods, one can generate a  $C_F'$  versus  $U_e$  lookup table. Sample  $C_F' - U_e$  data is listed in Table 5.1. Finally, it should be noted that there is a slight dependence of  $C_F' - U_e$  relationship on  $V_G'$ . However, the dependence is typically negligible.

## 5.2 Experimental Results

The MOS-C's employed for the measurements were fabricated on wafers M14, D2 and D514. Both M14 and D2 were wafer quadrants scribed from low defect 4" (100) float-zone refined silicon which was 0.055 cm thick. Sample D514 was a lower quality 2" wafer used for comparison purposes and was 0.0255 cm thick. MOS-C physical characteristics and the device processing history were recorded in Chapter 3. It should be noted that a large MOS-C gate area ( $A_G = 0.03675 \text{ cm}^2$ ) was chosen to minimize the lateral surface effect and also permits more detectable (hence more accurate) changes in

**Table 5.1** Sample  $C'_F-U_e$  Data with  $V'_G = -25$  volts;  $\delta C = C'_F - C_F$ .  
 ( $C_O = 86$  pF;  $C_F = 25$  pF;  $x_o = 0.1$   $\mu\text{m}$ ;  
 $N_D = 1.68 \times 10^{15}$   $\text{cm}^{-3}$ ;  $A_G = 2.5 \times 10^{-3}$   $\text{cm}^2$ ;  $T = 295\text{K}$ ;  
 $\tau_g = 100$   $\mu\text{sec}$ ;  $\tau_p = 1$   $\mu\text{sec}$  and  $\tau_n = 99$   $\mu\text{sec}$ . The  
 parameter values are the same as those used for Fig. 5.4.)

$\delta C$ [pF]	$U_e$
0.3847	1.00
0.7491	2.00
1.1552	3.00
1.5854	4.01
2.0424	5.01
2.5295	6.01
3.0505	7.01
3.6101	8.02
4.2141	9.02
4.8696	10.02
5.5857	11.02
6.3741	12.02
7.2508	13.03
8.2370	14.03

capacitance.

The measurement set-up of the photo/sweep method was given in Chapter 3. Specifically, the photo/sweep method is implemented by using a periodic *saw-tooth waveform* to generate the forward sweep. There are several advantages to this implementation. First, different sweep voltages can be achieved by simply adjusting the period and amplitude of the waveform. Second, since the sweep rate is periodic (and since lost carriers are rapidly replaced by the strong illumination), the measurement, instead of being one shot in nature as in the original forward sweep method, is continuously repeatable. As a result, electrical noise in the capacitance measurement can be minimized by averaging with a signal processor<sup>†</sup>.

Fig. 5.5 systematically illustrates the timing sequence of the measurement. A trigger is used for signal synchronization purposes. Prior to triggering the sawtooth waveform,  $C = C'_{F1}$ , the steady-state capacitance corresponding to illumination only. Once the sawtooth waveform is triggered, R is applied together with the illumination and the capacitance increases, finally reaching a dynamic steady-state value,  $C'_{F2}$ . With the abrupt termination of the voltage ramp and the return to the baseline bias, the capacitor becomes partially deep-depleted. However, because of the high level of illumination, the capacitor relaxes rapidly back to its original steady-state value. The whole sequence is then repeated with the next synchronous trigger. Also pictured in Fig. 5.5 are two sampling windows inputed to the DLTS signal processor. Note that the signal processor samples the photo-only and photo/sweep capacitances and automatically determine the capacitance difference.

It should be pointed out that a problem can arise concerning the intensity level of the illumination striking the MOS-C. As the photogeneration rate is increased, a point is eventually reached where the minority carriers are able to partially follow the a.c. signal used to measure the capacitance. When this happens the  $C-U_0$  theory (based on the high frequency assumption) is no longer valid. To assure high-frequency operation, we used the the C-t portion of the capacitance response right after the termination of the saw-tooth sweep to sense the onset of low frequency conditions (see Fig. 5.5(c), region 3). If the

<sup>†</sup> It should be mentioned that the signal processor of the DLTS S4600 system employed in the measurement is a specially designed instrument. It can average the input periodic signal; hence minimizing electrical noise and yielding accurate capacitance measurements.

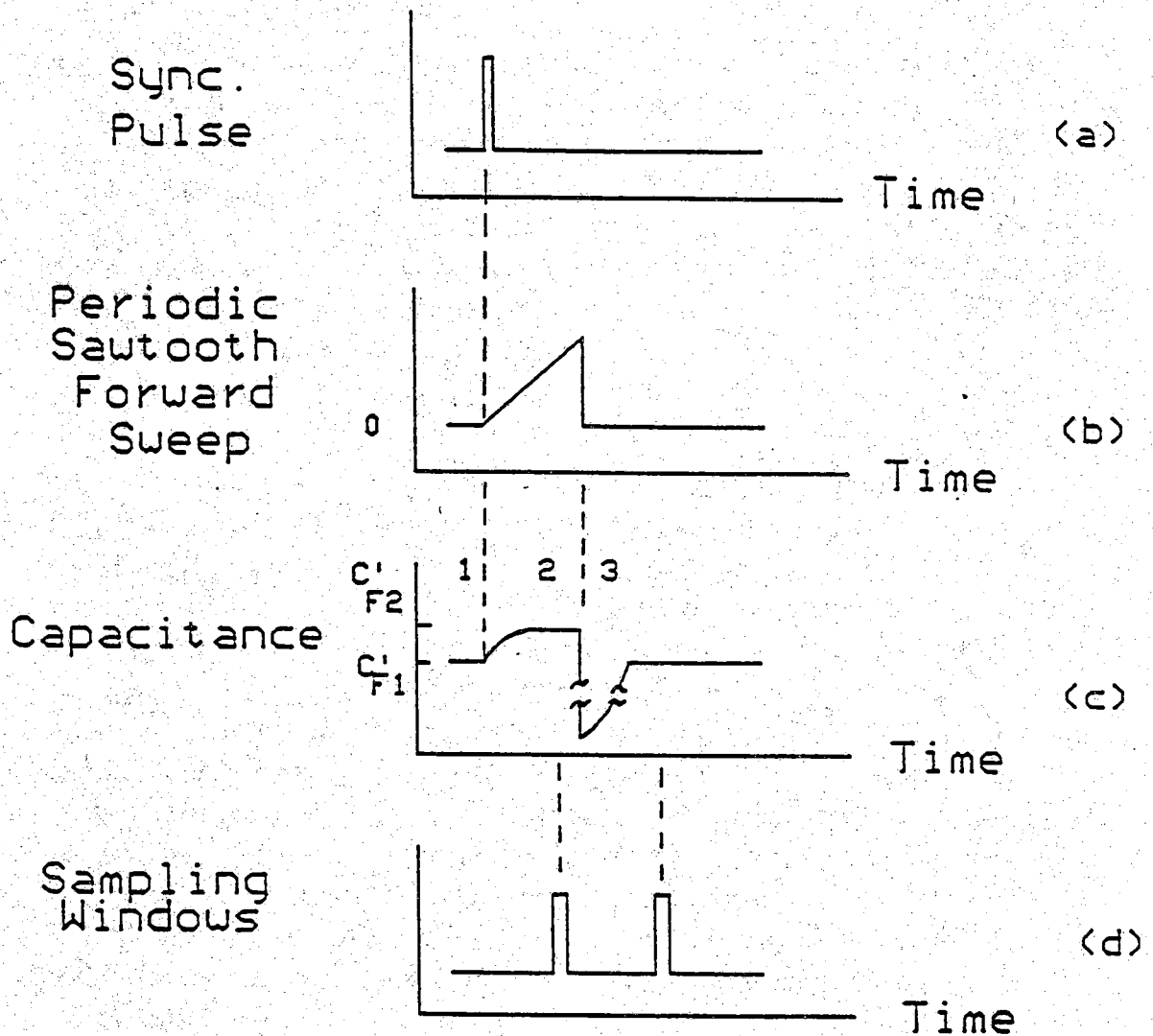


Fig. 5.5 Timing diagrams of the photo/sweep measurements. (a) the trigger pulse used for synchronization purposes; (b) the periodic saw-tooth waveform used to generate the forward sweep; (c) the capacitance response of the MOS-C under photo-only conditions (region 1) and photo/sweep conditions (region 2); region 3 is the illuminated fast C-t transient right after the termination of forward-sweep; (d) the two sampling windows inputted to the DLTS signal processor; the adjustable windows specify the time frames at which capacitance measurements are performed by the signal processor.

storage time to reach equilibrium for the C-t response is  $>100/f_{ac}$ , where  $f_{ac}$  is the small signal test frequency (typically  $f_{ac} = 1\text{MHz}$ ), then we can still assume high frequency conditions prevail. In our measurements, the shortest illuminated C-t transient storage time was about 1 msec. This value is greater than  $100/1\text{MHz}$  and places capacitance data in the high frequency domain.

To obtain a complete  $J_{INJ} = C_o(R+R^*)$  vs  $U_e$  plot, we combined photo/sweep and forward sweep data. The forward sweep data was derived using the MSI-CV system which has a continuously adjustable range of sweep rates varying from 0 to 25 V/sec. Each chosen sweep rate,  $R=dV/dt$ , was accurately determined from sweep voltages recorded periodically as a function of known sampling time using a Keithley 175 DVM. Table 5.2 and Table 5.3 record sample measured and deduced data from the forward sweep and photo/sweep measurements (device M14-1). An  $R+R^*$  vs  $U_e$  plot constructed from the data is shown in Fig. 5.6. Note that the upper portion of the plot is derived from the photo/sweep data while the remainder is constructed from forward sweep data. Using Eq. (5.18) and the data from Table 5.3, the deduced minority carrier diffusion length  $L_p \approx L'_p$  is about 0.031 cm and the corresponding minority carrier lifetime  $\tau_p$  is 84  $\mu\text{sec}$ . Employing Eq. (5.17), a reasonable good theoretical fit to the experimental plot is achieved if one set  $\tau_n \approx 600 \mu\text{sec}$ . It should be noted that  $\tau_g = 700 \mu\text{sec}$  employed in the computations was obtained from a pulsed C-t transient measurement (see Fig. 5.7(a) and 5.7(b)).

Figs. 5.8(a) and 5.8(b) show a second set of pulsed C-t transient and Zerbst plots from wafer M14. The deduced  $\tau_g$  for device M14-2 is 1.08 msec. Accordingly, one would expect  $\tau_p$  to be relatively larger for device M14-2 than device M14-1. This is indeed found to be the case; computations based on the forward-sweep and photo/sweep data yield  $L_p = 0.036$  cm and  $\tau_p = 112 \mu\text{sec}$ . The corresponding  $R+R^*$  vs  $U_e$  plot is presented in Fig. 5.9. Fitting the knee of the experimental plot additionally yields  $\tau_n \approx 900 \mu\text{sec}$ .

One should note that the "I-V" plots derived from device M14-1 and M14-2 exhibit a distinct diffusion-current dominated characteristics. This is not surprising since the  $\tau_g$  parameters for both devices are quite large. The recombination current  $J_{R-G}$  inside the depletion region is expected to be small relative to  $J_{DIFF}$  even at low biases.

It should also be pointed out that the  $\tau_n$  parameter comes into play through  $J_{R-G}$  in Eq. (5.17). However, since both devices M14-1 and M14-2

**Table 5.2** Sample Forward-sweep Data (Derived From Device M14-1;  
 $C_F = 303.8$  pF.)

$R$ [V/s]	$C'_F$ [pF]	$U_e$
0.0024	310.35	1.90
0.005	313.20	2.69
0.010	316.15	3.70
0.028	320.19	4.67
0.038	322.25	5.04
0.067	325.40	5.71
0.140	328.75	6.47
0.280	332.80	7.34
0.607	337.50	8.28
2.790	346.40	9.90
3.470	347.70	10.10
9.020	353.40	11.10

Table 5.3 Sample Photo/Sweep Data (Derived From Device M14-1;  
 $C_F = 303.8 \text{ pF}$ .)

	R [V/s]	$C'_{F2}$ [pF]	$U_{e2}$	$R^*$ [V/s]	$L'_P$ [cm]
Data set #1	10.0	362.280	12.435	22.70	0.031
$C'_{F1} = 359.8 \text{ pF}$	24.0	364.927	12.799	22.36	0.031
$U_{e1} = 12.07$					
Data set #2	9.09	364.5	12.740	34.65	0.031
$C'_{F1} = 362.8 \text{ pF}$	24.0	368.833	13.060	32.50	0.032
$U_{e1} = 12.507$					
Data set #3	9.09	376.233	14.235	177.3	0.032
$C'_{F1} = 375.8 \text{ pF}$					
$U_{e1} = 14.185$					

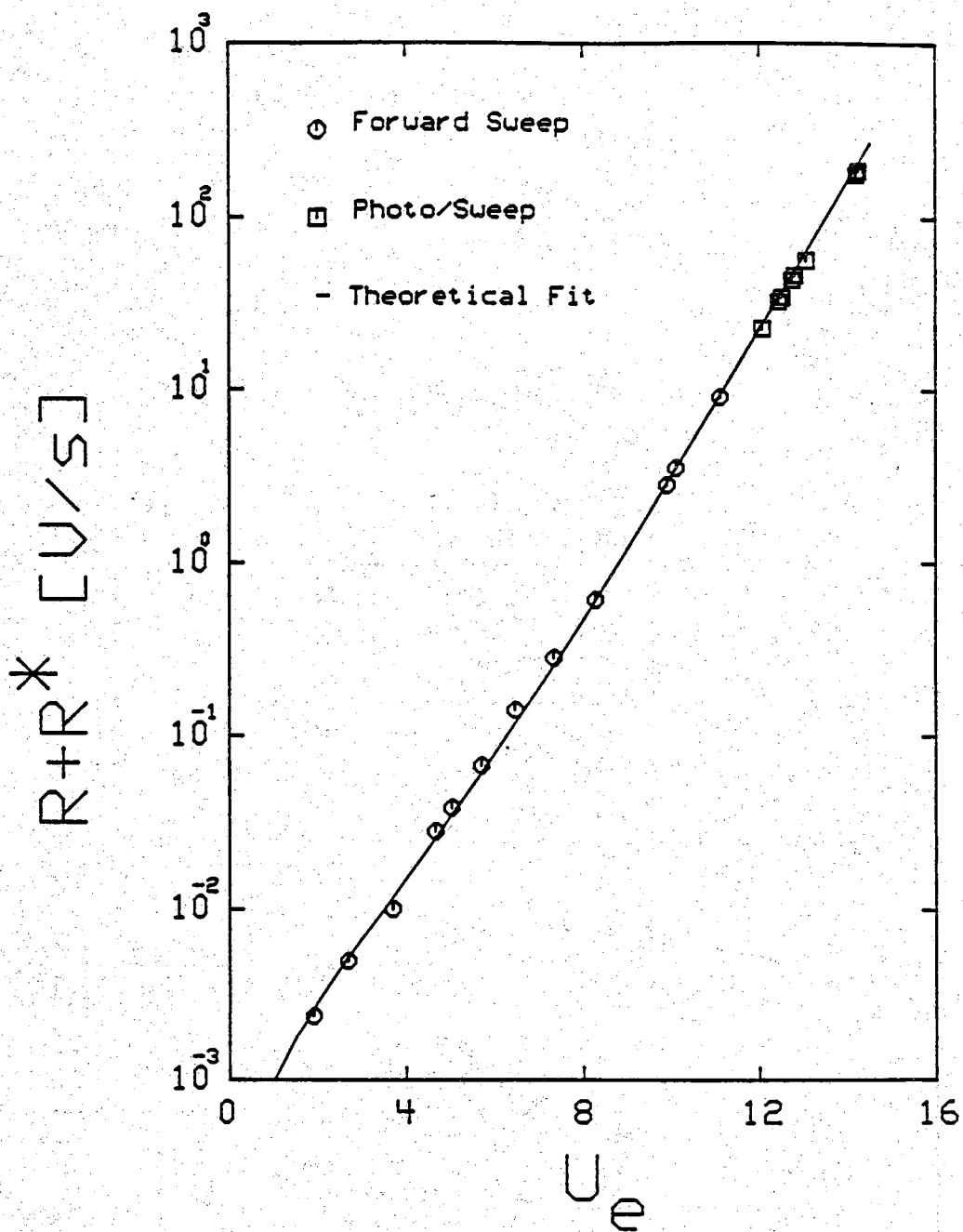


Fig. 5.6

$R+R^*$  vs  $U_e$  plot derived from device M14-1.

( $C_O = 665$  pF;  $C_F = 303.8$  pF,  $x_o = 0.191$   $\mu$ m;  
 $N_D = 1.87 \times 10^{15}$   $\text{cm}^{-3}$ ;  $A_G = 0.03675$   $\text{cm}^2$ ;  $T = 296$ K;  
 $\tau_g = 700$   $\mu$ sec;  $\tau_p = 84$   $\mu$ sec and  $\tau_n \approx 600$   $\mu$ sec.)



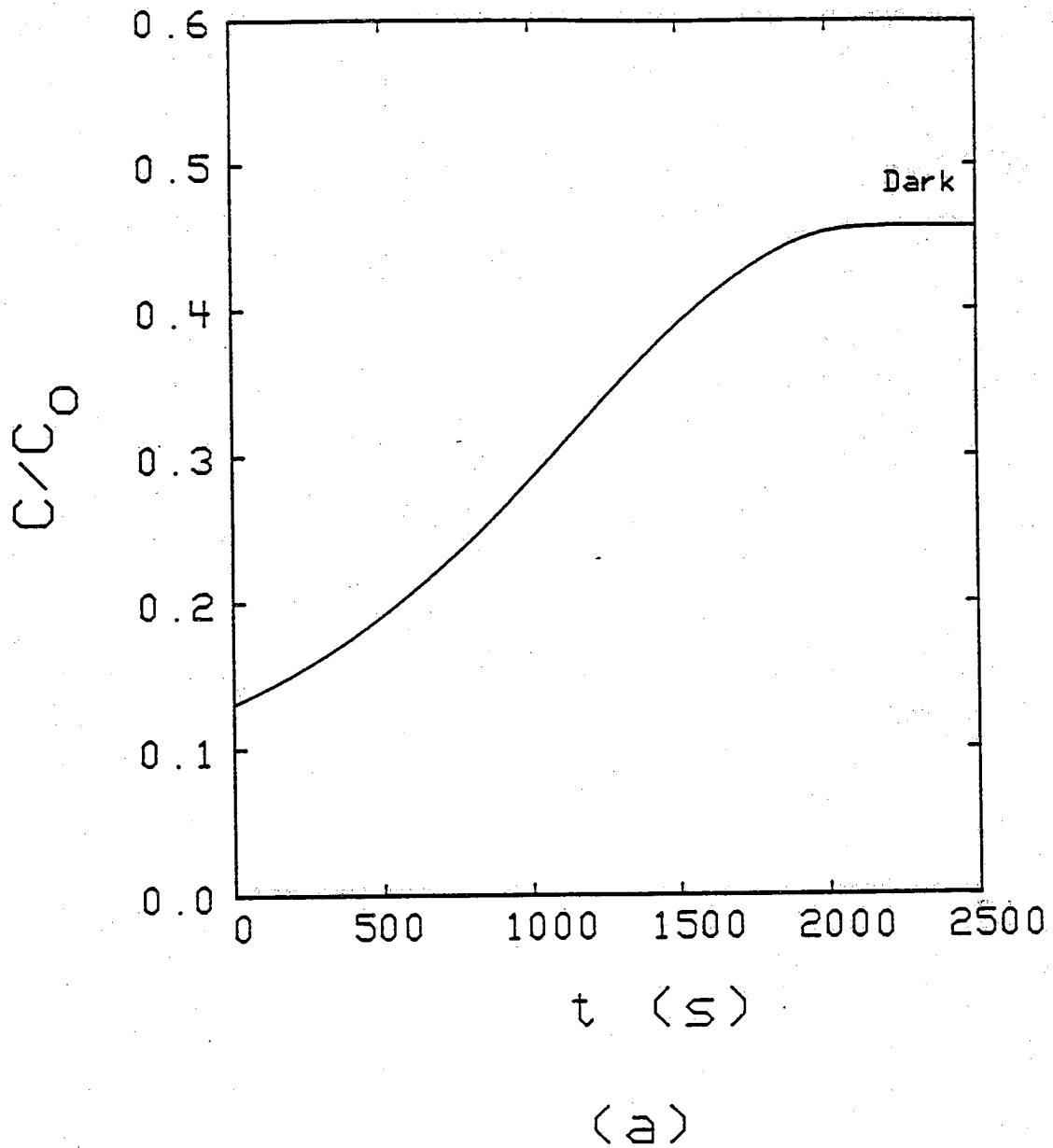


Fig. 5.7 (a) C-t transient of device M14-1 and (b) the corresponding Zerbst plot; deduced  $\tau_g = 700 \mu\text{sec}$ .

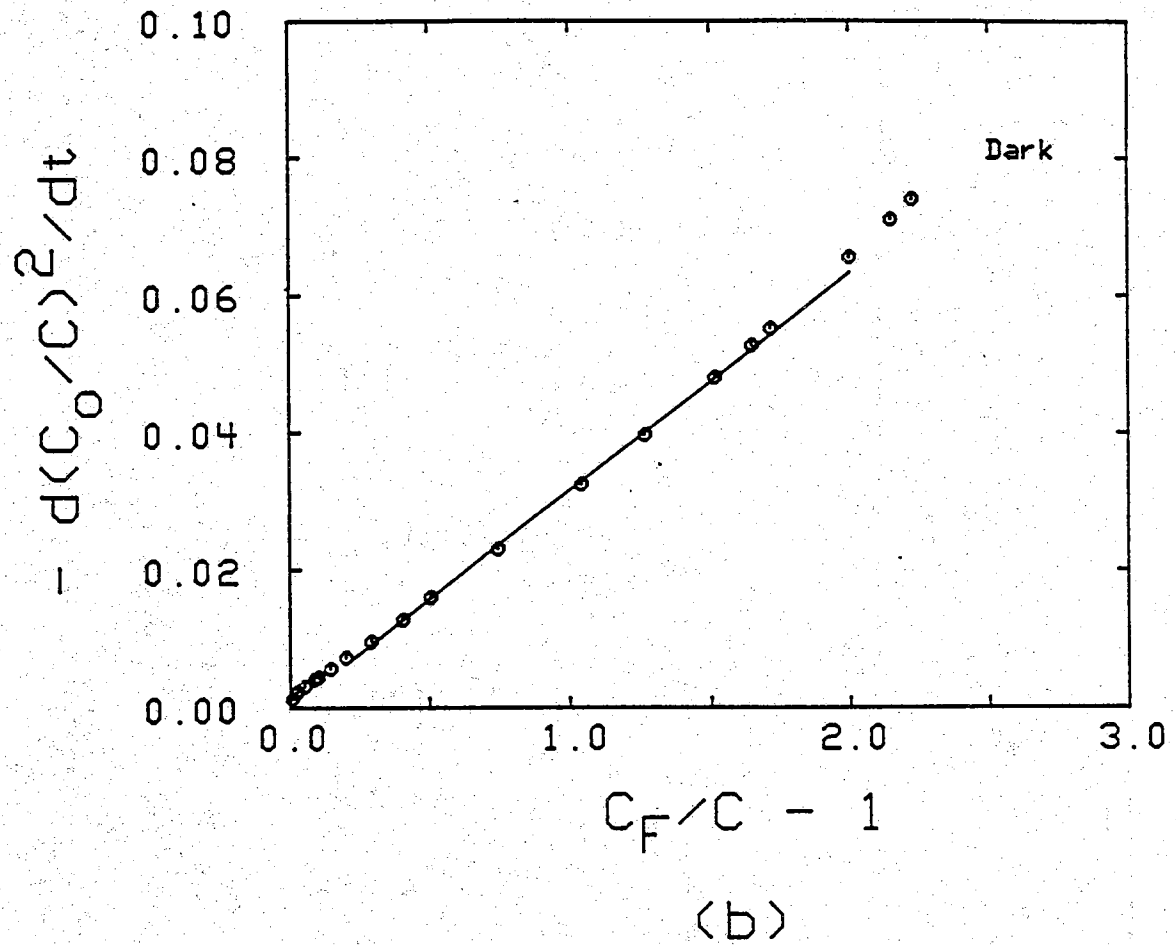


Fig. 5.7 Continued.

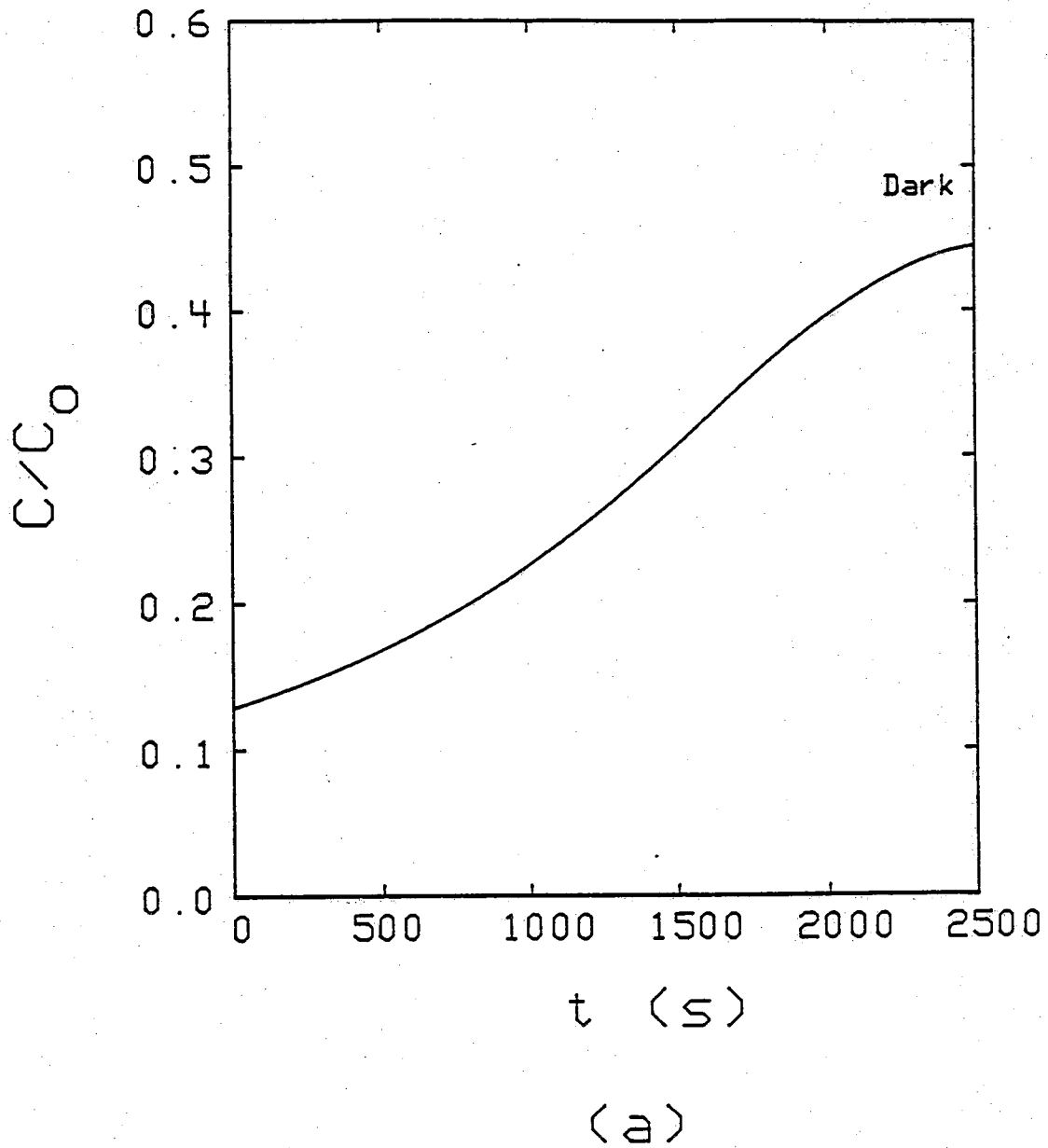


Fig. 5.8 (a) C-t transient of device M14-2 and (b) the corresponding Zerbst plot; deduced  $\tau_g=1.08$  msec.

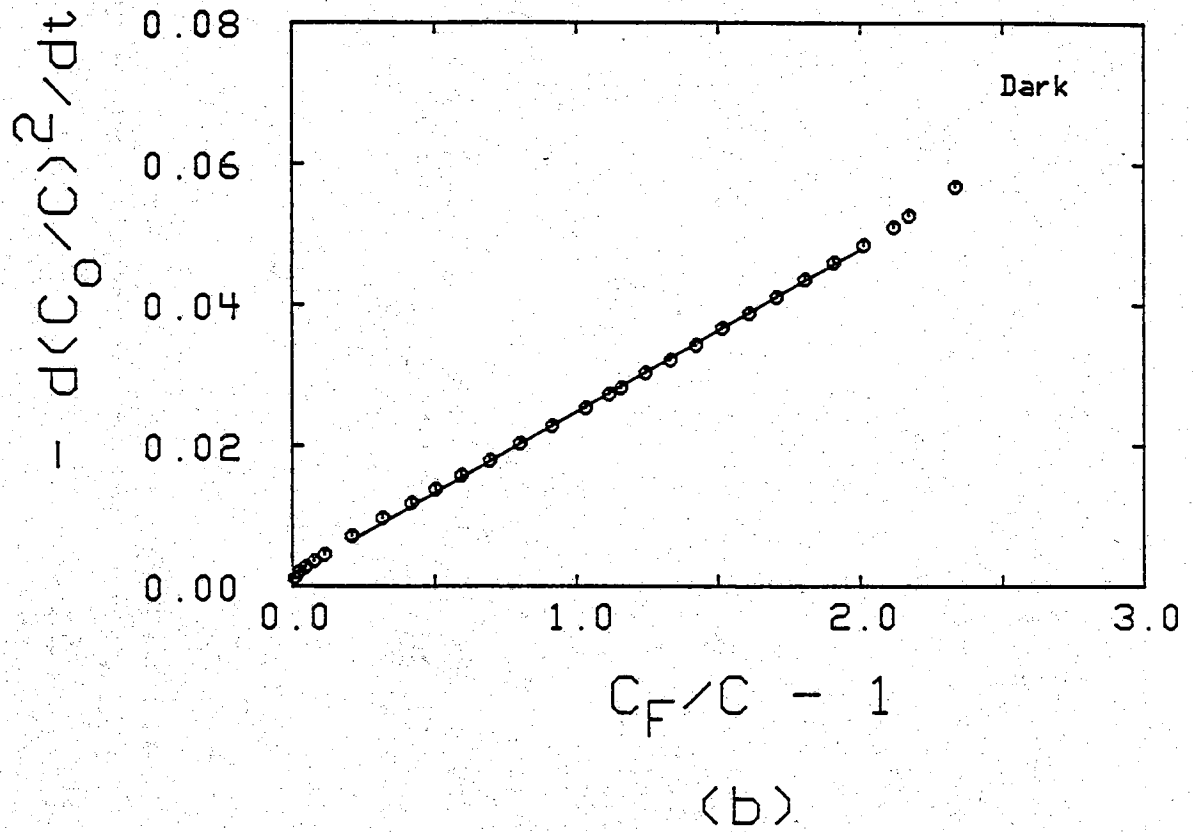


Fig. 5.8 Continued.

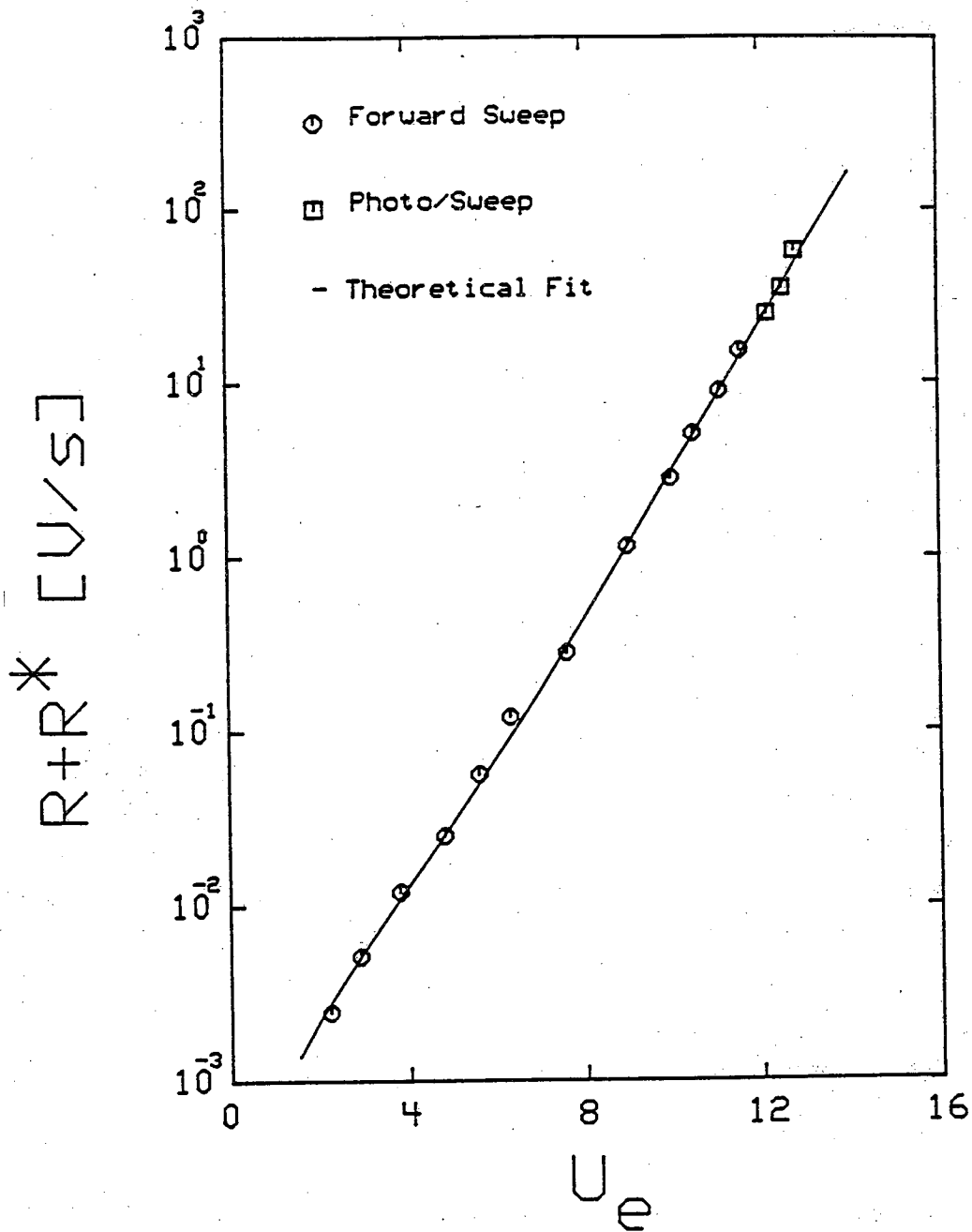


Fig. 5.9

$R+R^*$  vs  $U_e$  plot derived from device M14-2.

( $C_O = 659.8$  pF;  $C_F = 293.9$  pF;  $x_o = 0.192$   $\mu\text{m}$ ;  
 $N_D = 1.668 \times 10^{15}$   $\text{cm}^{-3}$ ;  $A_G = 0.03675$   $\text{cm}^2$ ;  $T = 296\text{K}$ ;  
 $\tau_g = 1.08$  msec;  $\tau_p = 112$   $\mu\text{sec}$  and  $\tau_n \approx 900$   $\mu\text{sec}$ .)

exhibit a relatively small  $J_{R-G}$  characteristic, the  $\tau_n$  values obtained from the theoretical fit are merely approximations.

Devices on wafer D2, with an expected shorter generation lifetime, were supposedly fabricated in an attempt to investigate the applicability of the photo/sweep and forward sweep methods to shorter lifetime devices. Wafer D2 was processed using an abbreviated wafer cleaning procedure and a much shorter phosphorus gettering time. Figs. 5.10(a) and 5.10(b) show the C-t transient and Zerbst plots derived from device D2-1. As expected,  $\tau_g$  is quite short, only 20  $\mu\text{sec}$ . Given the quoted  $\tau_g$  value, one would speculate that  $\tau_p$  is at least small in the near-Si-surface. (The C-t technique only probes the near-Si-surface region.) Consequently,  $J_{R-G}$  should be correspondingly large. Performing the forward-sweep measurements on device D2-1 indicates that  $J_{R-G}$  does indeed dominate at small biases (see Fig. 5.11)). Rather interestingly, however, upon applying the photo/sweep technique to device D2-1, we deduced a very large effective bulk diffusion length, a diffusion length greater than the thickness of the wafer. This implies that  $\tau_p$  in the quasi-neutral bulk is a quite large and different from the surface  $\tau_p$  value. As discussed previously, the precise  $\tau_p$  value inside the quasi-neutral bulk cannot be determined without knowing  $s_B$  (which is an unknown quantity) since the extracted diffusion length is larger than the thickness of the wafer.

One plausible explanation for the unusual result is that impurities were introduced onto the wafer surface during processing. The short gettering time, moreover, did not remove the added impurities. Meanwhile, the quasi-neutral bulk was properly gettered. As a result, the recombination rates in the near-Si-surface and in the bulk differed, thereby leading to two different lifetimes.

Turning to another topic, as mentioned in Subsection 5.1.2, the illumination-only method requires one to calibrate the light intensity levels to equivalent sweep rates  $R^*$ . One calibration scheme would be to obtain the same  $C_F'$  produced by known forward-sweep rates and by known levels of low-intensity illumination, giving  $R^* = R$ . Large  $R^*$  values, corresponding to high-intensity illumination, could then be deduced from an extrapolation of the calibration plot.

Figure 5.12 shows a sample calibration plot derived with device D514-1. It should be mentioned that the intensity levels shown in Fig. 5.11 were taken to be the transmission parameters of neutral density filters for a chosen intensity source.

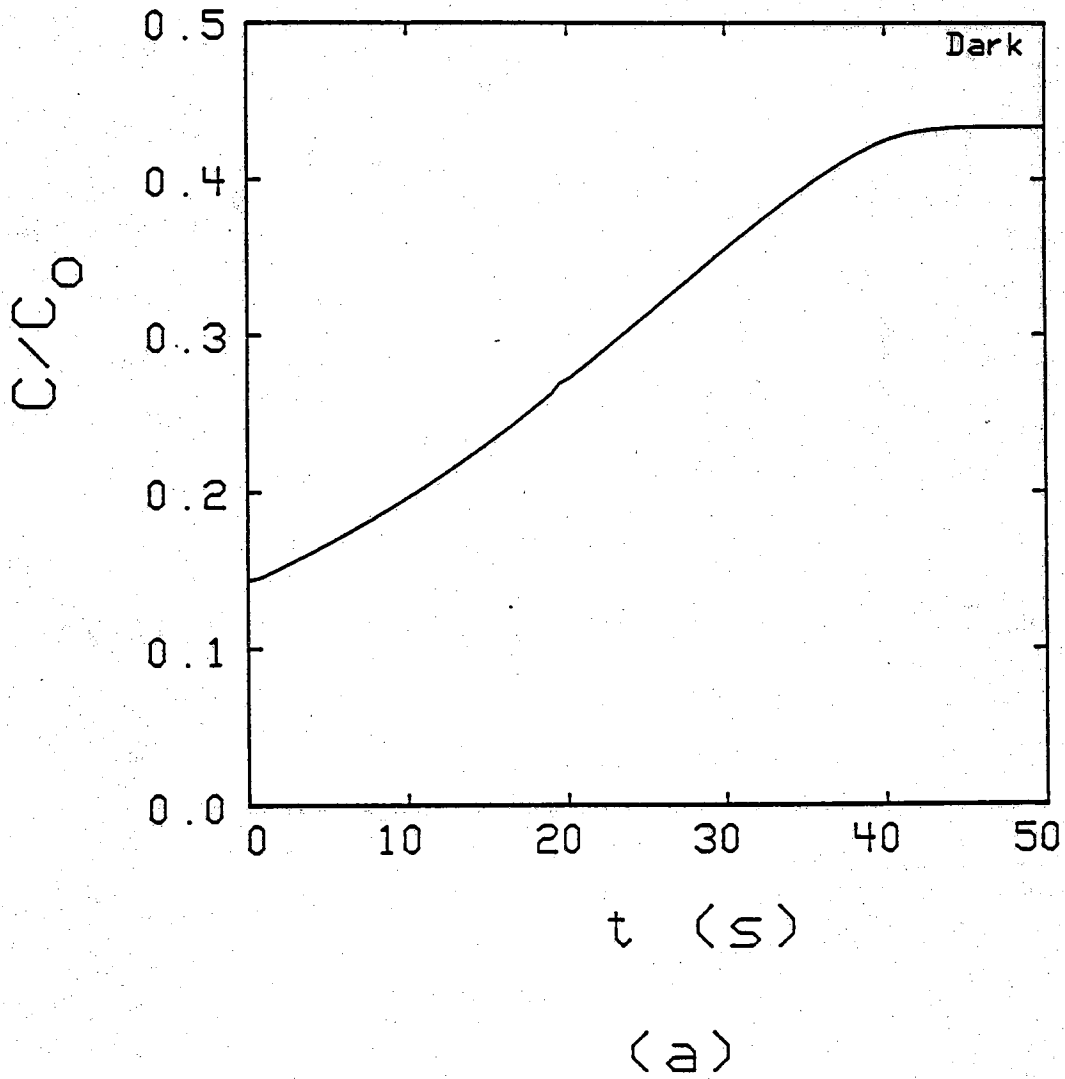


Fig. 5.10 (a) C-t transient of device D2-1 and (b) the corresponding Zerbst plot; deduced  $\tau_g = 20 \mu\text{sec}$ .

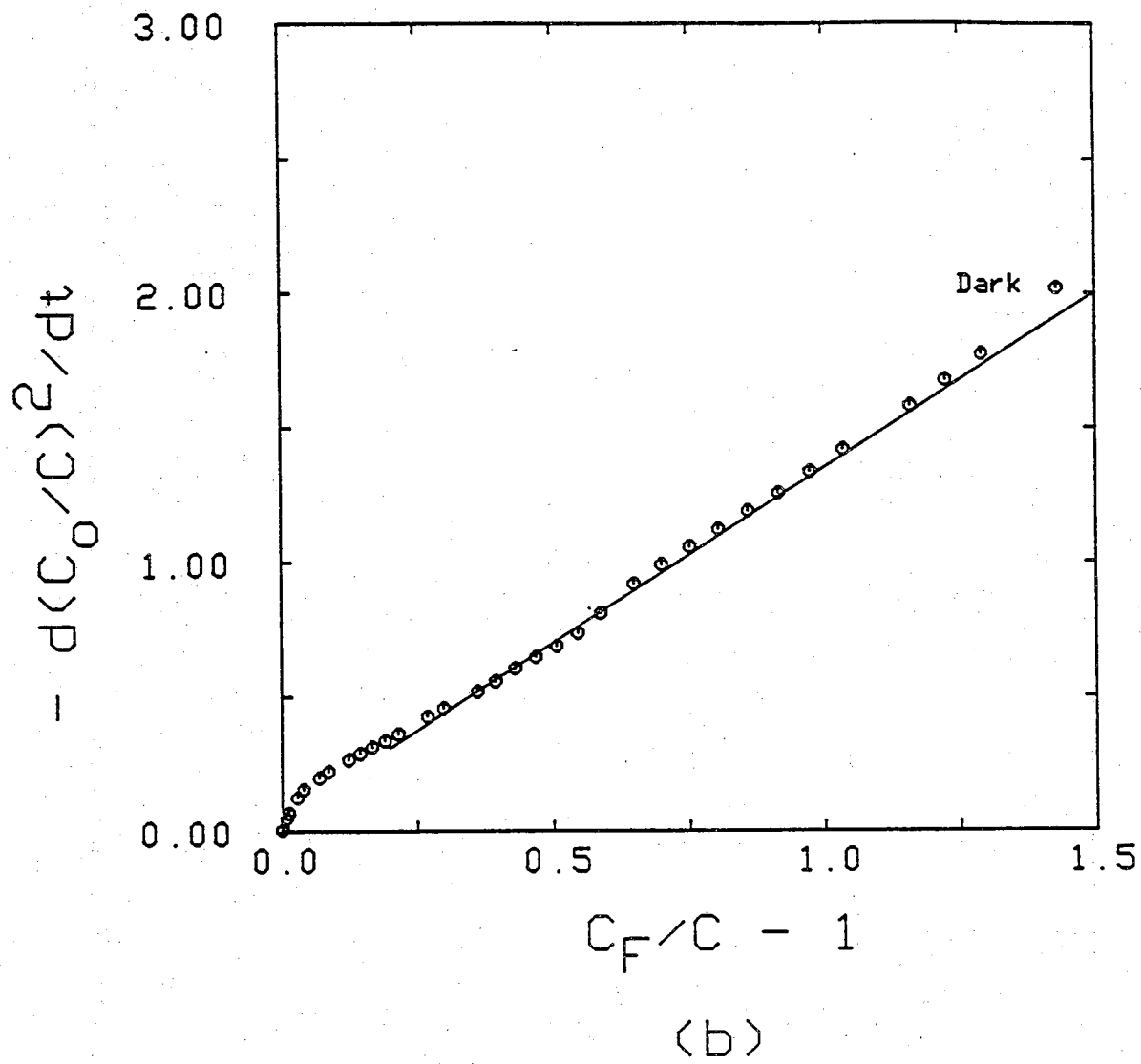


Fig. 5.10 Continued.



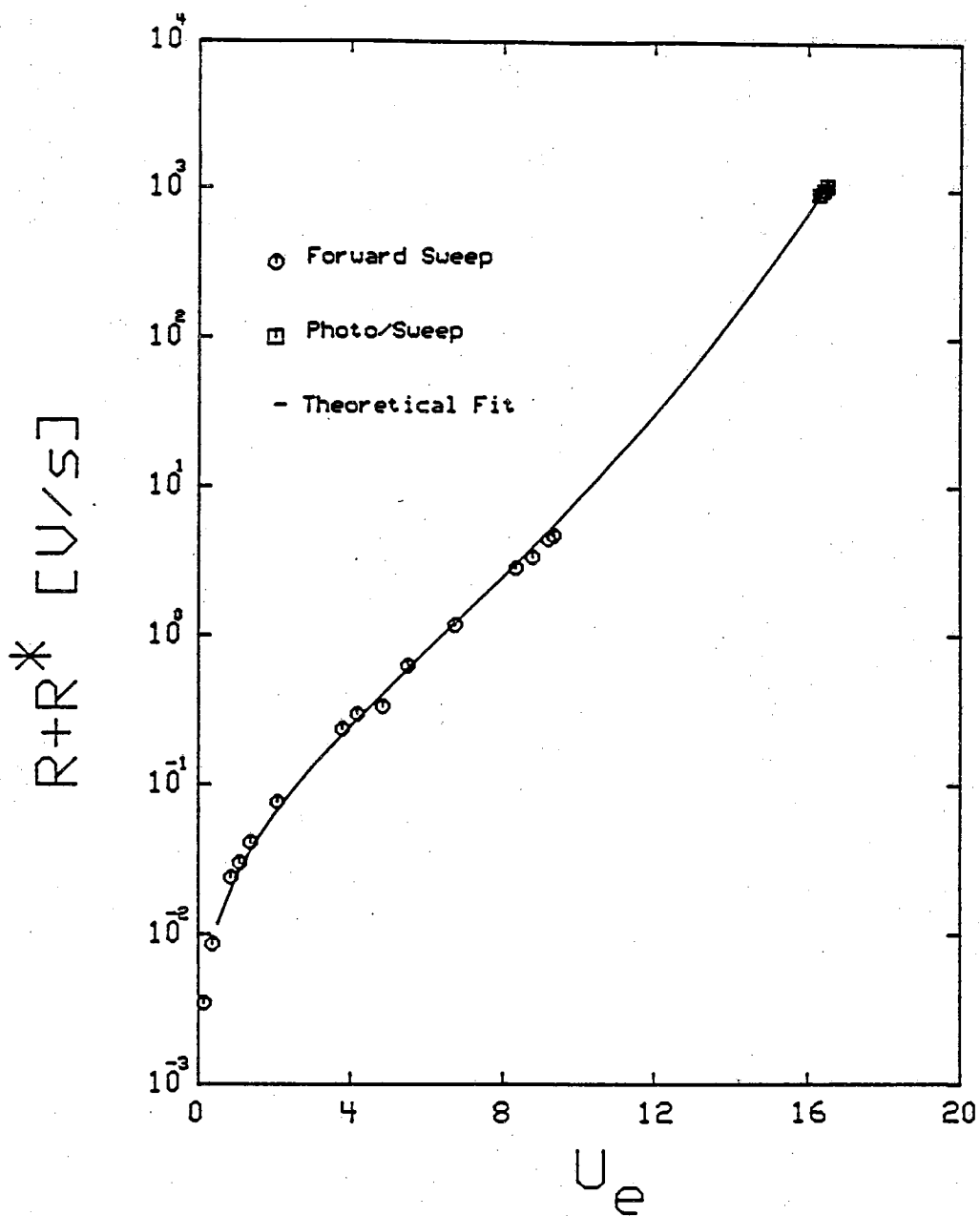


Fig. 5.11  $R+R^*$  vs  $U_e$  plot derived from device D2-1.  
 ( $C_O = 676$  pF;  $C_F = 293.2$  pF;  $x_o = 0.187$   $\mu\text{m}$ ;  
 $N_D = 1.61 \times 10^{15}$   $\text{cm}^{-3}$ ;  $A_G = 0.03675$   $\text{cm}^2$ ;  $T = 296\text{K}$ ;  
 $L_P = 0.09$  cm;  $\tau_g = 20$   $\mu\text{sec}$ ;  $\tau_n \approx 16$   $\mu\text{sec}$ ;  $\tau_p$  (at the near-Si-surface)  $\approx 3.75$   $\mu\text{sec}$ .)

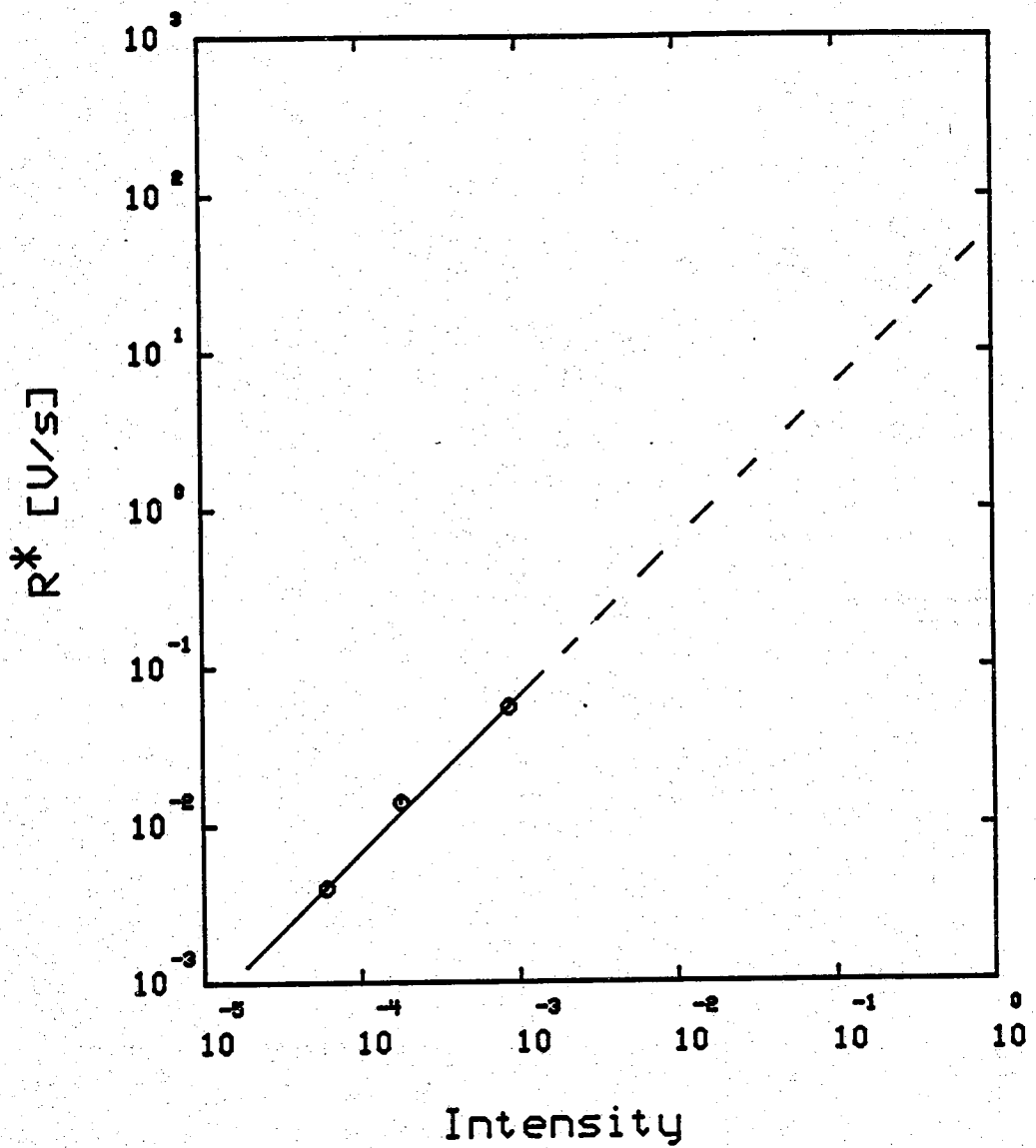


Fig. 5.12 Photo-calibration plot derived from device D514-1 under low-intensity illumination conditions. The extrapolated dash line was employed for deducing large  $R^*$  corresponding to high-intensity illumination.

The complete  $R+R^*$  vs  $U_e$  plot derived from device D514 is shown in Fig. 5.13. It clearly demonstrates that the data obtained from the calibrated illumination method are located on the same "I-V" regime as with the data obtained from the forward-sweep and photo/sweep methods. Similar to device D2-1, device D514-1 also exhibit a long  $\tau_r$  inside the quasi-neutral bulk and a short  $\tau_r$  in the near-silicon-surface. A best theoretical fit is obtained using  $\tau_g = 130.5 \mu\text{sec}$ ,  $\tau_p$  (at the near-Si-surface)  $\approx 13 \mu\text{sec}$ ,  $\tau_n \approx 110 \mu\text{sec}$ , and  $L_p = 0.075\text{cm}$ .

### 5.3 Summary

In this chapter we have explained, analyzed and demonstrated the MOS-C photo/sweep technique primarily developed to extract the carrier recombination lifetime. The measurement procedures are based on the increase in inversion capacitance  $C_F'$  in response to a set of illumination and linear sweep voltages applied to the MOS-C. Highly accurate capacitance measurements (which are required in the photo/sweep method to extract accurate  $\tau_r$ ) were achieved through the use of the DLTS S4600 system signal processor. Relative to other MOS techniques, the photo/sweep measurement method is simple, accurate, and allows one to determine  $\tau_r$  under room temperature conditions. We have illustrated use of the technique in characterizing solar cell material.

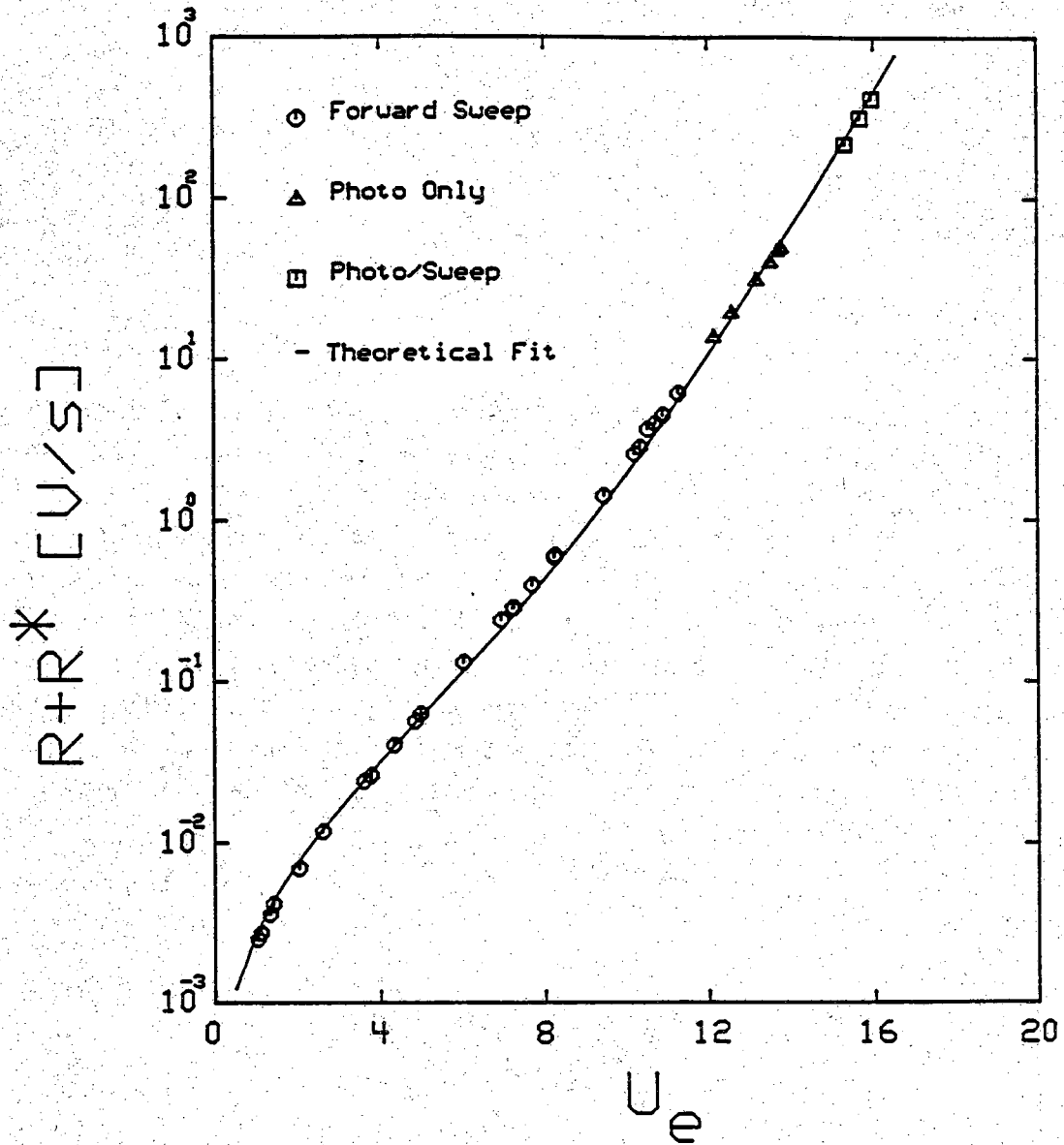


Fig. 5.13  $R+R^*$  versus  $U_e$  plot derived from device D514-1.  
 ( $C_O = 1303.5$  pF;  $C_F = 310$  pF;  $x_o = 0.091$   $\mu\text{m}$ ;  
 $N_D = 1.05 \times 10^{15}$   $\text{cm}^{-3}$ ;  $A_G = 0.03675$   $\text{cm}^2$ ;  $T = 296\text{K}$ ;  
 $L_P = 0.075$  cm;  $\tau_g = 130.5$   $\mu\text{sec}$ ;  $\tau_n \approx 110$   $\mu\text{sec}$ ;  $\tau_p$  (at the  
 near-Si-surface)  $\approx 13$   $\mu\text{sec}$ .)

## CHAPTER 6

### SUMMARY AND CONCLUSIONS

One of the design criteria for improving the silicon solar cell performance is to minimize carrier generation-recombination (G-R) rates throughout the device cell. The G-R rates, in turn, are closely related to processing. As a result, appropriate test structures, together with a systematic measurement approach, must be employed to characterize carrier generation-recombination.

The purpose of the research was to develop and employ modified and new measurement techniques for determining the carrier G-R parameters under carrier deficit and low-level carrier excess conditions using MOS-based test structures. The structures mainly consisted of MOS-capacitors (MOS-C) and Schottky-drained gate-controlled diodes (SGCD). Sample G-R parameters were extracted from test structures fabricated on 3-5 ohm-cm, (100)-oriented, float zone, n-bulk, silicon solar cell substrates as well as on lower quality n-bulk materials for comparison purposes.

Specifically, the photoaccelerated MOS-C Capacitance-time (C-t) transient technique, modified from the standard C-t method, was utilized to drastically reduce the observation time by simply illuminating the test structure during the transient; hence rapidly extracting the carrier generation lifetime ( $\tau_g$ ) while at the same time retaining the advantages of automated C-t measurements. This is important in dealing with solar cell material because of the typically long carrier lifetimes. It was shown that, in utilizing the photoaccelerated C-t technique, the observation time could be reduced by about an order of magnitude. The technique was successfully applied to MOS-C's fabricated on high quality silicon solar cell substrates, MOS-C's which exhibited generation lifetime on the order of 1 msec.

The SGCD structure, which consisted of an extended Schottky diode located next to a standard MOS-C, was developed and employed for extracting the surface generation velocity ( $s_g$ ). The structure has a distinct advantage over the conventional PN junction GCD in that it is only slightly

more complicated to fabricate and interrogate than a simple MOS-C. Typical sample  $s_g$  values were in the range of 1-3 cm/sec for well-annealed test structures. In addition, as a potential useful aside, it was demonstrated that steady-state deep-depletion C-V characteristics could be obtained using the SGCD structure.

An MOS-C photo/sweep measurement technique was developed primarily to permit the ready extraction of recombination lifetime ( $\tau_r$ ) under low-level carrier excess conditions. The new technique is based on the change in high frequency inversion capacitance in response to a set of illumination and forward-sweep voltages applied to the MOS-C. The technique allows one to extract  $\tau_r$  under room temperature conditions. It was shown that for homogeneous MOS-C's with long  $\tau_g$  (in 1 msec range), the extracted  $\tau_r$  was in the range of 100  $\mu$ secs. It had also been observed that, for some test structures, the  $\tau_r$  values at the near-Si-surface were less than the  $\tau_r$  inside the quasi-neutral bulk.

Finally, it should be re-emphasize that the work presented in this writing was in fact a portion of a larger research program. Cited MOS-based measurements established by the author were envisioned to be a means of correlating the results derived from the free carrier infra-red absorption measurement method. The latter method is under development by the author's colleague, Fati Sani, and is expected to provide the carrier recombination parameters ( $\tau_r$  and  $s_r$ ) under a broad range of carrier excess conditions. The combined systematic measurement approach will ultimately permit a complete characterization of carrier generation-recombination in the solar cell, and serve as a useful tool for further cell design and processing improvements.

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## LIST OF REFERENCES

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## **APPENDICES**

## Appendix A: Wafer Processing

This appendix outlines the step-by-step procedures for wafer cleaning, furnace operations, sputtering, photolithography and etching. Abbreviations and chemical symbols were used for the following chemicals: ACE-acetone, TCA-trichloroethane, HF-hydrofluoric acid,  $H_2O_2$ -hydrogen peroxide,  $H_2SO_4$ -sulfuric acid, DI-deionized water,  $POCl_3$ -phosphorus oxychloride, BHF-buffered hydrofluoric acid.

### A.1 Chemical Cleaning Procedures

All chemicals used in the following clean-up procedures were of electronic grade. The DI water had a resistivity of 18 Mohm-cm. Teflon and fluoroware beakers were used for the cleaning.

#### *Initial clean-up procedure #1*

1. ACE -- ultrasonically clean for 3 minutes.
2. TCA -- ultrasonically clean for 3 minutes.
3. ACE -- ultrasonically clean for 1 minute.
4. Rinse with DI -- 15 times.
5. 10:1 DI:HF -- agitate for 1 minute, then rinse in DI for several times.
6. 1:1  $H_2O_2:H_2SO_4$  -- occasionally agitate for 10 minutes.
7. Rinse in DI -- 15 times.
8. 10:1 DI:HF -- agitate for 1 minute, flush in DI for 1 minute, and then rinse in DI several times.

9. Pull dry in DI. If the wafer has been cleaned properly, no water should cling to the polished surface. If it does, repeat step 5 to 9.

*Initial clean-up procedure #2*

1. DI rinse -- 15 times.
2. 1:1 H<sub>2</sub>O<sub>2</sub>:H<sub>2</sub>SO<sub>4</sub> -- occasionally agitate for 10 minutes.
3. 50:1 DI:HF -- occasionally agitate for 10 minutes.
4. Rinse in DI -- 15 times.
5. Pull dry in DI.

*Re-clean procedure #3*

1. Rinse in DI -- several times.
2. 1:1 H<sub>2</sub>O<sub>2</sub>:H<sub>2</sub>SO<sub>4</sub> -- 10 minutes.
3. Rinse in DI -- 15 times.
4. Blow dry in N<sub>2</sub>.

## **A.2 Furnace Procedures**

The following procedures were adopted and modified from Cherne [89], and were used in fabrication procedures involving furnaces. The flow rates of gases and temperatures quoted below apply to the Tempress furnaces equipped with four inch tubes.

*Oxidation -- 1100 ° C in tube 5*

1. N<sub>2</sub> purge -- 10 minutes (2 liters/minute N<sub>2</sub>).

2. Load wafers and push to center of furnace in  $N_2$  -- 3 minutes.
3. Warm-up in  $N_2$  -- 5 minutes.
4. Oxidize in dry  $O_2$  -- 31 minute for  $0.1 \mu m$  oxide thickness or 2 hours for  $0.2 \mu m$  oxide thickness (2 liters/minute  $O_2$ ).
5. In-situ  $N_2$  anneal -- 10 minutes.
6. Pull in  $N_2$  -- 3 minutes.

*Phosphorus Gettering* -- 850 ° C in tube 6

1.  $O_2$  purge -- 15 minutes (120 cc/minute  $O_2$ ).
2.  $N_2$  purge -- 15 minutes (3 liters/minute  $N_2$ ).
3. Load wafers and push to the center of furnace in  $N_2$  -- 3 minutes push.
4. Warm-up in carrier  $N_2$  and  $O_2$  -- 3 minutes (3 liters/min  $N_2$ , 120 cc/min  $O_2$ ).
5. Phosphorous source on -- 4 or 20 minutes (40 cc/min source  $N_2$ , 3 liters/min carrier  $N_2$ , 120 cc/min  $O_2$ ).
6. Phosphorous source off -- 3 minutes.
7. Pull in carrier  $N_2$  and  $O_2$ .

*Post-Metallization Anneal (PMA)* -- 450 ° C in tube 8

1.  $N_2$  purge -- 10 minutes (2 liters/minute  $N_2$ ).
2. Load wafers and push to center of furnace -- 3 minute push.
3. Anneal for 30 minutes in  $N_2$ .
4. Pull in  $N_2$  -- 3 minutes.

### A.3 Sputtering Procedures

#### *Pre-check*

1. Check the cryopump temperature -- 20 K.
2. Switch the pumpdown control to *AUTO* mode.
3. Switch gas control to *Ar*.
4. Switch pressure gauge to *ST2*.
5. Select the *SPUTTER DEPOSIT* mode.
6. Select *TARGET 3* (aluminum target).

#### *Wafer Loading*

1. Press the *START* and *VENT* buttons simultaneously.
2. Wait for 10 minutes to unseal the vacuum.
3. Press the *HOIST* button to lift up the hoist.
4. Remove the substrate platform.
5. Load wafers onto the substrate platform.
6. Reinsert the substrate platform. Make sure that the platform does not contact the rim of the grounding plate.
7. Press the *HOIST* button to lower down the hoist.
8. Make sure the vacuum chamber is closed properly.
9. Press the *START* and *PUMP* buttons simultaneously.
10. Watch the pressure drops to about 100 microns. The cryopump value should engage automatically. If not, press the *START* and *PUMP* again.
11. When the pressure drops to 0 microns, switch *ST2* to *EMISSION*, then press the *FILAMENT* button.
12. The pressure of the vacuum chamber will gradually drop to  $10^{-7}$  torr range after 4 to 5 hours.



*Pre-Sputtering*

1. Switch from *EMISSION* to *ST2*.
2. Open the Ar cylinder valve.
3. Press the *START* and *GAS* buttons simultaneously.
4. Flip the *TOGGLE* switch to on.
5. Adjust the *NEEDLE* value until a steady pressure of 6 to 7 mtorr is attained.
6. Turn main power on.
7. Press the *HOIST POWER* on.
8. Select *TABLE 1*. (so that the substrate platform rotates away from target 3.)
9. Slowly and gradually turn the *POWER ADJUST* clockwise; adjust the *FORWARD* and *REVERSE* power to 300 watts and 5 watts, respectively, by using the *LOAD* and *TUNE* knobs.
10. Watch for a purple color plasma.
11. Pre-sputter for about 10 minutes.

*Sputter-Deposition*

1. Turn the *POWER ADJUST* counterclockwise to reduce the forward power to about 50 watts.
2. Select *TABLE 3* and observe the substrate platform rotates from position 1 to position 3.
3. Adjust the forward power to 100 watts. The reverse power remains at 5 watts.
4. Sputter for 30 minutes.

### *Wafer Removal*

1. Turn the *POWER ADJUST* fully counterclockwise.
2. Press the *HOIST POWER* to off.
3. Turn the main power off.
4. Flip the *TOGGLE* switch to off.
5. Close the Argon cylinder valve.
6. Press the *START* and *VENT* buttons.
7. Wait for 10 minutes to unseal the vacuum.
8. Press the *HOIST* button to lift up the hoist.
9. Remove the substrate platform.
10. Unload the wafers.
11. Reinsert the substrate platform.
12. Press the *HOIST* button to lower down the hoist.
13. Make sure the vacuum chamber is properly sealed.
14. Press the *START* and *PUMP* buttons simultaneously.
15. Watch the pressure drops to about 100 microns. The cryopump valve should engage automatically. If not, press the *START* and *PUMP* again.
16. When the pressure drops to 0 microns, switch *ST2* to *EMISSION*, then press the *FILAMENT* button.

## **A.4 Photolithographic and Etching Procedures**

### *AZ-1950J Positive Photoresist Application*

1. Prebake -- 10 minutes, 110 °C.
2. Apply resist -- 4400 rpm, 40 seconds.

3. Inspect; remove with ACE if necessary.
4. Soft-bake -- 15 minutes, 90 ° C.
5. Align and UV expose -- 1.5 minute exposure time.
6. Develop in AZ Developer for 60 seconds, follow with DI rinse for 60 seconds.
7. Inspect if the resist patterns are well defined; remove with ACE and start from step 1 if necessary.
8. Hard-bake -- 10 minute, 110 ° C.

#### *AZ-1350J Positive Resist Removal*

1. Agitate wafer in ACE for 5 minutes.
2. Rinse in fresh ACE for 2 minutes.
3. Rinse in DI for 1 minute.
4. Blow dry in N<sub>2</sub>.

#### *KTI 747 Negative Resist Application*

1. Prebake -- 10 minutes, 110 ° C.
2. Apply KTI 747 -- 3000 rpm, 40 seconds.
3. Inspect; remove with xylene if necessary.
4. Soft-bake -- 10 minutes, 85 ° C.
5. Align and UV expose -- 30 second.
6. Develop in Developer II solution for 90 seconds, then rinse in Rinse I solution for 30 seconds.
7. Inspect if the resist patterns are well defined. If not, remove with xylene and re-start from step 1.
8. Hard-bake -- 10 minutes, 110 ° C.

*KTI 747 Negative Resist Removal*

1. Moderately heat wafers in Nophenol for 5 minutes.
2. Rinse in TCA for 3 minutes, then in ACE for 2 minutes.
3. Rinse in DI for 1 minute.
4. Blow dry in N<sub>2</sub>.

*SiO<sub>2</sub> Etching Procedure*

1. Estimate etch time in advance; BHF etch rate  $\approx 1000 \text{ \AA}/\text{min}$ .
2. Agitate wafers in BHF for 80% of the estimated time.
3. Remove and rinse thoroughly in DI.
4. Inspect the opening with an microscope.
5. Etch again in BHF and repeat step 3 and 4 until the opening is properly etched.

*Aluminum Etch Procedures*

1. Agitate and watch wafers in aluminum acid etch until the aluminum is completely etched off.
2. Rinse 15 times in DI.
3. Blow dry in N<sub>2</sub>.

**Appendix B: Derivation of Eqs. (5.5), (5.6) and (5.7)**

Starting with the steady-state recombination rate  $R$ , we have

$$R = \frac{np - n_i^2}{\tau_n(p + p_1) + \tau_p(n + n_1)} \quad (\text{B.1})$$

or

$$R = \frac{np - n_i^2}{\tau_g n_i \left( 1 + \frac{\tau_p}{\tau_g} \frac{n}{n_i} + \frac{\tau_n}{\tau_g} \frac{p}{n_i} \right)} \quad (\text{B.2})$$

where

$$\tau_g \equiv \tau_n \left( \frac{p_1}{n_i} \right) + \tau_p \left( \frac{n_1}{n_i} \right) \quad (\text{B.3})$$

Assuming low-level injection, one can express the carrier concentrations as [69]

$$n = n_i e^{(U - U_F)} \quad (\text{B.4a})$$

and

$$p = n_i e^{(U_F + U_c - U)} \quad (\text{B.4b})$$

where

$$U_e \equiv \frac{E_F - F_P}{kT} \quad (\text{B.5})$$

$U_e$  is defined as the effective voltage (see Fig. 5.2b). In writing Eq. (B.4b) we have assumed that the quasi-Fermi level  $F_P$  of the minority carrier holes is spatially invariant throughout the space-charge region.

Substituting Eqs. (B.4a), (B.4b) and (B.5) into Eq. (B.2) yields

$$R = \frac{n_i(e^{U_e} - 1)}{\tau_g \left( 1 + \frac{\tau_p}{\tau_g} e^{U - U_F} + \frac{\tau_n}{\tau_g} e^{U_F + U_e - U} \right)} \quad (\text{B.6})$$

The relationship between the potential  $U$  and normalized electric field  $F$  is [69]

$$\hat{U}_s \frac{kT}{q} \frac{F(U, U_F, U_e)}{L_D} = \frac{-kT}{q} \frac{dU}{dx} \quad (\text{B.7a})$$

or

$$\hat{U}_s \frac{dU}{F(U, U_F, U_e)} = \frac{-dx}{L_D} \quad (\text{B.7b})$$

where

$$F(U, U_F, U_e) = \left[ e^{U_F + U_e} (e^{-U} + U - 1) + e^{U_F} (e^U - U - 1) \right]^{\frac{1}{2}} \quad (\text{B.8})$$

Multiplying both sides of Eq. (B.7b) by  $qR$  and integrating both sides accordingly gives

$$\hat{U}_s q \int_{U_s}^0 \frac{RdU}{F(U, U_F, U_e)} = -q \int_0^W \frac{Rdx}{L_D} \quad (\text{B.9a})$$

or

$$\hat{U}_s q \int_0^{U_s} \frac{RdU}{F(U, U_F, U_e)} = \frac{q}{L_D} \int_0^W Rdx \quad (\text{B.9b})$$

Notice that in writing Eq. (B.9b), we have used the boundary conditions that at  $x=W$ ,  $U=0$  and at  $x=0$ ,  $U=U_s$ . The recombination current  $J_{R-G}$  is expressed as

$$J_{R-G} = q \int_0^W Rdx \quad (\text{B.10})$$

Therefore, Eq. (B.9b) is rewritten as

$$J_{R-G} = L_D q \frac{n_i}{\tau_g} \gamma \left( e^{U_e} - 1 \right) \quad (\text{B.11})$$

or

$$J_{R-G} = q \frac{n_i}{\tau_g} W_R \quad (\text{B.12})$$

where

$$W_R = \gamma L_D \left( e^{U_e} - 1 \right) \quad (\text{B.13})$$

and

$$\gamma = \hat{U}_s \int_0^{U_s} \frac{dU}{\left(1 + \frac{\tau_p}{\tau_g} e^{U-U_F} + \frac{\tau_n}{\tau_g} e^{U_F+U_c-U}\right) F(U, U_F, U_c)} \quad (\text{B.14})$$



### Appendix C: Derivation of the $C_F' - U_e$ Relationship [84]

Two major assumptions are made in deriving the  $C_F' - U_e$  relationship. First, for an N-bulk MOS-C (which will be assumed henceforth), the quasi-Fermi level  $F_P$  of the minority hole carrier is taken to be spatially invariant throughout the space-charge region. Second, low-level injection conditions are assumed to prevail. Under low-level injection conditions, the minority carrier hole concentration will be negligible compared to the majority carrier electron concentration in the quasi-neutral bulk. Hence little error is introduced by taking  $F_P$  in the bulk to be the same as that in the space-charge region. In other words, we assume  $F_P$  is independent of positions throughout the substrate. The derivation then parallels the standard high-frequency exact  $C - V_G$  analysis which includes minority carrier redistribution [86,87].

After integrating the Poisson's equation, the normalized electric field is found to be

$$F(u, U_F, u_P) = \left[ e^{u_P} (e^{-u} + u - 1) + e^{U_F} (e^u - u - 1) \right]^{\frac{1}{2}} \quad (C.1)$$

where

$$u = U + \tilde{u} \quad (C.2)$$

$$u_P = U_P + \tilde{u}_P \quad (C.3)$$

$$U_P = U_F + U_e = \frac{E_{i_{\text{bulk}}} - F_P}{kT} \quad (C.4)$$

$u$  is the total normalized potential,  $U$  is the normalized dc potential,  $\tilde{u}$  is the

normalized ac potential,  $u_p$  is the total normalized quasi-Fermi level for holes,  $U_p$  is the normalized dc quasi-Fermi level, and  $\tilde{u}_p$  is the normalized ac quasi-Fermi level.

The normalized electric field at the Si-SiO<sub>2</sub> interface is

$$F_S = F(u_S, U_F, u_P) = \left[ e^{u_F}(e^{-u_S} + u_S - 1) + e^{U_F}(e^{u_S} - u_S - 1) \right]^{\frac{1}{2}} \quad (C.5)$$

The gate voltage, in turn, can be expressed as

$$V_G' = \frac{kT}{q} \left[ U_S + \hat{U}_S \frac{x_o'}{L_D} F(U_S, U_F, U_P) \right] \quad (C.6)$$

Eq. (C.6) can be solved for  $U_P$ , yielding

$$U_P = \ln \left[ \frac{\left[ \frac{[V_G'/(kT/q)] - U_S}{x_o'/L_D} \right]^2 - e^{-U_F}(e^{U_S} - U_S - 1)}{e^{-U_S} + U_S - 1} \right] \quad (C.7)$$

With the constraint that the total number of minority carriers remain invariant under the high-frequency conditions, we must have

$$G(u_S, U_F, u_P) = G(U_S, U_F, U_P) \quad (C.8)$$

where

$$G(u_S, U_F, u_P) = \int_0^{U_S} \frac{e^{u_P}(e^{-u}-1)}{F(u, U_F, u_P)} du \quad (C.9)$$

The G function is proportional to the total minority hole carrier concentration in the inversion layer. Expanding the left-hand-side of Eq. (C.8) in Taylor's series and retaining the first-order terms yields

$$\frac{\tilde{u}_P}{\tilde{u}_S} = - \frac{\frac{\partial G}{\partial u_S} \Big|_o}{\frac{\partial G}{\partial u_P} \Big|_o} \quad (C.10)$$

where  $\Big|_o$  means the partial derivatives are evaluated under dc bias conditions.

Under the inversion and depletion conditions the depletion width  $W_F'$  is related to the small signal surface electric field and surface potential by

$$W_F' = - \frac{L_D}{\tilde{F}_S / \tilde{u}_S} \quad (C.11)$$

Expanding Eq. (C.5) in a Taylor's series and, again, retaining only the first-order terms, one obtains

$$\frac{\tilde{F}_S}{\tilde{U}_S} = \frac{\partial F}{\partial u_S} \Big|_o + \frac{\partial F}{\partial u_P} \Big|_o \left[ \frac{\tilde{u}_P}{\tilde{u}_S} \right] \quad (C.12)$$

Substituting Eq. (C.10) into Eq. (C.12) gives

$$\frac{\tilde{F}_S}{\tilde{U}_S} = \frac{\partial F}{\partial u_S} \Big|_o - \frac{\partial F}{\partial u_P} \Big|_o \frac{\partial G / \partial u_S \Big|_o}{\partial G / \partial u_P \Big|_o} \quad (C.13)$$

Evaluating the four individual partial derivatives on the two right-hand-side

of Eq. (C.13), and after performing some mathematical manipulation, one obtains

$$\frac{\tilde{F}_S}{\tilde{u}_S} = \frac{e^{U_P}(1-e^{-U_S})/(1+\Delta) + e^{-U_F}(e^{U_S}-1)}{2F(U_S, U_F, U_P)} \quad (C.14)$$

where

$$\Delta = \frac{(e^{-U_S}+U_S-1)/F(U_S, U_F, U_P)}{\int_0^{U_S} \frac{e^{-U_F}(e^U-1)(e^{-U}+U-1)}{2F^3(U, U_F, U_P)} du} \quad (C.15)$$

From the foregoing analysis, we have the following set of control equations

$$C'_F = \frac{C_o}{1+(W'_F/x'_o)} \quad (C.16)$$

$$W'_F = -L_D \left[ \frac{2F(U_S, U_F, U_P)}{e^{U_F}(1-e^{-U_S})/(1+\Delta) + e^{-U_F}(e^{U_S}-1)} \right] \quad (C.17)$$

$$V'_G = \frac{kT}{q} U_S + \hat{U}_S \frac{x'_o}{L_D} F(U_S, U_F, U_P) \quad (C.18)$$

$$U_P = \ln \left[ \frac{\left[ \frac{[V'_G/(kT/q)] - U_S}{x'_o/L_D} \right]^2 - e^{-U_F}(e^{U_S} - U_S - 1)}{e^{-U_S} + U_S - 1} \right] \quad (C.19)$$

with

$$U_P = U_F + U_e \quad (\text{C.20})$$