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Pulse-Width Modulation Control of a Three-Phase Inverter

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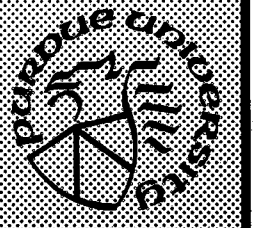

Pulse-Width Modulation Control of a Three-Phase Inverter

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this is dedicated
to the honor and glory of God

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ABSTRACT

O'Connor, Shawn M. M.S.E.E., Purdue University. August 1988. **PULSE-WIDTH MODULATION CONTROL OF A THREE-PHASE INVERTER.** Major Professor: Lawrence L. Ogborn.

The goal of this thesis was to design, construct, and prove operational a three-phase inverter. This inverter was to incorporate pulse-width modulation control and was to function as a classroom demonstration unit. Before constructing the full three- phase inverter, a single-phase inverter was constructed with four Darlingtons. A pulse-width modulation scheme was developed and applied to the single-phase inverter. Upon slight modification of the control scheme, controllable single-phase inverter operation was demonstrated. With this insight gained, a pulse-width modulation scheme was developed for a three-phase inverter. After adding a third set of Darlingtons to the initial four, the pulse-width modulation scheme was applied and three-phase inverter operation proved successful.

CHAPTER 1

INTRODUCTION

The object of this thesis was to design and construct a three-phase inverter capable of motor control. This speed control was to be achieved by pulse-width modulation. Darlington bipolar transistors, instead of thyristors, were chosen for the inverter switches since they didn't require forced commutation. In developing the three-phase inverter, several steps were taken. First, the requirements of the Darlington switches were chosen and thermal design was performed. A type of heat sink was chosen and tested to ensure performance. This process is described in Chapter 2 of this thesis. Next, four Darlingtons with their respective heat sinks were put together to form a single-phase inverter. Then, driver circuits were developed to provide sufficient current to turn a Darlington on given a logic signal input. An initial logic scheme was then designed to turn each of the four Darlingtons on at the proper time for single-phase inverter operation. However, upon testing, this design was found inadequate and a better successful logic scheme was implemented. These design features of the single-phase inverter are discussed in Chapter 3. In Chapter 4 the successful operation of the single-phase inverter is pictorially described and commented upon. The next step was to add two more Darlingtons onto the single-phase inverter structure, thereby converting it to a three-phase inverter. Drive circuits similar to those used for the single-phase inverter were put together and attached to their respective Darlingtons. Next, control logic was developed to turn on the Darlington transistors in the proper sequence to provide an AC output voltage at the switching frequency. After this control logic was tested separately for the correct logic timing, it was attached to the six Darlington drivers. The design features of the three-phase inverter are described in Chapter 5. In Chapter 6 the successful operation of the three-phase inverter is pictorially described and commented upon. Finally, Chapter 7 presents conclusions and recommendations for future research.

CHAPTER 2

DESIGN CONSIDERATIONS OF THE THREE-PHASE INVERTER

In the design for the three-phase inverter, it was desired that the input direct current voltage be 50 volts and that the Darlingtons switch 10 amperes. These parameters were chosen in hope of running a 50 volt, 10 ampere induction motor with the inverter. Therefore, 2N6577 NPN Darlingtons were chosen for the six switches. This choice was made since these Darlingtons can withstand a maximum forward biased voltage of 90 volts and can carry 15 amperes of current continuously. The internal connections of the Darlington is shown in Figure 2.1. Note the two resistors present in the device to dissipate charge from the pn junctions when the Darlington is off, and also the diode present to protect the Darlington from any reverse currents.

2.1 Heat Sink Design

After the choice of the 2N6577 NPN Darlington was made, a thermal analysis was made of the device in order to establish a proper heat sink for it [1]. The thermal circuit in Figure 2.2 was used as a model for the Darlington [2]. With the input to the inverter as 50 volts, it was desired to run 10 amps of current through the Darlington. The nominal "on" voltage of the Darlington from collector to emitter is 2.8 volts. Hence, each switch will dissipate about 28 watts. In designing for the heat sink, 30 watts was used as the value that each Darlington must dissipate. The junction to case thermal resistance, Θ_{JC} is 1.46 deg C/W as given by the Darlington data sheet. The thermal resistance, Θ_{CS}, of the silicon grease which was put between the Darlington case and the heat sink was .2 deg C/W. The total power dissipation at 25 degrees Celsius is 120 watts and it derates at .685 W/deg C above 25 degrees Celsius. Then the equation that is used to determine the Celsius temperature for a given power dissipated is:

$$^{\circ}\mathrm{C} = (-1 \,/\, .685) * (\text{power dissipated}) + 200$$

Putting the 30 watts that need to be dissipated into the above equation

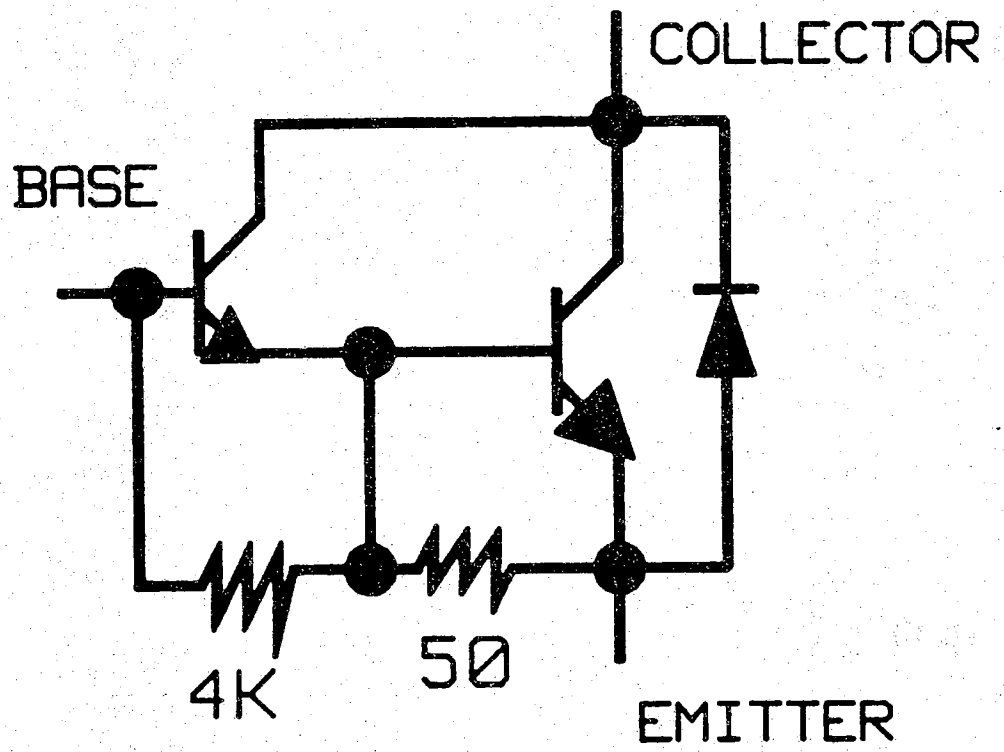

Figure 2.1. NPN Darlington.

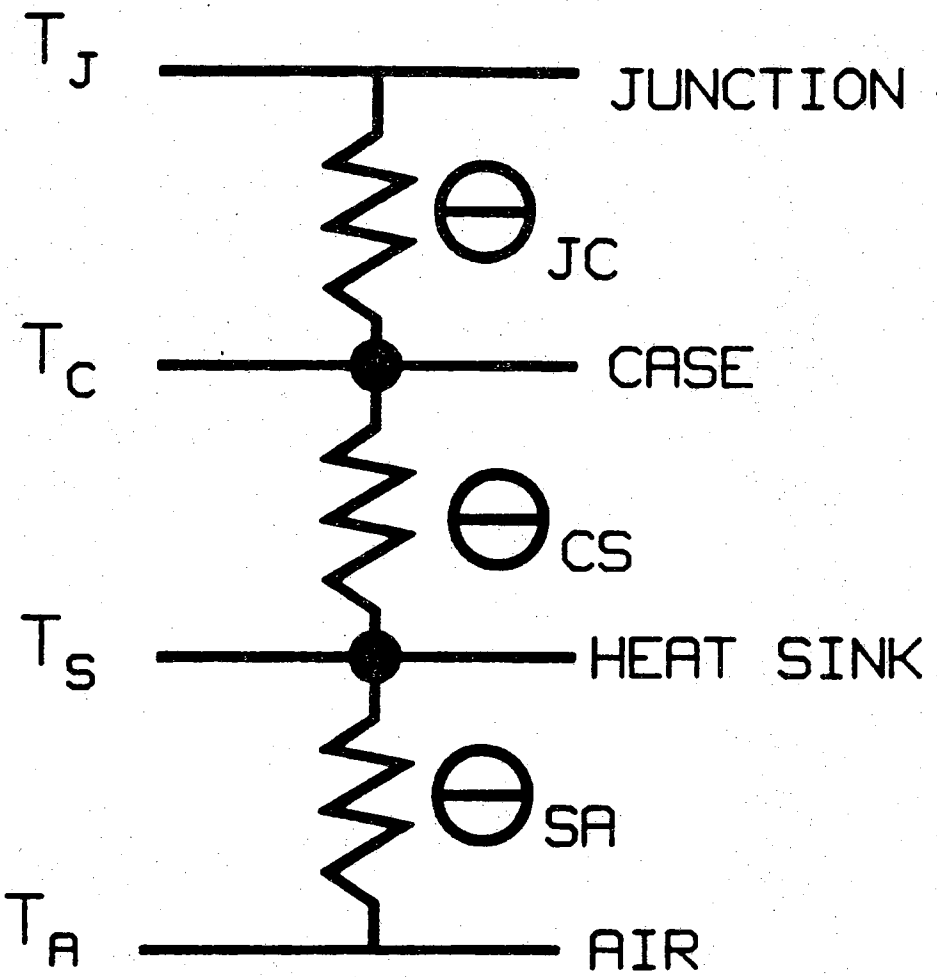

Figure 2.2. Darlington Thermal Circuit.

produces a maximum operating temperature of 156 deg C. The assumed theoretical ambient operating temperature is 25 deg C. Since thermal resistance, Θ, is defined as the change in temperature divided by the power dissipated, the maximum amount of thermal resistance allowable from the Darlington junction to the ambient air, Θ_{JA}, is:

$$\Theta = (156-25)\,^\circ\text{C} \,/\, 30\ \text{W} = 4.3\,^\circ\text{C/W}$$

Hence, it was determined that the desired heat sink's thermal resistance must be no greater than 2.64 deg C/W as shown below:

$$\Theta_{SA} = \Theta_{JA} - \Theta_{JC} - \Theta_{CS}$$

Upon putting in the values,

$$\Theta_{SA} = 4.3 - 1.46 - .2 = 2.64\,^\circ\text{C/W}$$

2.2 Heat Sink Choice Verification

A choice of a heat sink was made from available supplies. To test it, an Omega thermistor (part #ON-940-44007-SK @ 25 deg C) was procured. The thermistor resistance was measured versus temperature and the results are shown in Table 2.1. The thermistor was then mounted next to the Darlington in the heat sink. In order to make a thermal assessment of the Darlington, the circuit of Figure 2.3 was constructed. The leads of the thermistor were connected to an ohmmeter. With V_d adjusted to 10.17 volts, I_c was measured with an ammeter as 2.91 amps. This resulted with

$$\text{Power} = V_d * I_c = 10.17\ \text{V} * 2.91\ \text{A} = 29.59\ \text{W}$$

as the power dissipated through the Darlington. At this power level, the thermistor resistance was 388 ohms. By linearly interpolating Table 2.1 using this thermistor value, a temperature of 94.71 deg C was calculated. Using 22.5 deg C as the ambient air temperature, the thermal resisance was calculated as:

$$\Theta_{SA} = (94.71 - 22.5)\,^\circ\text{C} \,/\, 29.59\ \text{W} = 2.44\,^\circ\text{C/W}$$

This proved to be an adequate amount of thermal resistance since it is below the 2.64 deg C/W restriction set previously.

Table 2.1. **Thermistor Resistance Versus Temperature in Degrees Celsius.**

Temperature in Degrees C	Resistance in Kiloohms
98.0	.346
90.0	.448
85.0	.518
80.0	.629
75.0	.739
70.0	.883
65.0	1.045
60.0	1.255
55.0	1.493
44.0	2.26
40.0	2.66
35.0	3.20
30.0	4.00
25.0	4.95
22.5	5.59

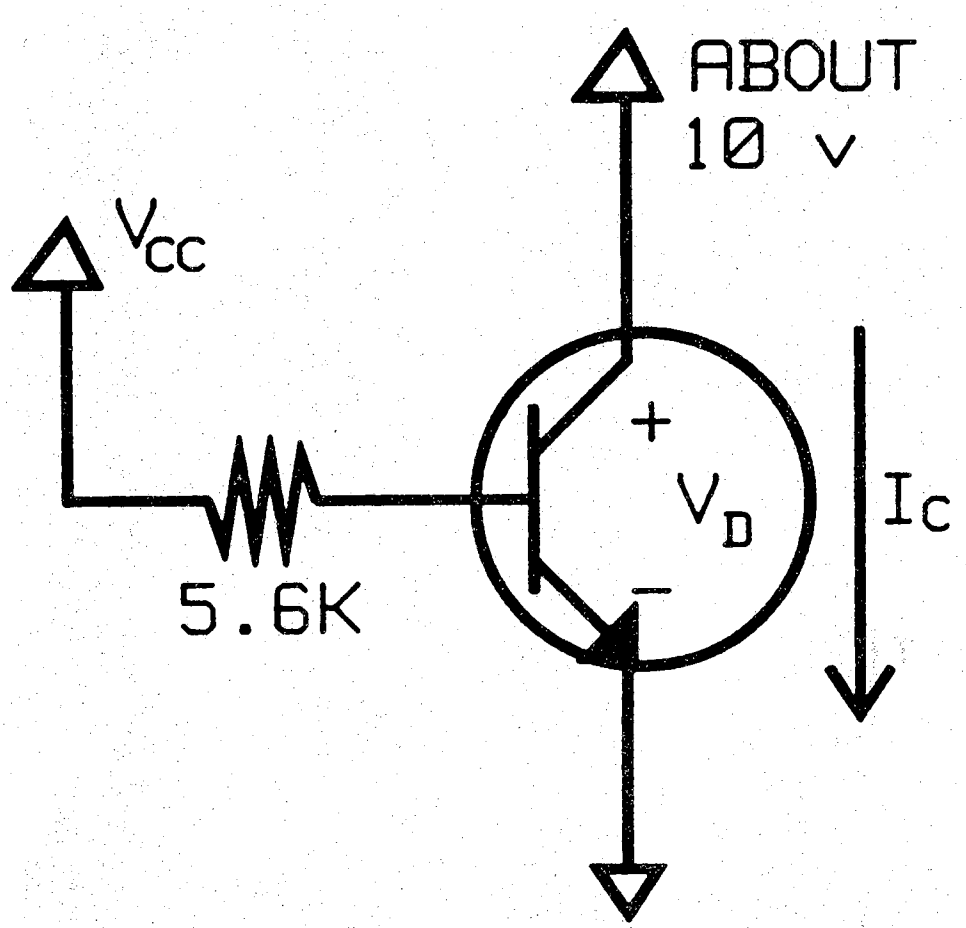

Figure 2.3. Darlington Hook-Up for Thermal Measurements.

CHAPTER 3

DESIGN OF THE SINGLE-PHASE INVERTER CONTROLS

Before constructing the entire three-phase inverter, it was decided to construct just a single-phase inverter with four of the Darlingtons and develop a control scheme for it. V_{DC} was a 50 volt power supply, but was generally set at points between 20 volts and 40 volts during testing. The single-phase circuit is shown in Figure 3.1. The Darlingtons are labelled A,B,C, and D.

3.1 Upper Darlington Switch Design

The upper two switches have drive circuitry as shown in Figure 3.2. In this diagram, the 2N6577 NPN Darlington is symbolized with a circle around it showing that it is more complicated than a single transistor. Since it is the upper switch, its collector is connected to the DC voltage supply and its emitter is attached to one end of the load. Its base is driven by a 2N2222 NPN transistor which in turn is driven by a 4N37 optocoupler. The optocoupler is symbolized by a diode and a transistor enclosed by a circle. The optocoupler provides electrical isolation, separating the low-power logic signal that provides the logic for switching the Darlington from the higher-power Darlington itself. The circuit was designed as follows. The desired maximum current for the Darlington was 10 amps from collector to emitter. The maximum saturation voltage from collector to emitter is 2.8 volts with the maximum base to emitter voltage as 3.5 volts. Hence, the base had to be higher than V_{DC} by .7 volts. Since the minimum beta of the Darlington is 500, the minimum base current needed was:

$$\text{Base current} = 10 \text{ A} / 500 = 20 \text{ mA}$$

It was decided that the base current of the Darlington should be 100 milliamps to ensure saturation. Therefore, a 5 volt power supply was added on to V_{DC} to drive 100 milliamps through the 2N2222 and to let the Darlington base voltage to be .7 volts above V_{DC}. The maximum saturation collector to emitter voltage of the 2N2222 is .4 volts. Therefore, the collector voltage of

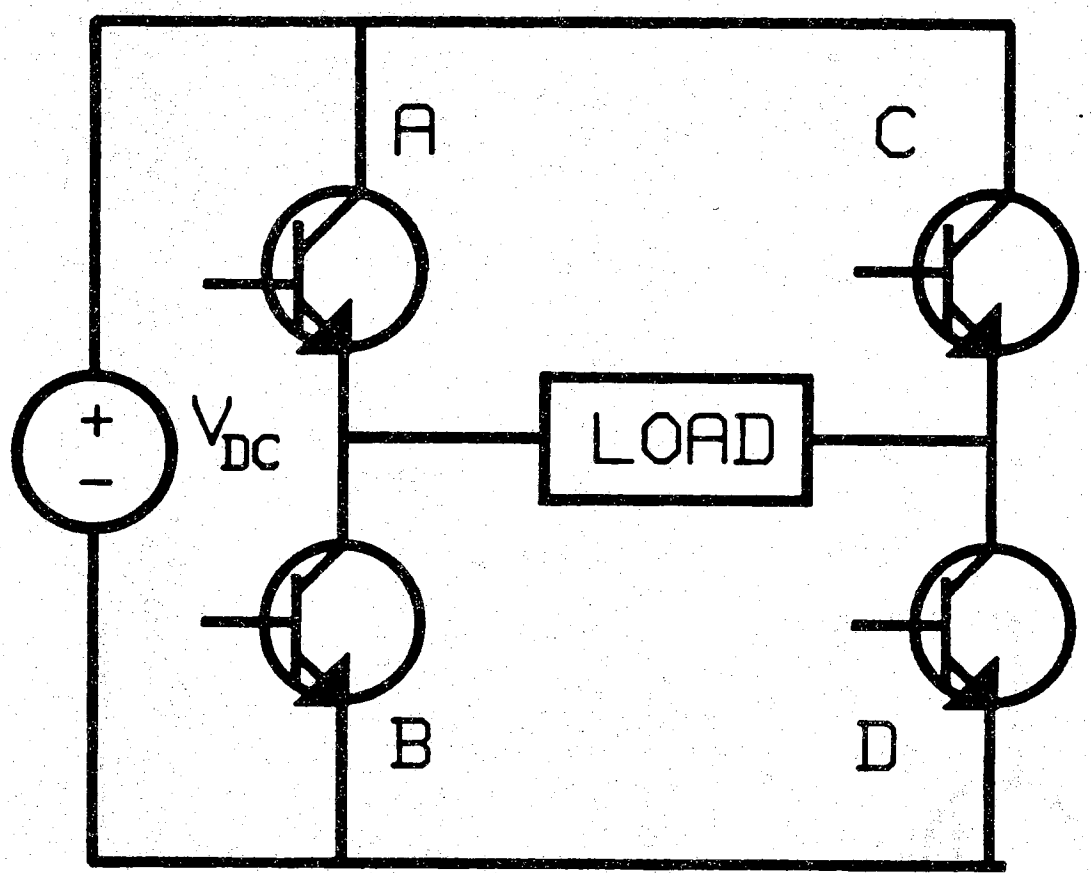

Figure 3.1. Single-Phase Inverter Circuit.

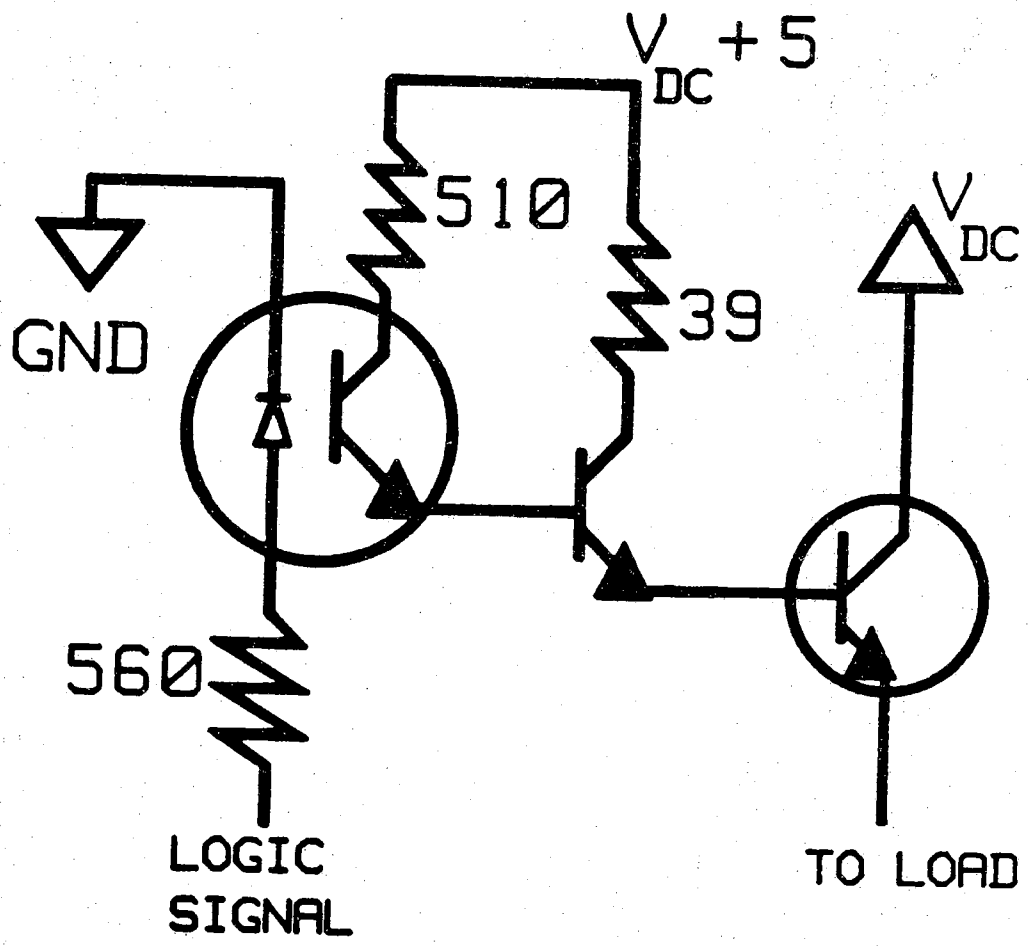

Figure 3.2. Upper Darlington Switch Drive Circuitry.

the 2N2222 was to be 1.1 volts above V_{DC}. The minimum beta of the 2N2222 transistor is 100; hence, if the emitter current is 100 milliamps, the base current would be 1 milliamp. However, to ensure saturation of the 2N2222, 5 milliamps was chosen as the desired base current. This leaves 95 milliamps as the collector current. The way the 39 ohm collector resistor, R_C, was calculated is shown below:

$$R_C = ((V_{DC} + 5) - (V_{DC} + 1.1))\ V/95\ mA = 41\ \Omega$$

A 39 ohm resistor was used since it was the closest conservative value resistor obtainable. The maximum base to emitter voltage for the 2N2222 is 1.3 volts and the maximum collector to emitter voltage for the optocoupler is .3 volts. Adding these values to the Darlington base voltage, which is already .7 volts above V_{DC}, we obtain the optocoupler collector voltage as V_{DC} + 2.3 volts. Since the optocoupler collector current is also 5 milliamps as is the optocoupler emitter current, R_{opt}, the optocoupler collector resistor is calculated below:

$$R_{opt} = ((V_{DC} + 5) - (V_{DC} + 2.3))\ V\ /\ 5mA = 540\ \Omega$$

A 510 ohm resistor was used since it was the closest conservative value resistor available. For 5 milliamps out of the optocoupler, it was found from a data sheet graph that 6 milliamps was needed as the input current. Also, the maximum diode voltage drop during conduction was tabulated as 1.5 volts. Therefore, since the logic signal was chosen to be a 0 or 5 volt signal, R, the resistor to buffer the logic signal, was calculated as:

$$R = (5 - 1.5)\ V\ /\ 6mA = 583\ \Omega$$

Therefore, a 560 ohm resistor was used because it was the closest conservative value resistor available.

3.2 Lower Darlington Switch Design

The lower two switches have drive circuitry as shown in Figure 3.3. As in the upper Darlington, the desired base current to ensure saturation of the lower Darlington is 100 milliamps. The maximum value of the base to emitter voltage of the Darlington is 3.5 volts. Therefore, when the Darlington is on, R_C needs to be:

$$R_C = (5 - 3.5)\ V\ /\ 100\ mA = 15\ \Omega$$

Recall that the saturated collector to emitter voltage of the 2N2222 is .4 volts; hence, when the Darlington is off, the collector current for the 2N2222

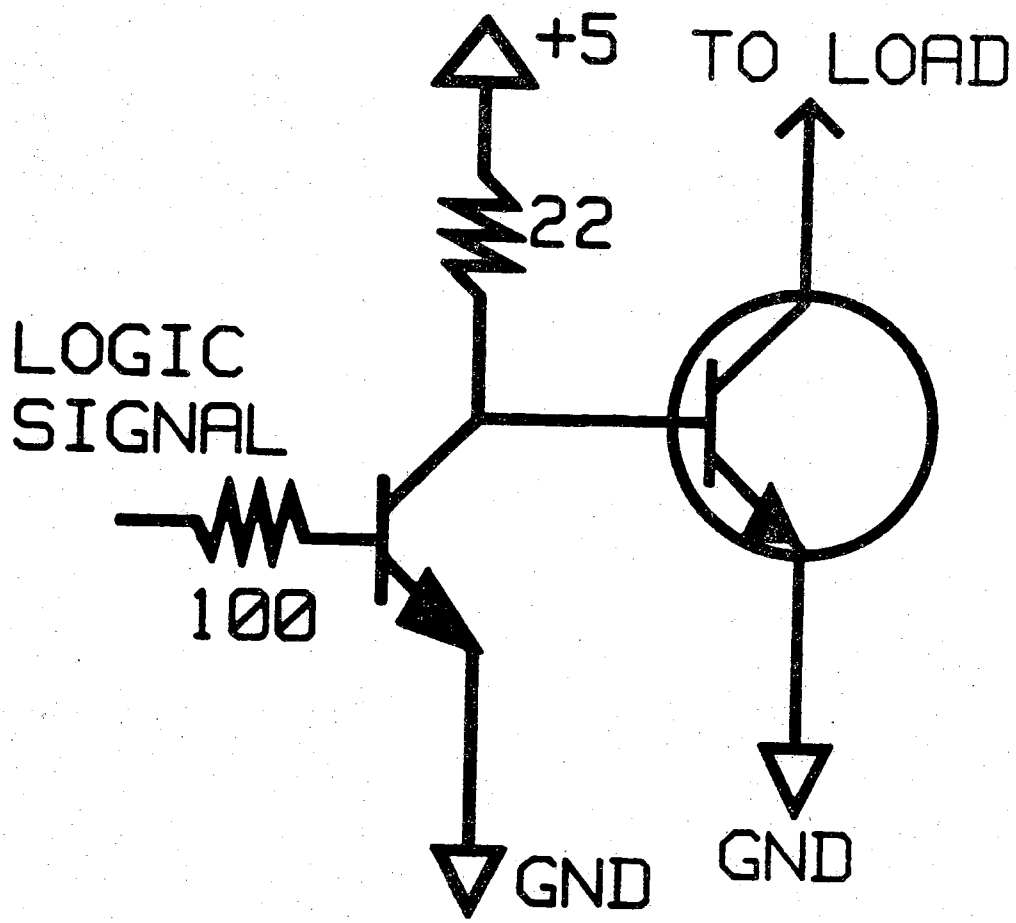

Figure 3.3. Lower Darlington Switch Drive Circuitry.

transistor is:

$$I_C = (5 - .4)\ V\ /\ 15\ \Omega = 307\ mA$$

The minimum beta for the 2N2222 is 30. Therefore, the minimum base current for the 2N2222 is:

$$I_B = 307\ mA\ /\ 30 = 10.2\ mA$$

To ensure saturation of the 2N2222, the base current was chosen to be 40 milliamps. Since the maximum base to emitter saturation voltage is 1.3 volts, the base resistance, R_B, is:

$$R_B = (5 - 1.3)\ V\ /\ 40\ mA = 92.5\ \Omega$$

Hence, R_B was chosen to be 100 ohms since this was a convenient obtainable value. Upon setting the circuit up and testing it, it was decided to use a 22 ohm resistor for the collector resistor because the 15 ohm resistor became extremely hot.

3.3 Pulse-Width Modulation Control Design

The circuitry which is responsible for producing the pulse-width modulated signal that is input to the four drive circuits is shown in Figure 3.4. In this circuit, the astable 555 block produces a clock frequency of 720 Hz. Its internal connections are shown in Figure 3.5. The value of the clock frequency, 720 Hz, was chosen arbitrarily. The total pulse width, T, is therefore 1/720. Desiring close to a 50% duty cycle for the clock pulse and using the following three equations,

$$t_1 = 0.693 * (R_A + R_B) * C_t$$

$$t_2 = 0.693 * (R_B) * C_t$$

$$T = 0.693 * (R_A + 2 * R_B) * C_t$$

values for R_A, R_B, and C_t can be calculated. These values are:

$$R_A = 2K$$

$$R_B = 39K$$

$$C_t = .025uF$$

The V_{CC} used was 5 volts and the .01uF capacitor was used to bypass noise. This 720 Hz is divided by 2 by the special hook-up of the JK Flip-flop.

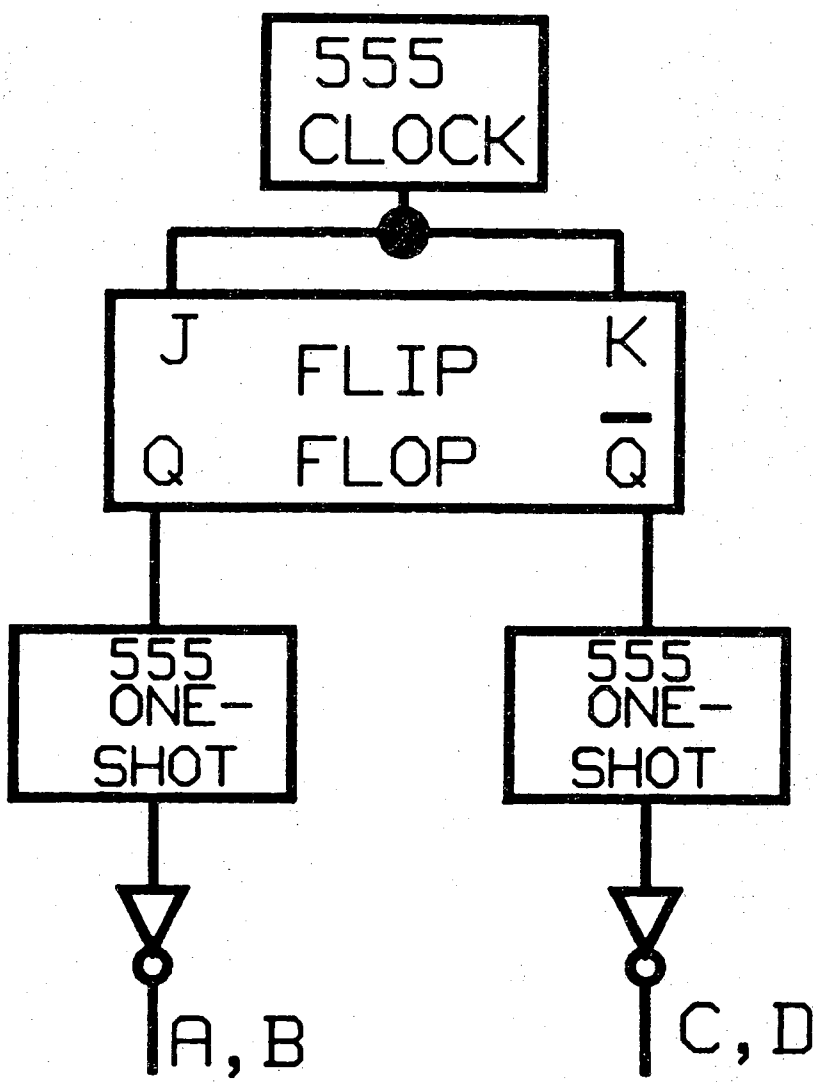

Figure 3.4. Pulse-Width Modulated Signal Generator Circuit.

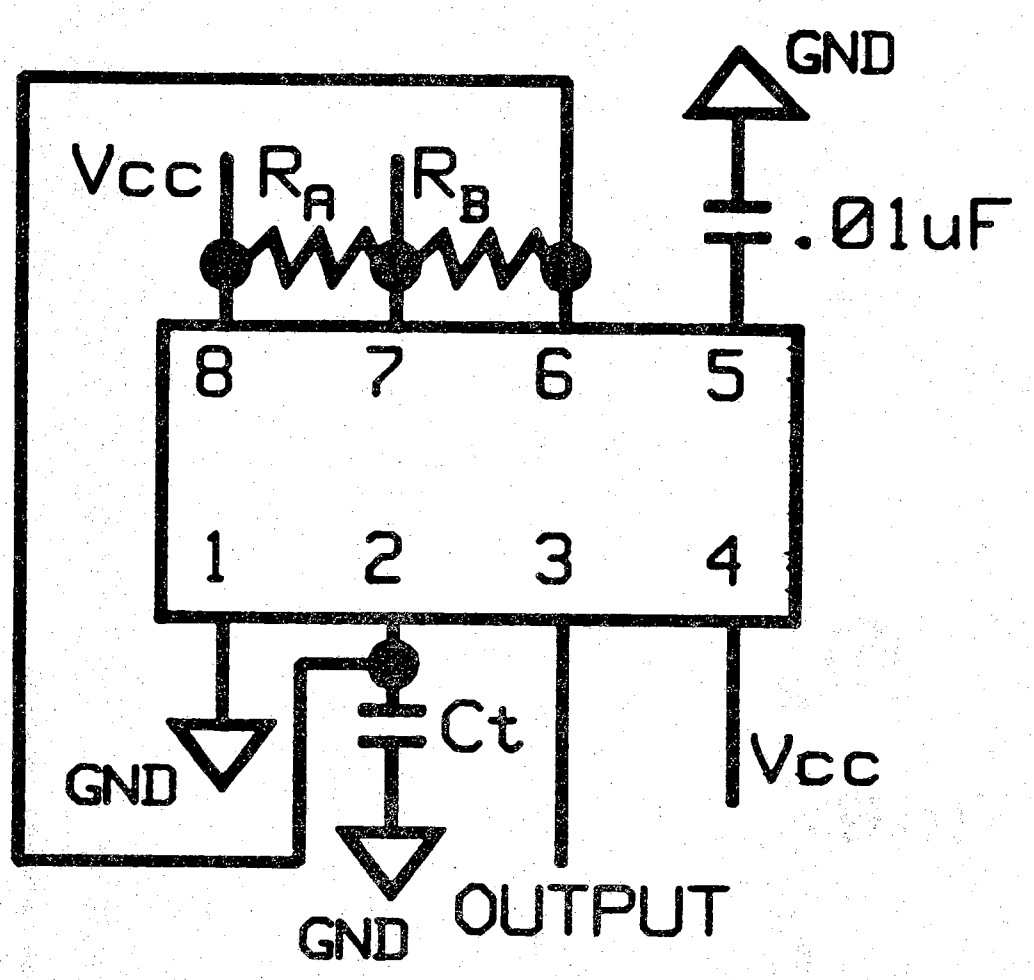

Figure 3.5. 555 Clock Connections For 720 Hz.

Therefore, a frequency of 360 Hz is input into each of the two identical one-shot 555 chips. The pulse width of the output of each one-shot 555 can be modulated by changing the potentiometer, R_t, in Figure 3.6. In the diagram, C_t was chosen arbitrarily as 1uF and the range that R_t must have to vary the duty cycle from 50 to 100% was calculated. The equation used was:

$$T = 1.1 * R_t * C_t$$

This range of R_t was around 1.2K for 50% duty cycle to around 2.5K for 100% duty cycle. Hence, a 10K potentiometer was used for R_t. Again the .01uF capacitor is used to filter out noise and V_{CC} was 5 volts. The value of the load resistor, R_L, was chosen arbitrarily as 10K. Each 50 to 100% duty cycle from both 555 one-shot devices is inverted to produce two 0 to 50% duty cycle pulses. Note that these two pulse-width modulated signals are 180 degrees out of phase. The output pulse from the left one-shot 555 is sent to the drives for Darlingtons A and B. Likewise, the output pulse from the right one-shot 555 is sent to the drives for Darlingtons C and D. This design will ensure that at any time either only Darlingtons A and D are switching or only Darlingtons B and C are switching or that all of the Darlingtons are off. For example, let us consider a pulse-width modulated signal with a 5% duty cycle coming out of both one-shot 555 timers' inverters. The timing for such a scenario is shown in Figure 3.7. Initially, the signals from both 555s are low and Darlingtons A and C are definitely off, while the same low signals cause Darlingtons B and D to be potentially on. That is, they would be on if there was a positive collector to emitter voltage presently across them; however, since both A and C are definitely off there exists no such positive voltage across B or D and they are presently off. When the left 555's signal goes high for its 5% duty cycle, this causes a high signal to be sent to Darlington A's drive circuitry causing A to switch on. At the same time, this 5% duty cycle signal causes Darlington B to be definitely off while A is on. However, Darlington D is still potentially on since a low signal from the right 555 is still applied to its drive circuitry. Hence, because A turns on, it now has a positive collector to emitter voltage across it and turns on. Darlington C is still off since its drive still receives a low signal. Hence, A and D are on providing a current path through the load, while B and C are off. Later, when the right 555's signal goes high for its 5% duty cycle with the left 555's signal low, Darlingtons B and C are on providing current through the load in the opposite direction, while Darlingtons A and D are off. Hence, it is impossible for any designed combination of the Darlingtons to be on that would short out the

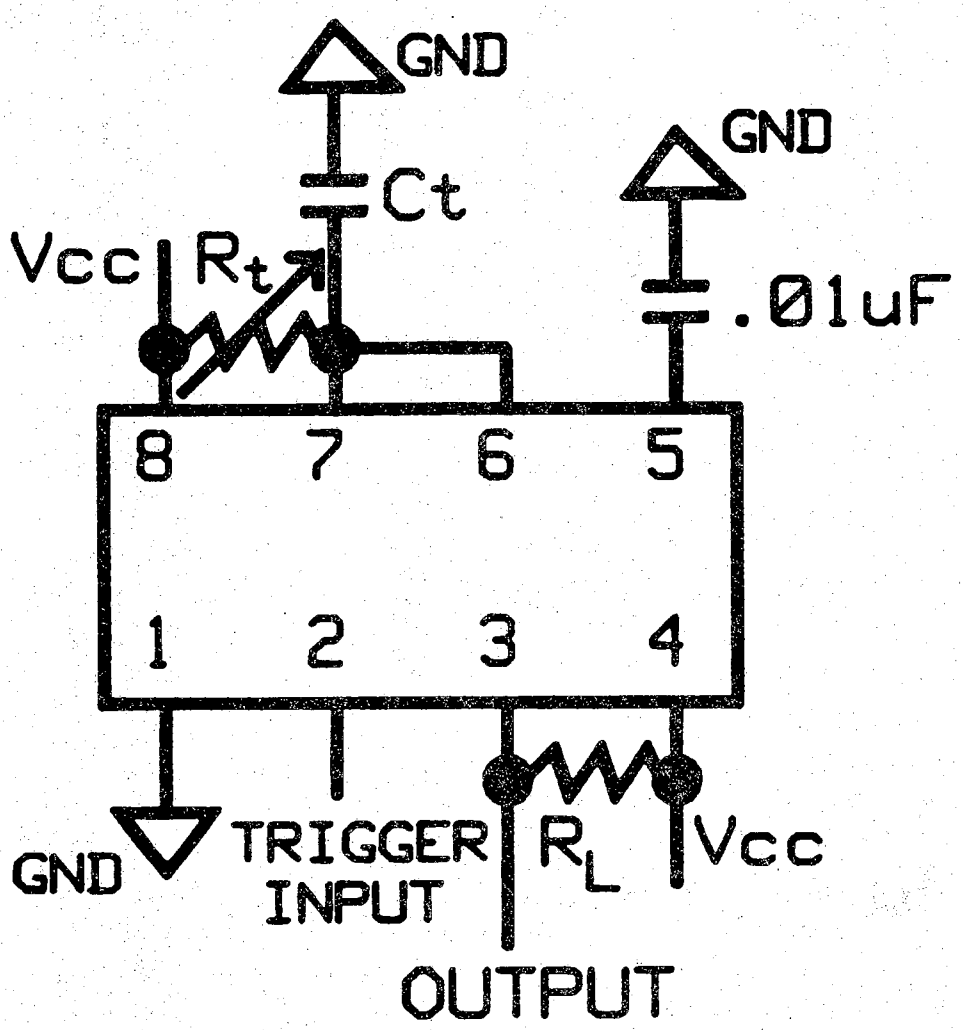

Figure 3.6. 555 One-Shot Connections.

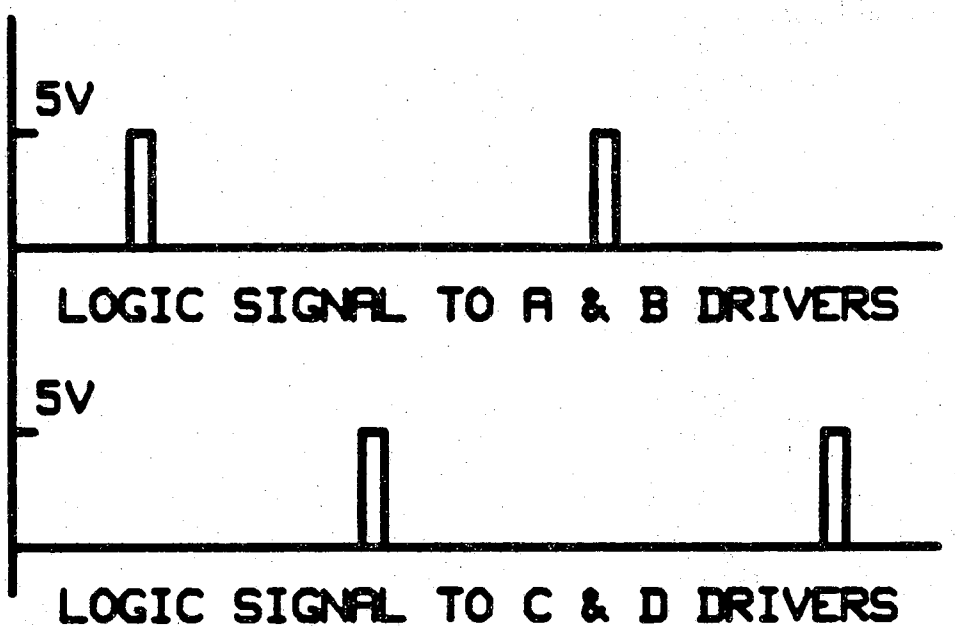

Figure 3.7. Timing for 5% Duty Cycle.

direct current voltage source.

3.4 Testing Initial PWM Control Design

After connecting the Pulse-Width Modulated Signal Generator circuit to the four driver circuits and integrating these with the four Darlingtons, the single-phase inverter was tested with a 6.3 ohm, 55 watt, wire-wound resistor as the load. The load current was observed on an oscilloscope using a Tektronix A6302 current probe. The duty cycle of the square PWM signal was set at approximately 5% and therefore load current was expected to flow positively for 5% duty cycle and negatively for 5% duty cycle. The load current was expected to be zero the rest of the time.

Darlingtons A and D did indeed conduct current at the same time. However, Darlington A stayed on after D turned off; this happened because at this time B was potentially on and turned on because of stored charge in the pn junctions of A's driver escaped through B. Therefore, the single-phase inverter was shorted through A and B until C turned on. Then C and B conducted for the 5% duty cycle they were expected to. However, Darlington C stayed on after B turned off because of the charge stored in the pn junctions of its driver. This charge shorted the single-phase inverter through D because D became potentially on due to the low logic signal sent to its driver. This malfunction was observed consistently for all values of V_{DC} from 20 volts to 40 volts. In summary, the single-phase inverter was on when it was supposed to be, but was shorting the voltage source when it was supposed to carry no current. Fortunately, the voltage source used was current limited.

3.5 Final PWM Control Design

To alleviate the problem of Darlingtons A and C staying on due to stored charge, two resistors were added to their drive circuits. As shown in Figure 3.8, these resistors will provide an escape path to ground for the stored charge in the pn junctions of the optocoupler and the 2N2222 drive transistor. In addition, to positively assure that no shorting through of the DC source will occur, the logic signals to switch the driver circuits were slightly changed. They were taken from different points of the Pulse-Width Modulated Signal Generator Circuit as shown in Figure 3.9. This new set of logic signals is shown in Figure 3.10 for the case when current flows through the load 5% of the time in each direction. Under this scheme, the logic signal to the Darlington D driver would be a 95% duty cycle square wave from the left 555

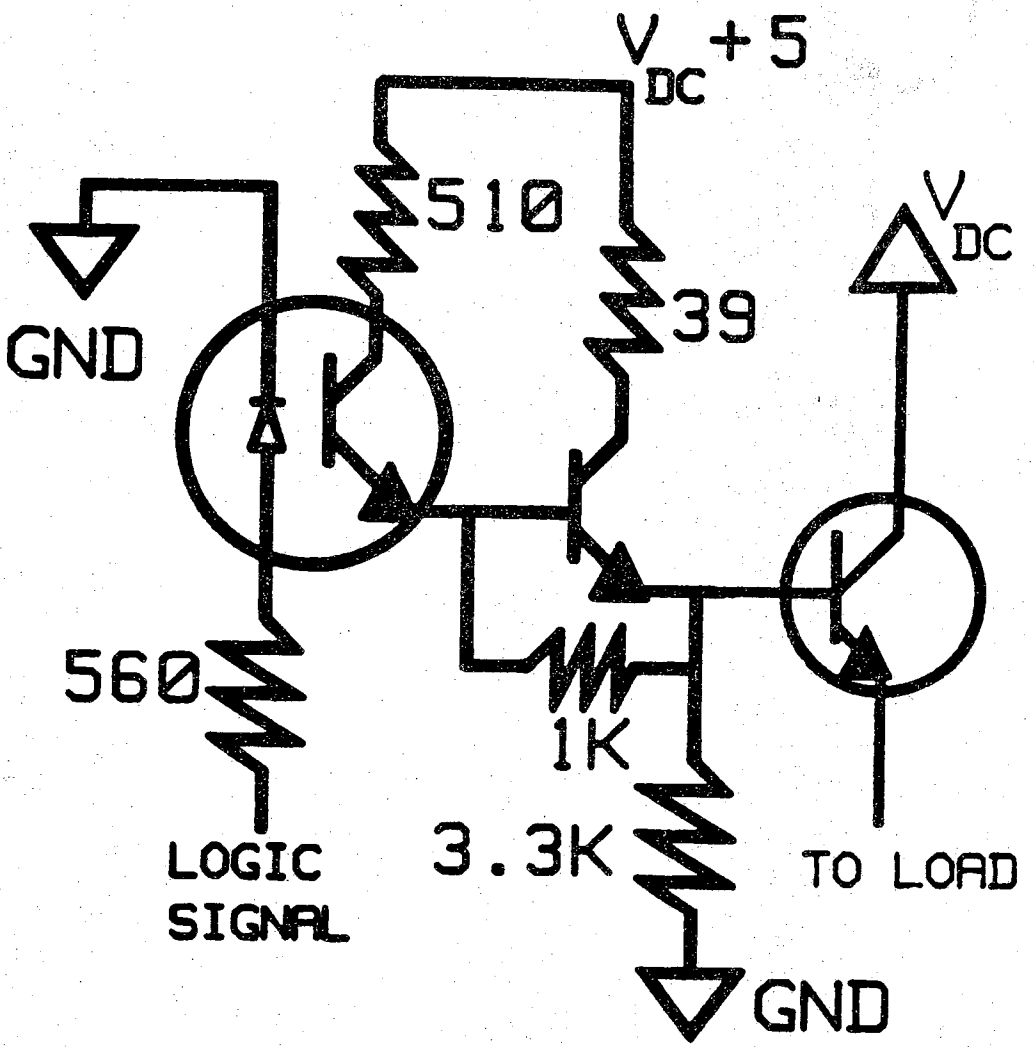

Figure 3.8. Updated Upper Darlington Switch Drive Circuitry.

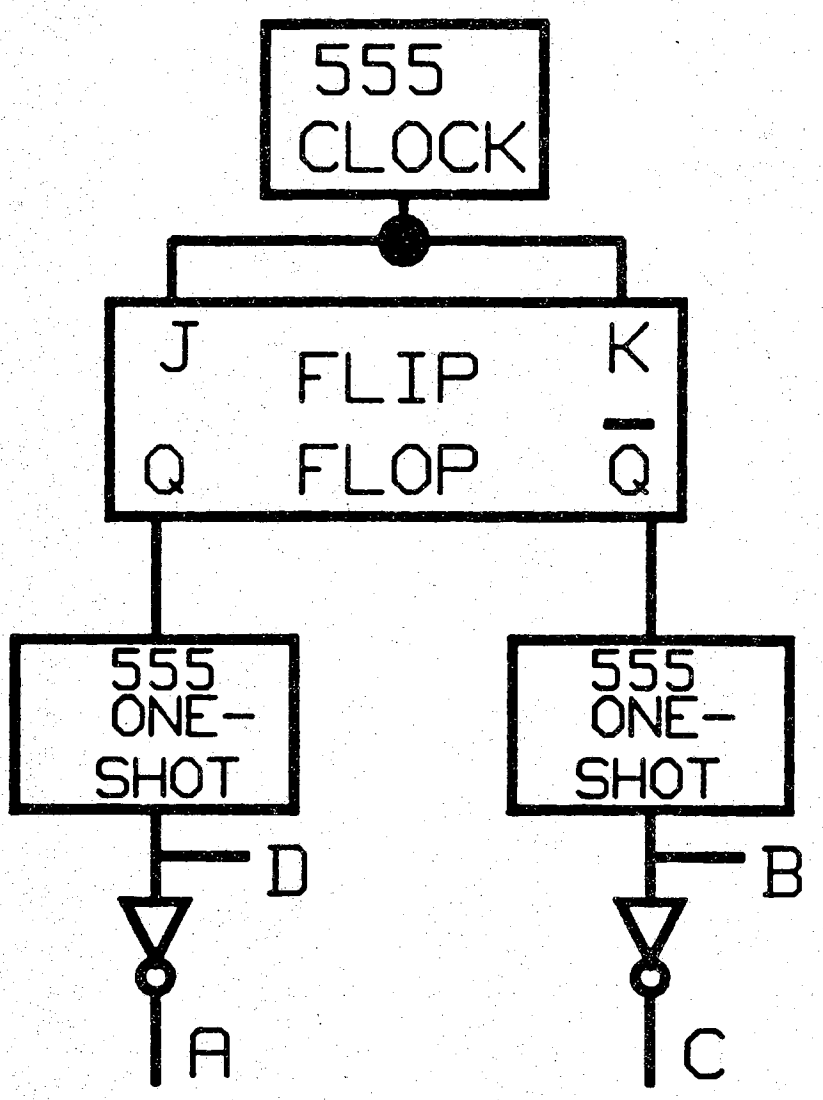

Figure 3.9. Final Pulse-Width Signal Generator Circuit.

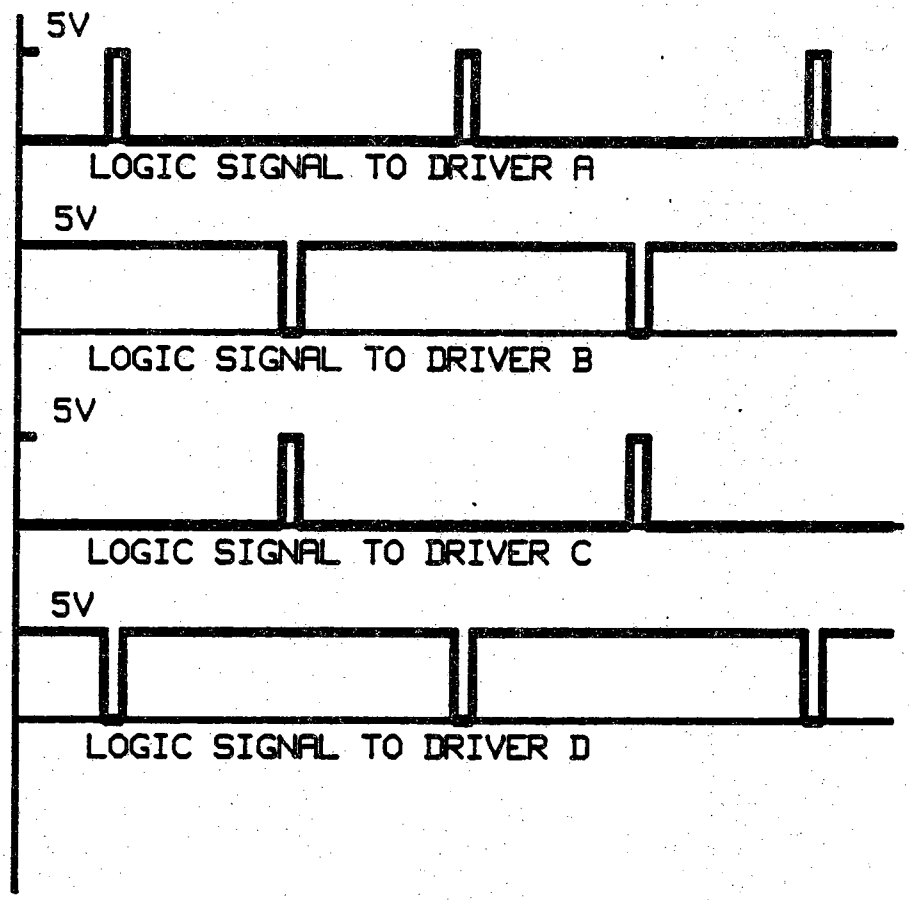

Figure 3.10. Final Timing for 5% Duty Cycle.

one-shot timer. It would turn Darlington D on only when low. As noted in the diagram, the logic signal to the A driver is the inverted logic signal of the logic signal to the D driver. This logic signal to the A driver would only turn A on when high. Hence, Darlingtons A and D would be on simultaneously and conducting current through the load only 5% of the time, as determined by the duty cycle. Also, due to the similarity of the logic signals for the B and C drivers to those for the A and D drivers, current will flow through the load in the opposite direction only 5% of the time. Upon testing with the same 6.3 ohm wire-wound resistor load, single-phase inverter operation was successful.

CHAPTER 4

OPERATION OF THE SINGLE-PHASE INVERTER

Upon successful testing of the single phase inverter, it was decided to document and comment on some of the results.

4.1 Purely Resistive Load Operation

In the circuit of Figure 4.1, a 6.3 ohm, 55 watt, wire-wound resistor was initially used for the load. The maximum allowed rms current was:

$$I_{rms} = (55\ W\ /\ 6.3\ \Omega\ )^{1/2} = 2.95\ A$$

Therefore, 2.5 amps was chosen as a convenient round conservative amount of peak current to be run through the load. V_{DC} needed to be set at 9.5 volts to obtain this amount of current. The duty cycle was set at approximately 20%. In Figure 4.2 the base voltage is shown for Darlington D on the top and Darlington B on the bottom. The photographs were taken with a Tektronix C-5C oscilloscope camera with the y-axis of the oscilloscope set at .5 volts per division and the x-axis set at .5 milliseconds per division. It shows that when the base voltage for one of the two lower Darlingtons is high, that Darlington is on and conducting current. When one of these lower Darlingtons is off, its base voltage, which is the collector voltage of its 2N2222 transistor driver, is around .2 volts. This demonstrates that its 2N2222 transistor driver is indeed saturated as desired. In Figure 4.3, the base voltage is shown for Darlington A on top and Darlington C on bottom. The x-axis was set at .5 milliseconds per division and the y-axis was set at 5 volts per division. Again it is shown that one of the upper Darlingtons has a high base voltage when it is on and conducting current. Since the two photos of Figure 4.2 and Figure 4.3 are referenced to the same time, it should be noted that Darlingtons A and D conduct at the same 20% duty cycle as do Darlingtons C and B. Note also that each set of Darlingtons conducts 180 electrical degrees out-of-phase with each other. This fact is equally demonstrated by comparing Figure 4.4, where I_A or I_D is shown, to Figure 4.5 where I_C or I_B is shown. These currents were

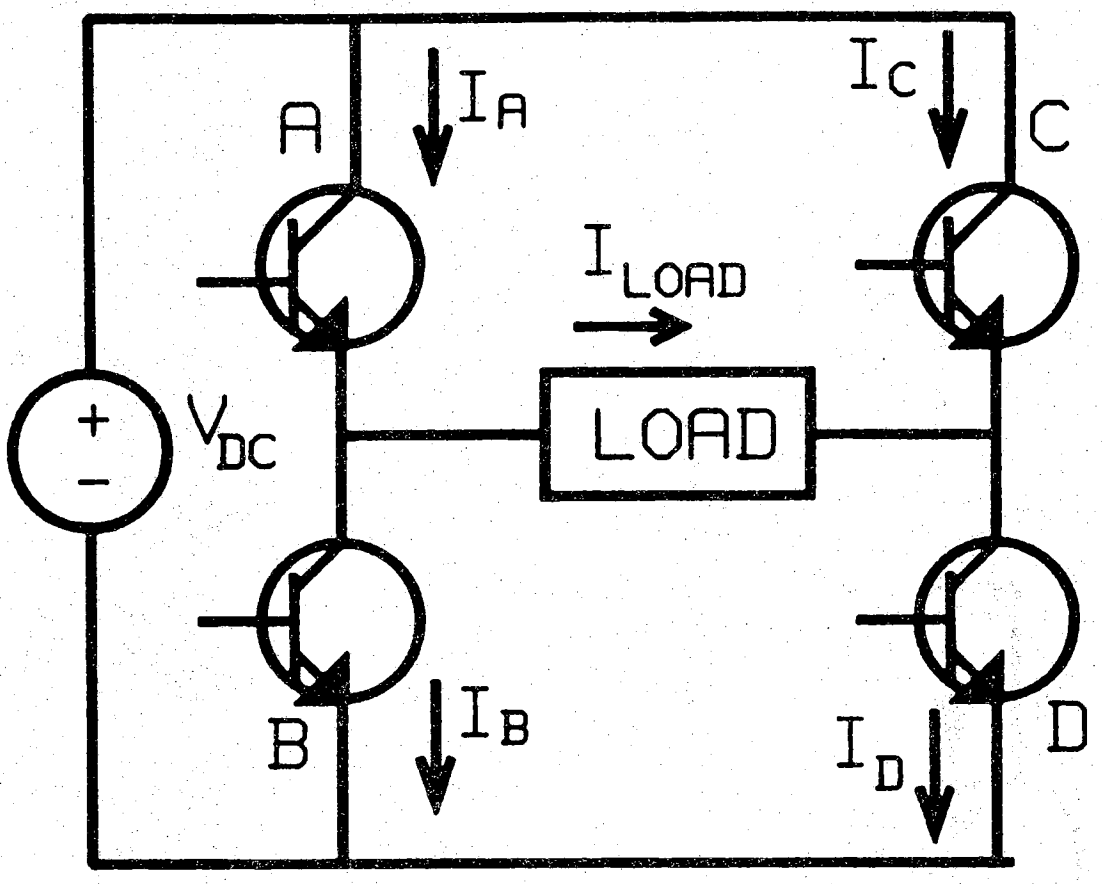

Figure 4.1. Single-Phase Inverter Circuit.

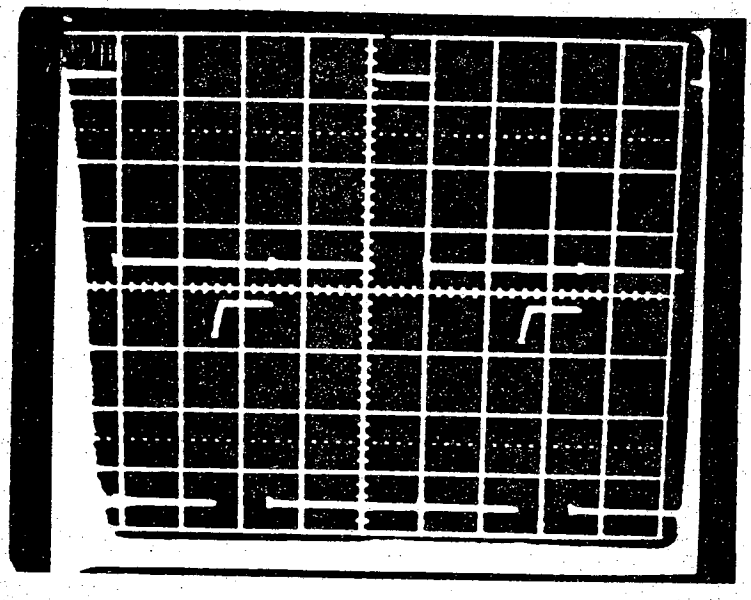

Figure 4.2. Lower Darlington Base Voltages.

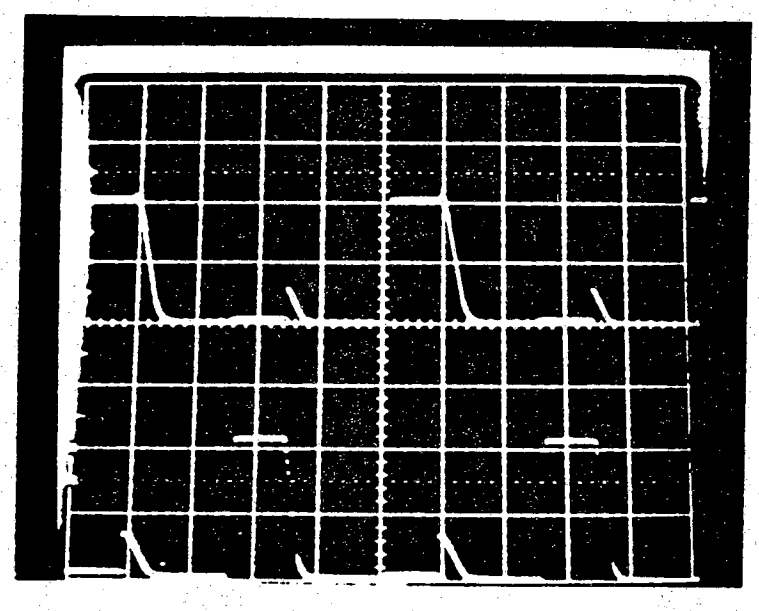

Figure 4.3. Upper Darlington Base Voltages.

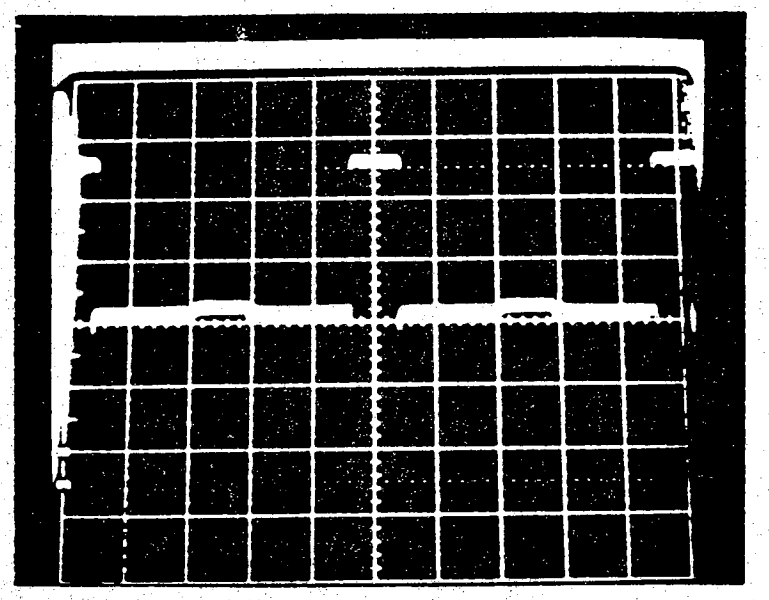

Figure 4.4. Current through Darlingtons A and D.

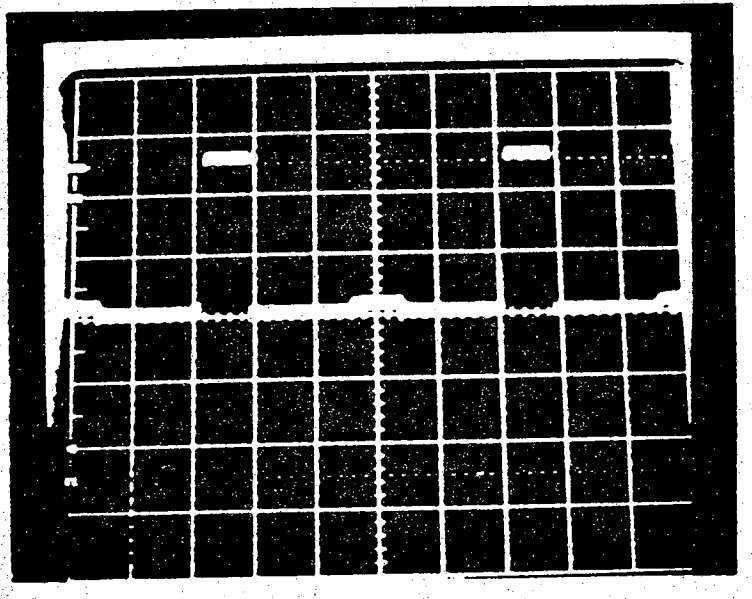

Figure 4.5. Current through Darlingtons C and B.

measured with a Tektronix A6302 current probe which sent its readings to the oscilloscope at 1 amp per division. Hence, the peak-to-ground current was 2.5 amps. A Kirchhoff Current Law analysis at the node to the left of the load will show:

$$I_{LOAD} = I_A - I_B$$

This can be visually demonstrated if one mentally inverts I_B in Figure 4.5 and adds it to I_A in Figure 4.4. The result is the load current, I_{LOAD}, shown in Figure 4.6. Hence, a fairly symmetrical alternating waveform was obtained for a purely resistive load using single-phase iverter operation.

Table 4.1 displays the turn-on times and turn-off times for the four Darlingtons. These were measured with the delayed sweep mode of the oscilloscope under the above load and current conditions. From this data, it can be seen that the lower Darlingtons, B and D, turn off extremely fast. The reason that the upper Darlingtons, A and C, turn off slower is that they have to dissipate the charge in the pn junction of their respective optocoupler, which is slow in forthcoming. The discrepancy in turn-on times between the A and D Darlington set and the B and C Darlington set is conjectured as being a result of mere small internal device differences. However, the main result is that the optocoupler is the device that limits overall switching time. Because turn-off time for two of the Darlingtons is greater than any of the turn-on times, current can be conducted in either direction only close to 50% of the cycle.

4.2 RL Load Operation

Next, a 2.1 millihenry inductor was placed in series with the 6.3 ohm resistor to simulate a RL load. Since the switching frequency was 360 hertz, one would expect the following inductance:

$$X_L = 2 * \pi * 360\ \text{Hz} * (2.1\text{E}{-3}\ \text{H}) = 4.75\ \Omega$$

The magnitude of the total load impedance is:

$$Z_{LOAD} = ((4.75)^2 + (6.3)^2\ )^{1/2} = 7.89\ \Omega$$

The phase angle of the total load impedance is:

$$\phi = \arctan(4.75\ /\ 6.3) = 37.0^\circ$$

Hence, the phase delay of the current should be 37 degrees behind the switching voltage across a set of the Darlingtons. The base voltage is shown on top of Figure 4.7 for Darlington D and on the bottom for Darlington B. It

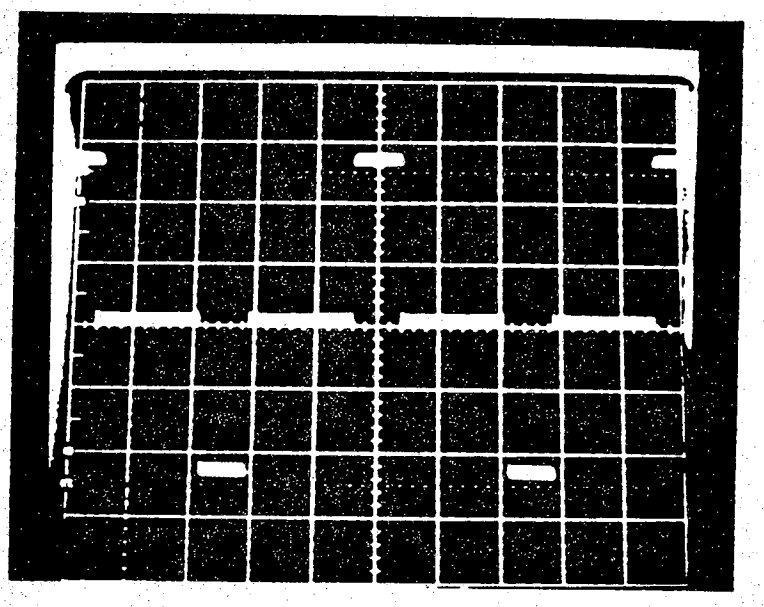

Figure 4.6. Load Current with Purely Resistive Load.

Table 4.1. Darlington Turn-on and Turn-off Times for Purely Resistive Load.

	Turn-on Time (us)	Turn-off Time (us)
Darlington A	22	275
Darlington B	70	1
Darlington C	72	200
Darlington D	15	1

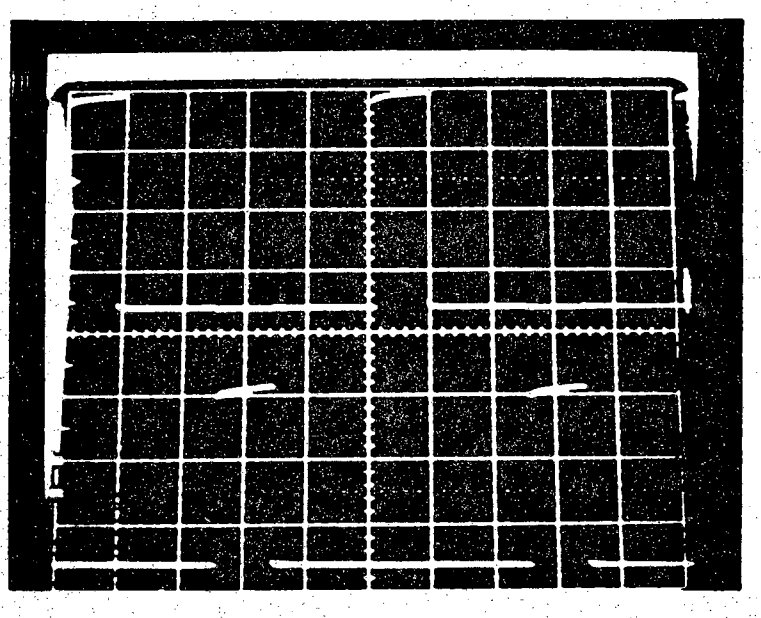

Figure 4.7. Lower Darlington Base Voltages with RL Load.

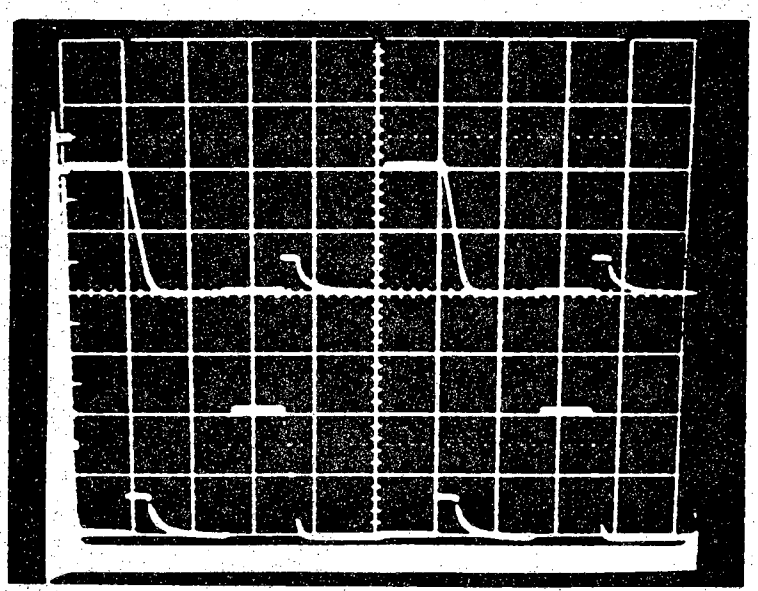

Figure 4.8. Upper Darlington Base Voltages with RL Load.

can be seen that these Darlingtons' turn-off times are barely affected by the addition of the inductor. However, Figure 4.8 shows how slow Darlington A on top and Darlington C on the bottom turn off. The data is summarized below in Table 4.2. Figure 4.9 shows the load current, I_{LOAD}, with the RL load. With the same V_{DC} of 9.5 volts as before, the peak current is around .42 amps. Since each Darlington has a maximum collector to emitter voltage of 2.8 volts, this value of load peak current is not too far from the following calculated value:

$$I_{LOAD} = (9.5 - 2 * (2.8))\ V\ /\ 7.89\ \Omega = .49\ A$$

The load current is not a square wave as before because the inductor delays the current and smooths it out.

Table 4.2. Darlington Turn-on and Turn-off Times for a RL Load.

	Turn-on Time (us)	Turn-off Time (us)
Darlington A	21	225
Darlington B	1	1
Darlington C	70	175
Darlington D	1	1

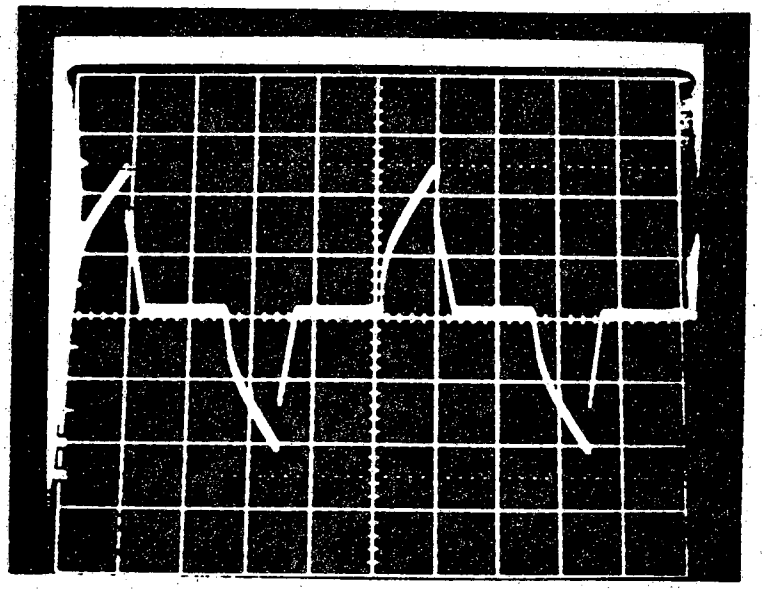

Figure 4.9. Load Current with RL Load.

CHAPTER 5

DESIGN OF THE THREE-PHASE INVERTER CONTROLS

After demonstrating single-phase inverter operation, the three-phase inverter was constructed as shown in Figure 5.1 [3].

5.1 Three-Phase Circuit Drivers

An Upper Darlington Drive Switch Circuit as shown in Figure 3.8 was used for each of the upper Darlingtons T1, T3, and T5. However, a Lower Darlington Drive Switch Circuit as shown in Figure 5.2 was used for each of the lower Darlingtons T2, T4, and T6. The design of the logic signals to drive the three-phase inverter is the subject of this chapter. The overall block diagram for such a design is shown in Figure 5.3.

5.2 Logic Signal Controller Description

First of all, the clock is a 555 used in the astable mode and is hooked up according to Figure 5.4. A 360 hertz clock frequency was desired so that it could be arranged for each Darlington to turn on 60 times per second. Theoretically, this should produce an output voltage of 60 hertz. Desiring close to a 50% duty cycle for the clock pulse and using the same equations as used in Chapter 3, namely,

$$t_1 = 0.693 * (R_A + R_B) * C_t$$

$$t_2 = 0.693 * (R_B) * C_t$$

$$T = 0.693 * (R_A + 2 * R_B) * C_t$$

values for R_A, R_B, and C_t were calculated. The values used were:

$$R_A = 2K$$

$$R_B = 39K$$

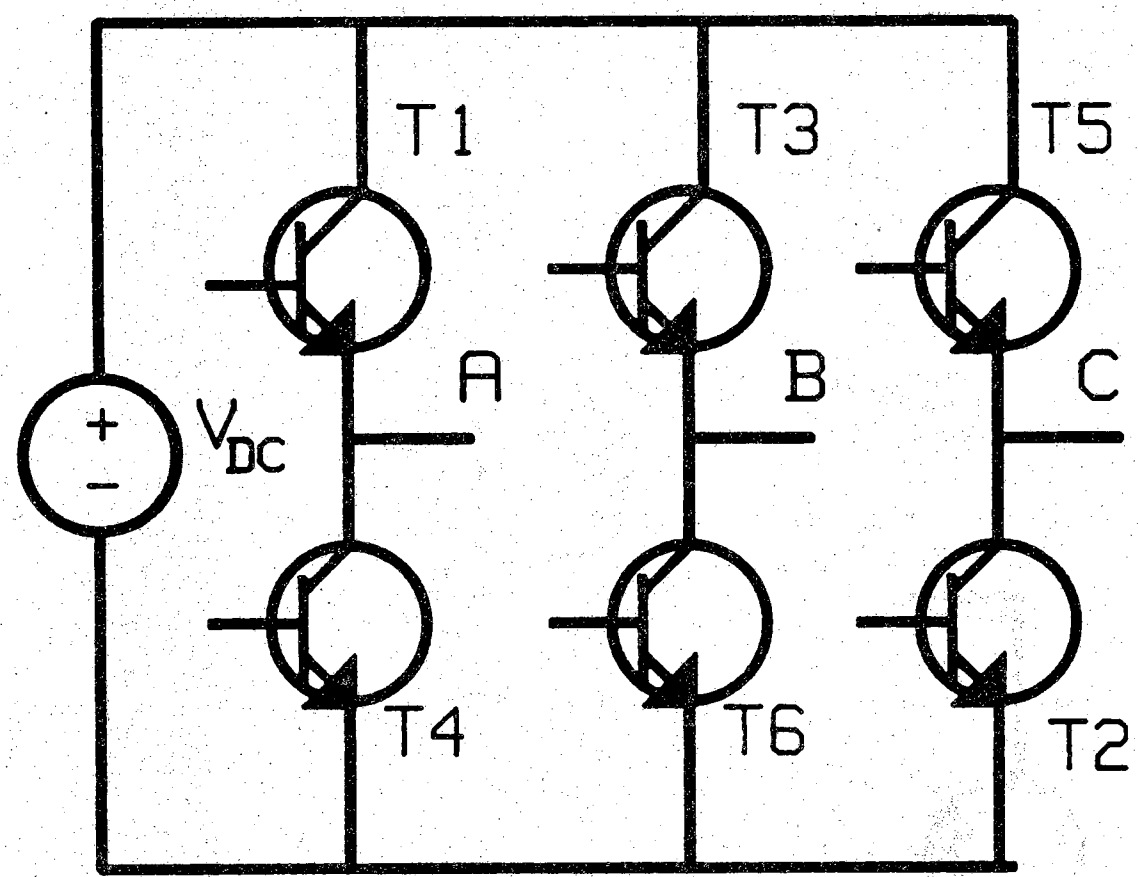

Figure 5.1. Three-Phase Inverter.

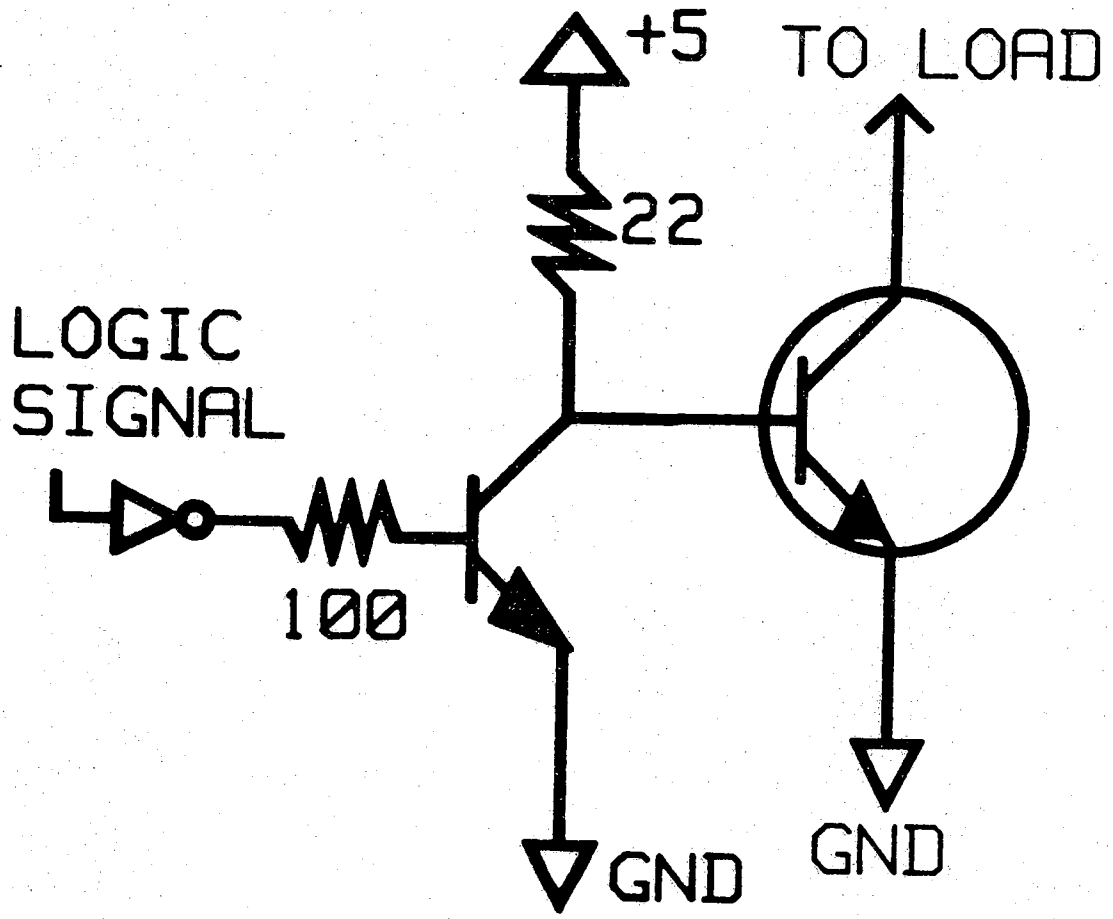

Figure 5.2. Lower Darlington Drive Switch Circuit.

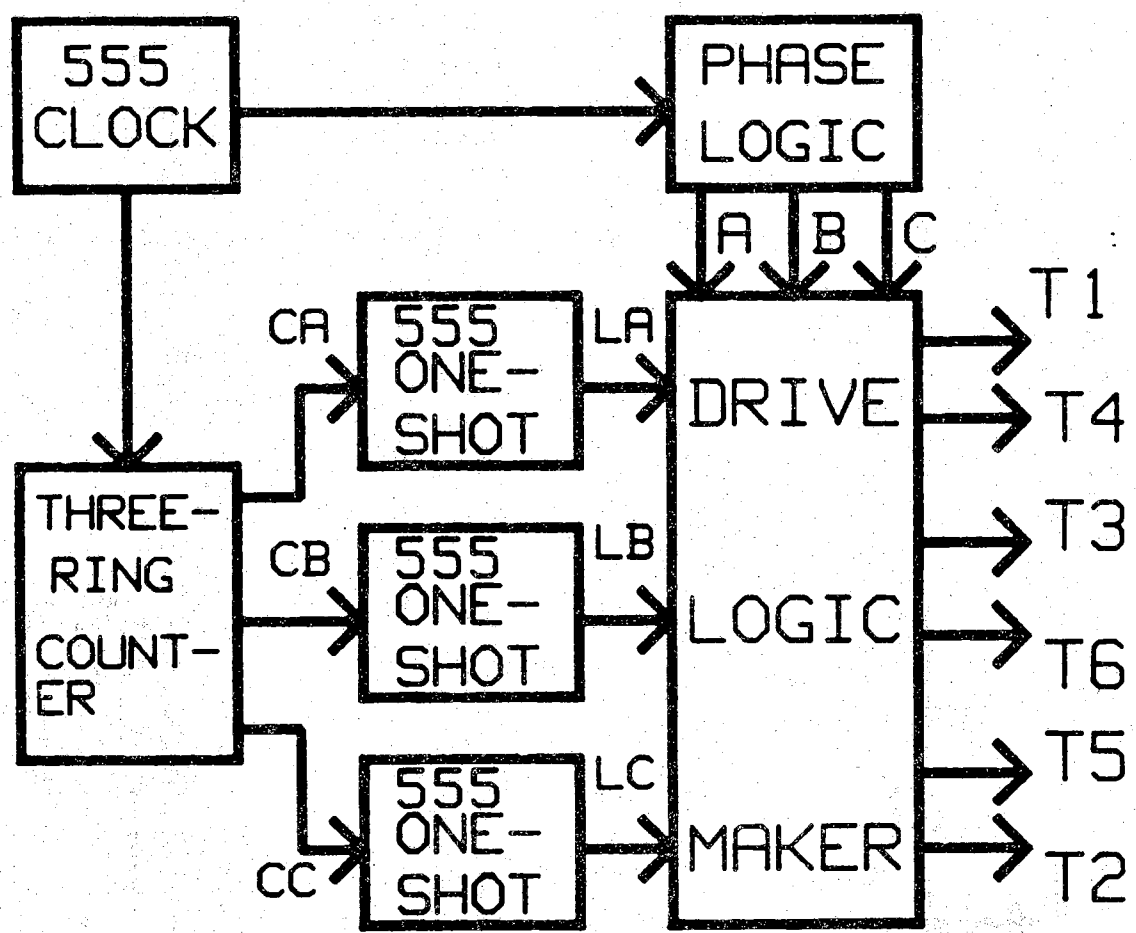

Figure 5.3. Logic Signal Controller.

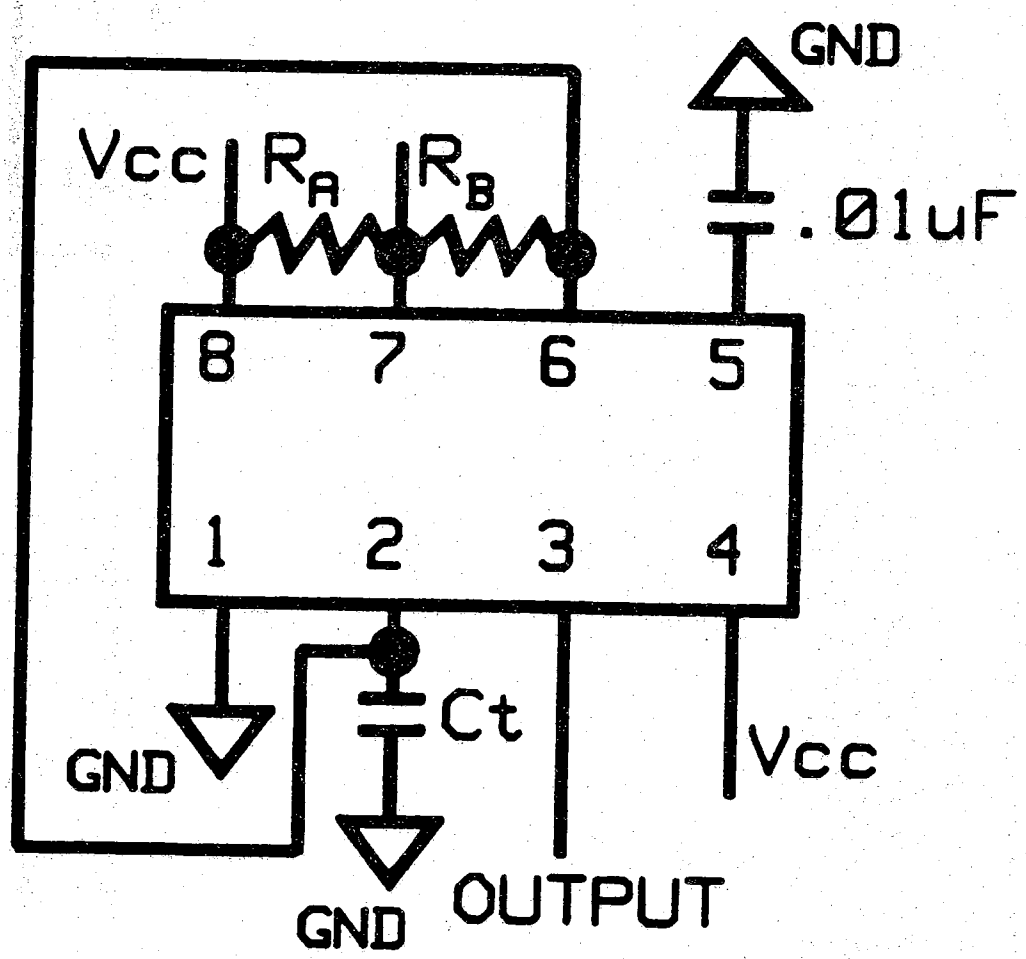

Figure 5.4. 555 Clock Connections For 360 Hz.

$$C_t = 0.025uF$$

Once again, the dc supply voltage, V_{CC}, was 5 volts and a .01 microfarad bypass capacitor was used to bypass noise.

5.2.1 Three-Ring Counter and 555 One-Shot Timers

The three-ring counter block is shown in Figure 5.5. As illustrated, it is composed of 2 JK Flip Flops and 3 Two-Input AND gates. The input to it is the 360 hertz clock pulse and it outputs 3 signals: CA, CB, and CC. Each one of these signals is a 120 hertz signal and each one goes to a 555 one-shot timer. Each one-shot timer is triggered on the falling edge of the three-ring counter output signals. It is desired for each 555 to produce an output signal that varies from 67% to 100% in duty cycle. This is desired so that three-phase inverter operation can have either two or three Darlingtons on at any time. Therefore, each of the one-shot 555 timers had a circuit diagram as shown in Figure 5.6; C_t was chosen as .1 microfarads and the value of R_t was calculated using the equation:

$$R_t = T / ((1.1) * C_t)$$

The value of R_t for a 67% duty cycle was around 5.1K and for a 100% duty cycle was 7.5K. In constructing the 555 circuits, a decade resistance box was used for each R_t so that the duty cycle could be varied from 67% to 100% as desired. Therefore, the outputs of the 555 one-shot timers, LA, LB, and LC, are signals of 120 hertz with adjustable duty cycles [4]. The timing relationships between the clock, the output signals of the three-ring counter, and the outputs of the three 555s are shown in Figure 5.7. In this diagram, LA, LB, and LC are shown with a 67% duty cycle.

5.2.2 Phase Logic Block

In the overall block diagram of the driver logic signals, the 360 hertz clock signal also goes to the Phase Logic block. The first part of this block receives the clock signal and is shown in Figure 5.8. It is a six state ring-counter that takes the 360 hertz clock signal and has six states, R1 through R6, each which produces a signal at 60 hertz [5]. As shown, 3 JK Flip Flops, 6 Three-Input NAND gates, and 1 Two-Input AND gate were used in constructing it. The second part of the Phase Logic block is shown in Figure 5.9. This part is composed of 3 Three-Input NAND gates that combine some of the states of the six state ring-counter to produce the phase signals, A, B,

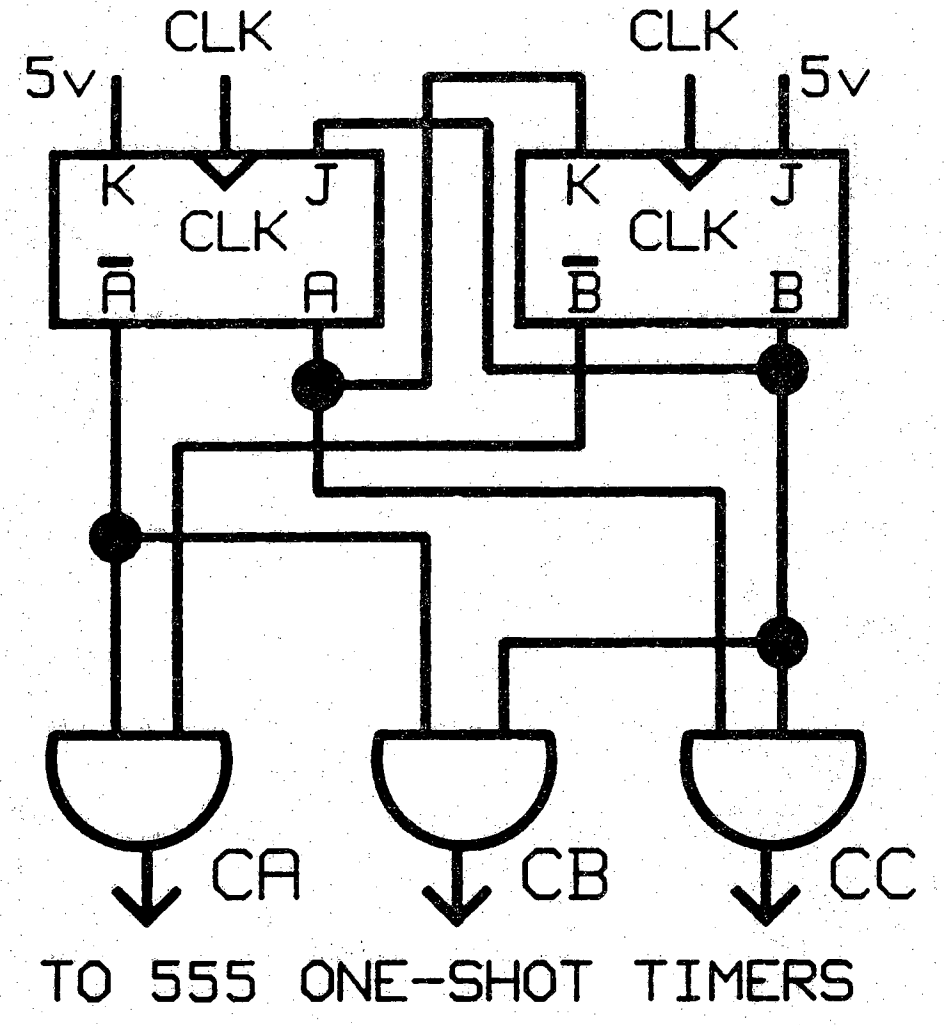

Figure 5.5. Three-Ring Counter.

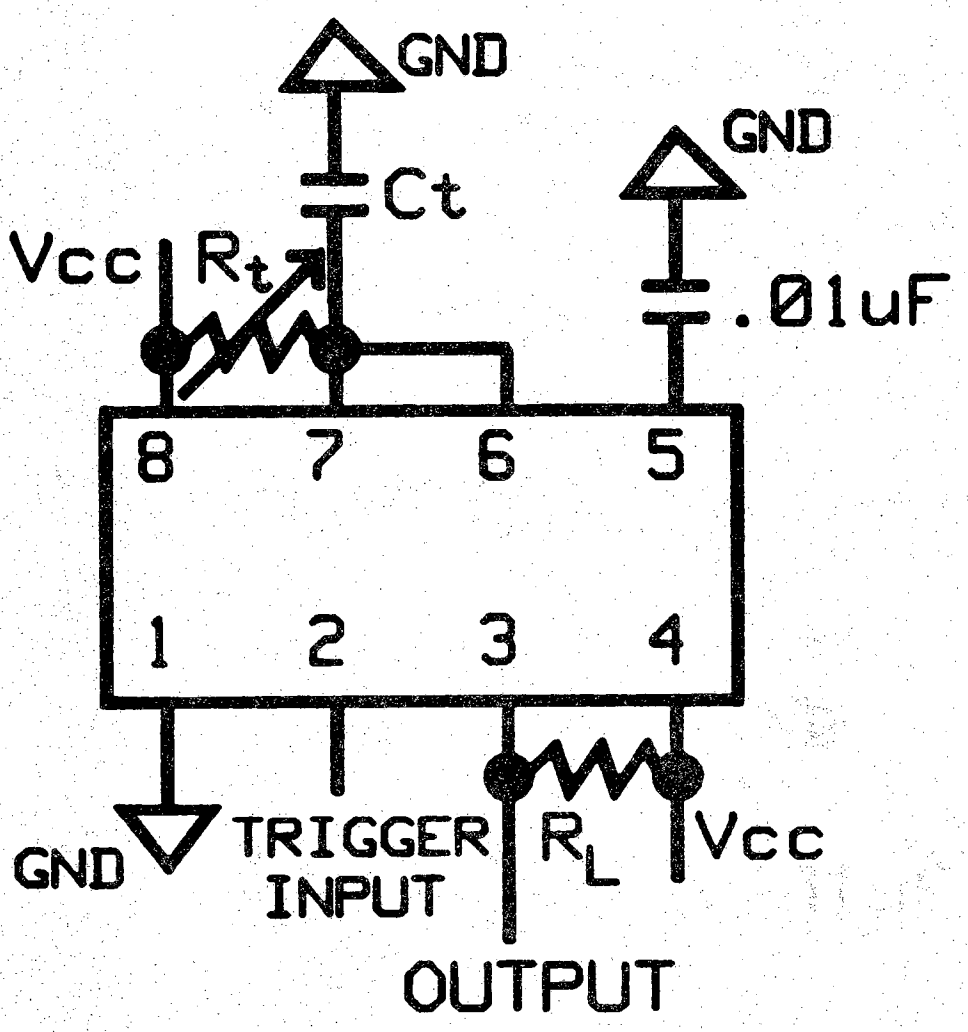

Figure 5.6. 555 One-Shot Timer Connections.

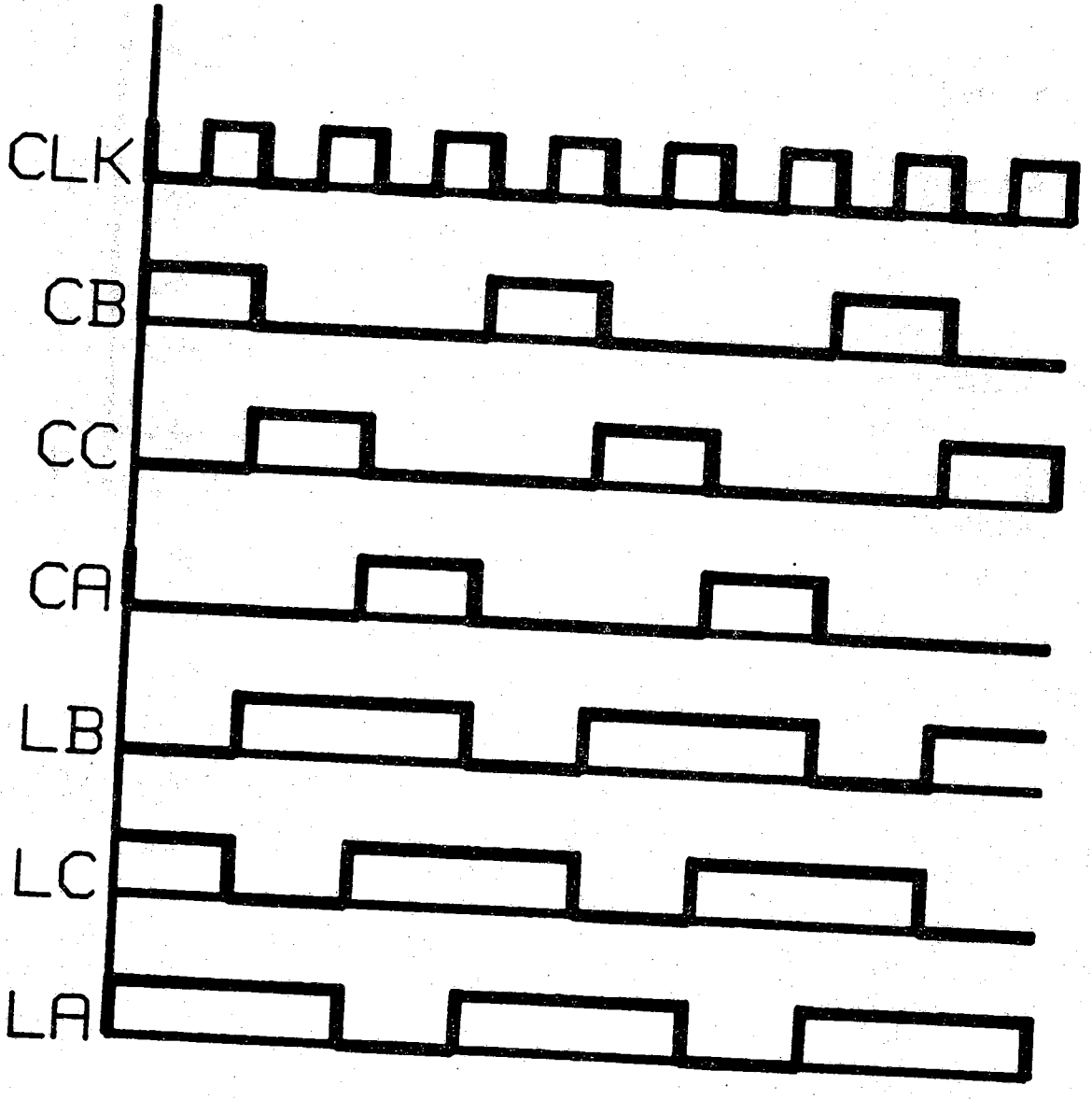

Figure 5.7. Timing Relationship for 555 Inputs and Outputs.

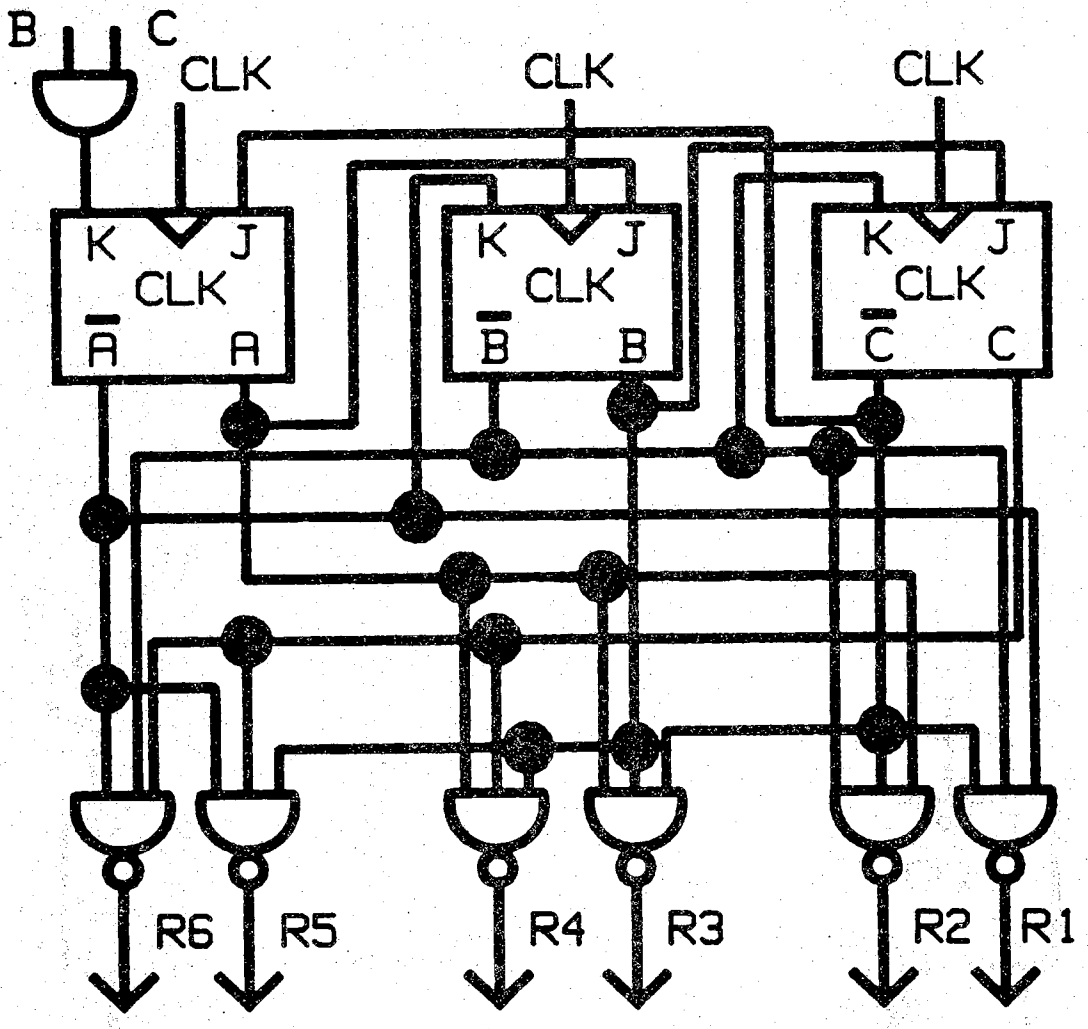

Figure 5.8. Six State Ring-Counter.

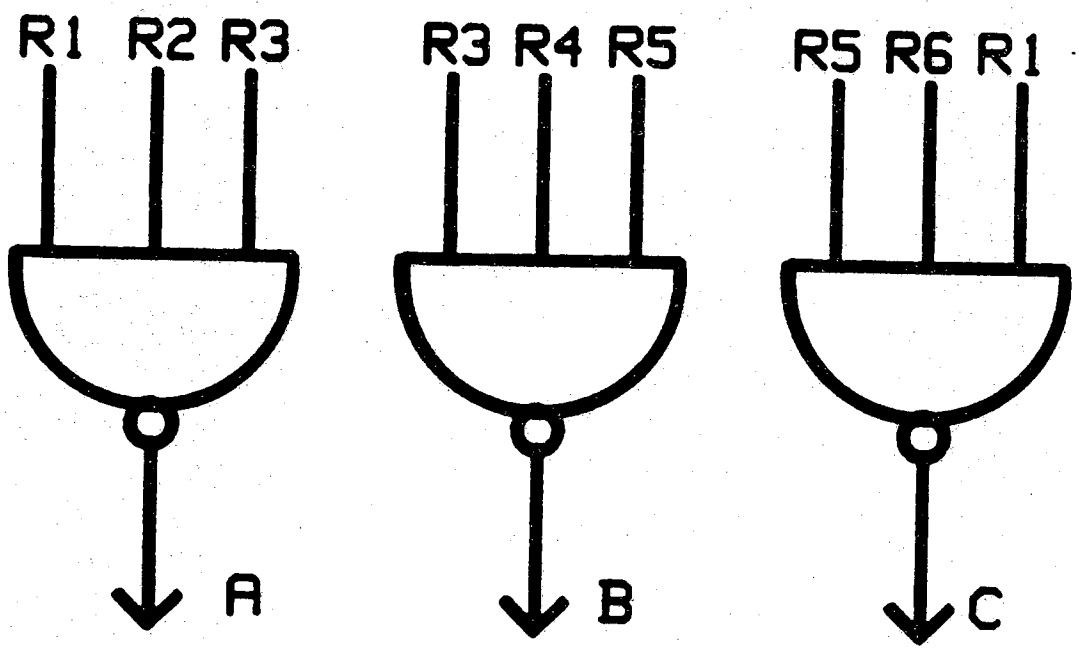

Figure 5.9. Combinational Logic.

and C. These signals are 120 degrees apart, have 50% duty cycles, and are 60 hertz square waves. The timing relationships between the clock, R1 through R6, and the phase signals are shown in Figure 5.10.

5.2.3 Drive Logic Maker

The Drive Logic Maker block accepts signals LA, LB, and LC from the 555 one-shot timers and the signals A, B, and C from the Phase Logic block. It uses combinational to form T1 through T6, the signals that turn on the Darlingtons in sequence and keep them on for the specified amount of time. The combination logic that makes up the Drive Logic Maker block is shown in Figure 5.11. The signals T1 through T6 produced by this block are shown in Figure 5.12. Note that since each Darlington is turned on by a 60 hertz signal, the output voltage across the three-phase load will also be a 60 hertz wave. Note also that each of the signals T1 through T6 is high for 120 electrical degrees. This is because LA, LB, and LC each have 67% duty cycles. Hence, Figure 5.12 was derived by mentally applying the combinational logic of the Drive Logic Maker block on the relevant signals in Figures 5.7 and 5.10. Since the signals T1 through T6 are high for 120 degrees of the cycle, this means that only two Darlingtons will be on at any given time. By increasing R_t of each 555 one-shot accordingly, the duty cycle of LA, LB, and LC can be increased; thereby, the Darlingtons stay on longer. If the Darlington turn-on signals, T1 through T6, are high anywhere greater than 120 degrees and less than 180 degrees, the three-phase inverter will alternate operating with three Darlingtons on for part of the cycle and only two Darlingtons on for the other part of the cycle. With the duty cycles of LA, LB, and LC set at 100% by adjusting their respective R_ts, each Darlington will be on 180 degrees of each cycle or on half of the time. Hence, three Darlingtons will be on at any given time. However, this mode of operation is undesirable because of the possibilities of shorting the DC source. That is, for example, if Darlingtons T2, T3, and T4 are on and T5 turns on quickly before T2 turns off completely, then V_{DC} will be short circuited. Nevertheless, functional control of the amount of time that the Darlingtons stay on can be theoretically achieved. Each Darlington can be on from 120 degrees to approximately 180 degrees of each electrical cycle. Thereby, the amount of output power can be adjusted from $(V_{DC})^2 / (2 * R_{LOAD})$ to $(2 / 3) * (V_{DC})^2 / R_{LOAD}$, respectively.

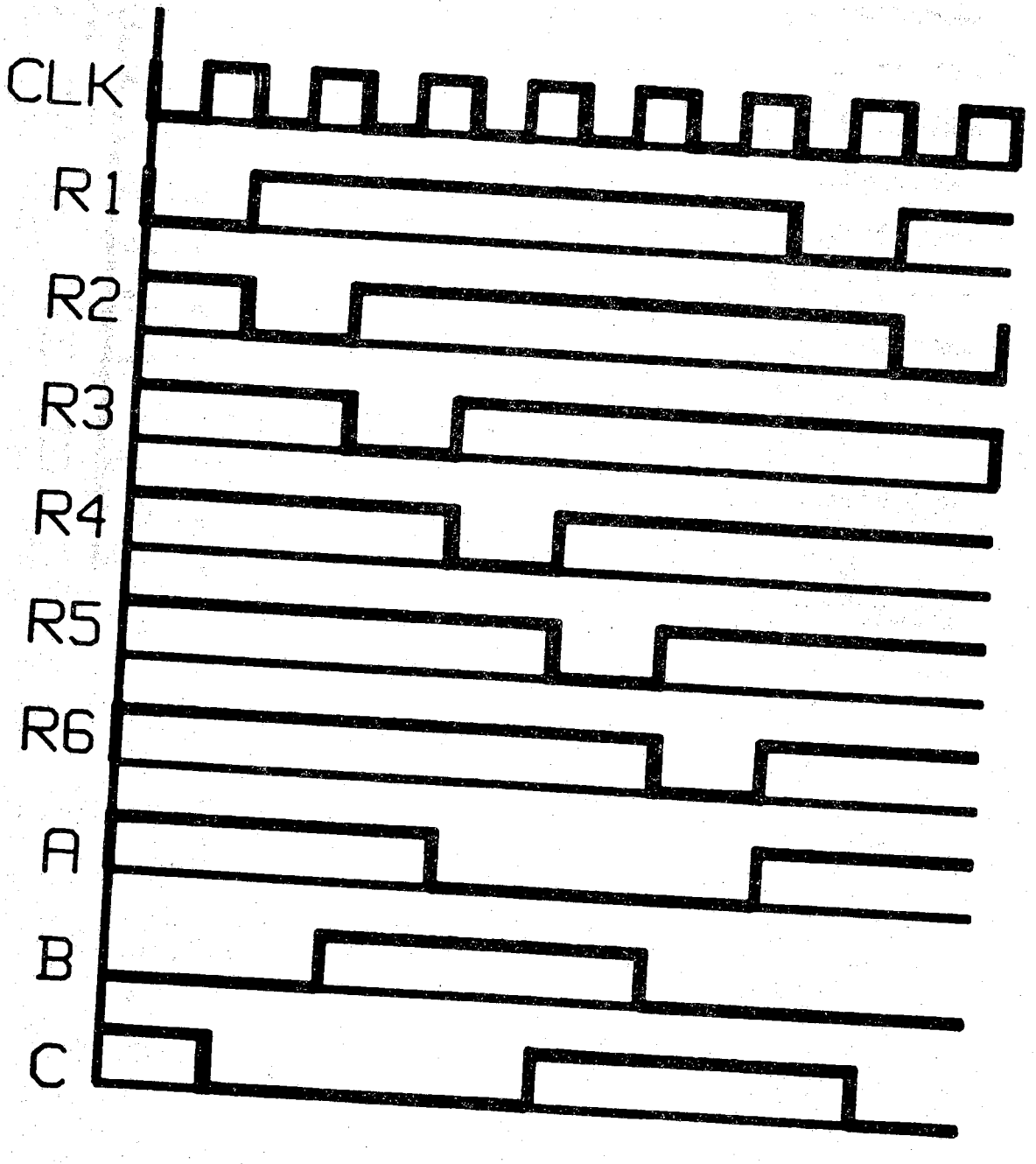

Figure 5.10. Timing Relationships between Ring-Counter States and Phase Signals.

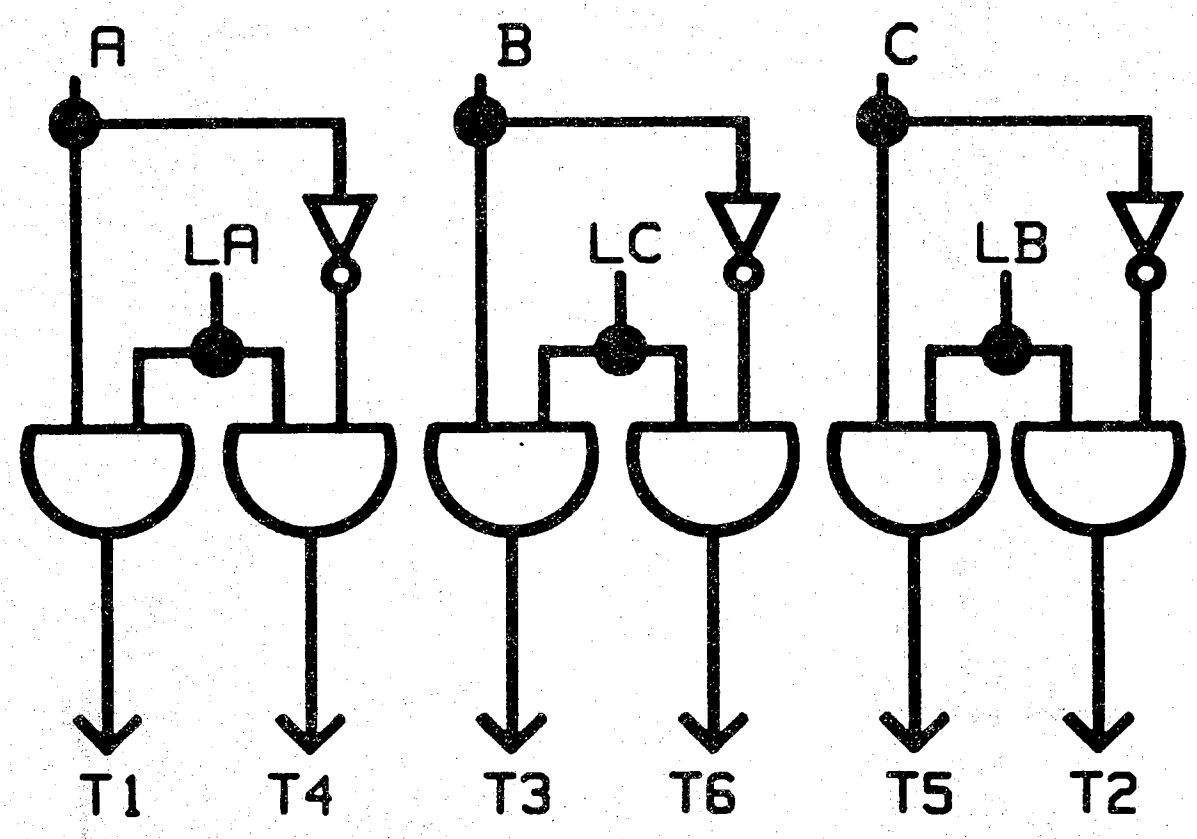

Figure 5.11. **Drive Logic Maker.**

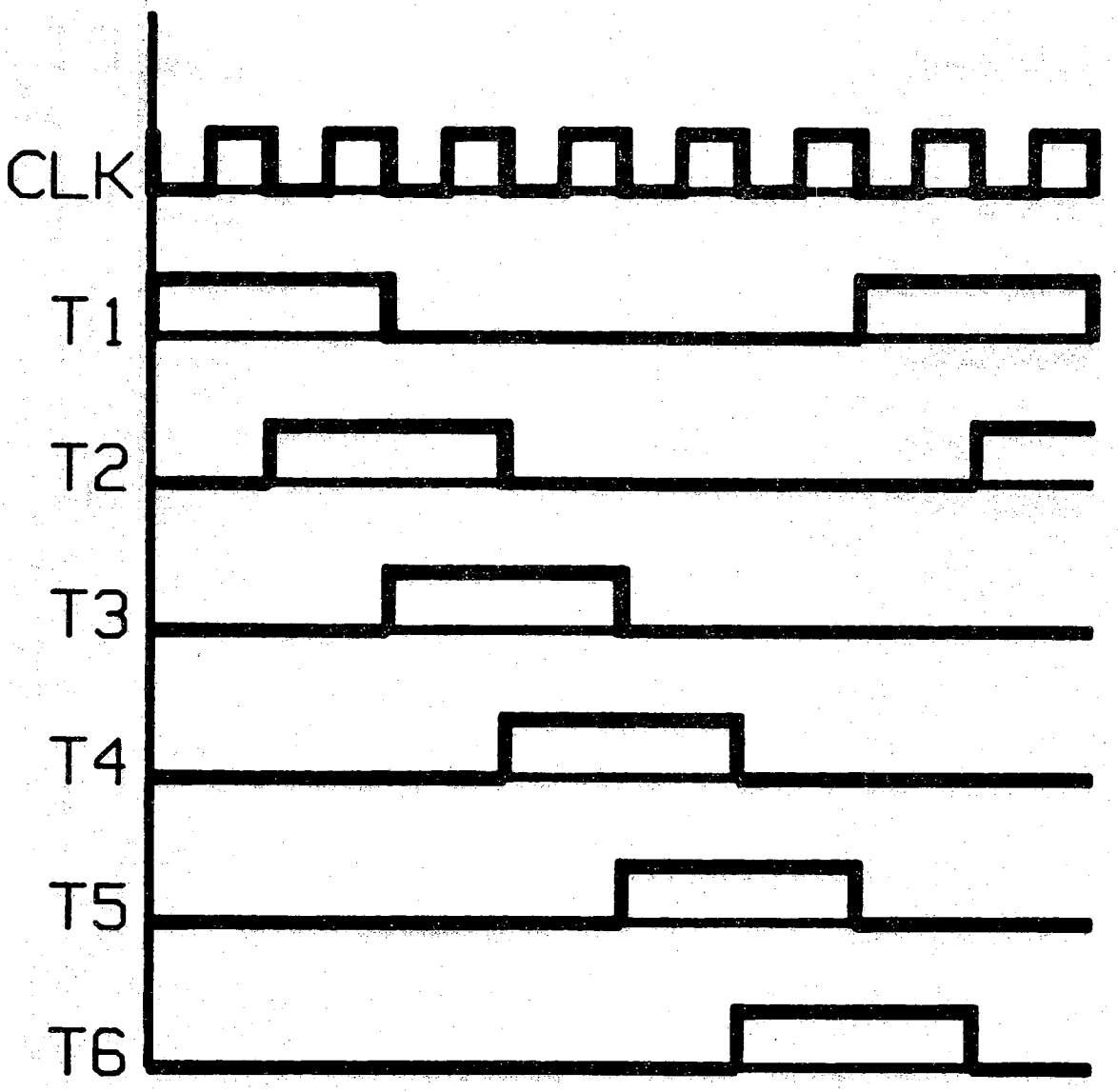

Figure 5.12. Timing Relationships for T1 through T6.

CHAPTER 6

OPERATION OF THE THREE-PHASE INVERTER

Upon successful testing of the three-phase inverter, documentation was in order. In the circuit of Figure 5.1, a three-phase load of three 6.3 ohm, 55 watt wire-wound resistors delta-connected was used. 2.5 amps was chosen as the value of peak current to be run through the load. V_{DC} was set at 10.0 volts to achieve this amount of current. The duty cycle of each of the 555 one-shot timers in Figure 5.3 was set at 67% by adjusting the R_t of each 555 circuit. This is the mode of operation where only two Darlingtons conduct at any one time. The phase-to-ground voltages, V_{AN}, V_{BN}, and V_{CN} are shown in Figures 6.1,6.2, and 6.3, respectively. Note that these voltages are 120 electrical degrees apart as expected for three-phase symmetry. Next, the individual Darlington currents, I_{T1} through I_{T6}, are shown in Figures 6.4 through 6.9 respectively. Note that each Darlington is only on for 120 electrical degrees of the total current wave. Observe also the clean cut square waves due to a purely resistive load. Figures 6.10, 6.11, and 6.12 show I_{AB}, I_{BC}, and I_{CA}, respectively. Note that these currents are 120 electrical degrees out of phase as expected. The line-to-line voltages are of similar waveshapes since the three-phase load is purely resistive.

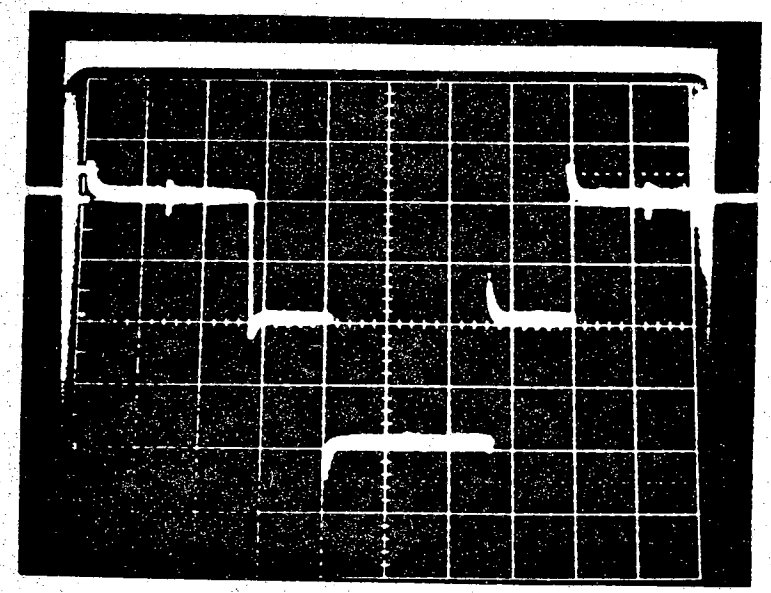

Figure 6.1. Voltage from Phase A to Ground.

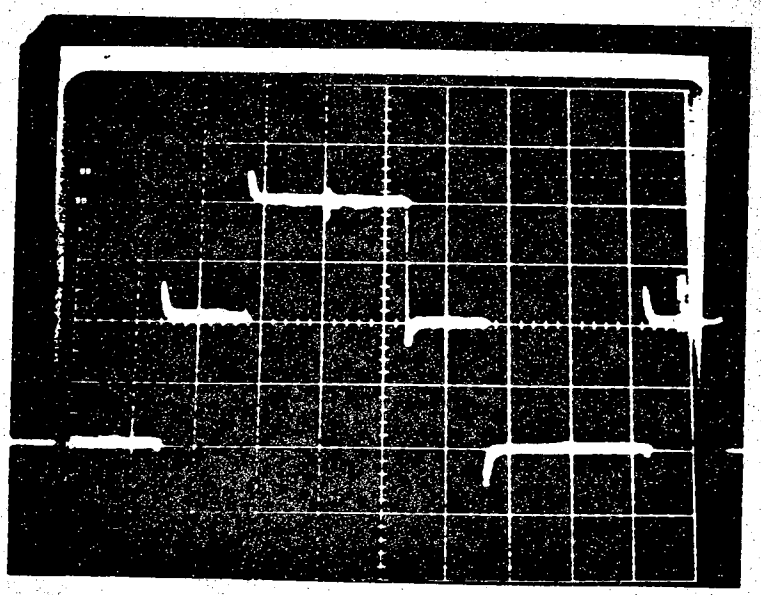

Figure 6.2. Voltage from Phase B to Ground.

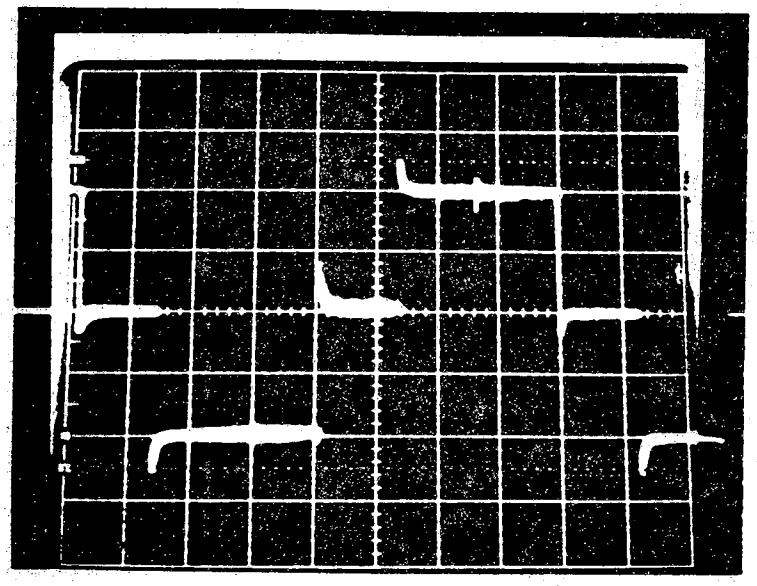

Figure 6.3. Voltage from Phase C to Ground.

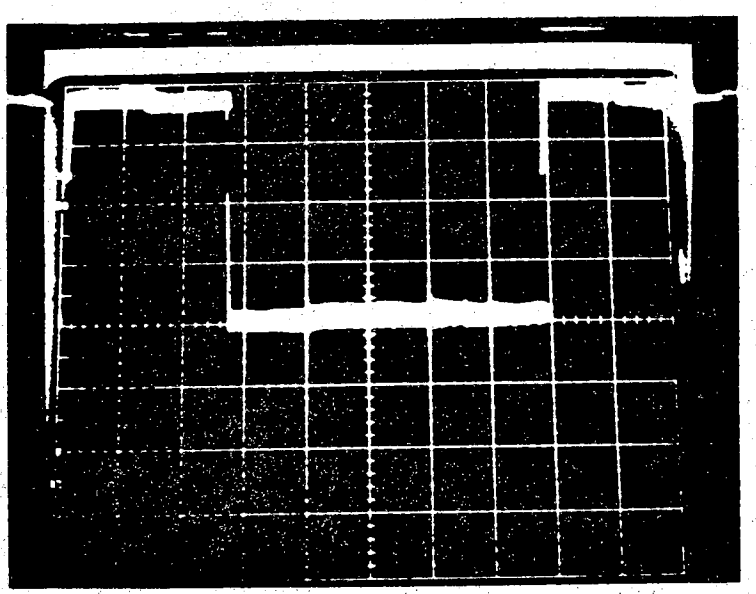

Figure 6.4. Current Through Darlington T1.

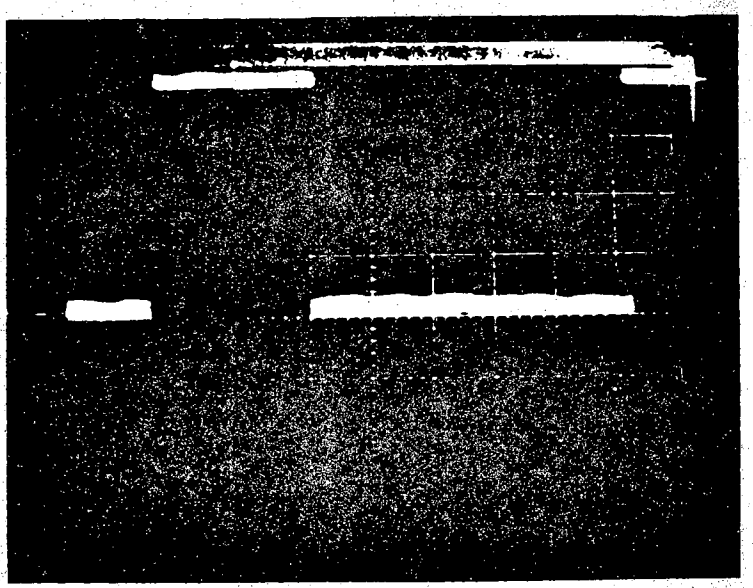

Figure 6.5. Current Through Darlington T2.

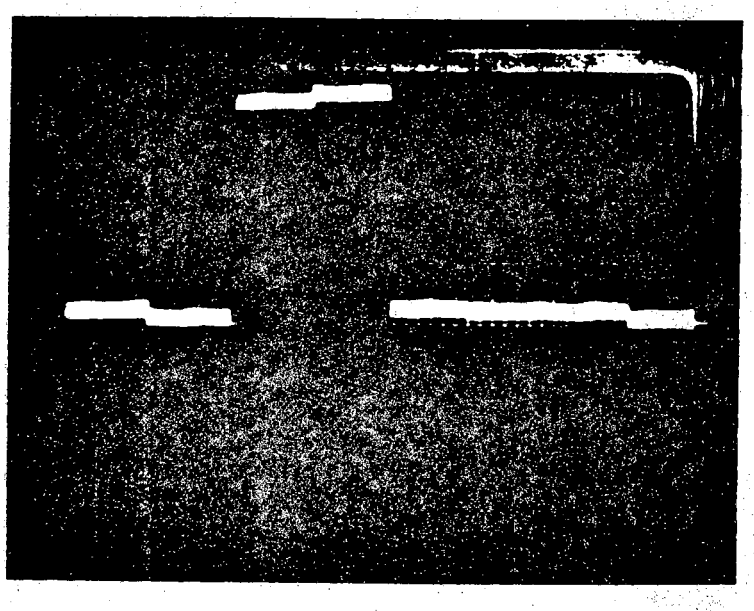

Figure 6.6. Current Through Darlington T3.

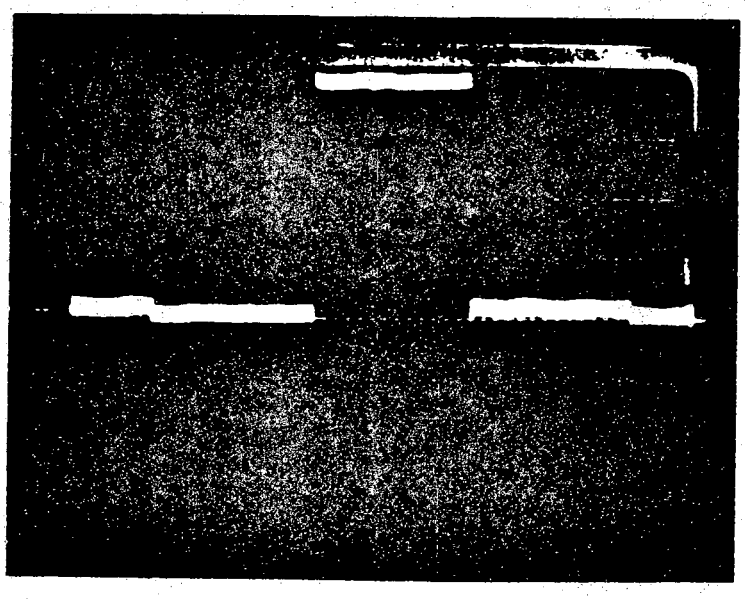

Figure 6.7. Current Through Darlington T4.

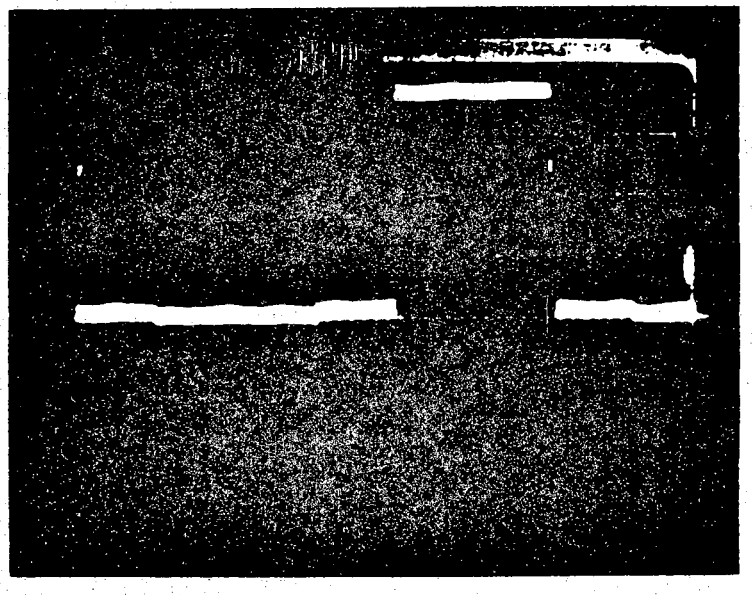

Figure 6.8. Current Through Darlington T5.

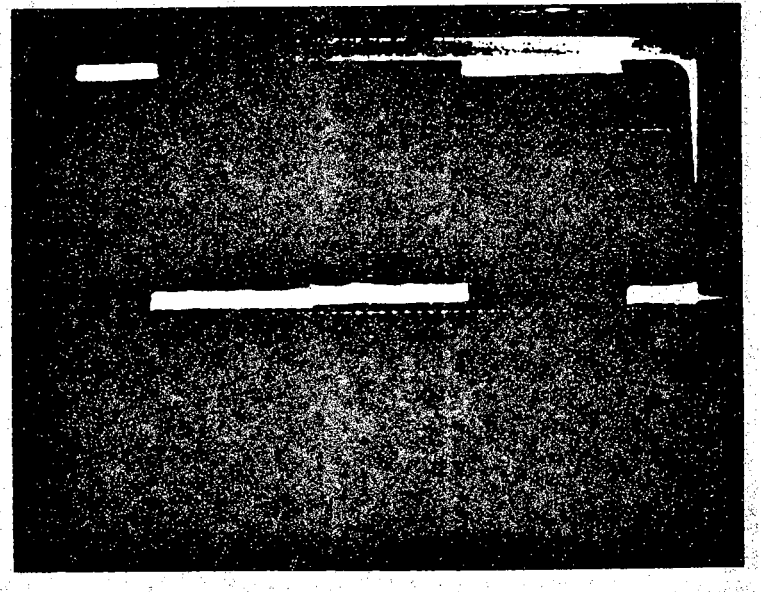

Figure 6.9. Current Through Darlington T6.

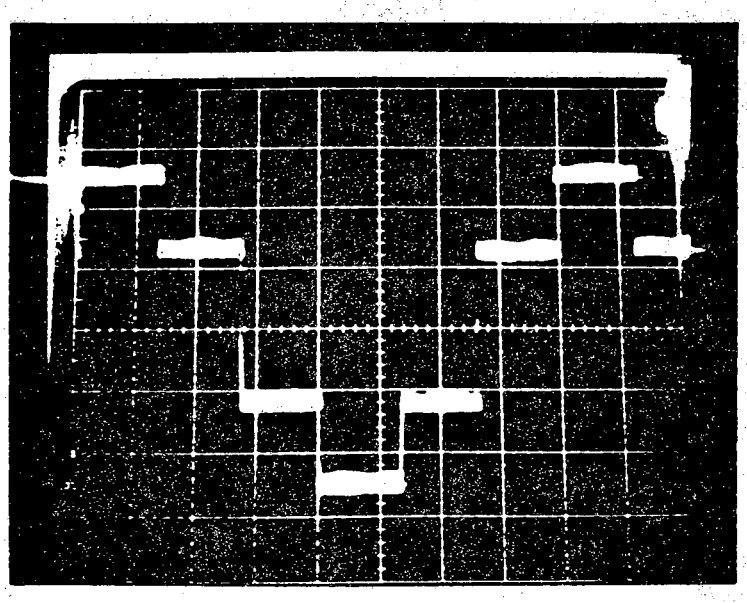

Figure 6.10. Current Through the Resistor Across Phases A and B.

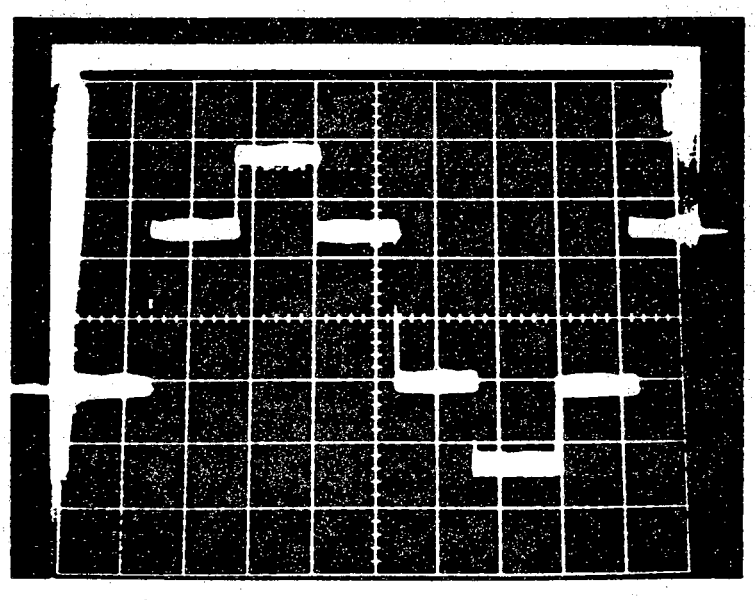

Figure 6.11. Current Through the Resistor Across Phases B and C.

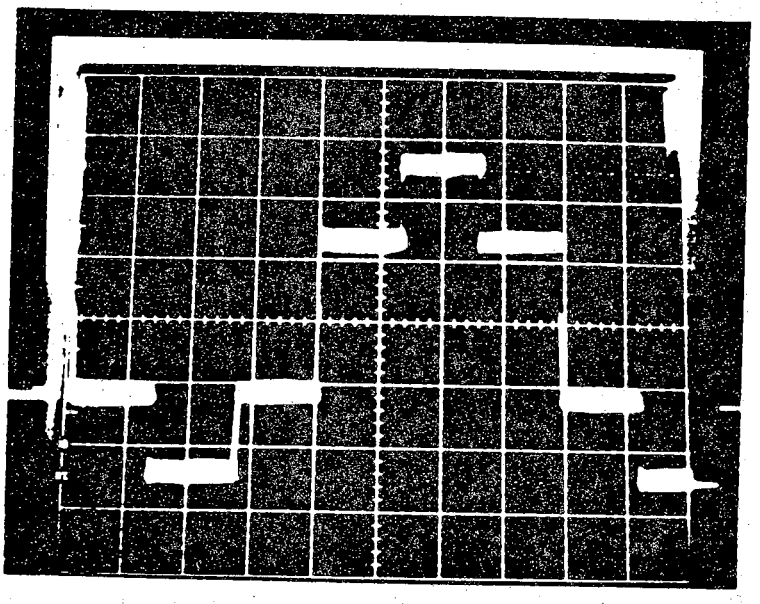

Figure 6.12. Current Through the Resistor Across Phases C and A.

CHAPTER 7

CONCLUSIONS AND RECOMMENDATIONS

The main result of this thesis is the production of a three-phase inverter, its drives, and pulse-width modulation logic circuitry. These units can be very helpful for classroom demonstrations. An additional product of this thesis is the single-phase pulse-width modulation control circuitry. Single-phase inverter operation can be demonstrated by disconnecting two Darlingtons and their respective drives from the three-phase inverter circuit and applying the single-phase pulse-width modulation control circuitry. With either single-phase or three-phase inverter operation, pulse-width modulation can control the pulse width of the output voltage, thereby controlling its rms value. If the fundamental frequency of the output voltage of the three-phase inverter was filtered out and used to run an induction motor, the speed of the motor would be readily controllable by adjusting the pulse width of the output voltage. This would be variable line voltage speed control and would only be practical over a limited range of speed [6]. However, if the clock of the three-phase inverter was made variable, variable-frequency variable-voltage speed control could be obtained. This changing of the clock frequency could be obtained by replacing C_t of Figure 5.4 with a variable capacitor. In addition, the three R_ts of the 555 one-shots in Figure 5.6 would have their ranges of operation adjusted accordingly.

The single-phase inverter and three-phase inverter should be used in power electronics and motor control courses as demonstration units. Also, additional research should be done to see how effective the single-phase inverter could control a single-phase motor and likewise how effective the three-phase inverter could control a three-phase motor. In addition, an attempt should be made to replace the present analog pulse-width modulation logic circuits with digital or software implementations. This would undoubtedly ensure more accurate switching and motor speed control.

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VITA

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