3-1-1988

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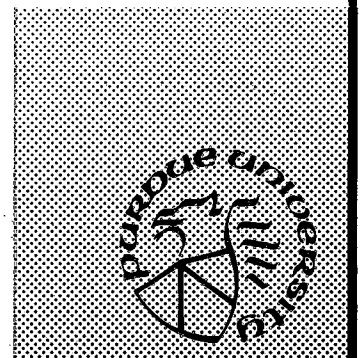
G. W. Neudeck
Purdue University

J. H. Pak
Purdue University

R. Bagri
Purdue University



A Polysilicon Contacted Emitter Bipolar Transistors: Fabrication Development

G. W. Neudeck
J. H. Pak
R. Bagri

TR-EE 88-12
March 1988

School of Electrical Engineering
Purdue University
West Lafayette, Indiana 47907

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CHAPTER I
INTRODUCTION

Traditionally bipolar transistors have monocrystalline emitters that are contacted by metal, usually aluminum. However, the current gain of conventional BJTs does not reach the highest values predicted by theory. This is due to the high doping effects which limit the emitter injection efficiency and/or high minority carrier recombination in the emitter [1].

Silicon bipolar technology has reached a state of advancement that the device characteristics and circuit performance are not only determined by the doping profiles but also by the emitter contact technology. In the last few years polycrystalline silicon has been used increasingly as the emitter contacting material. Polysilicon contacted devices have made it possible to achieve much greater emitter injection efficiencies, and possess the ability to greatly increase the current gain at a given base impurity doping concentration.

The performance of bipolar transistors has been considerably enhanced by the use of polysilicon as both a diffusion source and a contact for shallow emitter devices. Improvements in packing density and switching speed have resulted from the self-aligned structure [2], which has reduced device parasitics, and the lower base current as compared to metal contacted shallow emitter devices. With a lower base current, the base doping level can be increased to reduce the intrinsic base resistance without sacrificing the current gain of the original device [3]. Several researchers have investigated enhanced gains in polysilicon emitter devices, suggested various models to explain their operations, fabricated devices, and obtained good results. However, none of them reported reproducible devices or data from the devices they made in terms of beta variability.

The objective of this thesis lies not only in demonstrating that polysilicon emitter transistors have higher current gains than the conventional shallow emitter aluminum contacted devices but also in showing that the polysilicon emitter devices can be manufactured in a

consistently reproducible manner.

In fabricating n^+pn transistors, either arsenic or phosphorus can be used as the dopant for the emitter region in monocrystalline silicon and for the polysilicon contact. Arsenic was chosen for our process due to the superior shallow doping profile that could be obtained. The shallow emitter was formed in the monocrystalline substrate before the polysilicon was deposited on that region to make a polysilicon contact, which is also doped with arsenic. The emitter is then composed of both a monocrystalline and polycrystalline region.

The base currents of these shallow emitter devices are controlled by the material ,which is polysilicon contacting the emitter, and the interface between the contacting material and the emitter region under the contact. There are three major different theories proposed to explain the improvement in emitter injection efficiency and hence beta of polysilicon contacted transistors. These theories and a model of the conduction mechanisms in polysilicon are discussed in chapter II.

Polysilicon emitter contacted bipolar transistors were fabricated by the introduction of two extra masking steps into an existing four mask conventional shallow emitter bipolar process excluding isolation. The basic process and process development are discussed in chapter III. Before devices could be fabricated it was necessary to predict the device performance from the proposed fabrication sequence. The process simulators SUPREM II and SUPREM III have been useful in the design and optimization of integrated circuit technologies. SUPREM II, however, does not model structures that utilize polysilicon. SUPREM III, on the other hand, is an improved process simulator that can model up to five material layers, including polysilicon, and was available in the Enginnering Computer Network at Purdue University. Using SUPREM III, the proposed bipolar junction transistor (BJT) structure was modeled and optimized with the existing implants, oxidations, and design rules. The program has predicted that an acceptable profile can be obtained by varying those parameters. This is also included in chapter III. Other processes that were performed for the purpose of developing the polysilicon emitter contacted devices are described. Their characteristics are explained and compared with the test results.

Basic electrical measurements were made on both conventional devices and polysilicon emitter contacted devices that were fabricated in the same wafer and conditions except for the polysilicon contact part. Mainly

enhanced current gain in the polysilicon emitter contacted devices, the deviation in the current gain values, and resistance values for the contacts over numerous devices are used as the evaluating criteria. The measurement method and results of measurements are discussed in chapter IV. Conclusions and recommendations are made in chapter V.

CHAPTER II
LITERATURE REVIEW

2.1 Introduction

The performance of bipolar transistor has been considerably improved by the use of polysilicon either as an impurity diffusion source for the emitter itself or as a contact for the shallow emitter of a conventional transistor [3]. Improvements in packing density and switching speed or current gain can be achieved compared to metal contacted devices. The use of polysilicon as a diffusion source for the emitter leads to the self-aligned structure, which reduces device parasitics and the device feature size.

A higher gain can be achieved, by the use of the polysilicon as a contact for the shallow emitter, due to a reduction in base current, which in turn is a result of improved emitter injection efficiency. Also, with a lower base current, the base doping level can be increased to reduce the intrinsic base resistance without sacrificing the current gain of the device, so that switching speed can be enhanced. Minimum ECL gate delays as low as 73ps have been reported for the polysilicon self-aligned structure [4]. The mechanism that contributes to the lower base current, or the higher current gain, with polysilicon emitter contacts are explained in this chapter.

2.2 Current Flow and Emitter Injection Efficiency

This section pertains to the monocrystalline emitter and base regions and follows conventional analysis for uniform doping and low level injection.

An investigation of the mechanisms that cause base current to flow is fundamental in understanding the operation of bipolar transistors. An understanding of the components of the base current is required in order to understand how the presence of the polysilicon contact and the interface layer between monocrystalline and polycrystalline regions of the emitter affect those components resulting to the higher current gain of the

polysilicon contacted emitter devices.

The base currents of the conventional n^+pn bipolar transistor mainly consists of three components:

1) recombination current in the base region, I_{nE} - I_{nC}
2) recombination current in the emitter base depletion region, I_{rg}
3) recombination current in the quasi-neutral emitter region, I_{pE}

For state-of-the-art transistors, the base width is very small and hence the recombination current in the base region(#1) can be neglected. This is due to the fact that most carriers(electrons) that are injected from the emitter travel through the base region without recombining provided the base width is much less than the minority carrier diffusion length. The second component(I_{rg}) dominates at very low injection levels and depends on the emitter base depletion layer width and the bulk recombination rates for carriers in the depletion region. The third component(I_{pE}) is mainly determined by the doping level in the emitter, by band gap reduction effects, and by the minority carrier (hole) lifetime in the emitter. In shallow emitter transistors, emitter minority carrier recombination can be neglected, when the emitter depth is so shallow that it is much shorter than the minority carrier diffusion length. In this case most minority carriers would penetrate through the emitter and recombine at the metal contact. Therefore, the surface (i.e., contact) recombination current plays an important role for shallow emitter transistors [5]. The current I_{pE} is now dependent on the emitter depth and not the minority carrier diffusion length. The base current components are shown in Figure 2.1.

An important performance parameter in the analysis of a bipolar transistor is the emitter injection efficiency, γ. This measures the injected electron current compared to total emitter current for an n^+pn transistor. It measures the effectiveness of the emitter-base junction in injecting electrons from the emitter into the base. Equation (2.1) is the definition of γ.

$$\gamma = \frac{I_{nE}}{I_E} = \frac{I_{nE}}{I_{nE} + I_{pE} + I_{rg}} \tag{2.1}$$

At very low collector currents, the contribution of the recombination-generation current in the emitter-base depletion region may be large compared with the useful diffusion current of minority carriers across the base, so that the emitter injection efficiency is low. By minimizing the bulk traps in the emitter-base depletion region, the recombination-generation

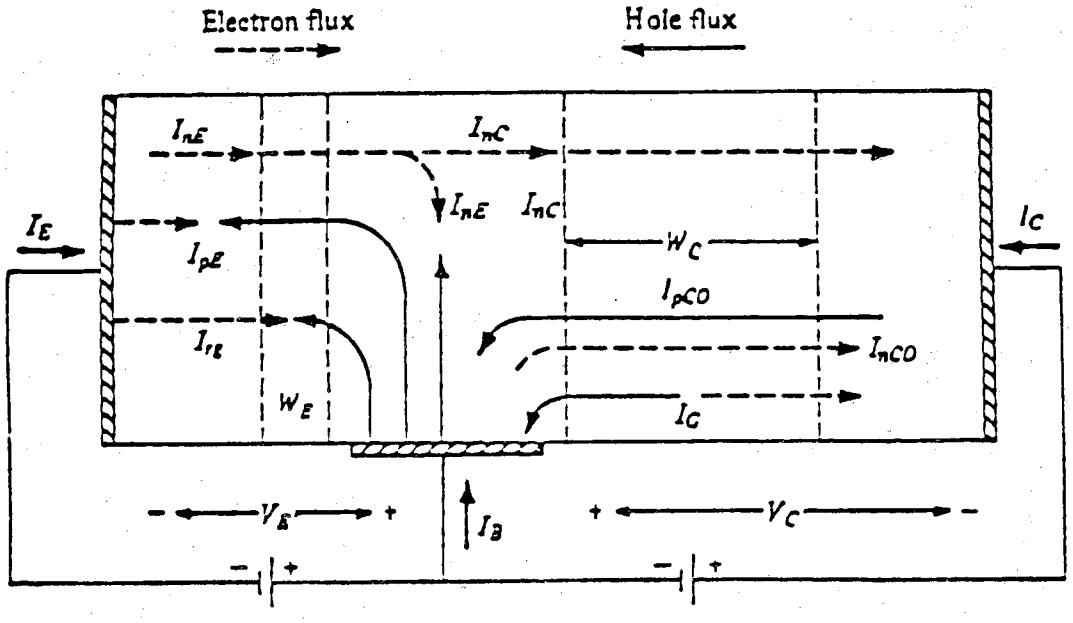


Figure 2.1 Current components of conventional n^+pn bipolar transistor.

current can be reduced. At large collector currents, I_{rg} can be neglected. Therefore, equation (2.1) can be approximated by equation (2.2).

$$\gamma = \frac{I_{nE}}{I_E} = \frac{I_{nE}}{I_{nE} + I_{pE}} \tag{2.2}$$

It should be noted that γ gets close to unity as I_{pE} approaches zero; that is, as the emitter is more heavily doped, I_{pE} becomes a smaller percentage of I_E (similar to the n^+-p diode current components). In actual n^+pn bipolar transistors, the departure from unity results from the recombination of holes injected from the base into the emitter. It can be recognized in equation (2.3a) assuming uniform doping,

$$\gamma = \frac{I_{nE}}{I_E} = \frac{D_B n_{B0}/W}{\frac{D_B n_{B0}}{W} + \frac{D_E p_{E0}}{L_E}}$$

$$= \frac{1}{1 + \frac{D_E}{D_B}\frac{p_{E0}}{n_{B0}}\frac{W}{L_E}} \quad ; \; V_{CB} = 0 \tag{2.3a}$$

,where D_E and D_B are the minority carrier diffusion coefficients in the emitter and base respectively; p_{E0} and n_{B0} are the thermal equilibrium minority carrier concentrations in the emitter and base respectively; and W and L_E are the quasi-neutral base width and the minority carrier diffusion length in the emitter. In equation (2.3a) as p_{E0} is made much less than n_{B0}, by doping the emitter, $N_{DE} >> N_{AB}$, then γ approaches unity. Also, $W << L_E$ helps γ approach unity.

In order to reduce device parasitics and side wall injection effects, shallow emitters were introduced. In very shallow emitter, L_E is replaced by W_E, the emitter depth, as shown in equation (2.3b). Now W is much smaller than W_E, and in fact they are of comparable size. Equation (2.3b) points out that γ is reduced, hence the beta is reduced.

$$\gamma = \frac{1}{1 + \frac{D_E}{D_B}\frac{p_{E0}}{n_{B0}}\frac{W}{W_E}} \tag{2.3b}$$

There is another important performance parameter in the analysis of a bipolar transistor. That is a base transport factor, α_T, which is defined as the ratio of the electron current diffusing into the collector to the electron current injected at the base-emitter junction in a n^+pn transistor. In a well fabricated device, which has the base width less than one tenth of the minority carrier diffusion length, α_T approaches unity. Therefore, the current gain is controlled almost entirely by the emitter injection efficiency.

In actual n^+pn transistors, at reasonable currents, the departure from unity of γ results from the recombination of holes injected from the base into the emitter. It is obvious that an improvement in current gain can be achieved by a reduction in this back-injected base current. The use of a heavily doped polysilicon layer either as a diffusion source for the emitter or as a contact to a monocrystalline emitter region increases the current gain by reducing the back-injected current component. There is, however, some controversy as to how exactly this is brought about. It will be discussed in the following sections.

2.3 Conduction Mechanism of Polysilicon Emitter

A controversy exists regarding the mechanisms that contribute to the lower base current with polysilicon emitter contacts. A variety of theoretical models have been proposed to explain the enhanced betas of polysilicon emitter transistors, and those are broadly of two types.

The first is a tunneling model[6] that explains the improved gain in terms of tunneling through a thin interfacial oxide layer. The second type of model explains the improved gains in terms of the transport properties of the polysilicon. Ning and Issac[2] showed that a factor of approximately three improvement in gain was obtained when the shallow emitter was contacted via a polysilicon layer, and this was explained by a lower mobility in the polysilicon. These two models and other related mechanisms are investigated in the following sections.

2.3.1 Tunneling Theory with Thin Interface Layers

The tunneling model through a thin oxide was originally proposed by De Graaff and De Groot[6] and later improved by Eltoukhy and Roulston[5]. Recently Van Halen and Pulfrey[7] have gone so far as to demonstrate that devices with an oxide interface layer can be modeled in exactly the same way as metal-insulator-semiconductor tunnel devices.

The theoretical model of De Graaff and De Groot assumes direct tunneling of both majority and minority carriers through the interfacial layer and band bending at its interface. This model explains the increase in emitter injection efficiency, based on the presence of a thin interfacial layer between the monocrystalline and polycrystalline regions, with the quantum mechanical tunneling of the carriers through the interfacial layer which generally consists of oxidized silicon, preferably 20 to 30Å thick. The oxide layer must be as close as possible to emitter-base junction in this model. Otherwise, it will only increase the device resistance. To obtain a higher emitter injection efficiency in an n^+pn transistor the tunneling probability for holes should be low. To avoid a large extra voltage drop across the interfacial layer which is more or less insulating, the tunneling probability for electrons should not be too low [6]. The significance of this is that the base current is suppressed, but the emitter current is not.

This model assumes that the impedance of the interfacial layer for holes is large and that the hole current is determined by this impedance. It also assumes the minority carrier injection at the monocrystalline p-n^+ junction, and that the tunneling model is not sensitive to the properties of the polycrystalline layer. This last assumption is true only when the interfacial layer or oxidized silicon is on the order of 20 to 30Å thick. If the oxide is extremely thin, less than 15Å, then the impedance of the oxide for holes is very small and the polysilicon layer plays an important role in determining the base current. On the other hand, if the oxide is thick enough, greater than 60Å, then the injected holes cannot tunnel through the oxide and a build-up of positive charge under the oxide takes place with concomitant increase in the voltage drop across the insulator. Electrons, however, have higher tunneling probability than holes and less effects will occur in the electron tunneling. But if the oxide becomes very thick, electrons will also be blocked. In this case, the emitter-base junction is almost zero biased and the device behaves as an open circuit [5].

The transistors with an interfacial layer fabricated by Graul et. al[8] showed gains which were approximately seven times higher than conventional transistors. The use of intentional chemically grown oxide interface as a tunneling barrier to hole injection has been shown to give the lowest base current. However, its use significantly degrades the high frequency performance capability of the devices by increasing the emitter resistance by an order of magnitude with respect to oxide-free interfaces, increases the low current leakage and reduces control of the emitter profile as the polysilicon is used as an impurity diffusion source [9,10]. These devices also showed nonideal I-V characteristics and an unusual temperature dependence of the current gain. It is also difficult to achieve precise control of the thickness of the interfacial oxide layer and thus difficult to get devices with predictable characteristics [11].

More recently, a conduction mechanism was suggested by H. Schaber, B. Benna, L. Treitinger, and A. W. Wieder [12]. According to this model, the emitter current is emitted by a combined thermal emission and tunneling mechanism across an interface barrier of $\phi_B \simeq 0.8$V in the conduction band. The base current flows via tunneling and recombination at the interface traps. The overall mechanism is summarized as in Figure 2.2.

2.3.2 Transport Properties of Polysilicon Emitter

The model to be discussed was originally proposed by Ning and Issac[2] and other authors[13,14] have refined this model and incorporated more detailed descriptions of the polysilicon structure. Neugroschel et al.[15] have suggested that the transport properties vary across the polysilicon, with the gain being controlled by a highly disordered layer within approximately 100Å of the interface.

Ning and Issac[2] attributed the improvement of the current gain to minority carrier transport in the bulk of the polysilicon layer itself. The polysilicon would extend the effective length of the emitter, while the low minority carrier mobility in the polysilicon would retard the transport of injected minority carriers. Neugroschel et al.[15] have shown that a reduction in base current is obtained, compared to devices with metal contacts, only if arsenic is segregated to the polysilicon/monosilicon interface. In addition, they suggested that minority carrier transport is dominated by a 200~300Å highly disordered layer at the interface. This

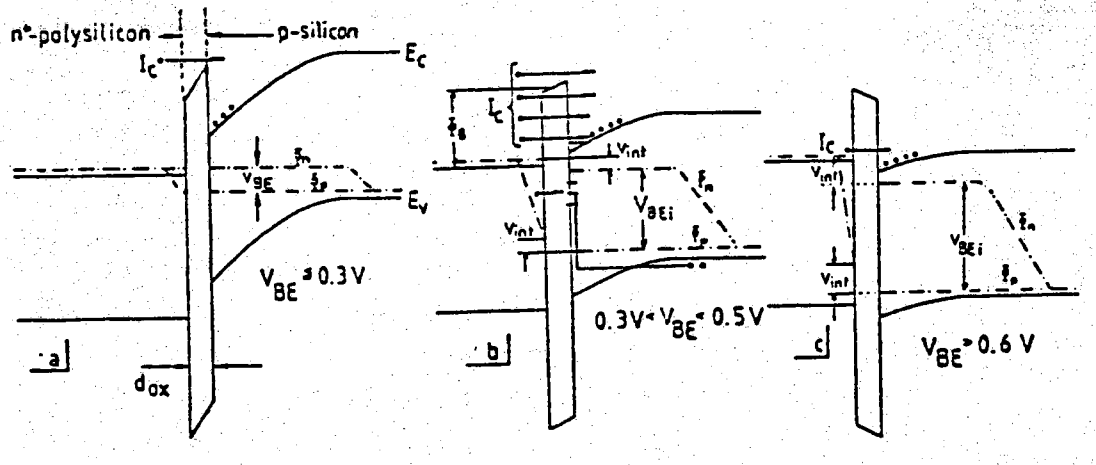


Figure 2.2 Energy band diagram at different forward bias: (a) "classical" transistor behavior, (b) thermionic emission and thermionic field emission, and (c) direct tunneling through interfacial layer. From Ref. 12.

region, if it existed, would be characterized by a very low minority carrier mobility.

Ning and Issac[2] demonstrated experimentally that the current gain improvements are related to the transport of minority carriers in the heavily doped polysilicon. They fabricated polysilicon contacted emitter transistors which have no intentional interfacial oxide layer between the monocrystalline and polycrystalline regions. They concluded that the current gain enhancement is not determined by the polysilicon/monosilicon interface properties, e.g., tunneling through an interfacial layer, but by the transport of holes in the n^+ polysilicon layer. A simple two-region (n^+ monosilicon region and n^+ polysilicon region) model is presented which satisfactorily explains the experimental results in terms of lower hole mobility in the n^+ polysilicon than in the n^+ monocrystalline silicon.

The two-region model for a shallow monocrystalline emitter with an n^+ polysilicon contact is schematically illustrated in Figure 2.3. If the monocrystalline emitter is contacted by metal at W_1, the concentration gradient will be very nearly linear with x because the emitter is short with respect to the diffusion length of the injected holes. All injected carriers(holes) from base are forced to recombined at the ohmic contact and the hole concentration for this case is represented by the dotted line. Since the hole current is linearly related to the minority carrier concentration gradient as shown in equation (2.4) [16], a steep gradient requires more holes to be injected from the base and this implies a large base current.

$$I_{Ep}(W_1+W_2) = qAD_E \frac{d\Delta p_E(x)}{dx}\bigg|_{x=W_1+W_2}$$

$$= \frac{qAD_E}{W_2} p_{E0}(e^{qV_{BE}/kT} - 1) \qquad (2.4)$$

If the monosilicon emitter is contacted with polysilicon instead of metal, a different concentration gradient results in the monocrystalline region due to a new boundary condition at W_1. The gradient is less steep in the monocrystalline silicon as shown in Figure 2.3. because the carriers are not forced to recombine at the ohmic contact once they traveled through the monocrystalline region. Assuming a continuous concentration at W_1, the holes from the base continue to diffuse over a longer region, namely Region 1 and Region 2, before they are forced to recombine at the ohmic contact.

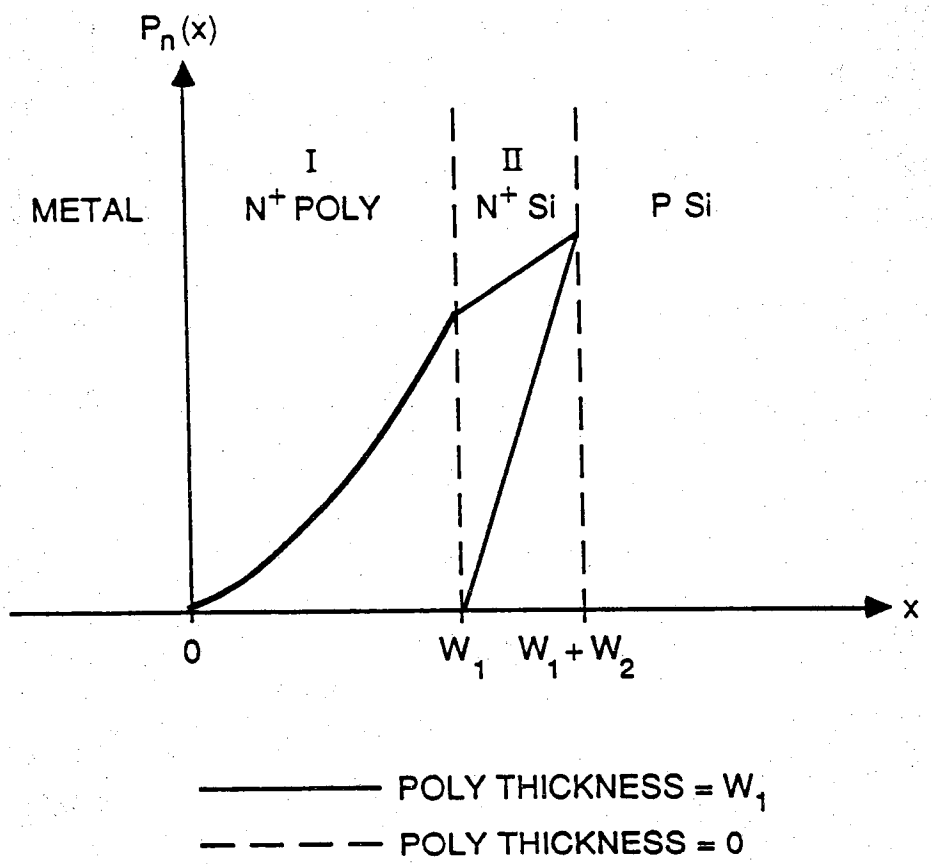


Figure 2.3 Schematic illustration of the two-region model for shallow emitter with n^+ polysilicon contact.

This is true if there is no trapping sites or defects at the polysilicon/monosilicon interface. The gradient in the polysilicon may be much steeper than in the monocrystalline region since the average minority carrier lifetime in polysilicon is much lower than similarly doped monosilicon. This is attributed to the fact that the grain boundaries of polysilicon can act as recombination centers or trapping sites [17]. Even though the steeper hole gradient of Region 1 must be supported, the base current for the entire structure is lower than the metal contacted shallow emitter case because the holes can diffuse longer. In other words, fewer holes are needed from the base to support the concentration gradients of the combined Region 1 and 2 of the emitter. The hole concentration gradient in Region 2 depends on the surface recombination at the polysilicon/monosilicon interface. Higher the surface recombination rate is, steeper the hole concentration gradient in Region 2 is.

The two-region model that has been used to explain the reduction in base current is in agreement with experiment results that show holes having lower mobility in the n^+ polysilicon than in the n^+ monocrystalline silicon [18]. This model also shows a dependence of the hole current on the polysilicon thickness. As the thickness increases, the reduction in base current is improved. However, the improvement levels off once the polysilicon thickness increases beyond some point. It is found that the optimal thickness of the polysilicon is 450~900Å [19] because of added resistance for thicker polysilicon layer and low minority carrier mobility in it.

Even though this two-region model satisfactorily explains the enhanced current gain in terms of lower hole mobility, it seems to be oversimplified without including effects such as a possible energy bandgap difference, a doping concentration difference between the n^+ monosilicon and the n^+ polysilicon, and possible hole recombination at the polysilicon/monosilicon interface [2].

2.3.3 Minority Carrier Injection into Polysilicon Contact

The most recent analysis concerning the physics of minority carrier injection into polysilicon contacted emitters was presented by Patton et al.[3]. Through a series of experiments they correlated the base current to the structure of the polysilicon/monosilicon interface. This work concentrated on devices with a "clean" polysilicon/monosilicon interface, i.e.,

devices given a BHF-dip etch prior to the polysilicon deposition to minimize any oxide contamination. Although the chemical composition and structure of the polysilicon/monosilicon interface and polysilicon grain boundaries are now becoming better understood, the local atomic arrangement and the nature of the chemical bonds in these regions are not known. It has been realized that this limits the possibilities of doing realistic modeling based on the properties of these regions. In any one device, it is possible that some regions may be controlled by tunneling through the native oxide layer while other regions, where the oxide has become discontinuous, are controlled by other mechanisms.

A novel approach was taken in the modeling of transport in emitters to quantify the minority carrier blocking properties of the polysilicon contacts. Their approach did not require assumptions about the interface and grain boundary properties. From a solution of the minority carrier transport equations, the relative importance of transport, surface recombination, and bulk recombination of minority carriers in the devices were identified [3]. From those results, the relative importance of the polysilicon/monosilicon interface and of the polysilicon grain boundaries in influencing minority carrier injection into the emitters were determined. For the comparison of the devices fabricated under different conditions, only the base current characteristics could be used. Recombination in the base-emitter depletion region and series resistance effects can be subtracted from the base current characteristics by using a curve fitting technique as illustrated in Figure 2.4. What remains is the component due to minority carrier injection into the emitter.

All of the physics of minority carrier injection lies in the constant, I_{bs}, which is in the equation listed on Figure 2.4. However, I_{bs} has both an area and a perimeter component, the latter being difficult to model. For large devices (with emitter dimensions of 200μ x 200μ, the area component can be extracted directly from I_{bs} and is known as J_{oe}, the emitter saturation current density. When J_{oe} is extracted for all devices, this parameter is used to study minority carrier injection into the polysilicon contacted emitter. The extraction of J_{oe} from the base current characteristics of the devices provides a direct measure of minority carrier injection into the emitter as a function of the various processing parameters. There are several factors which determine the value of J_{oe} : recombination in the single crystal silicon emitter, the transport of minority carriers across the monosilicon emitter region to the contact, and recombination at the contact. In the case of a

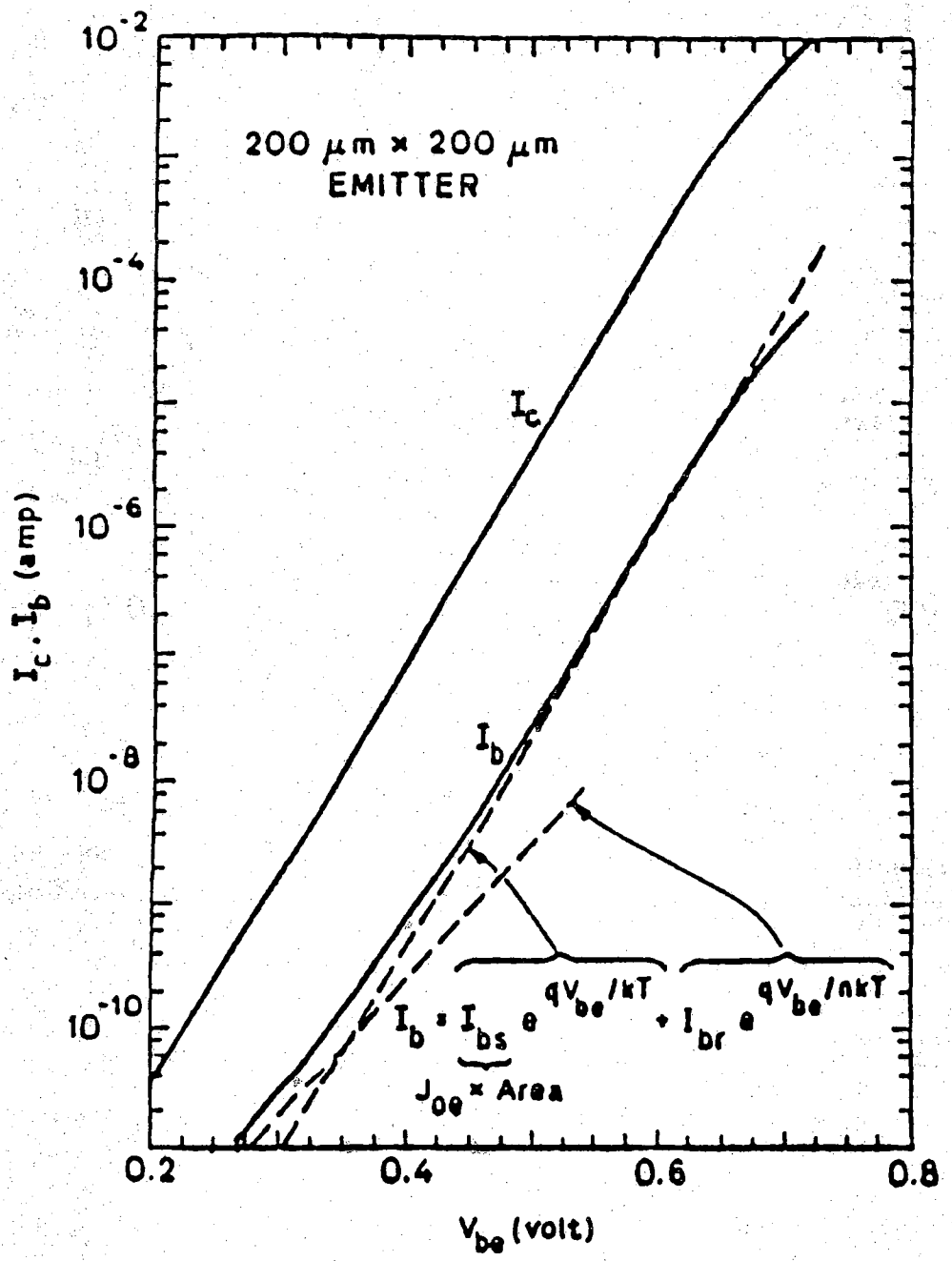


Figure 2.4 Gummel plot of a polysilicon contacted device which illustrates the extension of J_{oe}, the emitter saturation current density, from the base current characteristics. From Ref. 3.

polysilicon contact, recombination can occur both at the polysilicon/monosilicon interface and in the polysilicon layer itself. However, if minority carriers are blocked from entering the polysilicon by an interfacial oxide layer, as suggested by De Graaff and De Groot [6], then the contact recombination will mainly occur at the interface.

As the processing conditions are varied, both the polysilicon/monosilicon interface and the characteristics of the polysilicon contact will change. This means that the relative contributions of bulk recombination, bulk transport, and contact recombination in determining J_{oe} will vary. To exact quantitative information about the electrical properties of the contact alone, recombination and transport effects in the single crystal silicon must be removed from the analysis. This can be accomplished by solving the minority carrier transport equations for the single crystal silicon portion of the emitter. For this procedure, the technique of del Alamo and Swanson [20] was used. From the measured values of J_{oe} (which can be extracted by using the methods shown in Figure 2.4) and emitter doping profiles, the hole current, $J_p(x)$, and the separation of the quasi-Fermi levels, $V(x)$, can be determined at any point in the monocrystalline portion of the emitters, as illustrated in Figure 2.5. These distributions establish the relative importance of recombination and transport in the monocrystalline emitter and of recombination at the polysilicon/monosilicon interface.

Recombination at and in a contact is typically characterized by the lumped parameter, S_p, which is defined as the effective recombination velocity of minority carriers at the contact. The following relationship exists for the hole current at the interface ($x = W_E$):

$$J_{p(}W_E) = qS_p(p-p_0)\,\Big|_{x\,=\,w_E}$$

$$= qS_p p_0(W_E)\left(\exp\frac{qV(W_E)}{kT} - 1\right) \qquad (2.5)$$

where $p_0(x)$ is the equilibrium hole concentration. The extraction of S_p from equation (2.5) is extremely inaccurate because $p_0(W_E)$ must be evaluated using the expression

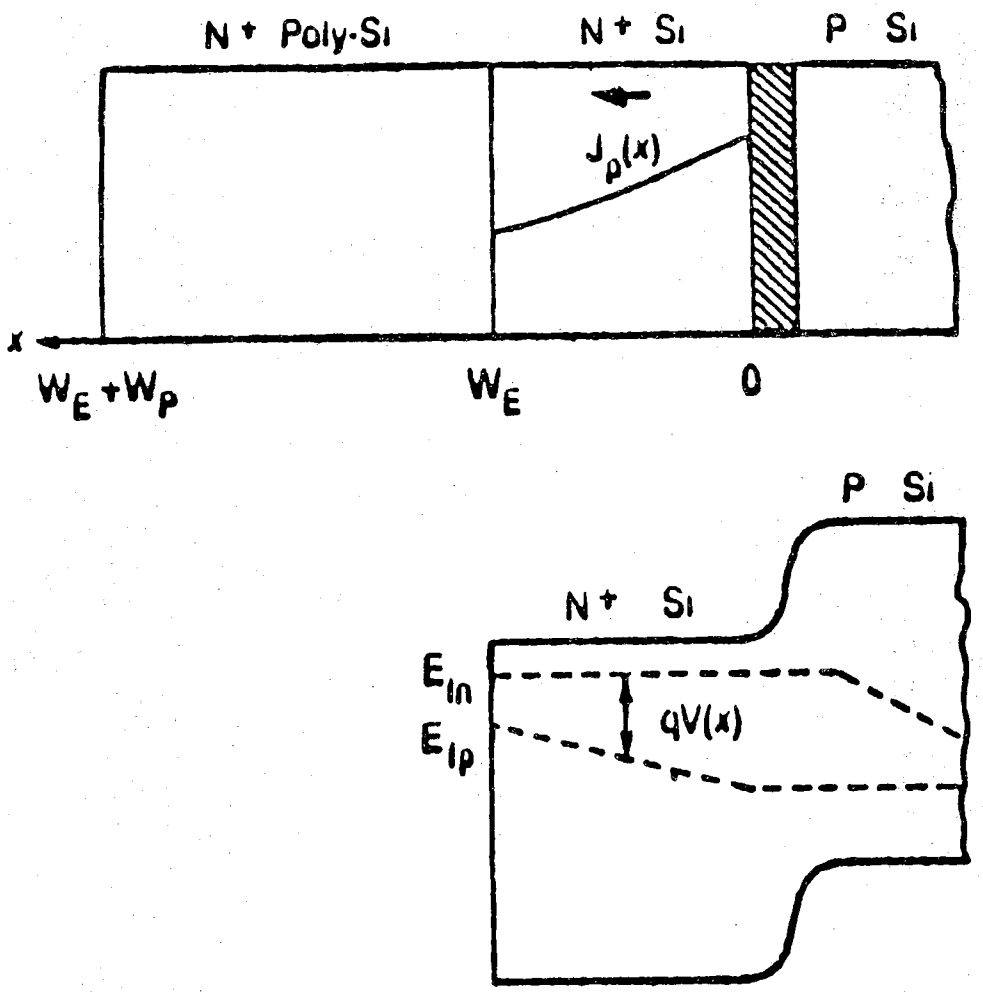


Figure 2.5 With the measured value of J_{oe} and the emitter doping profile, the minority carrier transport equations will yield the hole current, $J_p(x)$, and the separation of the quasi-Fermi levels, V(x), at any point in the monocrystalline portion of the emitter. The edge of the base-emitter depletion region on the emitter side is at x = 0, the original polysilicon/monosilicon interface at $x = W_E$, and the polysilicon/metal interface i at $x = W_E + W_p$. From Ref. 3.

$$p_0(W_E) = \frac{n_{i0}^2}{N_D(W_E)} \exp\left(\frac{\Delta E_g^{app}(W_E)}{kT}\right) \tag{2.6}$$

where n_{i0} is the intrinsic carrier concentration for undoped silicon and ΔE_g^{app} is the apparent bandgap shrinkage. Evaluating equation (2.6) requires an accurate knowledge of the relationship between bandgap narrowing and doping.

However, the dependence on the bandgap narrowing in equation (2.5) can be removed by characterizing the contact by the product of $p_0(W_E)$ and S_p as given in the expression

$$J_{os} = qS_p p_0(W_E) \tag{2.7}$$

where J_{os} is defined as the surface or contact saturation current density [20]. A parallelism exists between J_{oe}, which is the saturation current density at the junction, and J_{os}, which is defined at the polysilicon/monosilicon interface. This is illustrated in the following relationships for the hole current and potential at the junction ($x=0$) and at the interface ($x=W_E$):

$$J_p(0) = J_{oe}\left(\frac{qV(0)}{kT} - 1\right) \tag{2.8}$$

$$J_p(W_E) = J_{os}\left(\frac{qV(W_E)}{kT} - 1\right) \tag{2.9}$$

An additional advantage of using J_{os} is that it can be compared directly to J_{oe} in order to determine if the recombination or transport of minority carrier in the single crystal silicon emitter are influencing the base current. For certain values of J_{os}, recombination and transport effects in the bulk or monosilicon portion of the emitter are negligible. In these cases, the device is limited by surface recombination and J_{os} and J_{oe} are approximately equal. When the surface recombination rate is low (i.e., when J_{os} is small), recombination in the bulk may be an appreciable part of the hole current injected into the emitter. As a result, J_{oe} will be greater than J_{os}.

Alternatively, when the recombination rate at the contact is high, as in the case of metal contact, the transport of minority carriers to the contact may limit recombination there. As a result, J_{oe} would be limited to a value that is lower than J_{os}.

Increased arsenic penetration into the monosilicon region increases bulk recombination and adds to the barrier for minority carrier transport. When bulk recombination is a significant factor, J_{oe} will increase as a result of additional arsenic penetration. In this case, if J_{oe} were used to study changes in the electrical properties of the contact with processing parameters, the increase in J_{oe} might be incorrectly interpreted as an increase in contact recombination. Alternatively, when recombination at the contact is limited by the transport of minority carriers in the monosilicon emitter, the opposite effect also can occur: an increase in the recombination rate at the contact may not be fully reflected by an increase in J_{oe}. In this case, if J_{oe} were used to study changes in the characteristics of the contacts, these changes would be underestimated.

It is clear from the above discussion that J_{os} is the best parameter for characterizing the electrical properties of a contact. However, the previous discussion also illustrates that the contact is only one of three factors which affect the injection of holes into an emitter. Since J_{oe} is a direct measure of the injected hole current, J_{oe} is the relevant parameter for studying the behavior of a device. To put the J_{oe} value in perspective, they have been compared to simulations of the two alternative contacting schemes [3].

In the simulation, the minority carrier transport equations are solved for the single crystal silicon portion of the emitter, except that the polysilicon contact has been assumed to be replaced by metal. With a metal contact, $V(W_E)$ in Figure 2.5 is zero. With this boundary condition and emitter doping profile, $J_p(x)$ and $V(x)$ can be determined at all other points in the monocrystalline emitter. From this new solution, J_{oe} can be calculated for the metal contacted structure. The difference value for this simulated value of J_{oe} and the experimental value for the polysilicon contacted device is a measure of the actual improvements that has occurred by using polysilicon instead of metal for the same emitter profile in the single crystal silicon.

CHAPTER III
PROCESS DEVELOPMENT

This chapter discusses the process development that was done to fabricate consistently reproducible polysilicon contacted emitter devices with enhanced current gain over conventional metal (Al) contacted devices.

Preliminary polysilicon contacted emitter devices and conventional metal contacted emitter (control) devices were fabricated in the same die and tested to obtain proper parameters for the process. Then a new mask set was designed. The process was simulated with SUPREM III process simulation program along with the process development to determine optimum implant energies, doses and thermal cycles for the devices.

There are numerous variables for the entire process: dopant species for the single crystal shallow emitter and the polysilicon contact layer, doses of dopant species, deposition technique and related parameters, polysilicon annealing temperature, polysilicon thickness, and so on. After several fabrication runs and their evaluations, the basic full process was established and their results were used as a basis for the further development.

Main interests are polysilicon deposition techniques and polysilicon/monosilicon interface treatments. LPCVD and PECVD are two polysilicon deposition techniques used for the process development. All evaluations are done with a comparison of the current gain for the enhancement and emitter contact resistance of the polysilicon versus control bipolar transistor.

3.1 Process Outline

Four types of devices were fabricated (Figure 3.1): a standard BJT (control) device called "sub", polysilicon contacted emitter device called "1con", polysilicon emitter device called "em", and combination of the second and third type called "2con". In order to fabricate all 4 types of devices on

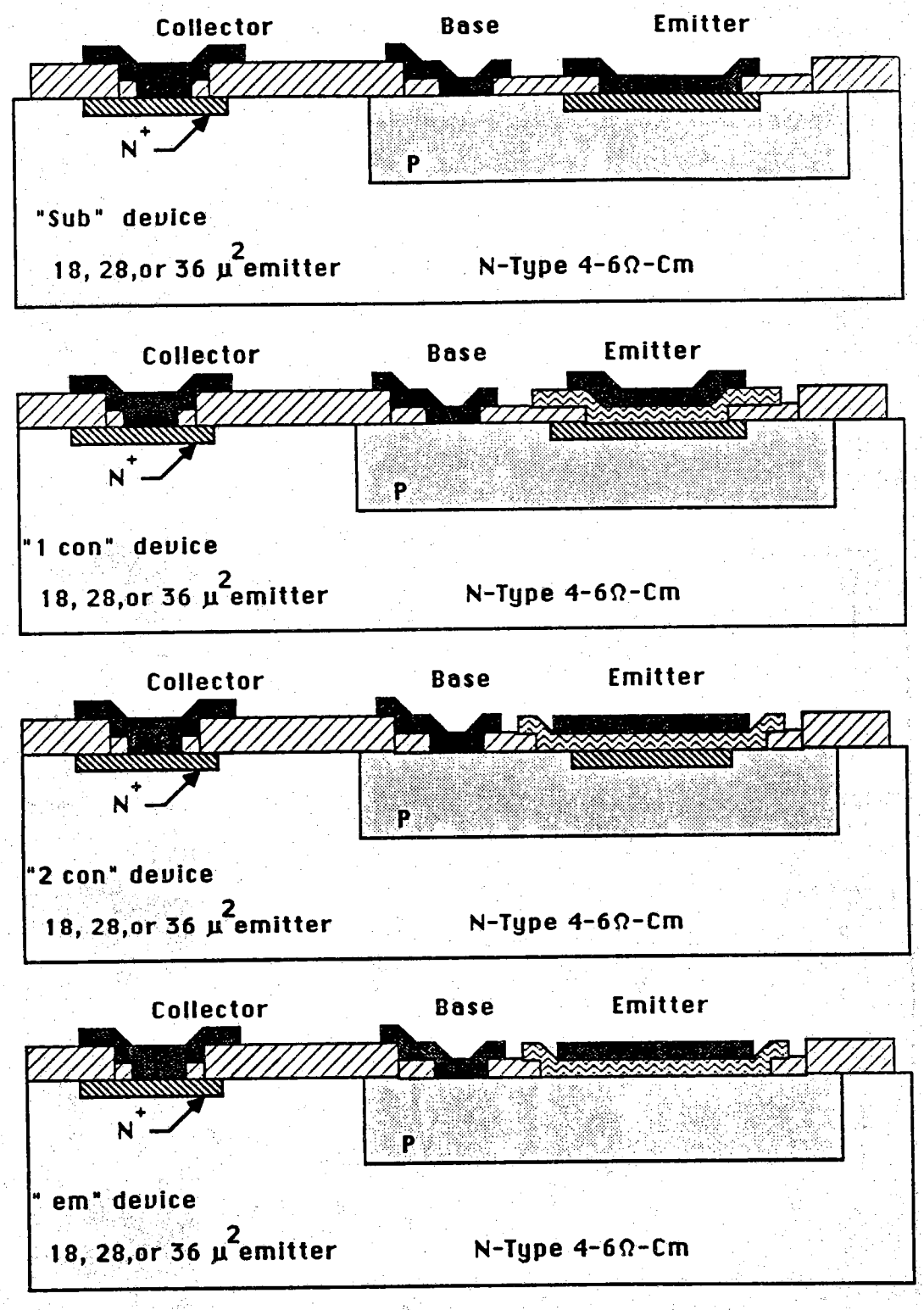


Figure 3.1 Four types of devices designed on test mask.

a wafer, six masks are needed: base pattern, emitter pattern, polysilicon contact openings, polysilicon pattern, metal contact openings, and metallization pattern. No passivation layer was used for these experiments.

All four types of devices were fabricated identically up to and including the emitter drive-in step. Thus the observed differences in device characteristics are attributable, unambiguously, to the different polysilicon contact technology. In addition, the Al contacted devices were made on the same wafer and in the same die with the polysilicon contacted devices, so that both devices have almost identical emitter and base profiles. Profiles may be affected by surface conditions, i.e. whether the surface is oxide or polysilicon. However, their effects are considered negligible on the device characteristics. Therefore, small variations in device characteristics can be detected and attributed to the polysilicon emitter-contact effect.

In preliminary device fabrication runs, it was investigated how different surface treatments prior to polysilicon deposition influence the electrical properties of polysilicon emitter transistors. In particular, devices similar to the "em" devices of Figure 3.1 were fabricated and tested. With the control BJT device as a reference, devices with two types of surface treatments were compared. One was with BHF dip etch and the other was with RCA clean.

The basic fabrication process used is as follows:

1) initial oxidation
2) mask #1 - base
3) boron implant
4) oxidation and drive-in
5) mask #2 - emitter
6) arsenic (or phosphorus) implant
7) oxidation and drive-in
8) mask #3 - polysilicon contact windows
9) polysilicon deposition (LPCVD or PECVD)
10) arsenic (or phosphorus) implant
11) mask #4 - polysilicon pattern
12) polysilicon annealing
13) mask #5 - metal contact windows
14) mask #6 - metal pattern
15) metallization (sputtering Al-Si)

To carry out the above process, preliminary control devices and polysilicon emitter devices were fabricated and tested. Once these results were evaluated, a set of new photoplate masks were designed and process modifications were made. The process design was simulated by SUPREM III simulator while the test mask set was designed and laid out on the graphics system available at Purdue university.

3.1.1 Preliminary Control and Polysilicon Devices

Several fabrication runs were made to determine what problems might occur in modifying Purdue's standard bipolar process to accommodate the polysilicon emitter devices. Standard phosphorus doped emitter bipolar transistors were developed and fabricated in our laboratories. The emitter was 100μ by 80μ and the total base was 217μ by 120μ. It must be noted that these devices were not made with a buried layer and hence would have large collector resistances. The emitter junction depth was simulated as 0.35μ and the base width as 0.52μ.

With the control device as a reference, several wafers were processed together through the base diffusion and drive steps. For the standard BJT, the collector contact and emitter were implanted with phosphorus and diffused simultaneously. For the polysilicon emitter devices the emitter window was not opened in the oxide for the implant, but the window for the collector was opened. Due to the fact that the polysilicon emitter devices did not have the implanted emitter, they would have larger base widths as compared to those of the standard BJT. Therefore, we could not expect as large a beta enhancement with the polysilicon emitters as would be the case if the base widths are the same between them.

The polysilicon was deposited after opening windows in the emitter of the polysilicon emitter devices and trying two types of surface treatments. One set of wafers was given a buffered hydrofluoric acid (BHF) dip to remove as much of the native oxide as possible; the other set was given the RCA clean[9] which creates a thin 15~20Å silicon-dioxide layer. The RCA clean consisted of a ten minute boil in a solution of NH_4OH:H_2O_2:H_2O in proportion 1:1:5, followed by a ten minute boil in a solution of HCL:H_2O_2:H_2O in proportion 1:1:6. The polysilicon was deposited in the LPCVD tube at 620 ° C for 50 minutes and then doped with phosphorus for

20 minutes at 900 ° C.

The polysilicon emitter devices with a BHF dip would probably have a nearly oxide free interface and represent the case of some impurities diffusing from the polysilicon to form a very shallow emitter or create the emitter-base junction near the surface of the monosilicon base region. Those with the RCA clean surface treatment would have the oxide barrier to give a heterostructure to the emitter-base and hence a good hole blocking barrier to the base current component (due to the holes injected to the emitter), as described by the tunneling theory in chapter 2. The RCA devices have shown to produce a good beta enhancement over the standard BJT. Table 3.1 shows the results of these preliminary fabrication runs after measuring the transistor characteristics with an HP4145A Semiconductor Parameter Analyzer. In the table only the peak betas are recorded and averaged over the number of samples measured. The standard or control BJT had the betas in the range expected from the standard process. Typically they have an Early voltage of about 68 to 74 volts. For the polysilicon emitter device with a BHF dip the betas were much smaller due to the large base width. The RCA clean devices had a maximum beta enhancement of greater than 3 and an average of 2.66 over the control devices. Maximum beta would have been greater if the base width of the polysilicon emitter device is same as that of the standard BJT. Figures 3.2 through 3.4 illustrates some of the I-V data taken on the devices.

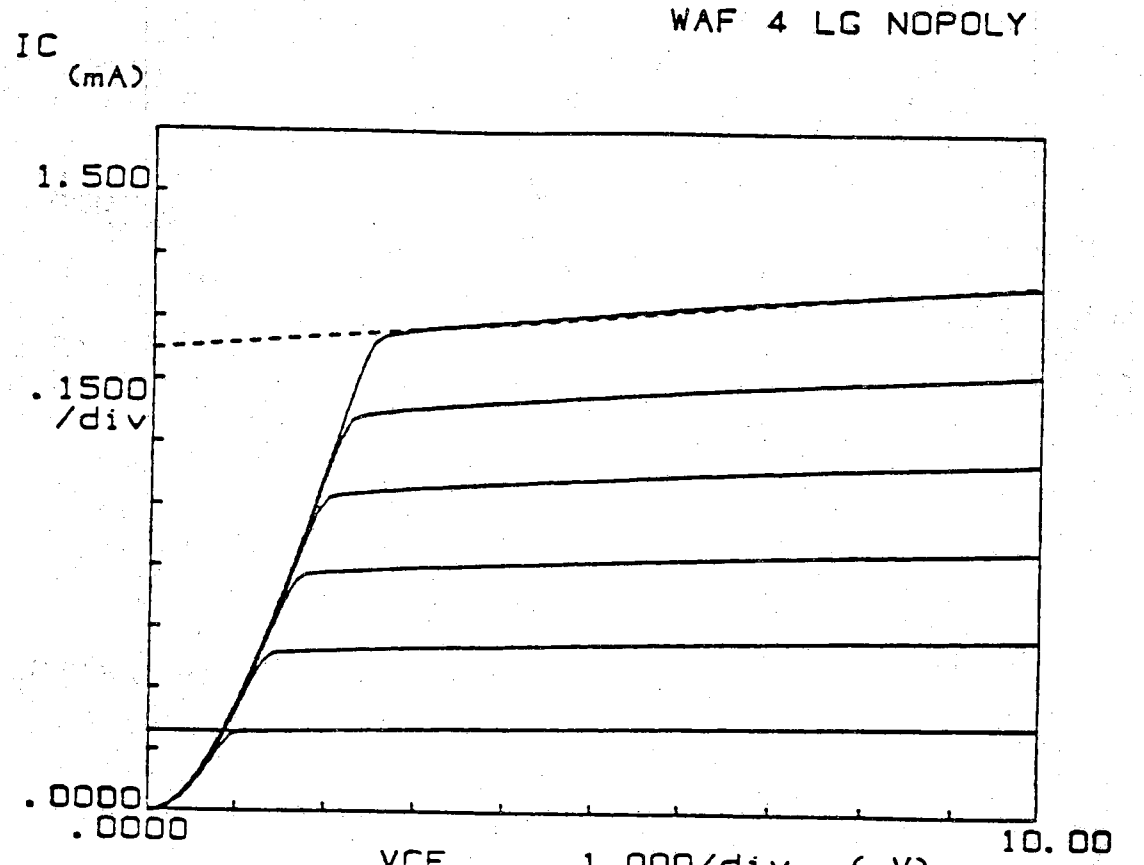
3.1.2 Layout

The preliminary results were quite encouraging and gave several insights into the design of a better fabrication process (to include poly-contacted emitter devices) and to layout a group of process evaluation test structures and BJT transistors. The layout is divided into four quadrants and each quadrant consists of three dies of transistors, two test areas, and one separated area including resolution marks and alignment keys.

Each die consists of transistors with same emitter size and four different types of devices formed into an array. They are labeled as 'sub', '1con', The emitter sizes are 18μ x 18μ, 28μ x 28μ, and 36μ x 36μ. The variations in emitter size are mainly to compare the differences in I-V characteristics and performances with area. Things that can be compared are current gain, contact resistance, base resistance, and potential drop in the base region,

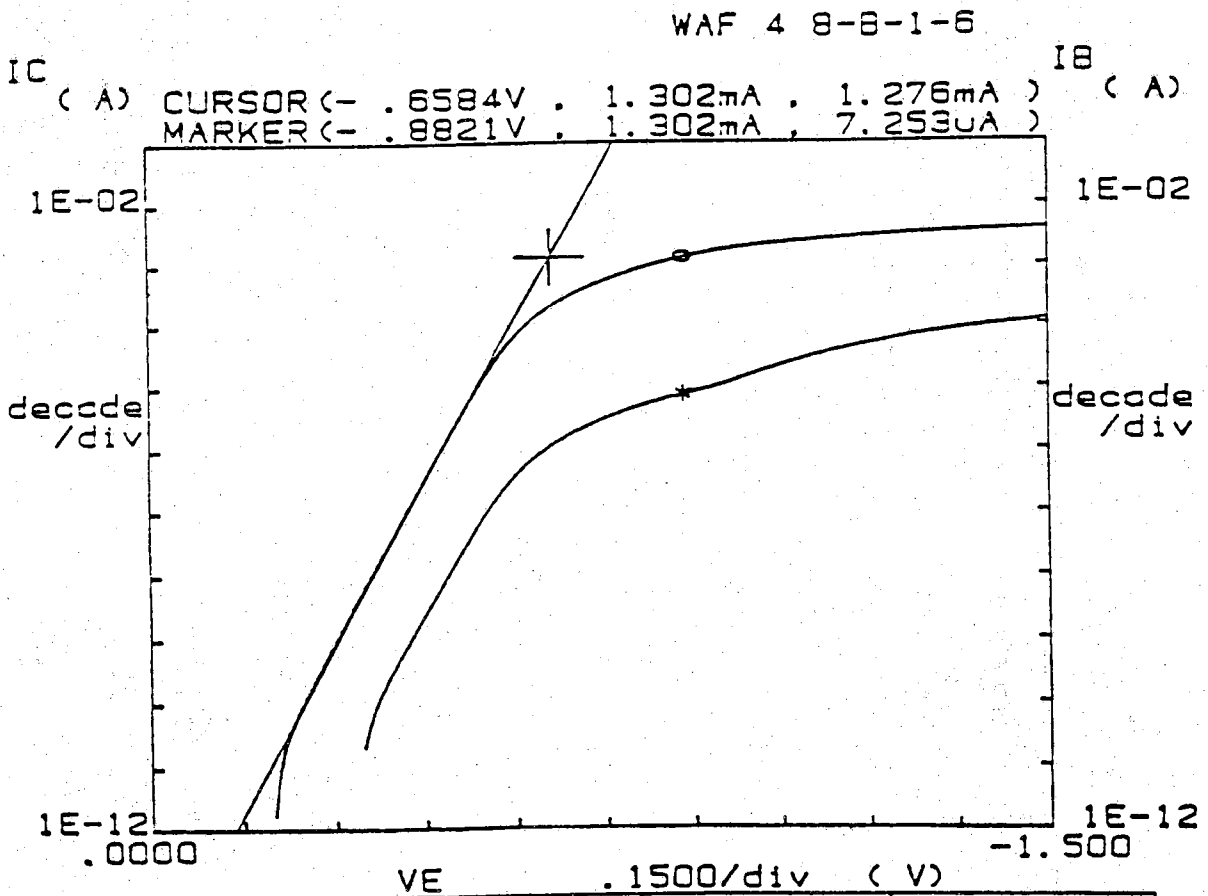
Table 3.1 Maximum current gains of preliminary devices.

Devices	Numbers Observed	Peak Beta Max.	Peak Beta Min.	Peak Beta Average
Control BJT	6	206	175	191.5
RCA Poly	2	635	386	510.5
BHF Poly	11	60.4	4.2	18.55



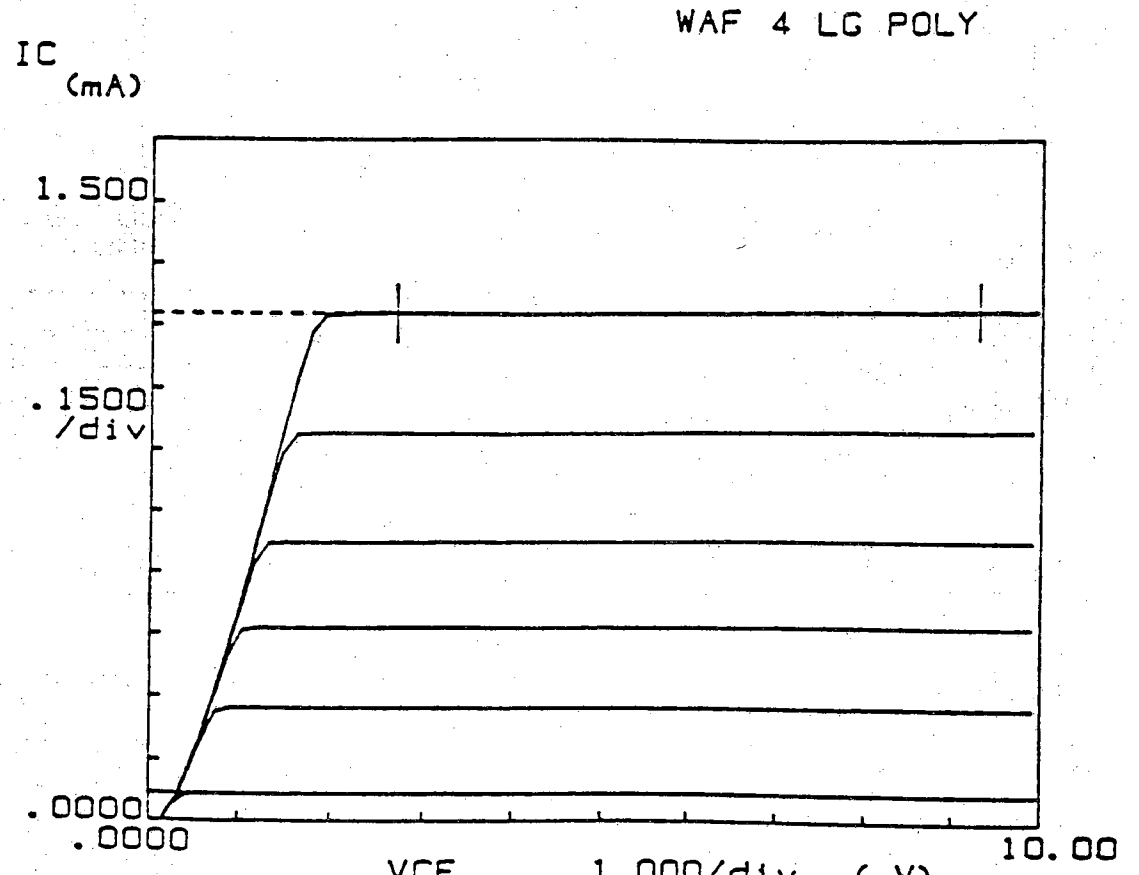
	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	2.60E-06	385E+03	-74.2E+00	193E-06
LINE2	16.5E-06	60.7E+03	-68.2E+00	1.12E-03

Figure 3.2 I_C versus V_{CE} characteristics for preliminary control BJT.



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	-17.3E+00	-57.7E-03	-825E-03	4.99E-15
LINE2				

Figure 3.3 I_B versus V_{BE} characteristics for preliminary control BJT.



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	100E-09	9.98E+06	-672E+00	67.4E-06
LINE2	1.07E-06	938E+03	-1.15E+03	1.23E-03

Figure 3.4 I_C versus V_{CE} characteristics for preliminary polysilicon emitter device with BHF dip etch.

etc. The base regions and collector regions differ depending on the emitter size. The base regions range from 52μ x 30μ with 18μ x 18μ emitters to 124μ x 80μ with 36μ x 36μ emitters. Their large variance is due to two additional masking steps, which are polysilicon contact windows and polysilicon contact definition. The collector regions vary from 30μ x 18μ to 60μ x 36μ respectively. The bonding pads are all 200μ x 200μ to conserve space and yet have easy bonding.

The test wafer layout of a full wafer is shown in Figure 3.5. It is noted that the layouts in each quadrant have the same components and the four quadrants are almost symmetrical. A layout of the quadrant I of the wafer is shown in Figure 3.6. As shown in Figure 3.6, every transistor is numbered so that they can be identified when one tests these devices. In one quadrant there are twelve devices of each type and size. Eventually, forty eight devices of each type and size are available. The large features on the outer side of the wafer are for the spreading resistance probe measurements, one for each step of the process. Note they are arranged around each quadrant.

There are two process related test areas in each quadrant. The layout of test areas is used to determine process characteristics, and to help debug the transistor array. One test area, as shown in Figure 3.7, consists of four sets of 1024 transistors connected in parallel, in which each set consists of transistors of the same type and three very large transistors. The three large transistors in this test area are '1con', 'em', and 'sub' devices with 256μ x 256μ emitters, and 288μ x 368μ base regions. They are fabricated for the comparison with other small devices in the other areas of that quadrant. They are good for comparison since they have less edge effect from the perimeter due to very large base and emitter regions. The 1024 transistors connected in parallel have the smallest emitter size, 18μ x 18μ, and share a common collector. They are used to check the quality of the metal contacts to different types of the transistors and to compare area to perimeter effects.

Figure 3.8 shows the other test area and its elements, which are resistors, contact chains, diodes, and capacitors. Resistors are included in each quadrant to measure the sheet resistances of the different regions corresponding to transistors. These regions are represented by the base diffusion, emitter diffusion, base pinch resistor under emitter region, doped polysilicon, and base pinch resistor under polysilicon.

The base, emitter, and doped polysilicon sheet resistances must be reasonably low to avoid excessive voltage drops in both control devices and

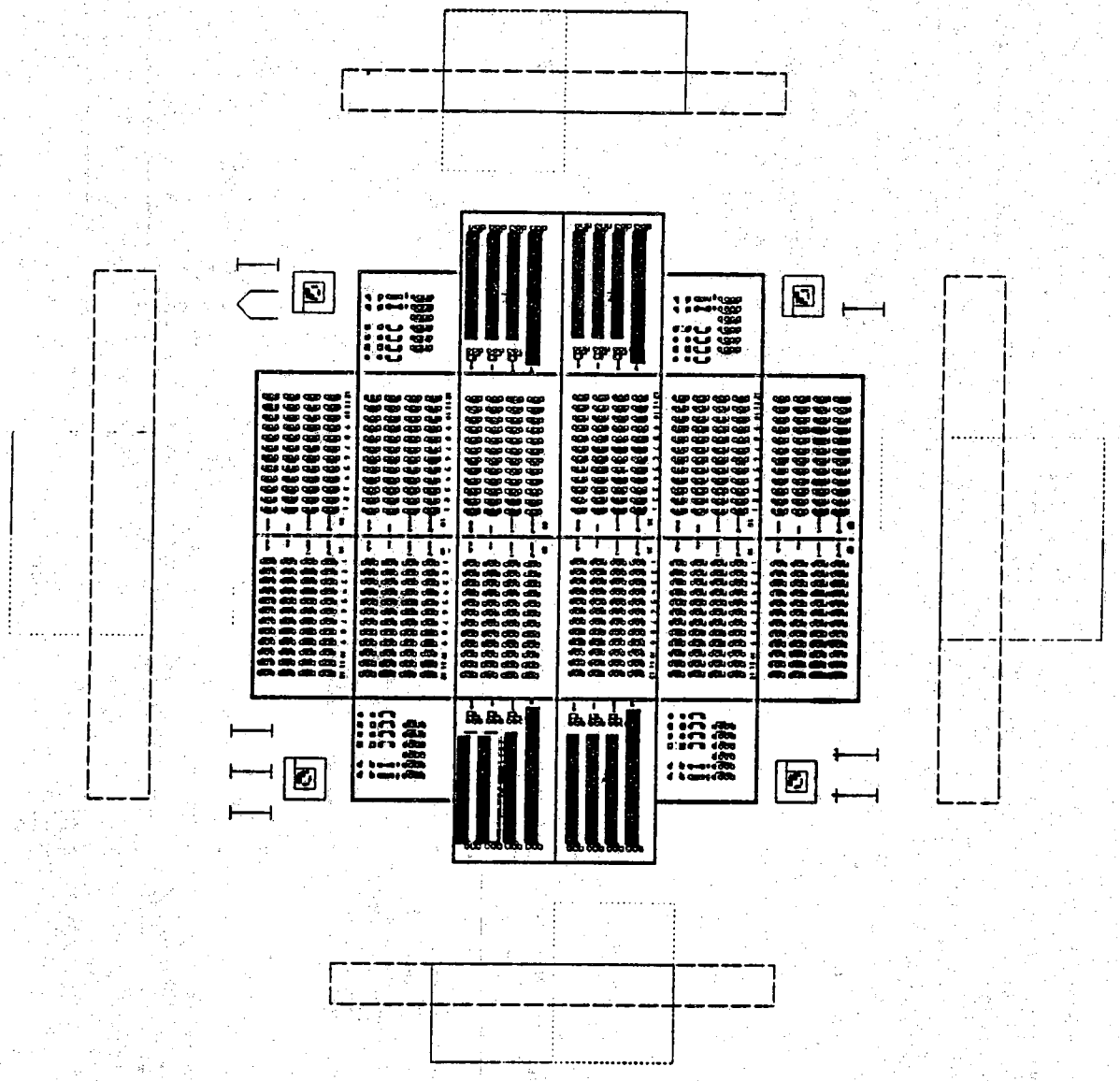


Figure 3.5 Full die of the test wafer layout.

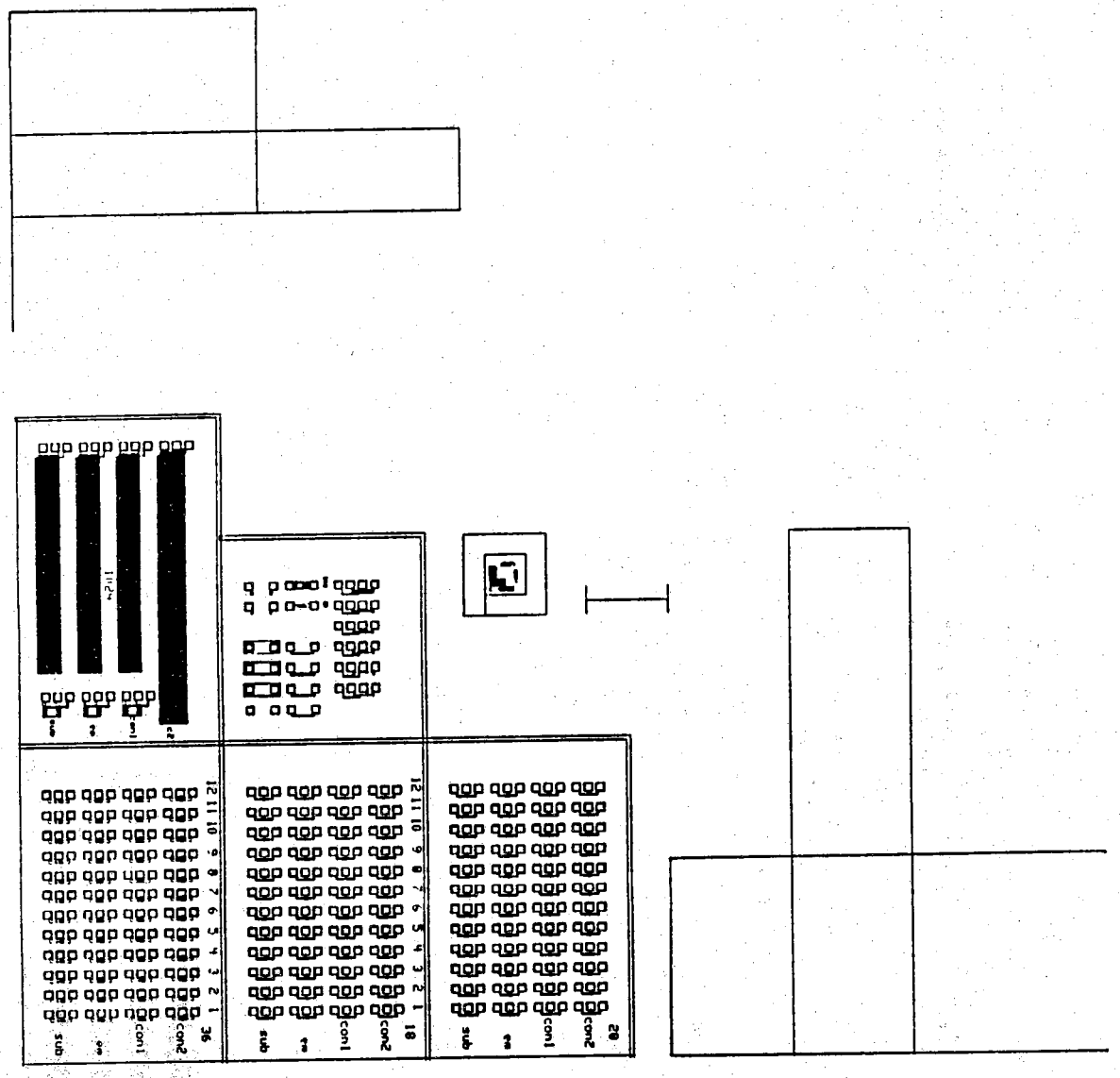


Figure 3.6 Quadrant I of the test wafer.

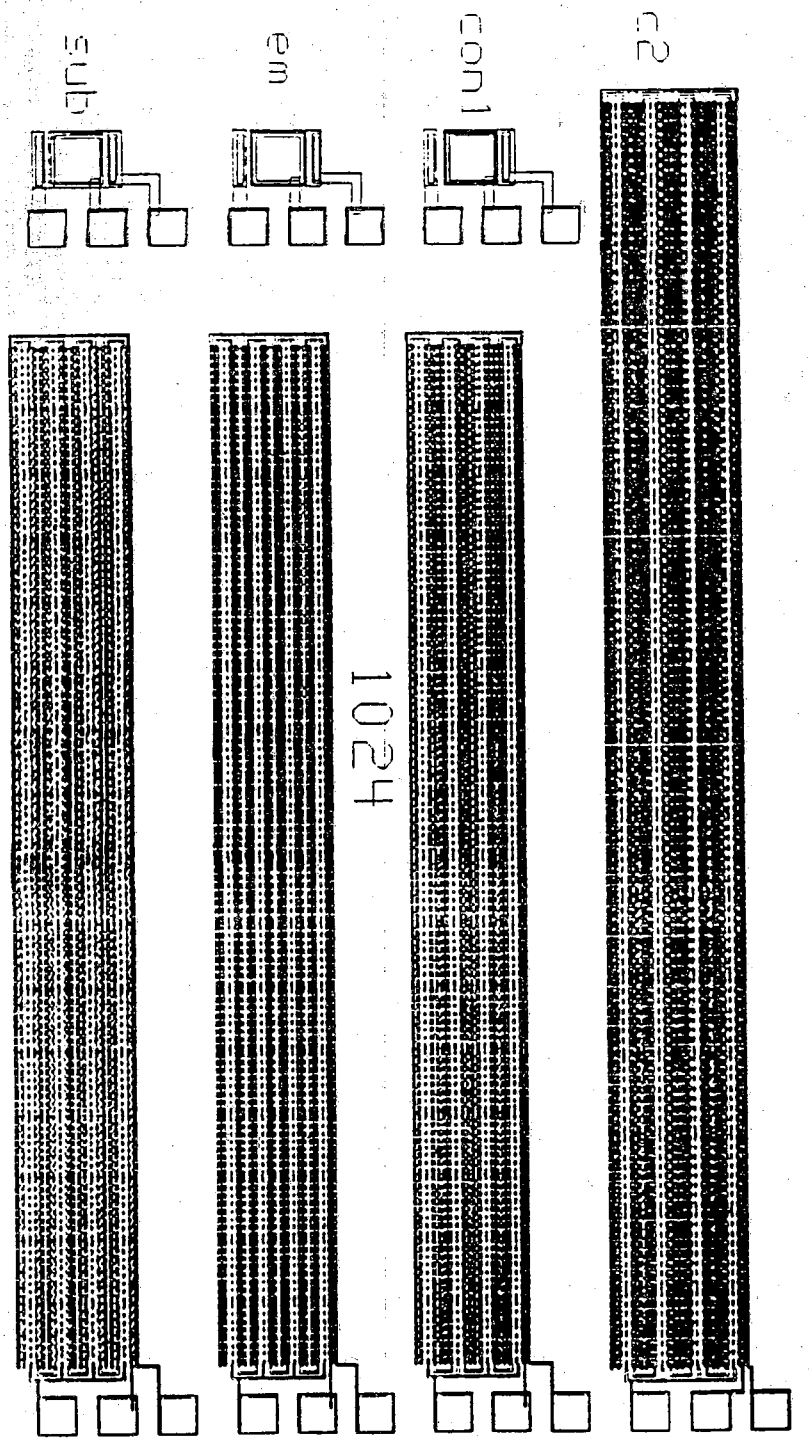


Figure 3.7 Test area of three large transistors and four types of 1024 transistors connected in parallel.

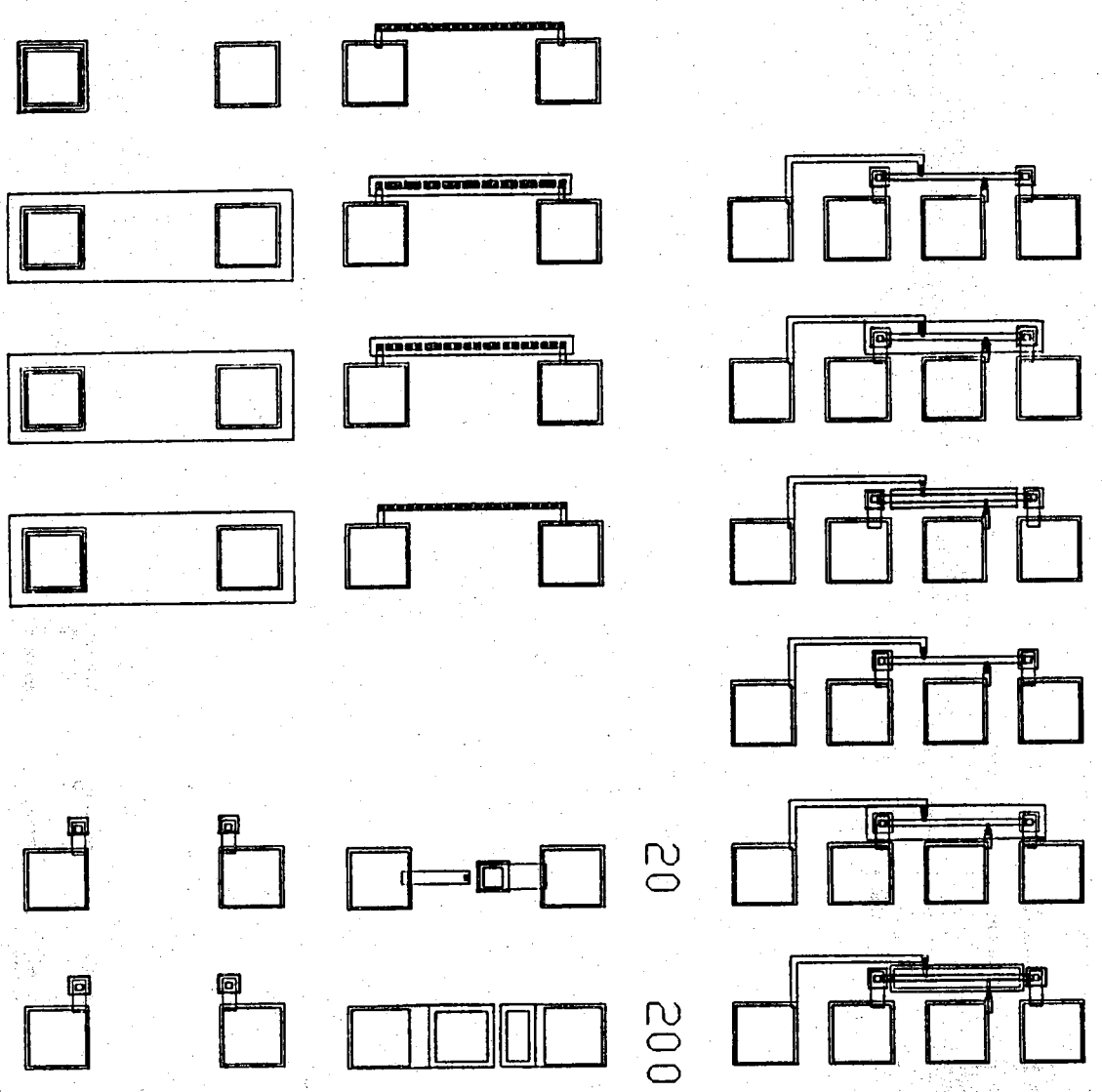


Figure 3.8 Test area containing resistors, capacitors, chain of contacts, diodes, and substrate contacts.

in polysilicon contacted emitter devices. These resistances also can be used to check the accuracy of the SUPREM simulations. Furthermore, they can be extracted for the purpose of simulating future circuits. The contact chains are used to check the quality of the metal to semiconductor contacts to the various silicon and polysilicon regions.

Resolution marks and alignment keys are located separately from the other parts, as shown in Figure 3.9. All alignments are basically made on the previous mask levels. The resolution marks are used to check for catastrophic errors during the masking and etching steps. The smallest resolution marks are 5μ lines with 5μ spaces.

The final set of masks include 48 devices of each type and size (4 types and 3 sizes), two test areas, and the area including resolution marks and alignment keys.

3.2 Process Development

The objective of this thesis lies not only in demonstrating that the polysilicon contacted emitter devices have higher current gains than conventional aluminum contacted devices but also in showing that the polysilicon contacted emitter devices can be fabricated in a consistently reproducible manner.

From the results of preliminary devices, the polysilicon emitter devices (em) with an intentional oxide layer made with RCA cleaning, seem to have better beta enhancement than the devices with BHF dip etch. The use of intentional chemically grown interface oxides as a tunneling barrier to hole injection has been shown to give the lowest base currents. However, the oxide barrier significantly degrades the high performance capability of the devices by increasing the emitter resistance by an order of magnitude and increasing the low current leakage [9,10].

For small emitters, this series resistance severly limits the speed and transconductance of the BJT device. In addition, the chemical oxide slows the diffusion of arsenic, when using the polysilicon as a diffusion source, from the polysilicon layer into the single crystal substrate. The emitter junction that is formed during annealing can be too close to the polysilicon/monosilicon interface, resulting in nonideal diode behavior [21]. Annealing at high temperatures can reduce the emitter resistance and the

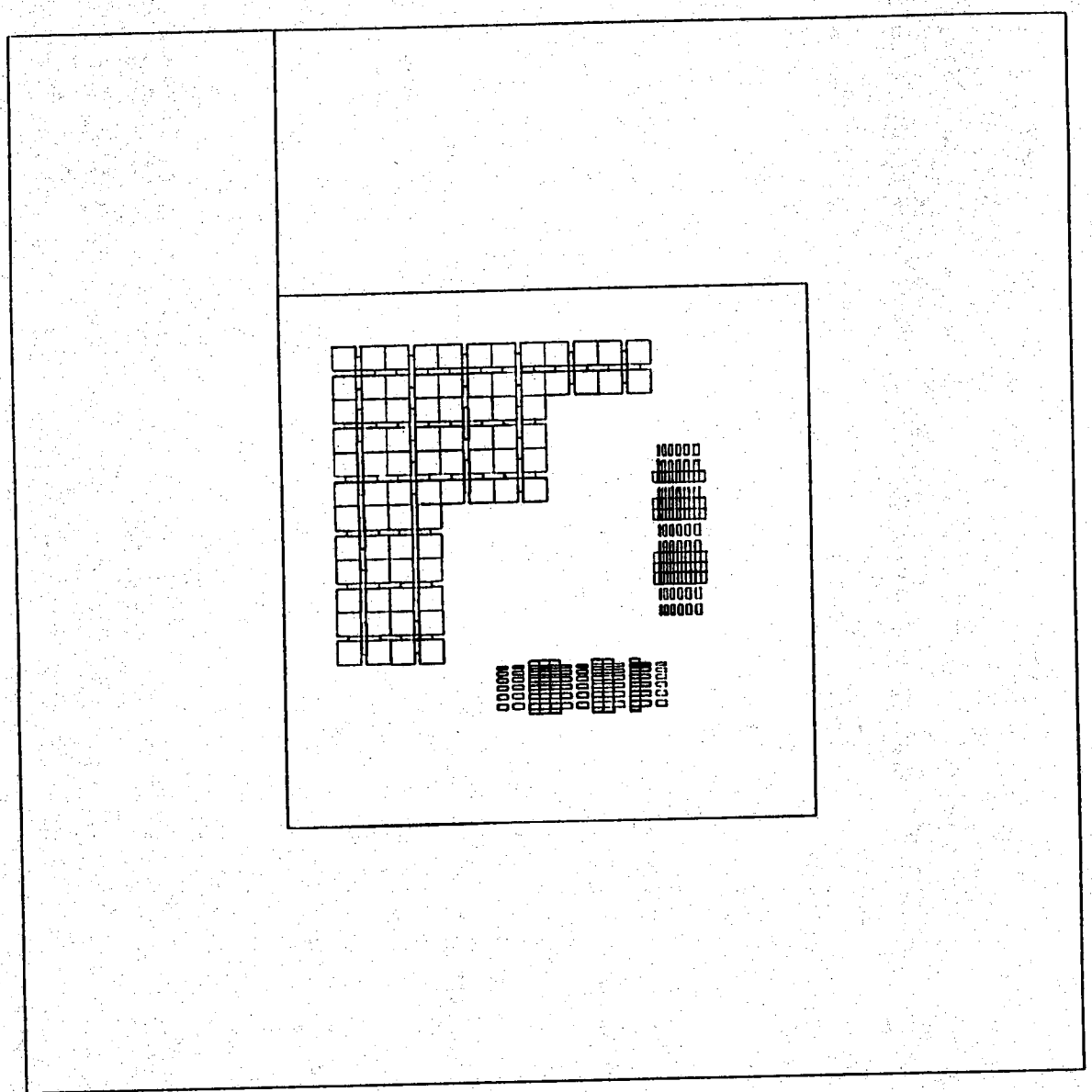


Figure 3.9 Resolution marks and alignment keys.

leakage by breaking up the chemical oxide and diffusing the junction deeper into the substrate. However, these improvements are achieved at the sacrifice of a higher base current, a wider base width, and a nonuniform interface.

It is known that the common-emitter current gain, β, of silicon n^+pn bipolar transistors with shallow emitters depends strongly on the emitter technologies. Particularly, for the polysilicon contacted emitter devices, the high gains are only obtained if the monocrystalline part of the emitter is extremely thin ($\leq$ 0.1 μm) so that the substrate recombination of holes in that region is minimized [22]. The polysilicon emitter devices (em) may produce higher current gain enhancement than the polysilicon contacted emitter devices (1con). However, they have been shown to produce variable beta enhancement ranging from 0 to 10,000. This implies reproducible diffusions are difficult to obtain. Moreover, the polysilicon emitter devices (em) have different emitter and base impurity profiles in the substrate silicon indicating that the direct comparison with the control devices (sub) is not appropriate.

On the contrary, the polysilicon contacted emitter devices and the control devices have almost identical substrate doping profiles, so that they can be directly compared. Observed differences in device characteristics can be attributed to the polysilicon contact effect. The advantage of the polysilicon contacted emitter device structure is that the doping profile in the monosilicon substrate is only minimally affected by the polysilicon for short annealing period.

Therefore, in this chapter, fabrication procedures and experimental results will be presented on the polysilicon contacted emitter devices (1con) without any intentional interfacial oxides. Much of this work is to investigate the effects of and how to remove any "native" oxide at the interface. Procedures were simulated with SUPREM III in order to estimate the process parameters for the fabrication development.

3.2.1 Process Targets

As mentioned earlier, the main objective is to establish the fabrication procedures that would produce consistently reproducible polysilicon contacted emitter devices with enhanced current gain over the conventional

aluminum contacted devices.

First of all, in order to obtain high current gains, the base width should be as thin as possible, so that the average diffusion length of the minority carrier, electron in this case, is much longer than the base width. Bipolar devices that have been properly scaled down, however, have a limiting base width of about 25 nm [23]. Because the base width is determined by the difference between the depths of the base-collector junction and the emitter-base junction, narrow base widths require the emitter depth to be reduced proportionately to maintain base width control and reproducibility. Another issue that should be considered in the evaluation of a given doping profile is the ratio of doping concentration of the base and emitter. The base doping must be low enough so that it does not degrade emitter injection efficiency. If it is too low, however, the collector will punch through the emitter. Because punch-through must be avoided, it is necessary to consider the voltage that will be applied to the device terminals. Depletion layer widths must be calculated to confirm that punch-through will not occur at reasonable voltages.

The effect of very high doping concentration in the emitter should be considered. As the emitter doping becomes very high the bandgap narrowing and the Auger recombination effect cause reductions in the current gains. The decrease in bandgap causes the intrinsic carrier concentration to be higher. This in turn causes the injected, from base to emitter, minority carrier concentration to increase and results in a corresponding decrease in current gain. The Auger effect is a recombination mechanism that involves the direct recombination between an electron and a hole with a transfer of energy and momentum to a free electron. At high carrier concentrations, Auger recombination becomes important. There is also a reduction in the minority carrier diffusion length. Since the emitter diffusion length is decreased, the emitter injection efficiency is also decreased [24]. Therefore, the emitter junction depth must be reduced to minimize the Auger effect. The shallow emitter junction depth is also necessary for reducing the sidewall effects, which play a significant role in the performance of the transistor when the lateral dimensions of the emitter are in the same order of magnitude as the emitter-base junction depth [25].

Secondly, in order to have the capability of fabricating the polysilicon contacted emitter devices in a consistently reproducible manner, it is necessary to have an "oxide-free" polysilicon/monosilicon interface assuming that the polysilicon layer itself dose not make a big effect. The presence of

the chemically grown interface layer with RCA clean creates high base-emitter resistance value, so that eventually the polysilicon contacted devices may reduce the speed of circuit. Also, it is extremely difficult to control the precise thickness of the interfacial oxide layer so that the devices with consistent electrical characteristics can never be fabricated. The devices in this research, therefore, are given an BHF dip etch prior to the polysilicon deposition to minimize any oxide contamination and make a "clean" polysilicon/monosilicon interface. Despite this treatment, a thin layer of contamination forms on the silicon surface during the subsequent exposure of the wafers to water and air. This "native" oxide can also generate high base-emitter resistance, although not as bad as the intentional chemically grown oxide. It is necessary to remove the native oxide to fabricate devices with consistent electrical characteristics. The native oxide layer was found to "break up" by thermal treatment at high temperatures [3]. Another possible technique is the plasma-etch of the native oxide before polysilicon deposition in the PECVD reactor without breaking vacuum. Both methods were studied in this work.

3.2.2. Basic Full Fabrication Process

From several experiments with different parameters and their results, the basic full process with final fabrication parameters was established. The wafer set V3 was fabricated by applying this basic full process. Wafer fabrication runs "A" through "U" were parts of the basic full process development.

The basic full process consists of two parts, a fixed part that is the same for all BJTs and a variable part concerning the polysilicon contact only. The fixed part includes the process steps that are common to both the polysilicon contacted emitter devices and the conventional devices. They are gettering, initial oxidation, base implant and drive-in, emitter implant and drive-in, metallization and its annealing. The main purpose of the fixed part is to create good shallow emitter "substrate" devices so that one can observe the beta enhancement from the polysilicon contacted emitter devices over the conventional aluminum contacted devices on the same die. The variables are the process steps which can vary over the different set of wafers fabricated. They are surface treatment before polysilicon deposition, polysilicon deposition technique and its parameters, and arsenic implant into

polysilicon and its annealing. The purpose of the variable part is to optimize the parameters so that one can obtain not only a good beta enhancement with low contact resistance but also small variations in the beta values by making a "clean" polysilicon/monosilicon interface.

3.2.2.1 Fixed Processing Part

The key features of the fixed part of this process are discussed in this section. The starting material is a Monsanto (111) n-type, phosphorus doped silicon wafer with resistivity of 4~6 Ω-cm ($N_D \simeq 1x10^{15}/cm^3$). After initial cleaning of the wafer, which is listed in Appendix A, the wafer is oxidized in order to mask the front side during gettering. A reasonable thickness of 2500Å is chosen to make the oxide easy to etch. This is grown in about 25 minutes at 1000 ° C.

Small concentrations of impurities and defects can have deleterious effects on silicon bipolar devices which lead to very poor yields. Even if the fabrication was done under completely contamination-free conditions a number of process induced defects still limit the circuit yield. This problem has led to a number of studies which have shown the ability of gettering operations in overcoming defects and contamination problems arising during processing. The basic idea of gettering is to remove undesirable defects and impurities from the critical areas on the wafer where the devices are fabricated [26].

Defects and other types of contamination may effect the performance of devices by introducing energy levels within the forbidden bandgap of silicon, where they act as recombination-generation centers and traps. Metallic impurities can result in a direct, unwanted, and often unstable contribution to the electric field in the active area of the devices. These lead to the two major problems frequently encountered in processing, degradation of minority carrier lifetime and increase in the junction leakage current [27].

Several gettering techniques were investigated. Among them, polysilicon deposition on the backside of the wafer has been found to be very effective. The grain boundaries, and high degree of disorder in polysilicon are believed to act as a sink for mobile impurities [28]. After etching the oxide off the back of the wafer, polysilicon deposition was performed in an LPCVD reactor at 620 ° C for 80 minutes to deposit about a 1μ thick layer

on the back.

After the gettering step, the polysilicon and the protective oxide on the front side are etched using the etching techniques described in Appendix B. Another oxidation was performed to provide masking for the base (boron) implant. An oxide layer of 2500Å was grown from wet oxidation at 1000 ° C for 25 minutes.

The base regions are defined on the initial oxide layer using the first mask. Then the oxide in the base regions are wet etched with buffered hydrofluoric acid. With the 2000~3000Å oxide thicknesses and with the reasonable size geometries, this etch performed satisfactorily. In order to minimize the base-emitter junction depth and thus to have a narrow base widths and a shallow emitter, the base implant is done at the energy of 25 keV, which is the lower limit for producing good metallurgical junctions. The boron dose was chosen as $3 \times 10^{13}/cm^2$ so as to prevent punch-through because the emitter was very heavily doped.

The second oxidation is for the base drive-in. A shorter oxidation time yields a steeper concentration profile. Here, the desired oxide thickness was determined by the energy of the emitter implant. There were two choices in the emitter dopant species, phosphorus and arsenic.

Arsenic has the highest solid solubility of the common n-type dopants. Since the arsenic atom is larger and has much lower diffusion rate than the phosphorus atom, it does not penetrate as far into the silicon as the phosphorus atom. The required high doping concentration in the emitter can thus be obtained with a shallower junction and steeper profile using arsenic as the dopant. As described earlier, a shallow emitter junction is desired in polysilicon contacted emitter devices for higher current gain since it reduces sidewall effects of the base-emitter metallurgical junction. Therefore, arsenic was used for the emitter implant in the single crystal region.

The emitter regions are defined on the second oxide layer using the second mask. The oxide in the emitter regions are etched with the same technique as before, and the arsenic implant is performed at 25 keV. The arsenic dose was chosen as $1 \times 10^{15}/cm^2$ in order to create a steep impurity profile with high doping concentration. The oxide thickness needed to mask the emitter implant was calculated analytically and determined to be

$$0.8 \times (0.02 + 4.3 \times 0.007) = 0.04\mu = 400 \text{ Å}$$

The 0.8 term in this equation is the relative stopping power (ability to stop the ions) of the oxide versus silicon, the 0.02 term is the implant range in silicon, the 0.007 term is the implant straggle in silicon, and 4.3 multiplied by the straggle gives the depth where the concentration drops to 1/10,000 of the peak concentration. This oxide thickness is grown with a 10min, 1000 ° C wet oxidation after the boron implant [29].

The third oxidation is only long enough to activate the implanted arsenic ions, and to anneal the physical defects in the silicon caused by the implant. In this case, a wet oxidation is also used because the faster growing oxide pushes the arsenic at the surface into the silicon as the oxide grows, resulting in a steeper dopant profile. The minimum activation-anneal time was found to be 10 minutes at 900 ° C [30]. A full anneal is critical to eliminate silicon defects which would cause large leakage currents due to Shockley-Read-Hall recombination.

All of the dopants implanted into the surface take advantage of the better dosage and depth control available with ion implantation as compared with pre-deposition tube techniques. All the ion implants were performed by the laboratory technicians. The wafers, dose, energy and dopant species need to be submitted to the technician for processing.

The metallization step is done toward the end of the process and this is also a common step to both polysilicon contacted emitter devices and control devices. Metal patterns are defined with the last (sixth) mask. Then the aluminum alloy sputtering was performed in the Perkin-Elmer RF sputtering system. The aluminum contains 1% silicon in order to prevent spiking. This step is described in Appendix G in more detail. The metallization etch uses the "lift-off" technique to insure that all of the metal between paths are removed. With the silicon incorporated in the aluminum, the standard aluminum wet etch did not work well, leaving behind chunks of metal. The lift-off method is easy to use and gives better pattern definition. After the lift off etch, the metal anneal was performed at 400 ° C in N_2 for 20min to create good metal/silicon contacts.

3.2.2.2 Variable Processing Part

The various processes involved with producing polysilicon are surface treatment prior to deposition, deposition, dopant implant, and oxidation. All of these processes are interdependent with all of the others. There are two techniques that have been used for making the polysilicon contacts, Low Pressure Chemical Vapor Deposition (LPCVD), Plasma Enhanced CVD (PECVD). In this section, the techniques and parameters used for the basic full process are described. Other techniques are discussed in the next section.

After the fixed part of the process, the polysilicon contact regions are defined on the third oxide layer using the third mask. Then they are subjected to a 3 min BHF dip etch to open the polysilicon contact windows on the monosilicon emitter regions where a polysilicon contacted emitter is desired. The oxides on the control devices (sub) remain to mask the devices. This is immediately followed by the deposition of an undoped polysilicon layer using the LPCVD system. The wafers are positioned vertically in the deposition tub with 1/4" spacing between wafers. They are placed in the center zone of the heated LPCVD reactor. A detailed description of the operation of the LPCVD system is contained in Appendix E.

As previously mentioned, the main objective of these variables is to get a clean polysilicon/monosilicon interface without a native oxide. The relative importance of this interface and of the bulk properties of the polysilicon in influencing the emitter saturation current has been examined by other researchers [2,3] by studying polysilicon deposition, annealing temperature, doping level, and polysilicon thickness.

The thickness of the polysilicon is a process parameter that can be varied and the research has shown that the optimum polysilicon is not thicker than 2000Å. Polysilicon thickness greater than 2000Å are not of interest since there is little improvement in the emitter injection efficiency past this point. Ning and Issac [2] observed a weak dependence of base current density on polysilicon thickness once the polysilicon contact is thicker than 1000Å. According to their results, the thinner polysilicon contacted devices show a higher base current with all the devices having the same polysilicon/monosilicon interface properties. This indicates that the hole current is not determined by the polysilicon/monosilicon interface properties but by the transport of holes in the polysilicon layer. Therefore, the $0.1 \sim 0.2\mu$ thick polysilicon layer was determined desirable for the

polysilicon contact.

The experimental parameters are available for the Purdue Solid State Laboratory LPCVD system [31]. The growth rate of polysilicon at 620 ° C, 200mT, flow rate of 50sccm is about 120Å /min. Therefore, deposition for 10min would produce a polysilicon of little more than 1000Å thick.

The following step is the implantation of the polysilicon layer with dopants. In order to optimize the device performance within the constraints of the existing process, two process parameters were varied:

i) the species used to dope the polysilicon and
ii) the dose and energy of the implanted dopant

Functional polysilicon contacted emitter devices with phosphorus doped polysilicon have been reported in literature, but it was shown that using arsenic as the doping species would result in a superior impurity profile [2]. Therefore, the polysilicon layer is implanted with arsenic and annealed in wet oxygen.

Neugroschel et al.[15] showed that segregation of arsenic to the polysilicon/monosilicon interface is essential in obtaining low values of base current. Similarly, Patton et al.[3] observed a dramatic reduction in the emitter saturation current density and the surface saturation current, which were described in chapter II, as the arsenic concentration increased from $3.3x10^{19}$ to $1x10^{20}/cm^3$. However, above $1x10^{20}/cm^3$ the dependence was weak.

Polysilicon doping levels below $1x10^{20}/cm^3$ should not be used for typical devices because of the high series resistance and high base current that would result. The high base current observed at the lower doping level can be explained by high recombination at grain boundaries in the polysilicon including the polysilicon/monosilicon interface, pseudo-grain boundary, due to a high density of interface states. These trapping densities result from the concentration of defects and dangling bonds which are present at the grain boundaries. The segregation of arsenic has been shown to affect the electrical activity of these regions. Several mechanisms have been proposed to explain this change:

1) arsenic segregation to dangling bonds at the grain boundaries, which decreases the density of trapping states
2) segregation to sites other than dangling bonds, where the dopant atoms can be easily ionized
3) arsenic segregation that stimulates recombination of the grain boundaries and, consequently, modifies the defect content of these regions [32].

For higher doping levels, $1\sim2x10^{20}/cm^3$, recombination at the polysilicon/monosilicon interface and at the grain boundaries in the polysilicon is reduced significantly, resulting in extremely low values of the surface saturation current. However, this current decreased only slightly as the doping level was increased from 1 to $2x10^{20}/cm^3$. This was explained by the effects of arsenic segregation having either saturated or little additional segregation occurring at these higher doping levels. In this higher doping regime, it was found that the most significant parameter is the time and temperature of the anneal.

As the arsenic concentration in the polysilicon was increased from 2 to $5x10^{20}/cm^3$, the surface saturation current increased. This increase can be explained by a lower minority carrier lifetime in the polysilicon due to the higher doping level. As a result, recombination should increase in the interior of the polysilicon grains and in the regions of the polysilicon layer that might have realigned epitaxially to the monosilicon substrate.

During annealing, some arsenic would segregate in the grain boundaries where they become electrically inactive. The active carrier concentration in the polysilicon was found to be considerably lower than the chemical concentration due to dopant segregation to the grain boundaries [32,33]. Therefore, in order to achieve carrier concentration of $1x10^{20}/cm^3$, higher dose is needed for the polysilicon layer than for single crystal silicon. The implanted energy and dose that produced the desired carrier concentration in 1000A° polysilicon layer are obtained by using an arsenic dose of $3x10^{15}/cm^3$ at an energy of 25keV. The implant is sufficiently shallow so as to confine the implant damage to the polysilicon layer and away from the interface.

As mentioned previously, for good process control, it is necessary to eliminate the oxide interface and boundary effects altogether. The next step, annealing the polysilicon layer, is the key process that can take care of

both problems.

Earlier work has shown that temperatures of 850 and 900 ° C are required to desorb the native oxide [34]. In XTEM analysis [35,36] and the work of Jergenson et al. [37], the native oxide layer was found to "break-up" at high temperatures and for high doping levels in the polysilicon. When this happens, the polysilicon comes into direct contact with the single-crystal silicon substrate and some fraction of the polysilicon realigns epitaxially to the silicon substrate. More recently, from the experiments of Patton et al.[3], it was shown that in the doping level of 1 to $2x10^{20}/cm^3$, the most significant parameter is the time and temperature of the anneal. When the anneal conditions were 1000 ° C/30min or 900 ° C/3-h, an increase in the surface saturation current occurred compared to a 900 ° C/1-h anneal. The increase in this current with high-temperature processing can be attributed to changes in the structure of the polysilicon/monosilicon interface. The interface for the device annealed for 1-h at 900 ° C was shown to be abrupt and few signs of epitaxial regrowth existed in XTEM examination. However, as the time or temperature of the anneal is increased, the native oxide breaks up and epitaxial realignment occurs. When the anneal conditions were increased to 1000 ° C/30min, epitaxial realignment structures extending several hundred angstroms into the polysilicon were found to cover almost the entire emitter surface, while the oxide forms small inclusions (20~30Å in diameter) within the realigned polysilicon and near the original interface. Here, the "original interface" refers to the position of the polysilicon/monosilicon interface after polysilicon deposition and the "regrown interface" refers to the polysilicon after annealing, i.e., after limited epitaxial regrowth has occurred. For a 3-h anneal at 900 ° C, epitaxial realignment had occurred over a majority of the surface area. Although the realignment structures typically extended no more than 50Å into the polysilicon, they clearly indicated that the native oxide layer had broken up over a large portion of the surface.

The presence of a native oxide just increases the series resistance in the polysilicon contacted emitter devices and incurs extra voltage drop between base and emitter resulting in the degradation in the performance, particularly in high frequency response. The removal of the interfacial oxide by either the removal of the oxide layer due to heat treatment or the epitaxial realignment at the interface will create a good low resistance contact between the polysilicon contact and the crystalline emitter. Since one merit of the polysilicon contact is the extension of the emitter without

having its sidewall effects, the polysilicon contact should not cause a high resistance in order to provide a beta enhancement to the polysilicon contacted devices over the metal contacted devices.

For the polysilicon contacted emitter devices, the annealing time must be as short as possible so that it does not change the emitter junction depth and the base width appreciably. Therefore, the annealing was done at 1000 ° C for 10min. After the implantation, the polysilicon patterns that cover the polysilicon contact windows are defined with the fourth mask and rest of the polysilicon is etched with RPZ poly etching. Then these regions are annealed in wet oxidation. This anneal is long enough to obtain a uniform doping level in the polysilicon and the temperature is high enough to break up a large portion of the interface oxide resulting in a low emitter resistance. Since the fraction of arsenic that outdiffused into the single-crystal substrate is small, the average chemical concentration of arsenic in the polysilicon is approximately the dose divided by the polysilicon thickness.

The fifth mask defines contact areas for metal contacts. After the contact windows are opened with a BHF etch, the metallization was done as described in the previous section.

3.2.3 Full Process Sequence

The basic full process sequence is as follows:

1) Wafer Clean
2) Hydrogen Burn Oxidation - 25min at 1000 ° C
3) Mask Front - AZ1350 Photoresist
4) BHF Etch (Back)
5) Remove Resist and Clean
6) Polysilicon Deposition (1μ) - 80min at 620 ° C
7) Mask Back - AZ1350 Photoresist
8) RPZ Poly Etch and BHF Etch (Front)
9) Remove Resist and Clean
10) Hydrogen Burn Oxidation - 25min at 1000 ° C
11) Define Mask Level #1 - Base Region
12) BHF Etch - 3min
13) Remove Resist and Clean

14) Boron Ion Implant - $3x10^{12}/cm^2$ at 25keV
15) Wafer Clean
16) Hydrogen Burn Oxidation - 10min at 1000 ° C
17) Define Mask Level #2 - Emitter Region
18) BHF Etch - 3min
19) Remove Resist and Clean
20) Arsenic Ion Implant - $1x10^{15}/cm^2$ at 25keV
21) Remove Resist and Clean
22) Hydrogen Burn Oxidation - 10min at 900 ° C
23) Define Mask Level #3 - Poly Contact Window
24) BHF Etch - 3min
25) Remove Resist and Clean
26) Polysilicon Deposition (0.1μ) - 8min at 620 ° C
27) Arsenic Ion Implant - $3x10^{15}/cm^2$ at 25keV
28) Define Mask Level #4 - Poly Definition
29) RPZ Poly Etch - 10sec
30) Remove Resist and Clean
31) Hydrogen Burn Oxidation - 10min at 1000 ° C
32) Define Mask Level #5 - Metal Contact Window
33) BHF Etch - 3min
34) Remove Resist and Clean
35) Dry Bake - 10min at 120 ° C
36) Define Mask Level #6 - Metal Definition
37) BHF Dip - 5sec
38) Sputter Al-1% Si - 25min at 100W
39) Lift-Off Etch - 30min in ACE in USC
40) Anneal Al-1% Si - 20min at 400 ° C
41) Test

3.2.4 Results of Wafer Set V3

This basic process produced a large number of working devices in several fabrication runs. Table 3.2 shows the results of the devices made with the basic full process. Mean values, standard deviations, and minimum and maximum values of the current gains for different devices are described in this table. The SUPREM III simulated device characteristics are shown in Table 3.3 with the process for wafer set V3 and the SUPREM III plot of net chemical impurity concentrations versus depth into the structure is shown in Figure 3.10.

Figure 3.11 is a graphical representation which describes the distribution of experimental data of the wafer set V3. A numerical summary of the data, including its range, median, and variance can be obtained with this descriptive statistics. The thick vertical line segment represents a median value of the current gains contained from a number of devices on a same die. The left and right hinge values are approximately the 25th percentile and 75 percentile of the number of points in the data. The left and right whiskers extend to values which represent 1.5 times the spread from the median to the corresponding edge of the box. Any data points falling outside these values are plotted as individual points. This is good for a quick comparison of the current gain for the polysilicon contacted emitter devices (1con) and the shallow emitter control devices (sub).

The devices with two different emitter sizes were tested. Both of them have shown a good current gain enhancement of the polysilicon contacted emitter devices over the control devices. However, the devices with 36μ x 36μ emitter have shown larger beta enhancement and relatively larger beta values compared to the devices with 18μ x 18μ emitters. The variation in peak beta was also smaller for the devices with the larger emitter. These are caused by a larger area/perimeter ratio of the devices with 36μ x 36μ emitter as compared to the devices with 18μ x 18μ emitter. The devices with larger emitter have less side-wall effects with same emitter junction depth, resulting in higher overall emitter injection efficiency by reducing junction recombination current at the surface.

Table 3.2 Comparison of maximum current gains for the wafer set V3.

Devices	Type	Numbers Observed	Median	Standard Deviation	$\frac{\beta(\text{con1})}{\beta(\text{sub})}$
V3-ii-18	sub	7	73.6	1.2	1.715
	con1	10	126.2	14.7	
V3-ii-36	sub	5	77.8	0.8	2.995
	con1	7	232.9	13.7	

Table 3.3 SUPREM III simulated device characteristics for the wafer set V3.

Parameter		Sub	1Con
Poly-contact Thickness (Å)		N/A	928
Junction Depth (Å)	base/emit	0.15	0.16
	base/coll under emit	0.73	0.68
Base Width (μ)		0.58	0.52
Effective Base Width (μ)		0.38	0.37
Sheet Resistance ($\Omega/\square$)	poly-contact	N/A	2,776
	emitter	109.9	65.3
	base-pinch	8,058	6,065
	base	3,517	4,291
Built-in Potential (V)	base/emit	0.97	1.00
	base/coll	0.69	0.71

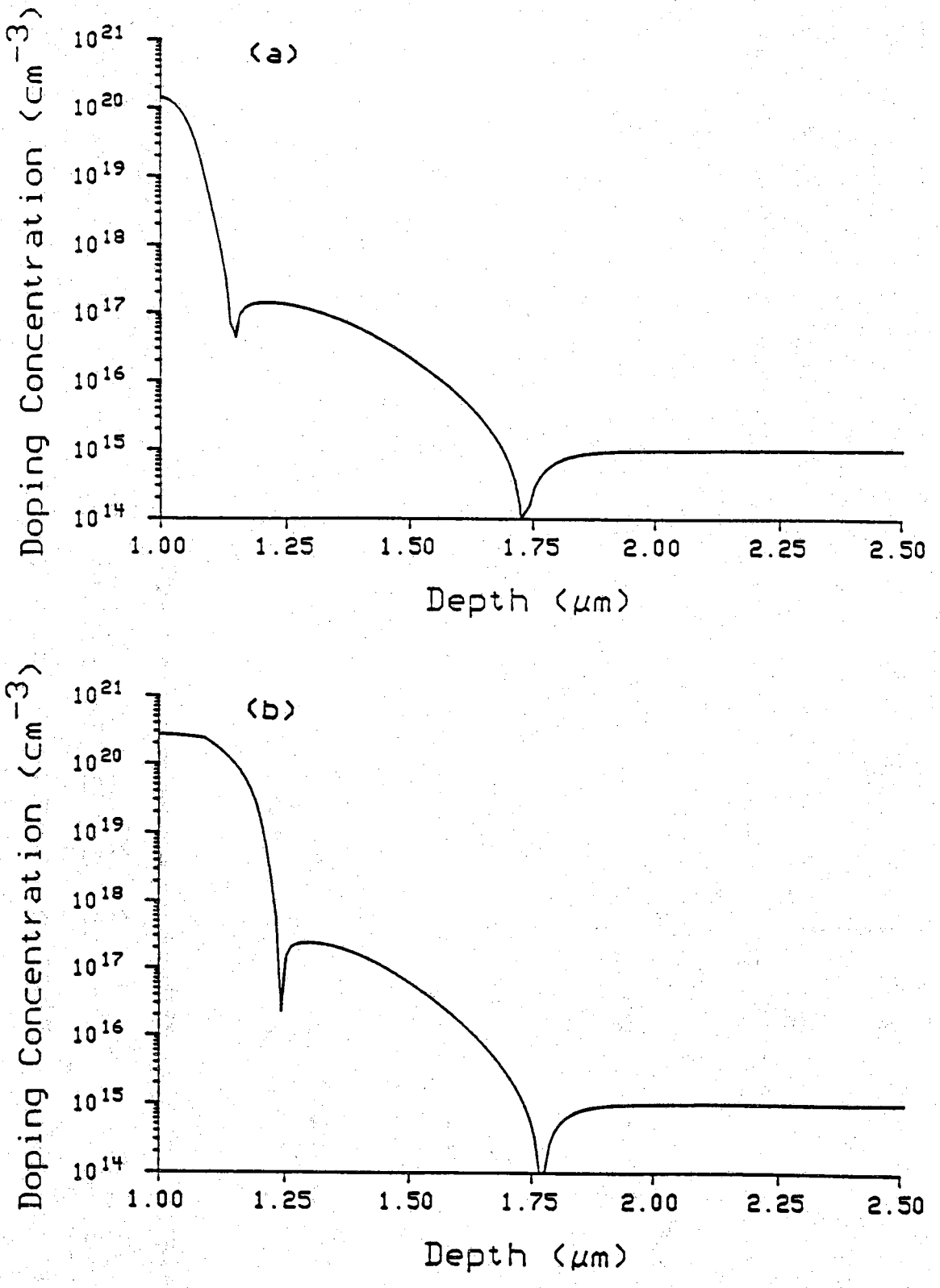
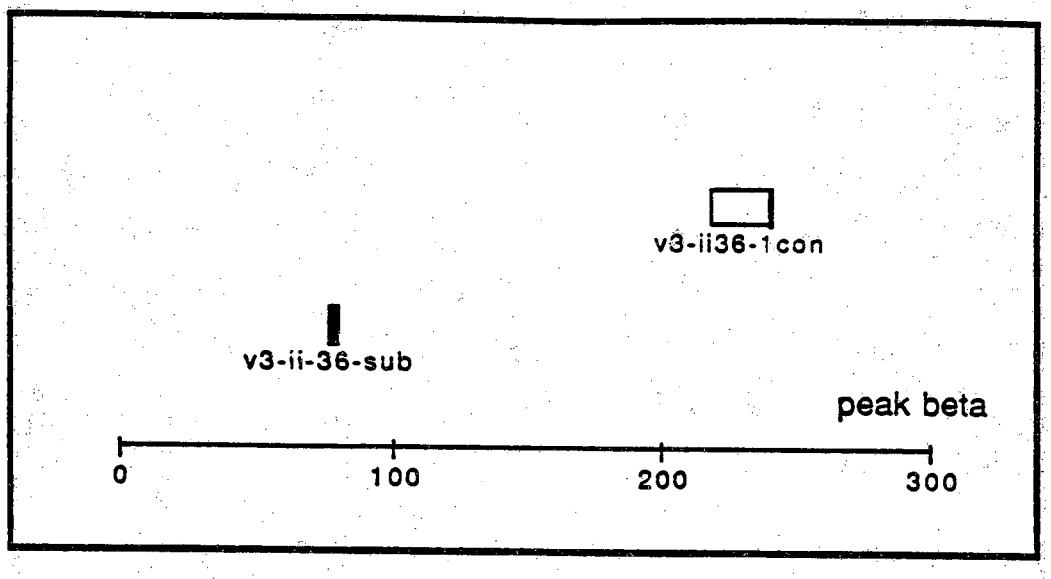
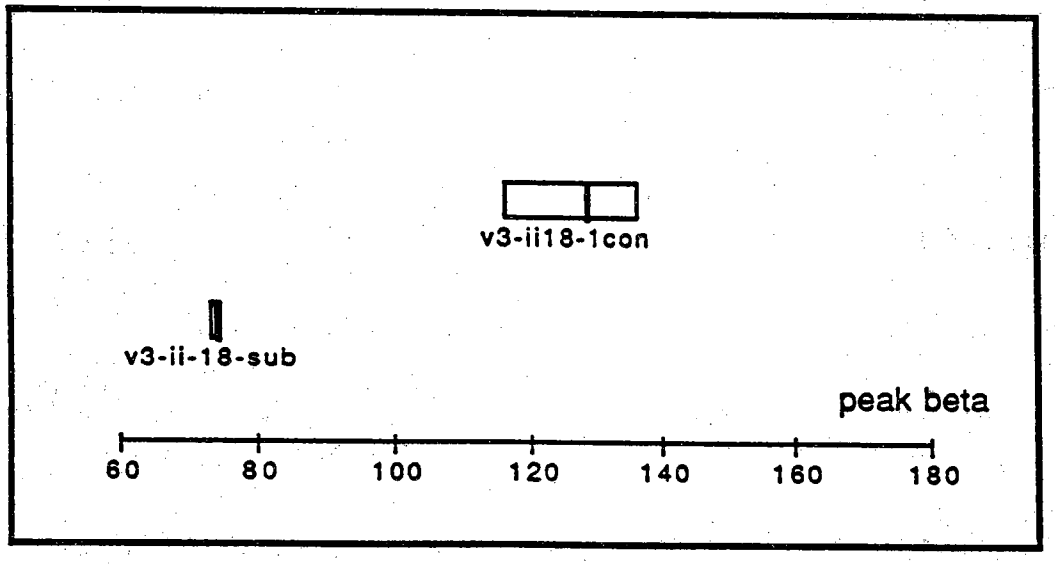


Figure 3.10 SUPREM III simulated plot of net chemical impurity concentrations versus depth into the structure for the wafer set V3: (a) sub and (b) 1con.



(a)



(b)

Figure 3.11 Statistical plot of measured data for the wafer set V3: (a) v3-ii-36 and (b) v3-ii-18.

3.2.5 Process Simulation

This section discusses the process simulations that were done to determine optimum implant energies and doses for the fabrication of polysilicon contacted emitter devices and control devices. The various stages of simulation are presented, leading to a final doping profile. In order to arrive at a process that would produce a device with acceptable characteristics, a process simulator, SUPREM III, was used. Process simulators have made it possible to predict device structures resulting from any proposed fabrication sequence. SUPREM III is an upgraded version of SUPREM II. The key feature of this new version is the capability to model process sequences that utilize polysilicon. The models for diffusion, oxidation, epitaxy, and ion implantation for single crystal silicon have also been improved [38].

There has been considerable work done on the models of polysilicon in SUPREM III. The process involved with polysilicon such as: deposition, oxidation, diffusion, and dopant segregation across the multiple crystallite and grain structure of polysilicon, involve many complex mechanisms. These mechanisms require models of grain growth, dopant segregation, and carrier trapping at the grain boundaries. All of these process are interdependent with all of the others. There are many techniques such as atmospheric pressure CVD, low pressure CVD (LPCVD), sputtering, and plasma enhanced CVD (PECVD), that could be used to deposit polysilicon.

There is, unfortunately, very little data of how the size of the polysilicon grain and dopant distribution vary as a function of deposition technique, temperature, time, pressure, doping process, and layer thickness. SUPREM III uses the most simplistic models. The grains are assumed to be spheres of uniform size. Grain boundaries are known to be a determining factor in the properties of polysilicon layers. Phosphorus and arsenic, in particular, segregate in the grain boundaries, where they become electrically inactive. The segregation at grain boundaries causes the effective doping to be lower. Arsenic is believed to segregate on the polysilicon side of the interface between polysilicon and monocrystalline silicon. This is not modeled accurately by the current version of SUPREM.

Dopant diffusion within polysilicon has been reported to be poorly modeled at this time. Dopant diffusion is known to be more rapid than in single crystal region. This is probably due to the enhanced diffusion that

occurs along grain boundaries. Since the necessary data to model this correctly is unavailable, SUPREM III assumes that the diffusion within polysilicon will be extremely rapid relative to the process time. This causes the polysilicon to be uniformly doped. In order to optimize the device performance within the constraints of the existing process, two process parameters were varied:

i) the species used to dope the polysilicon

ii) the dose and energy of the implanted species.

The thickness of the polysilicon is another process parameter that can be varied but research has shown that the optimum polysilicon thickness is about 1000Å

There is some freedom in varying the annealing time and temperature. This is for annealing after implanting acceptor and donor dopants for the base and emitter, respectively. There are two possible choices for the species to be implanted for the emitter region, phosphorus and arsenic. Modeling of these two species indicated that the arsenic forms shallower emitter junction depth than the phosphorus with the same dose, energy, diffusion temperature and time. Functional polysilicon contacted emitter devices with phosphorus doped polysilicon have been reported in literature, but it was shown that using arsenic as the doping species would result in a superior profile [2]. In general, a shallow emitter is desired for VLSI devices due to decreased lateral diffusion. The boron that is used for the base implant is also included in these profiles.

As mentioned earlier, the higher current gain for a bipolar transistor can be achieved in part by making the base width narrower. The ratio of doping concentration of the base and emitter is also an important factor in the determination of the current gain. Expressing a current gain in the following way allows simple calculation of a current gain from SUPREM III simulated chemical impurity concentrations.

$$\beta_{dc} = \frac{D_B}{D_E} \frac{N_{DE}}{N_{AB}} \frac{L_E}{W} \tag{3.1}$$

where D_E and D_B are the minority carrier diffusion coefficients, N_{DE} and N_{AB} are the doping concentrations in emitter and base, respectively, L_E is the emitter minority carrier diffusion length, W is the width of the base.

An effective diffusion coefficient for the emitter should be determined for use in the above equation for beta. It should take into account the different diffusion coefficients of the monocrystalline silicon and the polycrystalline regions of the emitter. As pointed out earlier, the diffusion coefficient for holes is much less in the polysilicon than in the monocrystalline emitter. The diffusion coefficient for each portion of the emitter is weighted to the width of each region. A formula for the effective diffusion coefficient is:

$$D_{eff} = \left[\frac{\frac{W_1}{W_1 + W_2}}{D_{p1}} + \frac{\frac{W_2}{W_1 + W_2}}{D_{p2}} \right]^{-1} \tag{3.2}$$

where D_{p1} and D_{p2} are the diffusion coefficients in the polysilicon and monocrystalline silicon respectively, W_1 is the thickness of the polysilicon contact which is 1000Å as discussed earlier in this chapter, W_2 is the width of the monocrystalline emitter, and W_1+W_2 is the addition of the monocrystalline emitter and the polysilicon contact.

The diffusion coefficients needed in the calculation of the effective diffusion coefficient are calculated using the Einstein relationship which is:

$$\frac{D}{\mu} = \frac{kT}{q} \tag{3.3}$$

where D is the minority carrier diffusion coefficient, μ is the mobility and kT/q at 300 °C is equal to 0.026V. Even though several models exist for hole mobility in heavily doped silicon, there is disagreement among those models. Due to the lack of information in the literature concerning the minority carrier hole mobility in polysilicon, in this calculation the parameters from the model of Ning and Issac[2], namely D_{p2}/D_{p1} and L_{p1}, are used.

According to the experiments of Ning and Issac [2], $D_{p2}/D_{p1} = 3$ and $L_{p1} = 50$nm were obtained for a peak emitter doping concentration of $1.2 \times 10^{20} cm^{-3}$, where L_{p1} is the diffusion length in the polysilicon. Also, the corresponding L_{p2}, the diffusion length in the monocrystalline silicon, was shown to be 170nm, assuming a hole mobility of 50 cm^2/V-s. The diffusion

coefficient in the monocrystalline silicon, D_{p2} is therefore 1.3 cm^2/s. (electron) mobility value which is obtained from the figure of mobility versus doping concentration. The effective base width, W, is obtained by excluding the transition regions which are the base-collector and the emitter-base depletion regions.

Applying the SUPREM III simulated device characteristics for the wafer set V3 shown in Table 3.3 into equation (3.2), assuming the polysilicon contact to be 1μ, the effective diffusion coefficient for the simulation is calculated as follows:

$$D_{eff} = \left[\frac{\frac{0.1}{0.26}}{0.43} + \frac{\frac{0.16}{0.26}}{1.3} \right]^{-1} = 0.73 \qquad (3.4)$$

Using equation (3.1), the approximated beta for the polysilicon contacted emitter device is calculated.

$$\beta_{1con} = \left[\frac{18.2}{0.73} \right] \left[\frac{7.7x10^{19}}{6.8x10^{16}} \right] \left[\frac{0.26}{0.37} \right] = 20{,}000 \qquad (3.5)$$

By the same method the approximated beta for the metal contacted (sub) device can be obtained.

$$\beta_{,sub} = \left[\frac{22}{1.17} \right] \left[\frac{4.34x10^{19}}{3.96x10^{16}} \right] \left[\frac{0.15}{0.38} \right] = 8{,}130 \qquad (3.6)$$

The use of an effective diffusion coefficient in the beta equation improves the accuracy of the equation of beta. The overall effect of using polysilicon as the emitter contacting material can not be taken into account with such a simple formula. Also, the degradation of beta due to bandgap narrowing is not taken into account, causing beta to be overestimated. The simple formula just allows for a calculation of beta for comparison purposes.

Considering the band gap narrowing due to heavy doping in monosilicon emitter, equation (3.1) can be modified as follows [24]:

$$\beta_{eff} = \beta_{dc} e^{-\Delta E_g/kT} \tag{3.7}$$

where β_{eff} is the effective current gain including the band gap narrowing effect and ΔE_g is the amount of the reduction of the band gap narrowed. Experimental values of the band gap narrowing, ΔE_g, for n-type silicon are readily available in the literature [24]. Taking the value from a plot of band gap narrowing versus doping concentration and assuming the band gap narrowing is same for both the polysilicon contacted emitter devices and the metal contacted devices, the effective beta can be calculated. From equations (3.5) and (3.7), assuming the band gap narrowing of 0.12eV,

$$\beta_{eff,1con} = 20{,}000 \text{ x } e^{-0.12/0.026} = 198 \tag{3.8}$$

and from equations (3.6) and (3.7),

$$\beta_{eff,sub} = 8{,}130 \text{ x } e^{-0.12/0.026} = 80 \tag{3.9}$$

The effective beta values of from equations (3.8) and (3.9) are pretty close to the experimental data shown in Table 3.2. Here, we have neglected possible and bending at the interface because, based on the generally accepted conduction mechanism in polysilicon [35], the band bending at the grain boundaries in heavily doped polysilicon is much smaller than thermal energy and therefore can be neglected. Also the field dependence of the mobility and Auger recombination have not been taken into account. Such a model requires knowledge of parameters such as the doping profile, the hole mobility as a function of doping, the polysilicon grain size, and the intrinsic Shockley-Read-Hall lifetime.

3.3 Other Processes

This section includes fabrication processes that were attempted for establishing the basic full process and for developing the basic full process further.

In order to see the effect of the doping concentration in polysilicon and annealing temperature on the properties of polysilicon , polysilicon contacted

emitter devices with the basic full process are compared with the devices with different process parameters.

The effect of polysilicon deposition technique was investigated. Amorphous silicon (α-Si) was deposited, instead of polysilicon, using LPCVD and PECVD techniques. It was then implanted with arsenic and heated to recrystallize into polysilicon. The prime objective for using PECVD α-Si is to remove any native oxide at the polysilicon/monosilicon emitter interface and therefore reduce the variance in the enhanced beta. Plasma etching with argon was tried to remove the native oxide.

The effect of base doping on the beta enhancement was also investigated by changing only the base doping from the basic full process and the results were compared.

3.3.1 Polysilicon Annealing Time and Temperature

A number of fabrication runs were made to determine the best method of depositing polysilicon and under what conditions. In this section, the effect of doping concentration and annealing temperature on the polysilicon contacted emitter devices is described. Transistors were fabricated with a minimal residual oxide at the surface prior to polysilicon deposition. The polysilicon deposition was done by LPCVD on the substrate for the polysilicon contacted devices. Then, ion implantation with different doses and annealing at different temperatures were performed on each wafer set. The implant dose was varied from $1x10^{15}/cm^2$ to $3x10^{15}/cm^2$ at 25keV, and the annealing temperature was changed from 800 to 1000 ° C. The properties of the polysilicon contact and the polysilicon/monosilicon interface can be modified by varying the arsenic content at the grain boundary through changes in doping level in the polysilicon or by increasing the annealing temperature from 800 to 1000 ° C.

The key process parameters are:

25 minute 1000 ° C wet oxidation
$3x10^{13}/cm^2$ 25keV boron implant
10 minute 1000 ° C wet oxidation
$1x10^{15}/cm^2$ 25keV arsenic implant
10 minute 900 ° C wet oxidation

8 minute 620 ° C LPCVD poly-deposition
1-3x10^{15}/cm^2 25keV arsenic implant
10 minute 800-1000 ° C wet oxidation

An electrical characterization is carried out by the measurement of both contact resistance and maximum current gain (peak beta). It has been a common practice to use the current gain for making comparisons between devices fabricated under different conditions. The results from five process variations are given in Table 3.4. The results indicate that there is a definite relationship between the base-emitter series resistance (or contact resistance) and the maximum beta value. As the contact resistance becomes smaller, the maximum beta value becomes higher and even the beta enhancement gets larger. With a high contact resistance value, the maximum beta of the polysilicon contacted emitter device can be even lower than that of the conventional device as shown in wafer set V7 and V8. This implies that the advantage of the polysilicon contacted emitter devices can be obtained only with a small polysilicon contact resistance. For comparison, the SUPREM III simulated device characteristics are shown in Table 3.5 with various doping concentrations and annealing temperatures of polysilicon for the polysilicon contacted devices. Also, the SUPREM III simulated plot of net chemical impurity concentrations versus depth into the structure for them is shown in Figure 3.12.

The higher resistance at lower temperature, 800 ° C, must be caused by the native oxide existing at the polysilicon/monosilicon interface. This increase in the contact resistance can contribute to a significant increase in series voltage drop and reduce the current gain. As the annealing temperature becomes higher, the native oxide is believed to coalesce into lumps or nodules instead of a sheet so that holes form in the oxide. Eventually the oxide breaks up at 1000 ° C resulting in a good contact with a low resistance between polysilicon contact and the substrate emitter. This is consistent with the results of other researchers who indicated that high-temperature causes the interfacial layer to become discontinuous [35]-[37].

Another factor that can cause a lower contact resistance is the doping concentration in the polysilicon layer. At the same temperature, 900 ° C, by increasing the arsenic dose for the implant from 1x10^{15} to 3x10^{15}/cm^2, the contact resistance was reduced by a factor of about 20. In this case the lower resistance must be caused by higher doping concentrations in the polysilicon grains. The resistance in the polysilicon has been found to

Table 3.4 Dependence of emitter contact resistance and current gain on doping concentration and annealing temperature for polysilicon contact.

1000A LPCVD Poly Emitter
8 min, 620 ° C, 200mT, and 50 sccm SiH_4
Emitter Drive-in = 900 ° C H_2 Burn
36μ x 36μ Emitter Area

Wafer	Poly Dose (cm^{-3})	Poly Anneal	Mean Peak β sub	Stand. Dev. sub	Mean Peak β con1	Stand. Dev. con1	β(con1) / β(sub)	con1 b/e Res. (kΩ)
V2	$1x10^{15}$	1000 ° C	56	2.5	128	4.2	2.3	0.3
V3	$3x10^{15}$	1000 ° C	78	0.8	233	13.7	3.0	0.3
V5	$3x10^{15}$	900 ° C	71	0.8	183	7.3	2.6	2.0
V7	$1x10^{15}$	900 ° C	73	3.1	41	8.5	0.6	35.8
V8	$3x10^{15}$	800 ° C	51	1.2	36	13.3	0.7	102.5

Table 3.5 SUPREM III simulated device characteristics with various doping concentrations and annealing temperatures for polysilicon contact of polysilicon contacted transistors.

Parameter		V2	V3	V5	V7	V8
Poly-contact Thickness (Å)		928	928	1342	1342	1463
Junction Depth (Å)	base/emit	0.15	0.16	0.09	0.09	0.09
	base/coll under emit	0.68	0.68	0.63	0.63	0.62
Base Width (μ)		0.53	0.52	0.54	0.54	0.53
Effective Base Width (μ)		0.38	0.37	0.43	0.43	0.42
Sheet Resistance ($\Omega/\square$)	poly-contact	5,654	2,776	2,109	5,017	2,340
	emitter	104.3	65.3	127.9	128.4	141.9
	base-pinch	5,987	6,065	4,134	4,134	3,971
	base	3,807	4,291	2,829	2,802	2,514
Built-in Potential (V)	base/emit	0.99	1.00	1.00	1.01	1.02
	base/coll	0.71	0.71	0.72	0.72	0.72

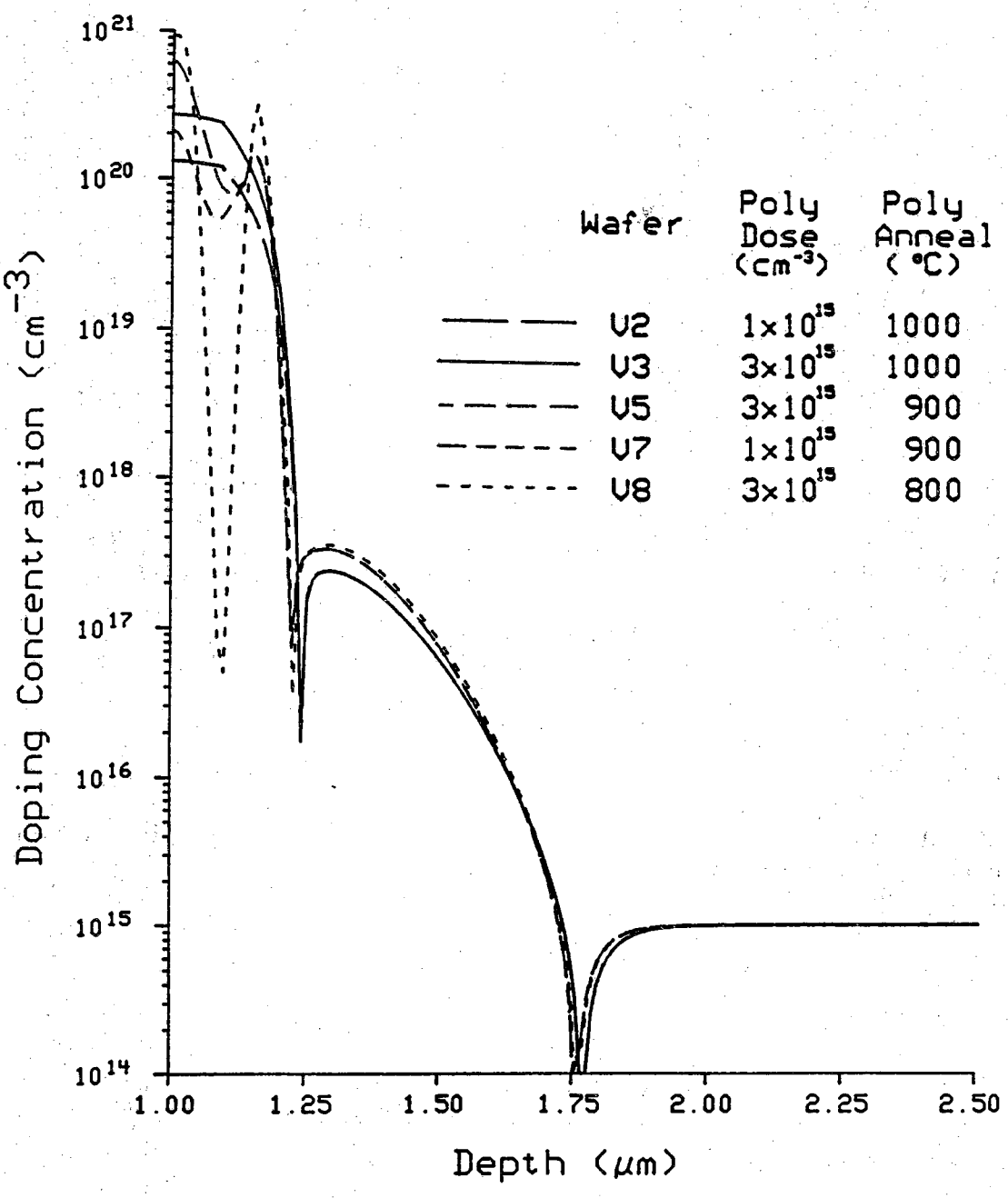


Figure 3.12 SUPREM III simulated plot of net chemical impurity concentrations versus depth into the structure of polysilicon contacted devices with various doping concentrations and annealing temperatures for polysilicon contact.

depend on the doping concentration in the polysilicon grains [32]. This reduction in the resistance increased the maximum beta value of the polysilicon contacted emitter devices by a factor of about 4.

The measurements of the contact resistance of the polysilicon contacted emitter devices with same arsenic concentration shows a stronger dependence on the annealing temperature than on the doping concentration. Once the interfacial oxide is removed, the polysilicon contact layer plays an important role. The devices with 1000 ° C polysilicon annealing revealed that higher doping concentration in the polysilicon contact layer generates a higher maximum beta value and a higher beta enhancement than lower doping concentration. This can be explained by the fact that the devices with lower doping concentration have more trapping states resulting from the high concentration of defects and dangling bonds at the grain boundaries, resulting in the larger base current and reducing beta.

By choosing the right combination of doping concentration and the annealing temperature for the polysilicon layer, the maximum current gain and the gain enhancement over the control device can be maximized. The process parameters of the wafer set V3 were chosen as the basis for the further process development.

3.3.2 LPCVD α-Si/Poly Contacted Emitter

The previous study of coupling the contact resistance with the maximum current gain allowed a more comprehensive electrical characterization of the properties of the polysilicon/monosilicon interface. A good beta enhancement from the polysilicon contacted emitter devices over the control devices was obtained with a low contact resistance.

There is some characteristics, such as grain size, that can not be predicted well from the polysilicon layer. Therefore, the polysilicon contacted emitter devices would produce, even with a controlled interface, a wide range of maximum beta values on the same wafer when grain size and grain boundaries play an important role. Controlled interface and the fine grained polysilicon should lead to more uniform and predictable beta enhancement for the polysilicon contacted emitter devices. One possible method of making finer grain size of polysilicon is depositing amorphous silicon and recrystallizing it instead of directly depositing polysilicon on the silicon

substrate.

A different method of fabricating a polysilicon contact was investigated. In an LPCVD reactor, either polysilicon or amorphous silicon (α-Si) can be deposited. By changing the deposition temperature, α-Si deposition was done at 580 ° C, whereas polysilicon deposition was done at 620 ° C. The effect of arsenic segregation and grain size is examined by first annealing samples at 600 ° C, after arsenic implant, to make a fine grain size and establish the structure of the interface. A subsequent anneal at 800 and 900 ° C will cause arsenic to be activated in the polysilicon. The key process parameters are as follows:

25 minute 1000 ° C wet oxidation
$3x10^{13}/cm^2$ 25keV boron implant
10 minute 1000 ° C wet oxidation
$1x10^{15}/cm^2$ 25keV arsenic implant
10 minute 1000 ° C wet oxidation
15 minute 580 ° C LPCVD α-Si deposition
$3x10^{15}/cm^2$ 25keV arsenic implant
60 minute 600 ° C α-Si recrystallization
10 minute 800-900 ° C wet oxidation

Electrical characteristics of the devices with the above process parameters are shown in Table 3.6. They are compared with the devices of the wafer set V3 and V8. The control devices made with this process showed lower beta values than expected. This indicates the parameters for the control devices must have deviated slightly such as shallower emitter junction depth in the substrate.

However, deposition of α-Si by LPCVD and recrystallization seem to remove the native interfacial oxide layer. The devices of the wafers V10 and V11 had low contact resistances even with low temperature annealing. It is noticed that the maximum beta and beta enhancement of the devices of the wafer set V11 are much higher than those of the devices of the wafer set V8. This suggests that it is unnecessary to anneal the polysilicon contact at high temperature, i.e. 1000 ° C, in order to remove the interfacial native oxide and make a good contact, when α-Si deposition and recrystallization is performed. Instead, the recrystallization of α-Si seems to "eat up" or "break up" the interfacial oxide and make a good contact.

Table 3.6 Comparison of polysilicon contacted devices with the contact recrystallized after LPCVD α-Si deposition.

1000A LPCVD Poly Emitter
15 min, 580 °C, 200mT, and 50 sccm SiH_4
Base Dose = $3x10^{13}/cm^2$
Poly Dose = $3x10^{15}/cm^2$
36μ x 36μ Emitter Area

Wafer	α-Si/Poly Cryst.	Poly Anneal	Mean Peak β sub	Stand. Dev. sub	Mean Peak β con1	Stand. Dev. con1	β(con1) / β(sub)	con1 b/e Res. (kΩ)
V10	600 °C	900 °C	43	0.3	51	1.4	1.2	0.3
V11	600 °C	800 °C	41	1.1	84	16.1	2.0	0.3
V8	N/A	800 °C	51	1.2	36	13.3	0.7	102.5
V3	N/A	1000 °C	78	0.8	233	13.7	3.0	0.3

SUPREM simulation for these fabrications was not performed because neither SUPREM II nor SUPREM III had the capability to model process sequences that utilize amorphous silicon.

3.3.3 PECVD α-Si:H/Poly Contacted Emitter

As mentioned earlier, the interfacial oxide can be removed with high temperature annealing by realignment of the oxide layer or epitaxial realignment at the interface, while the oxide is believed to form small inclusions within the realigned polysilicon and near the original interface. Although this heat treatment will create a good contact, the oxide inclusions are still existing at the interface and can act as trapping sites for the carriers. They also can contribute to the production of a wide range of maximum beta values of the polysilicon contacted emitter devices. Therefore, it is ideal to remove even the native oxide before depositing α-Si or polysilicon if possible.

In this section, a new fabrication technique which uses plasma etching of the shallow arsenic emitter location and without breaking vacuum, depositing hydrogenated amorphous silicon (α-Si:H) on the cleaned interface is introduced. This new technique can be accomplished with a Plasma Enhanced CVD (PECVD) system. By using PECVD system, either plasma etch or plasma deposit can be done in the same system by changing the gas mixtures and RF power levels. Several plasma etches are possible with different etchants, such as argon, CF_4, or hydrogen, in order to remove the native oxide. For these experiments, only argon etch was attempted. A detailed description of how to operate the PECVD system is contained in Appendix F.

With or without plasma etching, α-Si:H was deposited in the PECVD reactor at 5W or 25W. The α-Si:H is then implanted with arsenic and then heated to 800 or 900 ° C to produce the polysilicon contact, i.e. produce the polysilicon and activate the arsenic impurities in the polysilicon. Again, some wafer sets were heated at lower temperatures, 550-650 ° C, before the higher temperature annealing to see if the low heat treatment would determine fine grain size and structure of the interface.

The resulting process sequence is as follows:

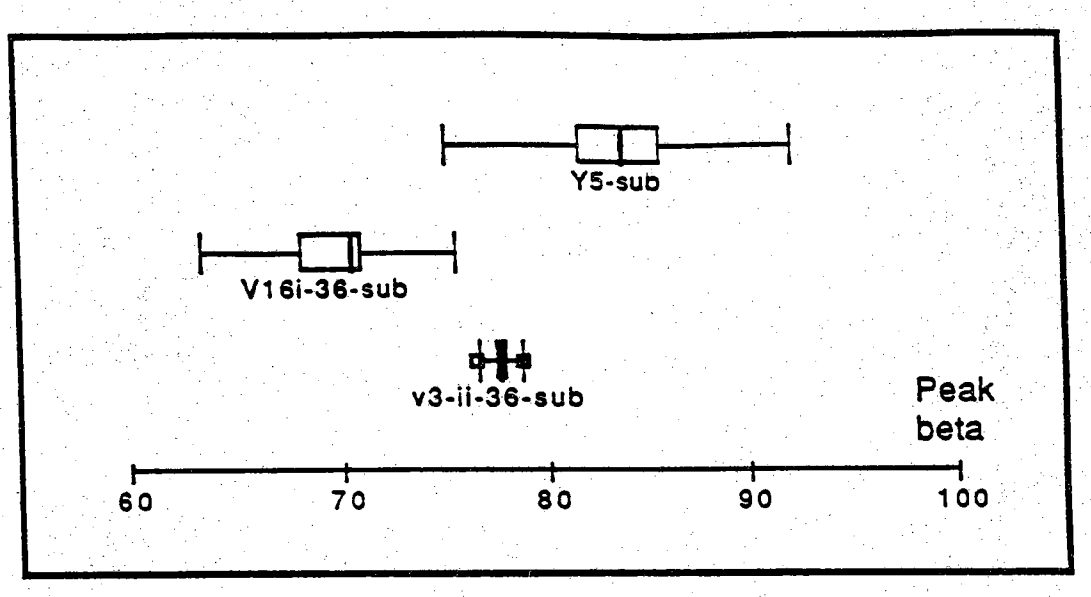
25 minute 1000 ° C wet oxidation
$3x10^{13}/cm^2$ 25keV boron implant
10 minute 1000 ° C wet oxidation
$1x10^{15}/cm^2$ 25keV arsenic implant
10 minute 1000 ° C wet oxidation
some - Ar^+ plasma etch
5W or 25W PECVD α-Si:H deposition
$3x10^{15}/cm^2$ 25keV arsenic implant
some - 60minute 550-650 ° C dry oxidation
10 minute 800-900 ° C wet oxidation

Maximum beta, beta enhancement, and contact resistance of the polysilicon contacted emitter devices with PECVD α-Si:H deposition are shown in Table 3.7. The results indicate that, with 900 ° C annealing after PECVD α-Si:H deposition, the contact resistance of the polysilicon emitter devices becomes as low as that of the metal contacted devices. This implies that the interfacial oxide is broken up and a reasonably good contact is obtained for the polysilicon contacted emitter devices. The polysilicon contacted emitter devices of the wafer set Y5 showed the highest maximum beta and largest beta enhancement among them. However, a large range in the enhanced betas, on the same wafer or die, were still observed, whereas the metal contacted shallow emitter control devices (sub) had a very tight standard deviation in the maximum current gain. Complete removal of the native oxide and the fine grained polysilicon, impregnated with hydrogen to heal the surface states and dangling bonds, should lead to more uniform and predictable enhanced betas. The statistical results of the measured peak beta values for the wafer sets V3, V16, and Y5 are shown in Figure 3.13.

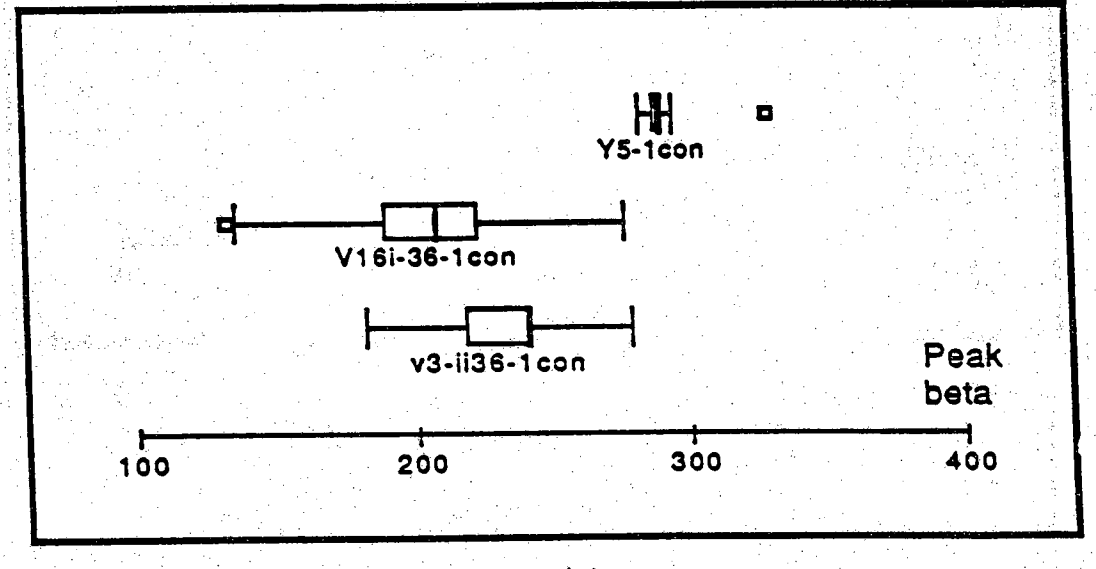
With 800 ° C polysilicon annealing, the contact resistance of the polysilicon contacted emitter devices was usually larger and less beta enhancement occurred as compared to those with 900 ° C. This can be explained by the existence of the unbroken native oxide layer. If the interfacial oxide was broken up as much as with 900 ° C annealing, the devices would have similar maximum betas and beta enhancement either with 800 ° C or 900 ° C polysilicon annealing. The polysilicon contacted emitter devices of the wafer set Y3, with 800 ° C annealing, showed low contact resistance values indicating that the interfacial oxide was broken up. This suggests that by optimizing the plasma deposition conditions of α-Si:H it was possible to eliminate the plasma etch step altogether. This

Table 3.7 Comparison of polysilicon contacted devices with the contact recrystallized after PECVD α-Si:H deposition.

Process Sequence Differences			Peak Beta		
α-Si:H Dose : As^+ - $3x10^{15}$ cm^{-2}					
Wafer	Deposition Step	α-Si:H Anneal	con1	sub	βcon1/βsub
V15	PECDV (25W, 7min)	800 ° C H_2 Burn	62.1	54.0	1.15
V16	PECVD (25W, 7min)	900 ° C H_2 Burn	200.4	69.1	2.90
V17	PECVD (25W, 7min)	650 ° C/800 ° C H_2 Burn	98.4	63.7	1.54
V18	PECVD (25W, 7min)	650 ° C/900 ° C H_2 Burn	180.6	79.2	2.28
V19	PECVD (25W, 7min)	550 ° C/800 ° C H_2 Burn	86.4	57.2	1.51
V20	PECVD/w Ar^+ etch	650 ° C/800 ° C H_2 Burn	105.9	56.39	1.89
Y3	PECVD (5W, 10min)	800 ° C O_2	128.4	77.7	1.65
Y5	PECVD (5W, 10min)	900 ° C O_2	293.6	83.4	3.52
Z1	PECVD/w Ar^+ etch	800 ° C H_2 Burn	83.7	76.5	1.09



(a)



(b)

Figure 3.13 Statistical plot for the comparison of measured peak beta from wafer sets V3, V16, and Y5: (a) sub and (b) 1con.

should be investigated in the future. The statistical results of the measured peak beta values for the wafer sets V3, V15, and Y3 are shown in Figure 3.14.

Some wafer sets, V20 and Z1, went through the plasma etch with argon but did not give any better results than those without plasma etch. The plasma etch with argon apparently must have created damages on the wafer surface and reduced the beta enhancement.

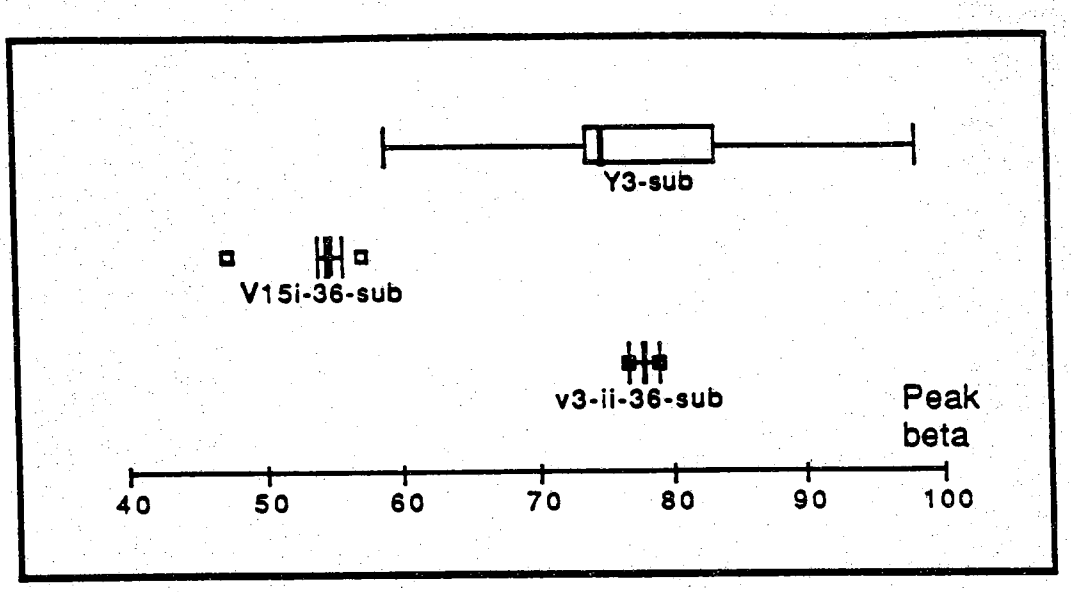
Here, the low temperature recrystallization of α-Si:H did not make a noticeable difference in the electrical characteristics of the devices. Instead, the high temperature anneal seems to play a major role in deciding the characteristics of the devices.

3.4 Tradeoff Between Enhanced Gain and Base Doping

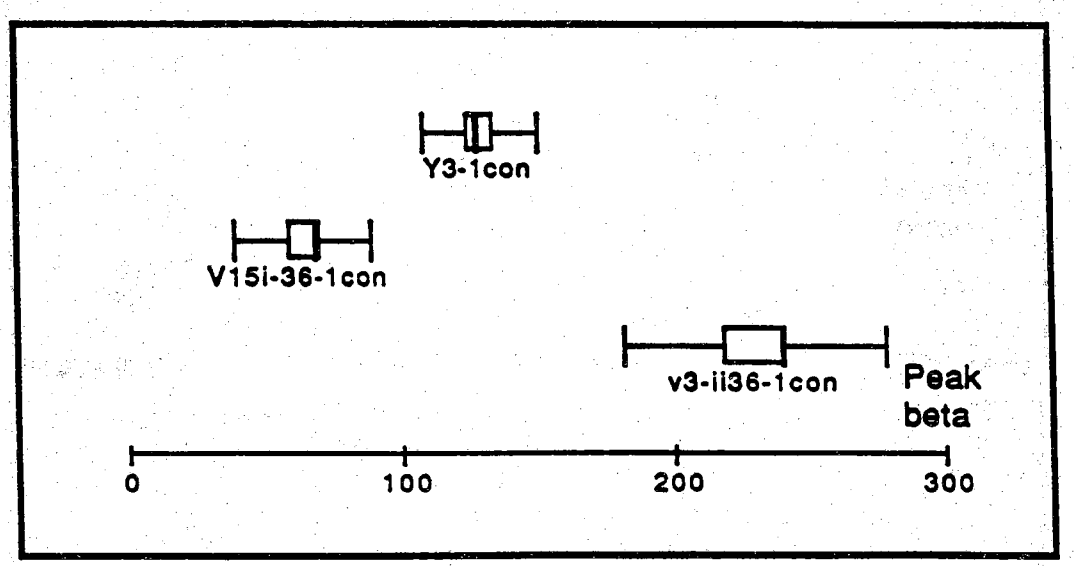
As mentioned previously, polysilicon contacted emitter transistors have several advantages over conventional metal contacted shallow emitter transistors for scaling to small geometries. One of the problems of scaling down a conventional bipolar transistor is current gain degradation which occurs as the vertical dimensions of the devices are shrunk [39]. This is a result firstly of the increased minority carrier gradient in the shallow emitter of the transistor [40], and secondly of the increased doping required in the narrow base region of the device in order to prevent punch-through [39,41]. In order to maintain a reasonable gain, a lower active base doping level is therefore required. However, this increases the base resistance of the transistor and can lead to a degradation of the circuit performance.

In contrast, for a polysilicon contacted shallow emitter transistor, very high current gain can be achieved without compromising base resistances and thus circuit performance. Depending upon the surface treatment prior to polysilicon deposition, the gain can be enhanced over a comparable conventional transistor. This allows the active base doping level to be increased significantly over that of a conventional transistor and the gain enhancement to be traded for a decrease in the base resistance, resulting in an improved circuit performance[39].

In this section, it is investigated to what extent the enhanced gain obtained from a polysilicon contacted emitter devices can be traded for a reduction in the base resistance of the transistor and, hence, for a potential



(a)



(b)

Figure 3.14 Statistical plot for the comparison of measured peak beta from wafer sets V3, V15, and Y3: (a) sub and (b) 1con.

improvement in circuit performance. An attention is given on the polysilicon contacted emitter devices without the interfacial oxide layer at the polysilicon/monosilicon interface, since this type of device has been shown to exhibit the current gain enhanced by a factor of about three over a conventional transistor, yet can be consistently reproducible.

With the exception of the boron implant for the base region, process parameters were identical for all devices fabricated in this experiment. In order to produce devices with a range of base doping levels, various boron doses ranging from $3x10^{13}$ to $8x10^{13}/cm^2$ were implanted. They were implanted at an energy of 25keV after etching the base region. The emitter was implanted with arsenic at 25keV. Prior to polysilicon deposition on the emitter of the polysilicon contacted emitter transistor, the interfacial layer treatment was carried out. This consisted of BHF etch to remove all the oxide from the silicon surface. Immediately following the surface treatment, the wafers were loaded into the LPCVD reactor, and approximately 0.1μ of undoped polysilicon was deposited. The polysilicon was then implanted with arsenic. This was followed by wet oxidation at 1000 °C for 10min for annealing. On completion of annealing, the polysilicon thickness was expected to decrease but not a significant amount. The SUPREM III simulated device characteristics with various base doping concentrations are shown in Table 3.8 and the SUPREM III simulated plot of net chemical impurity concentrations versus depth into the structure for those devices is shown in Figure 3.15.

In order to characterize the electrical behavior of these devices, collector and base currents were measured as a function of the base-emitter voltage for a number of devices on each wafer. Also, maximum current gain, peak beta, of both types of devices and beta enhancement of the polysilicon contacted emitter devices were obtained from them. As expected, increasing boron impurity concentration in the base has the effect of increasing the base Gummel number of the transistor, and the collector characteristics for these devices were seen to have the downward shift.

Also, an increase in the base current of these transistors was seen accompanying the decrease in the collector current. This is mainly due to the reduced emitter injection efficiency with increased base doping. As a result, a considerable decrease in maximum current gain was observed with increasing base doping as shown in Figure 3.16. The result is consistent with the results obtained by Cuthbertson and Ashburn [42]. One possible explanation for the observed increase in base current could be an increased

Table 3.8 SUPREM III simulated device characteristics with various base doping concentrations for polysilicon contacted devices.

Parameter		V3	W6	W7	W8
Poly-contact Thickness (Å)		928	928	928	928
Junction Depth (Å)	base/emit	0.16	0.15	0.15	0.15
	base/coll under emit	0.68	0.71	0.72	0.74
Base Width (μ)		0.52	0.56	0.57	0.59
Effective Base Width (μ)		0.37	0.45	0.48	0.51
Sheet Resistance ($\Omega/\square$)	poly-contact	2,776	2,777	2,777	2,778
	emitter	65.3	65.6	65.7	66.0
	base-pinch	6,065	3,578	3,012	2,325
	base	4,291	2,659	2,272	1,793
Built-in Potential (V)	base/emit	1.00	1.02	1.02	1.03
	base/coll	0.71	0.72	0.73	0.74

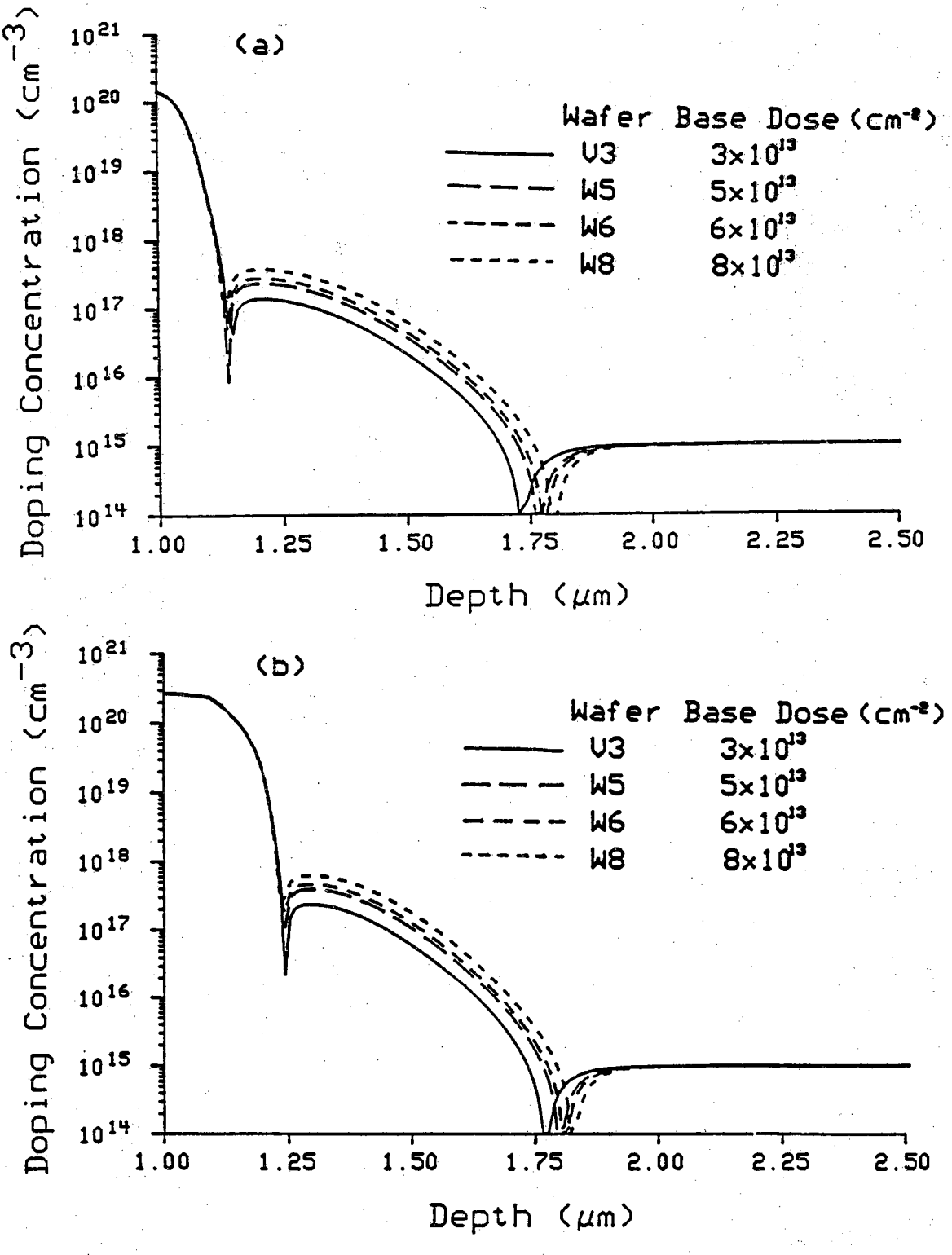
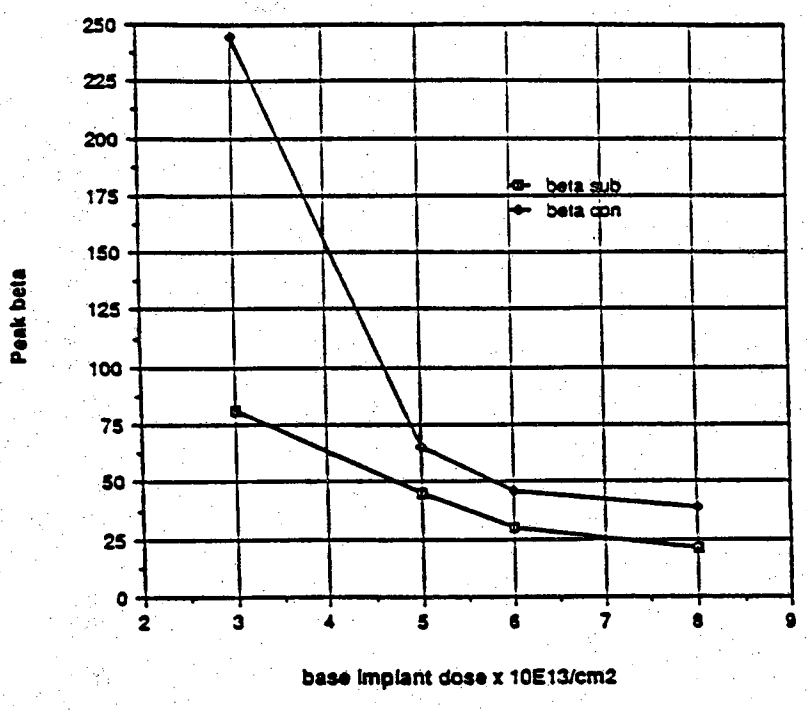
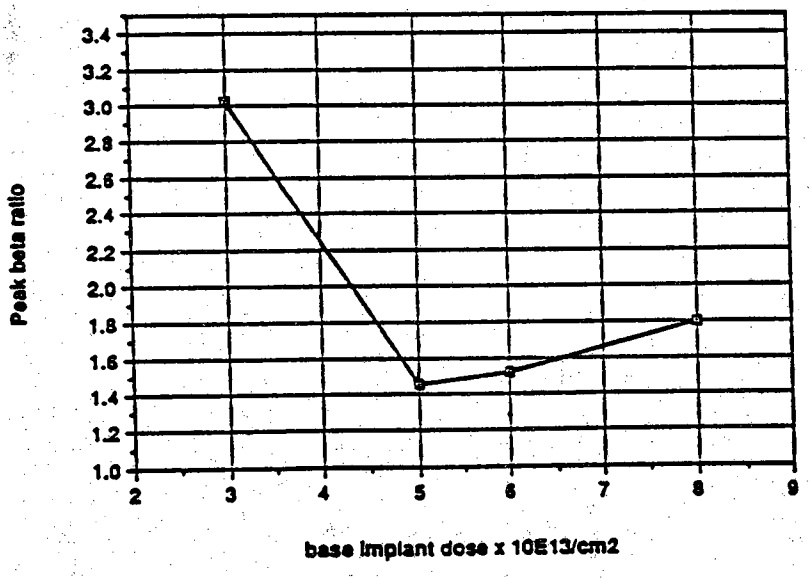


Figure 3.15 SUPREM III simulated plot of net chemical impurity concentrations versus depth into the structure with various base doping concentrations: (a) sub and (b) 1con.



(a)



(b)

Figure 3.16 Measured peak beta dependence on base doping concentration: (a) peak beta and (b) peak beta ratio.

carrier recombination in the neutral base region of the device. For conventional high-performance bipolar transistors with moderately doped base regions ($N_A \leq 10^{17} cm^{-3}$) and narrow base widths, this base current component is generally considered to be insignificant compared with the back-injected hole current into the emitter. However, since in these devices the base doping densities are well in excess of this value, the minority carrier lifetime in the base will decrease more rapidly with base doping ($\sim N_A^{-2}$) because of Auger recombination.

Since the collector current is approximately proportional to the base sheet resistance, the beta enhancement of the polysilicon contacted emitter transistor can therefore be traded for a proportionate decrease in its intrinsic base sheet resistance. Therefore, the devices which have almost the same current gain and lower base sheet resistance can be achieved by implementing the polysilicon contacted emitter device.

CHAPTER IV
ELECTRICAL MEASUREMENTS

Electrical measurements were performed on the polysilicon contacted emitter devices and the conventional (control) devices. The final process results were obtained from devices bonded into dual-in-line packages (DIPs). The electrical connections from the device to the DIP are made with ultrasonically bonded 1 mil. aluminum wires. Packaging the devices results in much more reliable electrical connections during testing, and thus yields much better (consistent) test data than data obtained with the probe station.

A test station was designed using a HP4145A Semiconductor Parameter Analyzer with a reconditioned probing station. All the process test data were recorded with the HP4145A controlled by a HP9845A desk top computer. The control program used to take data points was a modified version of the UNIX2 program originally written by Jeff Shields at Purdue University. This program gives the power supply in 0.01V increments from 0 to 1V to measure the forward bias I-V curves. Reverse bias testing down to -100V with decrements of 0.01V per step was also available.

The program automatically takes the I-V values and beta versus I_C data and loads them into a designated file on the UNIX ECN network for plotting etc. Then the results can be compared between the polysilicon contacted emitter devices and the conventional devices.

In order to show a typical set of I-V curves for the junctions and transistors, examples of test results were extracted from a 36μ x 36μ emitter device of the wafer set V3, quadrant ii on the wafer. This is denoted by "V3-ii-36". Each device also has a label. "Sub10" means the 10th device in the array of conventional metal contacted devices whereas "1con12" indicates the 12th device in the array of polysilicon contacted emitter devices.

From this data, I_s, res, I_{ebo}, V_{ebo}, η for the base-emitter junction, I_s, res, I_{cbo}, V_{cbo}, η for the base-collector junction, V_{ceo}, and max beta are extracted.

The saturation current or ideal leakage current, I_s, is extrapolated from the ideal region in the forward bias I-V curve. I_s is equal to the point where the ideal part of the I-V curve intersects the current (vertical) axis. The ideality factor, η, is also calculated from the ideal region in the forward bias I-V curve by taking the slope of the ideal region. The ideality factor was calculated as

$$\frac{(k_B T)/q \times \ln(10)}{(\text{slope of } \log_{10}(I_C) \text{ versus } V_{BE})} = \frac{4.3}{\text{slope}} = \eta$$

The resistance value can be calculated by either dividing the voltage difference between ideal and actual curve at a certain current value or dividing a certain voltage value by the current difference at that voltage. This must be calculated at the current or voltage value where the ideal current is larger than the actual current value. For our measurements the first method was applied. Figure 4.1 and Figure 4.3 show forward bias I- V curves for the base-emitter and the base-collector junctions.

The breakdown voltages of the base-emitter and the base-collector junction, V_{ebo} and V_{cbo} respectively, are measured from the reverse bias I-V curves. The breakdown voltage was selected when the reverse bias current exceeds $1\mu A$. The reverse bias leakage currents of the base-emitter and base-collector junction, I_{ebo} and I_{cbo} respectively, are also measured from the same curves. The reverse bias leakage current was selected at a certain voltage value between zero and the breakdown voltage. Reverse bias I-V curves for the base-emitter and the base-collector junctions are shown in Figure 4.2 and Figure 4.4.

The collector-emitter breakdown voltage with the base open, V_{ceo}, is obtained from the I_C-V_{CE} plot, particularly from the curve with the base current equal to zero. V_{ceo} is selected when the collector gets above 1mA. I_C-V_{CE} curve is shown in Figure 4.5.

The current gain, β, is calculated from a Gummel plot, I_C and I_B versus V_{BE}. A Gummel plot is shown in Figure 4.6. The values at very low current are sometimes erratic due to instrument error and they should not be

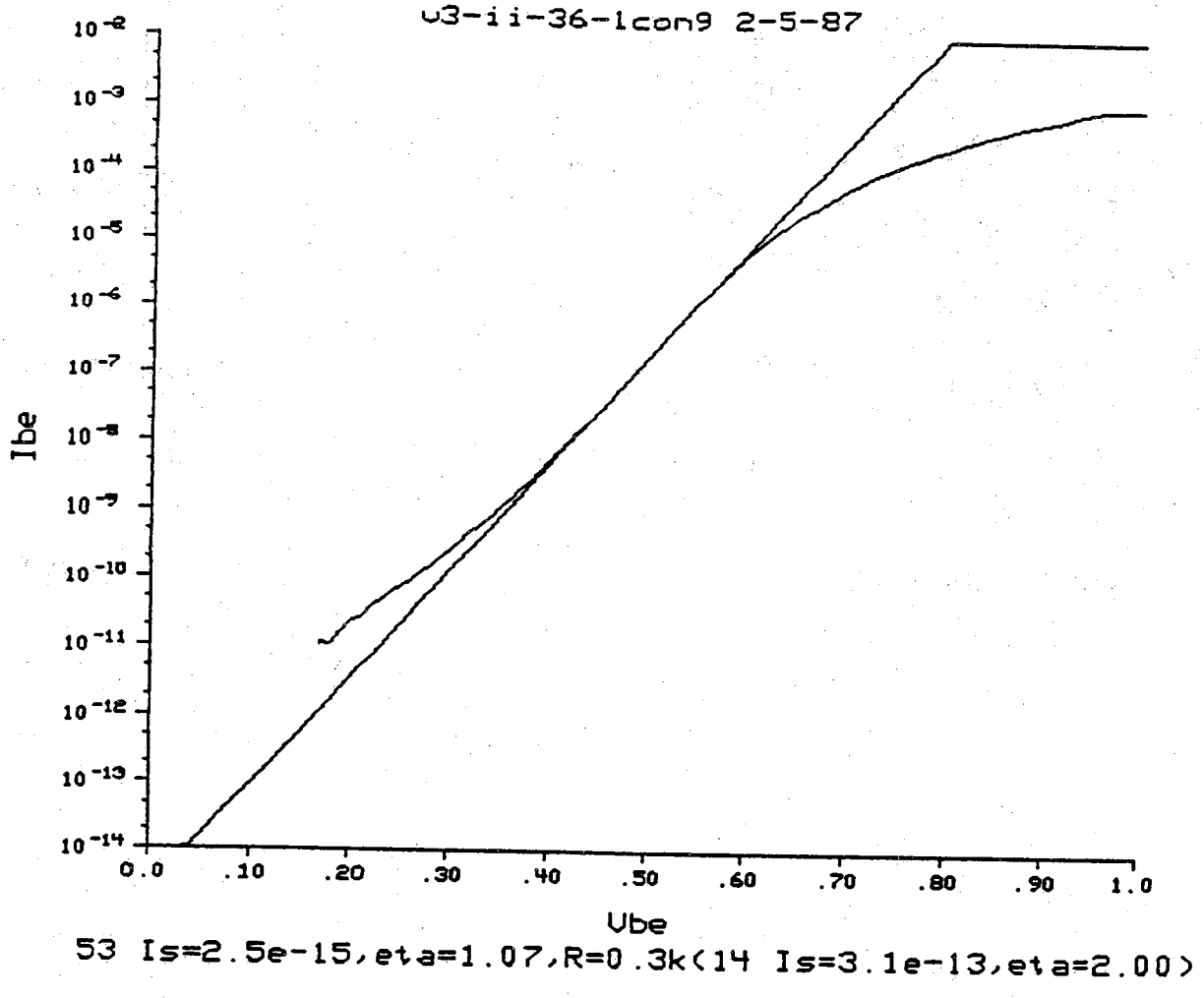


Figure 4.1 Measured I_{be} versus V_{be} forward bias characteristics for the device V3-ii-36-1con9.

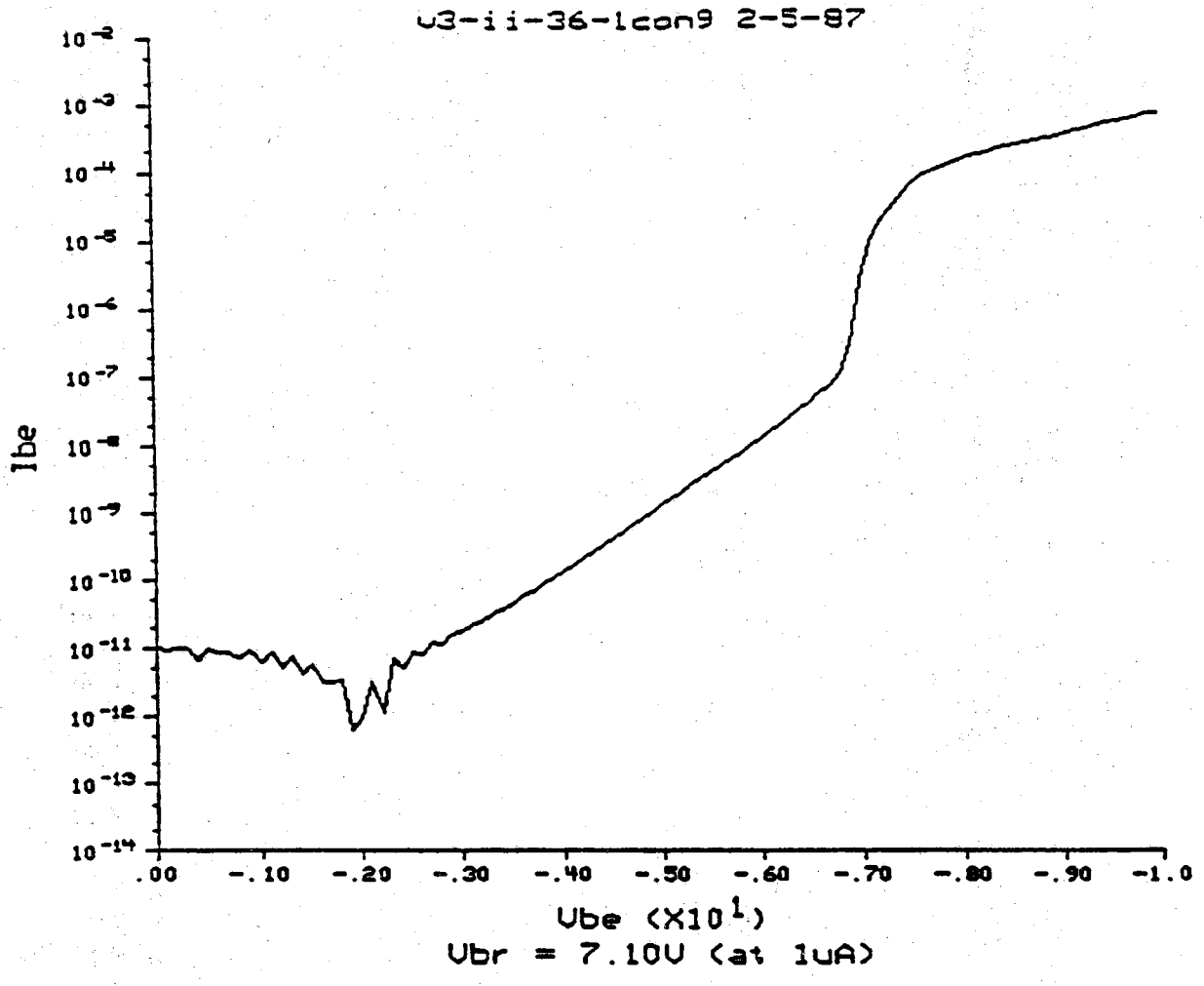


Figure 4.2 Measured I_{be} versus V_{be} reverse bias characteristics for the device V3-ii-36-1con9.

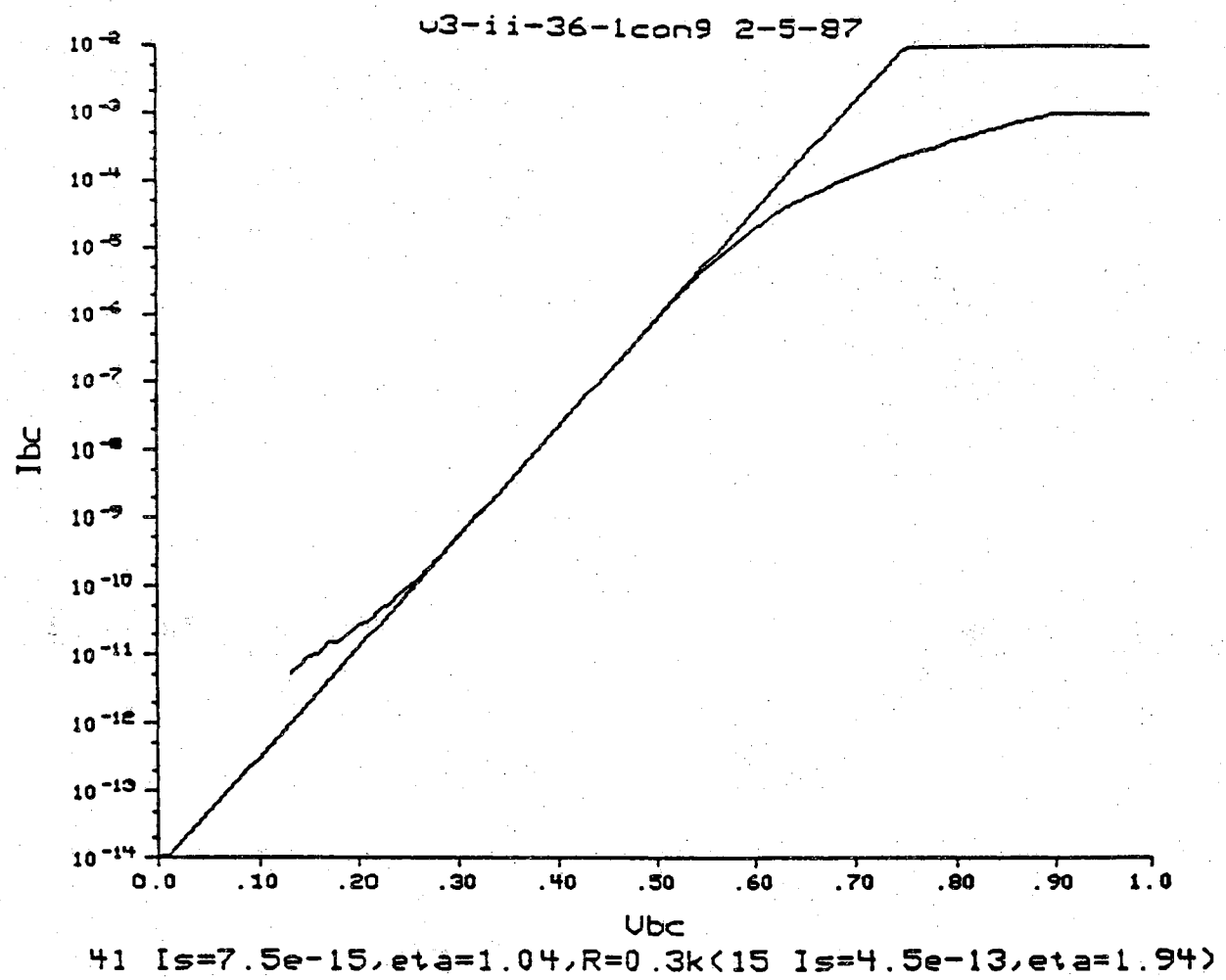


Figure 4.3 Measured I_{bc} versus V_{bc} forward bias characteristics for the device V3-ii-36-1con9.

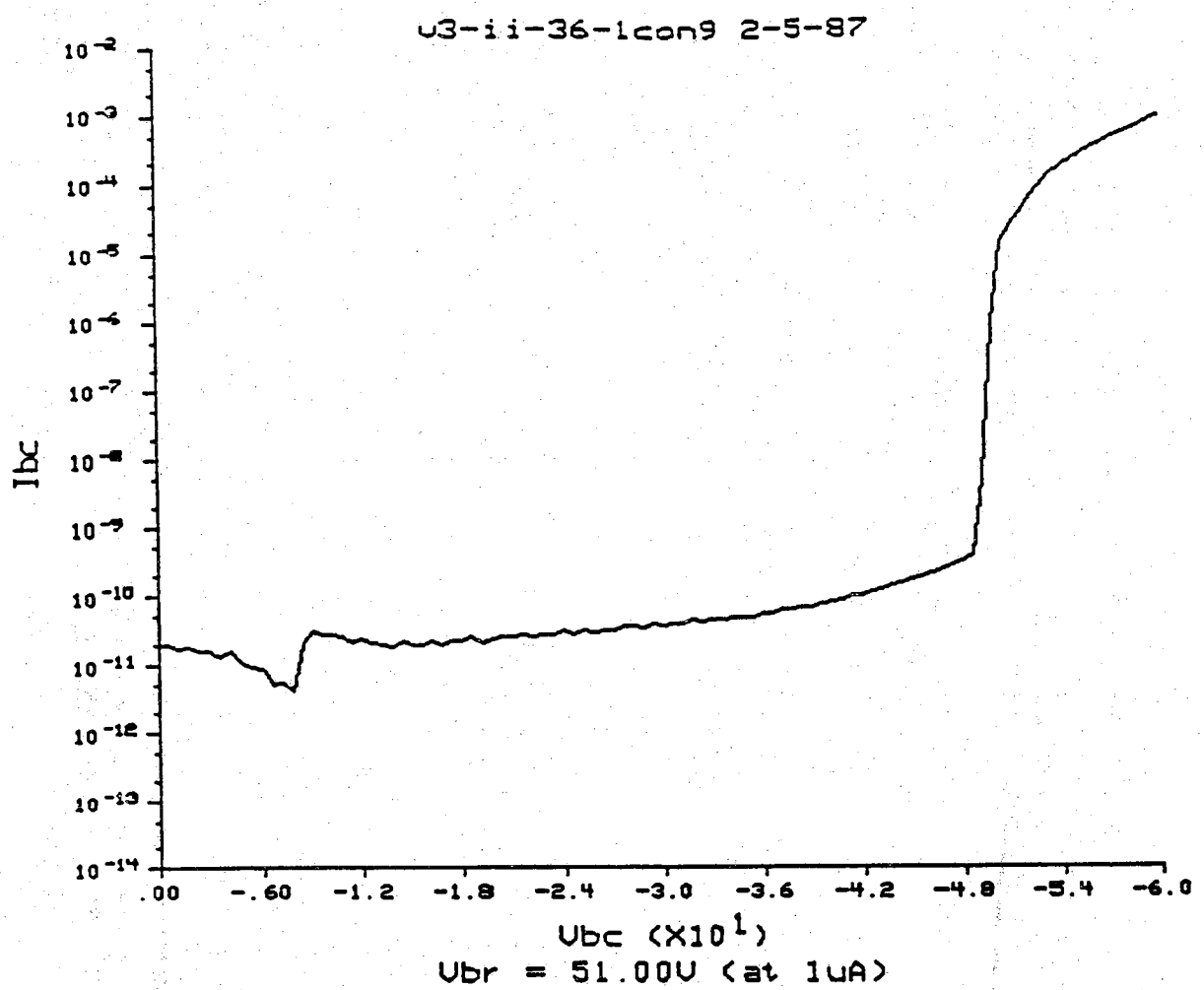


Figure 4.4 Measured I_{bc} versus V_{bc} reverse bias characteristics for the device V3-ii-36-1con9.

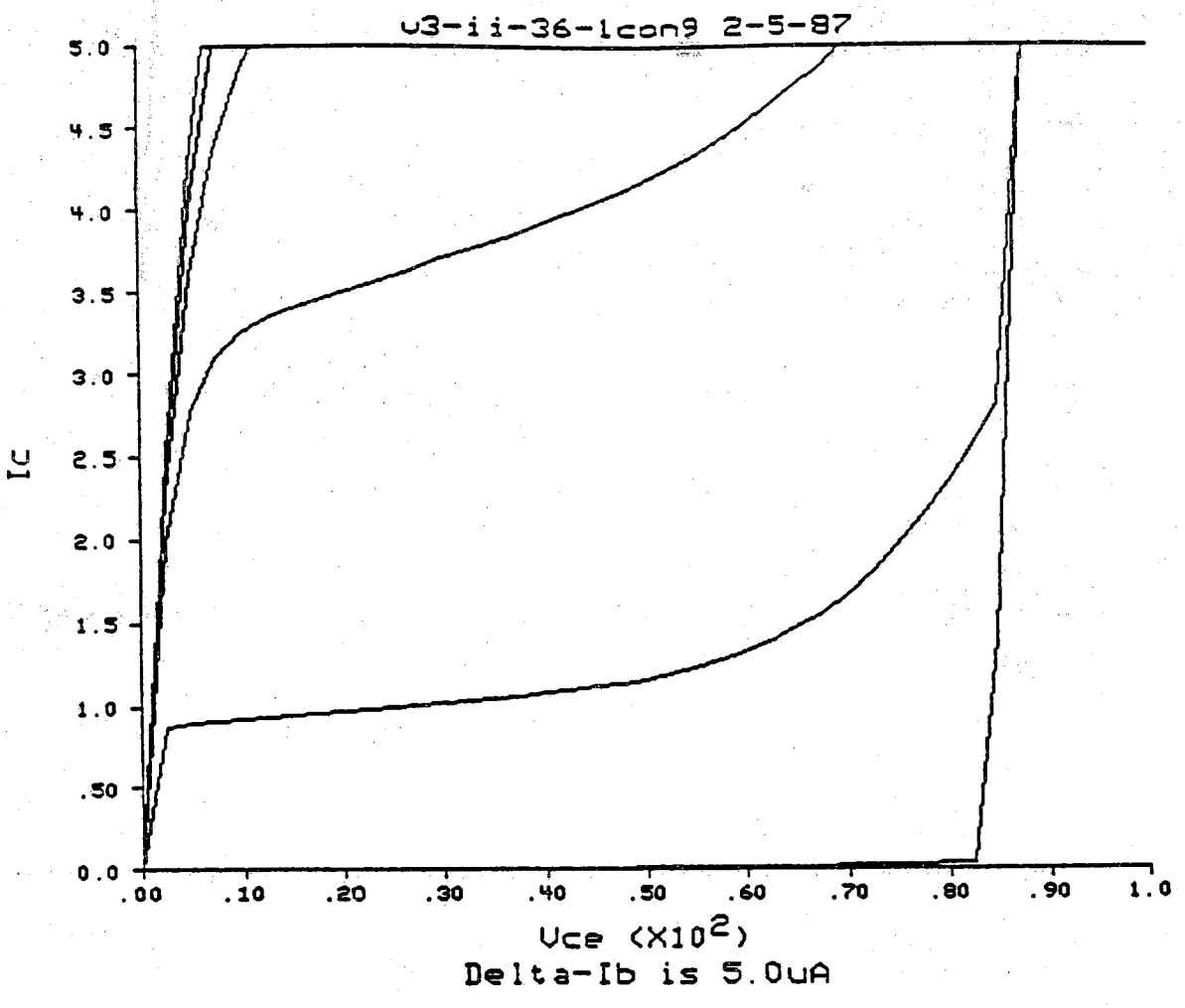


Figure 4.5 Measured I_c versus V_{ce} characteristics for the device V3-ii-36-1con9.

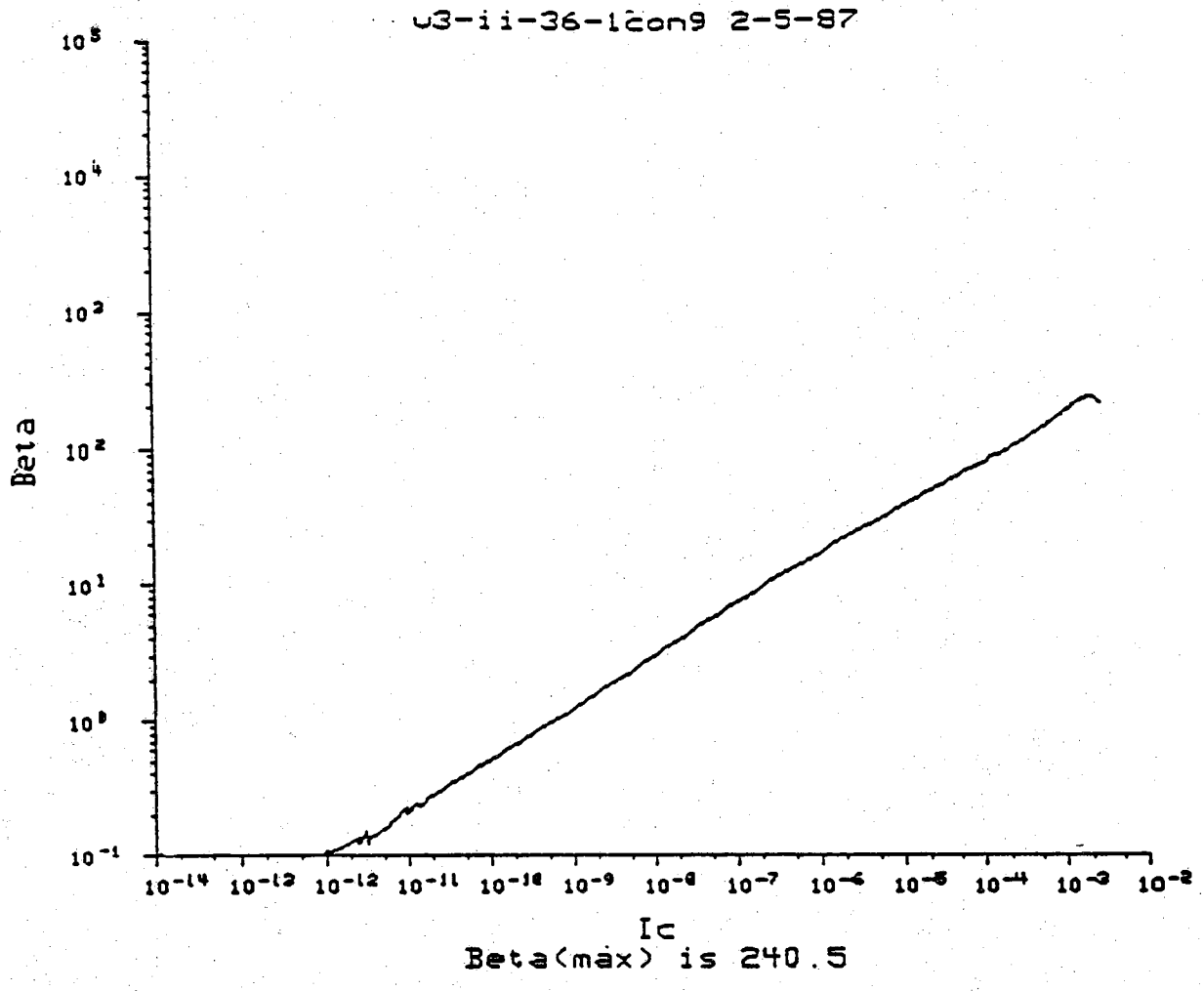


Figure 4.6 Measured I_b, I_c versus V_{be} characteristics for the device V3-ii-36-1con9.

considered meaningful. Ideally, the collector and base current should be parallel and should have same slopes. As I_C increases, however, the I_C curve deviates from ideal. This effect is due to a large series resistance in the collector, and beta drops off rapidly as I_C increases above certain values. Beta is obtained by calculating the vertical distance between these two curves at each tested V_{BE} value and plotted as shown in Figure 4.7. The peak beta is obtained from this plot. Examples of these values are shown in Table 4.1. They were chosen from the wafer set V3. All the values described above were obtained for both polysilicon contacted emitter devices and conventional devices. Mainly the peak beta was compared since the main advantage of the polysilicon contacted devices is a gain enhancement. Other were also inspected to see if the fabrication of the devices was good in general.

The low values of η and I_s indicate that the number of recombination centers, or defects, is low and that the fabrication technique is good. The low resistance ($\leq 0.3K\Omega$) of the polysilicon contacted emitter devices implies that the polysilicon/silicon interface was as clean for the polysilicon emitter contacted devices as that of the metal contacted devices. This leads us to believe that the interface for the polysilicon contacted devices is free of any oxide. Hence the direct comparison of the betas between two devices can be made with little discrepancies. The conventional devices almost always have good contacts and show low resistance values.

Four sets of parameters can be used to compare the experimental results with the SUPREM III simulated results. These parameters are the oxide thickness, the sheet resistance, the base width, and junction depth. The comparison is shown in Table 4.2. The experimental oxide thicknesses were determined using Nanometrix optic measurement device and Dektak stylus by Delco Electronics. The sheet resistances were measured from the test resistors, and the base width and junction depths were measured using Spreading Resistance technique by Delco Electronics.

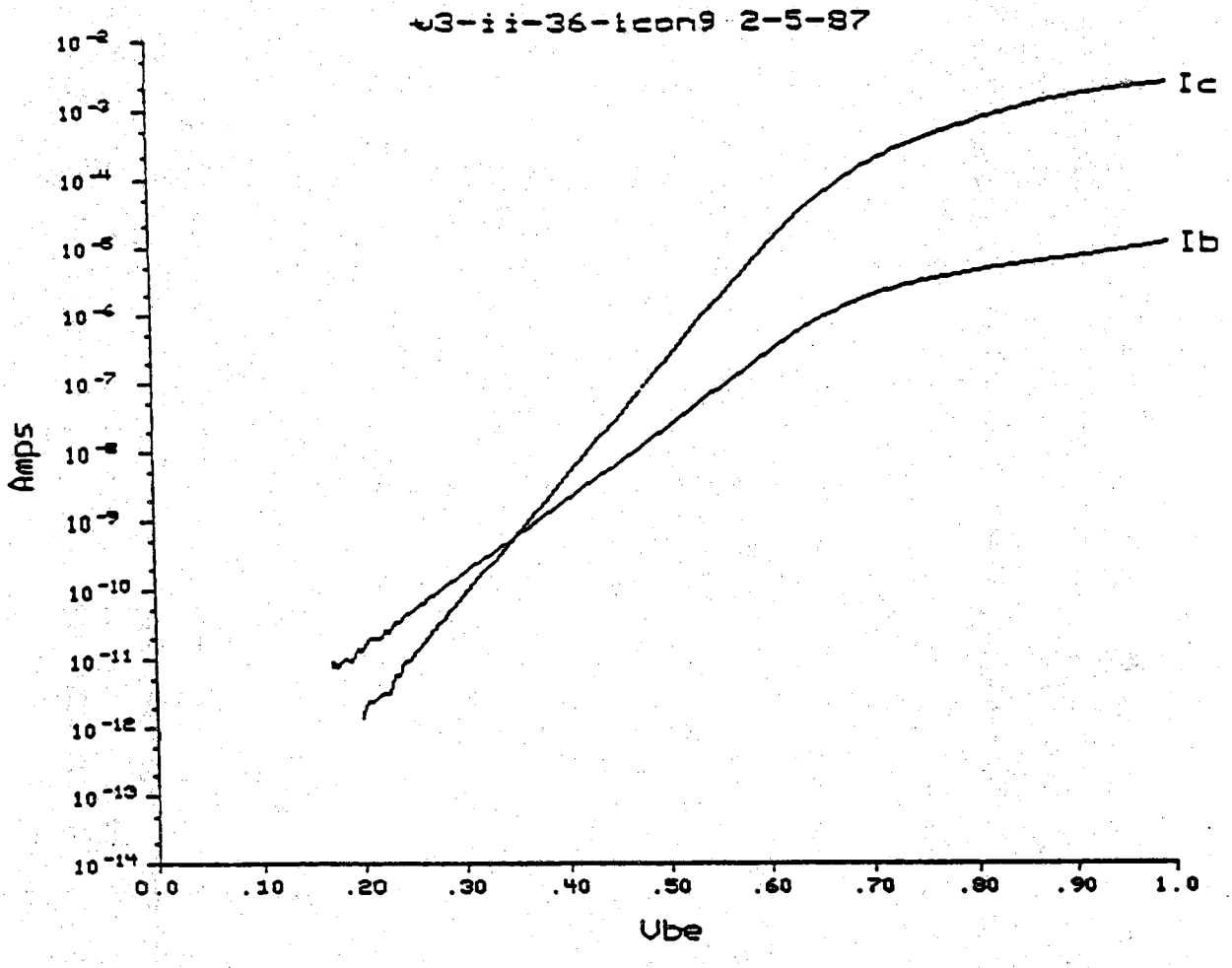


Figure 4.7 Measured beta versus I_c characteristics for the device V3-ii-36-1con9.

Table 4.1 Measured device characteristics of transistors in the wafer set V3.

	base/emitter					base/collector						
	Is Amps	eta	res kohms	Veb0 @1uA	Ieb0 Amps	Is Amps	eta	res kohms	Vcb0 @1uA	Icb0 Amps	max beta	Vce0 @1mA
v3-ii-18c- sub 1	1.5e-15	1.08	0.2	8.40	2.90e-12	5.1e-15	1.07	0.3	51.00	1.77e-10	70.1	51.22
v3-ii-18c-sub2	2.7e-11	2.00	0.1	0.20	1.57e-05	9.4e-15	1.08	0.3	17.40	5.64e-08	15.6	51.22
v3-ii-18-sub3	2.3e-15	1.10	0.2	8.40	2.28e-11	5.0e-14	1.20	0.3	53.00	4.19e-08	71.1	-53.66
v3-ii-18-sub4	1.7e-15	1.08	0.3	8.60	2.03e-11	6.6e-15	1.08	0.3	51.00	1.16e-11	10000.0	-51.22
v3-ii-18c-sub6	1.2e-15	1.07	0.2	8.40	7.00e-12	4.7e-15	1.06	0.3	50.40	1.39e-11	72.9	49.76
v3-ii-18c-sub8	1.3e-15	1.07	0.2	8.40	5.40e-12	4.9e-15	1.06	0.3	51.00	1.60e-11	70.9	51.22
v3-ii-18-sub9	1.9e-15	1.09	0.2	8.00	3.05e-11	7.4e-15	1.08	0.3	53.00	1.36e-11	74.2	-53.66
v3-ii-18-sub10	1.5e-15	1.08	0.2	8.40	2.71e-11	6.8e-15	1.07	0.3	53.00	2.71e-08	74.7	-53.66
v3-ii-18-sub11	1.6e-15	1.08	0.2	8.60	2.91e-11	6.2e-15	1.07	0.6	52.00	1.46e-11	2159.1	-56.10
v3-ii-18c-sub12	1.4e-15	1.08	0.2	8.50	8.10e-12	5.0e-15	1.06	0.3	52.20	1.59e-09	70.9	52.68
v3-iii-18c-sub11	1.7e-15	1.08	0.2	8.80	5.20e-12	5.3e-15	1.06	0.3	51.60	1.82e-11	74.1	51.22
v3-iii-18c-sub12	1.4e-15	1.07	0.2	8.70	4.65e-12	5.2e-15	1.06	0.3	51.00	1.13e-09	76.9	51.22
v3-iv-18c-sub2	1.6e-15	1.08	0.2	8.40	5.00e-14	6.2e-15	1.07	0.3	50.40	1.46e-11	82.5	51.22
v3-iv-18c-sub5	1.7e-15	1.08	0.2	8.60	7.35e-12	6.7e-15	1.07	0.3	49.80	1.25e-11	77.6	49.76
v3-iv-18c-sub11	2.1e-15	1.09	0.2	8.60	5.25e-12	7.1e-15	1.07	0.3	51.00	1.21e-11	76.3	51.22
v3-iv-18c-sub12	2.4e-15	1.09	0.2	8.60	1.60e-12	7.5e-15	1.08	0.3	51.00	1.37e-11	79.8	51.22
v3-ii-18-1con1	2.0e-15	1.11	0.6	7.40	6.69e-11	6.9e-15	1.08	0.3	53.00	2.44e-08	136.2	-53.66
v3-ii-18c-1con2	3.8e-15	1.12	0.5	5.90	1.76e-11	1.9e-07	2.32	0.5	1.20	8.56e-05	10000.0	4.39
v3-ii-18-1con3	1.5e-15	1.10	0.5	7.40	5.76e-11	5.4e-15	1.06	0.3	31.00	5.60e-11	148.6	-31.71
v3-ii-18c-1con4	1.4e-15	1.09	0.5	7.30	4.05e-12	4.8e-15	1.06	0.3	31.20	8.09e-09	135.4	49.76
v3-ii-18-1con5	4.1e-15	1.15	0.5	7.40	2.88e-11	7.4e-15	1.07	0.3	52.00	1.48e-11	122.3	-51.22
v3-ii-18c-1con6	1.3e-15	1.09	0.6	7.10	3.35e-12	4.6e-15	1.06	0.3	52.20	1.36e-11	127.3	52.68
v3-ii-18c-1con7	1.5e-15	1.10	0.6	7.30	6.20e-12	5.0e-15	1.06	0.3	51.60	6.65e-12	124.7	51.22
v3-ii-18c-1con8	1.5e-15	1.09	0.7	7.20	4.20e-12	5.1e-15	1.06	0.3	49.20	7.90e-12	131.8	49.76
v3-ii-18-1con9	1.9e-15	1.10	0.7	7.40	4.61e-11	8.6e-14	1.21	0.3	53.00	1.30e-11	116.1	-53.66
v3-ii-18-1con10	2.0e-15	1.11	0.8	7.40	4.69e-11	6.8e-15	1.07	0.3	53.00	1.18e-11	114.5	-53.66
v3-ii-18c-1con11	1.4e-09	1.59	1.8	2.80	3.27e-07	4.8e-15	1.05	0.3	51.00	1.51e-11	13.9	52.68
v3-ii-18c-1con12	1.1e-14	1.20	1.2	7.30	3.01e-09	1.4e-14	1.12	0.3	15.00	4.23e-07	70.5	30.73
v3-iii-18c-1con1	1.5e-15	1.09	0.9	7.30	5.10e-12	6.3e-15	1.07	0.3	50.40	1.35e-11	123.9	51.22
v3-iii-18c-1con2	1.2e-15	1.08	0.9	7.30	6.60e-12	5.5e-15	1.06	0.3	49.80	8.76e-10	121.0	49.76
v3-iii-18c-1con5	1.3e-15	1.08	1.0	7.40	6.40e-12	6.1e-15	1.06	0.3	50.40	1.30e-11	109.4	51.22
v3-iii-18c-1con8	1.2e-15	1.08	0.9	7.30	6.75e-12	5.9e-15	1.06	0.3	48.60	8.80e-12	125.9	49.76
v3-iii-18c-1con11	1.5e-15	1.09	0.8	7.40	6.40e-12	5.9e-15	1.06	0.3	47.40	7.20e-12	126.3	48.29
v3-iii-18c-1con12	8.7e-16	1.05	0.8	7.30	3.10e-12	3.3e-08	2.82	0.2	1.20	1.09e-05	3131.6	14.63
v3-iv-18c-1con1	4.9e-14	1.29	2.2	7.40	4.05e-12	5.8e-14	1.29	0.2	49.20	2.04e-11	99.2	49.76
v3-iv-18c-1con2	1.1e-15	1.08	1.0	7.50	8.50e-12	5.7e-15	1.07	0.3	51.00	1.05e-11	128.5	51.22
v3-iv-18c-1con5	1.2e-15	1.08	0.6	7.50	3.35e-12	6.4e-15	1.07	0.3	50.40	1.50e-11	122.3	51.22
v3-iv-18c-1con10	1.9e-15	1.10	0.3	8.40	2.95e-12	6.8e-15	1.07	0.3	50.40	1.28e-11	105.5	51.22
v3-iv-18c-1con11	2.1e-15	1.10	0.3	8.30	2.30e-12	7.2e-15	1.07	0.3	49.80	1.48e-11	109.5	49.76
v3-iv-18c-1con12	2.0e-15	1.10	0.3	8.60	1.70e-12	6.9e-15	1.07	0.3	51.00	1.25e-11	107.3	51.22

v3-ii-36c-sub1	4.2e-15	1.07	0.3	8.40	2.10e-12	1.4e-14	1.07	0.3	52.20	2.35e-11	75.7	51.22
v3-ii-36c-sub2	4.0e-15	1.07	0.3	8.40	3.70e-12	1.4e-14	1.07	0.3	51.00	2.43e-11	74.3	51.22
v3-ii-36-sub4	3.6e-15	1.06	0.3	8.30	1.70e-12	1.4e-14	1.07	0.3	50.40	8.90e-10	76.6	-49.76
v3-ii-36c-sub10	3.5e-15	1.06	0.3	8.40	3.15e-12	1.3e-14	1.07	0.3	50.40	2.34e-11	77.0	49.76
v3-ii-36c-sub11	3.9e-15	1.07	0.3	8.40	4.95e-12	1.3e-14	1.07	0.3	51.60	2.09e-11	75.9	51.22
v3-ii-36c-sub12	2.2e-15	1.02	0.3	8.40	2.64e-09	4.5e-10	1.73	0.3	9.00	1.87e-06	77.5	20.49
v3-iii-36c-sub6	4.7e-15	1.08	0.3	8.50	3.90e-12	1.7e-14	1.08	0.3	49.20	1.62e-11	79.7	49.76
v3-iii-36c-sub7	4.1e-15	1.07	0.3	8.50	2.80e-12	1.9e-14	1.08	0.3	48.60	1.58e-11	84.9	48.29
v3-iii-36c-sub11	4.3e-15	1.07	0.3	8.70	3.75e-12	2.0e-14	1.08	0.3	46.80	1.44e-11	84.1	46.83
v3-iii-36c-sub12	4.5e-15	1.07	0.3	8.70	1.50e-13	2.1e-14	1.09	0.3	51.00	2.16e-11	84.9	51.22
v3-iv-36c-sub7	8.6e-15	1.11	0.3	8.50	4.40e-12	4.9e-13	1.30	0.3	8.40	1.18e-05	81.4	11.71
v3-iv-36c-sub8	5.6e-15	1.08	0.3	8.60	4.05e-12	2.1e-14	1.09	0.3	51.00	1.51e-11	83.5	49.76
v3-iv-36c-sub9	5.2e-15	1.08	0.3	8.30	7.20e-12	2.1e-14	1.09	0.3	43.80	2.02e-08	83.5	46.83
v3-iv-36c-sub10	4.9e-15	1.08	0.3	8.50	3.55e-12	2.2e-14	1.09	0.3	49.80	3.64e-11	84.0	49.76
v3-iv-36c-sub11	6.4e-15	1.09	0.3	8.60	1.20e-10	2.9e-14	1.11	0.3	49.80	2.84e-08	84.5	49.76
v3-iv-36c-sub12	5.8e-15	1.07	0.3	8.60	2.62e-11	2.7e-14	1.10	0.3	18.60	2.33e-08	87.3	42.44
v3-ii-36c-1con1	3.4e-15	1.08	0.3	7.30	3.75e-12	8.6e-15	1.05	0.3	46.20	2.72e-11	228.9	46.83
v3-ii-36c-1con2	4.2e-15	1.09	0.3	7.30	2.25e-12	1.0e-14	1.05	0.3	52.20	4.24e-11	218.9	51.22
v3-ii-36-1con4	2.9e-15	1.07	0.3	7.30	4.45e-12	8.2e-15	1.04	0.3	51.00	1.33e-09	234.0	-51.22
v3-ii-36-1con7	2.7e-15	1.07	0.3	7.30	3.70e-12	8.2e-15	1.04	0.3	32.40	3.13e-10	240.3	-32.20
v3-ii-36-1con9	2.5e-15	1.07	0.3	7.10	3.35e-12	7.5e-15	1.04	0.3	51.00	2.60e-11	240.5	-49.76
v3-ii-36c-1con10	2.9e-15	1.07	0.3	7.30	4.80e-12	7.9e-15	1.04	0.3	50.40	2.04e-11	236.2	49.76
v3-ii-36c-1con11	3.3e-15	1.08	0.3	7.30	3.10e-12	8.4e-15	1.04	0.3	52.20	1.22e-10	224.8	51.22
v3-ii-36c-1con12	3.7e-15	1.08	0.3	7.30	2.85e-12	9.6e-15	1.04	0.3	53.40	1.98e-11	210.9	52.68
v3-iii-36c-1con1	2.2e-15	1.12	0.3	6.30	2.10e-10	1.4e-14	1.07	0.7	8.40	3.61e-06	74.0	51.22
v3-iii-36c-1con2	2.8e-16	1.06	0.3	6.80	6.05e-11	1.5e-14	1.07	1.4	50.40	2.62e-08	386.3	51.22
v3-iii-36c-1con4	5.2e-16	1.09	0.3	6.90	1.90e-10	1.1e-14	1.06	0.3	11.40	2.12e-06	85.0	11.71
v3-iii-36c-1con5	6.5e-16	1.08	0.3	6.90	2.02e-11	8.7e-15	1.04	0.4	50.40	5.15e-10	88.6	51.22
v3-iii-36c-1con6	1.6e-15	1.05	0.3	7.10	8.00e-12	1.1e-14	1.06	0.3	50.40	1.38e-11	324.4	49.76
v3-iii-36c-1con7	1.6e-15	1.04	0.3	7.30	5.05e-12	9.1e-15	1.05	0.3	50.40	4.43e-10	304.9	49.76
v3-iii-36c-1con8	1.8e-15	1.05	0.3	7.30	6.65e-12	9.5e-15	1.05	0.3	50.40	1.30e-11	281.8	49.76
v3-iii-36c-1con11	2.1e-15	1.05	0.3	7.40	5.35e-12	9.7e-15	1.05	0.3	51.60	6.95e-12	273.0	51.22
v3-iv-36c-1con1	4.3e-16	1.08	0.4	6.30	6.83e-10	1.1e-14	1.05	1.0	50.40	6.85e-12	26.9	51.22
v3-iv-36c-1con2	4.0e-16	1.08	0.4	6.80	7.32e-11	2.4e-14	1.10	1.4	6.60	5.77e-05	33.4	11.71
v3-iv-36c-1con3	2.9e-16	1.07	0.4	6.90	3.94e-11	9.3e-15	1.05	0.4	49.80	7.40e-12	27.5	51.22
v3-iv-36c-1con5	4.0e-16	1.07	0.4	6.90	2.54e-11	1.1e-14	1.05	0.3	49.80	5.85e-12	33.7	51.22
v3-iv-36c-1con6	3.0e-15	1.08	0.3	7.40	5.90e-12	1.3e-14	1.07	0.3	50.40	1.78e-11	205.1	49.76
v3-iv-36c-1con9	4.4e-15	1.09	0.3	7.90	3.50e-12	1.5e-14	1.08	0.3	49.80	2.52e-11	199.9	49.76
v3-iv-36c-1con10	4.9e-15	1.09	0.3	7.90	5.35e-10	1.8e-14	1.08	0.3	50.40	1.36e-11	212.7	49.76
v3-iv-36c-1con12	3.0e-15	1.06	0.3	7.80	6.50e-12	1.5e-14	1.07	0.3	52.20	1.49e-11	239.9	51.22

Table 4.2 Comparison of junction depth, base width, sheet resistance, and oxide thickness between SUPREM III simulation and measurement for the wafer set V3.

Parameter		Measurement	SUPREM
Poly-contact Thickness (Å)		1054	928
Junction Depth (μ)	base/emit	0.10	0.16
	base/coll under emit	0.30	0.68
Base Width (μ)		0.20	0.52
Sheet Resistance ($\Omega/\square$)	poly-contact	5,870	2,776
	emitter	150.0	65.3
	base-pinch	28,700	6,065
Oxide Thickness (Å) after	initial oxid.	2364	2625
	base diff.	1198	1410
	emitter diff.	398	423
	poly-anneal	1453	1300

CHAPTER V
CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE RESEARCH

5.1. Conclusions

This research was concerned with design and fabrication of polysilicon contacted shallow emitter bipolar transistors. The emitter of the transistor is composed of both a polysilicon region and a monocrystalline silicon region. The use of polysilicon as the material contacting the emitter is responsible for a higher current gain than that of the same device with a conventional aluminum contact. Essential to the process development was the formation of a shallow emitter junction depth and a narrow base width. Also a low base-emitter contact resistance was desirable.

Enhanced beta of a polysilicon contacted device over a conventional device was achieved only with a shallow emitter and a narrow base width. These conditions were satisfied by determining the appropriate implant species, dose, and energy for the base, emitter, and polysilicon contact. They also required the high temperature processes to be minimized. Implants for all species were done at the energy of 25keV for producing narrow but good metallurgical junctions. Arsenic was chosen as the emitter dopant because of its higher solid solubility and lower diffusion rate as compared to phosphorus.

The low base-emitter contact resistance resulted from a series of experiments which investigated the effects of the polysilicon/monosilicon contact scheme on polysilicon contacted device performance. These experiments demonstrated that high temperature annealing of the polysilicon contact was an effective technique to reduce the base-emitter resistance, which implies breaking up the native interface oxide layer. In particular, with 1000 ° C anneals of the polysilicon contact, after polysilicon deposition by LPCVD, the polysilicon contacted devices showed lower base-emitter resistances. They also successfully produced beta enhancement of a factor of

three over conventional metal contacted shallow emitter devices.

The standard deviations of the peak beta values of the polysilicon contacted emitter devices were reduced by depositing α-Si:H in a PECVD reactor, followed by implanting with arsenic, and then annealing it to form the polysilicon. The result was the capability of fabricating consistently reproducible polysilicon contacted devices. With 900 °C annealing, the polysilicon contacted devices, with low base-emitter contact resistance, produced very compact peak betas that are enhanced three times over those of the conventional devices. With 800 °C annealing, the polysilicon contacted emitter devices showed beta enhancement of a factor of two over the conventional devices. This reduced beta enhancement might have been caused by the interfacial oxide layer that was not broken up. Once the interfacial oxide layer is broken up removed completely, higher beta enhancements are expected even with low temperature ($\leq$800 °C) annealing.

Two other experiments were performed. As an effort of cleaning the interfacial oxide layer, *in situ* etching was attempted with Ar^+ gas before α-Si:H deposition in PECVD reactor. Also, the dependence of beta enhancement of the polysilicon contacted emitter devices on base doping concentration was investigated.

5.2. Recommendations for Future Research

The investigation described in this research has laid the foundations for additional work into the study of the polysilicon contacted, shallow emitter bipolar transistors. In particular, additional investigation needs to be done in the area of fabrication improvements and refinements.

Although the polysilicon contacted devices fabricated with the process sequence developed here are state-of-the-art, improvements are still desirable. For example, a completely "clean" polysilicon/monosilicon interface will produce consistently reproducible polysilicon contacted devices with good predictable beta enhancement. For this improvement, H_2 plasma etching seems promising because it may passivate some of the surface states and reduce the effects due to plasma etching. It is also beneficial to have H_2 in the polysilicon since it reduces carrier recombination at the grain boundaries. The hydrogen ions will bond the dangling bonds and defects at the silicon-oxide interface and at the grain boundaries reducing number of

traps, which reduces the surface leakage currents.

A "clean" polysilicon/monosilicon interface may be achieved by just using an improved set of optimized α-Si:H deposition parameters with PECVD. These parameters consisted of the RF power level, substrate temperature, pressure, and silane concentration used in the glow discharge deposition technique. With a "clean" interface, the characteristics of polysilicon contact will have a large effect on the device performance. More thorough research may also be required on the electrical properties of polysilicon and its dependence on the grain size, processing temperature, doping concentration, density of the trapping sites, and grain boundary barriers.

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APPENDICES

Appendix A: Cleaning Procedures

The following list contains the procedures for processing clean-ups used throughout the fabrications. Procedures for initial wafer clean, processing and equipment clean, and positive photoresist clean are listed below. The cleaning solvents are low sodium MOS grade acetone (ACE), trichloroethane (TCA), and methanol (METH). Abbreviations for other process chemicals are: deionized water (DI), and buffered hydrofluoric acid, NH_4:HF, 6:1 (BHF).

Initial Wafer Clean

1) Soak in H_2O_2 : H_2SO_4 (1:1) for 10 min.
2) DI rinse (10 times).
3) N_2 blow dry.

Equipment Clean (Ultraclean) for Tweezers

1) Soak 5 min. in ACE in the USC.
2) Soak 5 min. in TCA in the USC.
3) Soak 5 min. in ACE in the USC.
4) Soak 3 min. in METH in the USC.
5) DI rinse (10 times).
6) N_2 blow dry.

1350J or 1350J-SF Positive Photoresist Clean

1) Soak 1 min. in ACE in the USC.
2) Soak 1 min. in ACE in the USC.
3) Soak 1 min. in METH in the USC.
4) DI rinse (10 times).
5) Soak in H_2 : H_2SO_4 (1:1) for 10 min.
6) DI rinse (10 times).
7) N_2 blow dry

Appendix B: Chemical Etches

This section contains the chemical formula and chemical etching procedures. Etches for SiO_2, polysilicon, and amorphous silicon are listed. Etch rates and masking materials are stated and any exceptions noted.

Silicon Dioxide

1) Etchant:

   Buffered Hydrofluoric Acid (BHF)
   NH_4:HF (6:1)

2) Etch rate : $\sim$1100Å/min

3) Mask : any positive or negative photoresist

Note : Batch etching can be done with the wafers loaded vertically into a cleaning boat. Agitation is good to provide good etching in small holes ($\sim 10\mu$). Use only fluoroware or polypropylene equipment with BHF.

Poly and Amorphous Silicon

1) Etchant :

92 ml	HNO_3
47 ml	DI
5 ml	HF

2) Etch rate : $\sim$75Å/sec

3) Mask : AZ1350J or AZ1350J-SF positive photoresist

Note : good on all thickness of polysilicon and amorphous silicon films, excellent shelf life, etched patterns sharp to $\simeq 1.5\mu$. wait 2 hrs. after fresh mix for etchant to stabilize before use, will etch SiO_2 slightly.

Appendix C: Photolithography Procedure

This section contains the procedures for the application, exposure, and development of positive photoresist. The positive photoresist is Shipley AZ1350J or AZ1350J-SF. The mask aligner used is a Kasper 2" contact mask aligner. The photomasks used are 2 1/2" emulsion plates.

Positive Photoresist Procedure

1) hard bake @120 ° C for 10min.
2) Set resist spinner to 4000rpm and 30sec.
3) Place wafer on spinner and N_2 blow off the dirt.
4) Apply Shipley AZ1350J or AZ1350J-SF positive photoresist.
5) Spin wafer - resulting resist is $\sim 1.5\mu$ thick.
6) Soft bake @80 ° C for 15 min.
7) Start ultraviolet lamp on mask aligner - warm up 10 min.
8) Align photomask to wafer.
9) Expose photoresist - exposure setting at 12.0 (about 97 sec).
10) Develop photoresist.
    1:1 AZ developer:DI for 50-90sec
11) DI rinse.
12) N_2 blow dry (not too strong).
13) Inspect pattern - clean and repeat if necessary.
14) Hard bake @120 ° C for 20min.
15) Etch material.
16) Remove resist as outlined in cleaning procedure.

Note : Apply HMDS on wafer in vacuum jar for 10min under reduced pressure after step (1), if amorphous silicon was deposited.

Appendix D: Oxidation Procedures

This section contains the procedure and settings for thermal oxidations and anneals. The furnaces can be used in either manual or automatic mode. The manual mode is hand timed, while the automatic mode is microprocessor controlled. For our process, only the manual mode was used. The furnaces are 4" Tempress radiant heated furnaces with regulated gas flow. The procedures below are step by step instructions to perform the step. Timing information for the oxidations or anneals is contained in the complete process sheet.

Dry Oxidation

1) Furnace tubes #1, #4, or #5 can be used.
2) Set the furnace temperature - wait for stabilization ($>$ 30 min.).
3) Open O_2 bottle and set the regulator to $\sim$26.
4) Open O_2 overhead regulator and set it to $\sim$15.
5) Set N_2 flow rate to 50 on the flow meter (stainless steel ball).
6) Set the switches for O_2 and N_2 on the back panel to manual.
7) Set O_2 flow rate to 90 on the flow meter (black glass ball).
8) Reset the control switches to center off position.
9) Purge the furnace with O_2 for 5min.
10) Use the elephant to take the wafer boat out of the tube.
11) Load wafers on the wafer boat with shiny side inward the elephant.
12) Push the wafer boat into the tube from the elephant.
13) 3 min. push of the boat to the middle of the tube.
14) 2 min. N_2 purge.
15) Set the switches for O_2 and N_2 to manual.
16) Oxidize in dry O_2 - keep the flow rate to 60 (black glass ball).
17) Return the switches to center off.

18) 2 min. N_2 purge.
19) 3 min. pull of the boat in N_2 out of the tube.
20) Unload wafers and replace the boat.
22) Back off O_2 overhead gas regulator.
23) Close O_2 cylinder.

H_2 Burn Oxidation (Wet Oxidation)

1) Furnace tube #4 can be used only.
2) Set the furniture temperature - wait for stabilization ($>$ 30 min.).
3) Open O_2 bottle and set the regulator to $\sim$26.
4) Open H_2 bottle and set the regulator to $\sim$15.
5) Set the overhead gas regulators to 15/8 for O_2/H_2 respectively.
6) Set the control switches of O_2 and N_2 on back panel to manual
7) Set O_2 flow rate to 90 on the flow meter (black glass ball).
8) Set the control switch of H_2 to manual.
9) Set H_2 flow rate to 90 on the flow meter (black glass ball).
10) 2 min. purge of the tube with burning H_2.
11) Set the control switch of H_2 to center off.
12) Use the elephant to take the wafer boat out of the tube.
13) Load wafers on the wafer boat with shiny side inward the elephant.
14) Push the wafer boat into the tube from the elephant.
15) 3 min. push of the boat to the middle of the tube.
16) Set O_2 flow rate to 60 (black glass ball).
17) 2 min. dry oxidation (for stabilization).
18) Set the control switch of H_2 to manual.
19) Measure the oxidation time (keep the flow rate).
20) Return all control switches to center off.
21) 2 min. N_2 purge.

22) 3 min. pull of the boat in N_2 out of the tube.
23) Unload wafers and replace the boat in the tube.
24) Back off the overhead gas regulators for O_2 and H_2.
25) Close O_2 and H_2 cylinders.

Nitrogen (N_2) Anneal

1) Furnace tube #8 to be used only.
2) Follow the steps 4-22 of dry O_2 oxidation, substituting N_2 for O_2. No need to turn on oxygen at all.

Appendix E: LPCVD Operating Procedure

The Low Pressure Chemical Vapor Deposition (LPCVD) of polysilicon is performed in a microprocessor controlled, vacuum pumped, radiant heated quartz furnace.

LPCVD Operation

1) Set the furnace temperature - profiled for 580 ° C to 710 ° C.
   Back : +59.1 = 608 ° C
   Center : 601.0 = 600 ° C
   Front : +46.3 = 592 ° C
2) Change the wafer boat, if necessary.
   There are corresponding wafer boats for 3" and 2" wafers.
3) Turn on the pump system by pressing black button on the overhead.
4) Open N_2 and AUX Air gang valves on the overhead control cabinet (vertical position).
5) Switch 1, 2, and 3 up (flood tube with N_2).
6) Check the pressure of the tube.
   When the pressure is $\geq$ 760 Torr, the system is ready for loading.
7) Open the loading door, pull out the wafer boat, and load wafers.
8) Push the boat to the center of the tube.
   Push until the push-rod end aligns to the square entrance.
9) Close the loading door - make sure the flap is all the way down.
10) Open SiH_4 and N_2 pump/purge valves in the control cabinet overhead (vertical position).
11) Open N_2 cylinder, set N_2 to 32 psi (usually set).
    Switch 17 down, set the flow rate to 10 on the flow meter, and switch 17 back up.
12) Open SiH_4 cylinder.
    Regulator for the tank is always set (Do not change).
13) Switch 1, 2, and 3 down (stop all N_2 flow).

14) Turn the key to 'EXAM LOAD' and then to 'AUTO'.
15) Change the controller program at this time, if necessary.
16) Set SiH_4 mass flow controller to desired flow rate (50 sccm).
17) Select program # (#1) and press 'SYS RESET'.
18) Turn the key to 'MANUAL' and then to 'RUN'.
19) Turn the key switch from 'MANUAL' to 'AUTO'.

Now the deposition is proceeding under microprocessor control, and if the program aborts for any reason, immediately turn off the SiH_4 gang valve. Check the system to determine what caused the malfunction. If the abort is due to a programming fault, then check and correct the program. However, if the fault is mechanical in nature (i.e., valve, pump, mass flow controller, etc...), then continue to purge the tube and pump housing with N_2 and alert lab personnel to determine exact cause and potential hazard.

20) When the process is completed, close all 4 switches (SiH_4, N_2 pump/purge, N_2, and Aux Air gang valves) in the control cabinet overhead.
21) Close SiH_4 and N_2 cylinders.
22) Turn the key from 'AUTO' to 'MANUAL', then press 'SYS RESET'.
23) Open the loading door, remove the boat, unload wafers, replace the boat to the center of the furnace tube, and close the loading door.
24) Turn off the pump system power by pressing red button on overhead.

Appendix F: PECVD Operating Procedure

Plasma Enhanced Chemical Vapor Deposition (PECVD) has been used for more than 50 years to form metallic, semiconducting, and insulating thin film for a variety of applications. The use of a radio frequency (rf) glow discharge has become an attractive method for carrying out low temperature CVD, because the development of low-temperature processes has become essential to the continuing development of smaller, faster solid-state devices and circuits. In PECVD, high-energy electrons break chemical bonds, thereby promoting chemical reactions at reduced temperature and allowing temperature to be used as a variable to tailor film properties.

This section contains the procedure and settings for depositing α-Si:H using PECVD technique.

Pre-Deposition Set-Up

1) Inspect overall system integrity.

   Insure plugs are positioned an wall sockets for the Plasma Etch Unit (PEII-A), the Plasma Deposition Unit (PDII-B), the Exhaust Heater Controller (EHC), the Exhaust Valve Controller (EVC), and the Pump Switch Assembly.

   Also, insure that the gas and exhaust lines are intact and not kinked and that the pumps and water lines are not leaking.

2) Open N_2 cylinder and set the regulator to $\sim$3 psi.
   Make sure N_2 makes bubbling through the water.

3) Open the House N_2 valve, Air valve, and Water Supply and Return Lines.

4) Insure that the Ar tank is open (normally it is open). If not, open it.

5) Turn on POWER on the PEII-A, EVC, and EHC.

6) Set the EHC to 6 on the left switch (coarse control) and 4 on the right switch (fine control) located under the table, i.e. 6/4.

7) Turn on the mechanical pump and the oil filtration pump.

8) Push on the HEATER on the PDII-B and set the temperature to a desired value (275 °C for α-Si:H deposition).

9) Open the VENT valve on the PEII-A.
Wait for about 10 sec. until the pressure becomes atmospheric pressure and the top chamber lid is loose. Then close the VENT valve.

10) Open the chamber lid and place wafers on the plate concentric to the center. Then close the lid.

11) Insure the EVC control switch is set to OPEN and open the SOL'N valve.

12) When the pressure becomes ~0.5 Torr, open GAS 2 (Ar) and set the Ar flow rate so that the pressure becomes ~200 mTorr.
Wait for the temperature to stabilize to its set value (275 ° C here). It takes about 30 minutes.

α-Si:H Deposition

1) Insure the PDII-B/PEII-A switch on rear of the PEII-A is set to PDII-A (toward the left wall)

2) Set the DISPLAY CHANNEL to 3 on the PDII-B.
Press SET PT/READ switch to SET PT (upward) and adjust SET PT screw for correct sccm flow (40 sccm here) on the display.

3) Carefully open the SiH_4 gas line and cylinder.

4) Switch off the GAS 2 (Ar).
Switch on the GAS 1 (SiH_4) when the pressure becomes ~100 mTorr.
Switch on 3 (green light) on the PDII-B.

5) Change the EHC setting to 5/6.

6) Set the EVC control knob to AUTO mode.
If the pressure is different from the set valve, adjust the pressure to the desired value (400 mTorr here) using the controller on the EVC.

7) Turn the power knob fully c.c.w. and turn on the plasma power.
Turn the power knob c.w. to set to the desired power level (5W here).

8) Wait the desired time for deposition.

Shutting Down the System

1) Turn the power knob fully c.c.w. and turn off the plasma power.
2) Turn the EVC control knob to OPEN and turn off the switch 3 on the PDII-B.
3) When the pressure reaches about 100 mTorr, turn off GAS 1 (SiH_4) and turn on the GAS 2 (Ar) .
   Then increase the Ar flow rate until the pressure exceeds 0.5 Torr.
4) Close SiH_4 gas line and cylinder.
   Turn off POWER on the PDII-B.
5) Wait for 25 minutes or more. This is extremely important purge step!!!
6) Turn of the GAS 2 (Ar).
   Open the VENT valve and wait for about 10 sec.
   Close the SOL'N valve.
7) Wait for about 30 sec. and close the VENT valve.
   Open the chamber lid, unload the wafers, and close the chamber lid.
8) Cleaning the chamber - Refer to the next section.
9) Open the SOL'N valve.
   Wait until the pressure does not drop any more ($\leq$ 100 mTorr).
   Close the SOL'N valve.
10) Turn off EVC, EHC, mechanical pump, and PEII-A.
    Close N_2 valve, Air valve, and two Water lines.
    Close N_2 cylinder.

Cleaning the Chamber

1) Set the PDII-B/PEII-A switch on the rear of the PEII-A to PEII-A.
2) Open the SOL'N valve.
   When the pressure becomes $\sim$0.4 Torr, turn the EVC control knob to AUTO.
3) Open O_2, CH_4 cylinders.
4) Turn on the GAS 1 (O_2 and CH_4 mixture).
   Adjust the flow rate s O_2:CH_4 = 1:4 (7:28 on the flow meter).

5) Turn the power knob fully counter-clockwise.
Turn on the POWER on the PEII-A.
Slowly keep increasing power fully without making a flash in the chamber.

6) The power will increase as the plasma etches the chamber.
Wait until the power becomes about 497 watts.

7) Turn the power knob fully counter-clockwise
Turn off the POWER on the PEII-A.

8) Turn the EVC control knob to OPEN.
Turn off the GAS 1 (O_2 and CH_4 mixture) and turn on the GAS 2 (Ar).

Appendix G: Metallization Procedure (Auto Mode)

In this research, metalization was performed using Perkin-Elmer RF Sputtering Systems. The sputtering systems can deposit a wide variety of materials onto substrates such as ceramics, metals, plastics, glass, and semiconductors. Resulting thin films can range in thickness from a few angstroms up to a fraction of millimeter. They also can sequentially deposit up to three different materials onto a single substrate, thus attaining sandwich-structured films such as multi-layer optical interference filters or semiconductor devices. The systems also can be used for sputter-etching, a process in which material is removed from, rather than deposited on, the substrate.

This section contains the procedure and settings for depositing Al-1%SI for metallization.

Venting and Loading/Unloading Procedure

1) Check the log-book to make sure the system is ready for operation.
   If the key is not in AUTO, turn it to AUTO.
2) Turning off the ion gauge.
   - Set the gauge function switch to ST2 (chamber thermocouple gauge).
   - Set the gauge mode switch to AIR-HOLD (air calibration).
3) Press START and VENT simultaneously.

   The HIGH-VAC valve will close (LED off) immediately, if open.
   After a short delay (~5 sec.), the VENT valve will open (LED on).
   This backfills the chamber with N_2.

   Wait until one hears a 'click' indicating that the chamber is at atmospheric pressure. It takes about 4~5 min.
4) Press and hold the HOIST UP position in order to raise the sputtering head until the J-arm clears the chamber walls.
5) Check the TABLE POSITION.
   - If the TABLE POSITION is not set to TABLE 3, then turn on the main power switch of the RF generator (located on the front panel of

the generator, which is on the floor to the left of the system), change the table position to TABLE 3, and turn off the power. - If the TABLE POSITION is set to TABLE 3, then take the pallet under TARGET 3 out of the chamber.

6) Load/Unload the wafers on/off the pallet and slide it back into the chamber.
Insure the pallet does not touch the outer edge of the table.
Make sure that the J-arm/substrate is correctly positioned under the target.

7) Press and hold HOIST DOWN position to lower the sputtering head until motor quits.
- Align the top and the bottom and be careful not to pinch fingers.

8) Press START and PUMP simultaneously.

After a short time (~5 sec.), the ROUGHING VALVE will open (LED on). This connects the mechanical vacuum pump to the chamber.
When the pressure reaches the crossover point (TRIP LED on), the ROUGHING VALVE will close. After a short delay ($\leq$ 5 sec.), the HIGH-VAC valve should open (LED on), and the pressure should decrease quickly.

If the pressure is too high for the crossover, the TRIP LED will turn off and the pressure will increase. If this happens, repeat step 8.

9) When the pressure decreases quickly after the trip point, turn on ion gauge.
- Turn the gauge mode switch to ARGON-AUTO.
- Turn the gauge function to .1 position.
- Press FILAMENT momentarily (~1/2 sec.).

10) Wait until the pressure goes down to $2\text{-}3\text{x}10^{-7}$ Torr. This usually takes 2-3 hours after the HIGH-VAC valve is opened.

Presputter Procedure

1) Push START and GAS simultaneously.

The GAS mode will close THROTTLE VALVE (LED on) and the pressure will go down up to a little (still $\leq 10^{-6}$).

2) Set the gauge function to ST2 and the gauge mode to ARGON-AUTO.

3) Check if the Ar tank is open (it should be always open), and admit the Ar sputtering gas to the chamber by opening the right toggle switch on the sputtering head (switch up = open).

4) Adjust the Ar flow so that the pressure becomes about 8 mTorr using the needle valve on the sputtering head (usually value is ~18).

5) Turn on the main power switch of the RF generator.
Wait 60 seconds for the generator to warm up.
Select TARGET 1 (Al-Si) on TARGET SELECTOR and TARGET 3 for TABLE POSITION to move the wafers away from the TARGET 1 during presputter.

6) Select the SPUTTER DEPOSIT mode.

7) Turn the POWER ADJUST potentiometer fully counter-clockwise and turn on the POWER switch on the sputtering head (light will come on).

8) One can tune the system for a minimum in the reflected power by adjusting the tuning capacitor (TUNE) and the load inductor (LOAD) located on the front panel of the sputtering head.
Keep the reflected power below 20 watts while testing and about 10 watts while sputtering. Optimum position is about 6.2 for the LOAD and about 4 for the TUNE.

9) Start tuning up the power until the forward power becomes 300 watts.
Make sure the reflected power is still low.
Plasma (usually blue light) will appear when tuning up the power.

10) Keep an eye on the power gauge. The reflected power may go down after 1-2 min. since the presputter etches the surface (oxide and/or nitride) of the target.

11) Retune the system until the reflected power becomes less than 10 watts with the forward power being 300 watts.

12) Run for the desired amount of time (10 min. here) after settling down.

Sputtering Procedure

1) Adjust the POWER ADJUST to set the forward power to 100 watts.
The reflected power may change. If that happens, tune the system

again.

2) Set the TABLE POSITION to TARGET 1 (Al-1%Si).
   Make sure TARGET 1 is set for the TARGET SELECTOR.
3) Start sputtering for desired time (30 min. here) and fill in the data.
4) When the sputter is done, turn the POWER ADJUST knob fully counter-clockwise and turn off the POWER switch.
5) Close Ar gas by closing the toggle switch on the sputtering head (switch down = closed).
6) Change the TABLE SELECTOR to TARGET 3 and wait until the table gets to the right position.
7) Turn off the main power switch on the RF generator.
8) Unload the wafers following the procedure described in earlier section.

Appendix H: Electrical Test Procedures

All tests were performed using the HP4145A Semiconductor Parameter Analyzer after the devices were packaged in a dual-in-line package (DIP) for stability and accuracy. The 4145A is a fully automatic, high performance instrument designed to measure, analyze, and graphically display the DC parameters and characteristics of diodes, transistors, ICs, solar cells, and wafers during the fabrication process. It is equipped with four programmable stimulus/measurement units (SMUs). Each SMU can be programmed to function as a voltage source/current monitor or a current source/voltage monitor. Mode changes and channel reassignment are fully automatic, eliminating test lead connection changes. This feature simplifies operation and significantly increases measurement speed and reliability.

Measurement setups can be done manually for every measurement or up to 43 user-generated measurement setups (or 10 sets of measurement results) can be stored on a single built-in flexible-disc. The 4145A also can be remotedly controlled via the HP-IB (Hewlett-Packard Interface Bus), a carefully defined instrument interface, which is used to pass program control between the controller and the various instruments and wafer prober.

In this research, the HP9845A desk top computer was used to process the measurement data initially and then to transmit the data to the host computer, VAX 11/780. The host computer can then use this data to attach numerical values to device parameters and determine distribution patterns. Measurement setups for the transistor measurements are written in a control program, called "UNIXA", which is saved on a flexible disc.

Loading Test Program into HP9845A

1) Hold down CONTROL then press STOP on the 9845A key board to reset the 9845A.
2) Type **MASS STORAGE IS ":F8".** to specify the mass storage unit to be a flexible disc.
3) Press EXECUTE.
4) Insert the flexible disc into disc drive.

5) Type **LOAD "UNIXA"** and press EXECUTE.
6) Wait for the light on the disc drive to be turned off.
7) Take the flexible disc out of disc drive.

Setting Up the Test Station

1) Put the socket board with a 24-pin dual-in-line socket in the 16058A.
2) Set up the 16058A's Personality Board as follows:

   SMU1 : emitter
   SMU2 : base
   SMU3 : collector
   SMU4 : N/A

4) Insert the dual in-line package (DIP) containing bonded devices into the DUT socket.
5) Turn on the 4145A.

The HP16058A Test Fixture is designed for use with the HP4145A. The 16058A holds the device to be tested with the 4145A, and provides all necessary connections to the test input/output terminals of the 4145A. For stable and accurate measurements at extremely low current levels, the 16058A is equipped with an electrostatic light-shielding cover. To facilitate testing various types of devices, eight interchangeable socket bonds and three types of special plug leads are furnished with the 16058A.

Measurement and Data Collection

All measurements are directed by the control program called "UNIXA". The program starts by prompting the inputs for the Die, Device, and Date. These procedures are for making new directories with these names in a directory /a/poly/data. It also asks whether the default values would be used or not for the limits. The default values are generally used nevertheless the user can change the limits.

When these are done, the 4145A starts to test a device, graphically display the characteristics. There are six test routines; I-V characteristics of

base/emitter with reverse and forward bias, I-V characteristics of base/collector with reverse and forward bias, I_C-V_{CE} static collector characteristics with changing I_B, and I_C-V_{BE} & I_B-V_{BE} characteristics using Gummel plot. The 9845A collects the data and saves it in the buffer temporarily after each measurement. When testing is over, the 9845A sends all data into a file in the designated directory.

1) Press RUN to connect the 9845A to ECN UNIX system.
   Then the UNIX system will type a short message and wait for a login name.
2) Type login name (polye) and press CONT.
   Even though the message does not show the prompt "login:", you will see it when the login name is typed and CONT is pressed.
3) Press K2 (LOCAL ECHO ON/OFF) in Special Function Keys so that UNIX will not print (or echo) what you type on the terminal screen.
4) Type password and press CONT.
5) Press K2 to turn echo on then UNIX will prompt with "$" for input.
6) Press K0 (UPLOAD/DOWNLOAD) in Special Function Keys to run the program "UNIXA".
7) The program will prompt your input. An example is as follows:

PROMPT	INPUT
Die?	v3-ii-36
Device?	1con3
Date?	1-1-88

8) Respond to the prompts by giving names for each prompt as shown above.
   If the default values are to be used, type "y" to the last prompt.
   If "n" is typed, the program will ask you to type all the limit values.
   After the default values are determined the program will start to test the devices and send the data to a designated file.

Generating Device Parameters

When the data is transferred and stored in a file /a/polye/data/v3-ii-36/1con3/data, as an example, it is composed of a column of numbers. This data is converted into device parameters by using a program written in C language ,which is called ".ff.c". Running the executable file ".ff" calculates the device parameters and store them in three different files; "ll", "line", and "beta". A file called "beta" consists of only device name and beta value. Both "ll" and "line" have same parameters with slightly different format. An example of each is shown in Figure H.1. There is another program called ".format.c", which not only calculates the device parameters but also creates plots from the data by executing ".format". This file contains Qplot commands that are used to plot one vector versus another on various graphic devices.

The device parameters of a set of devices can be collected in one file by concatenating the files named as "line" of a set of devices.

1) Type "pwd" to see what the current working directory is.
2) If the current directory is /a/polye/data/Die/Device, type ".ff" to create "line", "ll", and "beta".
   If the current directory is not /a/polye/data/Die/Device, change the current directory to that and execute ".ff".