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Neudeck, G. W.; Gray, J. L.; Klaasen, W.; Egley, J.; Pak, J.; and Bagri, R., "Polysilicon Emitter Fabrication and Modeling" (1986). *Department of Electrical and Computer Engineering Technical Reports.* Paper 556.
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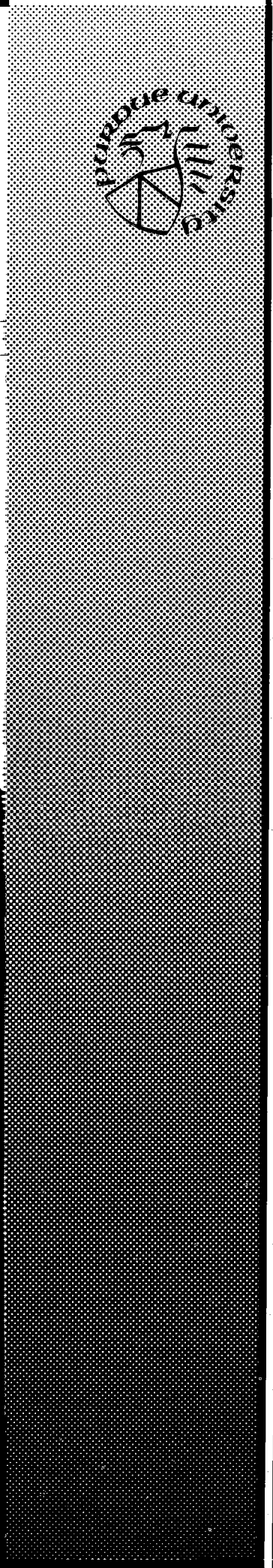

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TR-EE 87-7
January 1, 1986 to December 31, 1986

School of Electrical Engineering
Purdue University
West Lafayette, Indiana 47907

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Supported by Delco Electronics

Contents

Executive Summary

The research proposed for 1986 was to develop the technology for fabricating, measuring, and computer modeling the polysilicon emitter bipolar transistor. Fabrication consisted of producing three types of bipolar transistors; a regular bipolar device to act as the control, a polysilicon contacted emitter transistor, and a polysilicon emitter directly on the base region with a very thin oxide at the interface. The proposed fabrication research concentrated on investigating a new method of fabricating polysilicon contacted emitter bipolar transistors.

The new fabrication technique uses plasma etching of the emitter location on the base region and, without breaking vacuum, depositing amorphous silicon (a-Si) on the cleaned interface. The a-Si was then to be doped by ion-implantation and heated to 600-700 C° to produce the polysilicon emitter contact. The controlled interface and the fine grained polysilicon should lead to more uniform and predictable betas for the polycontacted transistors. Both polysilicon contacted emitters and polysilicon emitters were to be investigated over a range of base doping.

We proposed the modeling work in two directions: 1) 2-D simulation so that small geometry transistors can be accurately modeled and 2) simulation of polysilicon contacted emitter transistors. Measurements on the devices described above will be used to develop a polysilicon model. The objective of this part of the project is to develop a numerical device simulator with predictive capability, i.e. one that can be used with confidence in place of actual device fabrication. The numerical device models will be provided to Delco and should find many applications in development and manufacturing.

The fabrication highlights of the 1986 work were the design and fabrication of preliminary bipolar transistors and polysilicon emitters, the design and layout of the test wafer, and the fabrication and measurements on shallow arsenic doped emitter devices. There were 22 sets of fabrication runs made beyond the preliminary devices.

The last results of these runs show that the shallow Arsenic emitter (0.05 μ) and the very narrow base width (0.1 μ) control devices with metal emitter contact, have an average peak beta of about 75. Poly contacted emitter devices fabricated at the same time on the same wafer show a beta enhancement to 232, a factor of about 2.7 to 3.0 in the average peak beta. The polysilicon was deposited in a standard way in a LPCVD tube. We are presently fabricating polysilicon devices for studying the effects of the methods used in treating the surfaces before the poly is deposited and the way the poly is formed (amorphous PELPCVD).

1986 Goals/Progress

Goal #1. Polysilicon N^+-Contacted Emitter

(a) Modified existing bipolar process and produced *preliminary* poly emitter and regular BJT devices. Showed good beta enhancement.

(b) Developed test chip and photo plates for demonstrating the effect of Poly emitters as compared to a control (called substrate device) BJT. Completed successfully with phosphorous emitters.

(c) Amorphous silicon produced by LPCVD and PELPCVD deposited on emitter structures. Have completed 22 fabrication sets of each of 4 types of devices. The initial results were not as good as expected.

(d) Modified the bipolar process for the control device to have shallow arsenic emitters (an addition to the 1986 goals) so that base widths would remain constant between poly contacted and control devices for better comparison. We successfully completed a 0.05 μm deep As emitter with a 0.1 μ base with device with peak beta of from 70 to 130.

(e) Successfully completed the polysilicon contacted devices and measured an average peak beta enhancement of a factor of 3,
$\frac{232.9}{77.7} = \frac{\text{B(poly)}}{\text{B(metal)}}$.

Goal #2. Transistor Evaluations

A test station was designed and assembled using a HP 4145A Semiconductor Parameter Test set with a reconditioned probing station. System automatically takes the I-V and beta vs. I_C data and loads into the UNIX ECN network for plotting etc. to compare with the simulation results. This system works very well and has been used to measure countless devices.

Goal #3. 2D Modeling of Delco Thin Epi

This goal required the modification of an existing two-dimensional simulation code for silicon solar cells to model Delco Electronics "thin epi" silicon bipolar transistors. This involved having the student research assistant familiarize himself with the code (over 10,000 lines of FORTRAN), and then make the necessary modifications. Most of the necessary modifications have been completed. Realistic diffusion profiles, obtained from SUPREM simulations, have been incorporated. In addition, measured or analytic (i.e. ERFC or gaussian) profiles can also be used. A method for accurately extracting the base, collector, and emitter currents has been developed and is now being implemented. Some preliminary two dimensional simulations of Delco's "thin epi" bipolar transistors have been completed.

Goal #4. 2D Models of Polysilicon Emitter Contacts

The necessary code for modeling the minority carrier reflecting properties of polysilicon contacts is already incorporated in the simulation program.

LIST OF FIGURES

I. Introduction

The fabrication of extremely small self-aligned emitter structures for bipolar transistors has been realized by using polysilicon in forming the emitter. Two types of emitters are possible. One has polysilicon as part of the very shallow N^+ emitter of the N^+PN bipolar transistor, i.e. a poly-contacted emitter. The other has the N^+ polysilicon acting as the emitter directly on the P base region, i.e. a true or pure polysilicon emitter. The grain size of the polysilicon and any SiO_2 layer at the polysilicon-emitter base interface will determine the beta of the transistor in an extremely sensitive manner.

The proposed research was to concentrate on investigating a new method of fabricating polysilicon contacted emitter bipolar transistors and pure poly emitter devices. The technique uses plasma etching the emitter location on the base region and, without breaking vacuum, depositing amorphous silicon (a-Si) on the cleaned interface. The a-Si will then be doped by ion-implantation and heated to 600-700 C° to produce the polysilicon emitter, or made polycrystalline and then doped. The controlled interface and the fine grained polysilicon should lead to more uniform and predictable betas for the transistors. Both polysilicon contacted emitters and polysilicon emitters are to be investigated over a range of base doping.

We are proposed to continue the modeling work by extending it in two directions: 1) 2-D simulation so that small geometry transistors can be accurately modeled and 2) simulation of polysilicon emitter transistors. Measurements on the devices described above will be used to develop a polysilicon model. The objective of this part of the project is to develop a numerical device simulator with predictive capability, i.e. one that can be used with confidence in place of actual device fabrication. The numerical device models will be provided to Delco and should find many applications in development and manufacturing.

II. The Proposed Research

A. Fabrication

Polysilicon contacted emitters have been reported to increase the current gain, β, at a given base charge, Q_B, or alternatively allow for a much higher base charge at a given β value [1]. The result is the base resistance can be lowered by doping the intrinsic base region heavier, without an overall loss in β. Polysilicon emitters offer an increase in β from 2 to 50 times that of conventional devices. Reproducible fabrication of such enhanced β devices is however still being impeded by the lack of a basic understanding of the physical mechanisms involved at the polysilicon/silicon interface.

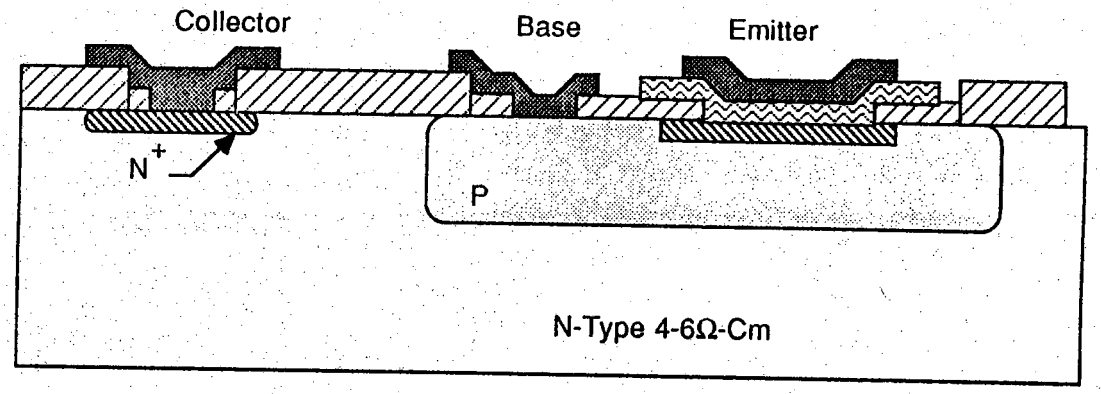
Two types of polysilicon emitter transistors have been identified as illustrated in Figure 1. The pure polysilicon emitter has an intentionally grown layer of SiO_2 (15 to 30 Å thick) at the interface between the polysilicon emitter and the base region [2]. This type of device leads to the largest beta enhancement but is the most unpredictable. The second type of device, the poly-contacted emitter, depends on keeping the interface as free of SiO_2 as possible [3]. In both cases the reduction of base hole current is achieved by reducing the number of holes being injected from the base region to the emitter (a N^+PN bipolar transistor). The reduced base current yields the β enhancement [4] by improving the emitter injection efficiency. It has been shown that in modern devices with very narrow base widths this base current component is the largest factor in determining beta.

The poly contacted emitter device has applications in very small, very fast digital VLSI devices where β enhancement is not too important but where the self aligned emitters are necessary to get extremely small size transistors and circuits. The self aligned emitter structure reduces the parasitics of the transistor and allows emitter widths of 0.35 micrometers. and have extremely shallow emitter junctions. Another possibility is to increase the base doping to reduce the intrinsic base resistance and speed-up the device without an effective loss in β from the regular transistor. Our work is to concentrate on the poly-contacted emitter. This requires a very shallow emitter and a narrow base width in order to see any beta enhancement.

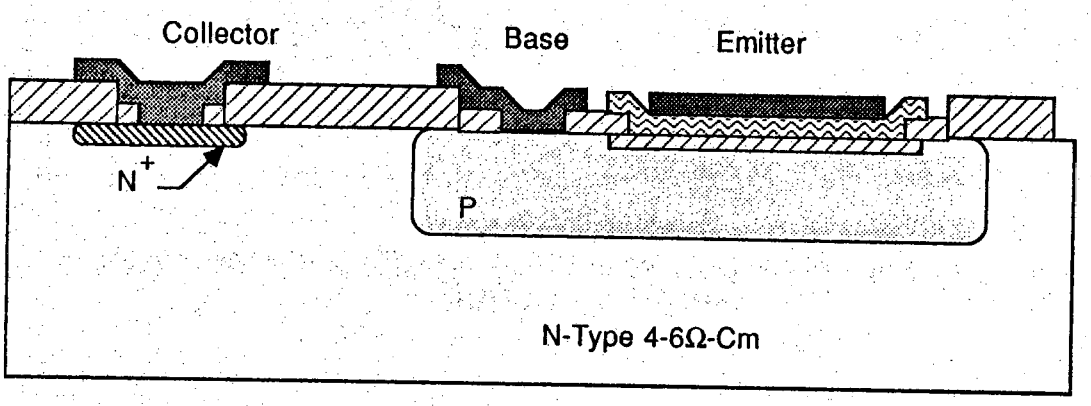
B. Computer Modeling.

Many of the important issues for modeling high performance silicon transistors are already being addressed here at Purdue University. With the experience gained from modeling silicon bipolar transistors in one dimension (under a previous contract with Delco Electronics) and in modeling high efficiency silicon solar cells, we have developed considerable confidence in the accuracy of the physical models used in the simulations.

Polysilicon Emitters



Poly-Contacted Emitter formed by N+ poly on top of a very Shallow As Emitter



Poly Emitter made by N+ poly and a very thin oxide interface between the Poly and P-silicon

Figure 1. Polysilicon Emitter and polysilicon contacted Emitter bipolar transistors.

In order to handle geometry-induced effects, a two-dimensional simulation code must be developed. A 2D code for the simulation of high efficiency silicon solar cells has already been developed and used extensively as an analytic and predictive tool. Modifying the code to handle transistor geometries is a relatively straight forward task. The necessary modifications include handling doubly diffused doping profiles, multiple contacts (as opposed to just two for solar cells), and an accurate method for extracting the terminal currents from the simulation results. Once these modifications are complete, modeling the DC characteristics of Delco's small geometry silicon bipolar transistors will be possible. It is expected that at this stage the code can be used as an analytic and predictive tool.

Further enhancements of the 2D transistor code which will increase the codes usefulness will also be addressed. These are a transient analysis option and a small signal, sinusoidal steady-state analysis option. These enhancements will make the extraction of important device parameters easier and more reliable.

The second phase of the proposed research, to develop such analytic and predictive models for polysilicon emitter transistors, will be considerably more challenging. Two approaches to this problem are proposed. First, for polysilicon contact transistors, the minority carrier reflecting properties of the polysilicon contact will be modeled by an effective surface recombination velocity. This capability already exists in the 2D solar cell code, and so is a logical first step. The second approach, which is considerably more difficult, will be to model the polysilicon as a separate material with its own set of physical characteristics, i.e. bandgap, mobility, lifetime, etc. For this approach, it will be necessary to develop an understanding of the transport properties of polysilicon.

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III. Summary of Work in 1986

A. Fabrication of Poly-contacted Emitters & Control Transistors

Preliminary Control (Substrate) and Polysilicon Devices:

Several standard and polysilicon fabrication runs were made to determine what problems may occur in modifying Purdue's standard bipolar process to accommodate the polysilicon contact to the base region and polysilicon emitter devices. Three types of devices were made; regular, polysilicon (with a thin oxide interface) and poly emitters (with little if any oxide at the interface). Once these results were evaluated a set of new photoplate masks and process modifications were designed. The process design was simulated by using the SUPREM III simulator while the test mask set was designed and laid out on our graphics system.

Table I lists the regular phosphorous doped emitter bipolar transistor parameters developed and fabricated in our laboratories. The emitter is 100 microns by 80 microns and the total base is 217 microns by 120 microns. It must be noted that these devices are not made with a buried layer and hence have large collector resistances. The emitter depth is 0.35 microns and the base width is 0.52 microns. Figures 2, 3, and 4 show its main electrical characteristics.

With the substrate device as a reference, several wafers were processed together through the base diffusion and drive steps. For the standard BJT, the collector contact and the emitter are implanted with phosphorous and diffused simultaneously. For the polysilicon devices the emitter window is not opened in the oxide for the implant, but the implant for the collector contact and drive are performed. As a result, the poly-emitter structure has a larger base width by the amount of the emitter diffusion. Suprem II simulations indicated the base widths are 0.46 micrometers and 0.73 micrometers. Therefore we could not expect as large a beta enhancement with the polysilicon emitters as would be the case if the base widths were the same.

The polysilicon was deposited after opening windows in the emitter of the poly-emitter devices and trying two types of surface treatment. For one set of wafers the windows were given a buffered HF (BHF) dip to remove as much of the native oxide as possible; the other given the RCA clean which will create a thin 15-20 Å SiO_2 layer. The polysilicon was deposited in the LPCVD tube at 620 ° C for 50 minutes and then doped in the phosphorous deposition tube for 20 min at 900 ° C.

The poly devices with the BHF will probably have a true oxide free interface and represent the case of some impurities diffusing from the poly to form a very shallow emitter or create the emitter-base junction at the surface of the single crystalline

Table I. Purdue Process #4 bipolar transistor measured parameters.

Parameters		Process #4 Wafer 11.ii Site 7 Trans DB
Peak Beta		230
Early Voltage		60V
I_{0L} at -4V	b/e	$2x10^{-8}$A
	b/c	$3x10^{-8}$A
I_{0D} at -4V	b/e	$2x10^{-12}$A
	b/c	$1x10^{-12}$A
V_{BR}	b/e	7.25V
	b/c	46V
Resistance Ω/□	emit	30
	base	1000
	base pinch	30,000

η	base-emitter	1.03
	base-collector	1.21
I_S	base-emitter	$3x10^{-15}$A
	base-collector	$8x10^{-14}$A
I_{0D}	b/e	$8x10^{-12}$A
	b/c	$9x10^{-11}$A
I_{0L}	b/e	$3x10^{-8}$A
	b/c	$5x10^{-8}$A
V_{BR}	base-emitter	7.25V
	base-collector	46V

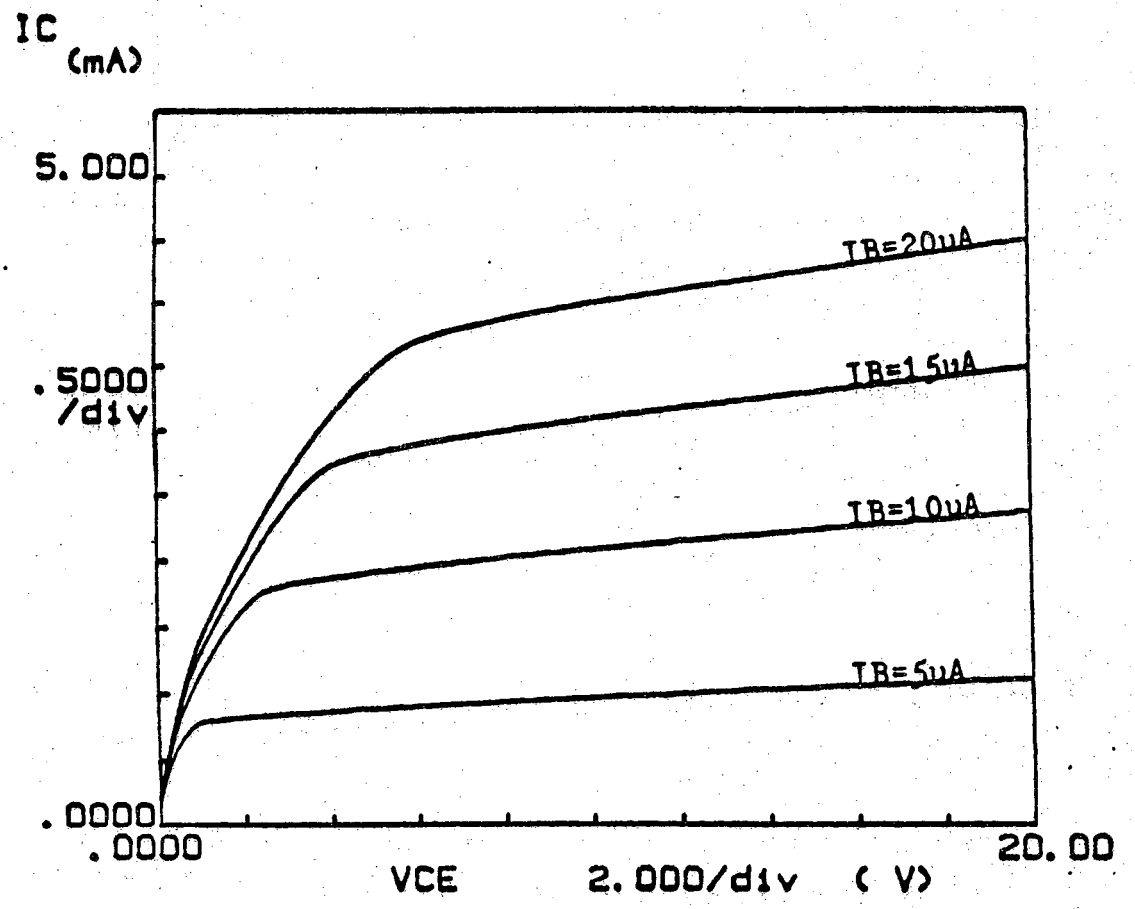


Figure 2. Transistor I-V curves measured on curve tracer. Process #4, wafer 11.ii, transistor 7 dB.

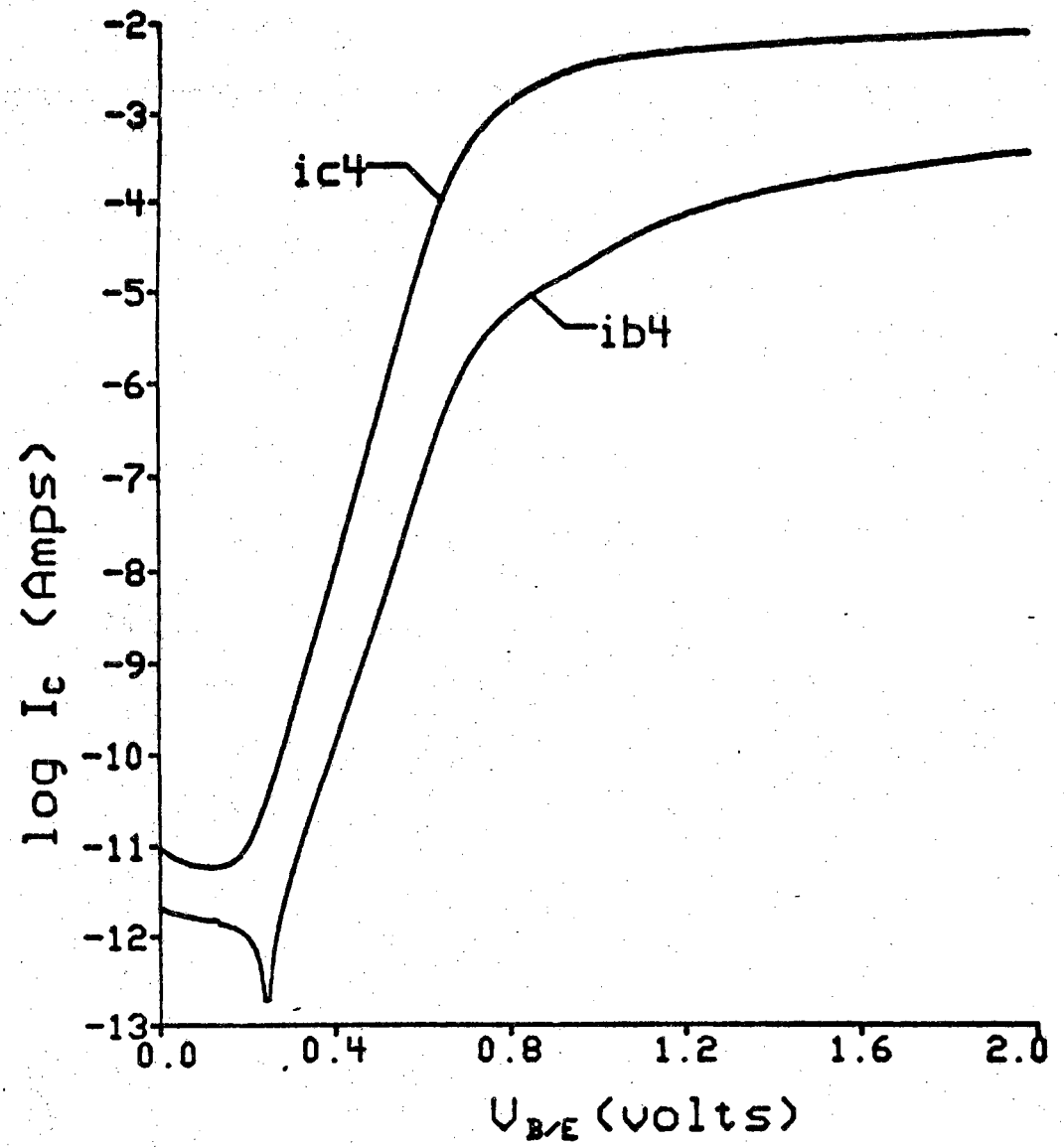


Figure 3. Base and collector currents vs. V_{BE} with $V_{CE} = 4V$. Process #4, wafer 11.ii, transistor 7 dB.

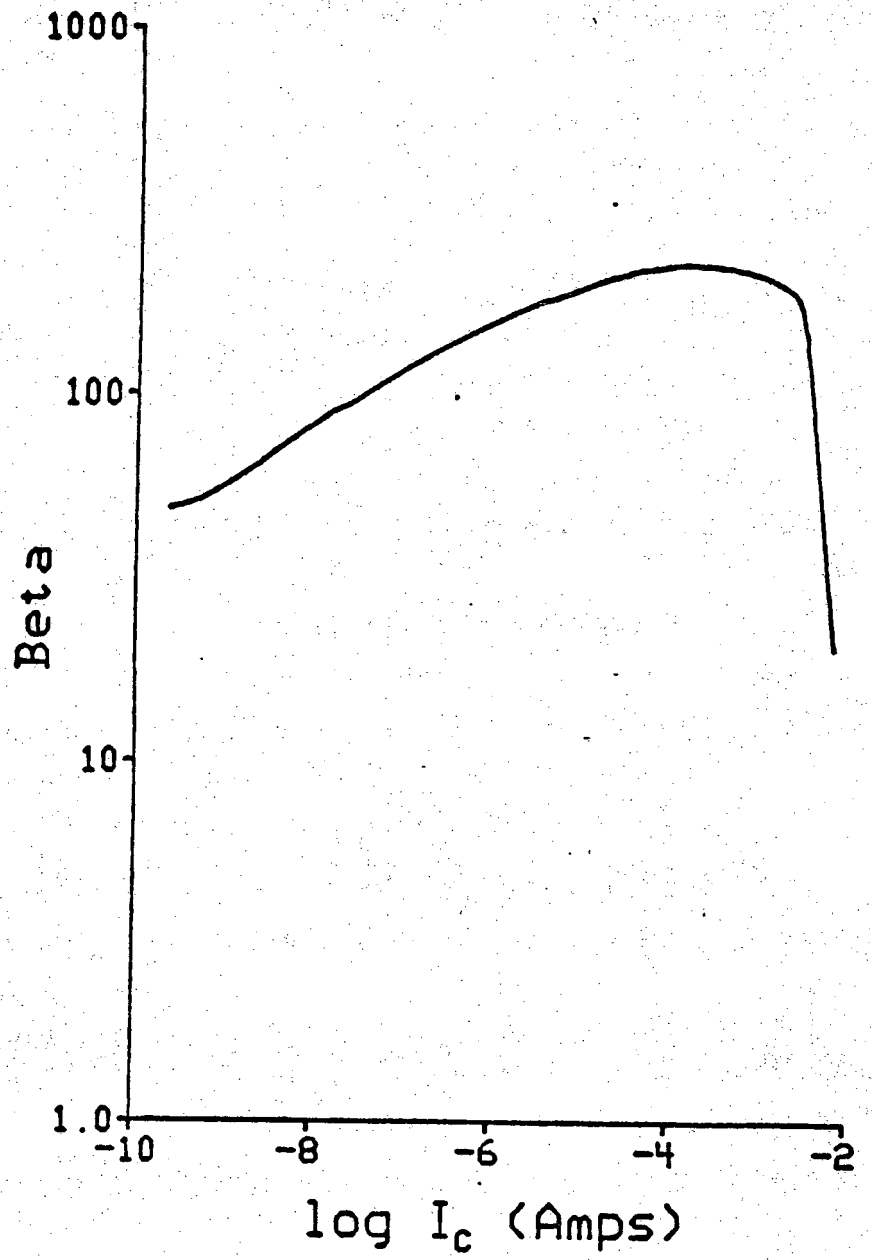


Figure 4. Beta vs. I_C. Process #4, wafer 11.ii, transistor 7 dB.

silicon base region. Those with the RCA clean surface treatment will have the oxide barrier to give a heterostructure to the emitter-base and hence a good hole blocking barrier to the base current. Hence the BHF type is expected to have a poor E-B junction (lots of generation-recombination centers) while the RCA type should have beta enhancement.

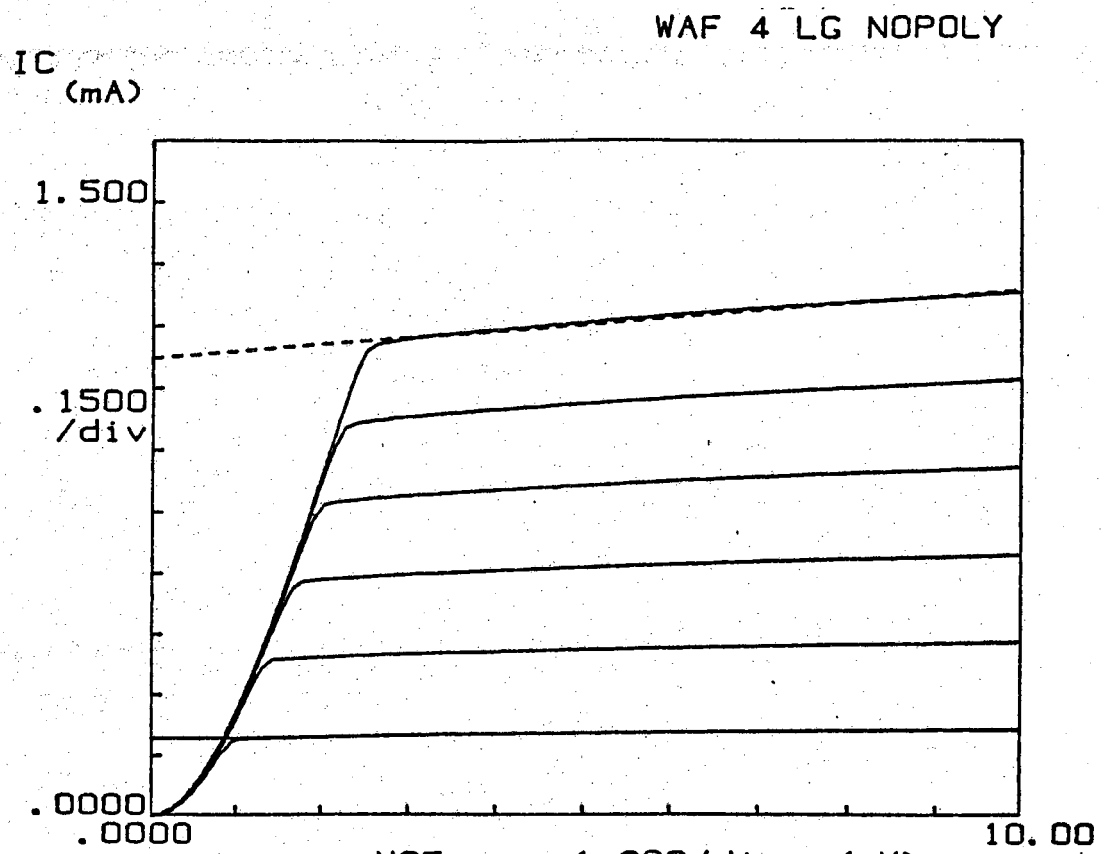
Table II shows the results of the fabrication runs after measuring the transistor characteristics with the HP 41245A Semiconductor Parameter Analyzer. In the table only the peak betas are recorded and averaged over the number of samples measured. The standard or control BJT has the betas in the range expected from our standard process. Typically they have an Early voltage of about 68 to 74 volts. For the poly emitter device with the BHF dip the betas are much smaller due to the larger base width and the interface region. Our SUPREM II simulations show that the impurity level at the polysilicon/silicon interface is small, which also reduces the beta. The RCA clean device has a maximum beta enhancement of greater than 3 and an average of 2.66. It is actually greater than that because the base width of the poly device is greater than the standard BJT. Figures 5 through 7 illustrate some of the I-V data taken on the devices.

Test Wafer Mask Design

The preliminary results were quite encouraging and gave us several insights into how to design a better fabrication process (to include poly-contacted emitter devices) and to layout a group of test structures and transistors. Four types of transistors were designed, each with a range of emitter sizes formed into an array. The emitter sizes are 18 X 18, 28 X 28, and 36 X 36 microns square. Forty eight devices of each type and size device are available. For example 48 control (substrate) devices with 18 X18 micron square devices are on each wafer. The other 3 types of devices are a polysilicon emitter (em), a poly-contacted emitter completely inside the shallow emitter (1con), and a poly-contacted emitter overlapping the shallow emitter (2con). Figure 8 illustrates the 4 device structures.

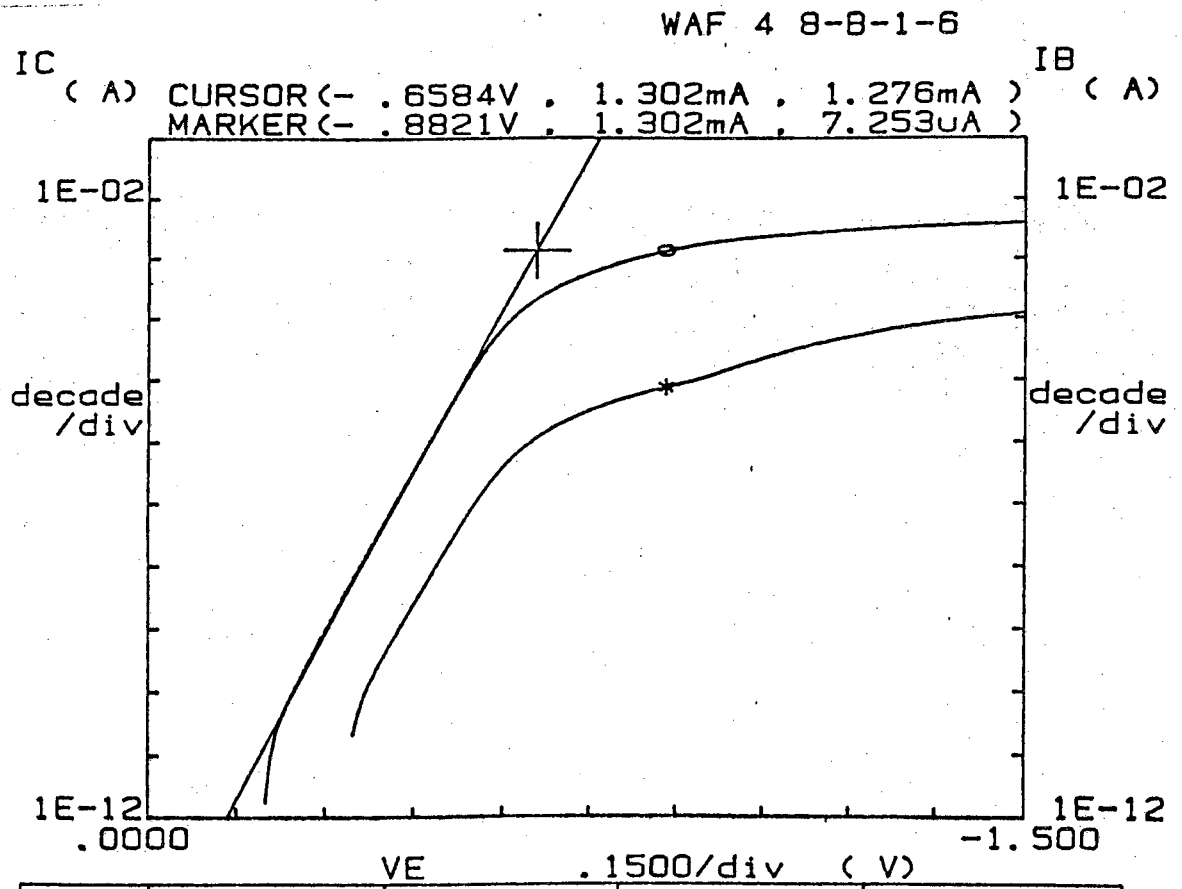
Table II. Preliminary Polysilicon Emitter Beta data.

Device	#	Beta max.	Beta min.	Beta average
Control BJT	6	206	175	191.5
RCA Poly	2	635	386	510.5
BHF Poly	11	60.4	4.2	18.55



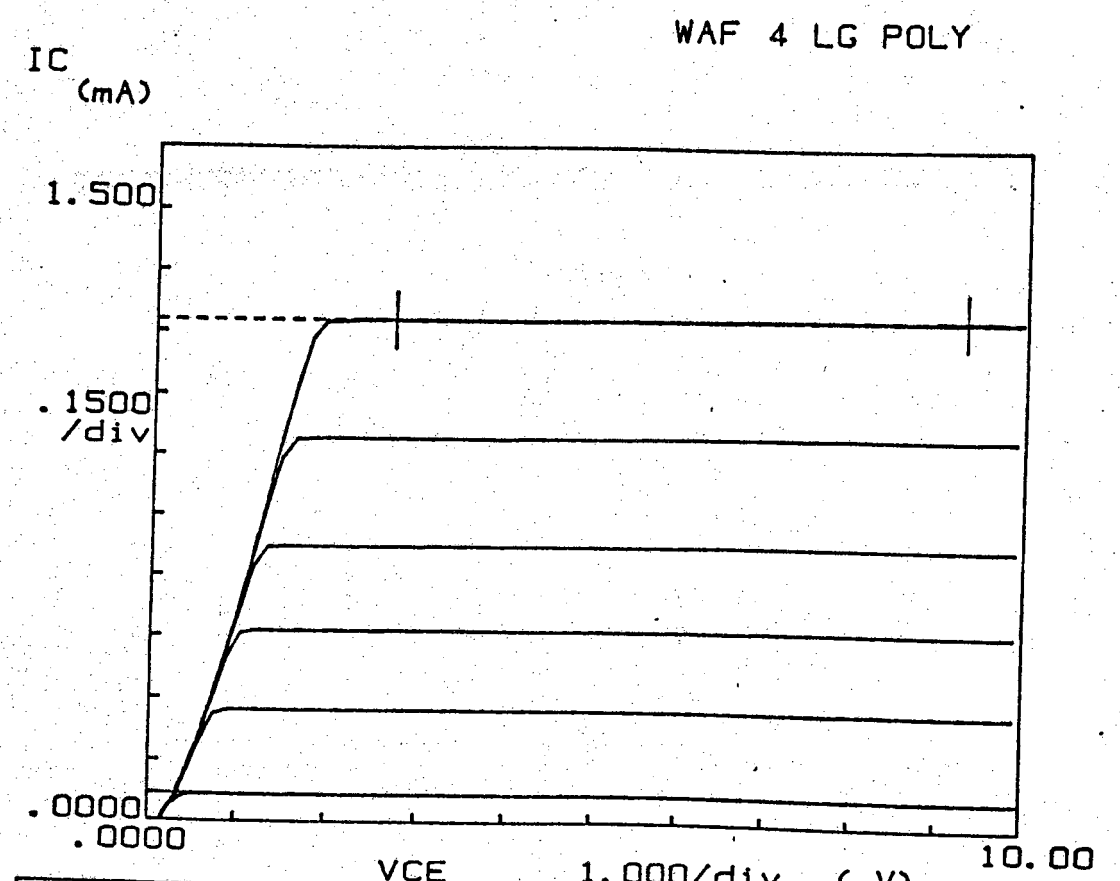
	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	2.60E-06	385E+03	-74.2E+00	193E-06
LINE2	16.5E-06	60.7E+03	-68.2E+00	1.12E-03

Figure 5. Control BJT I_C vs. V_{CE}



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	-17.3E+00	-57.7E-03	-825E-03	4.99E-15
LINE2				

Figure 6. Control BJT I_B, I_C vs. V_{BE}



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	100E-09	9.98E+06	-672E+00	67.4E-06
LINE2	1.07E-06	938E+03	-1.15E+03	1.23E-03

Figure 7. BHF dip Poly Emitter, I_c vs V_{CE}

Figure 7. BHF dip Poly Emitter, I_C vs. V_{CE}

The test die is shown in Figure 9. Note that it is symmetrical in four quadrants with alignment marks and resolution keys in each. Several large devices of each type have also been included with very large emitters, 576 X 576 microns. The remaining test transistors are 1024 18 X 18 micron emitters in parallel. A section to evaluate the fabrication process parameters is the nearly square section of Figure 10. Sheet resistance, conductance resistance, resistors, four point measurements, etc. have been included. The large features on the outside of the die are for the spreading resistance probe measurements, one for each step of the process.

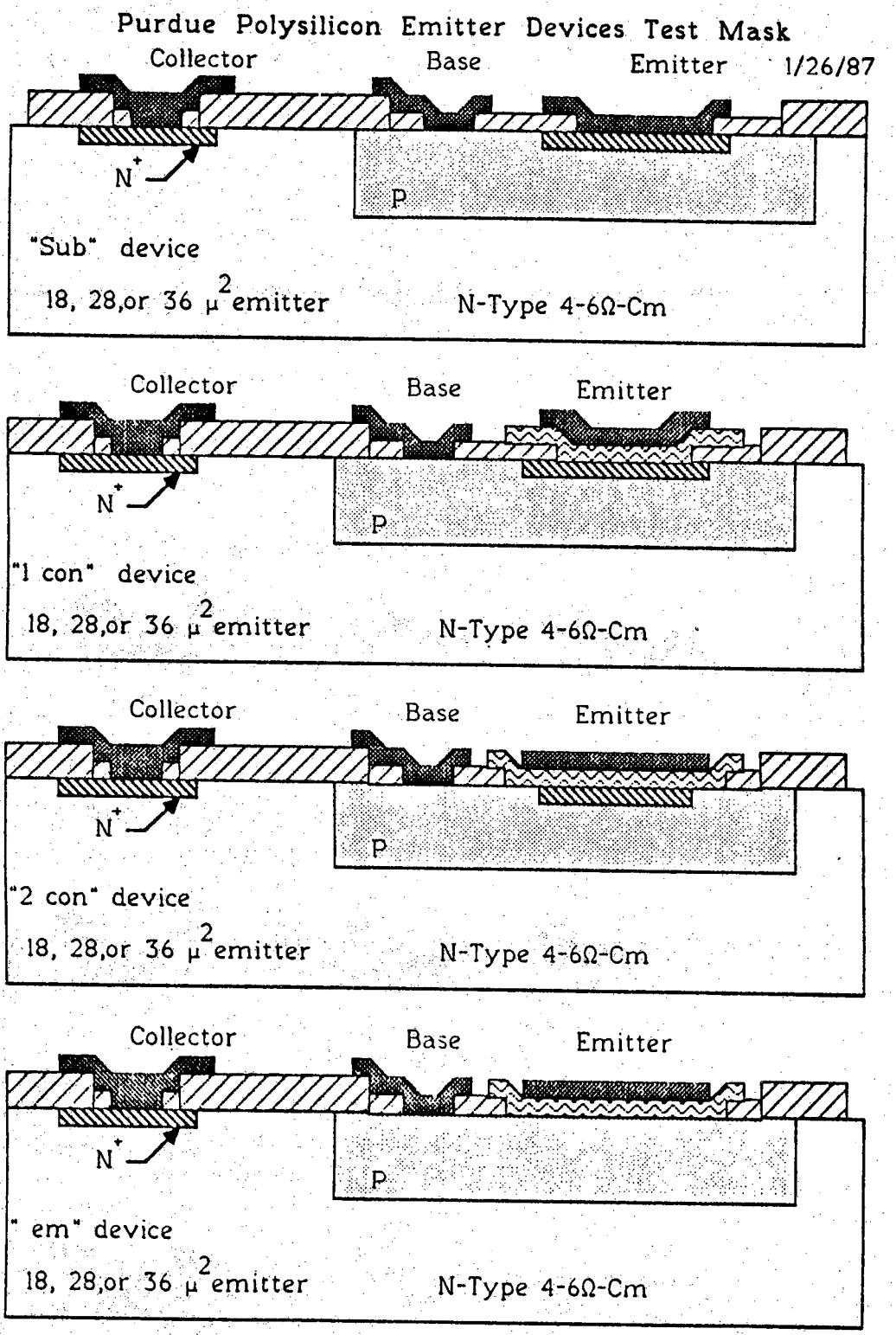


Figure 8. 4 Types of Devices on Test Mask

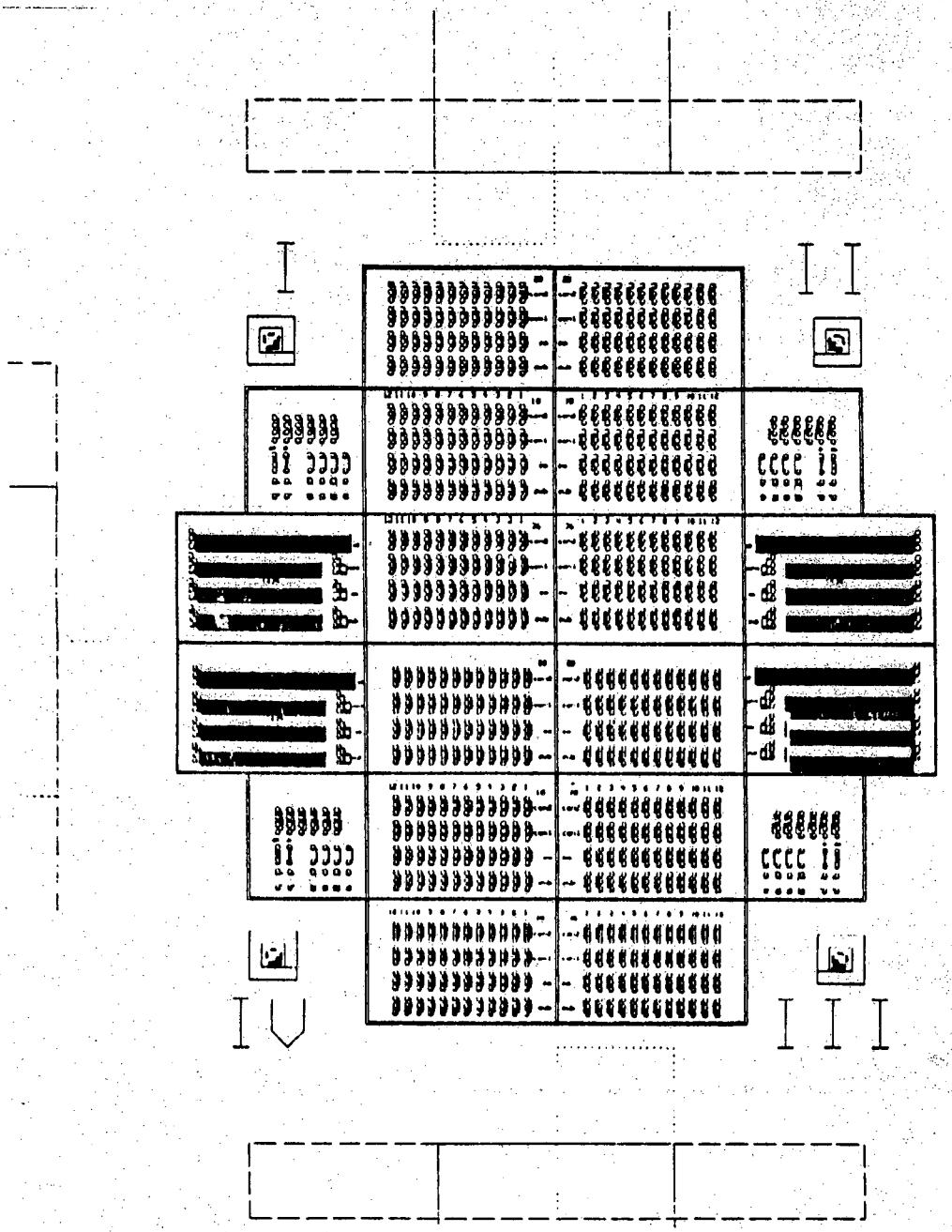


Figure 9. Test Wafer Layout, Full die.

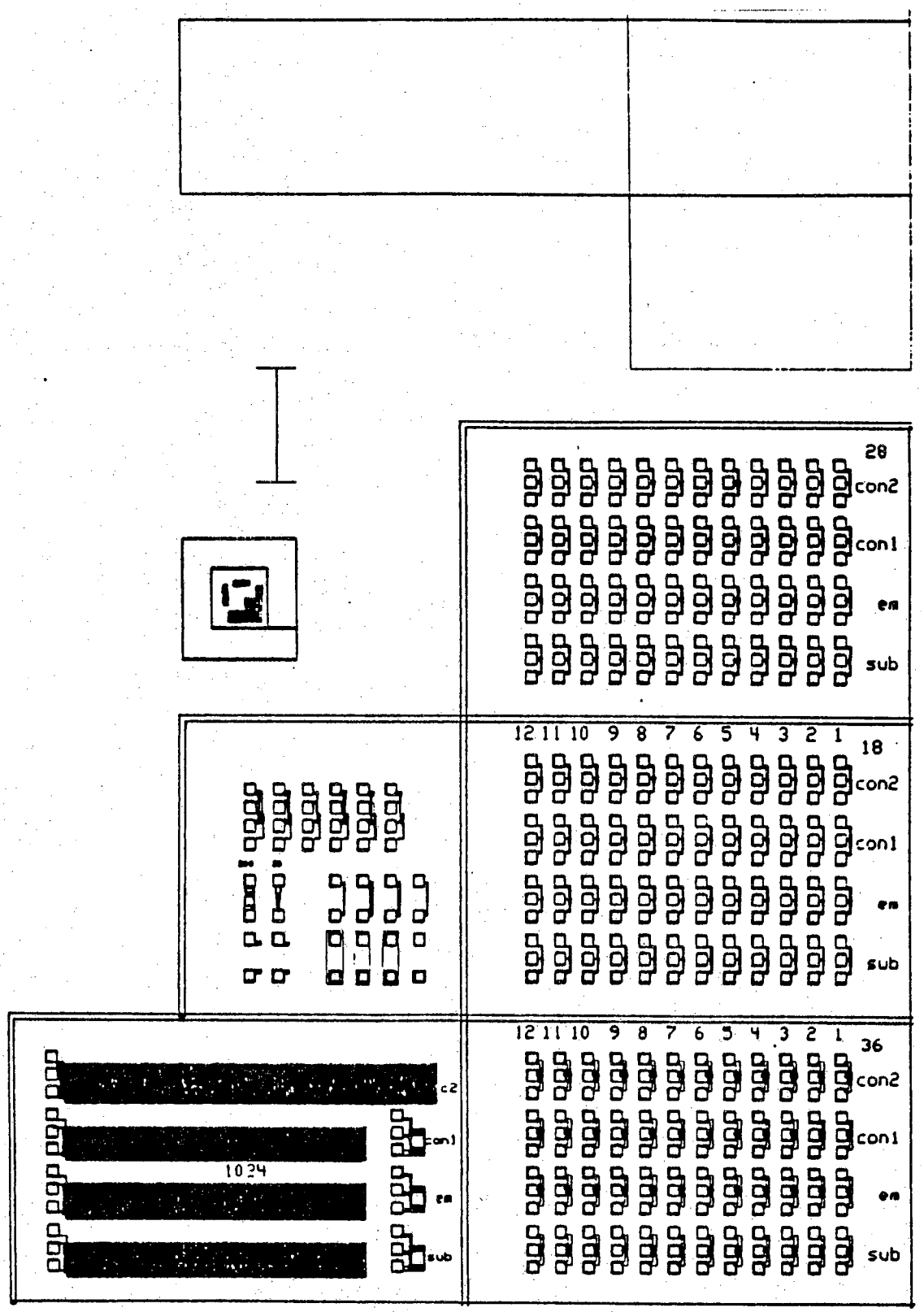


Figure 10. Quadrant I of test die.

Fabrication Runs "E" through "U"

The test die mask set was completed and verified before additional fabrication runs were attempted. The first goal was to establish the control (sub) transistors with the new mask set and with a slightly modified fabrication process. Figure 11 shows the basic process parameters for wafer set "E" with the measured beta for the "sub" devices of about 200. Note the two Boron implants in the base region and this was a phosphorous doped emitter. To further develop the process we attempted to make poly-contacted emitter devices along with the control devices in wafer set "F" as shown in Figure 12. Here the amorphous silicon was deposited by sputtering in the Ion Mill. The betas ranged from 20 to 200.

The requirement that the emitter depth be shallow in order to see the effects (improvement) with a poly-contacted emitter and to compare betas more equally with the control device base width, we attempted to make the emitter much shallower. Wafer set "G" of Figure 13 is the result. Note that again the betas are about 200 and the base width, from SUPREM II, is about 0.5 microns.

Set E - 4 2'' Wafers
Clean Test (solvents/BHF dip)

30 min. 1000° H_2 Burn Oxidation
Boron Implant, $3\times10^{13}/cm^2$ @ 140 KeV
Boron Implant, $4\times10^{13}/cm^2$ @ 35 KeV
20 min. 1050° H_2 Burn Oxidation
Phos. Implant, $7\times10^{15}/cm^2$ @ 80 KeV
20 min. 900° H_2 Burn Oxidation

$\beta \simeq 200$

Suprem II

	Junction Depth	Resistivity
E/B	.34μ	39$\Omega/\square$
B/C	.86μ	3.5k$\Omega/\square$

Figure 11. Wafer set E

Set F - 8 2′′ Wafers
Phos. Process Development

30 min. 1000° H_2 Burn Oxidation
Boron Implant, (varied)
20 min. 1050° H_2 Burn Oxidation
or 15 min. 1050° H_2 Burn Oxidation
Phos. Implant, $6 \times 10^{15}/cm^2$ @ 50 KeV
20 min. 900° H_2 Burn Oxidation
α-Si Deposition (Ion Mill)

β = 20 to 200

Figure 12. Wafer set F with phosphorous emitters

Set G - 3 2′′ Wafers
Deep As Emitter Process

30 min. 1000° H_2 Burn Oxidation
Boron Implant, $1\times10^{14}/cm^2$ @ 35 KeV
15 min. 1050° H_2 Burn Oxidation
30 min. 1050° Dry Oxidation
As Implant, $1\times10^{16}/cm^2$ @ 50 KeV
10 min. 1000° H_2 Burn Oxidation

$\beta \simeq 200$

Suprem II

	Junction Depth	Resistivity
E/B	.15μ	60$\Omega/\square$
B/C	.67μ	2.5k$\Omega/\square$

Figure 13. Wafer set G with a deep As Emitter

Set H - 8 2'' Wafers
Deep As Emitter Process Development

30 min. 1000° H_2 Burn Oxidation
Boron Implant, $3\times10^{13}/cm^2$ @ 140 KeV
Boron Implant, $4\times10^{13}/cm^2$ @ 35 KeV
25 min. 1000° H_2 Burn Oxidation
As Implant, $3\times10^{15}/cm^2$ @ 35 KeV
15 min. 1000° H_2 Burn Oxidation

$\beta \simeq 10$ to 15

Suprem II

	Junction Depth	Resistivity
E/B	.14μ	70$\Omega/\square$
B/C	.68μ	1.4k$\Omega/\square$

Figure 14. Wafer Set H, deep As emitter

Set I - 12 2'' Wafers
Deep As Emitter Process Development

30 min. 1000° H_2 Burn Oxidation
Boron Implant, $1-4\times10^{13}/cm^2$ @ 25-80 KeV
As Implant, $3-10\times10^{15}/cm^2$ @ 35 KeV
10 min. 1000° H_2 Burn Oxidation

$$\beta < 1$$

Suprem II

	Junction Depth	Resistivity
E/B	.02-.16μ	45-6800$\Omega/\square$
B/C	.3-.6μ	2.5-15k$\Omega/\square$

Figure 15. Wafer Set I

Set J - 8, 2" Wafers

Shallow As Emitter with Poly Contact

30 min. 1000° H_2 Burn Oxidation
Define Base Regions
10 min. 900° H_2 Burn Oxidation
Boron Implant, $1\times10^{13}/cm^2$ @ 35 Kev
Define Emitter Regions
10 min. 900° H_2 Burn Oxidation
As Implant, 6×10^{15} @ 35 Kev
10 min. 1000° H_2 Burn Oxidation
Define Poly Windows
RCA Clean
Poly deposition, 24min. @ 620° (.1 to .3μ)
As Implant, 1×10^{13}-10^{16} @ 35 Kev
Define Polysilicon
Metallization(Ion Mill), 25min. Al-Si-Cu

$\beta\sim$60 to 90

Figure 16. Wafer Set J, Shallow As Emitter

Set K

4, 2" Wafers, and 4 quarters of 1, 4" Wafer

Shallow As Emitter with Poly Contact

20 min. 1000° H_2 Burn Oxidation
Define Base Regions
10 min. 900° H_2 Burn Oxidation
Boron Implant, $1\times10^{13}/cm^2$ @ 35 Kev
Define Emitter Regions
10 min. 900° H_2 Burn Oxidation
As Implant, 6×10^{15} @ 25-35 Kev
10 min. 1000° H_2 Burn Oxidation
Define Poly Windows
RCA Clean
Poly deposition, 24min. @ 620° (.1 to .3μ)
As Implant, 1×10^{16} @ 35 Kev
Define Polysilicon
Metallization(Ion Mill), 30min. Al-Si-Cu

$\beta\simeq$100 to 170 (Tested in Package)

Figure 17. Shallow As emitter and a poly-contact

Set L - 4 quarters of 1, 4" Wafer

Shallow As Emitter with Poly Contact Annealed

20 min. 1000° H_2 Burn Oxidation
Define Base Regions
10 min. 900° H_2 Burn Oxidation
Boron Implant, $1\times10^{13}/cm^2$ @ 35 Kev
Define Emitter Regions
10 min. 900° H_2 Burn Oxidation
As Implant, 6×10^{15} @ 35 Kev
10 min. 1000° H_2 Burn Oxidation
Define Poly Windows
RCA Clean
Poly deposition, 6min. @ 620° (.1 to .3μ)
As Implant, 6×10^{15} @ 35 Kev
N_2 Anneal, 10min. @ 900-1000°
Define Polysilicon
Metallization(Ion Mill), 30min. Al-Si-Cu

Bad Contacts

Figure 18. Wafer set L shallow As emitter with poly contact anneals

Set M - 8 quarters of 2, 4" Wafers

Shallow As Emitter with Poly Contact Annealed

20 min. 1000° H_2 Burn Oxidation
Define Base Regions
10 min. 900° H_2 Burn Oxidation
Boron Implant, $1\times10^{13}/cm^2$ @ 35 Kev
Define Emitter Regions
10 min. 900° H_2 Burn Oxidation
As Implant, 6×10^{15} @ 35 Kev
10 min. 1000° H_2 Burn Oxidation
Define Poly Windows (#2-5,7,8)
RCA Clean (#2-4), BHF etch (#5,7,8)
Poly deposition, 9min. @ 620° (.1 to .3μ)
As Implant, 6×10^{15} @ 35 Kev
N_2 Anneal, 10-60min. @ 800-900°
Define Polysilicon
Define Contacts (#1-8)
Metallization(Ion Mill), 30min. Al-Si-Cu

$\beta = 20$ to 40

Figure 19. Wafer set M, shallow As emitter with poly-contact anneals

The next set of devices were designed to have Arsenic doped emitters for a shallower emitter depth. The diffusion of the emitter Arsenic impurities would be much slower than that of phosphorous. Wafer set H,I,J,K,L, and M are the result of these attempts. Another thing to notice is that the wafer sets J,K,L, and M were cleaned with the RCA cleaning method after their polysilicon window openings are defined. Here the amorphous silicon was deposited in a LPCVD tube and annealed to become polysilicon. Wafer sets "H" and "I" are just attempts to make control devices with As emitters for a shallow emitter depth. The effects of various implant energy, dose, and drive-in temperatures were investigated. The Figure 14 and Figure 15 show process parameters and the measured beta for wafer set "H and "I".

In wafer set "J", the As implant into the polysilicon was performed with various implant doses to investigate this effect. The poly-contact devices of wafer set "J" showed a beta of less than that of the control device. Figure 16 shows the process parameters for wafer set "J" with the measured beta values, which ranged from 60 to 90.

Up to wafer set "J", only 2" wafers were used for making devices. From wafer set "K", 4 inch wafers were often used after being cut into 4 quarters. Wafer set "K" had some variations in As implant energy to make shallower emitter depths. As shown in Figure 17, wafer set "K" had good control BJT's but the poly-contacted emitter had less gain, with the poly-emitter having no gain at all. They were tested after being bonded and packaged.

In wafer set "L, only 4 quarters of a 4" wafer were used and annealing of the polysilicon, after being implanted with As, was performed under different conditions to see the differences. The process parameters are in Figure 18. Wafer set "L" had bad contacts due to too thick an oxide in the window which was not completely etched.

In wafer set "M", part of wafers were cleaned using the RCA cleaning method, and the others were etched with BHF after the polysilicon windows were defined. Also the annealing of polysilicon, after implanted with As, was performed at different temperatures for various time periods. The beta values ranged from 20 to 40 as shown in Figure 19. Wafer set "M" was processed and parts of several wafers were sent to Delco for spreading resistance profiles. The results were somewhat inconclusive as to where the junctions were located due to not having a thick oxide.

The test results from the above fabrication runs indicated that we should consider "gettering" as part of the process to reduce the leakage currents and the generation-recombination in the junctions. Additional wafer fabrication sets M,N,O,P,Q, and R have been processed in an attempt to analyze the problem with the As doped emitter fabrication process. Up to wafer set "R", it appeared that we might have a contamination problem in the oxidation furnaces and with the metallization for the contacts. The metallization was solved by going from an evaporator system to a clean sputtering system for the aluminum. Previously we had used an Al-Si-Cu target in the Ion Mill but it degraded for some unknown reason.

In wafer set "N", different gettering methods were performed for comparison; i.e. polysilicon gettering, phosphorous gettering, or both. They were done by depositing those materials on the back of the wafers.

Set N - 4 quarters of 1, 4" Wafer

Gettering, Pd/Al Contacts

30 min. 1000° H_2 Burn Oxidation

#2,4 : Poly deposition(back), 40min. @ 660° ($\simeq 1\mu$)

#3,4 : Phosphorus deposition(back), 30min. @ 1000°

Drive-in, 30min. @ 1000°

20min. 1000° H_2 Burn Oxidation

Define Base Regions

10 min. 900° H_2 Burn Oxidation

Boron Implant, $1\times10^{13}/cm^2$ @ 35 Kev

Define Emitter Regions

10 min. 900° H_2 Burn Oxidation

As Implant, 6×10^{15} @ 35 Kev

10 min. 1000° H_2 Burn Oxidation

Define Contacts (#1-4)

Metallization (Ion Mill), Sputter Pd/Al

Pd : 10min. @ 15mA

Al : 20min. @ 20mA

Figure 20. Wafer set N, Pd/Al Contacts

Set O - 4 quarters of a 4" Wafer

Contacts

30 min. 1000° H_2 Burn Oxidation
Mask Back, Etch Front
Define Contacts
Metallization (Ion Mill)
- #1 : 10min. etch, 30min. coat Al-Si-Cu
- #2 : 30min. coat Al-Si-Cu
- #3 : 10min. etch, 10min. Pd, 30min. Al
- #4 : 10min. Pd coat, 30min. Al coat

Breakdown Voltages		
#	No Anneal	600° Anneal
O1	13V	13V
O2	11-12V	0-6V
O3	2-3V	0-4V
O4	0-1V	0-4V

Figure 21. Wafer set "O".

Set P - 4 quarters of a 4" Wafer

Shallow As Emitter with Different Contact Methods

No RCA Clean

Poly Getter (back)

40 min. 1000° H_2 Burn Oxidation

Poly Deposition, 10 min. @ 660°

20 min. 1000° H_2 Burn Oxidation

Define Base Regions

15-25 min. @ 900-1000° Dry Oxidation

Boron Implant, $1 \times 10^{13}/cm^2$ @ 35 Kev

Define Emitter Regions

10 min. 900° H_2 Burn Oxidation (#1,3)

25 min. 1000° Dry Oxidation (#2,4)

As Implant, 6×10^{15} @ 35 Kev

10 min. 1000° H_2 Burn Oxidation

Define Poly Windows

RCA Clean, BHF etch

Poly deposition, 9min. @ 620° (.1 to .3μ)

As Implant, 6×10^{15} @ 35 Kev

N_2 Anneal, 60min. @ 700°

Define Polysilicon

Define Contacts

Metallization(Perkin-Elmer), RF sputter Al

$\beta = 0$ to 300

Some Good Contacts, Still Bad Leakage

Figure 22. Wafer Set P, As Emitter with Various, Contacts Metal.

Set Q - 4, 2" Wafers

Boron P/N Diode

Poly Getter-Back (#2)

30 min. 1000° H_2 Burn Oxidation

Poly Deposition, 40 min. @ 660°

30 min. 1000° H_2 Burn Oxidation

BHF etch

As Implant-Back, $5\times10^{15}/cm^2$ @ 35 Kev

10 min. 900° H_2 Burn Oxidation

Boron Implant - Front

#1.2 : $3\times10^{13}/cm^2$, @ 140 Kev

$4\times10^{13}/cm^2$, @ 35 Kev

#3 : $1\times10^{13}/cm^2$, @ 35 Kev

#4 : $7\times10^{12}/cm^2$, @ 25 Kev

25 min. 1000° Wet Oxidation (#1,2)

20 min. 1000° Dry, 10 min. 1000° wet Oxidation (#3,4)

Define Contacts

Metallization(Perkin-Elmer), RF sputter Al 30 min.

#1 : N/P Junction? Front Contact $V_{BR}\simeq4V$, Forward O.K.

#2 : P/N Junction? Front Contact $V_{BR}\simeq4V$, Forward O.K.

#3 : P/N, Base - Back $V_{BR} > 4.0$, Forward Bad Junction?

Base - Collector $V_{BR} > 10$, Forward - High Resistance?

#4 : P/N Best Junctions - Back Contacts

Figure 23. Wafer Set Q, P-N Diodes

Set R - 4, 2" Wafers

Shallow As Emitter Process Development

25 min. 1000° H_2 Burn Oxidation

Define Base Regions

Boron Implant, $2\times10^{13}/cm^2$ @ 25 Kev

10 min. 1000° H_2 Burn Oxidation

Define Emitter Regions

As Implant, 1×10^{15} @ 25 Kev

10 min. 900-1100° H_2 Burn Oxidation

Define Contacts

Metallization(P-E), RF sputter Al, 25 min.

Al - not Annealed

Some Good/Bad Contacts

Figure 24. Wafer Set R, Shallow As Emitters

Set S - 4, 2" Wafers

Shallow As Emitter with Different Getterings

Poly Getter (back) - #1

30 min. 1000° H_2 Burn Oxidation

Poly Deposition, 80 min. @ 620°

Intrinsic Gettering - #2

30 min. 1000° H_2 Burn Oxidation

N_2 Anneal, 2-3 days @ 600°

BHF etch (front) - #1,2

30 min. 1000° H_2 Burn Oxidation

Define Base Regions

Boron Implant, $2\times10^{13}/cm^2$ @ 25 Kev

10 min. 1000° H_2 Burn Oxidation

Define Emitter Regions, $1\times10^{15}/cm^2$ @ 25 Kev

Define Contacts

Metallization(Perkin-Elmer), RF sputter Al

#1,2 : 15 min. Presputter, 5 min. Etch

12 min. Sputter, Lift-off

Contacts still bad, $\beta = 150$ to 100

#3,4 : 3 min. Etch, 30 min. Presputter and Sputter

Lift-off(#3), Wet etch Al(#4)

Contacts still bad, $\beta \simeq 20$

Figure 25. Wafer Set S; Gettering

Also, the metallization process was changed in this wafer set from Al-Si-Cu sputtering to Pd/Al sputtering with the hope of preventing Al spiking into the silicon. The change in metallization did not cure of the contact problem.

In wafer set "O", only metallization methods were investigated. Combination of etching and coating of Al-Si-Cu and Pd/Al was applied to the contact area, even for different time periods to figure out the best way for metallization. The process steps and data are shown in Figure 21.

The polysilicon gettering seemed to work consistently better than the phosphorous gettering and it does not cause problems in contaminating the furnace tubes as comparing to phosphorous gettering. Therefore, only polysilicon gettering was applied to wafer set "P". Another large change was that metallization was performed in Perkin-Elmer RF sputtering system instead of in the Ion Mill starting with wafer set "P". With the new metallization system, some devices showed good contacts, but there was still large leakage currents. The bad leakage currents may have come from pure Al sputtering and that it was removed when we used an Al-Si target. Boron (or As) implants were performed through very thin oxides so that we can obtain a narrow base width and a shallow emitter junction with reasonable value of implant energies. The betas of the "sub" devices ranged from 0 to 300 as shown in Figure 22.

Boron P/N diodes were made in wafer set "Q" with several variations of gettering, boron implant dose and energy, and drive-in times and temperatures. We measured P/N junction breakdown voltages and contact resistance. The results are shown in Figure 23.

Wafer set "R" shows another As emitter process development. Boron/As implant was performed after BHF etch of the base/emitter regions. Implant energy became almost the lower limit of the implanter (25 Kev) to make a narrow base width and a shallow emitter junction. Metallization was done by sputtering Al in the Perkin-Elmer, and the Al was not annealed. There were still some bad contacts.

Up to wafer set "R", bad contacts and high leakage current were the main trouble. Dislocations and stacking fault experiments were performed to determine the quality of both the 2" and the 4" wafers. This method is explained in a later chapter. It was found that quarters of 4" wafers had many more dislocations or stacking faults than 2" wafers. The method used to cut 4" wafers into 4 quarters generated large stress on the cutting edge and that turned out to be the main

cause for dislocations or stacking faults to occur. Therefore, from wafer set "R", 2" wafers were mainly used for the processing.

In order to reduce the junction leakage current in wafer set "S", both polysilicon and intrinsic gettering were applied. And for the contact problem, 8 different metalization techniques, which includes presputtering, etching, and Al sputtering, were used. The contacts were still bad, but some devices showed fairly good betas with ranges from 100 to 150. They are shown in Figure 25.

Some wafers had polysilicon gettering and some had oxide gettering on wafer set "T". The RCA cleaning method was used for all the wafers after the As implant. The metallization step included pre-etching of the target. Most devices showed poor quality base-emitter junctions as shown in Figure 26.

Set T - 8, 2" Wafers

Shallow As Emitter with Different Getterings

All Wafers Cleaned with RCA Clean

2 Wafers : Poly Gettering, 60 min. @ 620°

2 Wafers : Oxide Gettering, 2 days @ 600°

25 min. 1000° H_2 Burn Oxidation

Define Base Regions

Boron Implant, $2\times10^{13}/cm^2$ @ 25 Kev (#1-7)

$3\times10^{13}/cm^2$ @ 25 Kev (#8)

5 min. 1000° N_2 Anneal (#2-7)

Define Emitter Regions

As Implant, $1\times10^{15}/cm^2$ @ 25 Kev (#1-4,6,8)

$6\times10^{14}/cm^2$ @ 25 Kev (#5)

RCA Clean

10 min. 550° N_2 Anneal (#4-8)

10 min. 1000° N_2 Anneal (#3-8)

10 min. 1000° H_2 Burn Oxidation

Define Contacts

Metallization(Perkin-Elmer), RF sputter Al

Etch Wafer, Preetch Target, Coat Al 30 min.

Little or No Base-Emitter Junction

Probably Etched Emitter off before Al Deposition

Figure 26. Wafer Set T, gettering study.

Set U

6, 2" Wafers and 2 quarters of a 4" Wafer

Shallow As Emitter Process Development

Al-Si & Annealed Contacts

#6 : BHF Etch, RCA Clean

#1-8 : 30 min. 1000° H_2 Burn Oxidation

#1-4 : Phosphorus Deposition, 15 min. 1000°

Phosphorus Drive, 15 min. 1000° Dry Oxid.

#1-4,5,8 : Poly Deposition, 80 min. 620°

25 min. 1000° H_2 Burn Oxidation

Define Base Regions

Boron Implant, 2-5$\times 10^{15}/cm^2$ @ 25 Kev

#6 : Clean, BHF Dip, RCA Clean

10 min. 1000° H_2 Burn Oxidation)

Define Emitter Regions

As Implant, $1\times 10^{15}/cm^2$ @ 25 Kev (#1-4,6,8)

#6 : RCA Clean, 10 min. 1000° H^2 Burn Oxidation

Define Contacts

Metallization(P-E), RF sputter Al-Si 40 min.

N^2 Anneal @ 500° → Spiking

N^2 Anneal @ 400° → Good Contacts

Figure 27a. Wafer Set U.

From wafer set "U" on, the metallization was done with an Al-Si target instead of a pure Al target. Control devices with different getterings (polysilicon gettering and phosphorous gettering) and changes in the boron implant were fabricated. Also, the RCA cleaning method was used in one wafer. Metallization was done with an Al-Si target, and the devices were annealed at various temperatures. A 400 C° anneal in a nitrogen ambient made good contacts and 500 C° annealing caused spiking to occur. Some results are tabulated in Figure 27a.

Wafer Set V

In wafer set "V", all the devices had polysilicon gettering. Boron and As implants were done without any intentional oxide and the implant energy applied was 25 Kev for both materials. The control transistors had a very shallow emitter, reasonable leakage currents, good ideality factors, and betas ranging from of 50 to 70. In polysilicon emitter contact transistors, the As dose level implanted into the polysilicon and the temperature for annealing polysilicon had a large effect on the current gain. In wafer set "V3", we had good control (sub)transistors and polysilicon contact transistors (1 con). The next step will be to change the base doping and observe the difference in current gain for both types of devices.

Set V - 26, 2" Wafers (#0-25)

Shallow As Emitter With Poly Contacts

#1-25 : 30 min. 1000° H_2 Burn Oxidation

Poly Gettering, 80 min. @ 620°

25 min. 1000° H_2 Burn Oxidation

Define Base Regions

Boron Implant, $3\times10^{13}/cm^2$ @ 25 Kev

10 min. 1000° H_2 Burn Oxidation

Define Emitter Regions

As Implant, $1\times10^{15}/cm^2$ @ 25 Kev

#2-8 : 10 min. 900° H_2 Burn Oxidation

Define Poly Windows

Poly Deposition, 8 min. @ 620°

As Implant,

#2,3,7 : 1×10^{15} @ 25 Kev

#4,5,8 : 3×10^{15} @ 25 Kev

Poly Definition

10 min. 800-1000° H_2 Burn Oxidation

#0,1-5,7,8 : Define Contacts

Metallization(Perkin-Elmer), RF sputter Al-Si

Presputter 10 min. , Sputter Al 30 min.

Best Results Obtained

Figure 27b. Wafer Set V, good Poly Contacted and Control Devices.

Wafer set V Results

Wafer set V resulted in good substrate (control) devices and good polysilicon contacted devices. The average the peak betas, leakage currents, ideality factors, and breakdown voltages were all very reasonable. Preliminary results of wafer set are tabulated as shown in Figure 27b. Wafers labeled V2, V3, and V5 are listed.

The data in Figure 28 can be interpreted as follows:

1. The "wafer lot" is series "V", the wafer number is "V3"; "V3-ii-36" means from V3 quadrant "ii" on the wafer and a 36 micron by 36 micron emitter devices in the package.
2. The type of device is "sub" for the control or metal contacted BJT, while the polysilicon contacted emitter is called "1con" or "con1".
3. Each device has a label; i.e. "con1 12" is the 12th device in the array of polysilicon contacted devices. Therefore "V3-ii-36-con1-12" is from wafer set V, wafer 3, 2nd quadrant, a 36 $\mu \times 36\ \mu$ device, and polysilicon contacted emitter.
4. The complete testing data is enclosed for 18 $\mu \times 18\ \mu$ sub; 18 $\mu \times 18\ \mu$ 1con; 36 $\mu \times 36\ \mu$ sub; and 36 $\mu \times 36\ \mu$ 1con devices.
5. The data was obtained on a HP 4145A Semiconductor Parameter analyzer. Analysis of the data was with a computer program to take slopes, projections, maximum values, etc. Both the emitter base and the collector base junctions are measured, with IS as the forward biased extrapolated coefficient; η(eta) is the slope from ideal; res is the emitter or collector series resistances; Vebo is the E-B breakdown voltage, lebo is the measured reverse bias leakage current; Vcbo is the C-B breakdown voltage, lcbo is the measured reverse bias leakage current; Vceo is the C-E base open breakdown; Max beta is the peak beta, etc.

Figure 29 through Figure 33 are the statistical data on the devices tested. Figure 29 has all the statistical data on wafer "V2" for the 36 $\mu \times 36\ \mu$ 1con and substrate devices. Note that for the 36 μ by 36 μ devices the ratio of the beta poly-contacted/metal contacted is about 2.278 for the average peak betas. The squares are the 25% and 75% marks of the data and the solid line is the median. The tightness of the betas for the control devices is better than that of the poly-contacted devices.

Figure 30 illustrates a comparison of wafer V3 for the 18 $\mu \times 18\ \mu$ and 36 $\mu \times 36\ \mu$ devices, while Figure 31 lists the statistical data for the 18 $\mu \times 18\ \mu$ transistors. For the 18 $\mu \times 18\ \mu$ devices the ratio of the beta poly-contacted/metal contacted is about 1.715 for the average peak betas. Figure 32 shows that for the 36 μ by 36 μ devices the ratio of the beta poly-contacted/metal contacted is about 2.997 for the average peak betas.

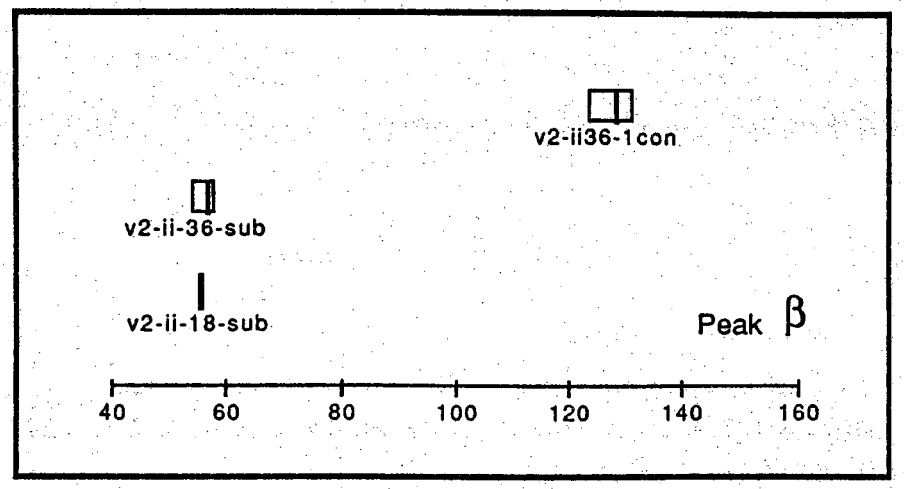
Figure 33 illustrates a comparison of wafer V5 for the 18 $\mu \times 18$ μ and 36 $\mu \times 36$ μ devices, while Figure 34 lists the statistical data for the 18 $\mu \times \mu$ transistors. For the 18 $\mu \times \mu$ devices the ratio of the beta poly-contacted/metal contacted is about 1.771 for the average peak betas. Figure 35 shows that for the 36 μ by 36 μ devices the ratio of the beta poly-contacted/metal contacted is about 2.566 for the average peak betas.

Figures 36 and 37 are a result of combining all the data from wafers V2, V3, and V5. Clearly the poly-contacted devices show a beta enhancement over the sub devices. All devices have identical processing on each wafer. The 36 μm emitter structures show better beta enhancement results because the ratio of the area to perimeter is larger. Wafer V3 had a 1000 C $^{\circ}$ poly anneal and wafer V5 had a 900 C $^{\circ}$ anneal. The results show that the 1000 C $^{\circ}$ anneal has produced a better set of poly contacted emitter devices. Figure 38 lists the "run sheet" for wafer V3.

	base/emitter					base/collector						
	Is Amps	eta	res kohms	Veb0 @1uA	Ieb0 Amps	Is Amps	eta	res kohms	Vcb0 @1uA	Icb0 Amps	max beta	Vce0 @1mA
v3-ii-18c- sub 1	1.5e-15	1.08	0.2	8.40	2.90e-12	5.1e-15	1.07	0.3	51.00	1.77e-10	70.1	51.22
v3-ii-18c-sub2	2.7e-11	2.00	0.1	0.20	1.57e-05	9.4e-15	1.08	0.3	17.40	5.64e-08	15.6	51.22
v3-ii-18-sub3	2.3e-15	1.10	0.2	8.40	2.28e-11	5.0e-14	1.20	0.3	53.00	4.19e-08	71.1	-53.66
v3-ii-18-sub4	1.7e-15	1.08	0.3	8.60	2.03e-11	6.6e-15	1.08	0.3	51.00	1.16e-11	10000.0	-51.22
v3-ii-18c-sub6	1.2e-15	1.07	0.2	8.40	7.00e-12	4.7e-15	1.06	0.3	50.40	1.39e-11	72.9	49.76
v3-ii-18c-sub8	1.3e-15	1.07	0.2	8.40	5.40e-12	4.9e-15	1.06	0.3	51.00	1.60e-11	70.9	51.22
v3-ii-18-sub9	1.9e-15	1.09	0.2	8.00	3.05e-11	7.4e-15	1.08	0.3	53.00	1.36e-11	74.2	-53.66
v3-ii-18-sub10	1.8e-15	1.08	0.2	8.40	2.71e-11	6.8e-15	1.07	0.3	53.00	2.71e-08	74.7	-53.66
v3-ii-18-sub11	1.6e-15	1.08	0.2	8.60	2.91e-11	6.2e-15	1.07	0.6	52.00	1.46e-11	2159.1	-56.10
v3-ii-18c-sub12	1.4e-15	1.08	0.2	8.50	8.10e-12	5.0e-15	1.06	0.3	52.20	1.59e-09	70.9	52.68
v3-iii-18c-sub11	1.7e-15	1.08	0.2	8.80	5.20e-12	5.3e-15	1.06	0.3	51.60	1.82e-11	74.1	51.22
v3-iii-18c-sub12	1.4e-15	1.07	0.2	8.70	4.65e-12	5.2e-15	1.06	0.3	51.00	1.13e-09	76.9	51.22
v3-iv-18c-sub2	1.6e-15	1.08	0.2	8.40	5.00e-14	6.2e-15	1.07	0.3	50.40	1.46e-11	82.5	51.22
v3-iv-18c-sub5	1.7e-15	1.08	0.2	8.60	7.35e-12	6.7e-15	1.07	0.3	49.80	1.25e-11	77.6	49.76
v3-iv-18c-sub11	2.1e-15	1.09	0.2	8.60	5.25e-12	7.1e-15	1.07	0.3	51.00	1.21e-11	76.3	51.22
v3-iv-18c-sub12	2.4e-15	1.09	0.2	8.60	1.60e-12	7.5e-15	1.08	0.3	51.00	1.37e-11	79.8	51.22
v3-ii-18-1con1	2.0e-15	1.11	0.6	7.40	6.69e-11	6.9e-15	1.08	0.3	53.00	2.44e-08	136.2	-53.66
v3-ii-18c-1con2	3.8e-15	1.12	0.5	5.90	1.76e-11	1.9e-07	2.32	0.5	1.20	8.56e-05	10000.0	4.39
v3-ii-18-1con3	1.5e-15	1.10	0.5	7.40	5.76e-11	5.4e-15	1.06	0.3	31.00	5.60e-11	148.6	-31.71
v3-ii-18c-1con4	1.4e-15	1.09	0.5	7.30	4.05e-12	4.8e-15	1.06	0.3	31.20	8.09e-09	135.4	49.76
v3-ii-18-1con5	4.1e-15	1.15	0.5	7.40	2.88e-11	7.4e-15	1.07	0.3	52.00	1.48e-11	122.3	-51.22
v3-ii-18c-1con6	1.3e-15	1.09	0.6	7.10	3.35e-12	4.6e-15	1.06	0.3	52.20	1.36e-11	127.3	52.68
v3-ii-18c-1con7	1.5e-15	1.10	0.6	7.30	6.20e-12	5.0e-15	1.06	0.3	51.60	6.65e-12	124.7	51.22
v3-ii-18c-1con8	1.5e-15	1.09	0.7	7.20	4.20e-12	5.1e-15	1.06	0.3	49.20	7.90e-12	131.8	49.76
v3-ii-18-1con9	1.9e-15	1.10	0.7	7.40	4.61e-11	8.6e-14	1.21	0.3	53.00	1.30e-11	116.1	-53.66
v3-ii-18-1con10	2.0e-15	1.11	0.8	7.40	4.69e-11	6.8e-15	1.07	0.3	53.00	1.18e-11	114.5	-53.66
v3-ii-18c-1con11	1.4e-09	1.59	1.8	2.80	3.27e-07	4.8e-15	1.05	0.3	51.00	1.51e-11	13.9	52.68
v3-ii-18c-1con12	1.1e-14	1.20	1.2	7.30	3.01e-09	1.4e-14	1.12	0.3	15.00	4.23e-07	70.5	30.73
v3-iii-18c-1con1	1.5e-15	1.09	0.9	7.30	5.10e-12	6.3e-15	1.07	0.3	50.40	1.35e-11	123.9	51.22
v3-iii-18c-1con2	1.2e-15	1.08	0.9	7.30	6.60e-12	5.5e-15	1.06	0.3	49.80	8.76e-10	121.0	49.76
v3-iii-18c-1con5	1.3e-15	1.08	1.0	7.40	6.40e-12	6.1e-15	1.06	0.3	50.40	1.30e-11	109.4	51.22
v3-iii-18c-1con8	1.2e-15	1.08	0.9	7.30	6.75e-12	5.9e-15	1.06	0.3	48.60	8.80e-12	125.9	49.76
v3-iii-18c-1con11	1.5e-15	1.09	0.8	7.40	6.40e-12	5.9e-15	1.06	0.3	47.40	7.20e-12	126.3	48.29
v3-iii-18c-1con12	8.7e-16	1.05	0.8	7.30	3.10e-12	3.3e-08	2.82	0.2	1.20	1.09e-05	3131.6	14.63
v3-iv-18c-1con1	4.9e-14	1.29	2.2	7.40	4.05e-12	5.8e-14	1.29	0.2	49.20	2.04e-11	99.2	49.76
v3-iv-18c-1con2	1.1e-15	1.08	1.0	7.50	8.50e-12	5.7e-15	1.07	0.3	51.00	1.05e-11	128.5	51.22
v3-iv-18c-1con5	1.2e-15	1.08	0.6	7.50	3.35e-12	6.4e-15	1.07	0.3	50.40	1.50e-11	122.3	51.22
v3-iv-18c-1con10	1.9e-15	1.10	0.3	8.40	2.95e-12	6.8e-15	1.07	0.3	50.40	1.28e-11	105.5	51.22
v3-iv-18c-1con11	2.1e-15	1.10	0.3	8.30	2.30e-12	7.2e-15	1.07	0.3	49.80	1.48e-11	109.5	49.76
v3-iv-18c-1con12	2.0e-15	1.10	0.3	8.60	1.70e-12	6.9e-15	1.07	0.3	51.00	1.25e-11	107.3	51.22
v3-ii-36c-sub1	4.2e-15	1.07	0.3	8.40	2.10e-12	1.4e-14	1.07	0.3	52.20	2.35e-11	75.7	51.22
v3-ii-36c-sub2	4.0e-15	1.07	0.3	8.40	3.70e-12	1.4e-14	1.07	0.3	51.00	2.43e-11	74.3	51.22
v3-ii-36-sub4	3.6e-15	1.06	0.3	8.30	1.70e-12	1.4e-14	1.07	0.3	50.40	8.90e-10	76.6	-49.76
v3-ii-36c-sub10	3.5e-15	1.06	0.3	8.40	3.15e-12	1.3e-14	1.07	0.3	50.40	2.34e-11	77.0	49.76
v3-ii-36c-sub11	3.9e-15	1.07	0.3	8.40	4.95e-12	1.3e-14	1.07	0.3	51.60	2.09e-11	75.9	51.22
v3-ii-36c-sub12	2.2e-15	1.02	0.3	8.40	2.64e-09	4.5e-10	1.73	0.3	9.00	1.87e-06	77.5	20.49
v3-iii-36c-sub6	4.7e-15	1.08	0.3	8.50	3.90e-12	1.7e-14	1.08	0.3	49.20	1.62e-11	79.7	49.76
v3-iii-36c-sub7	4.1e-15	1.07	0.3	8.50	2.80e-12	1.9e-14	1.08	0.3	48.60	1.58e-11	84.9	48.29
v3-iii-36c-sub11	4.3e-15	1.07	0.3	8.70	3.75e-12	2.0e-14	1.08	0.3	46.80	1.44e-11	84.1	46.83
v3-iii-36c-sub12	4.5e-15	1.07	0.3	8.70	1.50e-13	2.1e-14	1.09	0.3	51.00	2.16e-11	84.9	51.22

v3-iv-36c-sub7	8.6e-15	1.11	0.3	8.50	4.40e-12	4.9e-13	1.30	0.3	8.40	1.18e-05	81.4	11.71
v3-iv-36c-sub8	5.6e-15	1.08	0.3	8.60	4.05e-12	2.1e-14	1.09	0.3	51.00	1.51e-11	83.5	49.76
v3-iv-36c-sub9	5.2e-15	1.08	0.3	8.30	7.20e-12	2.1e-14	1.09	0.3	43.80	2.02e-08	83.5	46.83
v3-iv-36c-sub10	4.9e-15	1.08	0.3	8.50	3.55e-12	2.2e-14	1.09	0.3	49.80	3.64e-11	84.0	49.76
v3-iv-36c-sub11	6.4e-15	1.09	0.3	8.60	1.20e-10	2.9e-14	1.11	0.3	49.80	2.84e-08	84.5	49.76
v3-iv-36c-sub12	5.8e-15	1.07	0.3	8.60	2.62e-11	2.7e-14	1.10	0.3	18.60	2.33e-08	87.3	42.44
v3-ii-36c-1con1	3.4e-15	1.08	0.3	7.30	3.75e-12	8.6e-15	1.05	0.3	46.20	2.72e-11	228.9	46.83
v3-ii-36c-1con2	4.2e-15	1.09	0.3	7.30	2.25e-12	1.0e-14	1.05	0.3	52.20	4.24e-11	218.9	51.22
v3-ii-36-1con4	2.9e-15	1.07	0.3	7.30	4.45e-12	8.2e-15	1.04	0.3	51.00	1.33e-09	234.0	-51.22
v3-ii-36-1con7	2.7e-15	1.07	0.3	7.30	3.70e-12	8.2e-15	1.04	0.3	32.40	3.13e-10	240.3	-32.20
v3-ii-36-1con9	2.5e-15	1.07	0.3	7.10	3.35e-12	7.5e-15	1.04	0.3	51.00	2.60e-11	240.5	-49.76
v3-ii-36c-1con10	2.9e-15	1.07	0.3	7.30	4.80e-12	7.9e-15	1.04	0.3	50.40	2.04e-11	236.2	49.76
v3-ii-36c-1con11	3.3e-15	1.08	0.3	7.30	3.10e-12	8.4e-15	1.04	0.3	52.20	1.22e-10	224.8	51.22
v3-ii-36c-1con12	3.7e-15	1.08	0.3	7.30	2.85e-12	9.6e-15	1.04	0.3	53.40	1.98e-11	210.9	52.68
v3-iii-36c-1con1	2.2e-15	1.12	0.3	6.30	2.10e-10	1.4e-14	1.07	0.7	8.40	3.61e-06	74.0	51.22
v3-iii-36c-1con2	2.8e-16	1.06	0.3	6.80	6.05e-11	1.5e-14	1.07	1.4	50.40	2.62e-08	386.3	51.22
v3-iii-36c-1con4	5.2e-16	1.09	0.3	6.90	1.90e-10	1.1e-14	1.06	0.3	11.40	2.12e-06	85.0	11.71
v3-iii-36c-1con5	6.5e-16	1.08	0.3	6.90	2.02e-11	8.7e-15	1.04	0.4	50.40	5.15e-10	88.6	51.22
v3-iii-36c-1con6	1.6e-15	1.05	0.3	7.10	8.00e-12	1.1e-14	1.06	0.3	50.40	1.38e-11	324.4	49.76
v3-iii-36c-1con7	1.6e-15	1.04	0.3	7.30	5.05e-12	9.1e-15	1.05	0.3	50.40	4.43e-10	304.9	49.76
v3-iii-36c-1con8	1.8e-15	1.05	0.3	7.30	6.65e-12	9.5e-15	1.05	0.3	50.40	1.30e-11	281.8	49.76
v3-iii-36c-1con11	2.1e-15	1.05	0.3	7.40	5.35e-12	9.7e-15	1.05	0.3	51.60	6.95e-12	273.0	51.22
v3-iv-36c-1con1	4.3e-16	1.08	0.4	6.30	6.83e-10	1.1e-14	1.05	1.0	50.40	6.85e-12	26.9	51.22
v3-iv-36c-1con2	4.0e-16	1.08	0.4	6.80	7.32e-11	2.4e-14	1.10	1.4	6.60	5.77e-05	33.4	11.71
v3-iv-36c-1con3	2.9e-16	1.07	0.4	6.90	3.94e-11	9.3e-15	1.05	0.4	49.80	7.40e-12	27.5	51.22
v3-iv-36c-1con5	4.0e-16	1.07	0.4	6.90	2.54e-11	1.1e-14	1.05	0.3	49.80	5.85e-12	33.7	51.22
v3-iv-36c-1con6	3.0e-15	1.08	0.3	7.40	5.90e-12	1.3e-14	1.07	0.3	50.40	1.78e-11	205.1	49.76
v3-iv-36c-1con9	4.4e-15	1.09	0.3	7.90	3.50e-12	1.5e-14	1.08	0.3	49.80	2.52e-11	199.9	49.76
v3-iv-36c-1con10	4.9e-15	1.09	0.3	7.90	5.35e-10	1.8e-14	1.08	0.3	50.40	1.36e-11	212.7	49.76
v3-iv-36c-1con12	3.0e-15	1.06	0.3	7.60	6.50e-12	1.5e-14	1.07	0.3	52.20	1.49e-11	239.9	51.22

Figure 28. Transistor Measured Data.



v2-ii-36-sub

Data File:Copy of PE v 2-3-5-7

Variable: v2-ii-36-sub Observations: 6

Minimum: 52.900	Maximum: 59.200
Range: 6.300	Median: 56.550
Mean: 56.017	Standard Error: 1.015
Variance:	6.182
Standard Deviation:	2.486
Coefficient of Variation:	4.438
Skewness: -0.109	Kurtosis: -1.899

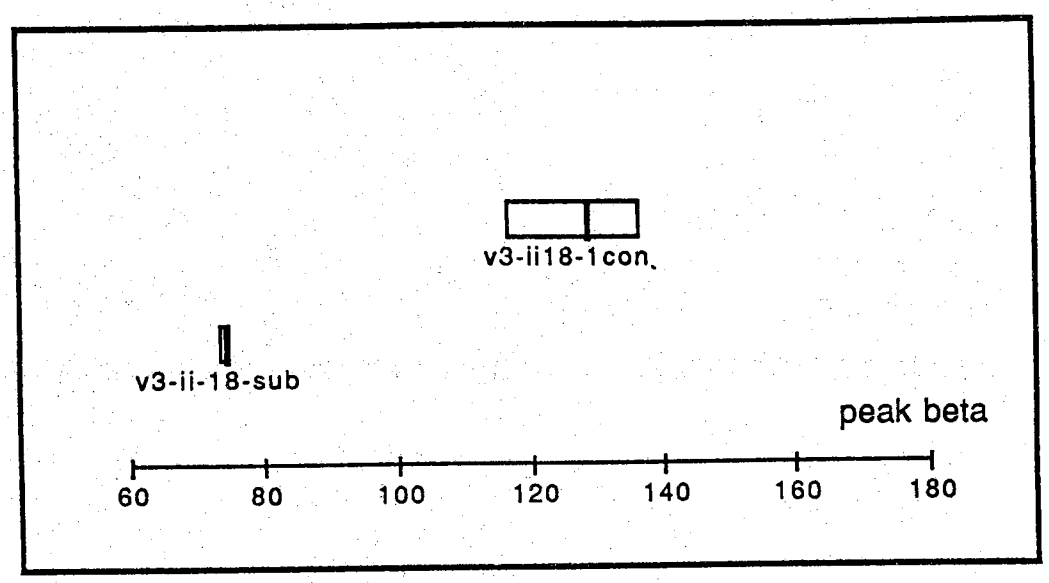
v2-ii36-1con

Data File: Copy of PE v 2-3-5-7

Variable: v2-ii36-1con Observations: 8

Minimum: 122.700	Maximum: 133.100
Range: 10.400	Median: 128.450
Mean: 127.588	Standard Error: 1.484
Variance:	17.630
Standard Deviation:	4.199
Coefficient of Variation:	3.291
Skewness: 0.024	Kurtosis: -1.810

Figure 29. Wafer V2, Beta Comparison



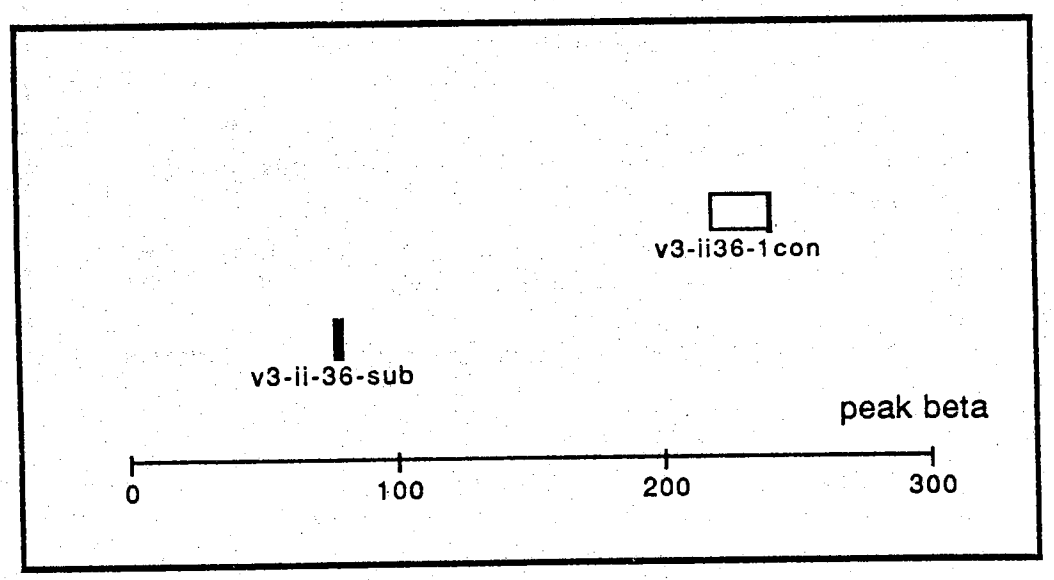


Figure 30. Set U, wafer V3: 18 $\mu \times 36$ μ Devices

v3-ii-18-sub

Data File: Copy of PE v 2-3-5-7

Variable: v3-ii-18-sub Observations: 7

Minimum: 71.100	Maximum: 74.700
Range: 3.600	Median: 74.100
Mean: 73.586	Standard Error: 0.458
Variance:	1.468
Standard Deviation:	1.212
Coefficient of Variation:	1.647
Skewness: -1.073	Kurtosis: -0.332

v3-ii18-1con

Data File: Copy of PE v 2-3-5-7

Variable: v3-ii18-1con Observations: 10

Minimum: 96.400	Maximum: 148.600
Range: 52.200	Median: 128.450
Mean: 126.210	Standard Error: 4.640
Variance:	215.325
Standard Deviation:	14.674
Coefficient of Variation:	11.627
Skewness: -0.478	Kurtosis: -0.628

Figure 31. Statistics of Wafer V3, 18 μ Devices

v3-ii-36-sub

Data File: Copy of PE v 2-3-5-7
Variable: v3-ii-36-sub Observations: 5

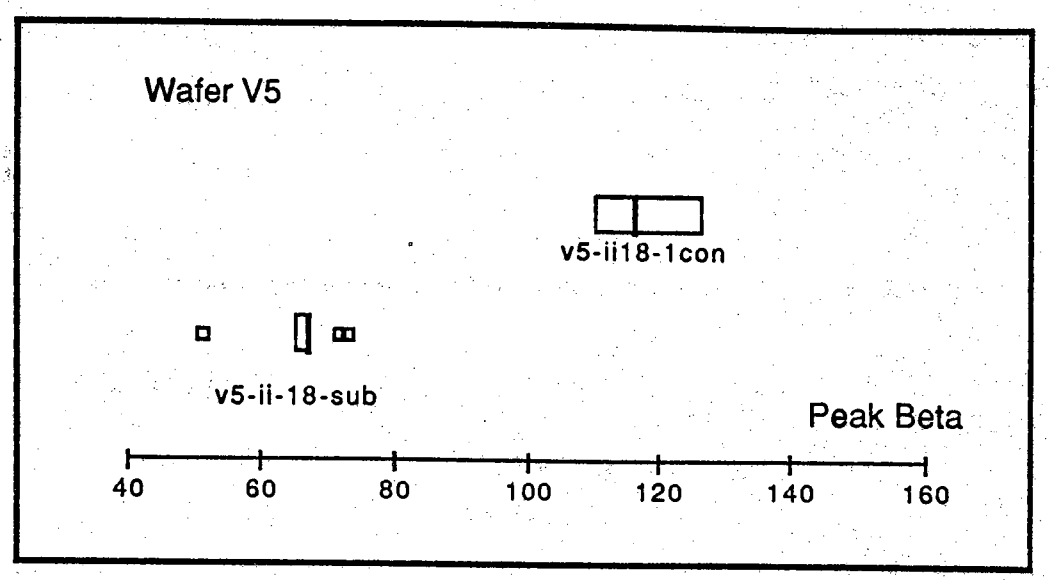
Minimum: 76.600	Maximum: 78.900
Range: 2.300	Median: 77.800
Mean: 77.760	Standard Error: 0.372
Variance:	0.693
Standard Deviation:	0.832
Coefficient of Variation:	1.071
Skewness: -0.029	Kurtosis: -1.539

v3-ii36-1con

Data File: Copy of PE v 2-3-5-7
Variable: v3-ii36-1con Observations: 7

Minimum: 209.700	Maximum: 246.000
Range: 36.300	Median: 240.300
Mean: 232.914	Standard Error: 5.190
Variance:	188.565
Standard Deviation:	13.732
Coefficient of Variation:	5.896
Skewness: -0.666	Kurtosis: -1.459

Figure 32. Statistics Set U, Wafer V3, 36 μ Devices



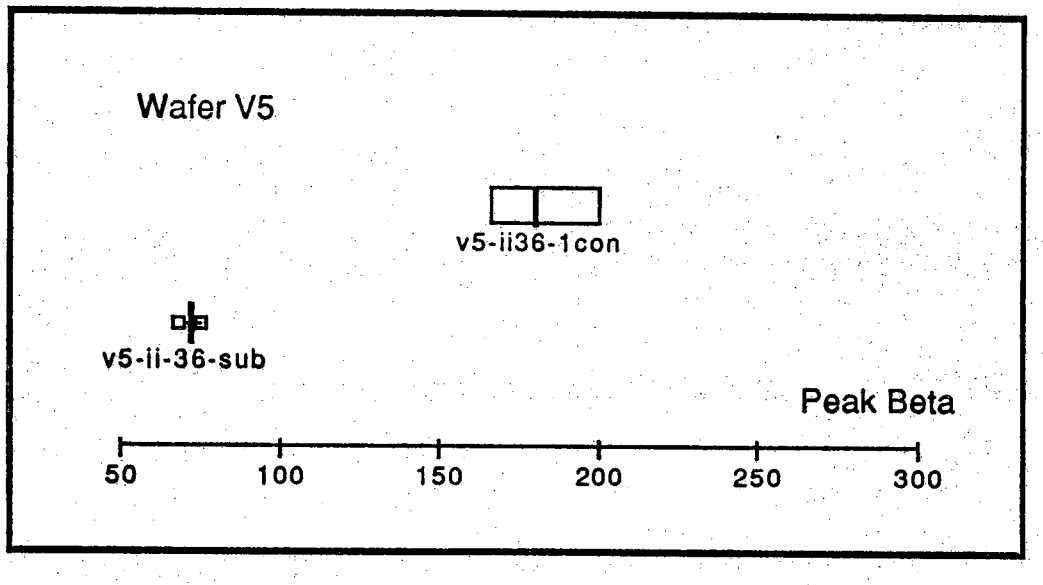


Figure 33. Set V, Wafer 5 Devices

v5-ii-18-sub

Data File: PE v 2-3-5-7
Variable: v5-ii-18-sub Observations: 13

Minimum: 51.100	Maximum: 72.800
Range: 21.700	Median: 66.800
Mean: 65.792	Standard Error: 1.470
Variance:	28.076
Standard Deviation:	5.299
Coefficient of Variation:	8.054
Skewness: -1.372	Kurtosis: 1.955

v5-ii18-1con

Data File: PE v 2-3-5-7
Variable: v5-ii18-1con Observations: 10

Minimum: 91.900	Maximum: 132.800
Range: 40.900	Median: 116.100
Mean: 116.520	Standard Error: 3.913
Variance:	153.095
Standard Deviation:	12.373
Coefficient of Variation:	10.619
Skewness: -0.416	Kurtosis: -0.882

Figure 34. Statistics Set V5, Wafer, 18 μ Devices

v5-ii-36-sub

Data File: PE v 2-3-5-7
Variable: v5-ii-36-sub Observations: 6

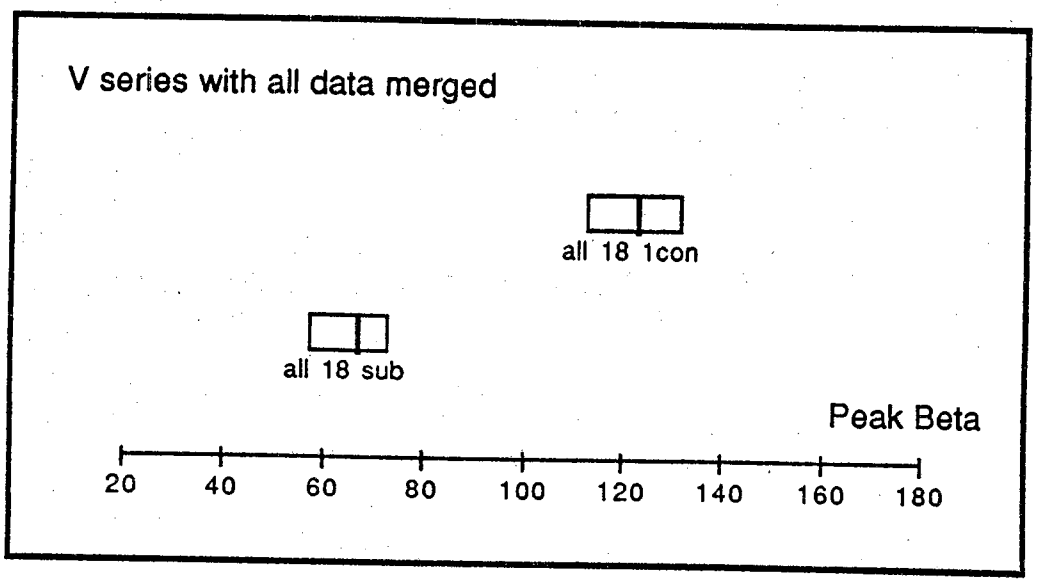
Minimum: 68.200	Maximum: 74.600
Range: 6.400	Median: 71.100
Mean: 71.317	Standard Error: 0.849
Variance:	4.330
Standard Deviation:	2.081
Coefficient of Variation:	2.918
Skewness: 0.099	Kurtosis: -1.123

v5-ii36-1con

Data File: PE v 2-3-5-7
Variable: v5-ii36-1con Observations: 8

Minimum: 159.600	Maximum: 213.500
Range: 53.900	Median: 180.100
Mean: 183.012	Standard Error: 7.271
Variance:	422.993
Standard Deviation:	20.567
Coefficient of Variation:	11.238
Skewness: 0.234	Kurtosis: -1.819

Figure 35. Set V5, Wafer, 36 μ Devices



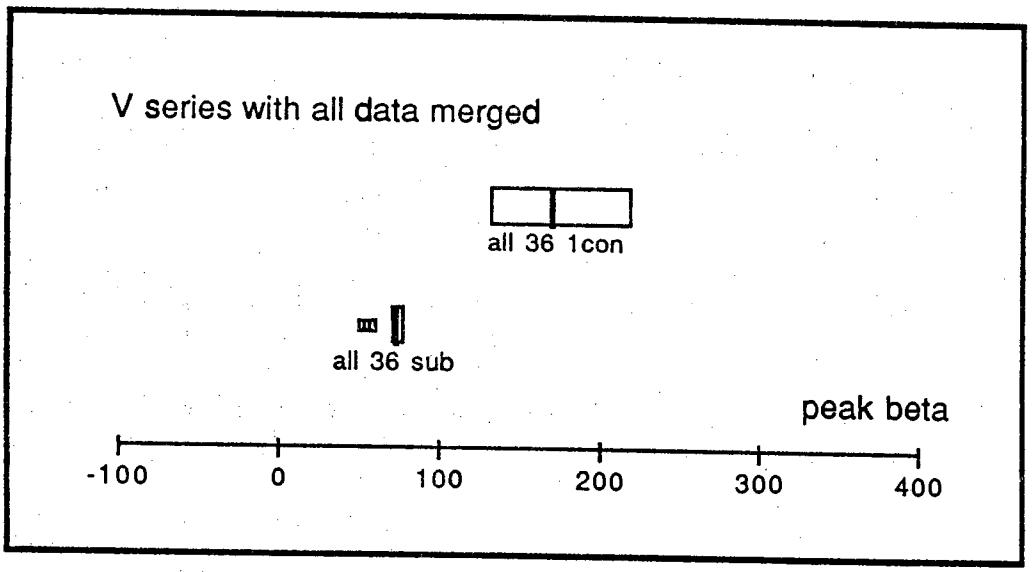


Figure 36. All Devices From Set V, V2, V3 and V5

Data File: PE v 2-3-5-7		**all 36 sub**
Variable: all 36 sub	Observations: 24	
Minimum: 52.900	Maximum: 78.900	
Range: 26.000	Median: 71.400	
Mean: 70.004	Standard Error: 1.662	
Variance:	66.266	
Standard Deviation:	8.140	
Coefficient of Variation:	11.628	

Data File: PE v 2-3-5-7		**all 36 1con**
Variable: all 36 1con	Observations: 23	
Minimum: 122.700	Maximum: 246.000	
Range: 123.300	Median: 170.600	
Mean: 178.922	Standard Error: 9.518	
Variance:	2083.528	
Standard Deviation:	45.646	
Coefficient of Variation:	25.512	

Data File: PE v 2-3-5-7		**all 18 sub**
Variable: all 18 sub	Observations: 26	
Minimum: 51.100	Maximum: 74.700	
Range: 23.600	Median: 66.800	
Mean: 65.515	Standard Error: 1.473	
Variance:	56.375	
Standard Deviation:	7.508	
Coefficient of Variation:	11.460	

Data File: PE v 2-3-5-7		**all 18 1con**
Variable: all 18 1con	Observations: 20	
Minimum: 91.900	Maximum: 148.600	
Range: 56.700	Median: 123.050	
Mean: 121.365	Standard Error: 3.156	
Variance:	199.224	
Standard Deviation:	14.115	
Coefficient of Variation:	11.630	

Figure 37. Statistics from All of V2, V3, and V5 Wafers

Poly Emitter Process Run Sheet

Step	Description	Date	Comments	Measurements
1	Clean			
2	H2 Burn Oxid 25min @ 1000			
3	Mask front AZ1350			
4	BHF etch - 3min			
5	Remove resist Clean			
6	Poly dep - 1u 80min @ 620			
7	Mask back AZ1350			
8	RPZ Poly etch BHF etch - 3min			
9	Remove resist			
10	Clean			
11	H2 Burn Oxid 25min @ 1000			
12	Mask #1 - Base AZ1350			
13	BHF etch - 3min			
14	Remove resist			
15	Boron Implant 3e13 @ 25keV x 3uA			
16	Clean			
17	H2 Burn Oxid 10min @ 1000			
18	Mask #2 - Emitter AZ1350			
19	BHF etch - 3min			
20	Remove resist			

Figure 38. V3 Run Sheet

Step	Description	Date	Comments	Measurements
21	As Implant 1e15 @ 25keV			
22	Clean			
23	H2 Burn Oxid 10min @ 900			
24	Mask #3 - Poly Window AZ1350			
25	BHF etch - 3min			
26	Remove resist Clean			
27	Poly dep - 0.1u 8min @ 620			
28	As Implant 3e15 @ 25keV			
29	Mask #4 - Poly Defin.			
30	RPZ Poly etch			
31	Remove resist Clean			
32	H2 Burn Oxid 10min @ 1000			
33	Mask #5 - Contacts AZ1350			
34	BHF etch - 3min			
35	Remove resist Clean			
36	Dry Bake 10min @ 120			
37	Mask #6 - Metal Defin.			
38	BHF dip - 5sec			
39	Sputter Al- 1% Si 25min @ 100W			
40	Lift-off metal 30min Ace in U.C.			

Figure 38 (continued)

B. 2D Silicon Bipolar Device Modeling

Introduction

In the early stages of semiconductor device modeling highly simplified one-dimensional models readily accessible to direct analytic treatment were used to understand device behavior and to improve design. With the advent of VLSI and miniaturization these simplified models have been rendered obsolete in most cases. Instead, the emphasis has shifted towards numerical simulation techniques, i.e. the solution of the semiconductor equations by use of discretization techniques and solution of the discretized equations by computer. This method was suggested by Gummel for the bipolar transistor [1], and by DeMari for the p-n junction diode [2,3]. As early as the late sixties some were applying two-dimensional discretizations [4-6].

The question of whether a particular device to be modeled requires higher dimensional discretizations to be modeled accurately depends on the geometry of the device and the desires of the engineer. If one desires only global quantities such as current-voltage characteristics, a one-dimensional model may be sufficient since most of the physical quantities can be treated in a heuristic manner. However, the main power of higher-dimensional device models lies in their capability to provide insight into the functioning of a device by means of the distributions of the various physical parameters inside the device. For some miniaturized devices, higher-dimensional models are often the only imaginable tool for the accurate prediction of device performance.

Modeling is becoming more and more relevant during the development phase of a particular device because of the possible decrease of the number of trial and error steps through this development. It has been estimated that the average savings in development effort can be on the order of forty percent [7]. It is expected that applications of device modeling will increase with the decreasing cost of computer resources compared to the skyrocketing cost of experimental investigations. Trial and error is still very much required because the uncertainties of several of the physical parameters in the models are still too large.

TRAN2D is a modification of a two-dimensional simulation code developed for silicon solar cells [8]. Some of the modifications included handling several diffusions, multiple contacts (as opposed to just two for solar cells), and an accurate method for extracting the terminal currents from the simulation results.

In the following pages a brief derivation of the discretized equations necessary in two-dimensional simulation is made. The method that TRAN2D uses to solve the subsequent set of equations is presented. Finally, the system developed for extracting terminal currents is explained and some results are presented.

The Semiconductor Equations

Three equations must be solved self-consistently to characterize the operating characteristics of a semiconductor device under steady-state conditions. These are, Poisson's equation,

$$\nabla^2 V = \frac{q}{\epsilon_s}(n - p - dop)$$

and the hole and electron continuity equations

$$\nabla \cdot \vec{J}_p = q(G - R)$$
$$\nabla \cdot \vec{J}_n = -q(G - R)$$

where ϵ_s is the semiconductor dielectric constant, assumed uniform, and dop is the net impurity density. TRAN2D assumes that all dopants are ionized. G is the generation rate, and R is the sum of Shockley-Read-Hall and Auger recombination processes [9],

$$R = (pn - n_{ie}^2)\left[A_n n + A_p p + \frac{1}{\tau_n(p + p_1) + \tau_p(n + n_1)}\right],$$

where a single trap energy level has been assumed. Doping dependence of the SRH term is included by letting [10],

$$\tau_n = \frac{\tau_{n0}}{1 + \frac{N_D + N_A}{N_C}}$$

and

$$\tau_p = \frac{\tau_{p0}}{1 + \frac{N_D + N_A}{N_C}}.$$

n_{ie}^2 is the effective intrinsic carrier concentration which may differ from n_i^2 in an undoped substrate due to bandgap narrowing effects. Bandgap narrowing and effects due to Fermi-Dirac statistics are included in the transport equations by the addition of a "quasi-electric field" term in the drift term [8,11],

$$\vec{J}_p = -\mu_p p \nabla V_p - \mu_p \nabla p$$
$$\vec{J}_n = -\mu_n n \nabla V_n + \mu_n \nabla n$$

where V_p and V_n are effective potentials.

$$V_p = V - (1-\gamma)\frac{\Delta_g}{q}$$

$$V_n = V + \gamma\frac{\Delta_g}{q}$$

where Δ_g is the effective bandgap shrinkage and γ is the asymmetry factor (i.e. how much of the shrinkage occurs in the conduction band and how much in the valence). It is generally taken to be 1/2. For a more detailed discussion of these parameters and their effects on the transport equations the reader is referred to the references [8,11].

Solution of a Non-Linear Equation by Newton's Method

In general the roots of a nonlinear equation $f(x)=0$ cannot be expressed in closed form. Consequently, one must resort to some approximation method, which generally involves some type of iterative scheme, which means an initial guess is made, say x_0, then improvements on the guess are made iteratively. This generates a sequence of estimates to the actual root, x_0, x_1, x_2, x_3..., which presumably converge to the desired root.

There are many methods for calculating the improvement during each subinterval of the iteration, each having different rates of convergence and requirements for the initial guess [13]. Here we will explore general features of Newton's method.

If α is one of the roots of f(x), and we are at the n^{th} iteration in our sequence then we obtain the $(n+1)^{th}$ approximation to α (i.e. x_{n+1}) in the following way. The curve f(x) is approximated by its tangent at the point $(x_n, f(x_n))$, and x_{n+1} is taken as the intersection of this tangent line with the x-axis. Thus for determining x_{n+1}, we have the following equation,

$$f(x_n) + f'(x_n)(x_{n+1} - x_n) = 0$$

solving for x_{n+1},

$$x_{n+1} = x_n - \frac{f(x_n)}{\left.\frac{df}{dx}\right|_{x=x_n}}.$$

Newton's method is a quadratically convergent method. The proof of this is straightforward. Let α be a simple root of f, then $f'(\alpha)\neq 0$, nor is the derivative zero for a certain neighborhood of α, and expand f in a Taylor series about x_n,

$$f(\alpha) = 0 = f(x_n) + f'(x_n)(\alpha - x_n) + \frac{f''(\eta)}{2}(\alpha - x_n)^2$$

where η is contained in the interval $\eta \leq |x_n - \alpha|$. Then dividing by $f'(x_n)$ and

rewritting

$$\frac{f(x_n)}{f'(x_n)} + (\alpha - x_n) + \frac{f''(\eta)}{2f'(x_n)} (\alpha - x_n)^2 = 0$$

from before,

$$\frac{f(x_n)}{f'(x_n)} = x_n - x_{n+1} ,$$

then,

$$- (x_{n+1} - \alpha) + \frac{f''(\eta)}{2f'(x_n)} (\alpha - x_n)^2 = 0$$

The error for the n^{th} iteration is defined by

$$\epsilon_n = x_n - \alpha,$$

then we have

$$\epsilon_{n+1} = \frac{1}{2} \epsilon_n^2 \frac{f''(\eta)}{f'(x_n)}$$

Thus we see that the error for the $(n+1)^{th}$ iteration depends on the square of the error for the n^{th} iteration, consequently Newton's method is said to be quadratically convergent [13].

Extension of Newton's Method to a Function of Several Variables

Newton's method can be extended to functions of several variables. Newton's method for a function of one variable was essentially derived from a Taylor expansion of f, keeping only linear terms. Analogously, Taylor's formula for n variables gives,

$$\mathbf{f}(\vec{x}) = \mathbf{f}(\vec{x}^{(k)}) + \mathbf{f}'(\vec{x}^{(k)})(\vec{x} - \vec{x}^{(k)}) + 0(||\vec{x} - \vec{x}^{(k)}||^2),$$

where $\mathbf{f}'(x)$ is an nxn matrix consisting of all the partial derivatives,

$$f'_{ij}(\vec{x}) = \frac{\partial f_i}{\partial x_j} (\vec{x}) \qquad 1 \leq i,j \leq n.$$

This leads to an iterative scheme which is now a matrix equation,

$$\mathbf{f}'(\vec{x}^{(k)})(\vec{x}^{(k+1)} - \vec{x}^{(k)}) = -\mathbf{f}(\vec{x}^{(k)})$$

$\mathbf{f}'(\vec{x}^{(k)})$ is called the Jacobian (to be denoted by **J** here). If we let $(\vec{x}^{(k+1)} - \vec{x}^{(k)}) = \Delta\vec{x}^{(k)}$, then this equation takes a form which is obviously a matrix equation,

$$\mathbf{J}\Delta\vec{x} = \vec{y}$$

where $\vec{y} = -\mathbf{f}(\vec{x}^{(k)})$. $\Delta\vec{x}$ is a vector of the corrections to be added to the previous

iteration's solution vector $\vec{x}$ once the matrix equation is solved. This can be done by whatever means desired.

Discretization of the Equations

The numerical solution of boundary value problems of elliptic partial differential equations usually takes the following three steps [14]:

i) The continuous problem is replaced by a set of non-linear equations whose approximate solution are to be found at a finite number of points. This is called discretization of the problem.

ii) Since the set of equations cannot generally be solved exactly, some type of iteration scheme is set up.

iii) At each iteration step a large, sparse, linear set of equations needs to be solved.

TRAN2D uses a classical finite difference discretization of the boundary value problem, by dividing up the domain into a fine rectangular grid (cf. Fig. 39). Differentials in the equations are approximated by difference quotients at the nodal points. In this way a large set of linear equations are generated. Newton's method is used to find the "solution vector". Assuming that the iteration converges, then this vector contains the hole and electron densities and the potentials at the grid points.

The second partials of the potential appearing in Poisson's equation on a two-dimensional grid are approximated in the following manner. First, we take a centered difference quotient about the nodes $(i+1/2,j)$, $(i-1/2,j)$, $(i,j+1/2)$, $(i,j-1/2)$ (cf. Fig. 40):

$$\left.\frac{\partial V}{\partial x}\right|_{i+1/2,j} \simeq \frac{V_{i+1,j}-V_{i,j}}{x_{i+1}-x_i}$$

$$\left.\frac{\partial V}{\partial x}\right|_{i-1/2,j} \simeq \frac{V_{i,j}-V_{i-1,j}}{x_i-x_{i-1}}$$

$$\left.\frac{\partial V}{\partial y}\right|_{i,j+1/2} \simeq \frac{V_{i,j+1}-V_{i,j}}{y_{j+1}-y_j}$$

$$\left.\frac{\partial V}{\partial y}\right|_{i,j-1/2} \simeq \frac{V_{i,j}-V_{i,j-1}}{y_j-y_{j-1}}$$

Second, we take centered-difference quotients of the first partials to obtain the Laplacian at (i,j):

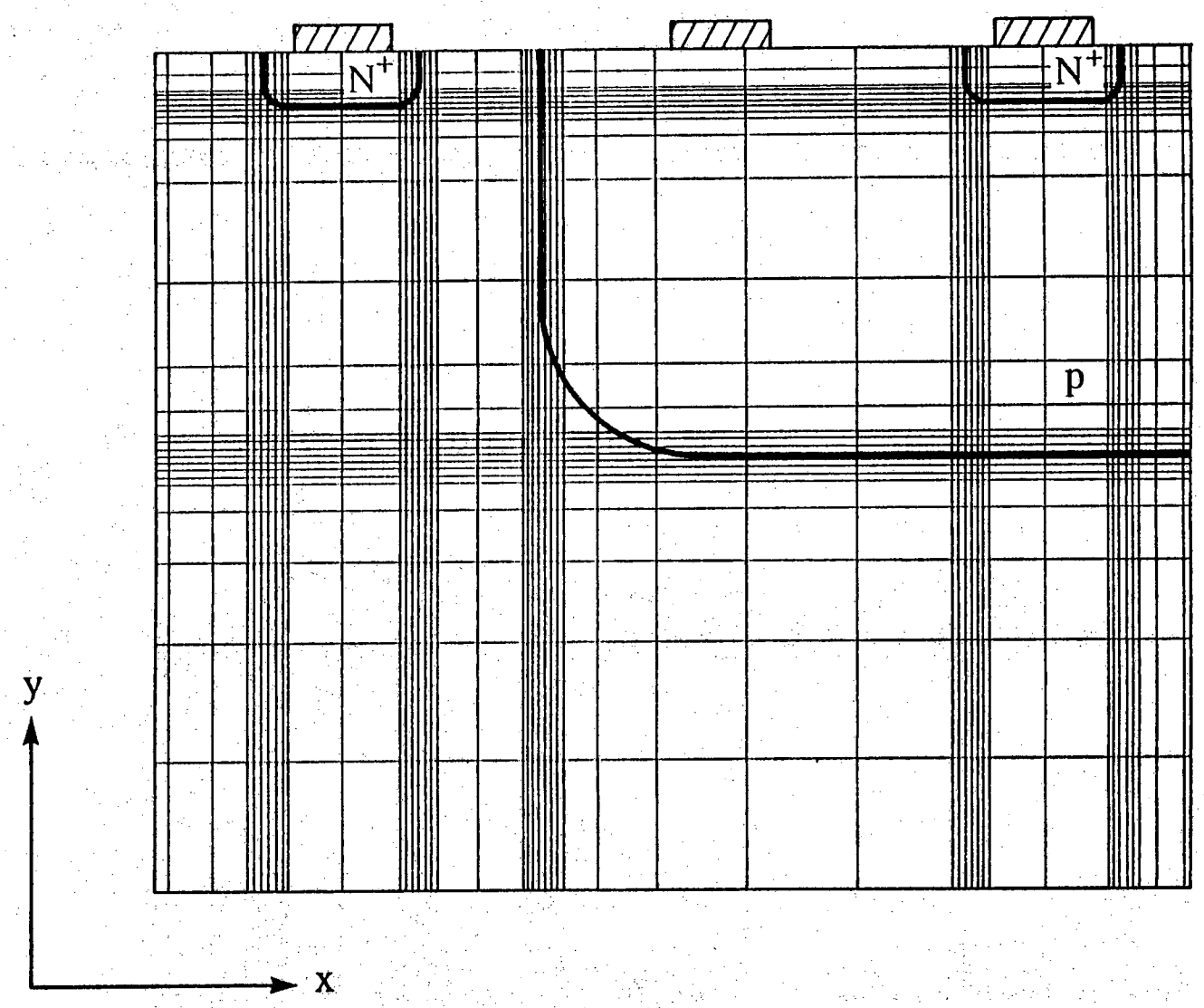


Figure 39

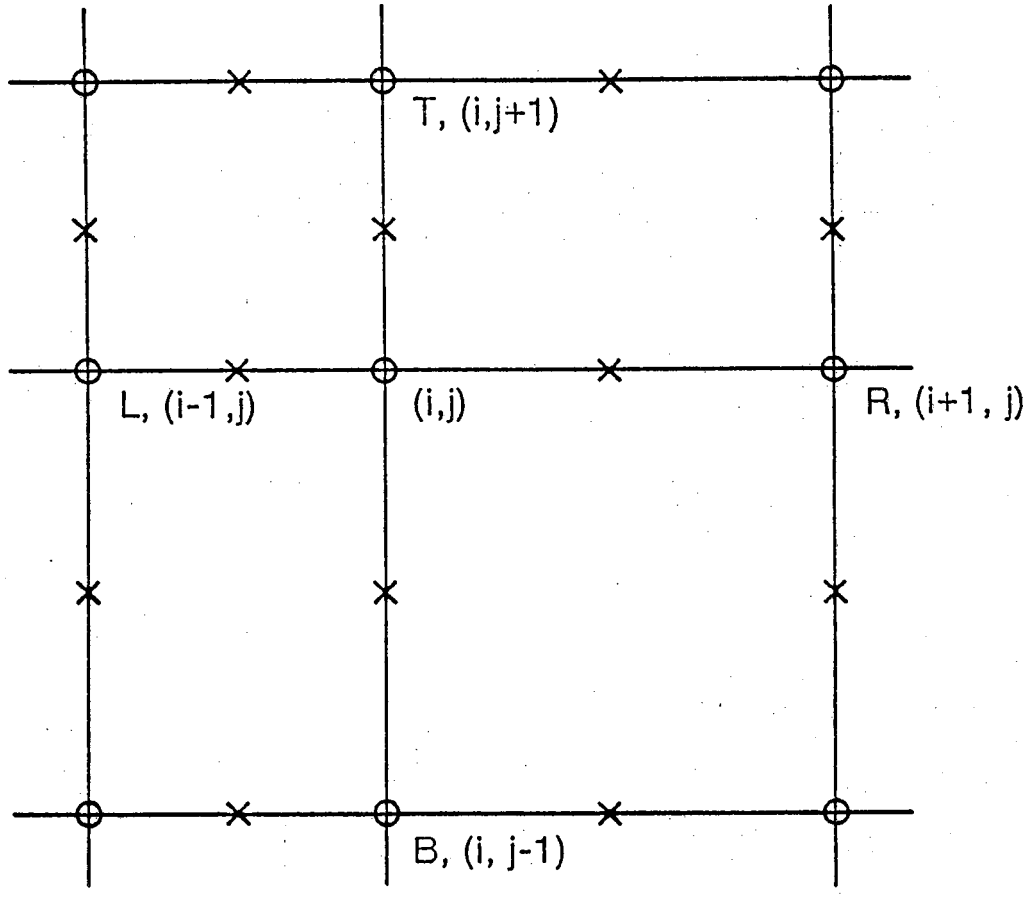


Figure 40

$$\left.\frac{\partial^2 V}{\partial x^2}\right|_{i,j} \simeq \frac{\left.\frac{\partial V}{\partial x}\right|_{i+1/2,j} - \left.\frac{\partial V}{\partial x}\right|_{i-1/2,j}}{1/2(x_{i+1}-x_i)+1/2(x_i-x_{i-1})}$$

$$= 2\,\frac{V_R}{h_R(h_L+h_R)} - 2\,\frac{V_{i,j}}{h_L h_R} + 2\,\frac{V_L}{h_L(h_L+h_R)}$$

where

$$V_R = V_{i+1,j} \qquad h_L = x_i - x_{i-1}$$
$$V_L = V_{i-1,j} \qquad h_R = x_{i+1} - x_i$$

Similarly in the y-direction,

$$\left.\frac{\partial^2 V}{\partial y^2}\right|_{i,j} \simeq 2\,\frac{V_T}{h_T(h_B+h_T)} - 2\,\frac{V_{ij}}{h_B h_T} + 2\,\frac{V_B}{h_B(h_B+h_T)}$$

the subscripts have a similar interpretation but now they refer to top and bottom in the y-direction (cf. Fig. 3).

Combining these, the following discretized form of Poisson's equation is obtained at node (i,j),

$$f_{v,ij} = \frac{2V_B}{h_B(h_B+h_T)} + \frac{2V_R}{h_L(h_L+h_R)} - 2\left(\frac{1}{h_B h_T} + \frac{1}{h_L h_R}\right)V_{ij}$$

$$+ \frac{2V_R}{h_R(h_L+h_R)} + \frac{2V_T}{h_T(h_B+h_T)} - q(n_{ij} - p_{ij} - dop_{ij}) = 0$$

A similar sequence is performed on the continuity equations and the following set of discretizations are obtained,

$$f_{p,ij} = \frac{2(J_{pR}-J_{pL})}{h_L+h_R} + \frac{2(J_{pT}-J_{pB})}{h_B+h_T} - q(G_{ij}-R_{ij}) = 0$$

$$f_{n,ij} = \frac{2(J_{nR}-J_{nL})}{h_L+h_R} + \frac{2(J_n-J_{nB})}{h_B+h_T} + q(G_{ij}-R_{ij}) = 0$$

with similar interpretations for the subscripts, except that now the right (R), left (L), top (T), and bottom (B) refer to the halfway points between the nodes (the x's in Fig. 3). This is necessary because the continuity equations involve only first partials of the current densities.

The $f_{v,ij}$, $f_{p,ij}$, $f_{n,ij}$ are the "vector functions" $f(\vec{x})$ previously mentioned in the extension of Newton's method to functions of several variables. We see that we don't

have one function of several variables but several functions each with several variables. There is one set $\{f_{v,ij}, f_{p,ij}, f_{n,ij}\}$ for each nodal point. In a loose sense the f's can be thought of as the variables of a bigger function, say F.

Problems with Current Calculations

We see that the discretization of the continuity equations requires knowledge of the currents at the half-way points. The currents can be written in terms of the independent variables p, n, and V by simple drift-diffusion. If, for example, we discretize the hole current equation at the top (T) node in the conventional manner, we obtain,

$$J_{pT} = -\frac{\mu_{pT}}{h_T}\left\{\frac{(p_{ij}+p_T)}{2}(V_{pT}-V_{pij}) + (p_T - p_{ij})\right\}.$$

However, it is well known to device modelers that this discretization approximates the continuous equation reasonably only if the change in the quasi-potential between mesh points is less than $2kT/q$ [15]. In a two-dimensional simulation, where nodes are scarce, it is very difficult to be sure that this criterion has been met. This difficulty can be avoided by using the discretization scheme of Scharfetter-Gummel [15]. The hole current equation in normalized form [8] is written,

$$J_p = -\mu_p\left\{p\frac{dV_p}{dx} + \frac{dp}{dx}\right\}$$

$$= -\mu_p e^{-V_p}\frac{d}{dx}(pe^{V_p})$$

then

$$-\frac{J_p}{\mu_p}e^{V_p} = \frac{d}{dx}(pe^{V_p})$$

Assuming that the mobility, current, and quasi-electric field $(-\nabla V_p)$ are constant between the mesh points x_j to x_{j+1} then V_p can be written,

$$V_p(x) = V_{pj} + \frac{V_{p,j+1}-V_{pj}}{h_{j+1}}(x-x_j).$$

Then if we integrate

$$\int_{x_j}^{x_{j+1}} = \frac{J_p e^{V_p(x)}}{\mu_p}dx = \int_{x_j}^{x_j+1}\frac{d}{dx}(pe^{V_p(x)})dx$$

we obtain

$$-\frac{J_{pR}}{\mu_{pR}}\frac{h_R}{\Delta V_{pj}}\left[e^{\Delta V_{pj}}-1\right]=p_R\,e^{\Delta V_{pj}}-p_j$$

where $\Delta V_{pj}=V_{p,j+1}-V_{pj}$ and the R's have the same meaning as before. Then the current density reads,

$$J_{pR}=-\frac{\mu_{pR}\,\Delta V_{pj}}{h_R}\left\{\frac{p_R\,e^{\Delta V_{pj}}-p_j}{e^{\Delta V_{pj}}-1}\right\}$$

The range of validity of the discretization is greater [14]. This allows for the use of fewer mesh points.

There is yet another problem from the standpoint of numerical error. It is well known that subtraction is not a benign operation on the computer. In fact, the relative error in the calculation $y=x_1-x_2$ is [13],

$$\left|\frac{\Delta y}{y}\right|\leq\frac{|\Delta x_1|+|\Delta x_2|}{|x_1-x_2|}$$

which can be substantial for $x_1\approx x_2$. If one uses either the conventional or the Scharfetter-Gummel discretization to calculate majority-carrier currents the results

can be off by orders of magnitude, because in these regions $p_R\simeq p_j$ and $\Delta V_{pj}\approx 0$.

There is a method developed by Lundstrom, whereby the currents into or out of the contacts are computed without calculating majority carrier current densities. The method is quite general, but it will be developed here for the special case of a transistor.

1) The domain is divided into as many subdomains as there are contacts.
2) The continuity equations

$$\nabla\cdot\vec{J}_p=(G-R)\qquad\text{(normalized)}$$
$$\nabla\cdot\vec{J}_p=-(G-R)\qquad\text{(normalized)}$$

are integrated over the regions where the current densities are minority carrier current densities near the contacts. For instance, in region I (cf. Fig. 41), since there is an N+ diffusion under that contact we will integrate $\nabla\cdot\vec{J}_p=(G-R)$ there.

$$\int_I \nabla\cdot\vec{J}_p\,d\Omega=\int_I (G-R)\,d\Omega$$

where $d\Omega$ is a differential area.

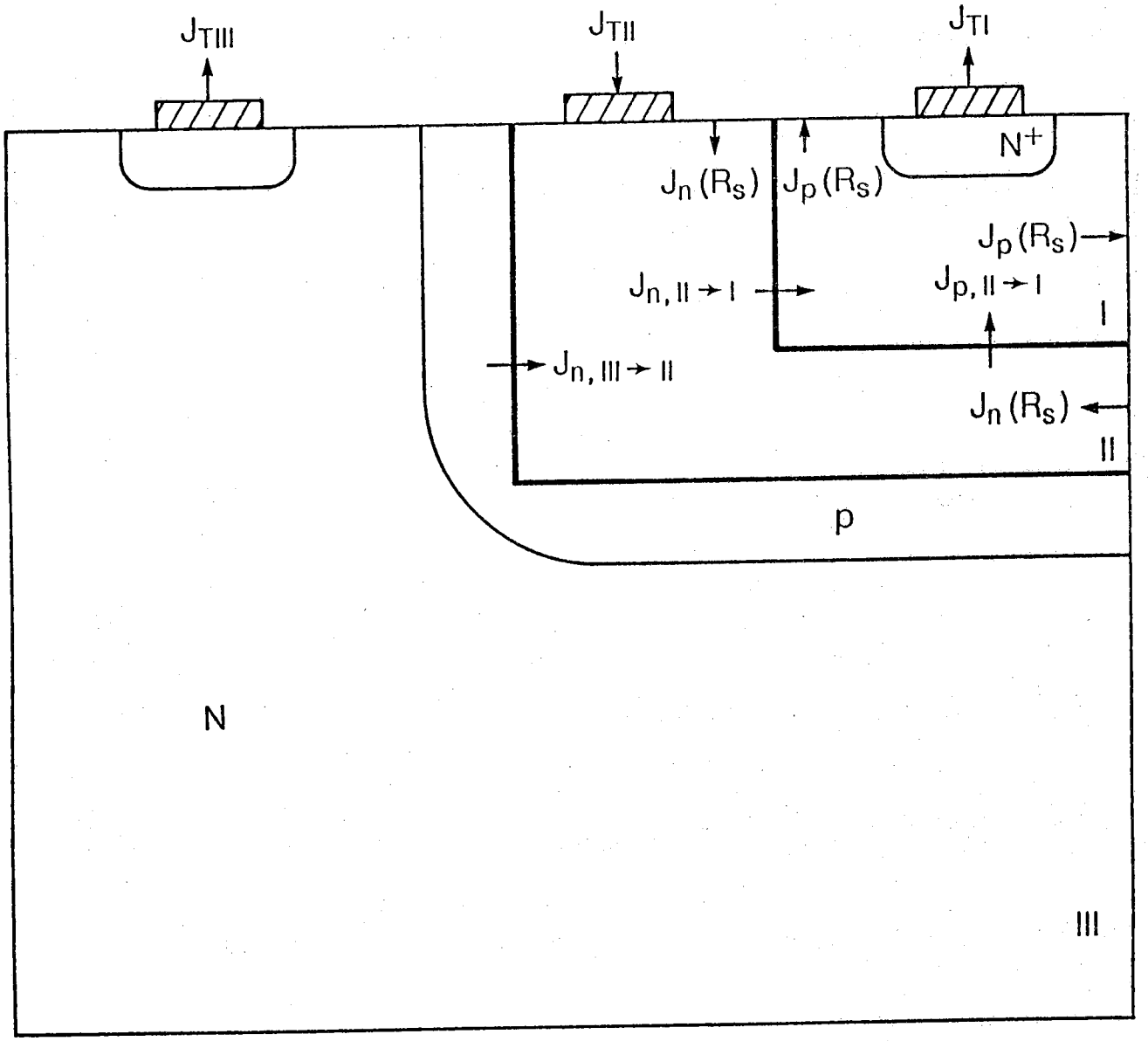

J_{TIII}
J_{TII}
J_{TI}
$J_n(R_s)$
$J_p(R_s)$
N^+
$J_p(R_s)$
$J_{n,II \to I}$
$J_{p,II \to I}$
I
$J_{n,III \to II}$
$J_n(R_s)$
II
p
N
III

Figure 41

Using the divergence theorem, the left hand side becomes an integral over the surface

$$\int_I \nabla \cdot \vec{J}_p \, d\Omega = \int_{S_I} \vec{J}_p \cdot \hat{n} \, ds$$

where S_I means the integral is to be performed on the surface defining region I. When integrating on a physical surface where there is no contact this is a surface recombination current. For region I then we have,

$$\int_{S_I} \vec{J}_p \cdot \hat{n} ds = \int_{\substack{\text{physical} \\ \text{surface}}} J_p(R_s) ds + \int_{\text{contact}} J_p ds$$

$$+ J_{p,II \to I} = \int_I (G - R) \, d\Omega$$

and for region II,

$$\int_{S_{II}} \vec{J}_n \cdot \hat{n} ds = - \int_{\substack{\text{physical} \\ \text{surface}}} J_n(R_s) ds + J_{n,II \to I} - J_{n,III \to II}$$

$$- \int_{\text{contact}} J_n ds = \int_{II} (G - R) d\Omega$$

where $J_{p,II \to I}$ is the total hole current flowing from region II into I. We see that this method is really just doing bookkeeping on the particle flux into a region. For instance, the total hole current flowing from region II into I ($J_{p,II \to I}$) has to either flow out the contact, recombine at the surface, recombine in the bulk, or be added to by generation (G). Thus we could immediately write,

$$J_{p,II \to I} = \int_{\text{contact}} J_p ds + \int_{\substack{\text{physical} \\ \text{surface}}} J_p(R_s) ds - \int_I (G - R) d\Omega,$$

and if we bear in mind that electron particle flow is opposite to the current flow,

$$J_{n,II \to I} - J_{n,III \to II} = \int_{\substack{\text{physical} \\ \text{surface}}} J_n(R_s) ds + \int_{\text{contact}} J_n ds - \int_{II} (G - R) d\Omega$$

We also know from Kirchoff's current law that the total current flowing into region I has to flow out the contact

$$J_{TI} = J_{p,II\rightarrow I} + J_{n,II\rightarrow I}$$

$$J_{TI} = \int_{\substack{\text{contact}\\ \text{in N+}}} J_p ds + \int_{\substack{\text{physical}\\ \text{surface in I}}} J_p(R_s) ds + J_{n,III\rightarrow II}$$

$$+ \int_{\substack{\text{physical}\\ \text{surface in II}}} J_n(R_s) ds + \int_{\substack{\text{contact}\\ \text{in p}}} J_n ds - \int_{I\&II} (G-R) d\Omega$$

We notice that there has been an assumption of current direction throughout. TRAN2D defines as positive current, that which is flowing from the outside world into a contact over a p-diffusion. If it is actually the opposite way the current will come out negative. This then gives the current out of contact I, a similar equation gives the current out of III, and the sum has to be equal to the current going into contact II (cf. Fig. 41).

Note that majority carrier current densities are not computed anywhere in the algorithm. The boundary lines for regions I and II are user supplied. The program prints the defining boundaries on a doping density plot of the device. The one source of possible numerical instability is the $J_{n,III\rightarrow II}$ term. In order to insure numerical stability the user should check that the defining boundary for II remains in the p-diffusion. Of course, if the device were p-n-p, then the relevant current would be $J_{p,II\rightarrow III}$ and the boundary should remain in the n-diffusion. The program automatically selects the minority carrier current.

Results

The following two figures are plots of output from a TRAN2D run on a shallow emitter n-p-n transistor. The doping density and the geometry of the device were input from a SUPREM simulation done on one of the transistors fabricated by Bill Klaasen here at Purdue.

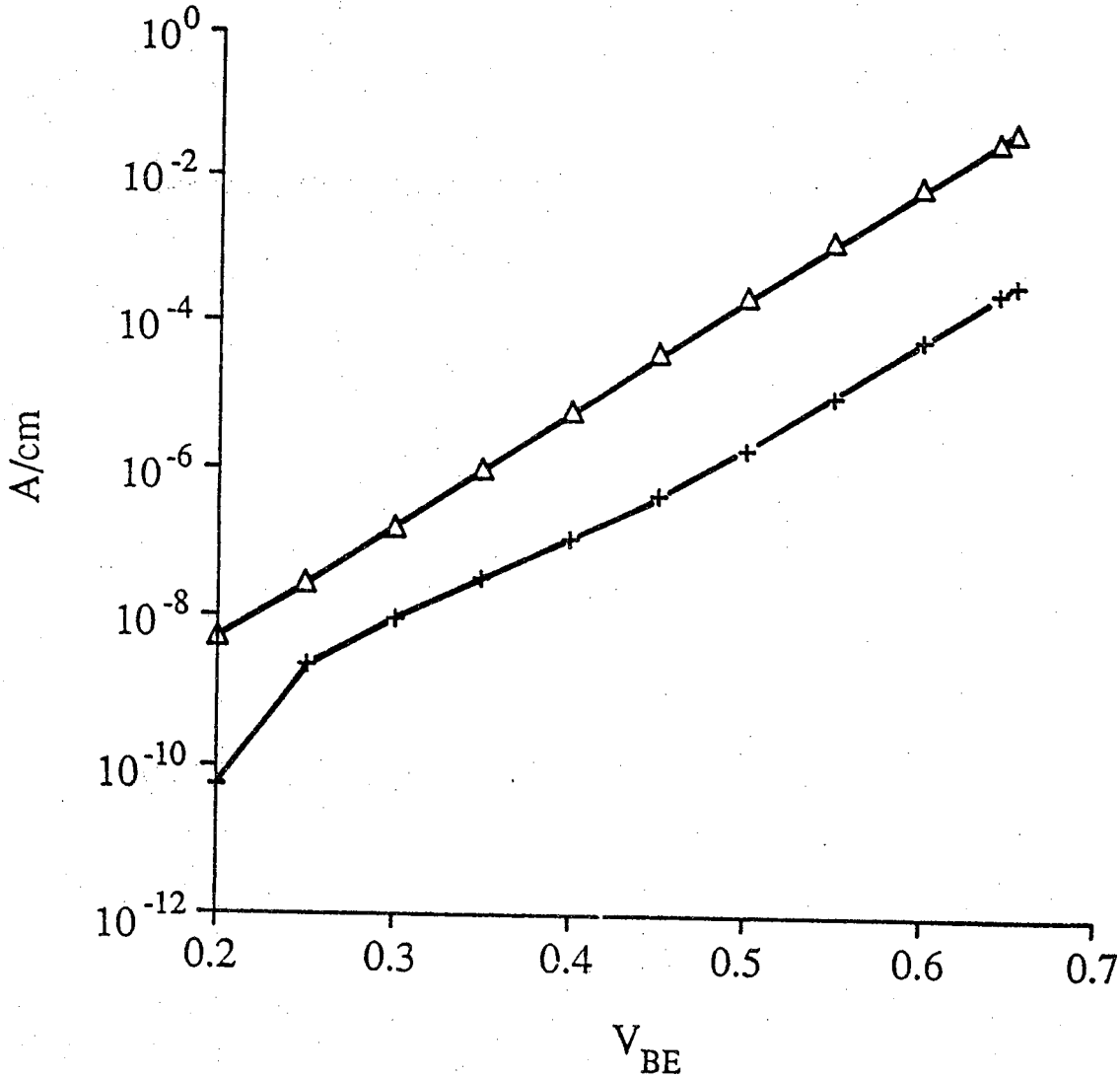


Figure 42

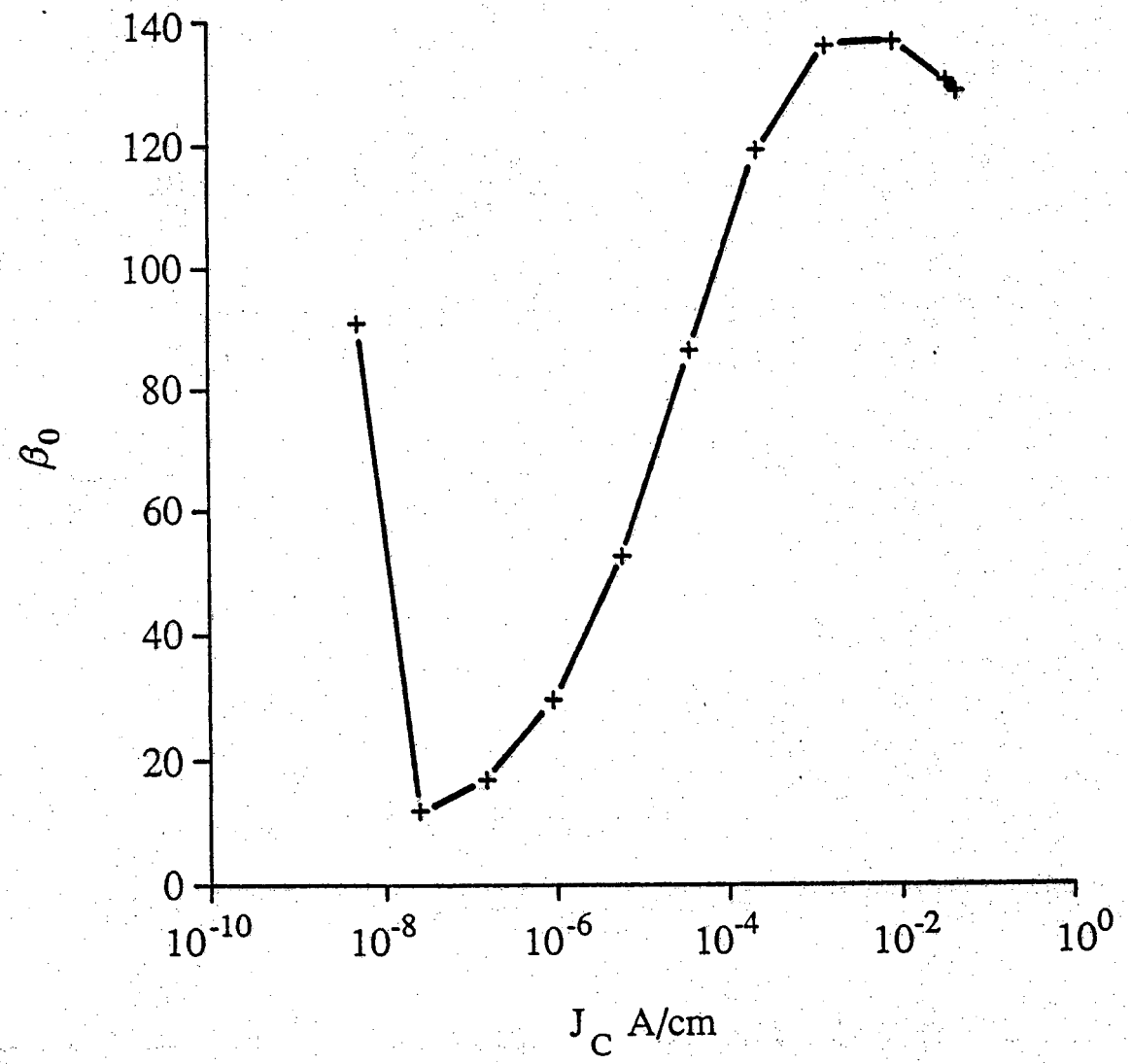


Figure 43

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IV. Proposed Research Goals for 1987

The goals expected to be completed in 1987, described below, are to be worked on by the co-principle investigators and two half time graduate research assistants. About half the effort will be in the fabrication of polysilicon emitter transistor structures and the other half on the computer simulations of regular and polysilicon emitter-contact bipolar transistors.

A. Fabrication

A fabrication process for producing heavily doped N^+ shallow As polysilicon on the N^+ doped emitter of a silicon bipolar transistor will be further developed. We call this structure a "poly contacted emitter". Now that we have completed the control transistor with a very shallow As emitter, reasonable leakage currents, good ideality factors, and betas of about 100, the next step is to investigate the polysilicon deposition methods and the effect of surface treatment before polysilicon deposition.

The fabrication procedures for producing and doping the polysilicon, at low temperatures, from amorphous silicon will be a key issue. Our approach will be to perform a second etch (a plasma etch) of the oxide window openings before the deposition of amorphous silicon to remove any native oxide at the surface, thereby creating a better, cleaner contact between the polysilicon and the N^+ shallow emitter. For the polysilicon contacted emitter structure the low temperature amorphous silicon should preserve the interface necessary for uniformity and greater beta enhancement. We will then further develop the process for fabricating regular and polysilicon-contact transistors to show the effects of a polysilicon on the peak beta and beta vs. I_C. Specifically we will dope the base heavier and measure the effect on Beta.

The regular and poly-contact transistors and processing test structures that have been fabricated will be measured for their electrical V-I characteristics will be measured using a Hewlett-packard 4145A Semiconductor Parameter measurement system. The beta vs. I_C plot, the V_{BE} vs. I_B and I_C plot are the main evaluation data peak Beta and the average of the peak beta will be emphasized. The measured data will be compared to similar results from the 2D simulations. It is expected that the close interaction between the simulations and the measured data will direct us to additional experiments.

B. Computer Modeling

As part of this continuation proposal, the 2D transistor code will be extensively tested to verify its accuracy and predictive capabilities. It is expected that, to insure the greatest possible accuracy, an energy balance equation will also need to be solved in conjunction with Poisson's equation and the continuity equations. This will improve the modeling of the transport properties, especially for small geometry devices. A further goal will be to include transient and small-signal sinusoidal steady-state analysis options in the code. This will allow a much more thorough analysis of device operation. In addition, the code will be modified to model both polysilicon contact and polysilicon emitter silicon bipolar transistors.

V. Defect Generation Study

A. Study of the Oxidation Stacking Faults and the Dislocation Generation at Si-SiO_2 Interface of Silicon

Studies show that if implantations (B, N, or P) at room temperature are followed by thermal oxidation, any extrinsic in micro-defects are expanded into large dislocations and stacking faults. These defects are large enough to be seen with an optical microscope, after chemical etching[1]. Oxidation creates an excess concentration of silicon interstitials at and near the Si-SiO_2 interface. These interstitials "plate out" on any micro-defect (nuclei), forming a stacking fault. Implantation provides defect nuclei which will grow when fed by a high concentration of silicon interstitials. These defects can degrade device performance. To avoid these defects, the recommended procedure is to anneal the wafer in neutral ambients (e.g., N, Ar) and then follow with any necessary oxidation. The following topics will be discussed.

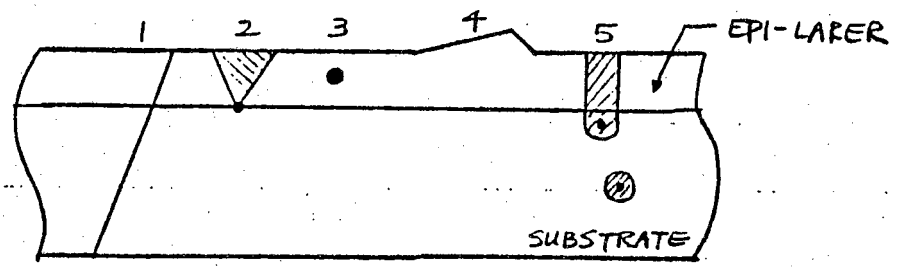
- Epitaxial Defects
- Oxidation-Induced Stacking Faults
- Influence of Oxidation-Induced Stacking Faults
- Experimental Results About Oxidation-Induced Stacking Faults and Dislocations
- Role of sequential annealing, oxidation, and diffusion upon defect generation in ion-implanted silicon surfaces
- Methods to avoid these defects.

Epitaxial Defects

The crystal perfection is a function of the properties of the substrate wafer and the epitaxial process itself. Defects arising from the substrate wafer can be related to the bulk properties of the wafer or its surface finish. Common defects occurring in epi-layers are shown in Figure 44.

Process-related defects include slip and impurity precipitates from contamination (item 3). Slip is a displacement of crystal planes past each other as the result of stress. Dislocations accompany the formation of slip. Contamination from the susceptor and the tweezers used in wafer handling also contaminate the epitaxial layer and substrate forms precipitates that act as defect nuclei in subsequent processing[2].

In general, the quality of the epitaxial deposit is strongly related to the quality of the substrate wafer, its cleaning, layer growth rate, and temperature[5]. For example, as the deposition temperature is lowered, minor flaws in the substrate surface act as points of preferential nucleation giving rise to stacking faults and pyramids. Higher



1. line (or edge) dislocation initially present in the substrate and extending into the expitaxial layer.
2. an epitaxial stacking fault nucleated by an impurity precipitate[1][2] on the substrate surface.
3. an impurity precipitate caused by epitaxial process continuation
4. Tripyramid, hillock, or other growth feature which can be related to the process[3] or the surface finish of the wafer.
5. bulk stacking faults one of which intersects the substrate surface thereby being extended into the layer.

Figure 44. Epitaxial Defects

growth rates at low temperatures aggravate the problem even further.

Another class of defects are misfit dislocations caused by lattice mismatch when the substrate is highly doped[7]. The resultant strain between the layer and substrate is relieved by the formation of dislocations.

Oxidation-Induced Stacking Faults

1. Mechanism of Oxidation-Induced Stacking Faults

Thermal oxidation of silicon can produce stacking faults lying on (111) planes. These planar faults are structural defects in the silicon lattice that are extrinsic in nature and are bounded by partial dislocations. The growth mechanism generally invoked involves the coalescence of excess silicon atoms in the silicon lattice on nucleation sites such as defects grown during crystal growth, surface mechanical damage present prior to oxidation, chemical contamination, or defects referred to as "saucer pits" or "hillocks". As a result of the oxidation process, especially at high temperature, it is believed that excess interstitial silicon is present near the Si-SiO_2 interface due to incomplete oxidation at the interface. This interstitial silicon supersaturation in the silicon determines the stacking fault growth rate[8], causing fault formation by nucleation at strain center in the bulk.

The growth of oxidation-induced stacking faults is a strong function of substrate orientation, conductivity type, and defect nuclei present. It is shown that the growth rate is greater for (100) than (111) substrates. Also, the density is greater for n-type conductivity than for p-type conductivity. Stacking fault length is a strong function of oxidation temperature[9]. For a given oxidation time, the size of the stacking fault first increases with temperature, reaches a peak at some temperature, and then decreases with temperature rather sharply until finally, the faults totally vanish. This is shown in figure 45. The figure shows two regions: a growth region and a retrogrowth region. In the retrogrowth region, stacking fault formation is suppressed while pre-existing stacking faults shrink.

In addition, both enhanced diffusion and stacking fault formation are more strongly affected by steam oxidation than dry oxidation. Typically the distribution of surface stacking fault lengths is very tight, except for an anomalous few percent which exhibit substantially greater lengths. Shorter-length stacking faults are usually bulk-nucleated stacking faults intersecting the surface. The length to depth ratio of the surface-oxidation stacking fault is approximately 3 to 10.

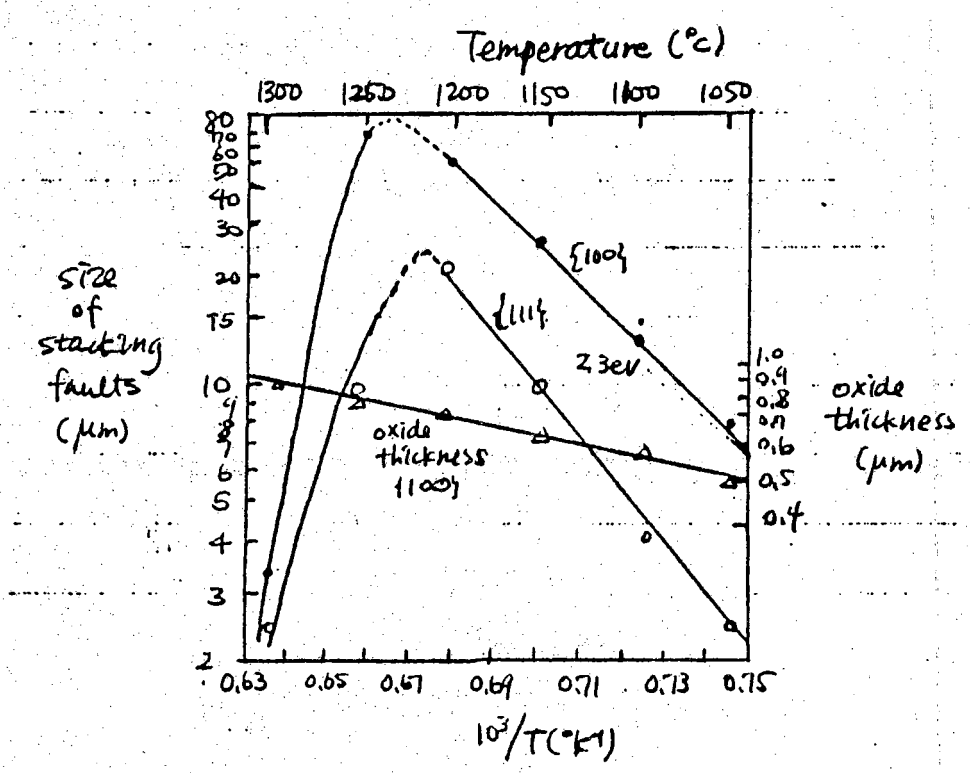


Figure 45. The growth vs temperature of oxidation stacking faults in steam for 1 hr.

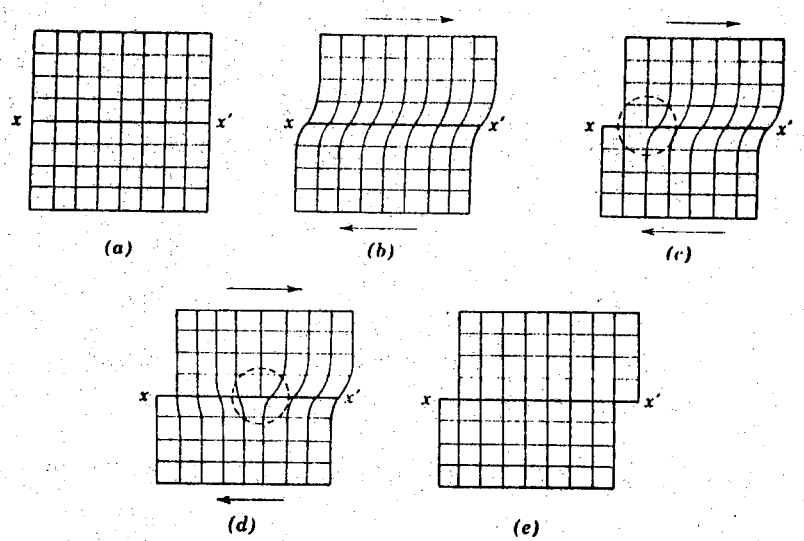


Figure 46. Defects

2. Influence of Oxidation-Induced Stacking Faults

The deleterious nature of oxidation-induced stacking faults is well known. Examples include degraded junction characteristics in the form of increased reverse leakage current; and storage time degradation in MOS structures. These problems occur when the stacking faults are electrically active as the result of being decorated with impurities, typically heavy metals. The decoration occurs both on the stacking fault itself and on the bounding dislocations. The dislocation, in particular, turn out to be favorable clustering sites because they represent a disarrayed high-energy region in the lattice.

The presence of decorated stacking faults in silicon has been shown to directly influence the reverse leakage characteristics of pn junctions[10]. The two possible interactions of a stacking fault with the p-n junction is shown[10] in the Figure 47. Since the junction is formed by the diffusion of boron into a surface covered with decorated stacking faults local contouring of the junction beneath the stacking fault can occur as shown in Figure 48. The presence of precipitation at the fault (possibly SiO_2 precipitates) can retard the diffusion front by directly blocking the boron atoms from diffusing. The effect is perhaps enhanced by the greater solubility of boron in the oxide precipitates. The accumulation of boron at the fault is also possible as a result of the differences in solubility of boron in the faulted and unfaulted regions of crystal, although this is probably a secondary effect. The curvature introduced in the junctions can result in excessive reverse leakage current.

In the event that the fault does not function as a block to the diffusion front, leakage can also be introduced in the junction due to the strain field associated with faults as shown in Fig. 48. Elastic strains have been demonstrated to generate leakage currents in p-n junctions. The precipitation at the fault results in strong electric fields in the lattice owing to different specific volume of the precipitating phase (SiO_2) as compared to that of silicon. These strains can extend to considerable depths into the bulk of the material and interact with the depletion field of the junction.

Much evidence of activity has been noted at the corners of the triangles formed where the defect penetrates through to the surface. This is most probably the result of impurity segregation at these points of stress concentration[11]. Since the fault size and the distribution of segregated impurity in the fault are interrelated, the electrical activity is obviously related to both these factors.

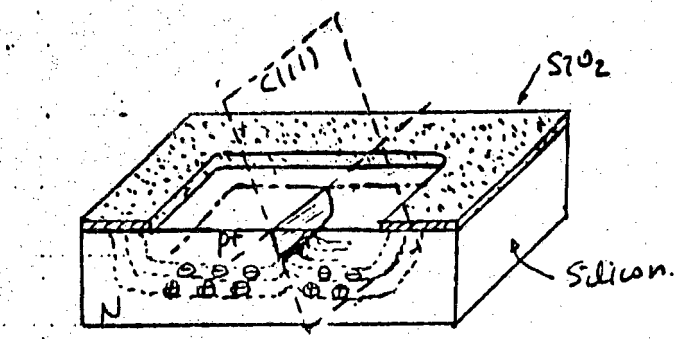


Figure 47

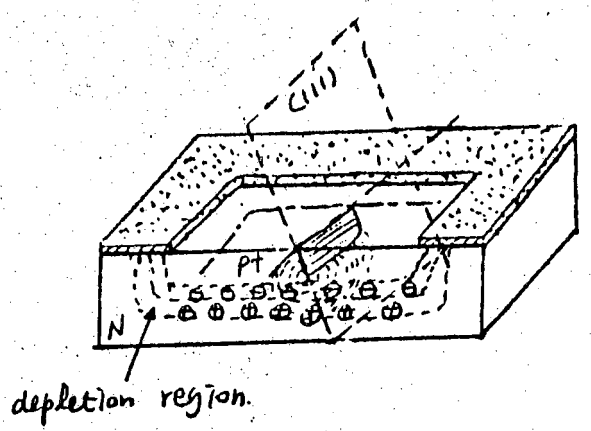


Figure 48

3. Experimental Results

Two different {111} oriented n-type wafers were examined for oxidation-induced stacking faults and dislocations. One was a 4" wafer that was cut into 4 quarters to be examined. This had an epitaxial layer on the Si-substrate. The other was a 2" wafer without an epitaxial layer. Their resistivities were ranging from 2Ω-cm to 5Ω-cm.

The cleaning procedure is as follows:

i) 5—10 sec dip in BHF
ii) Fully rinse in DI(deionized)water } optional

iii) Clean in5:5, H_2O_2:H_2SO_4

iv) Fully rinse in DI water .

The wafers were then oxidized (H_2 burn oxidation) at different temperatures ranging 900 ° C to 1100 ° C.

The Wright etch was performed after the oxidations. This particular etching method was used because the Wright etch[10] is known to work best for {111} oriented wafers. The composition of this etch is as follows: 60 ml concentrated HF(49%), 30 ml conc HNOS(69%), 30 ml of 5 M CrO_3 (lg CrO_3/2ml H_2O), 2g Cu $(NO_2)_2 \times 3H_2O$ (reagent grade), 60 ml conc. acetic acid (glacial), and 60 ml H_2O (de-ionized). In mixing the solution, the best results are obtained by first dissolving the $Cu(NO_3)_2$ in the given amount of de-ionized H_2O; otherwise the order of mixing is not critical. The wafer was etched with manual agitation for the desired length of time. The etch rate is slower compared to the Sirtl Etch and provides better etch control.

Several 2" wafers were oxidized at different temperatures for different length of time. After the Wright etch was performed, the results showed oxidation-induced dislocations but no stacking faults. The number of dislocations showed an increase with temperature. This relation is similar relation that of the growth vs. temperature of oxidation stacking faults described in S. M. Hu's result[9]. The results show the number of dislocations also increase with length of oxidation time. From this oxidation at 1000 ° C for 10 hours doesn't seem to induce a noticeable number of dislocations.

The 4" wafers had to be cut into 4 quarters to be processed. They are cut with a diamond scribe and hence, they show a large number of dislocations on the cut edges after the Wright Etch. Another wafer cut with a mechanical saw showed less dislocations on the cut edge. An accidentally cracked wafer (into big chunks) showed even fewer dislocations. These result lead us to cut the wafers with the mechanical saw instead of a diamond saw, with care, whenever necessary. One piece of wafer showed anomalous number of stacking faults which seemed to have some from the tweezer

marks.

Careful performance of the process can eliminate or minimize the stacking-faults and dislocations generated during process. Also, there are several methods suggested to suppress the stacking fault formation while pre-existing stacking faults shrink.

B. Role of Sequential Annealing, Oxidation, and Diffusion Upon Defect Generation in Ion-Implanted Silicon Surfaces

In bipolar device processing, we normally use ion implantation as a means of obtaining the uniform and reproducible deposition of electrically active impurity atoms. This is followed by high-temperature heat treatments which result in the redistribution of these deposited atoms. Such heat treatments will include the oxidation of the silicon surface as well as the diffusion of additional chemical species. The interaction of these heat treatments with the radiation defects introduced by the prior ion implantation, can play an important role in determining the methods of ion implantation for use in bipolar device fabrication.

According to the results of the experiments done by S. Prussin[12], when ion implantation of boron was substituted for the chemical deposition of boron, the n^+p^+ test diodes were found to exhibit excessive reverse leakage currents while the p^+n test diodes behaved normally. This was attributed to the defect structures developed by the interaction of sequential diffusion with defect nuclei introduced by ion implantation. It was found that the low-temperature annealing treatments, which are used to return full electrical activity to the implanted atoms, leave a high density of defect nuclei in the implanted area. When the silicon surface is subjected to wet oxidation, these defect nuclei expand to form stacking faults or dislocations of such a size that they can be detected by chemical etching and optical microscopy.

1. Experiments of Ion Implantation in Bipolar Devices

The wafers used were <111> oriented, 2" diameter wafers. They were boron doped to a resistivity of 2Ω-cm to 5Ω-cm and were dislocation free as determined by Wright etching. They were cleaned by H_2O_2:H_2SO_4 (50% : 50%) solution and rinsed in DI (de-ionized) water several times to make sure the wafer surfaces are clean. Then, four wafers were oxidized for 20 min at 1000 ° C for implant masking purposes. After opening windows in the oxide (two for base windows, the rest for emitter windows), boron and arsenic were implanted on those wafers with different doses and energies. The implant was carried out at room temperature with the ion beam normal to the wafer.

The other two wafers had both base and emitter impurities implanted into their windows. They were made that way in order to look at the effects of the implant on

the wafers close to our actual BJT devices. The doses and energies were also varied similar to the first four.

After the implantation, ay were given the burn oxidation at 1100 ° C for 1h, resulting in an oxide thickness of approximately 6000 Å. This step was effective in expanding defect nuclei present in ion-implanted or in ion-implanted and annealed wafers to a size that permitted study by optical microscopy the Wright etching for 10 min., the implanted reference areas were checked each time the adjacent implanted area was examined.

2. Experimental Results

Table 1 lists the defects developed by the H_2 burn oxidation for 1h at 1000 ° C followed by a Wright etch for a comparison of the different in procedure.

Table 1. Structures resulting from oxidation of ion-implanted surfaces.

No.	Window open	Oxide layer	Implant species	Dosage (atoms/cm^2)	Emerge (Kd)	Defect
A1	Base	No	B	2×10^{15}	50	many D.L. on thick oxide area
A2	B	No	B	2×10^{13}	25	None
B1	Emitter	No	As	1×10^{15}	25	few S.F. & D.L.
B2	E	No	As	1×10^{15}	25	few S.F. & D.L.
C1	B,E	~400Å	B,As	1×10^{13},6×10^{15}	35,35	some D.L. on base area
C2	B,E	~400Å	B,As	2×10^{13},1×10^{15}	25,25	few D.L.

Samples B_1 and B_2 had exactly the same conditions except that B1 had an annealing in N_2 at 550 ° C for 10 min. It seemed that the annealing didn't have much of an effect on reducing (S.F.) stacking faults
or (dislocations) D.L. The stacking faults and dislocations from B_1 and B_2 seemed to come from surface damage caused by the As ion implantation.

Many dislocations on the thick oxide area of A1 might have come from the stabilized defect nuclei of implanted impurity which penetrated through the masking SiO_2; which probably was not thick enough to mask the implanted B with 50 KeV. If parts of these impurities, particularly boron, are implanted into the Si-SiO_2 interface, they can easily become the nuclei for dislocations or stacking faults.

3. Discussion

The requirements for shallow junctions for n^+ layers are rather easily met by the implantation of As. Arsenic has a very shallow range implant Rp(~300Å) while using a convenient implantation energy, 50 KeV. If a shallower junction is desirable, smaller energy can be used without an oxide layer, even though it may cause surface damage. The heavy ion species results in an amorphous layer, so low-temperature solid phase epitaxy can be used to produce a doped layer without appreciable atomic diffusion. If necessary, the arsenic layer can be annealed at 900 ° C with very little diffusion.

The lowest practical energy for obtaining high beam currents for implantation is 25 KeV or 30 KeV. With these low energies, the surface damage can be minimized so that dislocations or stacking faults caused by implantation can be minimized. It is important to make sure that the masking SiO_2 is thick enough.

Boron diffusion occurs partly by the interstitially mechanism, so that enhanced diffusion effects are observed with this dopant. Arsenic, on the other hand, diffuses in silicon by a purely substitutional mechanism, so that enhanced diffusion behaviour is not observed. There are several ways to minimize, reduce, or eliminate stacking faults or dislocations induced by ion-implant, oxidation, or diffusion processes. They are discussed in the next following section.

C. Study of Elimination of Stacking Faults

There are several ways suggested to eliminate stacking faults by several people. S. Prussin[12] investigated the effectiveness of annealing treatments in reducing ion-implant damage by using a two-step heat treatment. According to G. A. Rozgoni et al.[13] the gettering of the nucleation sites, whether they be process induced such as impurity precipitation or native to the original crystal growth such as vacancies or impurities, can be achieved by the controlled introduction of interfacial misfit dislocations on the back side of the wafer. Here, the dislocations interact with the stacking fault nucleation sites such that the nuclei diffuse from the active device side of the wafer to the line defects which are confined to within a few microns of the back surface. This is called a pre-oxidation gettering procedure (called POGO) and it prevents the formation and/or activation of stacking faults nucleation sites during oxidation. In this way the stacking faults and their possible device degrading influences can be eliminated at the start of a processing schedule. In addition, the gettering medium can be retained through all subsequent high temperature processing, thereby continuing to suppress the formation of stacking faults.

H. Shiraki[14] explained another way to eliminate stacking faults by clarifying the effects of HCl on the generation and expansion of stacking faults, which were produced from grown-in defects and surface mechanical damage. In his experiments, for

dry O_2 oxidation, stacking faults expanded with increasing oxidation time except for oxidation at extremely high temperature (>1200 ° C). For HCl oxidation, they generally expanded during the first stage of oxidation, reached a maximum and finally began to shrink. A complete suppression of stacking fault generation was observed for higher HCl concentrations. The elimination of grown-in defects occurred during HCl oxidation. It was considered that the suppression of stacking fault generation and expansion, and the elimination of grown-in defects, are considered to occur due to the interaction of these defects with vacancies which are produced on the silicon surface during HCl oxidation.

The method disclosed by T. Hattori and T. Suzuki[15] involves heating silicon wafers for a short period in a dry nitrogen atmosphere containing small concentrations of HCl and oxygen. This process results in the elimination of the oxygen-induced stacking faults generation during the subsequent oxidation without causing any problem like a nitrogen reaction, a pit formation, and a blotchy appearance on the silicon surface.

Another technique, developed by S. P. Murarka et al.[16], of eliminating oxidation-induced surface stacking faults involves heating clean silicon wafers in an inert or HCl-inert ambient in the same furnace where subsequent oxidation- wet or dry- will be carried out. Typical fault densities after oxidation, without in situ cleaning, are 1000-5000 and 50-500/cm^2 for n- and p-type wafers respectively. These numbers are reduced to 10-100 and 0 respectively when in situ cleaning is used. The details of the procedure is described in reference 16.

Approaches which have been shown to reduce the size, density, and leakage currents of (oxide-induced stacking faults) OSF include pre-oxidation back side gettering (POGO)[3], preoxidation inert gas anneal[16], high temperature dry oxidation[3], processing in low oxygen[12], or chlorine containing[14] atmospheres, and deliberately misorientation from low index planes. When the bipolar device shows high leakage currents, one of the above processes or any other better method will need to be applied. In any rate, performing fabrication with care will avoid unnecessary stacking faults or dislocations.

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VI. Gettering Study

1. Introduction

Small concentrations of impurities and defects can often have deleterious effects on the operation of silicon bipolar devices which lead to very poor yields. Even if the fabrication was done under completely contamination free conditions a number of process induced defects still limit the circuit yield. This problem has led to a number of studies over the past decade which have shown the ability of gettering operations in overcoming defect and contamination problems arising during device processing. The basic idea of gettering is to remove undesirable defects and impurities from the critical areas on the wafer where the devices are fabricated [1].

Defects and other types of contamination may effect the performance of devices by introducing energy levels within the forbidden bandgap of silicon, where they act as recombination-generation centers and traps. Metallic impurities can result in a direct, unwanted, and often unstable contribution to the electric field in the active area of the devices. These lead to the two major problems frequently encountered in processing; degradation of minority carrier lifetime, and increase in the junction leakage current [2].

2. Defects in Silicon

Table I consists of a brief listing of the defects most generally observed in silicon and their effects on device performance [1].

Table I - Defects in Silicon [1]

Defect	Origin	Influence on Material Properties	Influence on Device Performance
Stacking fault	Oxidation; Epi growth	Precipitation site; Affects diffusion profile	Junction leakage enhancement; Soft breakdown; Lifetime degradation
Dislocation	Mechanical or thermal stress; Mislit of dopant or impurity atoms; Swirl defects	Precipitation site; Affects diffusion profile; Slip lines	Junction leakage enhancement; Lifetime degradation; Current gain degradation
Oxygen impurity	Crystal growth; Oxidation	Precipitate formation; Origin of OSF; Donor formation	Junction leakage enhancement; Lifetime degradation; Donor concentration enhancement
Carbon impurity	Crystal growth	Precipitate formation; Origin of swirl defect; Origin of OSF	Junction leakage enhancement; Lifetime degradation
Metallic impurity	Crystal growth; Processing	Precipitate formation; Affects diffusion profile	Junction leakage enhancement; Lifetime degradation

2.1. *Stacking Faults*

Stacking-faults originate as grown-in defects during crystal growth. They can also form during (a) epitaxy, (b) ion-implantation, and (c) oxidation in IC processing. The sources of these excess atoms include supersaturated self- interstitials and self-interstitials created during the growth of oxygen precipitates, or silicon atoms generated by the formation of silicon dioxide at the wafer surface [3].

Stacking faults have been found to greatly enhance the recombination current, and by introducing locally enhanced electric fields they perturb the diffusion profile leading to excessive leakage currents. They have been found to be strongly affected by temperature and the ambient conditions. At temperatures greater than 1200 C°, stacking fault formation is suppressed and the existing faults shrink in size.

One particular kind of fault that has received much attention lately is oxidation-induced stacking faults (OSF). OSF density is directly proportional to the interstitial oxygen concentration, and for concentrations below $7x10^{17}/cm^3$ OSF's are also highly dependent on temperature, By choosing an appropriate temperature OSF can be completely annihilated.

An important point to note is that the degradation characteristics introduced by OSF's and stacking faults are not correlated to the faults themselves, but to the impurities which condense on these faults.

2.2. *Dislocations*

Dislocations are formed due to stresses in the silicon wafer which may arise due to mechanical deformation or thermal gradients in the wafer. They may also result due to stresses built up by oxygen precipitates or by the misfit of dopant atoms.

The primary effects of dislocations is to enhance junction leakage current and degrade minority carrier lifetimes. As was the case with stacking faults, these effects are caused primarily due to condensation of metallic impurities on dislocations.

Dislocations are very often created during the base drive-in in bipolar transistors, and are a result of stresses formed during the base diffusion. When the emitter is subsequently put in, phosphorus atoms preferentially diffuse along these dislocations formaing n-type "pipes" which short the emitter to the collector (Figure 44). This shorting drastically reduces the current gain in bipolar transistors [1].

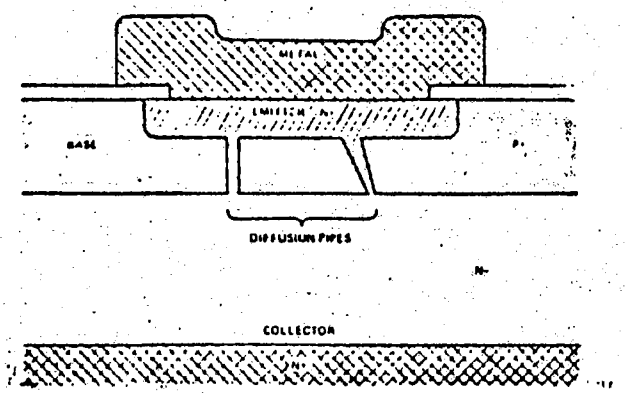

Fig. 49 - Diffusion pipes [1].

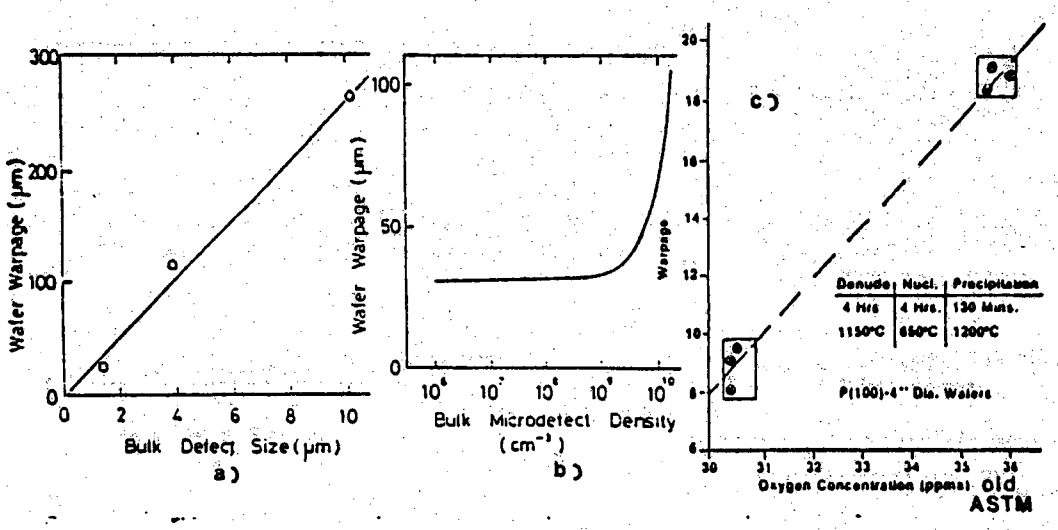

Fig. 50 —(a) Dependence of wafer warpage on bulk microdefect size. (b) Wafer warpage as a function of bulk microdefect density. (c) Effect of initial oxygen content of wafer on warpage. [17]

2.3. *Oxygen and Carbon impurities*

Oxygen and carbon are introduced into the silicon crystal during its growth from the ambient. Since this is a grown-in contamination there is not much control over the defect density that they generate. Oxygen is responsible for the formation of OSF's, while carbon introduces swrill defects into the silicon substrate. Hence, oxygen and carbon contamination lead to the enhancement of junction leakage current and degradation of minority carrier lifetime.

2.4. *Metallic Impurities*

One of the major sources of contamination in silicon wafers is that of heavy metals. The reason is because there are various sources that can give rise to this type of contamination; like the following:

(a) stainless steel fixtures in ion-implant machines that get sputtered during the ion implantation process,

(b) the diffusion of heavy metals from the heater coils through the quartz walls of diffusion furnaces,

(c) impurities originating from the sputtering of components of reactive ion-etching systems,

(d) release of transition metals by graphite susceptors of epitaxial reactors, and

(e) handling of silicon wafers with metal tweezers.

The electrical characteristics of metallic impurities depend on their location within the silicon lattice. Metal atoms can occupy either a substitutional or interstitial location in the lattice. They can also form precipitates by nucleating on other defects such as stacking faults, dislocations, or another precipitates. The behavior of metallic impurities lead to the introduction of energy levels within the forbidden bandgap of silicon, which act as recombination centers and result in a decrease in minority carrier lifetime and an increase in the junction leakage current.

3. Influence of Defects on Device Performance

As noted earlier, almost any kind of contamination or defect formation in silicon leads to an increase in the junction leakage current and a decrease in the minority carrier lifetime. We also noted the formation of n-type "pipes" due to preferential

diffusion along dislocations which leads to the shorting of the collector-emitter junction in bipolar transistors. Along with these the following effects also need special attention.

3.1. *Gate-oxide Quality*

Metallic contamination in the silicon substrate lead to the formation of oxidation-induced stacking faults during oxidation, which enhance the oxide leakage current, and lower the oxide breakdown voltage in MOS transistors. High surface defect density is also known to cause low breakdown voltages in thin oxides [1].

3.2. *Threshold Voltage Control*

One of the factors that determine the threshold voltage of MOS transistors, is the resistivity of the substrate. Due to limitations of the CZ growth process, the resistivity can vary from wafer-to-wafer. In addition, thermal donors from oxygen precipitates can significantly alter the carrier concentration in low resistivity material [1].

3.3. *Wafer Resistance to Warpage*

Warpage in silicon wafers is the introduction of stress in the lattice which destroys the planar form of the wafer. This happens when the wafers are cooled down to room temperature which lead to the formation of stresses in the wafer that cannot be relived by plastic deformation.

Warpage gets progressively worse throughout an IC process, and is most pronounced at contact and metal patterning. Among the various methods used to reduce warpage are edge rounding of wafers, improved polishing techniques for the wafer, and the suppression of micro-defects during crystal growth. Process optimization steps to reduce thermal stresses, such as slow push-pull of wafers into furnaces and ramping furnace temperature up and down, have also helped in reducing warpage (Figure 50) [17].

Table II is a brief summary of the effects that defects have on bipolar and MOS devices.

Table II - Influence of defect on Device Performance

Bipolar Devices	MOS Devices
1. Microplasma and junction leakage	1. Standby power increase in CMOS
2. Low junction breakdown voltage	2. Threshold voltage drift in static RAM's
3. Current channeling, such as emitter-collector shorts	3. More frequent refresh cycles in dynamic RAM's
4. Low current gain	4. Limitation to upper temperature use, due to generation-recombination currents, of both static and dynamic RAM's
5. Hot spots due to nonuniform power dissipation	5. Leakage in CCD memories and dark current spikes in CCD imagers

4. Gettering Techniques

As stated earlier, gettering is the removal of unwanted defects and contamination from the critical areas of the wafer where devices are fabricated. The impurities are either completely removed from the wafer or moved down further into the bulk area of the wafer where their influence is insignificant.

Gettering processes can be divided into two groups - extrinsic and intrinsic. *Extrinsic gettering* involves the use of external means to create the damage or stress in silicon the lattice that leads to the creation of extended defects or chemically reactive sites at which the mobile impurities are captured. *Intrinsic gettering* involves the localization of impurities at extended defects which exist within the bulk material of the silicon wafer, and whose origin is due to an "intrinsic" property of the starting wafer, such as its oxygen content acquired during CZ crystal growth.

Table III gives a brief description of the different types of gettering techniques and the defects they getter. Looking at the table one notices the distinctive use of one kind of crystalline defect to getter another. For example, backsurface damage is used to getter metallic impurities, excess vacancies created by chlorinated oxides getter stacking faults, and misfit dislocations act as condensation sites for metallic impurities and stacking faults.

4.1. Extrinsic Gettering Techniques

4.1.1. *Back-surface Damage*

This is basically mechanical damage produced on the backside of the wafer by abrasion, grooving, or sandblasting. The purpose of this damage is to introduce strains in the silicon lattice which form dislocations during subsequent annealing steps that act as segregation sites for impurities. The disadvantage of this technique is the introduction of dislocations and micro-defects which reduce the mechanical strength of the wafer and make it susceptible to warpage during heat cycles. As a result, this technique is now being replaced by ion-implantation gettering and laser-induced damage gettering techniques.

4.1.2. *Ion-Implant Induced Damage*

This type of gettering basically involves the introduction of arrays of defects into the silicon substrate which compete with native defects for interstitial atoms and

metallic impurities. Since defects expand under oxidation and diffusion conditions, extreme care must be taken as to where these defects are introduced on the silicon wafer. This is normally done on the backside of the wafer [3].

The effectiveness of ion species for implantation gettering was compared by Seidal, Meek, and Cullis. They found argon to be more efficient for gettering than silicon, oxygen, phosphorus, boron, and arsenic for equal doses [15].

A similar study was done by Beyer and Keh, who studied the effectiveness of argon, oxygen, silicon, and xenon in the presence and absence of a silicon-dioxide layer. They found that argon had a higher gettering capability as compared to the others. They found that when ions were implanted through a thin silicon-dioxide layer, considerable damage was produced at the silicon surface, and this contributed significantly towards gettering efficiency.

Singh, Fonash, and Rohtagi studied the impact of low energy implanted hydrogen ions on slow (Ti and V) and fast (Cr and Au) diffusing impurities. Their results indicated that only fast diffusing impurities could be effectively gettered by the hydrogen ion, which they attributed to the enhanced diffusivity of fast diffusing impurities created by hydrogen implantation (Table IV) [7].

A disadvantage of this technique is that high energy implants change the silicon surface to an amorphous condition, and hence we require a high temperature annealing step to restore the original state of the wafer surface.

4.1.3. *Laser-Induced Damage*

In principle this technique is similar to the mechanically induced damage, but is introduced by a cleaner and more controllable process. A high power laser beam is used to cause enough thermal shock to create dislocation nests in the irradiated region. These act as gettering sites, where the impurities segregate.

4.1.4. *Diffusion*

Heavy diffusion of either phosphorus or boron can generate misfit dislocations in the silicon lattice, which act as gettering sites for unwanted defects. Typically, diffusion gettering is done on the backside of the wafer before any device processing.

Lecrosnier, Paugam, Ricjor, and Pelous showed that a low temperature phosphorus diffusion can efficiently getter gold even when dislocations are not induced, the critical parameter being the surface concentration of phosphorus (Fig.3) [10].

Table III

Technique	Gettered Defects	Application
Back surface abrasion	Metallic impurities Stacking faults	Preprocess (back surface)
Laser induced damage	Metallic impurities Stacking faults	Preprocess (back surface)
Ion implant induced damage (Ar, O, P, As, B, etc.)	Metallic impurities Stacking faults	Preprocess (back surface)
Intrinsic gettering (oxygen precipitates and dislocations)	Metallic impurities Stacking faults	In-process
Chlorine oxidation (HCl, Cl_2, C_2HCl_3, etc.)	Metallic impurities Stacking faults Oxygen	Preprocess or In-Process
Phosphorus diffusion ($POCl_3$) or Boron Diffusion (BN, BBr_3)	Metallic impurities Stacking faults Dislocations	Preprocess (back surface) or In-process (front surface)
Film deposition (nitride, silicide, etc.)	Metallic impurities Stacking faults Dislocations	Preprocess (back surface) or In-process (front surface)
Annealing	Stacking faults	Preprocess or In-process

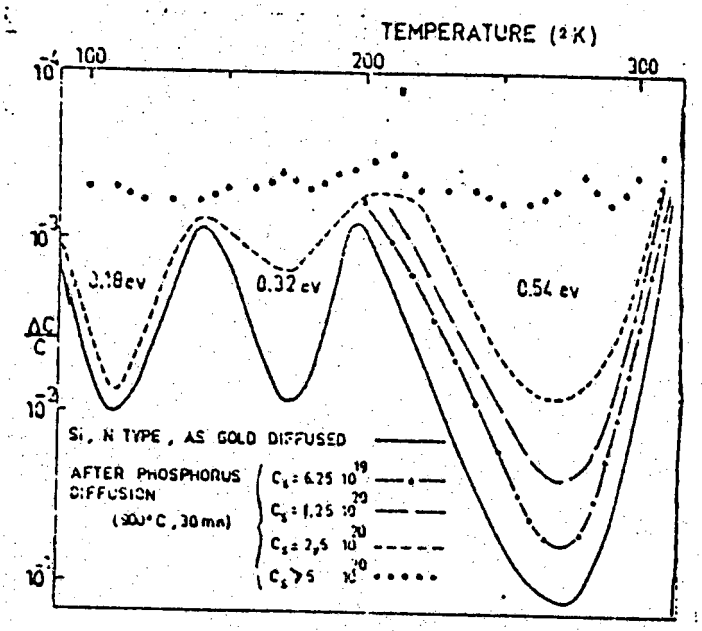

Fig. 51 *DLTS spectra obtained on gold-doped samples gettered with phosphorus diffusion. [10]*

Phosphorus getters nickel in silicon by the formation of SiP particles at the Si/phosphosilicate glass interface, which emit a large concentration of silicon interstitials which getter nickel by forming $NiSi_2$ particles at the interface [12].

A disadvantage of this technique is that large amounts of phosphorus on the wafer backside can contaminate epitaxial layers as a result of auto-doping.

4.1.5. *Chlorine Oxidation*

Chlorine has been found to annihilate stacking faults when silicon is oxidized in an oxygen ambient which contains a certain percent of HCl, C_2HCl_3, or $C_2H_2Cl_3$. Among the theories that explain this phenomena is one that suggested an excess number of vacancies is created at the interface, and that these vacancies diffuse into the silicon annihilating the atoms comprising of stacking faults. Another theory suggested that the out-diffusion of the extra silicon atoms due to a reduction in the silicon interstitial concentration at the oxide-silicon interface led to the shrinkage of stacking faults [1].

It has been found that oxidation in presence of chlorine gegger metallic impurities, which leads to an improvement in the minority carrier lifetime. Baginski and Monkowski showed in their work the differences in the ability of chlorine to getter different metals. They found that copper could be easily removed by the addition of 3% to 10% HCl to the O_2 ambient, whereas gold was not affected significantly. They attributed this behavior to the existence of a volatile copper chloride and the lack of any stable gold chloride at the temperatures used in their study [13].

4.1.6. *Film Deposition*

Film deposition on the backside of wafers produces stress in the silicon lattice and can be effectively used as a gettering mechanism. Silicon nitride and Boron silicide films have been successfully used. Polysilicon deposition has been found to be very effective. The grain boundaries, and high degree of disorder in polysilicon act as a sink for mobile impurities [17].

Chen and Silvestri compared the effectiveness of polysilicon, silicon nitride, and a combination of polysilicon/silicon nitride films as getterers. They found the polysilicon/silicon nitride combination to be the most effective. Table IV is a brief summary of their results [9].

Table IV - MOS retention time data obtained by Chen & Silvetri [9].

Areas	(1)	(2)	(3)	(4)
Gettering arrangement	Poly-Si	Poly-Si plus Si_3N_4 (700Å)	Si_3N_4 (700Å)	None
Total No. of devices measured	69	47	48	55
Yield:* $T_R \geq 1$ sec	62.3%	76.6%	35.4%	23.6%
$T_R \geq 5$ sec	53.6%	72.3%	22.9%	12.7%
$T_R \geq 10$ sec	49.3%	68.1%	20.8%	7.3%
$T_R \geq 60$ sec	30.4%	51.1%	12.5%	1.8%
$T_R \geq 100$ sec	5.8%	29.8%	0	0
$T_R \geq 140$ sec	0	10.6%	0	0
Average T_R (sec), all measured devices	33.0	61.6	10.6	3.8
Devices with $T_R \geq 1$ sec only	52.9	80.4	30.7	15.8

* Yield means percentage of total number of measured devices with retention time $T_R \geq t$ sec.

4.1.7. *Annealing*

Annealing has been found to reduce oxidation-induced stacking faults in an ambient consisting of either H_2, Ar, or N_2. At higher temperatures the shrinkage occurs at a greater rate, and at all temperatures N_2 is most effective than either H_2 or Ar. Another important use of annealing is in intrinsic gettering as will be discussed in the following section.

Even though a lot these techniques are very effective in gettering impurities, the primary limitation of intrinsic gettering is its instability at high temperatures which results in the dissolution of the gettered metal back into the wafer and the annealing out of dislocations. This limitation is the reason for extensive investigation of intrinsic gettering as a complementary gettering technique.

4.2. Intirnsic Gettering Technique

The basic idea behind this technique is the precipitation of supersaturated oxygen in silicon wafers which form clusters within the wafer during thermal processing. As these clusters grow in size with temperature, they can be relieved by punching out dislocation loops. These dislocations become sites at which impurities can be trapped and localized.

The advantages that this technique has over *extrinsic* gettering are as follows:
(a) the wafer is not subjected to any external damage other than heating,
(b) the entire bulk of the wafer now acts as a sink for impurities, and
(c) the gettering region is now much closer to the region where devices are built, as a result the impurities have to travel a very short distance before getting trapped.

The implementation of this technique is based on the requirement of a minimum concentration of oxygen in the starting wafers. The lower level on this concentration limit is there to initiate precipitation, and this is typically not a problem because the oxygen concentration in CZ grown wafers is higher than this limit. The upper limit is there to prevent the formation of very high density of precipitation which may lead to wafer warpage and dislocation generation near the active devices. Assuming that the initial oxygen requirement is met, intrinsic gettering can be achieved by a sequence of three temperature cycles.

The first step is a high temperature step (1100 - 1200 ° C, 30 - 240 min.), which causes the oxygen near the top and bottom of the wafer to diffuse out leaving behind a region of low oxygen concentration. This region is called the *denuded zone,* and the step is called *denuded zone formation.* Nitrogen and argon have been suggested as appropriate ambient gases, but oxygen is particularly helpful for high temperatures ($>$ 1200 ° C) to avoid pitting.

The second step is a low temperature step (600 - 800 ° C, 4 - 64 hrs), which causes the interstitial oxygen in the wafer bulk to from the nuclei required for the subsequent precipitation and gettering events of the next step.

Finally, the third step is a high temperature process (900 - 1250 ° C, 4 - 16 hrs), which causes the clusters formed in the previous step to grow in size. The growth of these clusters lead to the formation of dislocation loops, which function as the desired gettering sites (Fig. 52) [17].

Intrinsic gettering helps to reduce material slip, s-pit formation, p-n junction leakage current, and improves MOS generation lifetime.

Now that we have discussed the various gettering techniques used today, stated below are some of the developments in these techniques.

As mentioned earlier, metallic impurities in silicon is one of the major problems faced today. A large portion of these impurities are introduced during the high temperature furnace operations during device fabrication. In his paper, Schmidt has discussed the furnace contamination problem and its remedies. Among the various solutions suggested are the use of furnace liners, single-wall and double-wall quartz furnace tubes, silicon furnace tubes instead of quartz, high purity silicon carbide tubes, and a linerless furnace operation technique [4].

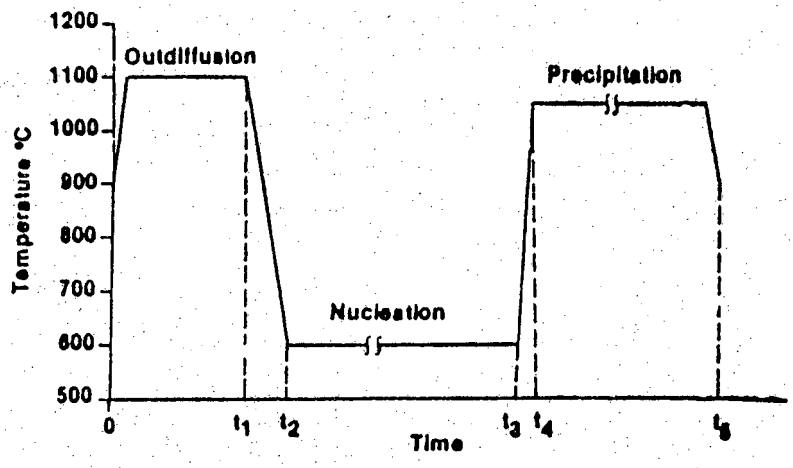

Fig. 52 - Three step thermal cycle to obtain intirnsic gettering [17].

Ward in his paper related the low circuit yield in shallow, ion-implanted bipolar process to the presence of iron rods in the emitters of transistors. The source of this contamination was found to be the unprocessed wafers as supplied by the manufacturer, which had an iron concentration of almost 1 ppmW [6]. Bailey, Bowling, and Bean discussed how intrinsic gettering could be successfully used to control excessive carbon and oxygen concentration in silicon wafers [11].

Finally, it should be noted that no one gettering technique can result in optimum results. The effectiveness of any technique is dependent on the type of impurity and the type of process being used. Many times, a combination of different techniques may give optimum results. Schmidt, Katz, and Pearce found a three step gettering process to be very effective in gettering impurities. The three steps consisted of laser-induced damage (LID) on the back surface of the wafer, a modified high temperature HCl treatment, and formation of oxygen precipitates in the bulk of the wafer [15].

5. Conclusion

As the constraints on VLSI circuits kept getting tighter and tighter, many different gettering techniques have been developed over the past years, and this effort will continue on in order to obtain yet better methods. It is due to the extensive attention given to this process that we have been able to overcome some of the serious limitations of silicon devices, and today gettering has become an indispensable process step in device fabrication.

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VII. Conclusions

The results of wafer set "V" runs show that the shallow Arsenic emitter (0.05 μ) and the very narrow base width (0.1 μ) control devices with metal emitter contacts have an average peak beta of about 75. Poly contacted emitter devices fabricated at the same time on the same wafer show a beta enhancement to 232, a factor of about 3.0 in the average peak beta. The polysilicon was deposited in a standard way, in a LPCVD tube. We are presently fabricating polysilicon devices for studying the effects of the methods used in treating the surfaces before the poly is deposited and the way the poly is formed (amorphous PELPCVD).