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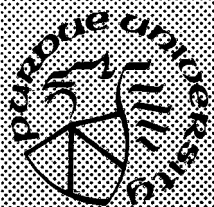*Purdue University*

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ABSTRACT

Schwartz, Stephen Sylvester. Ph.D., Purdue University, May 1985. Zinc Oxide-on-Silicon Surface Acoustic Wave Devices. Major Professor: Robert L. Gunshor.

A monolithic ZnO-on-silicon surface acoustic wave (SAW) memory correlator has been fabricated which utilizes induced junctions separated by ion implanted regions to store a reference signal. The performance characteristics of this device have been investigated including storage time, dynamic range, and degenerate convolution efficiency. Verification of the existence of charge storage regions is possible prior to completed device fabrication.

A theory explaining the charge storage process is developed and applied to the implant-isolated storage correlator. The implant-isolated correlator theory is applied to related structures which employ slightly different storage mechanisms. The ion implanted correlator is used to determine the wave potential associated with a propagating SAW.

Characteristics of ZnO-on-Si SAW resonators with sputtered ZnO films limited to the interdigital transducer (IDT) regions are investigated. Upper limits on propagation loss for surface waves on silicon substrates are determined by employing externally coupled limited ZnO SAW resonators. Resonator Q-values are enhanced by restricting the lossy ZnO area and predictions are made as to achievable Q-values for resonators fabricated in the externally coupled configuration. Experimental results for limited ZnO, internally coupled ZnO-on-Si resonators are also given.

A complete theory for the mode conversion resonator is presented which predicts the array separation for proper device operation. The theory also gives way to a special condition for spatial independence of resonator output with respect to IDT placement. Mode conversion resonators are fabricated which experimentally verify these predictions.

CHAPTER 1

INTRODUCTION

The introduction of surface acoustic wave (SAW) devices has permitted the performance of many signal processing functions on the surface of crystals which previously required unwieldy waveguides and microwave structures. Because surface acoustic waves propagate at velocities of the order of 10^5 times slower than electromagnetic waves at the same frequencies, signal processing functions in the UHF-VHF range involving many rf cycles can take place on a very small area of the substrate. Single crystal piezoelectric materials such as quartz, $LiNbO_3$, and GaAs permit the transduction between electrical and acoustic microwave signals. The excitation of surface acoustic waves has also been demonstrated on non-piezoelectric substrates through the use of piezoelectric thin films deposited on their surfaces. Boundary conditions imposed by the surfaces of these material configurations support surface acoustic wave modes (Rayleigh waves) which propagate with wave energy confined to within roughly one wavelength of the surface. In the layered medium case, where the piezoelectric film thickness is much less than a wavelength, most of the wave energy is in the silicon substrate.

Signal processing capabilities afforded by SAW devices include delay functions[1,2], filtering[3,4,5], and SAW resonators[6,7,8,9,10]. Furthermore, when used in conjunction with semiconductors, these devices can be used to perform

such functions as convolution[11,12,13], correlation[14,15,16], parametric amplification[17], and optical imaging[18]. Although some of these operations are possible using bulk waves, it is the ability to alter, reflect, and sample waves at the surface of the material which allows most of the functions to exist.

In this report we are concerned with a variety of SAW devices which use a thin rf sputtered piezoelectric ZnO film atop thermally oxidized silicon substrates for wave excitation. It is important to note that despite the need for only very thin ZnO layers for SAW excitation, the piezoelectric has a significant effect upon the wave velocity, dispersion, and coupling level. An exhaustive study of these properties of wave propagation in the layered medium has been undertaken by several authors[19,20,21]. In this work we utilize the results of their investigations in the fabrication of several devices.

The layered configuration, shown in Fig. 1.1, consists of a silicon substrate which has been thermally oxidized. The oxide layer, which is an excellent surface on which to grow well oriented ZnO films (necessary for high electromechanical coupling), serves to passivate the substrate and to isolate the silicon from the semiconductive ZnO film. In addition, it has been shown that by controlling the SiO_2 thickness, one can make SAW resonators which are temperature stable over a wide temperature range[22]. The piezoelectric ZnO film permits not only the excitation of surface acoustic waves, but it allows one to capitalize on SAW-semiconductor interactions. Because of the ZnO layer, an acoustic wave has a propagating electric field associated with it which penetrates into the underlying silicon substrate through the thin SiO_2 layer, thereby enabling one to take advantage of the nonlinear effects of the semiconductor. More about this later.
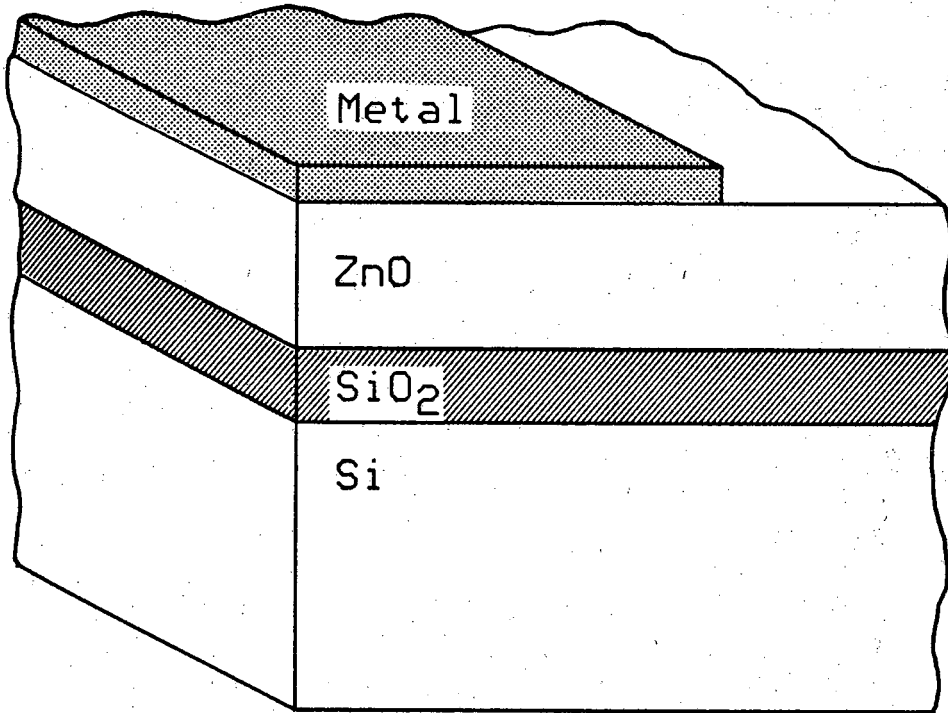
Figure 1.1

The layered MZOS configuration.

The layered $ZnO/SiO_2/Si$ configuration has been a starting point for many signal processing devices. The attractiveness of the composite structure is that it allows one to fabricate rugged monolithic devices capable of being integrated as on-chip components as part of an existing silicon technology. In this report we present results associated with a new monolithic SAW storage correlator and several resonator configurations, all fabricated in some form of the ZnO-on-Si composite structure.

1.1 Research Summary

Common to all devices in the layered $ZnO/SiO_2/Si$ structure, are the use of interdigitated metallization patterns placed either on the top or lower surface of the ZnO layer, for SAW excitation. Interdigital transducers (IDT's), as they are known, are the most efficient means for exciting surface acoustic waves and an understanding of IDT operation is essential in the design of SAW devices. We discuss transduction in the layered medium in the next chapter.

As mentioned above, surface acoustic wave devices, when fabricated in conjunction with a semiconductor, enable one to exploit the nonlinear interactions between semiconductor charge carriers and the electric fields associated with acoustic waves to perform many signal processing tasks. These devices are useful in that the real time multiplication of signals can take place to yield both the convolution and correlation of two signals. A storage correlator is a device which is capable of storing the replica of a reference signal as a spatially varying charge pattern. At some later time, while the reference signal still exists in the device, a "reading" signal is introduced which excites a surface acoustic wave whose envelope is the correlation of the stored reference signal and the applied reading signal.

In Chapter 3 we describe both the convolution and correlation processes which can be performed in SAW devices. Additionally, we review briefly the history of correlators and present results of a new surface acoustic wave storage correlator. Although signal storage in correlators has been demonstrated effectively through the use of surface states and diodes at the silicon surface, the implant-isolated storage correlator, presented in Chapter 3, is a device which utilizes induced junction storage regions which are isolated from one another by ion implanted regions. We present a theory for charge storage in the implant-isolated storage correlator which is based upon MOS fundamentals and we obtain excellent agreement with experiment. Our theory is used to predict accurately the behavior of a closely related pn diode correlator structure.

The new correlator is seen to exhibit long storage times, bias stability, and the promise for high dynamic range. Furthermore, the simple structure of the implant-isolated device enables one to determine, experimentally and analytically, the electrical potential associated with a propagating surface acoustic wave.

In addition to nonlinear acoustoelectric interactions available in SAW-semiconductor configurations, acoustic reflections alone are employed for many SAW device applications. Scattering of surface acoustic waves from short-circuited metal strips, isolated metal strips, and grooves etched into piezoelectric surfaces have been employed in the fabrication of SAW resonators, reflective array compression devices and, recently, a mode conversion resonator which exploits the conversion between propagating surface wave modes for its operation. The reflection mechanisms from the various reflector configurations on numerous piezoelectric materials have been studied in some detail. Our

interest lies in the reflections of surface acoustic waves from reflectors on the ZnO surface in the ZnO-on-silicon composite structure.

To date, SAW resonant cavities have been formed by placing reflector arrays opposite one another on the surface of the ZnO. Surface acoustic waves excited between the reflectors by an IDT are confined to the two dimensional area between reflectors. The resonant standing wave is then detected via another IDT. ZnO-on-silicon SAW resonators have been fabricated which utilize reflectors of metal strips, as shown in Fig. 1.2, but the most efficient reflectors are those made by ion milling grooves into the ZnO surface. Resonators fabricated with such reflectors have yielded Q values in excess of 12,000. Device Q's are limited by propagation loss associated with the lossy ZnO layer. Furthermore, attenuation due to the piezoelectric film is thought to increase as f^2. The frequency squared loss dependence would severely limit any practical applications for these devices at frequencies above a few hundred megahertz. As such, one focus of our research has been the design of SAW resonators on silicon with reduced propagation loss.

Results of our resonator studies, included in Chapter 4 of this work, deal with ZnO-on-silicon devices constructed in a variety of configurations to maximize efficiency for high frequency applications. We have fabricated externally coupled and internally coupled resonators with ZnO limited to transducer regions only. In addition to enhanced Q values achieved by restricting the ZnO area, we have minimized previous problems related to velocity dispersion and unnecessary radiation damage caused by sputtering. Furthermore, the limited ZnO devices allow one to predict the SAW attenuation for waves propagating in the SiO_2/Si configuration and on unoxidized silicon.

REFLECTOR ARRAY

TRANSDUCER

ZnO (1.6 μm)

AL (0.1 μm)

SiO_2 (0.1 μm)

n-Si

(111)-cut,

$<2\bar{1}\bar{1}>$ prop.
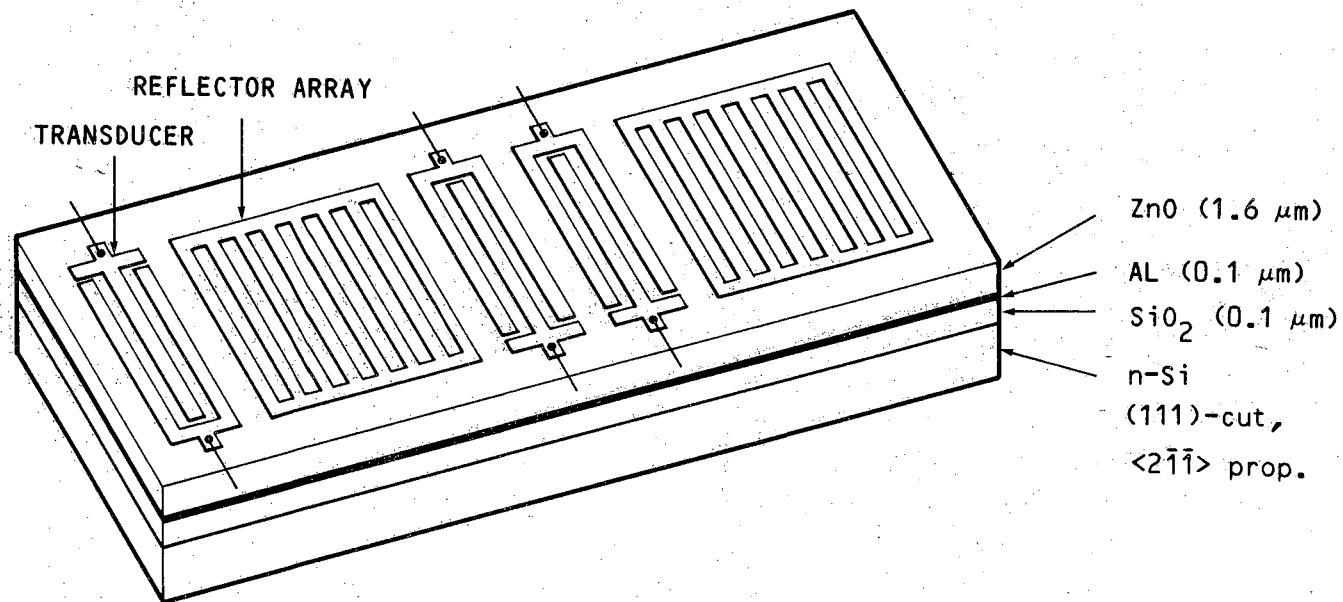
Figure 1.2

Schematic for a two-port $ZnO/SiO_2/Si$ SAW resonator employing electrically shorted metal gratings for reflector arrays.

The implant-isolated correlator of Chapter 3 and the resonators described in Chapter 4 are devices which utilize the first order Rayleigh mode of the ZnO-on-silicon layered configuration. When the ZnO layer is of sufficient thickness, one can excite not only the Rayleigh mode, but also the second order Rayleigh mode, also known as the Sezawa mode. The Sezawa mode has been employed in convolvers and correlators because of the large bandwidth capability afforded by its high electromechanical coupling. Recently, Melloch et. al[23]. observed the conversion between Rayleigh and Sezawa modes when propagating a surface wave through an array of strips or grooves with periodicity corresponding to neither the Rayleigh or Sezawa wave periodicity at the conversion frequency. In the experiment, a forward propagating Sezawa wave was scattered as a backward propagating Rayleigh wave with very high conversion efficiency.

The mode conversion process was studied and then applied to a resonator configuration where, rather than Bragg reflection of a single longitudinal mode, the conversion back and forth between Rayleigh and Sezawa modes was utilized for confinement of SAW energy. The principle behind the mode conversion resonator is that by placing an IDT of Rayleigh or Sezawa periodicity between properly spaced mode converting reflectors, one can simultaneously create standing Rayleigh and Sezawa waves by excitation from a single IDT. The two standing wave patterns are a result of contra-propagating traveling waves and will be explained in more detail in Chapter 5.

The advantages of the mode conversion resonator are that by coupling into the resonant cavity through one mode and coupling out of the cavity through another, one can reduce the direct acoustic coupling level below that found in conventional resonators which employ IDT's of the same periodicity.

In SAW resonators fabricated to date, the separation distance between the IDT's and the properly spaced reflector arrays is critical for proper operation. In Chapter 5 we present a revised version of the theory for the mode conversion resonator. We use the theory to predict and experimentally verify the positional independence of IDT placement between properly spaced mode conversion reflectors for both one-port and two-port resonator structures.

Finally, Chapter 6 consists of a summary of the research effort and recommendations for further research.

CHAPTER 2

TRANSDUCTION IN THE LAYERED MEDIUM

To date, the most efficient means of exciting and detecting surface acoustic waves (SAW) on piezoelectric substrates as well as layered piezoelectric/semiconductor systems is through the use of interdigital transducers (IDT's). A typical IDT, shown in Fig. 2.1, consists of a periodic pattern of metal electrodes which are alternately connected to different busbars and separated from one another such that fingers and spaces have the same widths. When an rf signal is applied between the two busbars of the IDT, the adjacent fingers of alternating polarity induce periodic stresses in the piezoelectric layer which in turn excite acoustic waves which propagate along the surface of the device. The center of the transducer frequency response occurs when the IDT finger width and spacing are one-quarter wavelength of the excited wave. It should be noted that, in addition to the IDT structure shown in Fig. 2.1, other IDT configurations are routinely employed to provide apodization, special weighting, and even unidirectionality. One variation on the surface acoustic wave transducer, the separate comb transducer[24], will be described for use in the implant-isolated storage correlator.
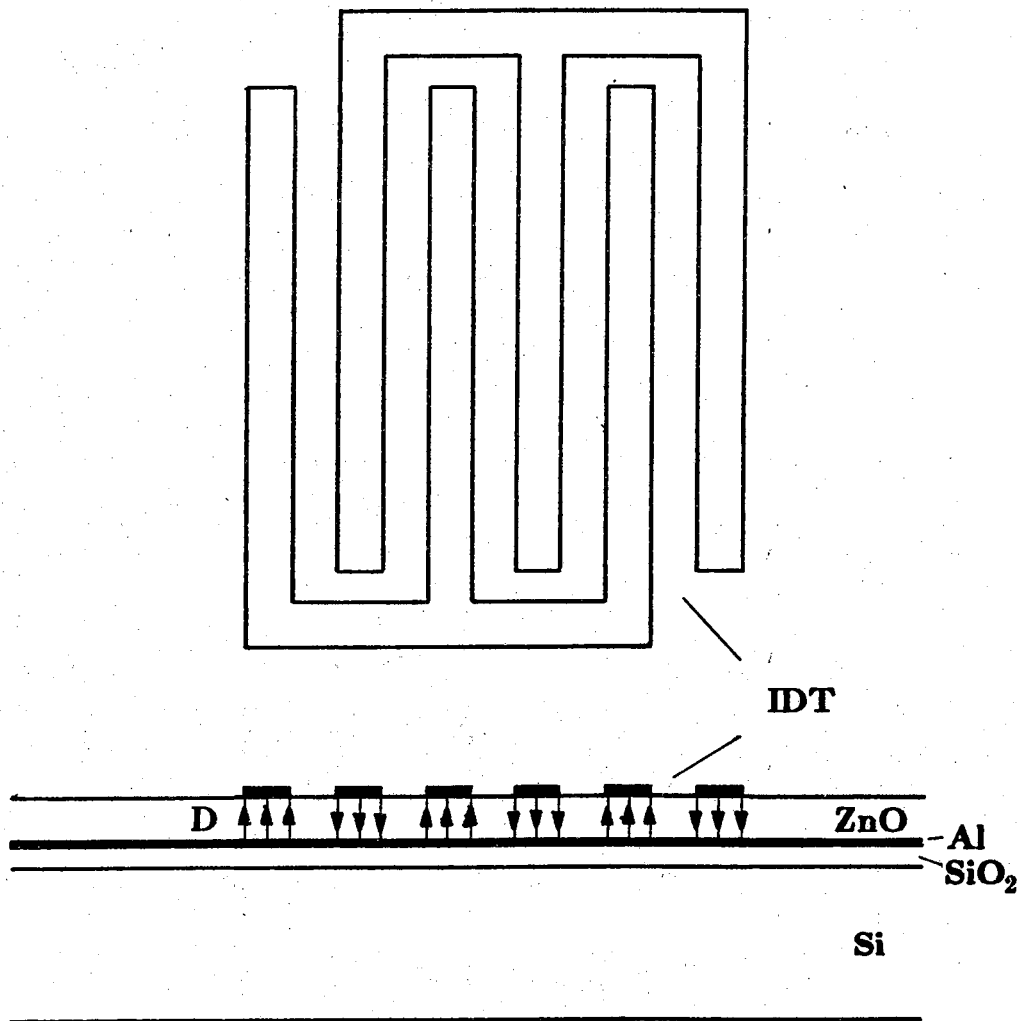
Figure 2.1

Interdigital transducer (IDT) configuration and accompanying crossed-field pattern.

2.1 IDT Coupling

To perform an analysis of IDT operation, it is imperative that one know the phase velocity, v, and the degree of perturbation in phase velocity, Δv, which occurs when a massless conductor is placed upon the previously unperturbed surface. The parameter $\dfrac{\Delta v}{v}$ is related to the electromechanical coupling coefficient k^2, by $\dfrac{\Delta v}{v} = \dfrac{k^2}{2}$. In both single crystal substrates and layered piezoelectric-on-semiconductor configurations, $\dfrac{\Delta v}{v}$ is the most important parameter used for calculating electromechanical coupling.

In the $ZnO/SiO_2/Si$ layered structure there are four possible boundary conditions which are used in the calculation of $\dfrac{\Delta v}{v}$ for different IDT configurations. These configurations are shown in Fig. 2.2 where the shorting plane(s) (if any) are placed at different positions in the $ZnO/SiO_2/Si$ structure. We refer to the IDT coupling $\dfrac{\Delta v}{v}$ for a particular configuration as

$$\Delta_{ij} = \frac{\left| v_i^A - v_j^A \right|}{v_j^A} \quad , \tag{1.1}$$

where the superscript, A, refers to a particular propagating mode such that A=R and A=S denote the Rayleigh and Sezawa modes respectively. The value v_i^A refers to the unperturbed wave velocity, that is, the wave velocity for a wave propagating in a structure made up entirely of the configuration which exists between IDT fingers. Similarly, the perturbed wave velocity, v_j^A, refers to the velocity of the wave propagating in a structure of the same configuration that exists at an IDT finger. As an example, the Rayleigh wave coupling strength for the transducer configuration of Fig. 2.1, is denoted Δ_{13}^R.

SHORTING PLANES

ZnO

SiO$_2$

Si

0   1   2   3
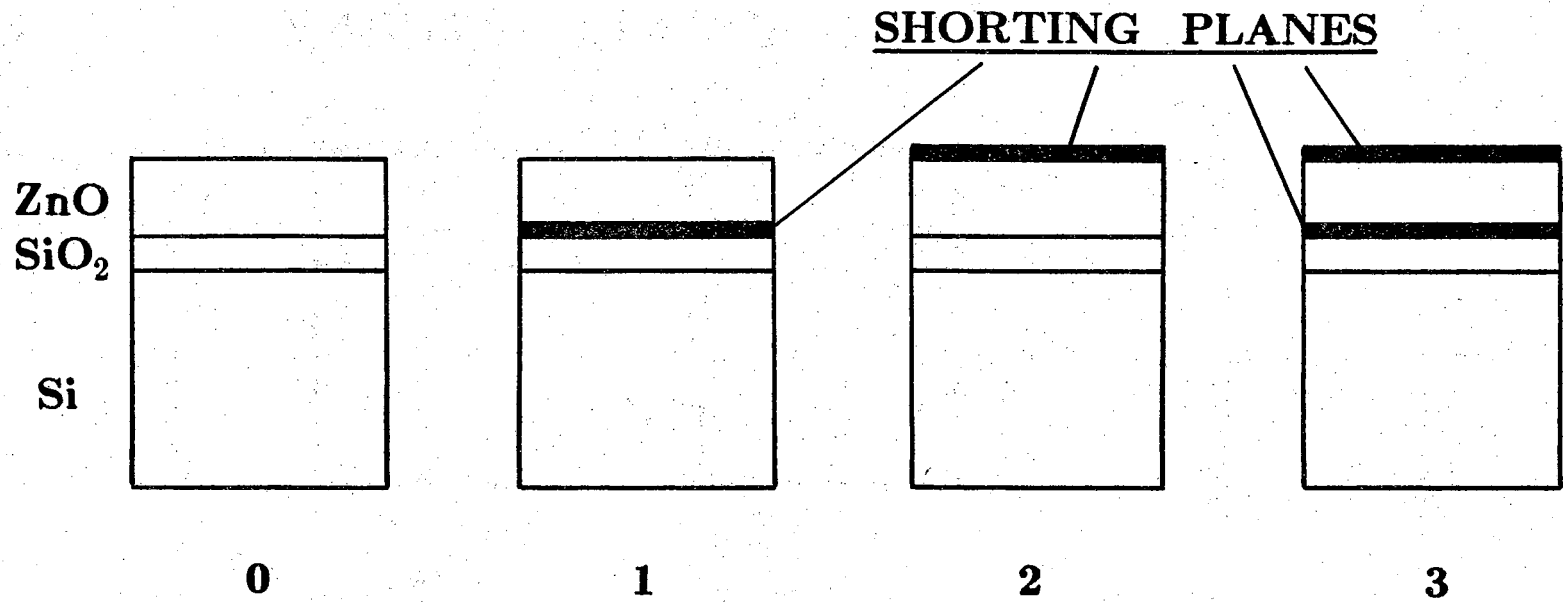
Figure 2.2

The electrical boundary conditions available when employing shorting
planes above and/or below the ZnO layer.

Phase velocity versus normalized film thickness as well as coupling coefficients for various boundary conditions are shown in Figs. 2.3 and 2.4 and Figs. 2.5 and 2.6 for two different orientations of silicon. The normalized film thickness, hk, consists of h, the film thickness and k, the wavenumber of the propagating SAW. In Figs. 2.3-2.6, all values were computed for a ZnO film thickness 49 times greater than the SiO_2 layer thickness. The surface wave velocity plots were computer generated from a program written by K. L. Davis of the Naval Research Laboratory, while the electromechanical coupling curves are from Elliott[25].

In the plots of electromechanical coupling there are peaks of Rayleigh coupling for Δ_{13}^R and Δ_{23}^R for hk $<$ 0.5 on both (100)-cut and (111)-cut silicon substrates. To maximize the coupling level in devices such as convolvers and memory correlators, ZnO films are grown whose thicknesses correspond to maximum coupling at the synchronous frequency. For example, when fabricating a Rayleigh wave SAW convolver on (100)-cut [010]-propagating silicon with IDT's at the top surface of the ZnO (Fig. 2.1), one would grow a ZnO film of thickness h such that hk=0.30 (corresponding to the first maximum) at the IDT center frequency. At 125 MHz, this corresponds to a ZnO film thickness of 1.7 μm. It should be noted that higher electromechanical coupling for the Rayleigh mode is possible using very thick ZnO films but such films increase propagation loss and decrease operating frequency.

Because of the significant differences in achievable coupling levels between the two silicon orientations shown in Figs. 2.4 and 2.6, different substrates are used for different applications. Since available coupling levels on (100)-cut silicon are higher than on (111)-cut silicon for the same ZnO thicknesses, (100) substrates are most common for convolvers and correlators where high coupling
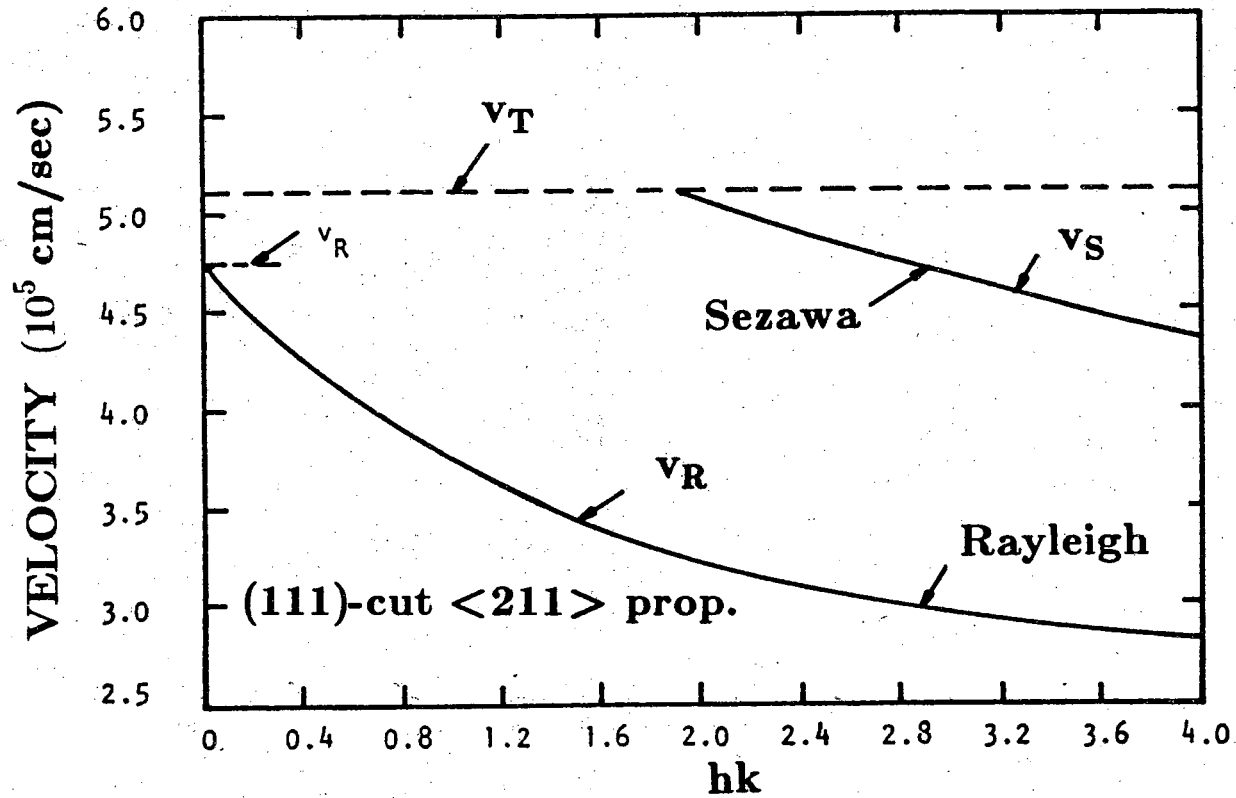
Figure 2.3

SAW velocity dispersion for (111)-cut, <211>-propagating silicon.
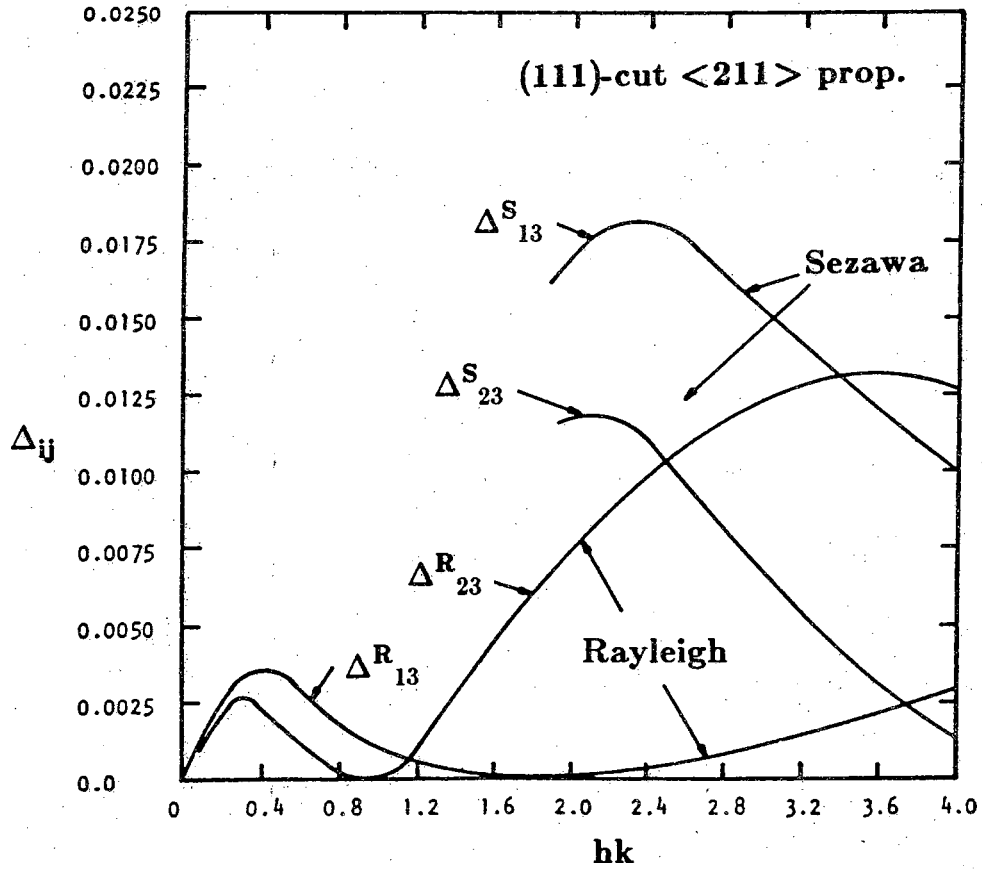
Figure 2.4

$\frac{\Delta v}{v}$ for Rayleigh and Sezawa waves on (111)-cut, <211>-propagating silicon.
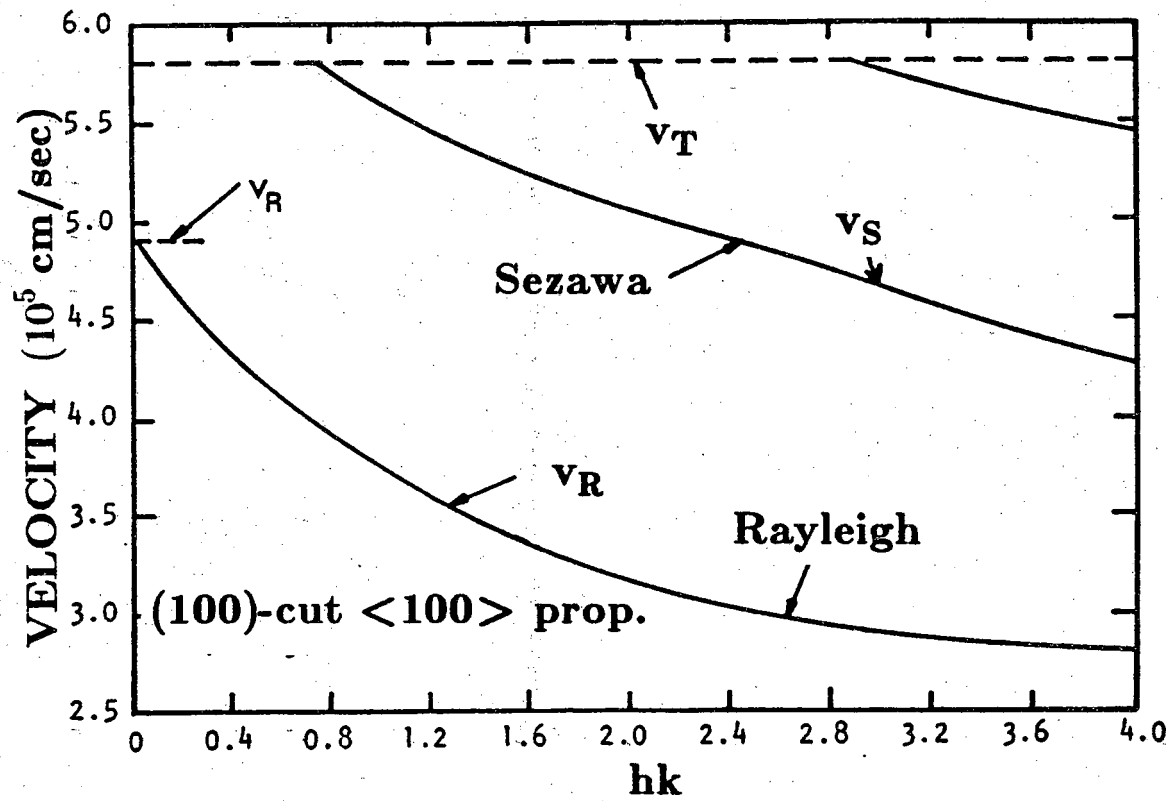
Figure 2.5

SAW velocity dispersion for (100)-cut, <100>-propagating silicon.
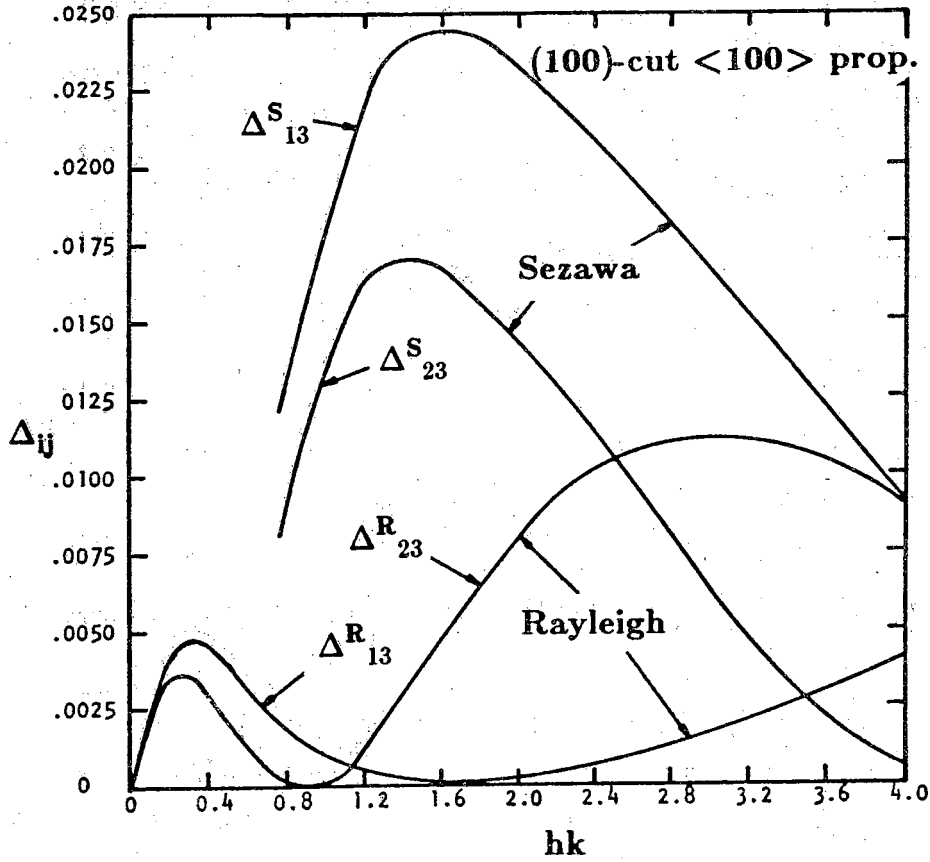
Figure 2.6

$\dfrac{\Delta v}{v}$ for Rayleigh and Sezawa waves on (100)-cut, <100>-propagating silicon.

is desired. In SAW resonator configurations, however, maximum coupling is not necessary or desired because large peak-to-background levels are sought. Additionally, thinner ZnO films give lower propagation loss and higher Q values. As a result, SAW resonators are usually fabricated with ZnO films which are thinner than those corresponding to the first coupling peak. Typically, ZnO-on-(111)-cut silicon resonators are fabricated with hk = 0.15. It should be noted, however, that the mode conversion resonators, which will be discussed in Chapter 5, are fabricated on (100)-cut silicon substrates because one can couple to the Sezawa mode on (100)-cut [010]-propagating silicon with a ZnO film less than half as thick as would be necessary on (111)-cut silicon and at the same time, achieve greater maximum coupling.

2.2 Electrical Characteristics

In the devices discussed in this work, the interdigital transducer configuration of Fig. 2.1 is employed most often and a knowledge of its electrical properties are essential. Characterization of IDT's has been performed for interdigital transducers on semi-infinite piezoelectrics[26, 27] as well as IDT's on piezoelectric thin films deposited on non-piezoelectric substrates[20]. The treatment of IDT analysis varies with assumptions made concerning the field patterns emanating from the transducer electrodes. In the ZnO-on-Si composite structure we assume, because of the proximity of the IDT fingers to the shorting plane, that the electric displacement lies beneath each finger and is perpendicular to the substrate surface. This field configuration, depicted in Fig. 2.1, is known as the "crossed-field" model and has been dealt with in detail by Smith et. al[27].

In the analysis of an IDT which has a crossed-field configuration, the IDT can be modeled as a shunt circuit similar to the one shown in Fig. 2.7. The IDT model consists of a capacitor (C_T) representing the static capacitance of the transducer, and $G_a(\omega)$ and $B_a(\omega)$ which are the acoustic radiation conductance and radiation susceptance of the IDT respectively. The radiation conductance, $G_a(\omega)$, is real and varies with the amount of electrical energy which is transduced into acoustic energy. The admittance terms near the synchronous frequency are given by

$$G_a(\omega) = \hat{G}_a \left[\frac{\sin(x)}{x} \right]^2 \qquad (1.2)$$

and

$$B_a(\omega) = \hat{G}_a \left[\frac{\sin(2x) - 2x}{2x^2} \right] \, , \qquad (1.3)$$

where $x = N\pi \frac{(\omega - \omega_o)}{\omega_o}$ and $\hat{G}_a = \left[\frac{4}{\pi} \right] k^2 (\omega_o C_s) N^2$. Here, C_s is the capacitance per IDT period, and N is the number of IDT periods (finger-pairs).

The synchronous frequency, ω_o, occurs when the excited wave has wavelength equal to the IDT periodicity. It should be noted that at $\omega = \omega_o$, $B_a(\omega)$ becomes zero and the radiation conductance is maximized. Furthermore, the radiation conductance (more often referred to by its reciprocal, radiation resistance) is a function of N^2. Additionally, the zeros of the IDT response (and hence the bandwidth) are also dependent upon the number of IDT periods because of the $\mathrm{sinc}(x)$ dependence of the radiation conductance.

It is interesting to note that the radiation conductance at $\omega = \omega_o$ is the same as that calculated by Martin[28] in his approach which also uses a crossed-
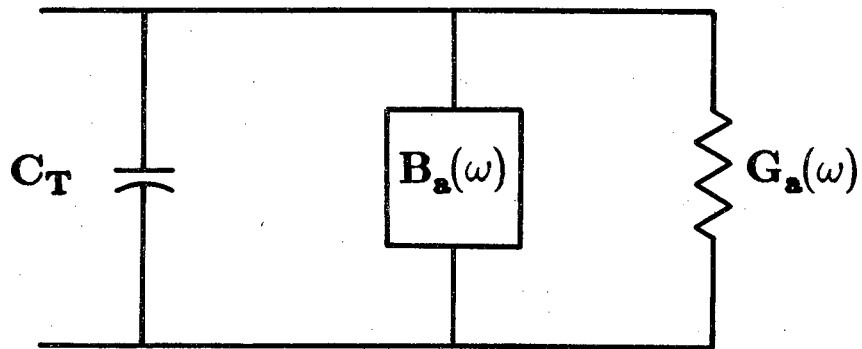
Figure 2.7

Electrical model for an IDT.

field approximation. The difference of a factor of eight between the expressions is that the technique of Smith considers N to be the number of periods (finger pairs) and C_S to be the capacitance per period whereas Martin's N represents the number of IDT fingers and C_f is the capacitance per finger.

We make reference to the approach used by Martin because it will be used in a discussion of the mode conversion resonator in Chapter 5. Whereas the model of Smith predicts accurately the operation of an isolated IDT on an infinite substrate, Martin's technique allows one to compute IDT characteristics in the presence of propagating acoustic waves.

CHAPTER 3

IMPLANT-ISOLATED SAW STORAGE CORRELATOR

3.1 Introduction

The original acoustic wave convolvers were fabricated as bulk wave devices which employed the nonlinearities associated with a stressed crystal to produce the convolution of two signals. The bulk crystal nonlinearity relating the electric displacement, D, to the strain, S, is given by[29, 30]

$$D = KS^2 \tag{3.1}$$

where K is a constant. It was determined, however, that significant enhancement in the nonlinear effects of piezoelectric substrates could be achieved via interactions of surface wave induced electric fields with charge carriers in semiconductors.

The first SAW devices which exploited the nonlinear characteristics of the semiconductor were fabricated in a separated medium configuration as shown in Fig. 3.1, where a piezoelectric material and a semiconductor are mounted in close proximity (typically < 2000 Å). In a separated medium device, transverse electric fields accompanying propagating acoustic waves extend outside the piezoelectric crystal and penetrate into the semiconductor creating a depletion condition inside the semiconductor. The depletion region width, W, is related to E_s, the electric field at the surface of the semiconductor, by
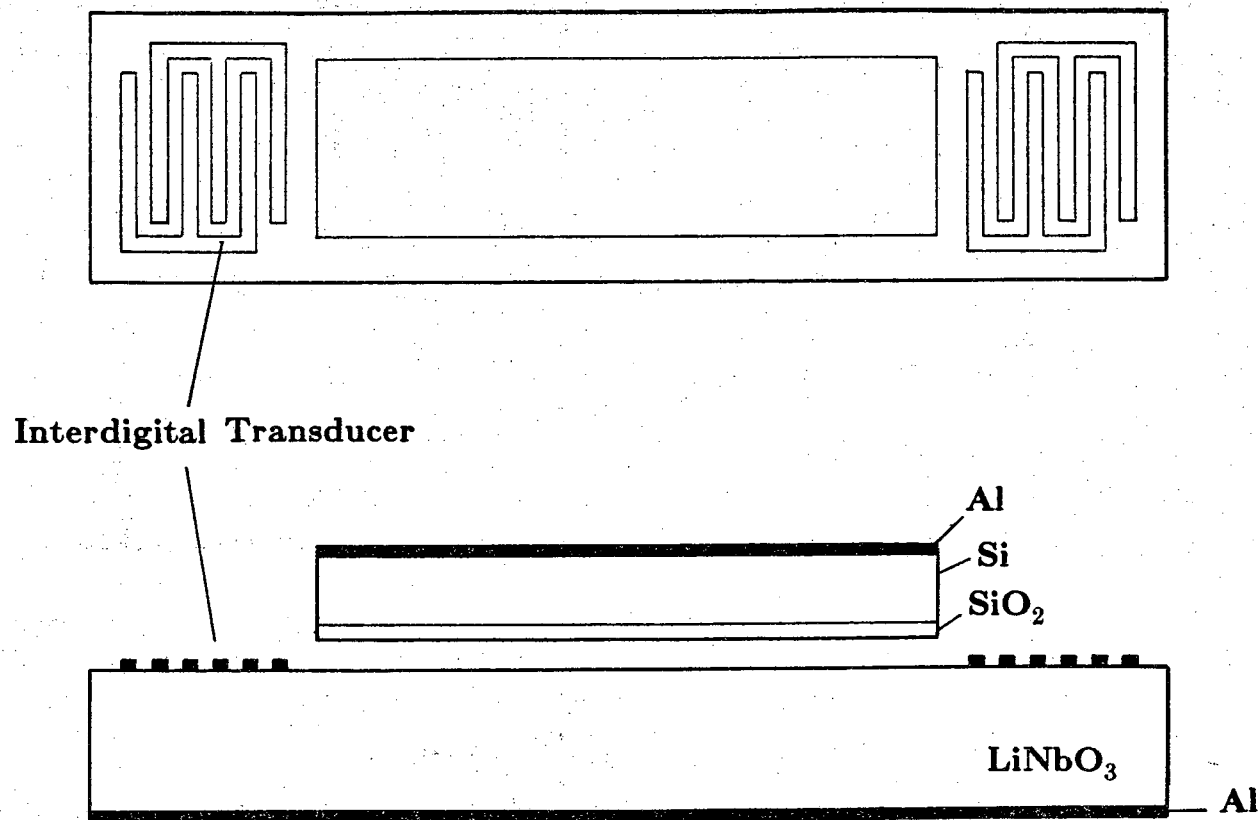
Figure 3.1

Schematic for a separated medium SAW convolver.

$$E_s = \frac{qN_dW}{\epsilon_s} \quad , \quad\quad\quad (3.2)$$

where N_d is the donor density inside the semiconductor and ϵ_s is the permittivity of the semiconductor. The corresponding semiconductor surface potential Φ_s due to the propagating SAW field is given by

$$\Phi_s = \frac{qN_dW^2}{2\epsilon_s} = \frac{\epsilon_s}{2qN_d} E_s^2 \quad . \quad\quad\quad (3.3)$$

The squared dependence of potential upon electric field is the nonlinearity which is exploited in SAW convolvers and correlators. Because of the enhanced nonlinear effects available in the SAW/semiconductor system, surface acoustic wave devices rapidly overtook their bulk wave counterparts.

Another attractive feature of the separated medium configuration is that both semiconductor and piezoelectric can be interchanged to exploit the different characteristics of each. For example, $LiNbO_3$ is a popular piezoelectric material because its high electromechanical coupling yields high efficiency and wide bandwidth capability. Silicon is a common semiconductor material because its properties are well known. It should be emphasized, however, that it is the characteristics of the piezoelectric crystal and properties of the semiconductor, including resistivity and surface state density, which determine the strength of the interaction between the SAW and the semiconductor.

Although a great deal of work has been performed on the separated medium devices[31,13,32,33], several drawbacks to this configuration have been noted. A mechanically complex structure to fabricate because of the critical spacing requirement of the air gap, quantity production of these devices is

impractical. These devices also suffer from a large background spurious bulk wave signal level due to modes launched in the gate region by rf signals. Furthermore, to control the surface bias condition of the silicon (essential for optimizing device performance) large bias voltages of the order of 1000 V are required, making the necessary accompanying electronics rather inconvenient. To alleviate problems associated with the separated medium configuration, monolithic piezoelectric-on-semiconductor devices have been fabricated as an attractive alternative.

The schematic of a typical monolithic $ZnO/SiO_2/Si$ SAW device is shown in Fig. 3.2, consisting of a piezoelectric thin film sputter deposited atop a thermally oxidized silicon substrate. The top surface metallization pattern is defined by standard photolithographic techniques in a single masking step. Shorting planes located at the piezoelectric/oxide interface serve to enhance the electromechanical coupling of the IDT's (Chapter 2). The layered configuration affords several advantages over separated medium devices related to rugged construction, ease and repeatability of fabrication, and enhanced interaction uniformity. Because of the proximity of the metal gate electrode to the semiconductor, the surface condition of the substrate is readily controlled with the application of modest bias voltages of the order of a few volts. Furthermore, because of the thin ZnO film, the plate mode resonant frequency of the gate for a device fabricated to operate at 125 MHz is greater than 1 GHz. Thus, the monolithic configuration is without the inherent spurious bulk wave interference present in its separated medium counterpart, allowing for an increase in available dynamic range.

Once a limitation to the usefulness of layered medium SAW devices, the bandwidth of these devices has been increased dramatically through the use of
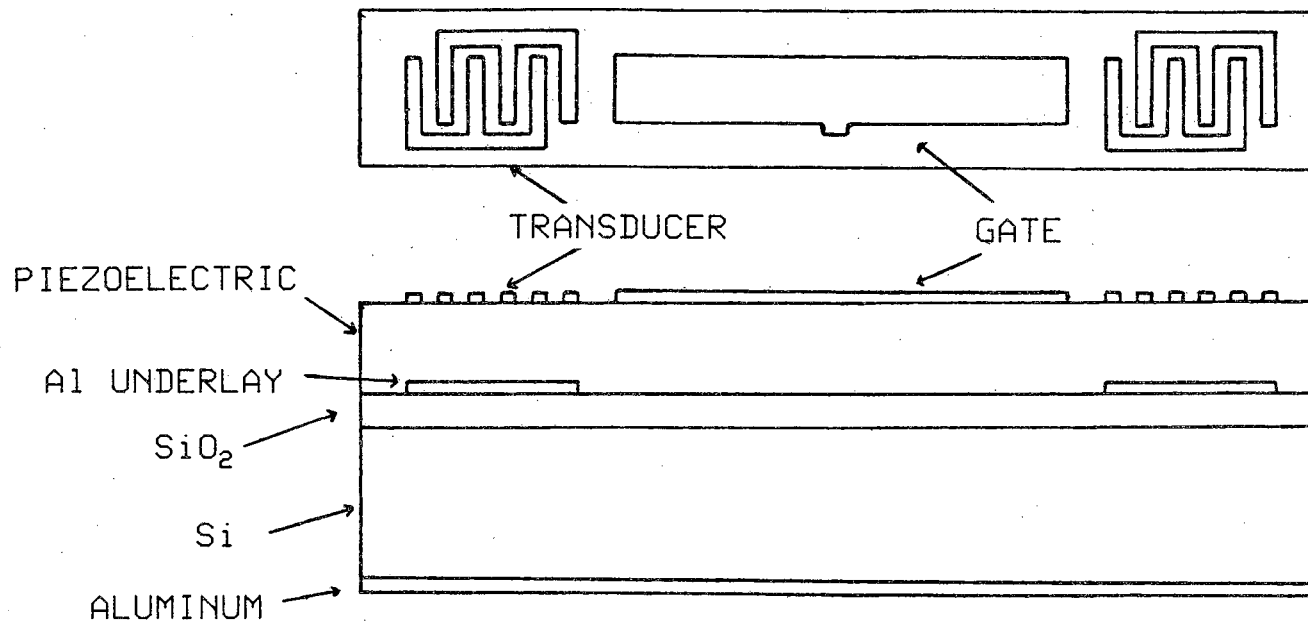
Figure 3.2

Schematic of a typical monolithic SAW correlator.

higher order surface wave modes. It has been shown that the second order or Sezawa mode of the layered $ZnO/SiO_2/Si$ configuration can be efficiently excited in high quality films[34]. The electromechanical coupling coefficient available from this mode exceeds that for Rayleigh waves in bulk ZnO, and is close to the value for $LiNbO_3$. Thus, the wide bandwidth capability of the separated medium is challenged by employing the high electromechanical coupling of a higher order Rayleigh mode. Several convolvers and diode storage correlators which exploit the bandwidth advantage of the Sezawa mode have been reported[35, 36, 12, 37].

The family of monolithic SAW devices includes structures fabricated on GaAs substrates which have demonstrated outstanding time bandwidth products[38]. Because of the relatively weak piezoelectric nature of the GaAs, however, these devices, when implemented without a piezoelectric film overlayer, have lower correlation efficiencies at wide bandwidth compared with other configurations, although substantial progress has been made toward improving these efficiencies[39]. The development of layered medium monolithic SAW devices has emphasized the use of ZnO and AlN as piezoelectric films. Although ZnO was the first thin film having high performance in the SAW context[40], and hence has received the most attention[41, 42], AlN[43, 44, 45] has some attractive features related to ruggedness and the potential for low dispersion. Both materials can be utilized to achieve a temperature stable configuration.

3.2 Convolution

It is useful to examine the convolution of two rf signals using a SAW convolver because of the similarity between the convolution and correlation processes. We refer to Figs. 3.1 and 3.2 in our discussion of convolution.

The simultaneous application of modulated rf signals to each of the two transducers of a convolver causes surface acoustic waves to be launched which propagate toward one another in the gate region of the device. Because the piezoelectric ZnO exists everywhere between the two IDT's, the propagating acoustic waves have electric fields associated with them. More specifically, if the input signals $V_1(t)e^{-j\omega t}$ and $V_2(t)e^{-j\omega t}$ are introduced at IDT 1 and IDT 2 respectively, the associated contra-propagating acoustic wave potentials present in the gate region will be of the form* $V_1(t - \frac{z}{v})e^{-j\omega(t - \frac{z}{v})}$ and $V_2(t + \frac{z}{v})e^{-j\omega(t + \frac{z}{v})}$. The electric fields associated with these propagating waves extend beyond the ZnO layer (or piezoelectric substrate) and penetrate into the semiconductor through the oxide layer (or air gap). Due to the nonlinear effects of the semiconductor, the resultant combined signal is proportional to the product of the two signals, such that at any point

$$V = A\left[V_1(t - \frac{z}{v})e^{j\left[\frac{z}{v}\right]t} V_2(t + \frac{z}{v})e^{-j\left[\frac{z}{v}\right]t} \right]e^{-j2\omega t} \quad , \qquad (3.4)$$

where v, the acoustic wave velocity and ω, the radian frequency, are taken to

---

* Because bi-directional transducers are used, waves are launched in both directions from each IDT. We assume, however, that waves launched out the ends of the device (which are potential sources of spurious signals) are acoustically absorbed and do not contribute to the processed signal.

be the same for both inputs. The coupling factor, A, relates the strength of the nonlinear interaction to the output voltage.

The function of the metal plate electrode (also known as the gate) between IDT's at the surface of ZnO shown in Fig. 3.2 (or the metal contact on the back of the semiconductor in the separated medium device of Fig. 3.1) is to sum the total signal over the entire interaction region giving as an output signal

$$V_{out} = e^{-j2\omega t} \int_{-\frac{L}{2}}^{\frac{L}{2}} AV_1(t - \frac{z}{v})V_2(t + \frac{z}{v})dz \quad , \tag{3.5}$$

where L is the gate length. Assuming that the coupling, A, is uniform over the interaction region, and making a change of variables such that $\tau = t - \frac{z}{v}$, one obtains

$$V_{out} = Ae^{-j2\omega t} \int_{-\infty}^{\infty} V_1(\tau)V_2(2t - \tau)d\tau \quad . \tag{3.6}$$

In Eq. 3.6 the limits of integration have been changed assuming both input signals have time duration less than or equal to $\frac{L}{v}$. The resultant output waveform is, therefore, the convolution of the two functions V_1 and V_2 with time scale reduced by a factor of two because the signals are propagating toward one another with relative velocity 2v.

It can be noted from Eq. 3.6 above that if either V_1 or V_2 had been time inverted before application to the IDT, the resultant output would be the correlation of the two signals (again, compressed in time). An electronic time reversal technique[46] has been demonstrated in a convolver system[47], but at a

sacrifice of high insertion loss which leads to a degraded dynamic range. Furthermore, to be most useful as a practical device, the SAW convolver must be able to convolve between a reference signal and a signal which may appear at a convolver input at some unknown time. An incoming signal arriving at an unknown time necessitates repeated application of the reference signal to counter the uncertainty of the arrival time which in turn leads to a smaller effective time-bandwidth product.

The storage correlator is a device which can perform both convolution and correlation without the need for time reversal and without concern for the uncertainty of the arrival time of the signal to be interrogated. Hence, two of the major drawbacks of performing correlation with the convolver system are eliminated by utilizing a memory correlator.

3.3 Storage Correlation

A simplified description of the storage correlation process can be given with the aid of Fig. 3.3 which depicts a typical memory correlator. Under normal operation, one introduces a signal at one of the transducers such that a sampled version of this reference signal, S(t), is stored beneath the gate of the device by one of several possible writing procedures. At some later instant, but still within the storage time of the reference signal, a second signal, R(t), known as the reading signal, is applied to the gate of the correlator. The introduction of R(t) at the gate electrode excites two contra-propagating signals representing the product of R(t) and S(t), which subsequently appear at the two output transducers; it can be shown that the correlation appears at one transducer, while the convolution output is available at the other.

$R(t)e^{jwt}$

$R(t)*S(t)$

$R(t)**S(t)$

$S(x)e^{-jkx}$
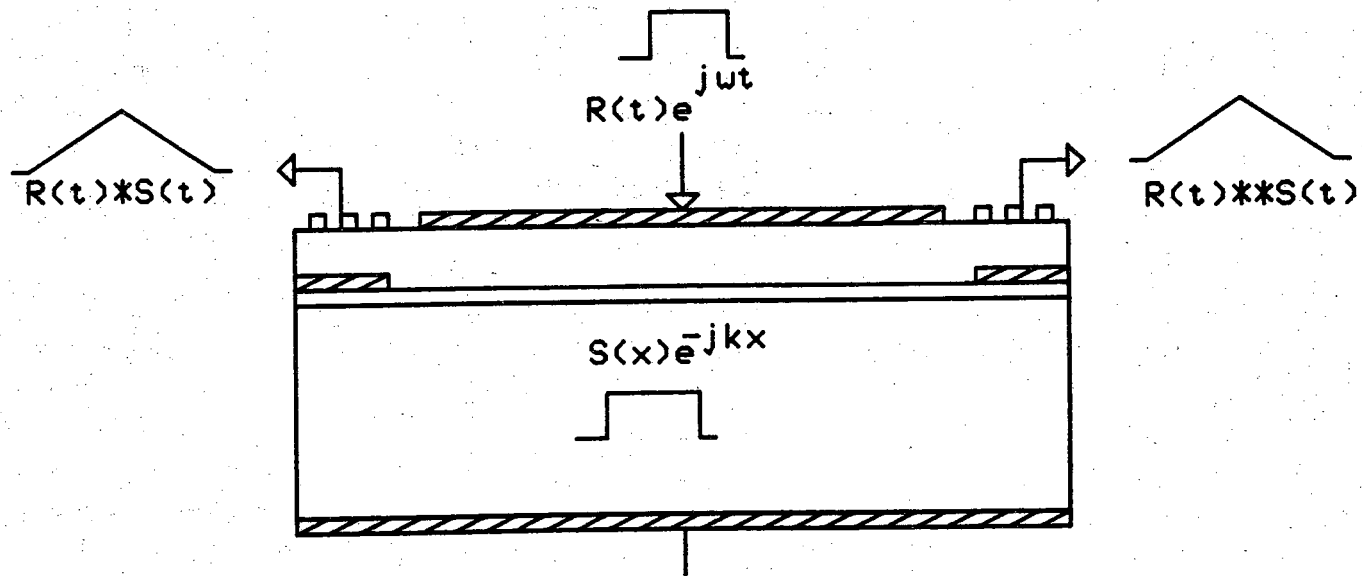
* : CONVOLUTION

** : CORRELATION

Figure 3.3

Correlation and convolution using a storage correlator.

By applying a particular "writing" process to the correlator, one introduces a reference signal to be stored as a spatially varying charge pattern by one of several storage mechanisms. Schemes for signal storage by means of surface states[14,48], pn diodes[49,50,36,51,16], and Schottky diodes[15,52,53] have been examined. More recently, a new type of junction storage correlator has been introduced[54] in which the spatial variation of inversion layer charge at the SiO_2/Si interface of the layered monolithic configuration has been utilized for signal storage. With the exception of this "induced junction" storage correlator, the various storage schemes have been employed in both monolithic and separated medium configurations.

3.3.1 Storage Mechanisms

The first memory devices utilized semiconductor surface states for signal storage[14,48]. In a surface state memory correlator, the electric field pattern associated with an applied signal causes a bunching (periodic spatial concentration) of free electrons at the Si/SiO_2 interface. Subsequently, a portion of the electrons are trapped at the interface thereby producing a spatially varying charge pattern. The storage time of these devices corresponds to the detrapping time which is a function of the properties of the interface.

Surface state storage was subsequently replaced by more easily controlled and repeatable diode storage arrays. Figure 3.4 is a schematic of a monolithic pn diode storage correlator. In a pn-diode or Schottky diode array, the application of a writing sequence imposes a time varying standing wave signal proportional to the reference signal at the top surface of the diodes. When the applied writing signal is positive, the diodes become forward biased and minority carrier holes are injected into the n-type semiconductor where some
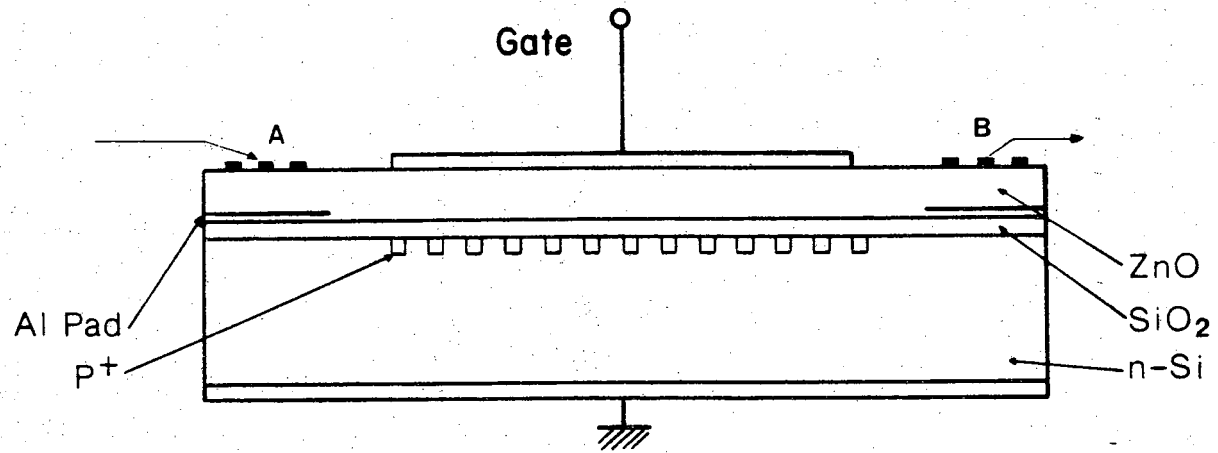
Figure 3.4

Monolithic ZnO/SiO$_2$/Si pn diode memory correlator configuration.

recombine. When the signal goes to zero or becomes negative, however, most of the injected holes are swept back into the p^+ region, less an amount which recombined, leaving the diode depletion widths altered by an amount proportional to the number of recombined holes. The recombined holes increase the depletion widths of the diodes and create a reverse bias condition in the diodes. A replica of the reference signal is stored in the spatially varying depletion widths of the diodes.

Recently, reference signal storage in induced junctions was reported[54]. In both diode and induced junction array processes, the principle of charge storage is essentially the same. Recombination of minority carriers injected out of a p^+ region (or inversion layer in the case of the induced junction device) by an applied signal causes an alteration of the diode (induced junction) depletion width. More will be mentioned about the induced junction storage process in a later section.

3.3.2 Writing Techniques

There are many modes of operation which are used in the SAW memory correlator structure, all of which are very similar. We limit ourselves to a discussion of the "gate-acoustic" writing technique and the "gate-to-acoustic" reading technique in the implant-isolated storage correlator. We use Fig. 3.5 to illustrate these writing and reading methods[19]. Descriptions of other writing techniques can be found in the literature[55, 56].

Consider the application of an rf signal $S(t)e^{-j\omega t}$ to one of the device transducers. As in the convolver structure, an acoustic wave is excited which is of the form $S(t - \frac{z}{v})\cos(\omega t - kz)$. In the case of the memory correlator
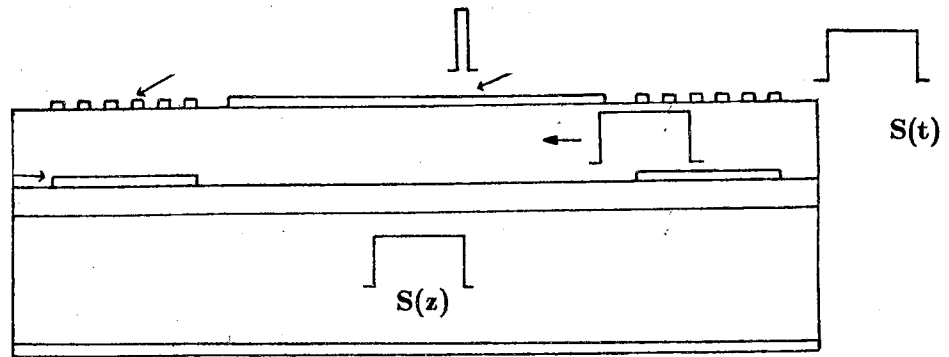
(a)
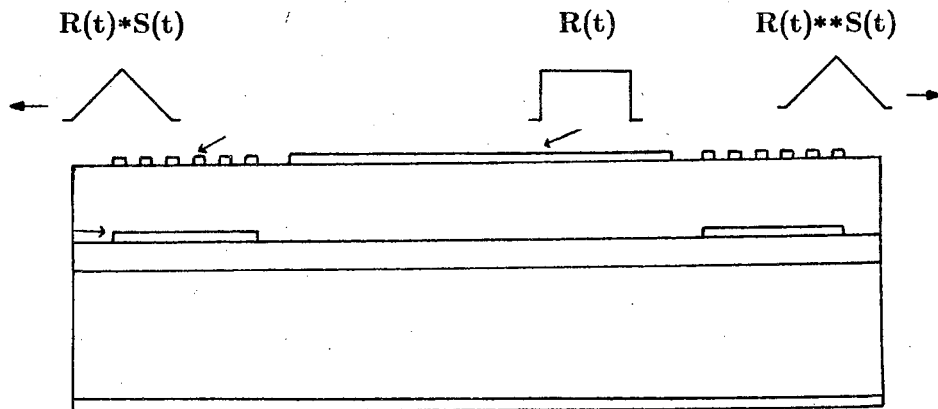
(b)

** CONVOLUTION

** CORRELATION

Figure 3.5

(a) Gate-acoustic writing (b) Gate-to-acoustic reading.

operating in the gate-acoustic writing mode, we apply an rf "writing" signal, $G(t) = W\cos(\omega t)$ (of short duration compared to the inverse bandwidth of S), to the gate in the presence of the propagating reference signal (Fig. 3.5a). Summing the components present in the gate region, one obtains a net potential given by

$$V \propto \sqrt{(S^2 + 2SW\cos kz + W^2)}\cos(\omega t - \phi(z)) \quad . \tag{3.7}$$

Under normal operation $|W| \gg |S|$ which implies the net potential during the writing process is of the form

$$V \propto (W + S\cos(kz))\cos(\omega t - \phi(z)) \quad . \tag{3.8}$$

Thus, what exists in the gate region during the writing process is a standing wave pattern which consists of a uniform writing component, W, as well as the spatially varying acoustic portion, S. During the positive cycles of this writing process, the storage regions (surface states, diodes, etc...) will be charged as described above. This technique involving a propagating SAW and an rf gate signal is known as the rf gate-acoustic (or parametric) writing mode.

If instead of an rf writing signal, one applied a very narrow pulse, V_p to the gate at time t_o in the presence of the propagating wave $S(t - \frac{z}{v})\cos(\omega t - kz)$, the resultant gate potential would be given by (assuming $V_p \gg |S|$)

$$V \propto V_p + S(t_o - \frac{z}{v})\cos(\omega t_o - kz) \quad . \tag{3.9}$$

Thus, a signal is applied across the diodes which is an imprint of the reference signal superimposed on a uniform writing pulse. The electric field components associated with this signal cause a signal to be stored which consists of a uniform writing pulse component, V_p, and a spatially varying acoustic portion

S(z). This writing technique is known as the flash mode of operation.

If the rf gate-acoustic writing mode is utilized, the injection of holes takes place many times (each positive cycle of the signal) during a writing sequence depending upon the length of the writing signal. Each rf writing cycle contributes to the change in depletion width but with each subsequent cycle contributing less than the previous one (assuming uniform signals). The parametric writing technique has been used for signal storage when employing pn diodes, Schottky diodes, and surface state memory arrays. When operating in the flash mode, however, there is a net forward bias of the diodes only once per writing sequence and only for a very short time.

To effectively write a reference signal into the gate region using the flash mode, the response time of the diodes or surface states must be very fast. It was originally demonstrated[56] that the flash mode was an efficient writing technique in the separated medium configuration for pn diodes in a mesa V-groove array but the accompanying theory did not apply well to ZnO-on-silicon planar diode array configurations[57,58]. The flash mode has been discussed at great length in the literature and the consensus is that only Schottky diode and surface state storage are practical when using the flash writing mode in the monolithic configuration. This is by no means a limitation because pn diode memory arrays have been shown to be very efficient when utilizing the parametric writing mode.

Irrespective of the writing technique used, the subsequent correlation output is obtained by introducing a "reading" signal to the gate electrode. This gate-to-acoustic reading mode is shown in Fig. 3.5b. Application of the rf reading signal launches contra-propagating acoustic waves whose envelopes

represent the convolution and correlation of the stored reference signal and the applied reading signal.

3.3.3 The Induced Junction Memory Correlator

Recently, a new type of monolithic ZnO-on-Si memory correlator was fabricated[54, 59] which utilized induced junctions to store a replica of a reference signal. The induced junction storage correlator developed by Weng et al[54]. stores a reference signal by successfully exploiting the otherwise undesirable charge injection phenomena associated with sputtered ZnO films. Because some similarities exist between the implant-isolated storage correlator and the induced junction device, it is worthwhile to review operating characteristics of the induced junction storage correlator.

The induced junction device, a schematic of which is shown in Fig. 3.6, is no more than a typical metal/ZnO/SiO$_2$/Si (MZOS)[60, 61] convolver with a metal grating at the ZnO/SiO$_2$ interface. It is the metal grating, however, and a phenomenon known as charge injection which define the storage regions of the induced junction storage correlator.

Charge injection is an imperfection which occurs in devices fabricated in the MZOS layered medium configuration. The charge injection phenomenon, which has been examined by several authors[62, 14], is a process whereby electrons are injected into the conductive ZnO at the gate electrode and migrate into traps at the ZnO/SiO$_2$ interface. The rapid trapping and relatively slow detrapping of these states leads to what is known as bias instability. An example of bias instability is illustrated by the large hysteresis in the capacitance-voltage (C-V) characteristics of the MZOS capacitor shown in Fig. 3.7. The magnitude of the swing in the C-V curve is determined by the
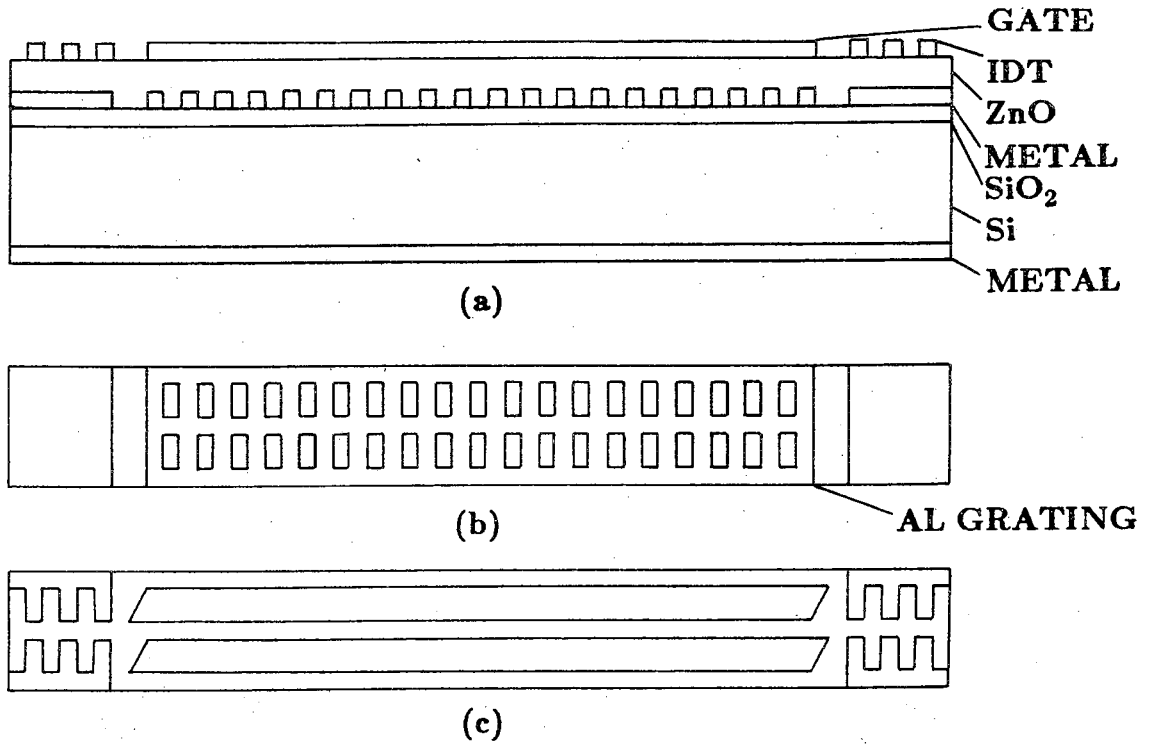
Figure 3.6

Schematic for the induced junction storage correlator showing (a) cross-sectional view of the device, (b) top-view of the aluminum grating pattern, and (c) top-view of the gate region.
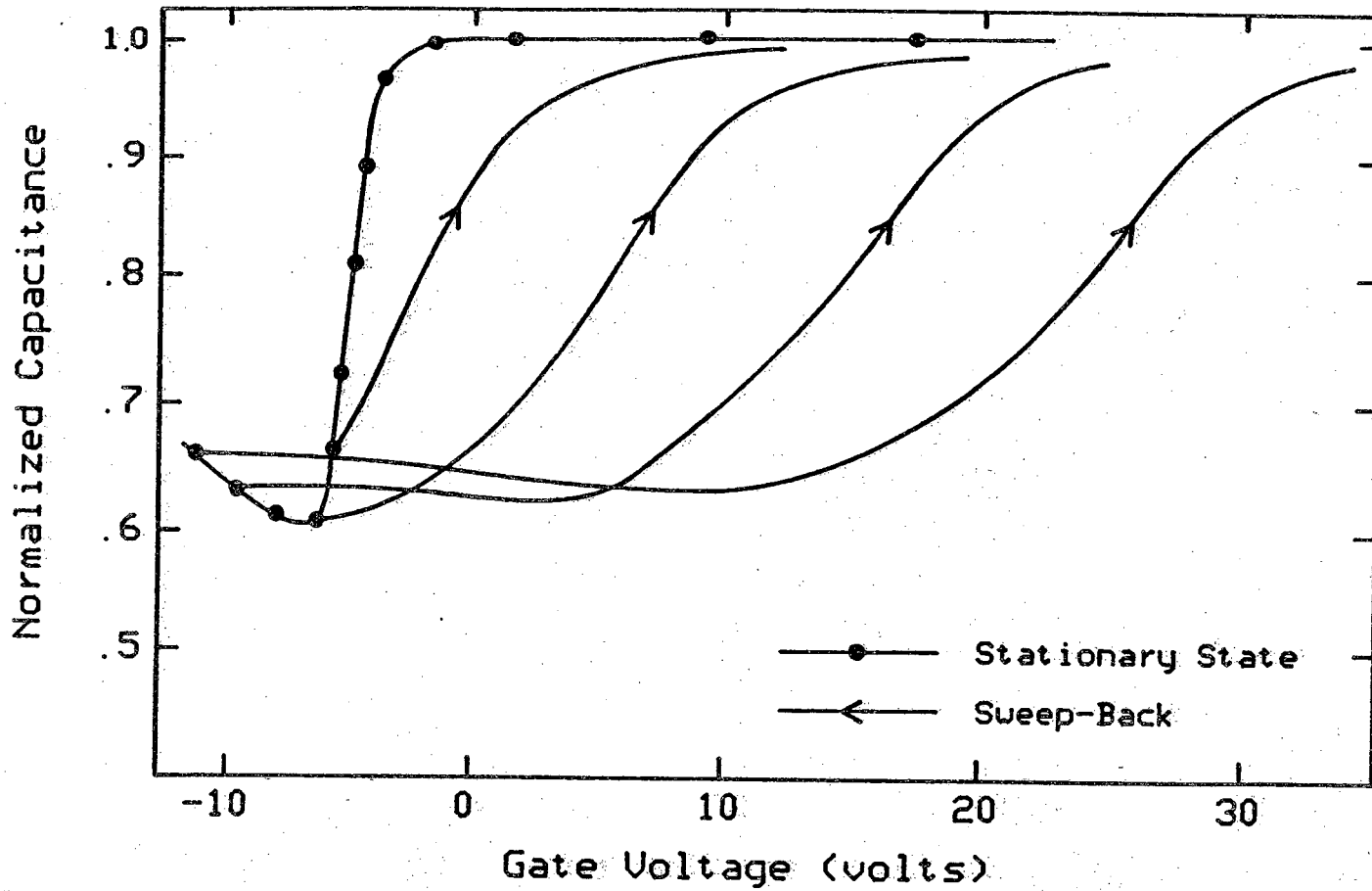
Figure 3.7

Capacitance-Voltage curves for an MZOS capacitor exhibiting charge injection.

amount of charge which has been injected into the ZnO and, therefore, changes depending upon the reverse bias voltage applied prior to sweeping back toward accumulation voltages. The induced junction storage correlator was designed to utilize this otherwise undesirable condition in a constructive manner.

Application of a negative dc bias to the gate of the induced junction device begins the injection of electrons into the semiconducting ZnO layer. Eventually there is zero electric field present in the ZnO layer; the entire voltage drop is across the SiO_2 and the silicon. Under steady state conditions, electronic charges are collected on the metal grating or located between metal regions in deep level traps at the ZnO/SiO_2 interface. If the gate bias is sufficiently negative, an inversion condition exists at the silicon surface and a minority carrier inversion layer exists at the SiO_2/Si interface as shown in Fig. 3.8. At this point,[*] by making the gate voltage more positive, electronic charges located on the metal grating are readily withdrawn from the ZnO but the electrons trapped in the regions between the metal grating are stored for long periods of time, typically days. The result of the positive voltage shift leaves the silicon surface ready as a storage medium with an array of induced junctions as shown in Fig. 3.9.

The induced junctions are inversion regions located beneath the trapped electrons. The minority carrier inversion layers are separated from one another by depletion regions directly beneath the aluminum grating. Charge storage in the induced junction device is similar to that which occurs in a pn diode correlator whereby the application of a positive pulse causes the injection of

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[*] Typically, a negative bias of -35 V was used to invert the silicon and fill the traps at the zinc oxide-silicon dioxide interface. The device was usually operated with a gate bias of approximately -2 V.
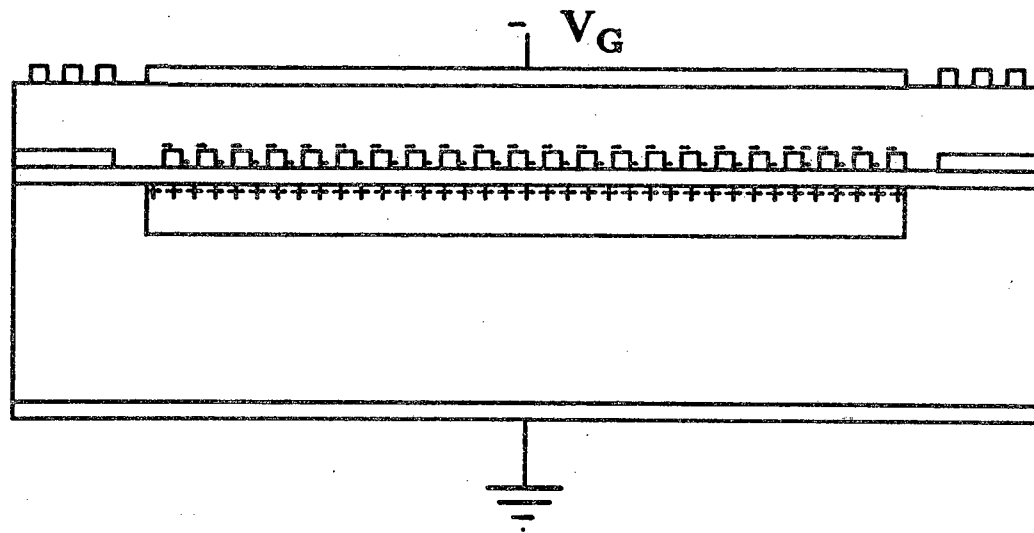
Figure 3.8

Creation of an induced junction array by total inversion of the semiconductor.

$$-V_G + \Delta v_G$$
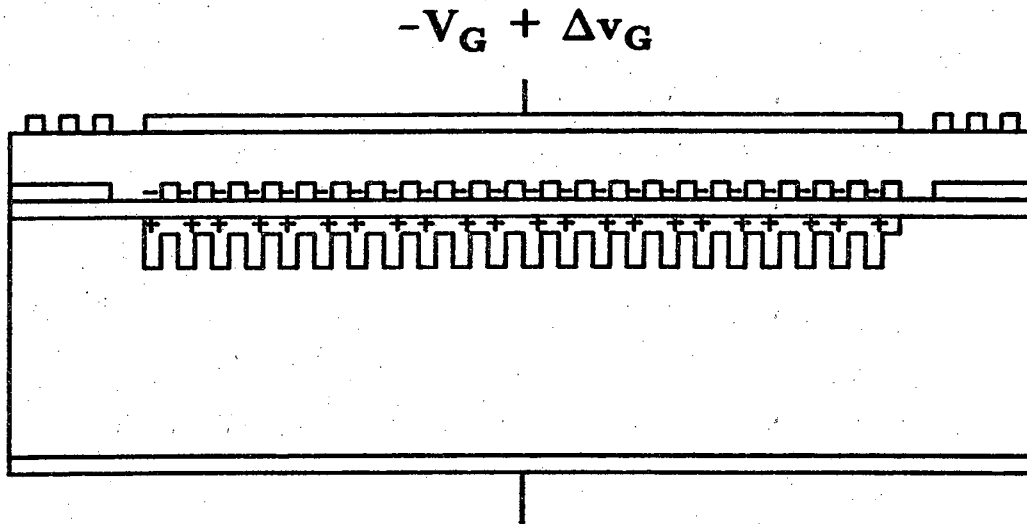
(b)

-- : ELECTRONS
++ : HOLES
⌐⌐ : DEPLETION REGION EDGE

Figure 3.9

Array of induced junctions formed after inverting the entire gate region.

inversion layer minority carriers into the depletion region where some recombine before the pulse is turned off. The recombination of injected inversion layer holes changes both the equilibrium surface charge density and depletion width of the storage regions, thereby altering the equilibrium depletion capacitance of the storage regions. The depletion widths associated with signal storage are greater than the maximum equilibrium inversion layer depletion widths; a condition known as deep depletion. Thus, just as in a pn diode array, a signal can be stored in a spatially varying pattern of depletion widths.

Similar to the induced junction device, the monolithic implant-isolated memory correlator, discussed next in this chapter, utilizes depletion regions in the silicon to store a reference signal in an MOS region of n-type silicon only; that is, no diodes or surface states are employed for storage. Furthermore, the uncontrollable and often undesirable charge injection process[62, 18, 53, 63] which was used constructively by the induced junction storage correlator is successfully ignored in the implant isolated storage device.

In the following section we present a detailed description of the implant-isolated storage correlator fabrication and operation as well as experimental verification of the existence of induced junction storage regions. Section 3.5 contains an in-depth discussion of charge storage in the implant-isolated device. An approximation for the effective recombination lifetime of minority carriers is also presented. Experimental results for the implant-isolated storage correlator are given in Section 3.6 followed by a discussion of unique device applications in Sections 3.7 and 3.8.

3.4 The Implant-Isolated Structure

The implant-isolated storage correlator presented in this chapter is a unique monolithic SAW device which uses alternating regions of highly doped and lightly doped silicon to store a reference signal for correlation or convolution at some later time. The implant-isolated device will be shown to be a bias stable device capable of signal storage more than ten times longer than any other monolithic storage correlator reported to date. Additionally, the implant isolated structure provides a means by which the electrical potential of a surface wave can be determined.

3.4.1 Device Structure

The implant isolated storage correlator, pictured in Fig. 3.10, consists of an n-type 10 Ω–cm (100)-cut silicon substrate which is ion implanted with phosphorus in a grating pattern at the sample surface. Charge storage, it should be noted, occurs in the non-implanted regions. Subsequent to the grating region implantation, a wet oxidation is performed at 900 °C for 40 minutes. This oxidation, yielding a 1000 Å thick insulating layer, simultaneously passivates the silicon surface and activates the implant. Prior to depositing the 1.7 μm ZnO layer by rf sputtering, 1000 Å thick aluminum shorting planes are evaporated on the substrate in the regions below the transducers to enhance the electromechanical coupling. The top aluminum metallization pattern consists of two pairs of single comb transducers[24] and a split gate electrode arranged so as to form a dual track structure[64]. The transducers, used to excite Rayleigh waves, have equal 17.75 μm finger widths and gaps; the center frequency of the transducer response is 128 MHz. The separate comb dual track structure is employed because this technique has been
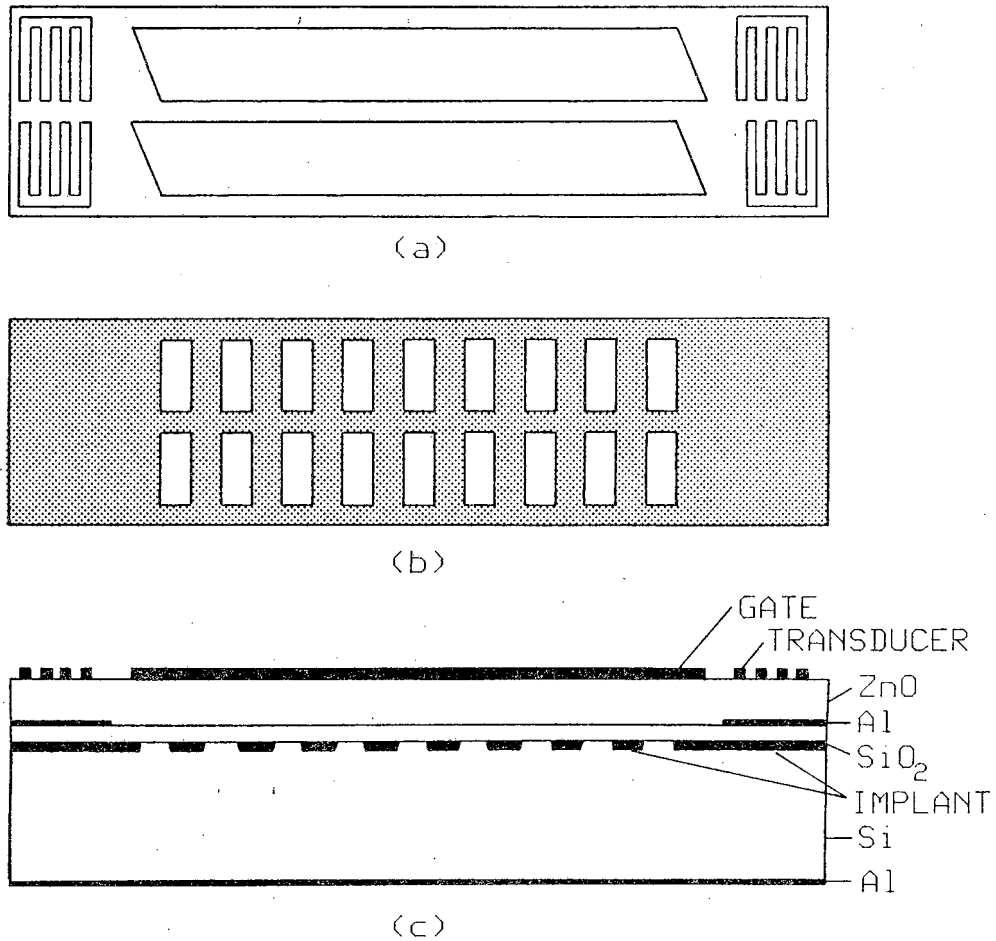
Figure 3.10

Schematic of an implant-isolated storage correlator. (a) Top view of dual gate structure and single comb transducers. (b) Ion implantation pattern. (c) Side view of completed device.

shown to suppress the self convolution caused by reflections from the transducers[64]. By slanting the gate metallization pattern adjacent to the transducers one minimizes the undesirable output observed at the transducers caused by waves launched at the ends of the gate. In Table 1 we summarize the important device parameters for the implant-isolated storage correlator.

3.4.2 Implant Isolation Concept

Insight into operation of the implant isolated storage correlator can best be achieved by understanding the method in which charge is stored in the device. We present a qualitative explanation based on typical n-type MOS capacitance versus voltage characteristics. To first order the ZnO layer can be modeled as a constant capacitance in series with the constant SiO_2 layer capacitance; the combination can in turn be modeled as a single effective insulating layer. C-V curves for two structurally identical but differently doped MIS-capacitors are displayed in Fig. 3.11. Note that for both devices, accumulation occurs over the same bias range. However, the onset of inversion occurs for different values of capacitor bias. Suppose the two differently doped devices were side-by-side as part of the same substrate and covered by the same insulator and metal gate. Under this condition a range of gate bias voltages would exist where the higher doped device would be depleted and the lower doped device would be inverted. In the implementation of the implant-isolated storage correlator, higher doped depletion regions are used to isolate the lower doped storage or inversion regions.

To achieve lateral variations in doping density one can employ either ion implantation or diffusion; ion implantation was chosen because it offered advantages in ease of fabrication. Phosphorus was implanted into the

Table 1

Device parameters for the implant-isolated storage correlator

Silicon type	n
Resistivity	10 Ω-cm
Silicon cut	(100)
SAW Propagation direction	<100>
ZnO thickness	1.7 μm
SiO_2 thickness	1000 Å
Wavelength	35.5 μm
Center frequency	128 MHz
Fingers per comb	20
Storage region width	5 μm
Grating periodicity	10 μm
Gate length	1.4 cm
Gate width	0.1 cm
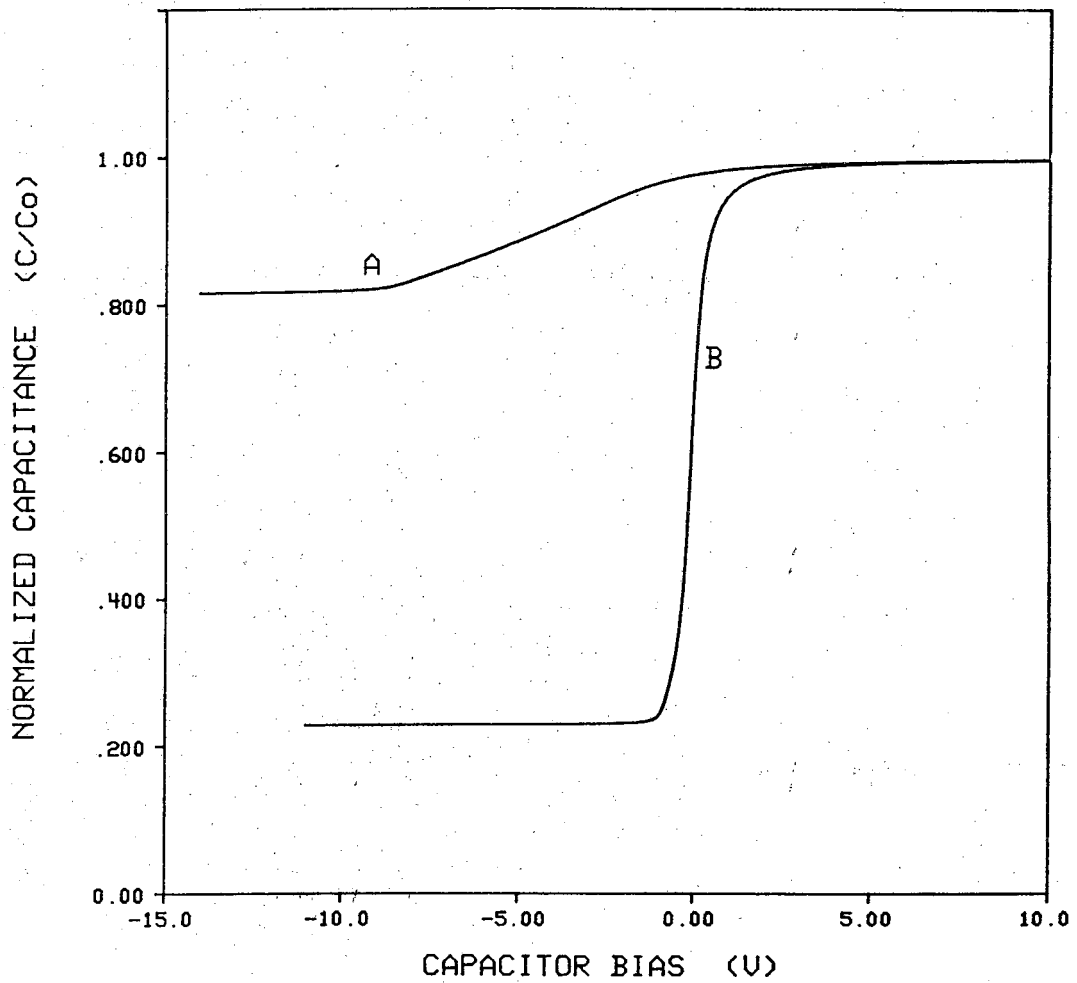
Figure 3.11

Normalized C-V curves for typical MOS capacitors
(A) highly doped (1.25×10^{17} /cm^3) n-type Si
(B) moderately doped (5.0×10^{14} /cm^3) n-type Si.

unoxidized silicon wafer through a photoresist mask at a concentration level of $8.0 \times 10^{12}/cm^2$ using an implant energy of 25 KeV. The implant concentration varies of course as a function of depth into the semiconductor. An estimate of the doping profile derived from the C-V profiling technique[*], however, indicates that the semiconductor may be approximately modeled as uniformly doped ($\sim 10^{17}/cm^3$) in the bias ranges of interest. As a result of the ion implantation, a periodic grating pattern of alternating highly doped and lowly doped semiconductor is established beneath the gate of the correlator. The periodicity of the grating corresponds to 5 μm wide storage regions separated by 5 μm wide implanted regions. A simple electrical model for the correlator gate appears in Fig. 3.12, while Fig. 3.13 shows experimental C-V curves derived from an unimplanted wafer, a wafer implanted over its entire surface area, and a grating structure wafer. (The rise in the capacitance of the grating structure capacitance near -8.0 volts is caused by lateral effects.) It is apparent from the curves in Fig. 3.13, that one can select a bias voltage between -1.0 volts and -10.0 volts such that the inverted storage (non-implanted) regions will be electrically isolated from one-another by depletion regions in the implanted areas. This is the desired result as illustrated schematically in Fig. 3.14. The implant-isolated storage regions, however, in contrast to those formed by charge injection and trapping at the ZnO/SiO_2 interface[54], are established by a repeatable, well-controlled fabrication process and simple selection of the proper operating gate bias.

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* Performed by Dr. R. F. Pierret
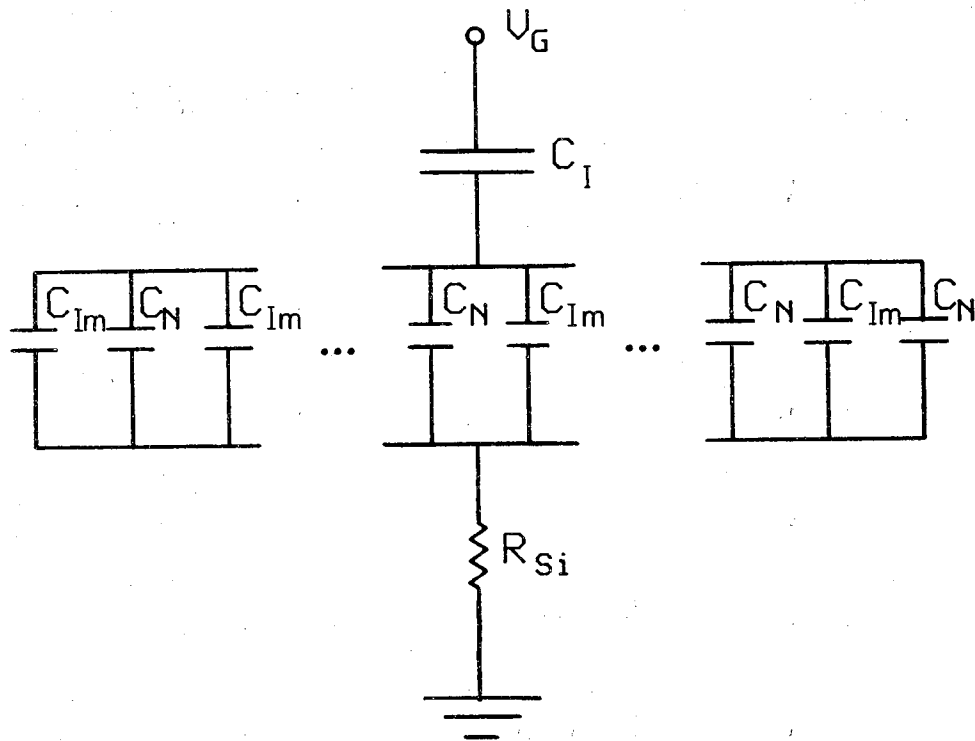
Figure 3.12

Electrical model for the gate of the implant-isolated storage correlator. The implanted and non-implanted regions are denoted by C_{Im} and C_N respectively. R_{Si} is the bulk silicon resistance and C_I is the combined oxide capacitance.
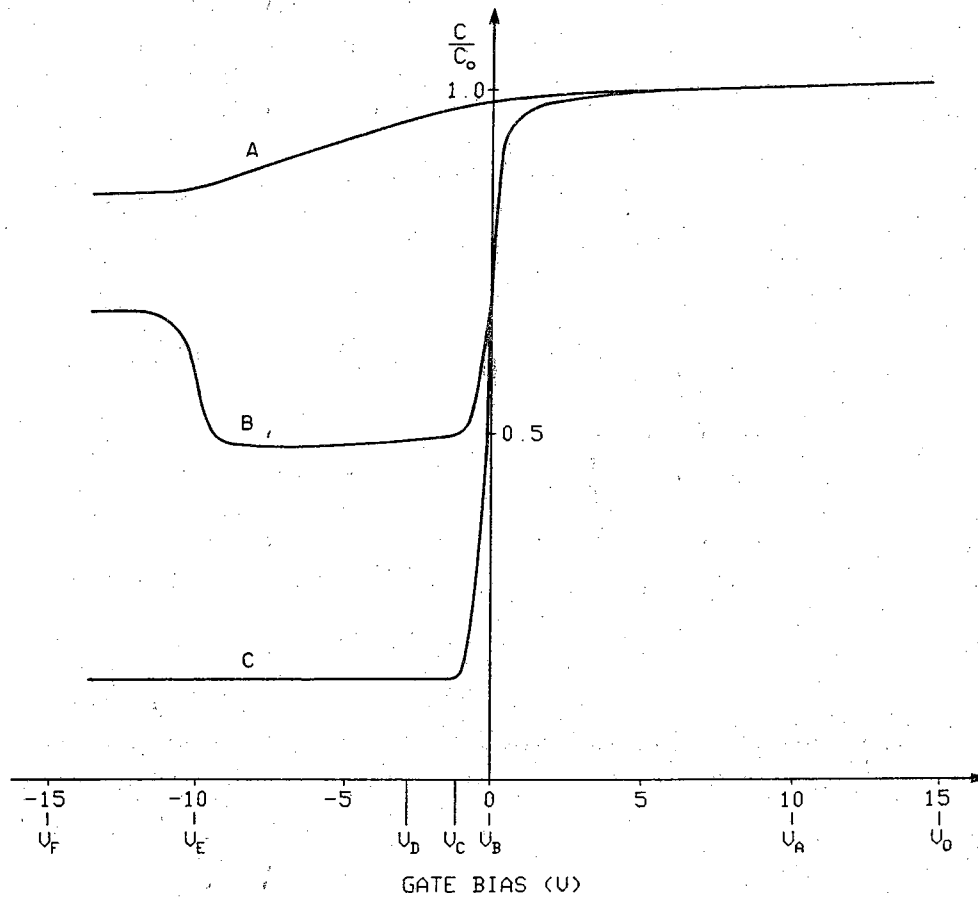
Figure 3.13

Experimentally determined C-V characteristics derived from a (A) totally implanted (B) combined (grating) (C) non-implanted wafer. (V_A, V_B, etc. refer to the curves in Figure 8)
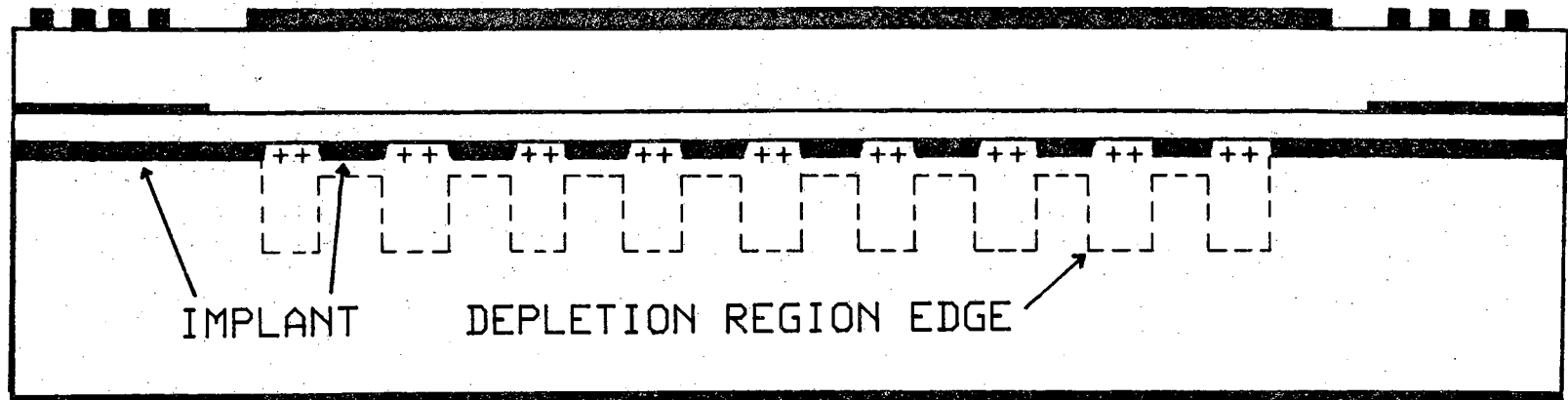
Figure 3.14

Schematic of charge storage regions (induced junctions). Plus signs denote inversion layer charge.

3.4.3 Verification of Storage Region Isolation

Subsequent to ion implantation, implant activation during thermal oxidation, and deposition of the shorting pad metallization, special gate-pattern test structures were formed directly on the oxidized silicon surface. The test structures were subjected to a post-metallization anneal* at 480 °C for five minutes to minimize the SiO_2/Si interface state concentration. Capacitance-versus-time (C-t) transient measurements were then performed on the SiO_2/Si system in order to determine the storage capability of the grating, and to examine the effectiveness of the implant in isolating the storage regions.

The C-t transient results can be readily explained with the aid of Figs. 3.13 and 3.15. Figure 3.15 shows a series of capacitance-versus-time characteristics of the grating region when pulsed from an equilibrium state at $V_G = V_o$ (accumulation) to various voltages (V_A, V_B, etc.) labeled in Fig. 3.13. Trace A shows the result of pulsing the capacitor from the accumulation reference bias V_o, to an applied bias which is still in accumulation. As expected, there is no change in capacitance with time. Similarly for Curve B, when both the storage and isolation regions are depleted the $t > 0$ capacitance is time independent, but is lower because of the increased depletion widths of the two regions. Once the device is pulsed such that the non-implanted region beneath the gate is inversion biased (curve C), the sudden pulse causes a deep depletion condition in the non-implanted region with an accompanying finite relaxation time back to equilibrium. The difference in the C-t transient of curves C and D is that a larger negative pulse causes a greater degree of depletion in the implanted region and also a greater deep depletion width in

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* Developed by Dr. R. D. Cherne and Dr. R. F. Pierret
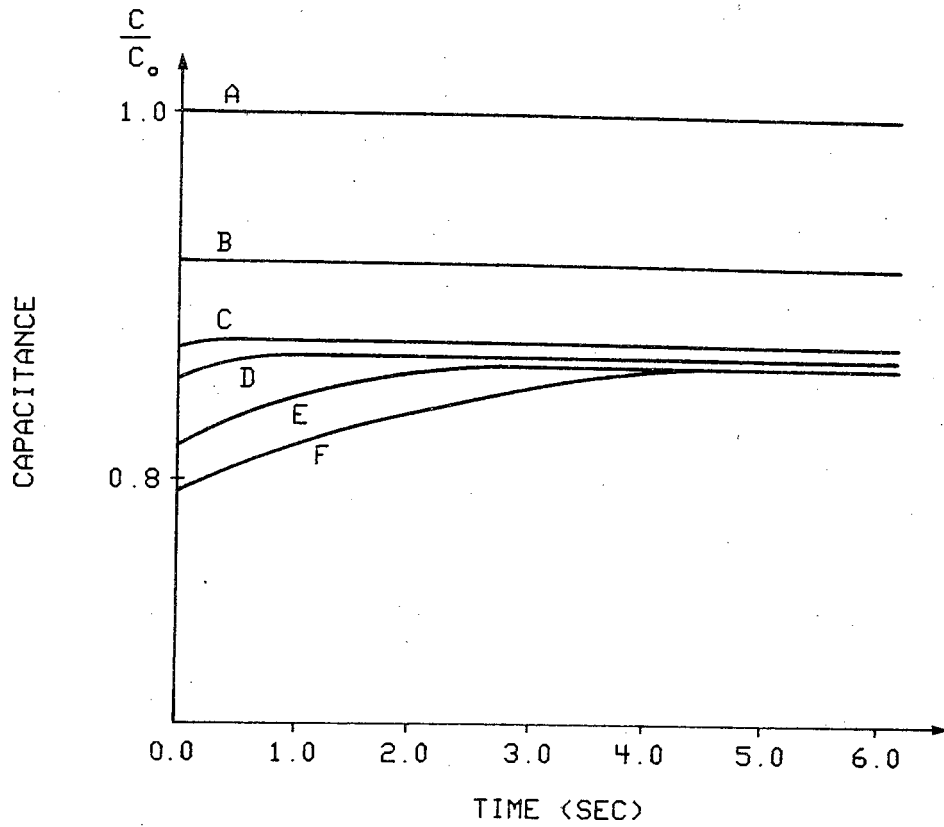
Figure 3.15

Capacitance versus time (C-t transient) results for applied pulses described in the text.

the non-implanted regions. After relaxation, the non-implanted depletion widths remain at their maximum values. However, the total equilibrium capacitance is lower due to the larger depletion width in the implanted region. Once the gate is pulsed from accumulation to a bias tending to invert both the implanted and non-implanted regions, the total capacitance always relaxes to the same minimum value as exemplified by Curves E and F. This is true even though a larger negative pulse deep depletes the capacitors farther and for a longer time. The existence of a biasing range where the device relaxes to a decreasing final capacitance, followed by a biasing range where the final capacitance is always the same independent of bias, is direct verification of the underlying device concept -- implant isolation of the storage regions. The biasing range over which the device relaxes to a decreasing final capacitance corresponds, of course, to the set of biases used in the normal operation of the storage correlator.

It should be noted that ion implantation is a well defined process with excellent repeatability. Even slight variations in dose or energy level, however, would not affect the implant-isolated storage correlator because signal storage occurs in the non-implanted regions. Variations in implant parameters, however, would have a noticeable effect upon the operation of a pn diode correlator.

3.5 The Writing Process

Several methods for writing a reference signal into the storage regions of a device have been demonstrated including the flash mode[15] and various rf writing techniques[55]; we limit ourselves to the rf gate-acoustic writing mode for the implant-isolated storage correlator. As mentioned in Section 3.3.2, the rf

gate-acoustic writing method involves the application of an rf signal of short duration to the gate of the correlator while the reference signal to be stored is propagating beneath the gate. The resultant electrical potential in the gate region during the writing process has components of potential due to the acoustic reference signal, $V_a(t)\cos(\omega t - kz)$, (launched by a transducer) and the writing signal, $V_g(t)\cos\omega t$, applied to the gate. Both signals contribute to the total gate potential associated with the writing process which is given by

$$V_S(z,t) = \sqrt{v_a^2 + 2v_a v_g \cos kz + v_g^2}\,\cos(\omega t - \phi) \quad , \qquad (3.10)$$

where

$$\phi = \tan^{-1}\left(\frac{v_a \sin kz}{v_g + v_a \cos kz}\right) \quad . \qquad (3.11)$$

Here v_a and v_g are the acoustic signal and gate signal potentials referenced to the gate[65]. As will be described below, $V_S(z,t)$ determines the surface charge density during a write sequence for any (z,t).

In this section a simple model is presented to describe the information storage process. At any point in the gate region during the writing process, the applied signal appears as a constant amplitude time varying sinusoid. To gain physical insight into the operation of a storage array, we first examine the response of the inversion layer charge and depletion capacitance of a single element of the storage region (located at $z = z_0$) to a narrow (much shorter than one rf period) pulse applied to the gate. After analyzing the effect of a narrow pulse, each period of the rf signal of Eq. 3.10 is treated as a discretized sequence of narrow pulses as shown in Fig. 3.16. Using this discretized representation, the charge storage in response to any time varying writing signal can be estimated.

$$V_s(z_o, t)$$
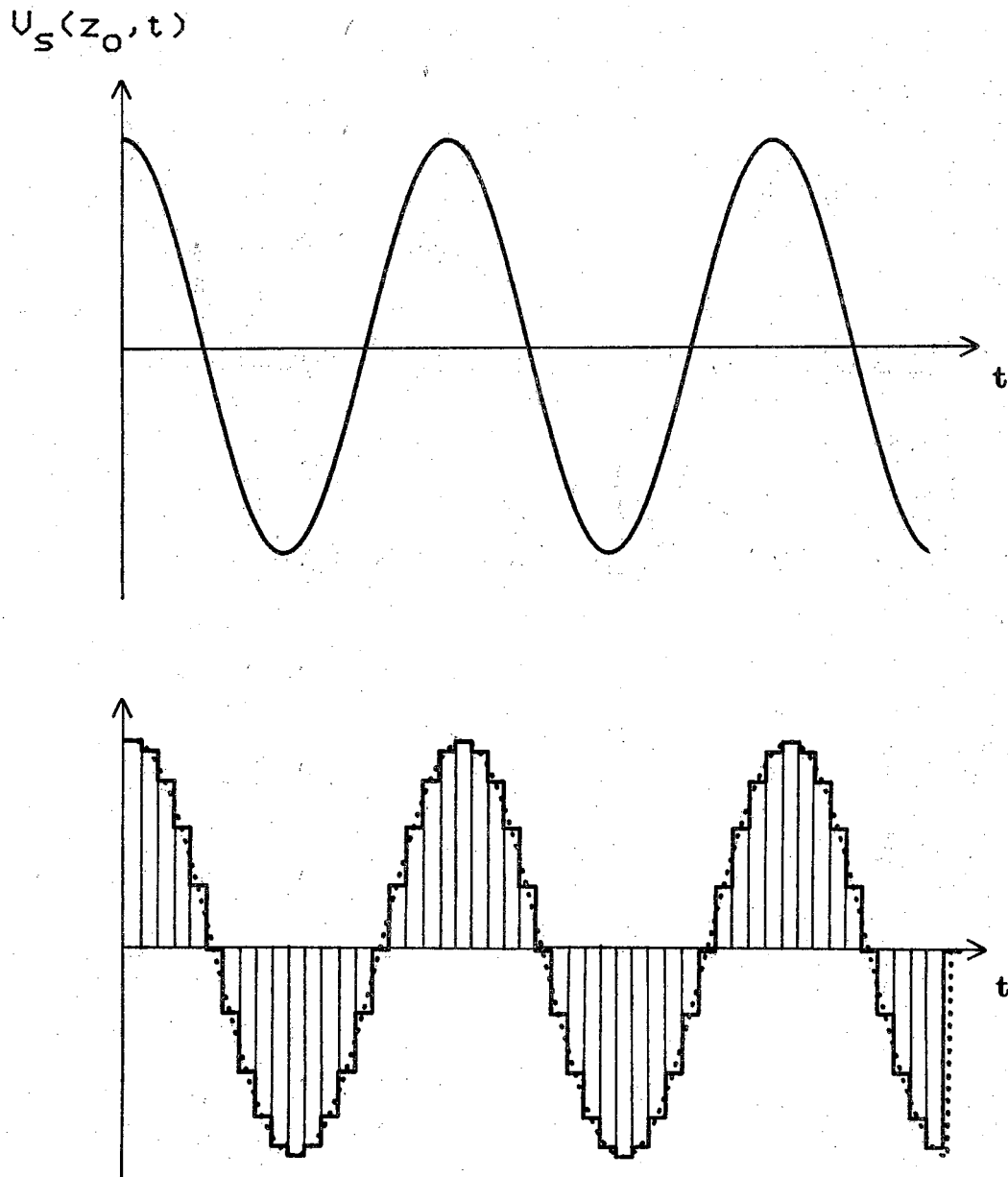
Figure 3.16

Applied writing signal at a single storage region (a) actual signal and (b) discretized signal approximation.

3.5.1 Charge Storage

Consider the effect upon a single storage region resulting from the application of a narrow positive pulse at the gate of a device which is biased for normal operation. Under equilibrium inversion conditions there is a maximum depletion width in the silicon. Application of a short duration positive pulse to the gate while it is under equilibrium inversion bias will cause the storage region depletion width to narrow by some amount dependent upon the pulse amplitude and duration; at the same time, minority carrier holes in the inversion layer will be injected into the semiconductor depletion region where some will recombine. Termination of this pulse causes the depletion width to instantaneously assume a new value equal to its equilibrium width plus an increment dependent upon the amount of minority carriers which recombined during the pulse. The change in depletion width changes the capacitance of the storage region, thereby contributing to signal storage in much the same way as in a pn diode memory correlator.

In a quantitative description of the charge storage process, some assumptions have been made regarding the recombination and generation of minority carriers in the silicon. Herein it is assumed that the recombination rate of injected holes, crucial to information storage, can be modeled by an effective recombination lifetime, τ_R. Moreover, the generation of carriers during a narrow negative pulse (part of the negative going portion of the writing cycle) can be neglected because, as is obvious from the lengthy storage times, the return to equilibrium is very slow compared to the writing recombination rate. Surface states, traps in the semiconductor and ZnO, and charges in the oxides will also be neglected because they complicate the analysis without offering any insight into the writing process. With the stated assumptions, a quantitative

description of the charge storage process has been performed (outlined below) for a single storage region.

As discussed in Section 3.4, proper operation of this device is dependent upon the selection of an appropriate operating point gate bias. Assuming that a bias of V_G has been applied to the gate, one can, using the δ-depletion approximation[66], calculate the inversion layer charge at the silicon surface. Because the ZnO layer is only semi-insulating, the d.c. charge applied to the gate is readily injected into the ZnO film and is subsequently stored in traps adjacent to the ZnO/SiO$_2$ interface; i.e., under steady-state conditions a virtual gate is formed at the ZnO/SiO$_2$ interface[63]. The ZnO layer, therefore, can be neglected when calculating the equilibrium minority carrier inversion layer charge density whose magnitude is given by

$$Q_{seq} = C_o \left[V_G - \frac{2kT}{q} U_F - \frac{qN_D}{C_o} \sqrt{\frac{4\kappa_s \epsilon_o}{qN_D} \frac{kT}{q} \left| U_F \right|} \right] \quad , \quad (3.12)$$

where C_o is the capacitance (per unit area) of the SiO$_2$ layer, N_D is the background doping level of the n-type silicon substrate, and U_F is the substrate doping parameter. The dielectric constant of the silicon is represented by κ_s, the temperature by T, ϵ_o is the permittivity of free space, and k is Boltzmann's constant. The constant U_F is given by

$$U_F = - \ln \left(\frac{N_D}{n_i} \right) \quad , \quad (3.13)$$

where n_i is the intrinsic carrier concentration.

Due to the localization of injected charge at the ZnO/SiO$_2$ interface, the equilibrium inversion layer charge under dc bias is independent of the ZnO layer capacitance. However, this is not true of the inversion layer charge

density when there are rapid changes in the gate bias. For rf signals in the frequency range of interest, voltage changes are too fast for the gate-injected electrons to follow the applied signal. Hence the capacitance of the ZnO layer must be included in any calculation of the redistributed surface charge. The condition just described can be visualized more easily with the aid of Fig. 3.17. In this figure, the solid curve represents a normal C-V characteristic for an n-type semiconductor; V_G is the bias point. In a normal MOS capacitor one would have to pulse the gate to some bias greater than V_T to move out of inversion and into depletion. In the case of a correlator with an injecting ZnO film, however, the gate must be pulsed to $V_{T_{eff}}$ (on the dashed curve) to be at the edge of inversion. For comparison to the redistributed charge it is therefore more convenient to rewrite the equilibrium inversion layer charge density (Eq. 3.12) for a given gate bias V_G in terms of $V_{T_{eff}}$ and C_I (the series combination of the ZnO and SiO_2 capacitances). The resulting equivalent expression for Q_{seq} is given by

$$Q_{seq} = C_I \left[V_G + V_{T_{eff}} - \frac{2kT}{q}U_F - \frac{qN_D}{C_I} \sqrt{\frac{4\kappa_s \epsilon_o}{qN_D} \frac{kT}{q} \left| U_F \right|} \right] \quad (3.14)$$

where

$$C_I = \frac{C_{SiO_2} C_{ZnO}}{C_{SiO_2} + C_{ZnO}} \quad . \quad (3.15)$$

The analysis of the charge storage process deals with the redistribution of this surface charge in response to an applied signal.

The application to the gate of a narrow positive pulse of amplitude V_A will cause a portion of the equilibrium surface charge to be injected into the semiconductor where some of it will recombine. The amount of charge which
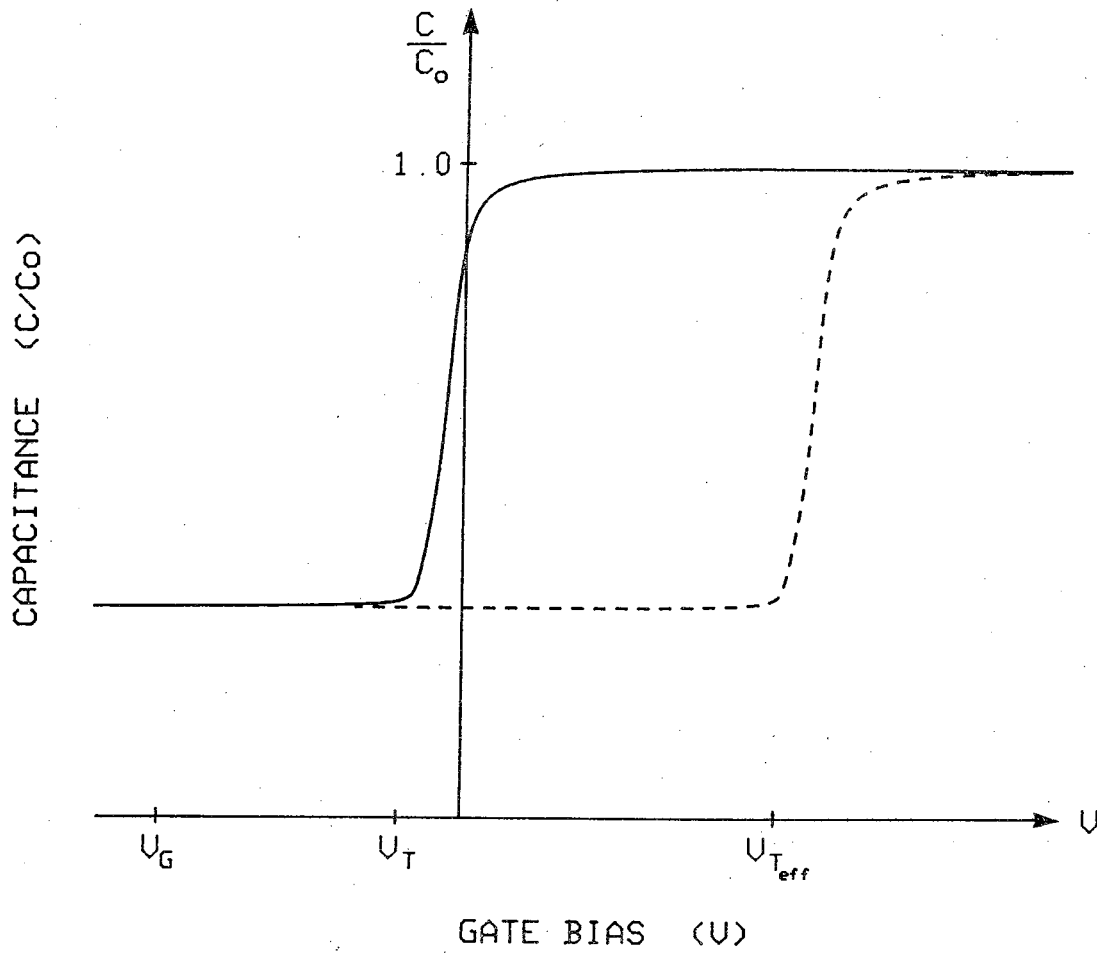
Figure 3.17

C-V characteristics of a typical MIS capacitor (solid curve) and an MZOS capacitor exhibiting charge injection into the ZnO.

recombines per pulse is dependent upon the pulse amplitude, pulse duration, the minority carrier recombination rate, and the inversion layer charge available prior to each pulse. Repeated applications of such a pulse within an interval that is short compared to the device storage time ($\tilde{\ }$ 1 sec) eventually leads to a "steady-state" deep depletion condition beneath the gate where the new inversion layer surface charge density, Q_A, saturates at

$$Q_A = C_I \left[V_G - V_A + V_{T_{eff}} - \frac{2kT}{q}U_F - \frac{qN_D}{C_I} \sqrt{\frac{4\kappa_s\epsilon_o}{qN_D} \frac{kT}{q} \left| U_F \right|} \right] \quad (3.16)$$

For a given V_A, the maximum charge storage by one storage region in the implant-isolated correlator is therefore

$$\Delta Q = Q_{seq} - Q_A = C_I V_A \quad . \quad (3.17)$$

Assuming an effective recombination lifetime, the application of a dc pulse of amplitude V_A and arbitrary duration t_p changes the inversion layer charge by an amount

$$\Delta Q_s = C_I V_A (1 - e^{-t_p/\tau_R}) \quad . \quad (3.18)$$

The expression for the inversion layer surface charge as a function of gate bias, applied pulse magnitude, and applied pulse duration is given by

$$Q_s(V_G, V_A, t_p) = Q_{seq} - C_I V_A (1 - e^{-t_p/\tau_R}) \quad . \quad (3.19)$$

If one were to pulse the device again immediately after the application of the first pulse, the starting inversion layer minority carrier density would be $Q_s(V_G, V_A, t_p)$ instead of Q_{seq}. The subsequent surface charge after additional pulses would be dependent upon the pulse durations as well as the pulse amplitudes.

As mentioned above, the change in surface charge caused by recombination during a positive pulse of duration t_p results in an increase in the depletion width of the storage regions; the new depletion width is given by

$$W(V_G, V_A, t_p) = \frac{\kappa_s \epsilon_o}{C_o} \left[-1 + \left(1 + \frac{V_G - \frac{Q_s(V_G, V_A, t_p)}{C_o}}{V_\Delta} \right)^{1/2} \right] , \quad (3.20)$$

where

$$V_\Delta = \frac{\kappa_s \epsilon_o q N_D}{2 C_o^2} . \quad (3.21)$$

The modified depletion width corresponds to a decreased capacitance given by

$$C(V_G, V_A, t_p) = \frac{C_I}{1 + \frac{C_I}{C_O} \left[-1 + \left(1 + \frac{V_G - \frac{Q_s(V_G, V_A, t_p)}{C_o}}{V_\Delta} \right)^{1/2} \right]} \quad (3.22)$$

Thus far we have described a method for determining the change in the depletion capacitance of a single storage region in response to a narrow pulse applied to the device gate. To elaborate on the writing process, it is necessary to determine the effect of a time varying signal on the several hundred storage regions. That is, for a complete description of the writing function, one must define the depletion capacitance (stored charge) as a function of time and position. The treatment of a time varying signal is dealt with in Appendix A for a signal represented by a sequence of pulses of finite duration.

It is important to note that as a storage region becomes deep depleted it will eventually reach a steady-state saturation value. That is, as a storage region nears saturation, only the maximum portion of each rf cycle contributes

to the stored reference signal and the effective writing time of each signal decreases. We illustrate this with the aid of Fig. 3.18 which shows the deep depletion C-V characteristics for a single storage region during various stages of the writing process. Also shown in Fig. 3.18 are select rf writing cycles during the writing process showing which portions of the rf cycle actually contribute to signal storage.

3.6 Experimental Results

In the remainder of this chapter we present experimental results associated with our implant-isolated storage correlator. The writing sequence described for the gate-acoustic writing technique is shown in Fig. 3.19a along with the corresponding correlation output voltage after the application of a read signal to the gate. The correlation output shown in the photograph of Fig. 3.19b was obtained using identical writing and reading signals (128 MHz bursts of duration 1.0 μs). The time delay between read and write sequences was 10 ms. The duration of the output signal is 2.0 μs which, as expected, is twice the duration of the reading signal. Furthermore, the frequency of the output signal is 128 MHz, the same as the reading signal frequency.

To obtain the results shown in Fig. 3.19, an rf writing signal of 200 ns duration was used because it produced a maximum correlation output. It is important to note that simply increasing the duration of the writing signal does not necessarily increase the correlation output. Rather, the lengthy writing signal can upset the phase information previously preserved by the writing process. In Fig. 3.20 we show the variation of correlation output versus writing time for a single writing sequence. The maximum correlation output occurs for a short writing time and then decreases as the writing signal increases. The
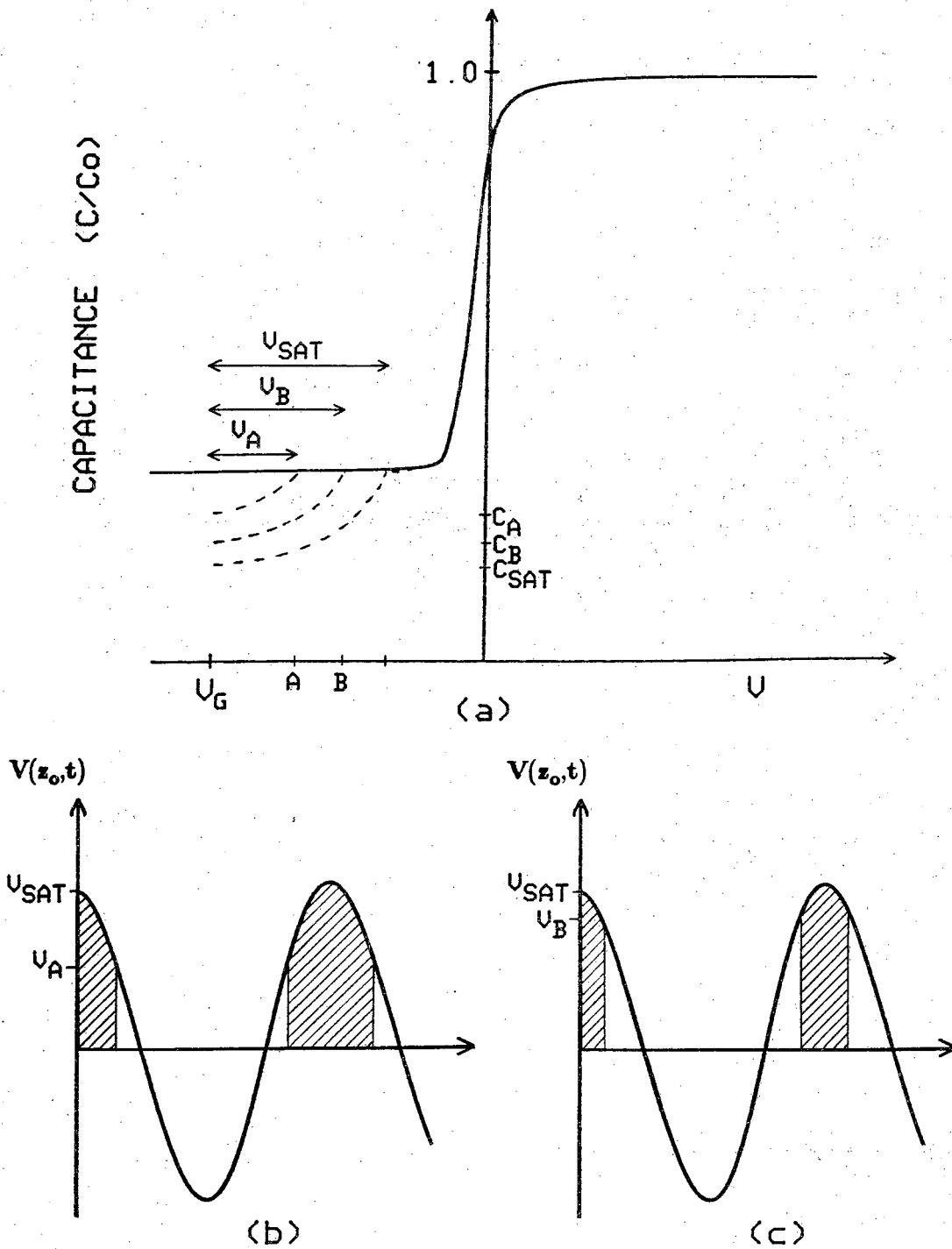
Figure 3.18

(a) C-V characteristics at different times during the writing process. (b)-(c) Portion of each writing cycle which contributes to signal storage is shown by the cross-hatching.
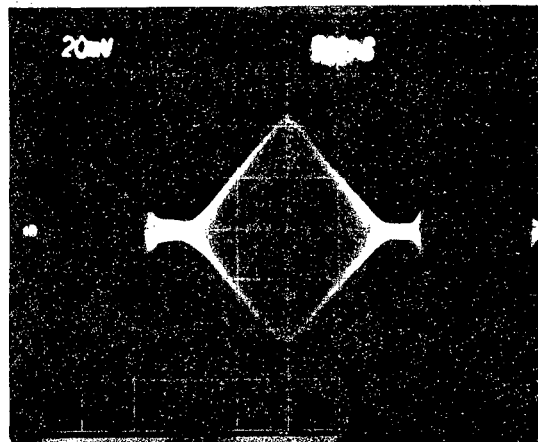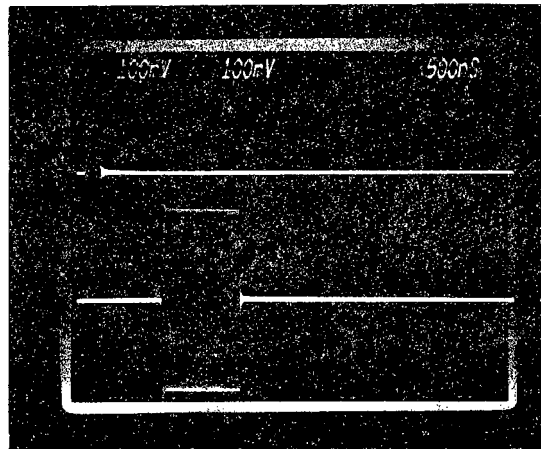
Figure 3.19

Memory correlation experiment (a) Write-in sequence consisting of an acoustic pulse (upper trace) and reference signal (lower trace). (b) Correlation output.
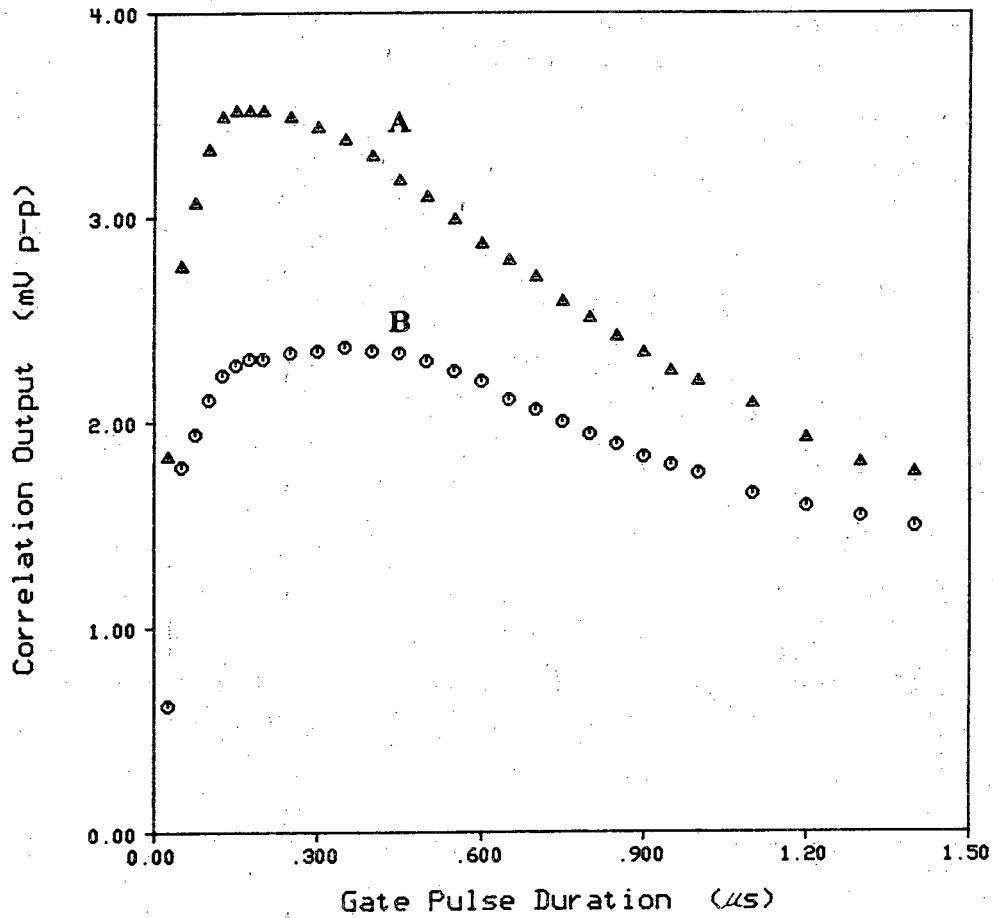
Figure 3.20

Correlation output vs. writing pulse duration for a reference signal power level of 30 dBm applied to the IDT and write pulse power, P_W, and read signal power, P_R, of (A) P_W = 37.1 dBm, P_R = 34.5 dBm and (B) P_W = 32.5 dBm, P_R = 29.5 dBm.

unexpected decrease in correlation output versus writing time for a single write sequence is due to phase slippage which is caused by the difference in the acoustic wave velocity between the implanted and non-implanted regions. To increase the effective writing time without the phase slippage problem, one must perform more than one writing sequence per readout. That is, to avoid phase slippage, one must write the same reference signal twice with write signal duration 0.2 μs to have an effective writing time of 0.4 μs.

In the photograph of correlation output shown in Fig. 3.19b, one can see not only the correlation output but also rectangular pulses 1.0 μs wide on both sides of the correlation output. The first rectangular signal is a direct rf pickup of the gate-applied reading signal at the output IDT. The rectangular signal which appears after the correlation output (3.0 μs after the first signal) corresponds to an acoustic signal launched by the input IDT caused by direct rf pickup of the read signal by the input IDT. Both of these spurious signals cause problems in the fabrication of SAW correlators and great amounts of effort have been taken to reduce these spurious levels. It should be noted that in a degenerate convolver, the spurious rf signals can be filtered out because the convolution output occurs at the sum frequency of the two inputs. In the memory correlator, however, the correlation output is at the same frequency as both the input signal and the reading signal which makes simple filtering impractical.

3.6.1 Effective Recombination Lifetime

As described in the previous section, the amount of charge stored in the gate region of the device is dependent upon the amplitude and duration of the write signal, the effective recombination lifetime, and many parameters which

are determined by the materials used. In this section an experimental method is presented for determining the effective recombination lifetime for the correlator.

To obtain the desired correlation output after a reference signal is stored beneath the gate, one applies the rf signal to be correlated at the gate electrode (gate-to-acoustic reading mode). This process is analogous to the reading process in a pn diode memory correlator[55]. Due to the spatially varying depletion capacitance, electric fields are established in the ZnO film which excite contra-propagating acoustic signals representing the convolution and correlation of the stored reference signal with the applied reading signal. Furthermore, it can be shown that the correlation output voltage is directly proportional to the amount of stored charge in the device. Therefore one can determine the effective recombination lifetime by fitting the predicted stored charge dependence of Eq. A.3 to the actual correlation output versus writing time.

To observe the variation of correlation output with write time, an experiment was performed using the gate-acoustic writing mode and the gate-to-acoustic reading mode. The reference and reading signals were of 1.0 μs duration and the writing signal duration was 0.2 μs. To vary the writing time, multiple writing sequences were performed in rapid succession prior to each reading sequence. The number of successive writes determined the effective writing time (200 ns writing pulse times the number of writes prior to each read). In this manner, the effective writing time is increased without degradation of the output due to phase slippage.

The writes were performed 20 μs apart so any storage region relaxation between write pulses can be ignored. The experimental variation of correlation

output versus write time is seen in Fig. 3.21. All values are normalized to the maximum value of correlation output. (It should be noted that in this experiment the time between readouts was several seconds to ensure sufficient decay of the stored signal before initiating a new write sequence.) The solid curve represents the predicted dependence of the correlation output voltage for an effective recombination lifetime of $\tau_R = 0.67$ μs as computed for the discretized sinusoidal approximation.

It should be noted that each of the inverted storage regions is very similar to a pn diode in that minority carrier injection governs the charge storage procedure. As such, the model for charge storage in the implant-isolated storage correlator can be applied directly to the pn diode correlator structure. A similar correlation output versus effective writing time experiment was performed by Tuan and Kino[65] for their pn diode storage correlator, enabling us to use their data to test our theory. We plot one minus the normalized correlation output versus effective write time for the pn diode memory correlator in Fig. 3.22. The data is plotted on a semi-logarithmic plot to demonstrate that the information charge storage process is not purely exponential. The non-exponential behavior is due to the time variation of the writing signal.

In addition to the data points presented in Fig. 3.22 for the pn diode device, Tuan's theoretical prediction for correlation output dependence is shown by the dashed curve in Fig. 3.22. The disparity between theory and experiment stems from the fact that, in Tuan's theory, each writing signal is treated identically with every other. We argue, however, that consecutive identical rf cycles of a writing signal will have different contributions to the writing of a reference signal because a smaller portion of later cycles contribute
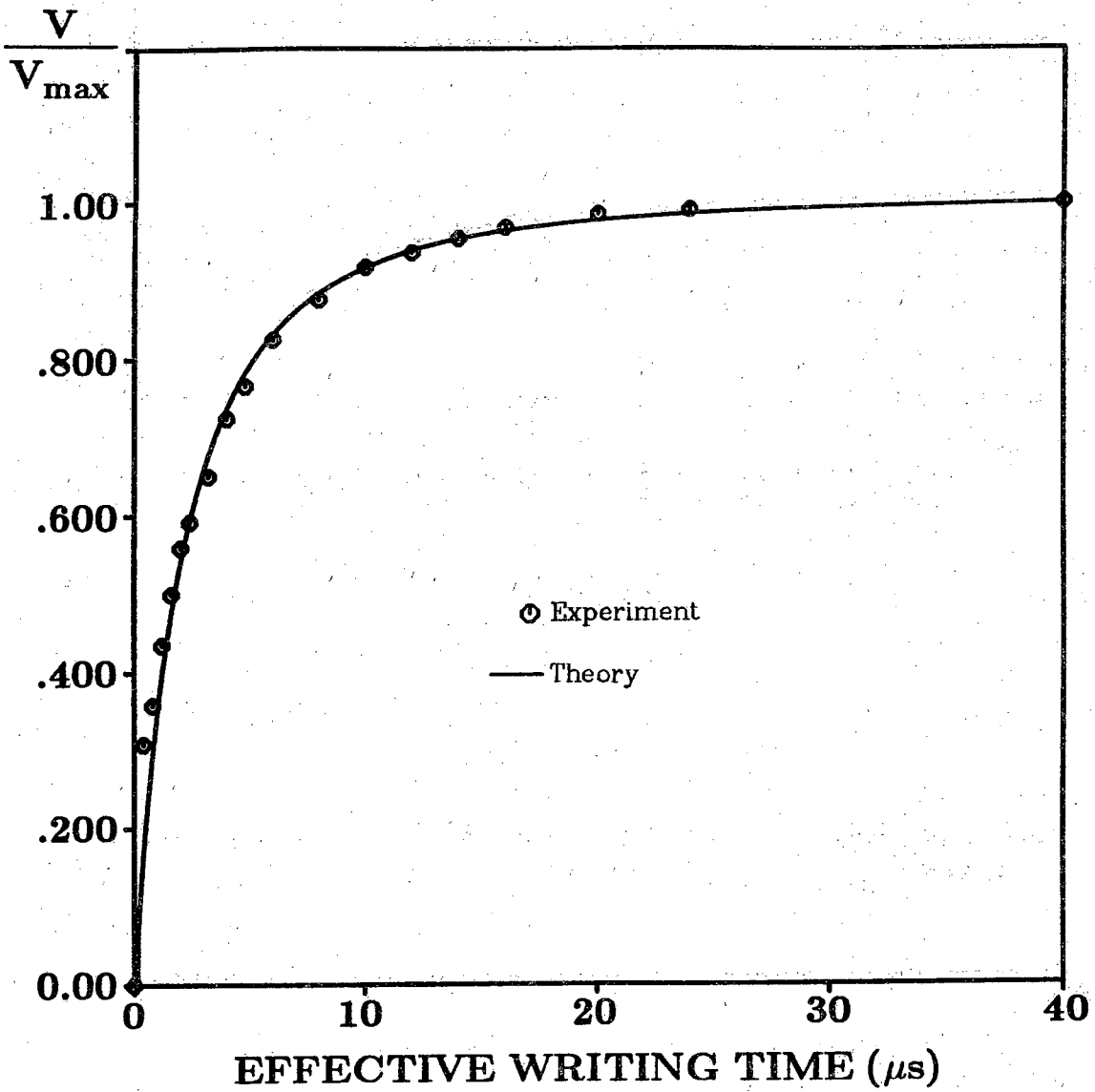
Figure 3.21

Normalized correlation output voltage versus effective writing time. Solid curve corresponds to an effective minority carrier lifetime of $\tau_R = 0.67$ μs.
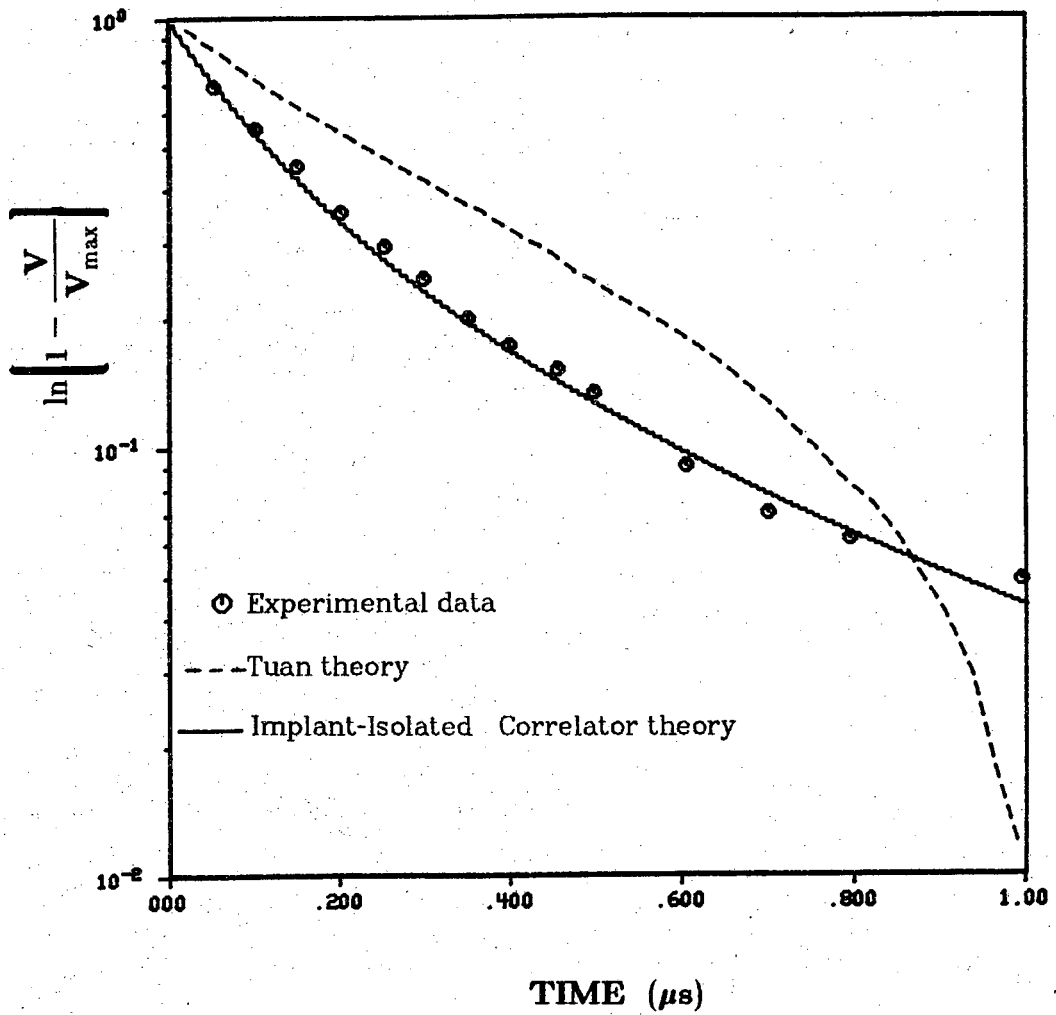
Figure 3.22

Normalized correlation output for a pn diode storage correlator employing multiple writes.

to signal storage as discussed in Section 3.5. In the implant-isolated storage correlator theory, each rf signal is treated independently and the charge storage prior to any writing cycle is taken into account in the computation of additional charge storage.

In Fig. 3.22 we plot the predicted normalized correlation output versus effective write time (solid curve) using an effective recombination lifetime of $\tau_R = 0.044$ μs. Our prediction for the pn diode device is within 3% of the experimental value at every point. It is interesting to note that in a fast charging system like the pn diode array correlator, fewer rf signals are necessary to saturate the diode storage regions. Careful inspection of our predicted curve for the pn diode correlator shows it to consist of many steps. Each of these steps represents the contribution from a separate rf cycle. There are 128 cycles depicted in Fig. 3.22. For the slower charging implant-isolated storage correlator, shown in Fig. 3.21, however, approximately 5000 rf cycles are necessary to saturate the device so the effect of individual cycles is not evident.

Thus, we have demonstrated the application of our theory for the implant-isolated storage correlator and obtained excellent agreement with experiment. Furthermore, our theory, when applied to the pn diode storage correlator, gives good agreement even for a much faster charging system.

3.6.2 Operational Characteristics

In this section we present experimental results for the correlation of two 1.0 μs rf bursts in order to examine correlator storage time, dynamic range and efficiency. All correlation measurements were performed using the rf gate-acoustic writing mode and the gate-to-acoustic reading mode. It should be

pointed out that the implant-isolated storage correlator presented in this report is bias stable; results of all correlation measurements are totally repeatable at any time without any special precautions, irrespective of the previous gate bias.

A key feature of the implant isolated correlator device is the time the device is capable of storing a reference signal. Figure 3.23 displays the correlation output versus storage time; the data points fall along the dashed curve which corresponds to a 3 dB storage time of 0.56 seconds. Although this is certainly a long storage time compared to other previous MZOS correlator configurations, with advanced fabrication procedures it is not unreasonable to expect storage times of at least several seconds.

A plot of normalized correlation output versus gate bias is shown in Fig. 3.24 for three different values of read-write power level combinations. It is seen that for gate biases less than a certain value, the correlation output always remains within 85% of its maximum. This indicates a very wide bias range over which one may operate the device without significant degradation of the output signal. Based on theoretical considerations, one might expect that once the d.c. gate bias was sufficiently large to invert not only the storage regions, but also the ion implanted separation (and lateral) regions, then the lateral flow of inversion layer minority carriers from implanted regions surrounding the storage areas would eliminate the stored signal. The experimental result presented, however, indicates that the implanted region is of insufficient area to supply the signal eliminating flow of minority carriers. The top surface of the device after sawing and mounting extends approximately one millimeter to either side of the one millimeter wide gate. This area is subject to lateral effects and should contribute to the overall relaxation, but it is apparently too small to degrade the output significantly.
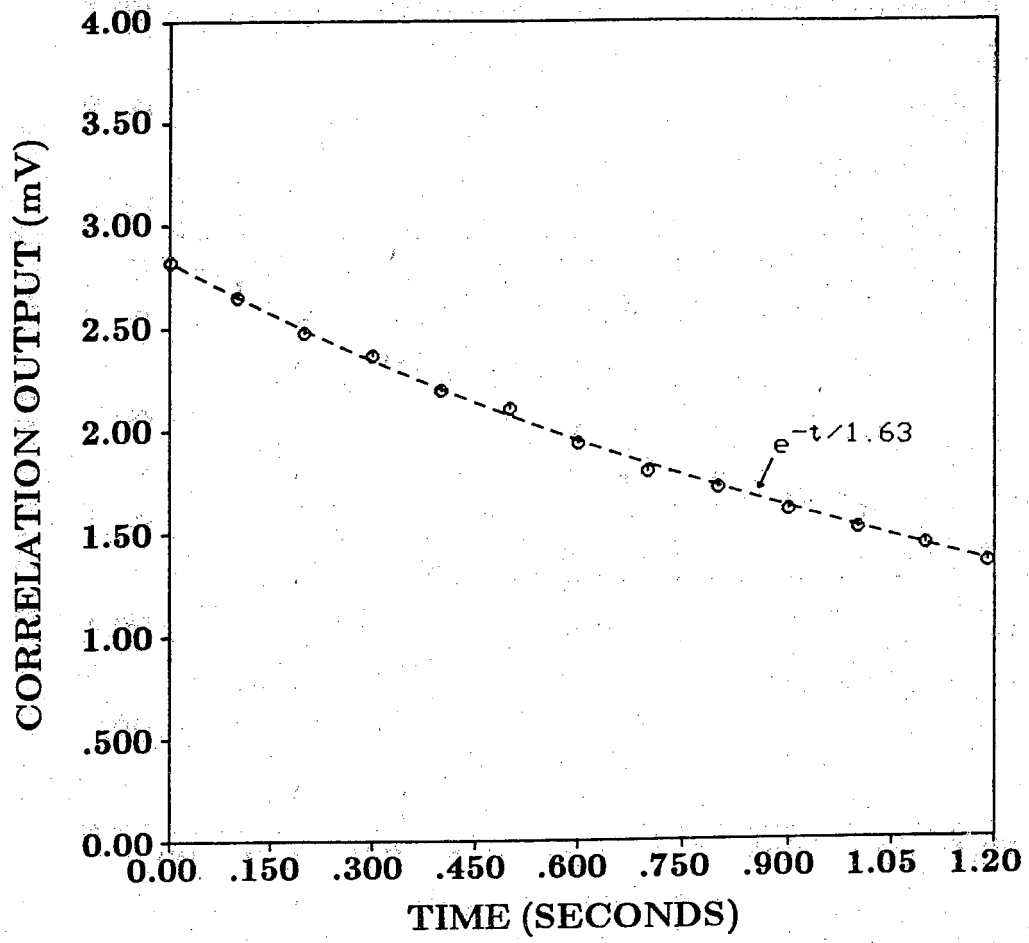
Figure 3.23

Correlation output versus storage time.
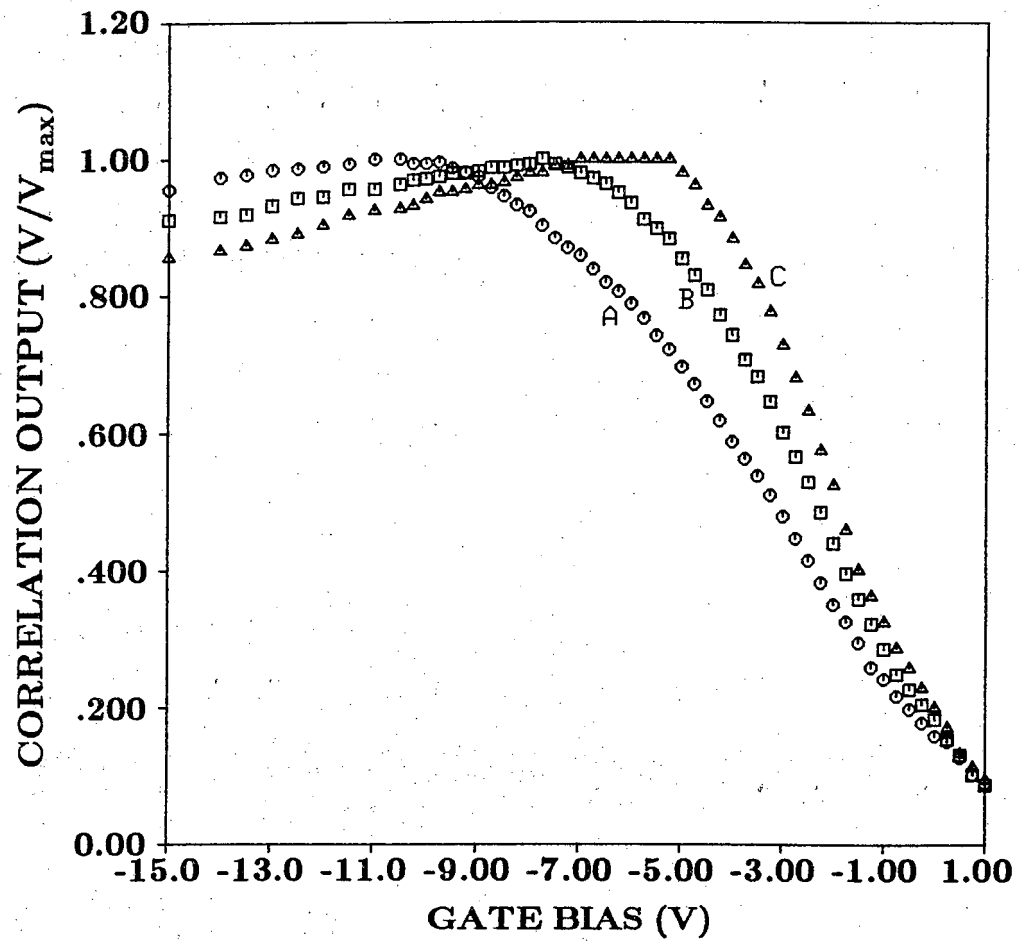
Figure 3.24

Correlation output versus gate bias for different read-write power level combinations

(A) $P_W = 40.1$ dBm, $P_R = 36.7$ dBm

(B) $P_W = 37.1$ dBm, $P_R = 33.7$ dBm

(C) $P_W = 34.1$ dBm, $P_R = 30.7$ dBm.

An rf writing signal of 140 nanoseconds (18 cycles) was found to produce the highest correlation output, and this writing pulse duration was used when performing the correlation measurements shown in Fig. 3.25. Figure 3.25 shows the correlation output versus the reference signal amplitude and the result is linear over a 25 dB range in correlator output power. The dynamic range is limited on the low power end due to noise and spurious signal levels and on the high power end measurements were halted before exceeding the power limitation of the IDT. The correlation output versus read pulse power can be seen in Figure 3.26, here again the dynamic range of the device is approximately 25 dB. It is the dynamic range of the output power with respect to the read signal power which is important in signal processing applications. In all measurements the correlation efficiency is between -100 and -110 dBm. The efficiency and dynamic range of this device are lower than expected. ZnO film quality during this particular sputter produced a delay line insertion loss some 14 dB more than in previous devices with the same dimensions. (The same was true for non-implanted test structures.) A better piezoelectric film should upgrade both figures of merit into the range of previously reported monolithic memory correlators.

3.7 The Implant-Isolated Device as a Degenerate Convolver

In addition to storage correlation and storage convolution, the implant-isolated device affords the possibility to perform degenerate convolution. The implant-isolated correlator is, afterall, identical to the standard monolithic $ZnO/SiO_2/Si$ convolver pictured in Fig. 3.3 with the addition of the ion implanted grating pattern in the interaction region. We wish to determine the
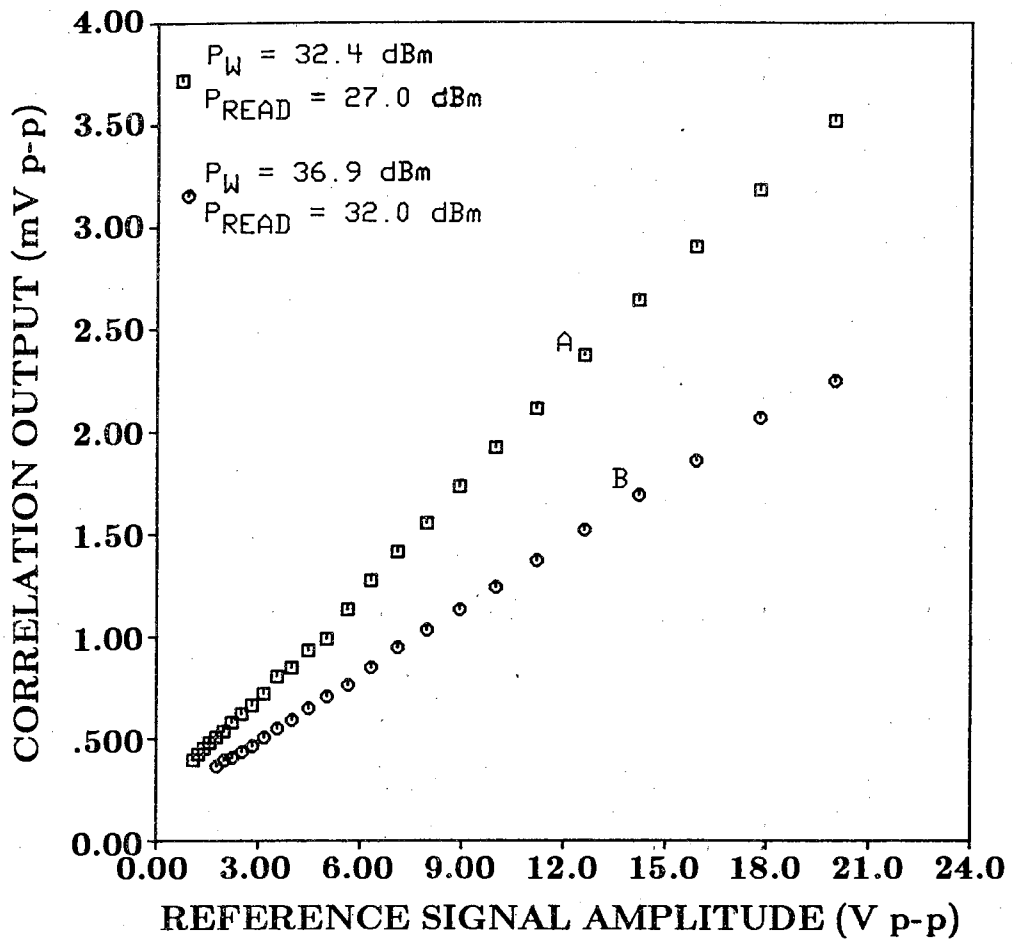
Figure 3.25

Correlation output versus reference signal amplitude.
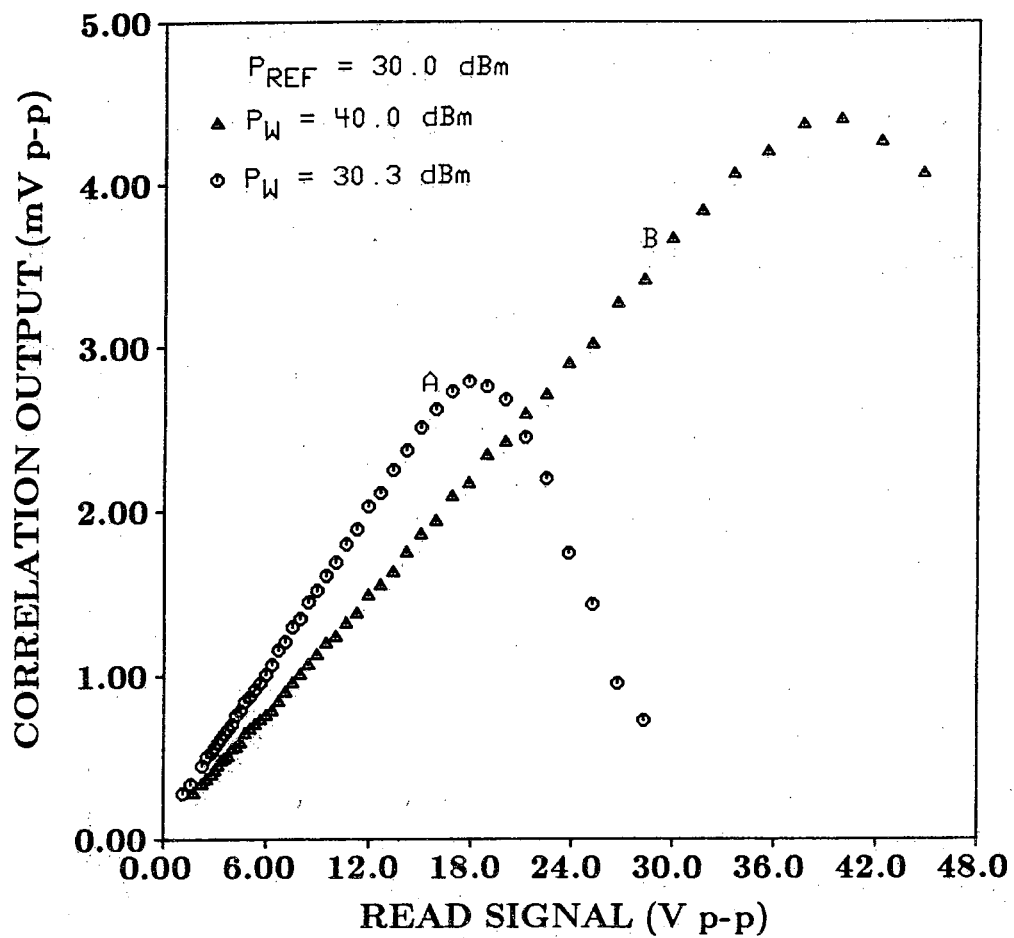
Figure 3.26

Correlation output vs. read signal amplitude.

effect of the ion implanted region on the degenerate convolution of the implant-isolated structure.

If again one considers the gate region to be made up of alternating regions of highly doped ($10^{17}/cm^3$) and lightly doped ($5 \times 10^{14}/cm^3$) n-type silicon, one can view the implant-isolated degenerate convolver as two uniformly doped independent convolvers connected in parallel. The power levels in each of the two convolvers would be half that found in the composite structure and each convolver would have different doping levels as mentioned above. Analyzing the implant-isolated degenerate convolution in this manner greatly simplifies the process since detailed convolver analyses have already been performed for uniformly doped monolithic convolvers. Using an existing convolver model, we determine the relative convolution efficiencies for these two differently doped convolvers.

3.7.1 Convolution Efficiency

The terminal convolution efficiency, F_T, is a figure of merit defined by

$$F_T = P_c - (P_1 + P_2) \; , \qquad (3.23)$$

where P_c is the convolution output power and P_1 and P_2 are the terminal input power levels applied to IDT 1 and IDT 2 respectively. Also known as the external convolution efficiency, F_T takes into account transduction loss, mismatch loss at the terminals, and propagation loss in the device. The internal convolution efficiency, however, does not include these additional losses and is a measure of open-circuit output voltage as a function of the acoustic power levels of the propagating surface waves. Since we assume identical convolver structures (same physical dimensions, electrical connections, coupling

levels, IDT configurations, etc...), the difference between the terminal convolution efficiency between a highly doped device and a lightly doped device will be due only to a difference in their internal efficiencies.

The literature is full of reports of different types of SAW convolvers and almost an equal number of theories explaining the operations of the devices. We take our results from Lo[19] as his structure is nearly identical to our device. Since a complete analysis has already been performed, we repeat only the result here for internal convolution efficiency, M, of a $ZnO/SiO_2/Si$ convolver which is given by

$$M = \frac{\sqrt{2}\left[1 + \frac{\epsilon_s}{\epsilon_{ox}}M_p\right]^2 M_k}{A^2} \left|\frac{\Delta v}{v}\right| \left|\left(\frac{1}{C}\right)\right| \left|\frac{dC}{dV_G}\right| , \qquad (3.24)$$

where M_p and M_k are constants associated with a device of particular dimensions[19] and $\frac{\Delta v}{v}$ is the electromechanical coupling constant. The quantity A is given by

$$A = \frac{1 + \frac{\epsilon_s}{\epsilon_o}\frac{M_p}{k}G(\phi_{so})}{1 + \epsilon_s\left[\frac{y_p}{\epsilon_{yy}} + \frac{y_o}{\epsilon_o}\right]G(\phi_{so})} , \qquad (3.25)$$

where $G(\phi_{so})$ is a function of the applied gate bias, ϵ_s, ϵ_o, and ϵ_{yy} are the permittivities of the silicon, SiO_2, and ZnO respectively. The thickness of the ZnO layer is given by y_p, and the SiO_2 layer thickness is y_o. The last two terms on the right side of Eq. 3.24 involve C, the gate capacitance of the composite structure, and V_G is the applied gate bias. A detailed explanation of all of the above parameters can be found in Lo[19].

At this point we use the expression of Eq. 3.24 to compute the relative internal convolution efficiencies of the highly doped and lightly doped regions. If the relative efficiencies are comparable in certain bias ranges, one would expect to observe contributions to the convolution from both type regions in the structure. If the relative efficiencies are very much different, then one would expect a significant contribution in only one-half of the area beneath the gate and hence a decrease in convolution efficiency of approximately 6 dB from what could be achieved if the entire silicon surface had been a single doping.

Since the calculation of convolution efficiency for a particular configuration depends upon knowledge of the capacitance versus voltage characteristics (Eq. 3.24), the C-V characteristics of devices with and without ion implantation were determined by digitizing actual C-V curves. From the C-V data we have determined the relative convolution efficiencies of the differently doped regions and normalized them to the maximum efficiency calculated. The results of this computation which are shown in Fig. 3.27 are informative yet not surprising. The maximum convolution efficiency was achieved for the lightly doped substrate configuration (curve D) and the maximum occurred when the silicon is in depletion. The heavily doped sample convolution efficiency (curve C) can be seen to dominate over a much wider range of operation than does the lightly doped device, yet the maximum efficiency for the highly doped region is two orders of magnitude lower than for the lightly doped silicon. The results of this computation indicate a contribution to the degenerate convolution in essentially just half of the interaction region so one would conclude that the maximum convolution efficiency attainable in the implant-isolated correlator structure is 6 dB less than the maximum for a uniformly doped device.
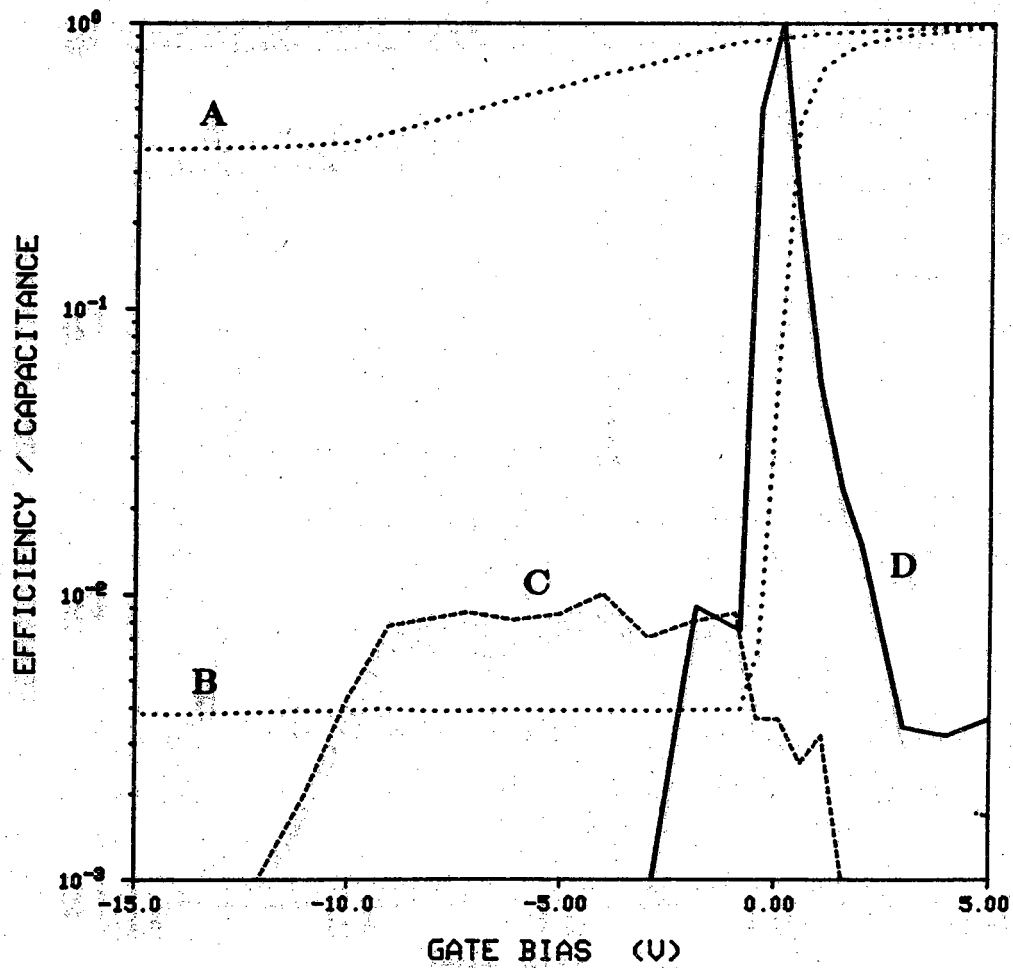
Figure 3.27

Internal convolution efficiency for (C) uniformly doped (10^{17} /cm^3) silicon substrate convolver and (D) uniformly doped (5×10^{14} /cm^3) silicon substrate convolver for the C-V characteristics of (A) and (B) respectively.

3.7.2 Experimental Results

To verify this result experimentally, convolution measurements were performed for both the implant-isolated structure as well as a non-implanted uniformly doped ($5 \times 10^{14}/cm^3$) convolver with the same dimensions and a ZnO film sputtered in the same run. Results of this experiment are shown in Fig. 3.28 with the efficiency of the non-implanted device ~4 dB greater than for the implant-isolated device. An explanation for the discrepancy between experimental results and our prediction stems from the fact that the implant-isolated device used in this experiment had non-implanted regions comprising approximately 60% of the interaction region. Thus, a greater portion of the gate area would contribute to the maximum convolution resulting in an expected difference of only ~4.4 dB from the maximum possible convolution output.

A plot of F_T versus gate bias is shown in Fig. 3.29 for an implant-isolated correlator. As expected, the maximum convolution output occurs for gate biases which deplete the non-implanted regions. For biases more negative, the implanted region dominates, as predicted from the calculation of internal convolution efficiency plotted in Fig. 3.27. It should be noted that although one doping region dominates the overall convolution efficiency in any particular bias range, the efficiencies are comparable for gate biases between -1V and -3V. This is indicated in Fig. 3.29 by the gradual transition from the maximum efficiency toward the region where the heavily doped device dominates.
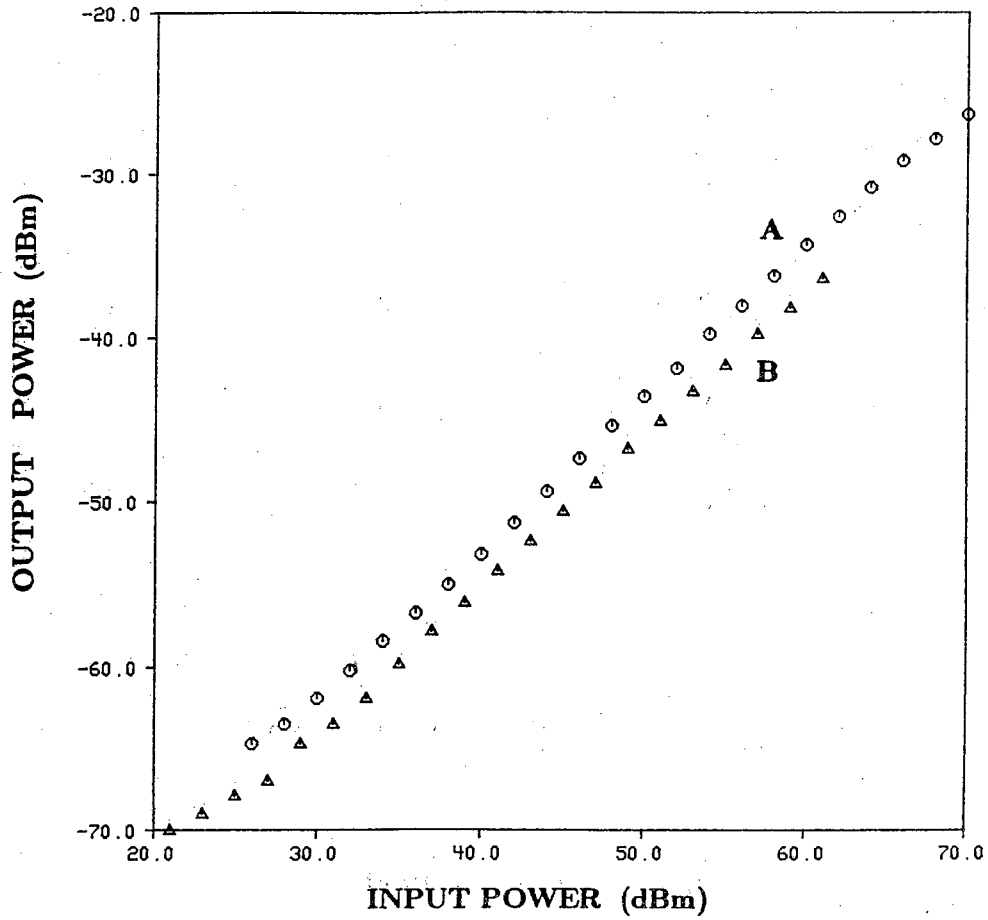
Figure 3.28

Convolution efficiency for (A) a uniformly doped $(5 \times 10^{14}/cm^3)$ convolver with no implants and (B) an implant-isolated storage correlator operated as a degenerate convolver.
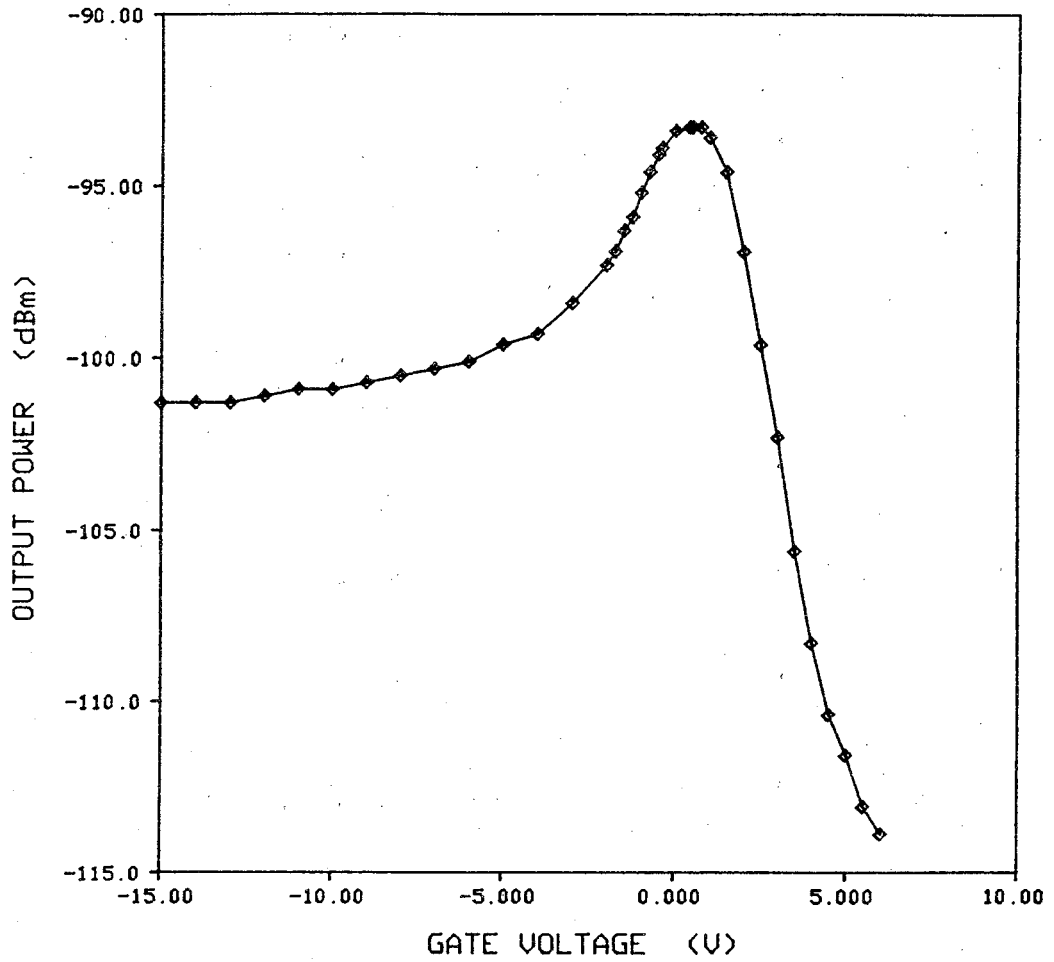
Figure 3.29

Terminal convolution efficiency for an implant-isolated storage correlator operated as a degenerate convolver.

3.8 Measurement of SAW Potential

In the design of nearly all devices fabricated in the layered $ZnO/SiO_2/Si$ configuration which utilize the interaction of the silicon carriers and the electric fields of the SAW, a knowledge of the silicon surface potential associated with the acoustic wave is essential. Information about the wave potential is invaluable in the design of convolvers and correlators as well as SAW charge transfer devices[67,68] and SAW CCD's[69]. We have designed an experiment in which the implant isolated storage correlator is utilized to determine this potential relative to transducer input power.

Beginning in an equilibrium state with the correlator gate biased at some value for normal operation, one has a condition in the gate region similar to that shown in Fig. 3.14. Application of any short duration positive signal will cause the injection of some minority carrier inversion layer charge into the semiconductor bulk where some will recombine. When the applied signal is no longer positive, the depletion regions will be changed by some amount dependent upon the amount of recombined holes resulting from the positive portion of the signal. As mentioned in Section 3.5, when the applied signal is a spatially varying standing wave pattern, information will be stored in the gate region. As described above, application of an rf gate-acoustic writing sequence introduces a gate potential V_g given by

$$V_g(z,t) = V_w \cos(\omega t - \phi) \quad , \tag{3.26}$$

where V_w, the writing signal is given by

$$V_w = \sqrt{v_a^2 + 2v_a v_g \cos(kz) + v_g^2} \quad . \tag{3.27}$$

The value v_a is the unknown magnitude of the acoustic wave potential referenced to the gate electrode and v_g is the magnitude of the gate-applied rf

writing signal. Whenever $V_g > 0$, there is information storage and a subsequent readout signal, R(t), gives the correlation between the stored reference signal and R(t), the readout signal.

It was noted that during negative going cycles of the applied writing signal, there is no contribution to the stored signal. Furthermore, after the presence of a negative signal component, the gate region will remain in exactly the same condition as it was before the negative signal was applied. If one were to apply a negative dc pulse of amplitude ΔV_G to the gate immediately prior to writing the reference signal and leave it on for the duration of the writing sequence, the total gate signal during the writing process would be

$$V_g(z,t) = V_w\cos(\omega t - \phi) - \Delta V_G \quad . \tag{3.29}$$

Clearly, if the applied pulse ΔV_G is greater than V_w, then no signal will be stored because $V_g(z,t)$ will always be negative. If, however, ΔV_G is less than V_w, it is possible to store a reference signal.

By actually applying a dc pulse ΔV_G during the writing process, a great deal of information about SAW signal levels can be determined. The effect of ΔV_G upon the writing process can be observed by monitoring the correlation output as a function of ΔV_G. As long as some signal is being written into the gate region (i.e. $\left|\Delta V_G\right| < v_a + v_g$), then the correlation output V_c is nonzero. While varying ΔV_G, the correlation output voltage disappears when $\Delta V_G = \Delta V_{G_T} = v_a + v_g$ where ΔV_{G_T} represents the threshold value at which the writing process will no longer store a reference signal.

The interesting feature about this observation is that, experimentally, ΔV_{G_T} and v_g can be measured directly at the gate, allowing v_a, the acoustic wave potential referenced to the gate, to be easily determined. The

experimental setup is diagramed in Appendix B. The experiment consists of the standard correlation experiment described in Section 3.6 (consisting of the gate-acoustic writing mode and the gate-to-acoustic reading mode) with the addition of a pulse ΔV_G applied to the gate just prior to the introduction of the writing signal. In the experiment, ΔV_G, the applied gate pulse, is varied during the writing process and the correlation output is monitored for each of the ΔV_G values. When the correlation output becomes zero, this implies that no signal is being written into the device and $\Delta V_G = \Delta V_{G_T}$.

3.8.1 Experimental Results

Experimental results of V_c versus ΔV_G are shown in Fig. 3.30. The shape of the curve can be explained with the aid of Fig. 3.31 which shows the gate signal during the writing process including the dc pulse, ΔV_G. Since only positive portions of the total signal contribute to the stored signal, the correlation output is extremely sensitive to the applied pulse magnitude. Furthermore, the stored writing signal (and hence the correlation output) is dependent upon not only the magnitude of the positive swing during writing but also the time duration of the positive signal because the amount of charge storage varies as $V(1 - e^{-\frac{t}{\tau}})$. Clearly, as ΔV_G becomes more negative, not only does the magnitude of the positive signal decrease but the effective writing time decreases as illustrated in Fig. 3.31. Thus, the change in correlation output with ΔV_G is dependent not only upon the change in writing signal magnitude but also writing signal time duration.

It is difficult to obtain an analytical expression for the effective writing time when the negative dc pulse is applied in addition to the writing sequence,
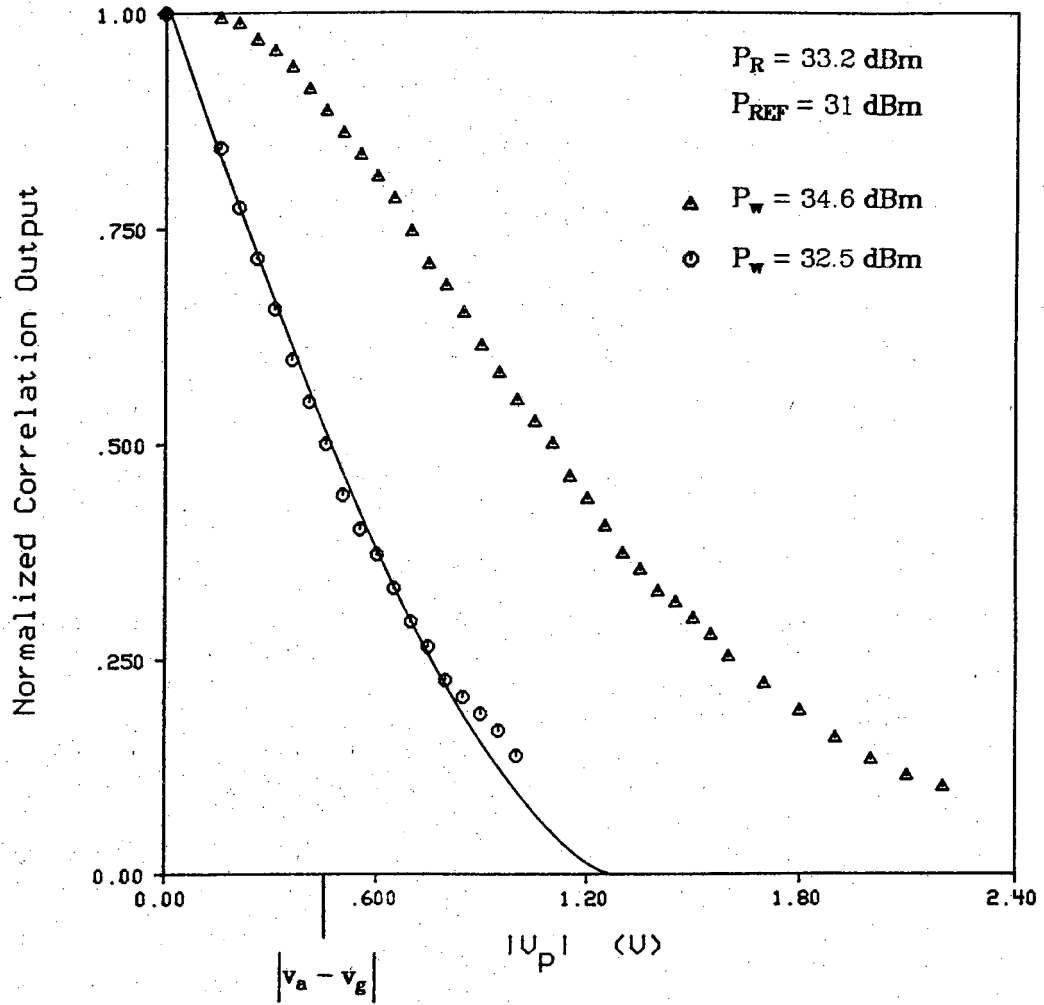
Figure 3.30

Correlation output versus negative pulse magnitude.
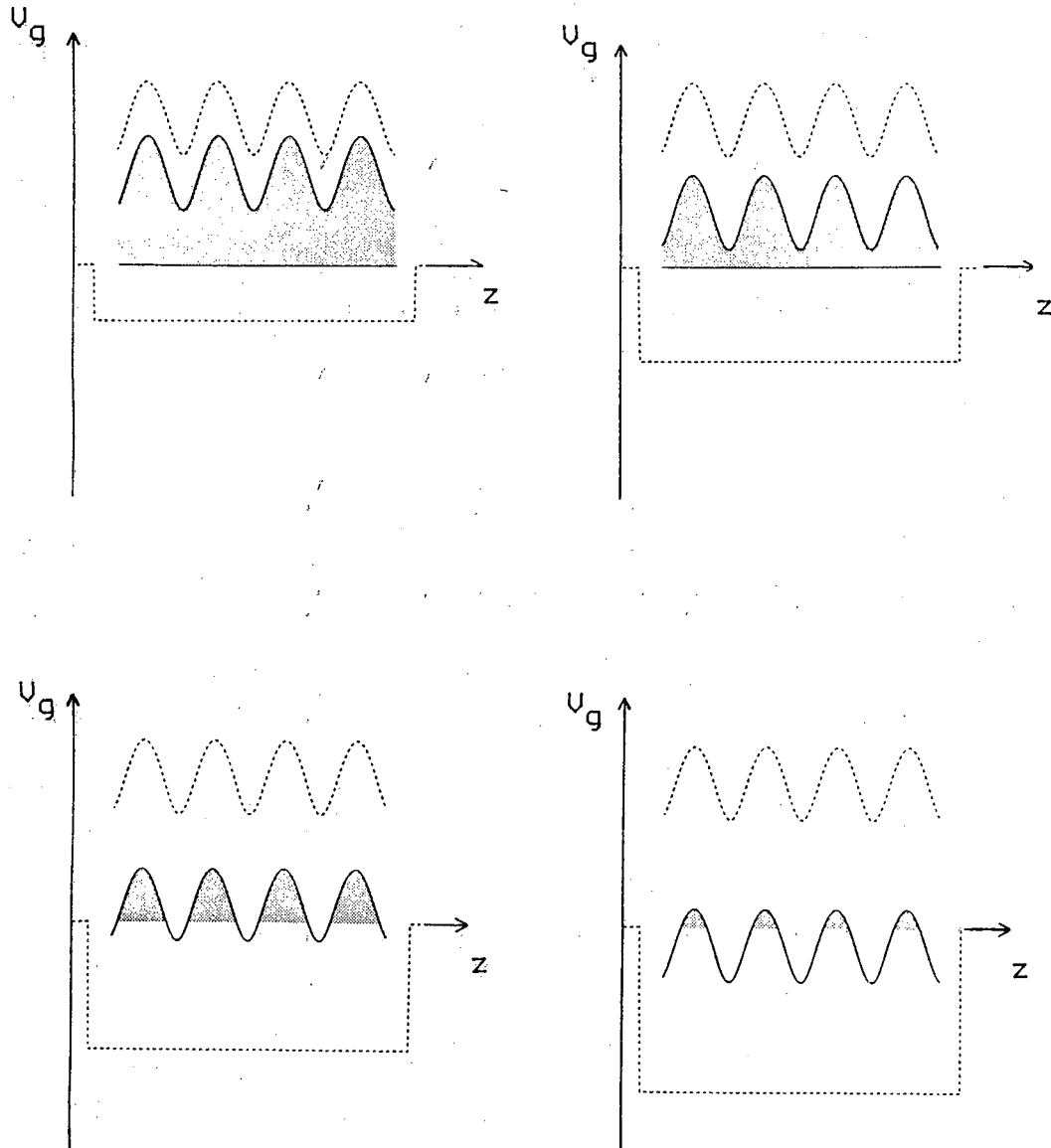
Figure 3.31

Total gate writing signal including pulse. The effective writing signal is shown in the shaded areas.

but it is easily calculated with the aid of a computer. Results of a predicted V_c versus ΔV_G (using the method of Section 3.5) are shown in Fig. 3.30 along with the experimental results. The nonlinear behavior of the plots is due to the fact that the effective writing time changes in response to ΔV_G as explained above. Furthermore, once $\Delta V_G > | v_a - v_g |$ as can be seen in Fig. 3.30, the reference signal becomes distorted because the lower portion of the writing signal is essentially cutoff. That is, for $| v_a - v_g | < \Delta V_G < | v_a + v_g |$, the stored reference signal will change drastically with changes in ΔV_G. The predicted points where $\left| \Delta V_G \right| = | v_a - v_g |$ are shown on each of the curves in Fig. 3.30.

In the experiment, v_g and ΔV_G were measured at the gate of the device using an rf voltmeter. From these values we compute v_a for many different acoustic signal power levels. In Fig. 3.32 we show the gate-referenced acoustic wave potential as a function of IDT terminal voltage for an operating point gate bias of -10V. Because of the dependence of the acoustic wave attenuation on the silicon surface potential, one would expect the acoustic potential versus transducer potential to be dependent upon gate bias.

3.9 Electronic Erasure

To be useful as a signal processing device in practical applications, the storage correlator must be able to process signal comparisons at a very high rate ($>$ KHz). Since signals can be stored for more than seconds and the reading process is non-destructive, the memory correlator must have a mechanism by which the no-longer-needed reference signal can be erased prior to the occurrence of an ensuing writing sequence. In other correlator structures
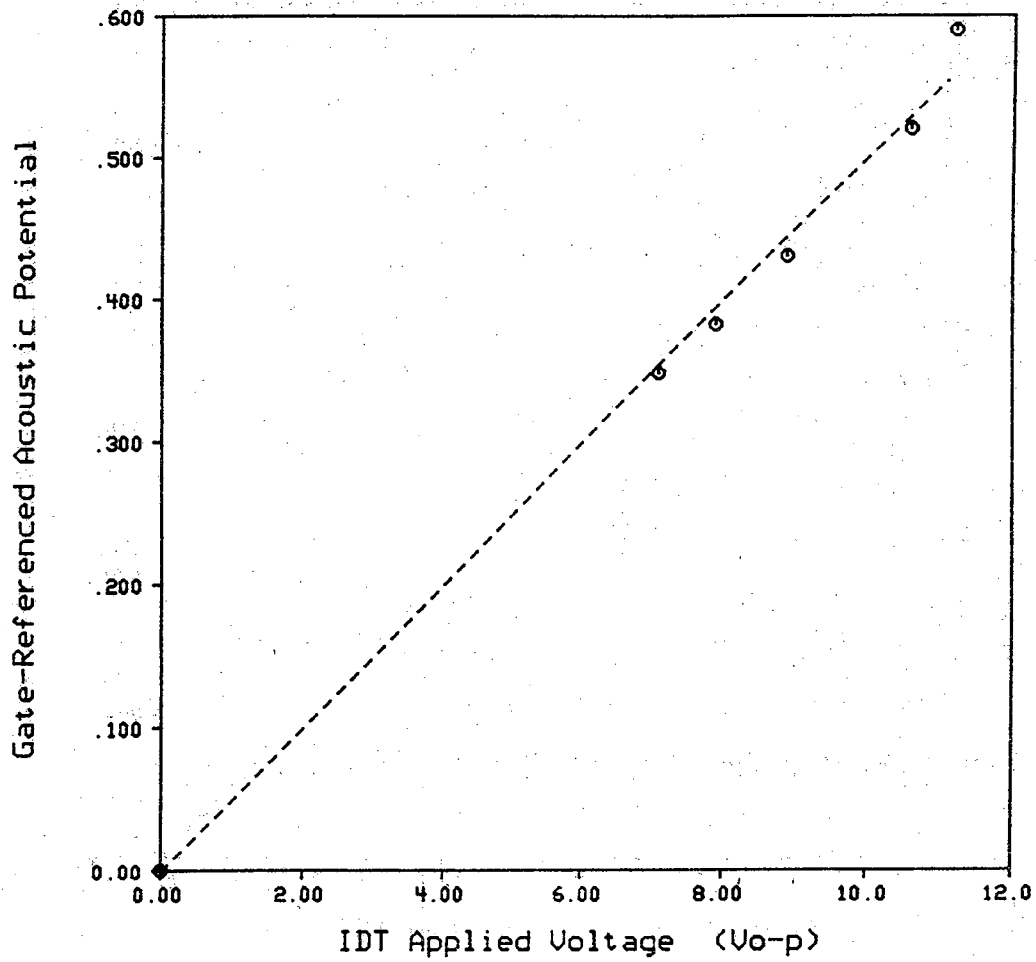
Figure 3.32

Gate-referenced acoustic wave potential versus terminal-applied transducer voltage.

erasure has been achieved by a number of means, the most common being illumination of the device using light emitting diodes (LED's) mounted inside the device package[58]. The rapid photogeneration of carriers inside the silicon is sufficient to relax the depletion widths to their equilibrium values within a few microseconds and erasure is accomplished.

An electronic erasure scheme for the induced junction storage correlator has been demonstrated by Weng[54, 59]. The electronic erasure method relies upon a narrow negative pulse applied to the gate which is sufficiently large to deep deplete the semiconductor in the entire region below the gate. This deep depletion condition creates shunting paths between what once were isolated storage regions. The erasure is completed when minority carrier holes from the regions surrounding the gate are swept into the gate region and a uniform inversion layer exists at the silicon surface. At this point in the erasure process the semiconductor is in the same condition as when setting up the induced junctions so that relaxation of the erasure pulse leaves the device immediately ready for storage of another signal.

In the construction of the implant isolated storage correlator it was initially thought that a type of electronic erasure similar to that of the induced junction device might be used. Experimentally, however, we observe that negative pulses applied to the device gate up to several tens of volts in magnitude do little to reduce the amount of stored signal. This is consistent with our predictions of Section 3.5 that the application of a negative pulse to the gate has little effect upon the stored charge. Additionally, the plot of correlation output versus gate bias shown in Fig. 3.24 indicates that the electronic erasure scheme will not work because increasing negative bias has little effect upon the correlation output. It is presently thought that the lateral

area surrounding the gate supplies an amount of holes which is insufficient to wash-out the reference signal in a short period of time. The simplest form of erasure, time relaxation, and the electronic scheme are eliminated as possibilities for reasons mentioned above so an alternative method is sought.

One of the reasons for utilizing a monolithic configuration is the ease of fabrication and rugged construction and although this implant isolated correlator has proven to be extremely sensitive to even the slightest illumination, it seems self-defeating to incorporate another discrete component (an LED) into the device package. The device erasure scheme we propose involves using a voltage controlled diode for injection of the destructive minority carriers necessary for erasure. The gate controlled diode erasure scheme is identical to the electronic erasure shown by Weng except that the signal erasing carriers are injected from an external source rather than generated internally.

A schematic diagram of the proposed erasable correlator structure is shown in Fig. 3.33. It consists of the same components and dimensions as the implant isolated correlators fabricated to date with the addition of a diode surrounded by a metal ring adjacent to the gate region on one side of the device. The diode serves as the source of the injected holes and the metal strip is biased during the correlation process to form a potential barrier between the diode and the gate region. The diode is constructed via a p^+ (Boron) ion implantation following the initial phosphorus grating implant and oxidation to avoid contamination of the boron drive furnace tube during the anneal. The aluminum contact is made directly to the p^+ implanted silicon.

The electronic erasure process with this structure can best be explained with the aid of Fig. 3.34 which shows a side view of the diode, barrier, and

guard ring diode

(a)

p^+

(b)

n^+
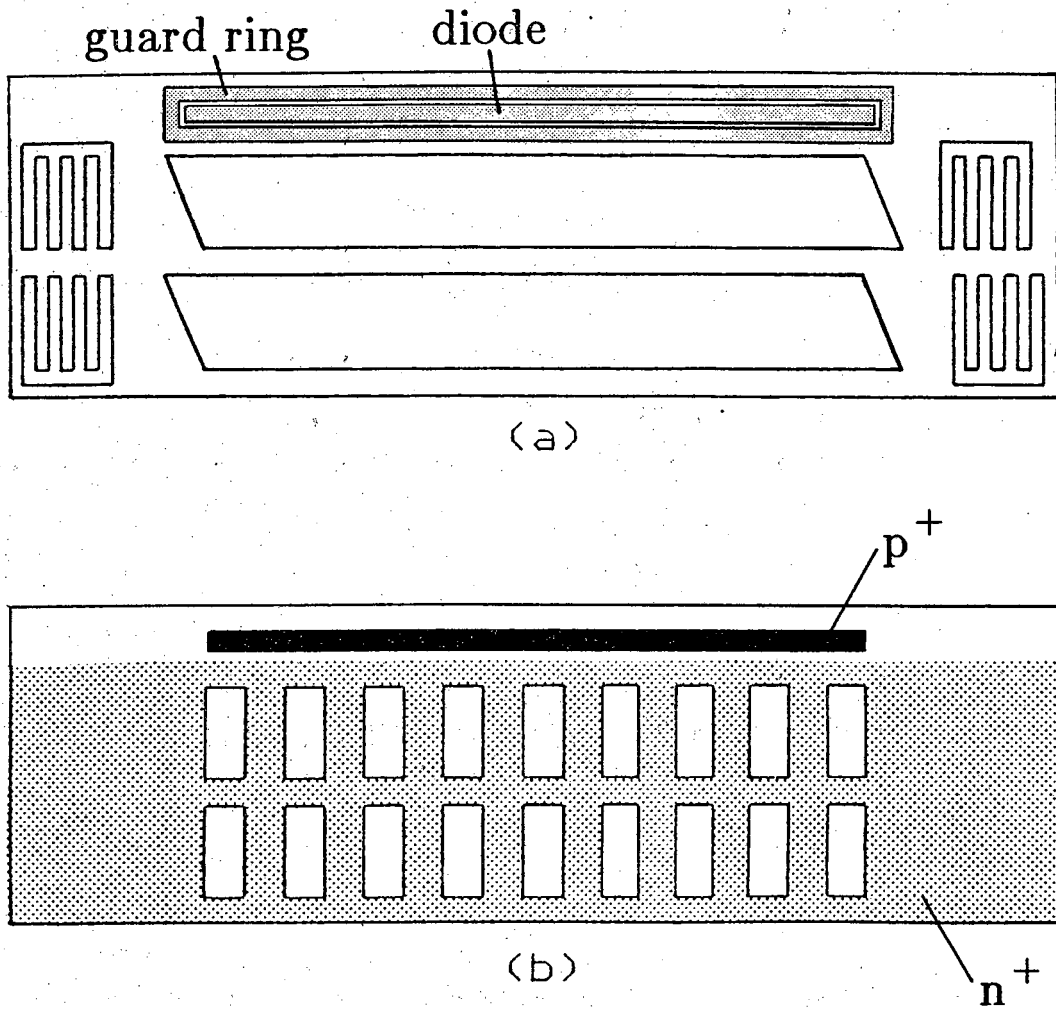
Figure 3.33

Implant-isolated storage correlator with erasure. (a) Top metallization pattern (b) ion implantation pattern at silicon surface.
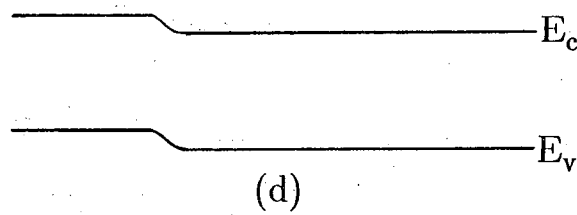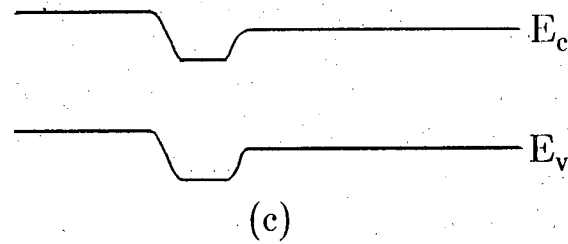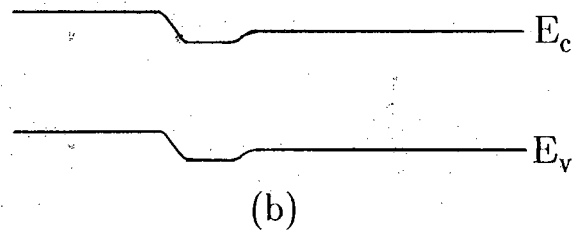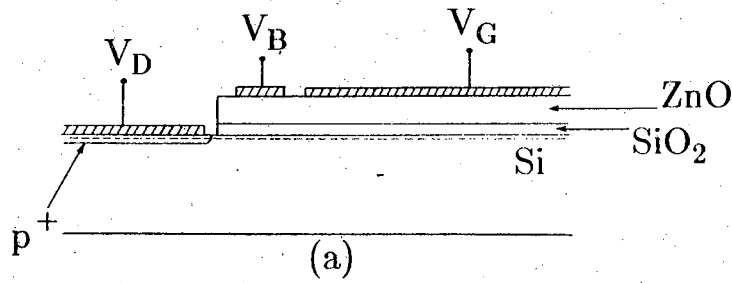
Figure 3.34

(a) Cross sectional view of diode, guard ring, and storage region. (b) Energy band diagram at equilibrium, $V_d = V_b = V_G = 0$. (c) Energy band diagram for $V_G < V_b < V_d = 0$ showing the barrier between regions. (d) Energy band diagram during erasure for $V_G = V_b < V_d$.

grating regions and energy band diagrams for various biasing schemes. The energy band diagrams are sketched with reference along the plane shown by the dashed curve of Fig. 3.34a. Figure 3.34b shows the equilibrium condition of the semiconductor with no bias voltages applied to the device. Under normal operating conditions, however, the gate bias is negative ($V_G = -8V$) and the diode voltage is zero ($V_D = 0$). To prevent premature erasure of the reference signal stored beneath the gate, the barrier voltage, V_B, will be held at -2V. This reverse biases the diode and prevents communication between holes in the diode and those in the inverted gate region by increasing the potential barrier between regions. The condition just described can be visualized in Fig. 3.34c. With this biasing in effect, the correlator should operate exactly as it did without the diode. Erasure is accomplished by removing the barrier between the gate and diode regions by pulsing the guard ring voltage to V_G (Fig. 3.34d) thereby flooding the deep depleted storage regions with minority carrier holes. This rapid diffusion of holes should cause complete erasure of the stored signal within a few microseconds.

This erasure mechanism involves a few extra fabrication steps but no more electronics than any other erasure technique. Furthermore, erasure will be accomplished without complicating the device package with LED's but in the same time period.

CHAPTER 4

SAW RESONATORS

In marked contrast to the monolithic SAW memory correlator which utilizes the nonlinear electrical properties of the silicon for its operation, the SAW resonator relies upon the scattering properties of surface acoustic waves from surface discontinuities for proper operation. As a matter of fact, electrical interaction of propagating acoustic waves with metal features or semiconductor charge carriers gives rise to undesirable acoustoelectric losses which can severely limit device performance. In the SAW resonator, one relies upon efficient reflectors to confine acoustic wave energy to a resonant cavity. The reflections can be both mechanical and electrical in nature but reflections which are dependent upon electrical loading effects are less efficient than purely mechanical reflections.

Long before the introduction of SAW resonators, acoustic bulk wave resonators were demonstrated to be high Q, low loss elements. Because very thin piezoelectric membranes are needed for high frequency bulk wave resonators, however, their practicality extends into the frequency range only as high as thin film machining will allow. Kline and Lakin[70] have fabricated bulk wave resonators on GaAs with operating frequencies higher than 1 GHz. In their devices, sputtered AlN films are effectively removed from the GaAs substrate by chemically etching pouches in the underlying substrate. Using

this technique, the ability to achieve resonance at a particular frequency depends upon ones ability to control the sputtered film thickness.

Alternatively, the utilization of surface acoustic wave structures has resulted in resonator operation as high as 2600 MHz[71] with excellent frequency control which is determined by the accuracy of the pattern definition on the substrate surface. As such, surface acoustic wave resonators have proven to be effective high frequency, narrowband filters[72,73,74,75,76] and are used as frequency control elements in oscillators in the UHF-VHF range[77,78]. These devices have also been used as pressure sensors[79], accelerometers[80] and gas detectors[81].

Fabricated on single crystal piezoelectrics such as quartz and lithium niobate[82,6,83,8,84,85] as well as in the $ZnO/SiO_2/Si$ layered medium configuration[7], SAW resonators are rugged high Q devices[86,10,9] capable of operating at frequencies above 1 GHz[87,88]. Single crystal substrate SAW resonators fabricated on $LiNbO_3$ are attractive because of the possibility for low insertion loss by virtue of its high electromechanical coupling coefficient while the advantages offered by resonators on quartz are temperature stability and low propagation loss.

Recently, the single crystal SAW resonators have been challenged by devices fabricated in the $ZnO/SiO_2/Si$ layered configuration[7]. Martin et al.[22], have demonstrated high Q resonators which can be made temperature stable by exploiting the compensating nature of the temperature coefficient of phase delay from a thick SiO_2 layer. Additionally, by varying the dimensions of the SiO_2 film, one can make these devices temperature stable over a temperature range selected by the designer. One further advantage of the layered medium resonator, not possible with single crystal resonators fabricated to date, is the

possibility of incorporation of the resonator as an on-chip element which can be fabricated alongside other components in monolithic circuits. Moreover, in addition to their rugged construction, ZnO-on-silicon SAW resonators have displayed potentially favorable aging characteristics[89].

In this chapter we discuss further contributions to the study of on-silicon SAW resonators in an effort to increase their attractiveness for high frequency applications. We present a brief discussion of the operation of a typical SAW resonator followed by experimental results dealing with new on-silicon resonator configurations.

4.1 Introduction

The operation of any SAW resonator involves the confinement of the acoustic wave inside a resonant cavity. The resonant cavity is formed by placing SAW reflectors some distance L apart such that at a particular frequency, a standing wave pattern will exist inside the cavity. The surface acoustic wave which is to be confined is introduced by way of interdigital transducers and the resonant condition standing wave is detected using either the same (one-port), or another (two-port), IDT. The operation of IDT's for wave excitation was outlined in Ch. 2 and we now turn our attention to the reflector array properties.

In a SAW resonator, ideally one would utilize abrupt discontinuities (either parallel cleaved substrate edges or two very deep grooves) to achieve total reflection of the surface acoustic wave. Such a structure, however, would lead to severe conversion to bulk modes and hence a power loss which would greatly decrease the resonator performance. Instead of large reflections from a single reflector, reflection consisting of contributions from a series of distributed

reflectors has been successfully employed.

The fundamental principle behind the operation of a SAW resonator is that near total reflection of a surface acoustic wave can be achieved by using an array of distributed reflectors consisting of a large number of periodic discontinuities placed normal to the propagation path[90,73]. It is because the SAW resonator utilizes waves propagating on the surface of a substrate, that enables one to employ surface perturbations for the reflection process. Furthermore, if the periodicity of the perturbing features is one-half wavelength, only a small fraction of the incoming wave energy need be reflected by each of a large number of reflectors to form an efficient Bragg reflector capable of large coherent reflection over a narrow bandwidth. A resonant cavity is formed when two such reflectors of the same periodicity are placed opposite one another thereby confining SAW energy between the reflectors. Resonance occurs whenever the surface acoustic wave lies within the bandwidth of the reflectors and the total round trip phase shift of the confined wave is a multiple of 2π. When the resonant condition is satisfied one has a standing acoustic wave in the cavity. Furthermore, the use of a sufficient number of distributed reflectors per grating has been shown to make the bulk mode conversion loss in SAW resonators negligible compared to other energy loss mechanisms present in the system[91,92].

A conventional SAW resonator consists of one (single-port) or two (two-port) interdigital transducers placed between symmetric reflector arrays on a piezoelectric surface. The schematic of a typical two-port $ZnO/SiO_2/Si$ SAW resonator with etched groove reflector arrays is shown in Fig. 4.1. The etched groove reflector arrays actually consist of ridges rather than grooves. From Figs. 2.3 and 2.5 one can determine that the wave velocity in the ridges (where

RIDGE REFLECTORS

ZnO
AL
SiO$_2$

(111)-cut
<2$\bar{1}\bar{1}$> prop.
Si
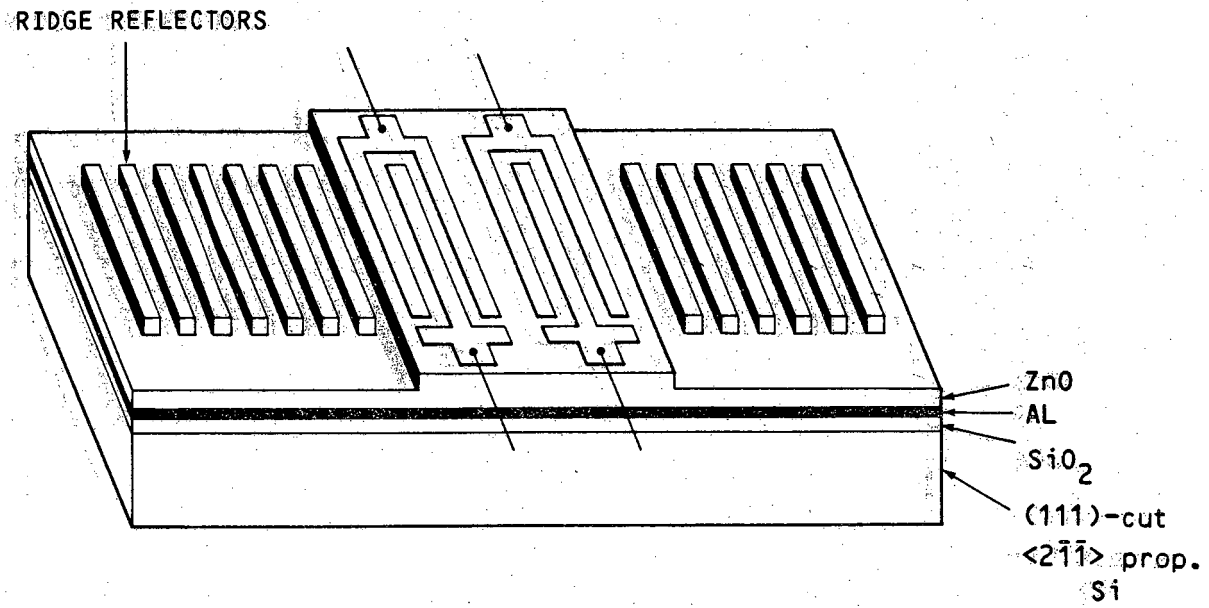
Figure 4.1

Schematic for a two-port SAW resonator employing ion milled groove reflectors.

the ZnO is thicker) is slower than in the region surrounding the reflector array. That is, the effective SAW velocity in the grating region is slower than in the surrounding region. Thus, a waveguiding effect occurs which tends to confine the SAW laterally within the grating region. Placement of transducers between reflector arrays allows one to couple energy into and out of the cavity. The two-port internally coupled configuration, as well as an externally coupled structure, (transducers outside the resonant cavity) will be discussed later.

4.2 Reflector Array Properties

In SAW resonators fabricated to date, it has been demonstrated that the surface reflector arrays can consist of metal strips either shorted or isolated[22] as well as grooves etched either chemically or by ion milling[7]. Although metallized reflector resonators are easiest to fabricate, and ZnO is etched readily with a dilute nitric acid solution, the most efficient reflectors have proven to be gratings of ion beam etched grooves in the substrate surface. As such, the majority of our work deals with devices fabricated in the ion beam etched groove configuration. Since the operation of the SAW resonator is critically dependent upon the confinement of energy, we will examine the grooved reflector array in some detail as a means of establishing an efficient resonant cavity.

Traditionally, the reflective grating has been modeled as a periodically mismatched transmission line as shown in Fig. 4.2; this report is no exception. The transmission line model, first applied to the SAW reflector array by Sittig and Coquin[93], has proven very accurate for long reflector arrays utilizing small perturbations. In our device configurations, the ridges are modeled as having a characteristic impedance of Z_2 while the impedance of the grooves is given by

One Reflector Period

$$[T_n] = \begin{bmatrix} A_n & B_n \\ C_n & D_n \end{bmatrix}$$
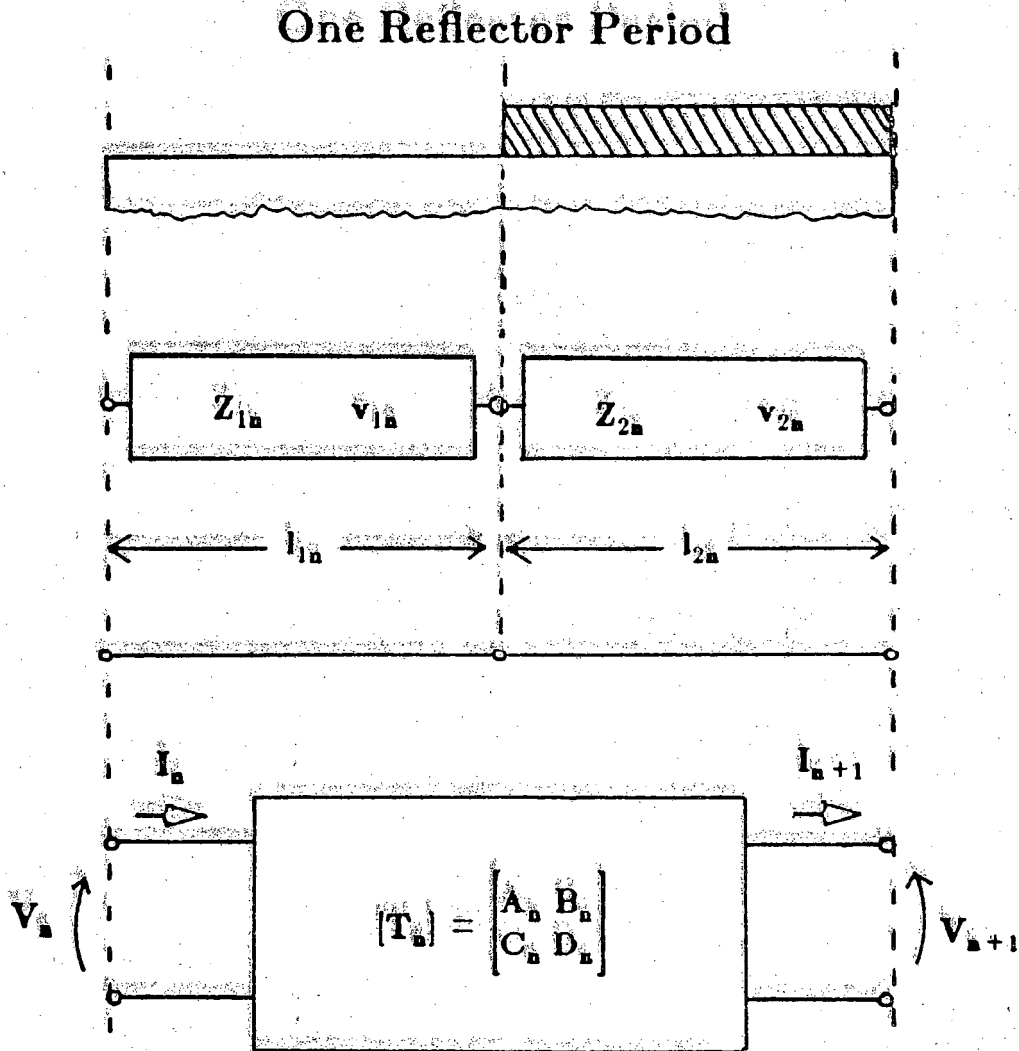
Figure 4.2

Matrix representation of one reflector period.

Z_1. By assuming a particular impedance mismatch between regions 1 and 2, one can determine the reflection (and transmission) magnitude and phase for a reflector array of N periodic sections. Figure 4.3 shows a plot of reflection magnitude versus number of reflectors for different values of impedance mismatch per section. One can see that as the number of reflectors increases (for a fixed impedance mismatch), the reflection magnitude of the array becomes nearly total. Figures 4.4 and 4.5 show plots of calculated reflection magnitude and phase versus frequency, assuming a lossless reflector. From Fig. 4.4 one can see that as the number of reflectors increases, not only does the reflection magnitude increase, but the reflector bandwidth decreases. Furthermore, as shown in Fig. 4.5, the reflection phase variation is nearly linear at the reflector center frequency. This enables one to model the grating as a single reflector located a distance L_p away from the grating edge with reflection coefficient equal to that of the entire array. The distance L_p is given by[90]

$$L_p = \frac{f_o}{4\pi} \left| \frac{d\phi}{df} \right|_{f = f_o},$$

(4.1)

where f_o is the reflector center frequency and ϕ is the reflection phase. The reflection phase is dependent upon the number of reflectors per array as well as the impedance mismatch per periodic section. A plot of L_p versus impedance mismatch, ϵ, is shown in Fig. 4.6 for three different values of N, the number of reflectors per array. In general, for a constant $N\epsilon$, L_p will be greatest for large N and small ϵ. Additionally, if the wave excited by the IDT is within the reflector bandwidth, and the separation between reflectors, L_o, is an integer number of half-wavelengths[7], a resonant cavity will be formed with an effective cavity length L_{eff} given by
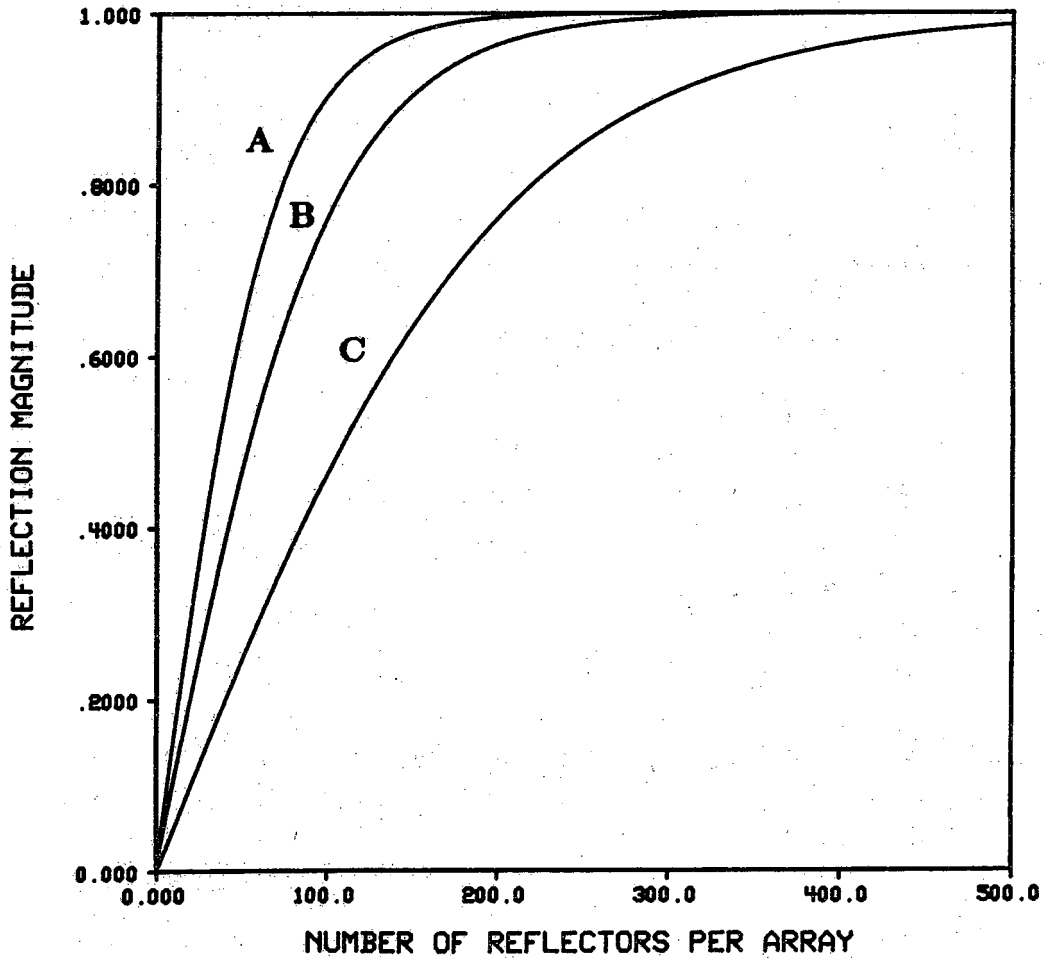
Figure 4.3

Reflection magnitude for a reflector array with impedance mismatch per section of 1% for (A) 400 (B) 200 and (C) 100 reflectors per array.
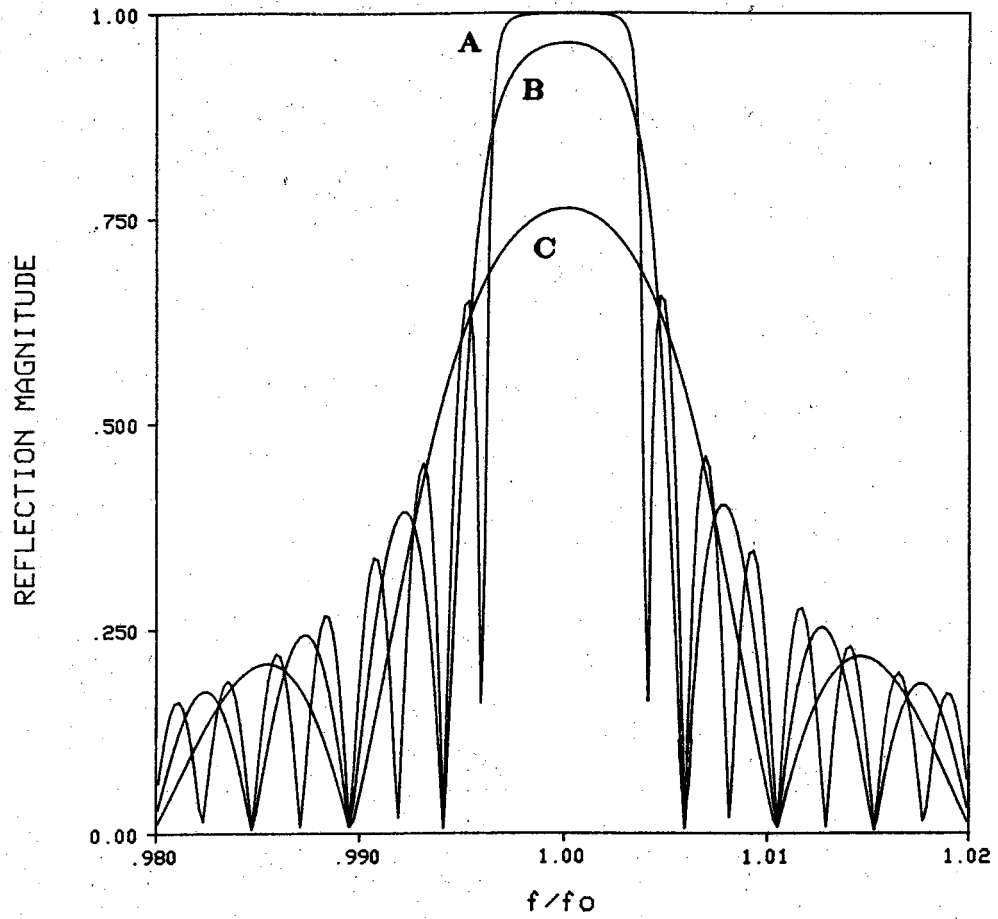
Figure 4.4

Reflection magnitude for a reflector array with impedance mismatch per section of 1% for (A) 400 (B) 200 and (C) 100 reflectors per array.
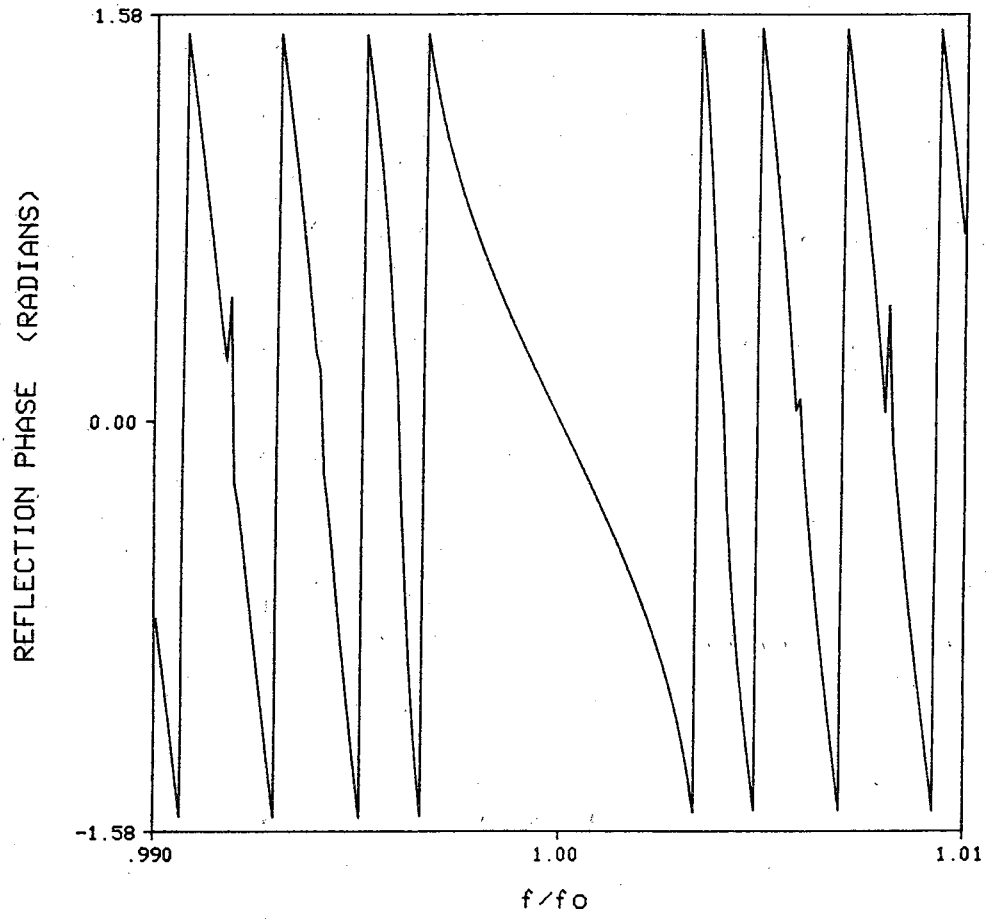
Figure 4.5

Reflection phase for an array of 400 ion milled grooves with a reflectivity per groove of 1 %.
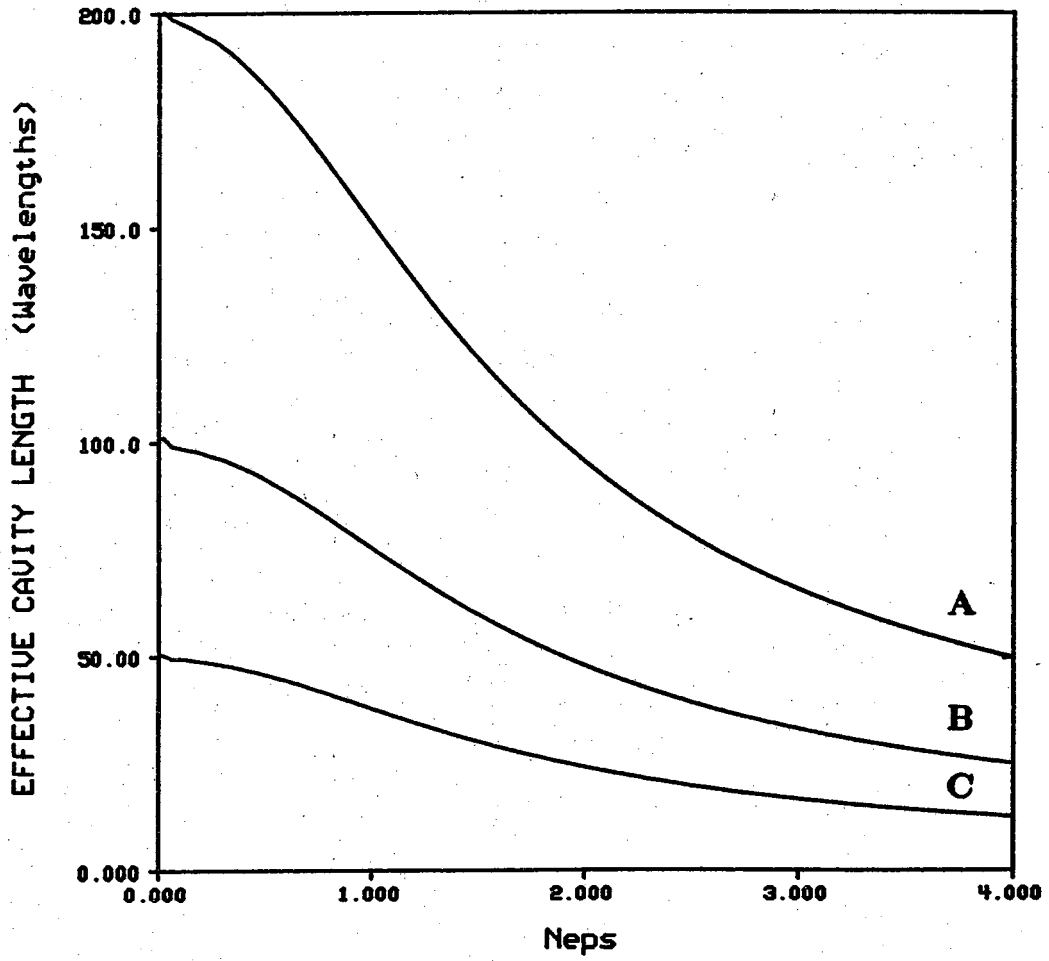
Figure 4.6

Effective cavity length for arrays consisting of (A) 800 (B) 400 (C) 200 reflectors.

$$L_{eff} = 2L_p + L_o \quad . \tag{4.2}$$

4.3 Resonator Q

The effectiveness of a resonant cavity for confinement of energy can be determined by means of a figure of merit known as the device Q, or quality factor. The Q of a resonant cavity is a measure of the ability of the cavity to store energy and is given by

$$Q = \frac{2\pi U}{P_L} \quad , \tag{4.3}$$

where U is the peak energy stored in the cavity, and P_L is the power lost per cycle. An alternative expression for the device Q assuming no losses except for radiation out the ends of the reflector arrays caused by insufficient reflection, is given by

$$Q = \frac{2\pi L_{eff}}{\lambda(1 - |R|^2)} \quad , \tag{4.4}$$

where λ is the wavelength at the synchronous frequency and R is the magnitude of the reflection coefficient. Clearly, to obtain a high Q resonator, one desires to increase the effective cavity length, and at the same time, maximize R. At this point the problem appears to be a simple one as both conditions for enhanced Q can be met by increasing the number of reflectors per grating and decreasing the reflectivity per groove (shallower grooves). The actual solution, however, is not so simple because one must take into account practical considerations by dealing with the various loss mechanisms in the resonator.

4.3.1 Loss Mechanisms

Any losses which increase the power lost per cycle, increase P_L, thereby lowering the device Q (Eq. 4.3). The main sources of loss are due to propagation loss (viscous damping and air loading), diffraction loss and other leakage out the sides of the device, losses due to conversion of the Rayleigh wave to bulk waves, and radiation loss from the ends of the reflecting arrays. The overall Q one can attain is limited by each of these mechanisms. That is, as one takes into account the Q's associated with various loss mechanisms, one can determine the overall device Q as follows

$$\frac{1}{Q} = \Sigma_i \frac{1}{Q_i} = \frac{1}{Q_r} + \frac{1}{Q_d} + \frac{1}{Q_b} + \frac{1}{Q_p} + \ldots, \qquad (4.5)$$

where the Q's on the right side of Eq. 4.5 are the radiation, diffraction, bulk wave loss, and propagation loss Q's respectively plus any other loss mechanism Q's. We assume the four loss mechanisms mentioned here to be the dominant Q-limiting factors associated with our resonator structures. Several efforts have been made at reducing each of the losses[94]; two which can be minimized by changing the grating dimensions are diffraction loss and bulk wave conversion loss.

Diffraction loss is caused by incomplete confinement of the wave energy at the edges of a reflector array. Li, et. al[95,9] have shown that diffraction loss Q varies as the square of the beamwidth and that a sufficiently wide grating aperture ($\sim 50\ \lambda$) will make diffraction losses negligible with respect to the other losses. Losses associated with generation of bulk waves from grooved reflector arrays has been examined[96] and it has been shown that bulk wave generation can be made negligible by utilizing a large number of reflectors with very small perturbations (shallow grooves)[91]. A thorough analysis has yet to be performed

for bulk mode conversion in the layered ZnO/SiO$_2$/Si configuration and as will be seen later, this will be a major concern in the design of low loss, high Q resonators.

The radiation Q for a SAW resonator is dependent upon the reflection magnitude of each reflector array. As discussed earlier, the reflection magnitude is a function of the number of reflectors per array as well as the impedance mismatch per periodic section (groove depth). Also entering into the computation of the reflection magnitude, however, is the propagation loss per unit length associated with a given structure. The propagation loss will be shown to have a profound affect upon the device Q.

To maximize device Q one requires a large effective cavity length and near total reflection from each of the reflector arrays. One assumes that this can be achieved by using a large number of very shallow grooves. As the effective cavity length L_{eff} is increased, so is the effective propagation path of the confined SAW, so in the expression for radiation Q, the increased L_{eff} from shallower grooves may be more than offset by the decrease in R. That is, depending upon the propagation loss in a particular resonator configuration, increasing L_{eff} while holding Nϵ constant may or may not increase the device Q.

The rather complex goal of the SAW resonator designer is to maximize the device Q while keeping the device dimensions to a reasonable size. In the ZnO/SiO$_2$/Si layered medium configuration, the main source of loss (and hence the limiting Q factor) is propagation loss due to the viscous nature of the ZnO layer. That is, it is assumed that the device is limited by Q_p and that diffraction loss, bulk wave loss, and radiation loss are comparatively small. These assumptions will be verified in following sections.

4.3.2 Propagation Loss

It should be noted that the SAW resonator has long been a valuable diagnostic tool in the determination of wave attenuation because the Q provides a very sensitive measure of propagation loss within a structure[95,9]. By minimizing all other loss mechanisms (by methods described above), one can assume all remaining loss to be due to propagation loss thereby allowing an attenuation factor, α, to be determined from the well known relation

$$Q = \frac{\pi}{\lambda \alpha} \quad , \quad (4.6)$$

where λ is the wavelength of the SAW at the synchronous frequency and α is the propagation loss per unit length. The value of α computed from Eq. 4.6 is an upper bound on propagation loss.

Propagation loss in the ZnO layered medium is much greater than for Rayleigh waves propagating in silicon or on bulk ZnO. Hickernell[97] reports losses for sputtered ZnO films typically eight to 30 times greater than predictions made based on bulk ZnO samples. The higher propagation loss is believed to be caused by physical discontinuities at the grain boundaries of the polycrystalline ZnO films as well as surface roughness which is an unavoidable result of any sputtering process. It has been shown that as surface roughness and defect density increases, so does propagation loss[97]. An added complication associated with the propagation loss in the thin film ZnO layer is that the propagation loss increases with the square of the frequency[97]; a potential limiting factor in the operation of high frequency SAW resonators.

To observe the effect of propagation loss upon the device Q we have simulated the response of a SAW resonator using the cascaded transmission line model while incorporating propagation loss. We have assumed a

propagation loss of 0.45 dB/cm and have let the separation between arrays (L_o) be 30λ. Q is then calculated from Eq. 4.4 where the computed reflection coefficient includes the effect of propagation loss. Figure 4.7 is a plot of resonator Q versus $N\epsilon$, the number of reflectors times the impedance mismatch per reflector, where the number of reflectors per grating was held constant and ϵ was varied. For this particular array separation and propagation loss, the maximum Q is achieved for small impedance discontinuities and actually decreases slightly as the impedance mismatch per periodic section (groove depth) increases. That is, as groove depth increases, the reflection magnitude increases but the effective cavity length decreases and the overall Q decreases. The degradation of Q is attributed to the fact that the slow increase in the reflection coefficient from deeper grooves is not sufficient to counteract the decrease in effective cavity length because the propagation loss in the cavity region between reflectors dominates the device Q.

Understanding the relationship between these effects is especially important in the design of high frequency resonators where it is thought the propagation loss will increase dramatically because of the f^2 loss mechanism. One should also keep in mind the fact that once propagation loss becomes large, one no longer gains a great deal in the way of maximum Q by increasing the number of reflectors in the gratings. Rather, by sacrificing a small percentage of the maximum Q one can reduce the size of the device by great amounts; a very important consideration if these devices are to be incorporated into monolithic circuits. Note in Fig. 4.7 that a device represented by the data of curve A corresponds to a device of approximately one-half the area of the device of curve B which is half the area of the device represented by curve C. Thus, one has significant savings in valuable substrate real estate without
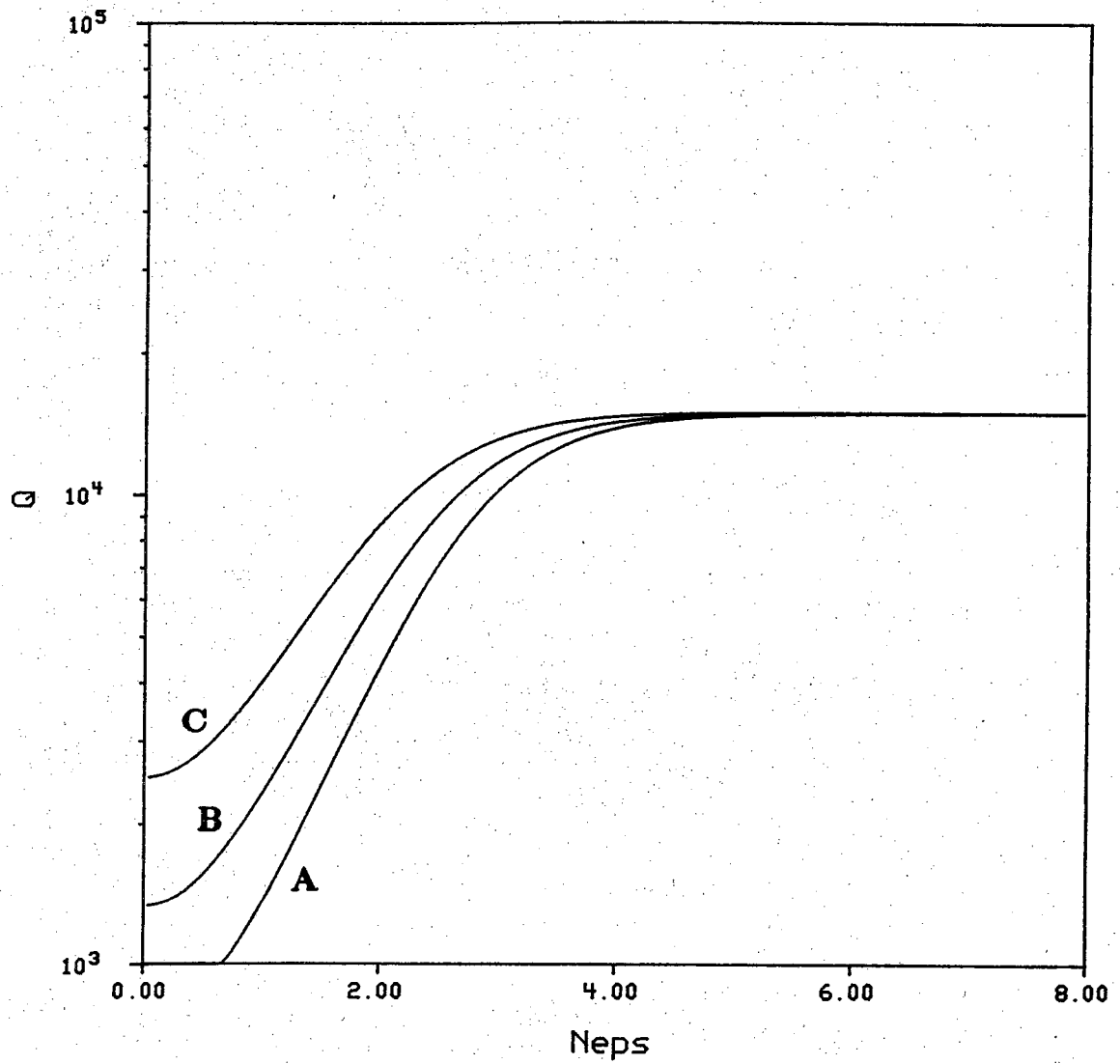
Figure 4.7

Q-value versus Nϵ for (a) 200 (b) 400 and (c) 800 reflectors per grating.

sacrificing an appreciable amount of the resonator quality factor. From the curves of Fig. 4.7 one can see that it is unreasonable to expect higher Q values from different combinations of groove depth and grating length after a point because the device performance is limited by propagation loss.

4.4 Limited ZnO SAW Resonators

To improve the ZnO film quality and to reduce the propagation loss associated with the $ZnO/SiO_2/Si$ composite structure, various annealing techniques have been employed. Results of a laser annealing experiment have been reported by Martin et. al[28]. whereby the grating regions of a SAW resonator were laser annealed in an attempt to reduce the number of defects located at the ZnO/SiO_2 interface. These interface defects are highly concentrated in sputtered films and are thought to contribute significantly to surface wave attenuation. The results of the CO_2 laser experiment by Martin are shown in Fig. 4.8. Clearly the slight increase in device Q is not enough to warrant significant interest in the laser annealing technique as a method of reducing propagation loss. It was not noted in this experiment whether there was a change in the optical propagation loss which is what had been of interest to those laser annealing ZnO up to this point[98].

In addition to laser annealing, thermal annealing in furnaces has been attempted[99] but with no improvements noted in either optical or acoustic propagation loss.
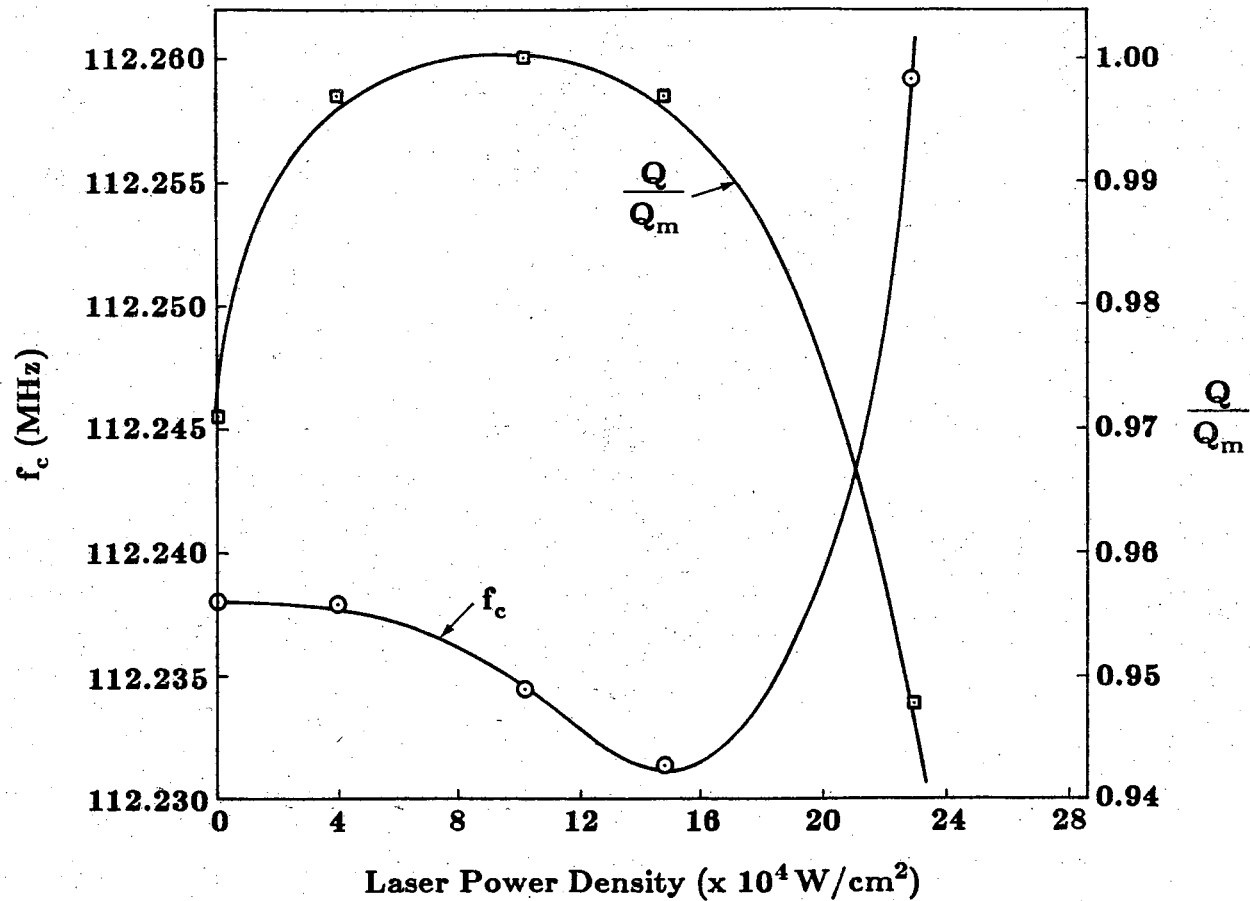
Figure 4.8

Center frequency and Q-value resulting from the laser annealing of an externally coupled $ZnO/SiO_2/Si$ SAW resonator at successively higher power densities.

4.4.1 Device Configuration

Rather than resign ourselves to the fact that nothing can be done to reduce the surface wave attenuation caused by the ZnO film, we have attempted to circumvent the problem through the use of alternate configurations which are variations of the devices fabricated to date. The function of the piezoelectric ZnO layer is that it provides a means by which electrical energy can be transduced into acoustic energy and vice-versa thereby allowing a means for coupling into and out of the resonant cavity. Efficient reflection of surface waves can be achieved without the ZnO film. By reflecting the waves using grooves etched into the SiO_2 layer (ZnO removed), the lossy ZnO layer can be limited to the transducer regions. To examine the effect of elimination of the ZnO on device Q, resonators similar to those depicted in Fig. 4.9 have been fabricated. One will note the transducer regions are the only places where ZnO is to be found. These ZnO regions can be defined either by chemically etching the ZnO layer or by using a shield during the sputtering process. An advantage of the latter technique is that sputtering damage can be restricted to a minimum area of the wafer.

A feature associated with the growth of thin films is the possibility of some nonuniformity in thickness over a sample. In fabricating resonators using etched grooves in the ZnO layer, it is important to maintain good control of the film thickness in the grating region; this is especially important due to the velocity gradient associated with a change in film thickness of the dispersive ZnO layer. The velocity gradient can both degrade the reflection magnitude and increase the bandwidth of a reflective array. The nonuniformity problem is alleviated in devices constructed using grooves in silicon or grooves in SiO_2 where the dispersion is considered negligible.
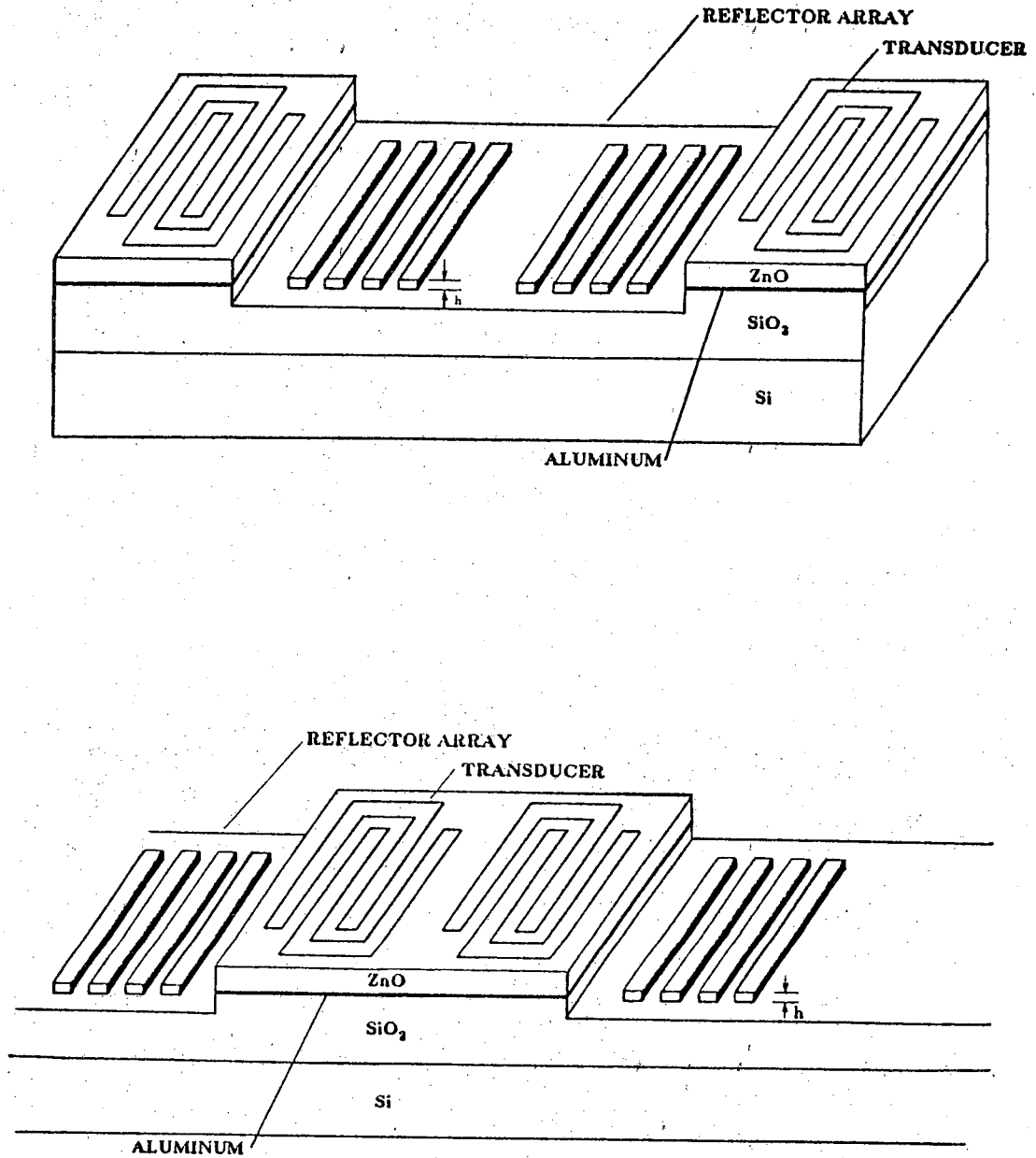
Figure 4.9

Limited ZnO resonator configurations (a) externally coupled and (b) internally coupled.

A series of experiments involving the measurement of the transmission through reflector arrays of 400 ion-milled grooves were performed to determine the reflectivity per groove for various values of groove depth. A plot of reflectivity per periodic section versus normalized groove depth, hk, is shown in Figure 4.10. Experimental points together with a theoretical curve for grooves both in silicon and SiO_2 indicate that experimental results appear to be in close agreement with theory[101, 102]. Also included in the figure is a line showing experimental reflectivity data for grooves etched into the surface of a 0.7 μm ZnO film on 3.05 μm SiO_2 as previously reported[7]. All measurements and predictions are for (111) cut [2$\overline{1}\overline{1}$] propagation direction silicon substrates. Clearly, by elimination of the ZnO layer in the grating region, one must use deeper grooves, more reflectors, or a combination of these two to obtain the same amount of reflection from a grating etched into silicon or SiO_2. An increase in the groove depth will eventually decrease Q due to scattering into bulk modes, whereas an increase in the number of reflectors per grating will increase the effective cavity length and hence, raise the Q at the expense of an increased device size.

With this reflectivity information as a starting point, resonators similar to those shown in Fig. 4.9a were constructed with 400 grooves per reflector array and a periodicity of 20 μm. The separation between reflector arrays was 30 wavelengths. The motivation behind using an externally coupled resonator was to leave the transducers outside of the resonant cavity to try to maximize the device Q by not loading the cavity with the output port. The resonators were constructed with grooves etched into a 3.05 μm SiO_2 layer and also grooves in unoxidized silicon. The Q's for these devices were 25,900 and 31,400 respectively; a significant improvement over the previous high of 14,400 for an
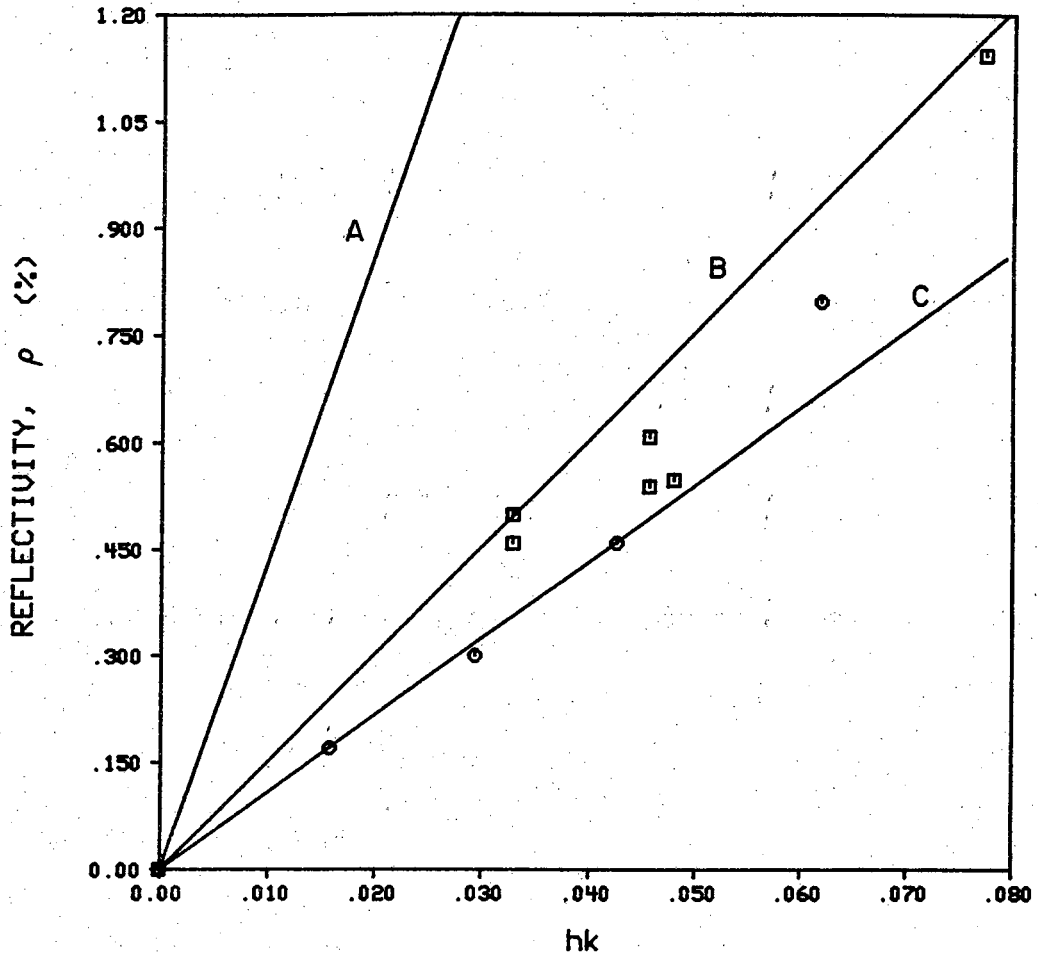
Figure 4.10

Reflectivity per groove vs. normalized groove depth for the following configurations:

(A) Grooves in 0.7 μm ZnO on 3.05 μm SiO$_2$,

(B) Grooves in 3.05 μm SiO$_2$

(C) Grooves in unoxidized silicon. All substrates are (111)-cut, <211> propagating silicon.

externally coupled SAW resonator with grooves etched into the ZnO layer. Experimental results of Q versus impedance mismatch per periodic section for the just described configurations are shown in Figs. 4.11 and 4.12. The experimental data obtained in these measurements was used in the resonator simulation program to determine values for propagation loss for each configuration. In the SiO_2 reflector configuration a value of $\alpha = 0.24$ dB/cm best fits the data and similarly $\alpha = 0.19$ dB/cm for the unoxidized array in silicon. The computed values of resonator Q using these factors are represented by the solid curves of Figs. 4.11 and 4.12. These factors are far below the value of $\alpha = 0.45$ dB/cm computed from the best resonator with grooves in ZnO. Using these values, an extension of the resonator model leads us to believe Q's of at least 27,600 and 36,100 are attainable at 115 MHz for the silicon dioxide and silicon groove arrays respectively. This information enables us to examine not only the degree of surface wave attenuation which can be attributed to the ZnO layer, but we can also begin to draw conclusions about the effect of the SiO_2 layer on propagation loss.

The two-port transmission magnitude response of an externally coupled resonator is shown in Fig. 4.13. The sharp resonant peak centered within the reflector array stopband is characteristic of these devices. The peak-to-background level is approximately 25 dB but only in a narrow frequency band near resonance and the insertion loss at resonance is nearly 50 dB. Externally coupled resonator filters are useful for narrowband applications where gain is not an important factor.

The two-port internally coupled resonator, however, has a large peak-to-background level over a wide frequency range, and has exhibited insertion losses in the layered medium configuration of less than 5 dB. A two-port
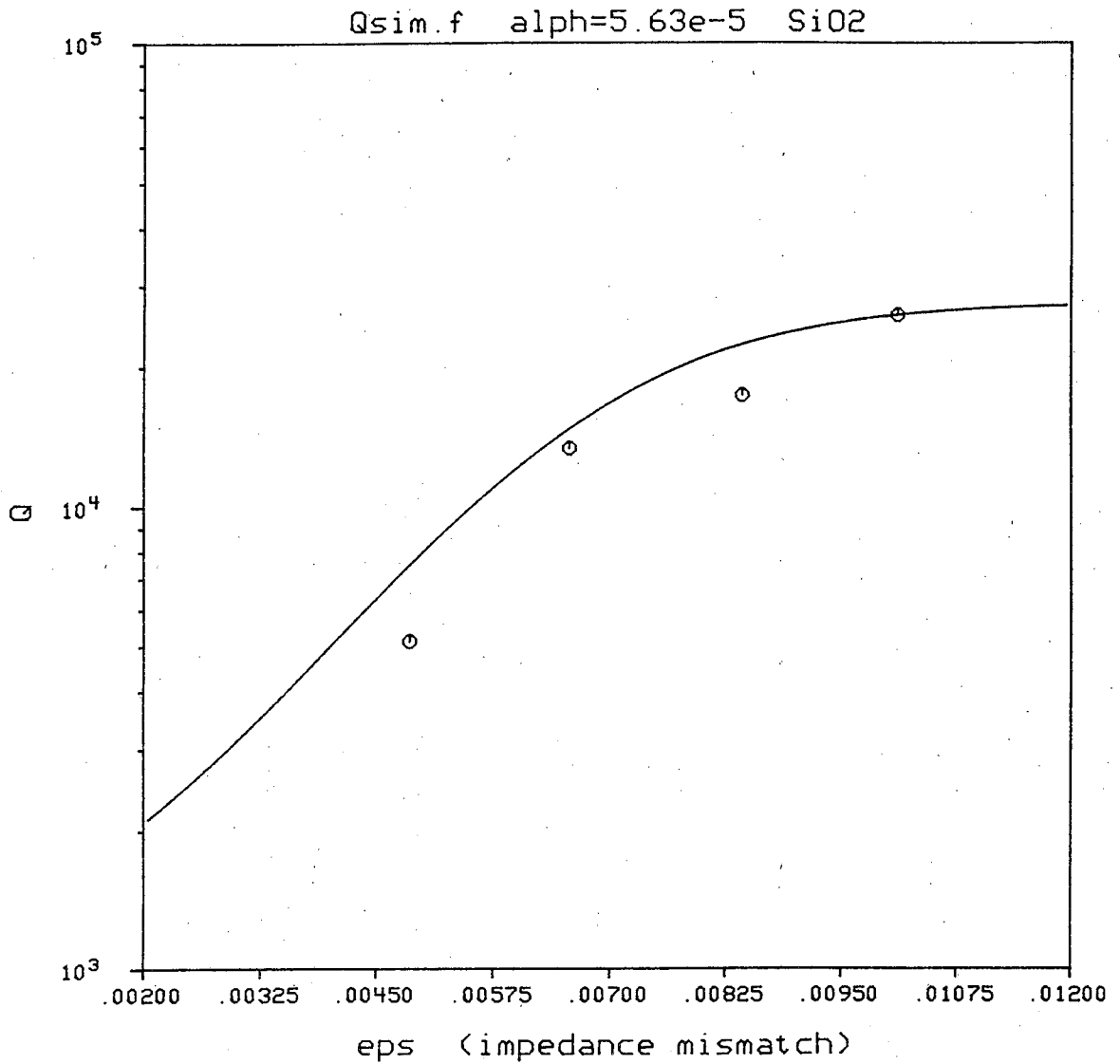
Figure 4.11

Resonator Q versus reflectivity per periodic section for limited ZnO externally coupled resonators with grooves etched into SiO_2.

Qsim.f alph=4.25e-5 Silicon
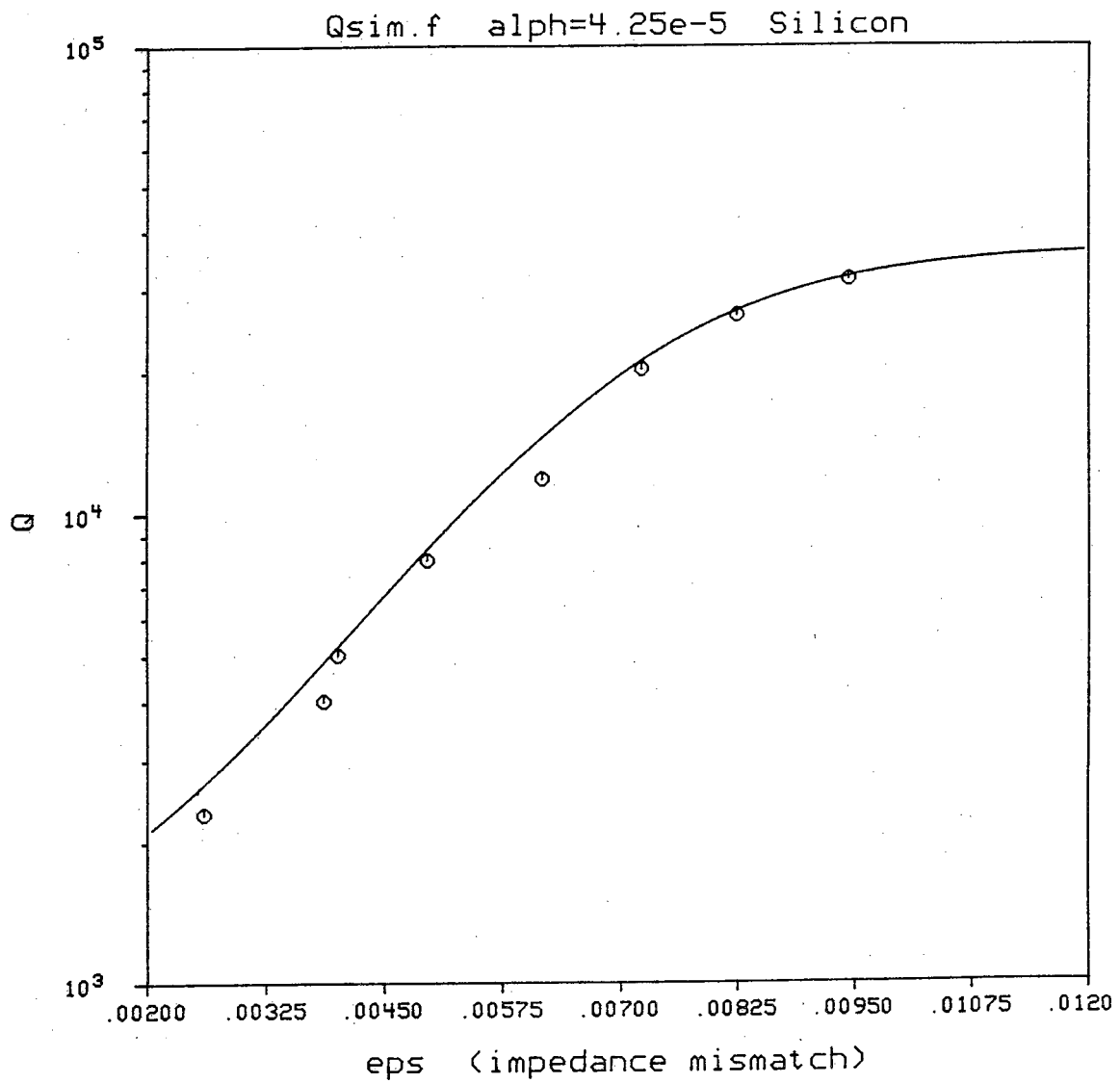
Figure 4.12

Resonator Q versus reflectivity per periodic section for limited ZnO externally coupled resonators with grooves etched into unoxidized silicon.
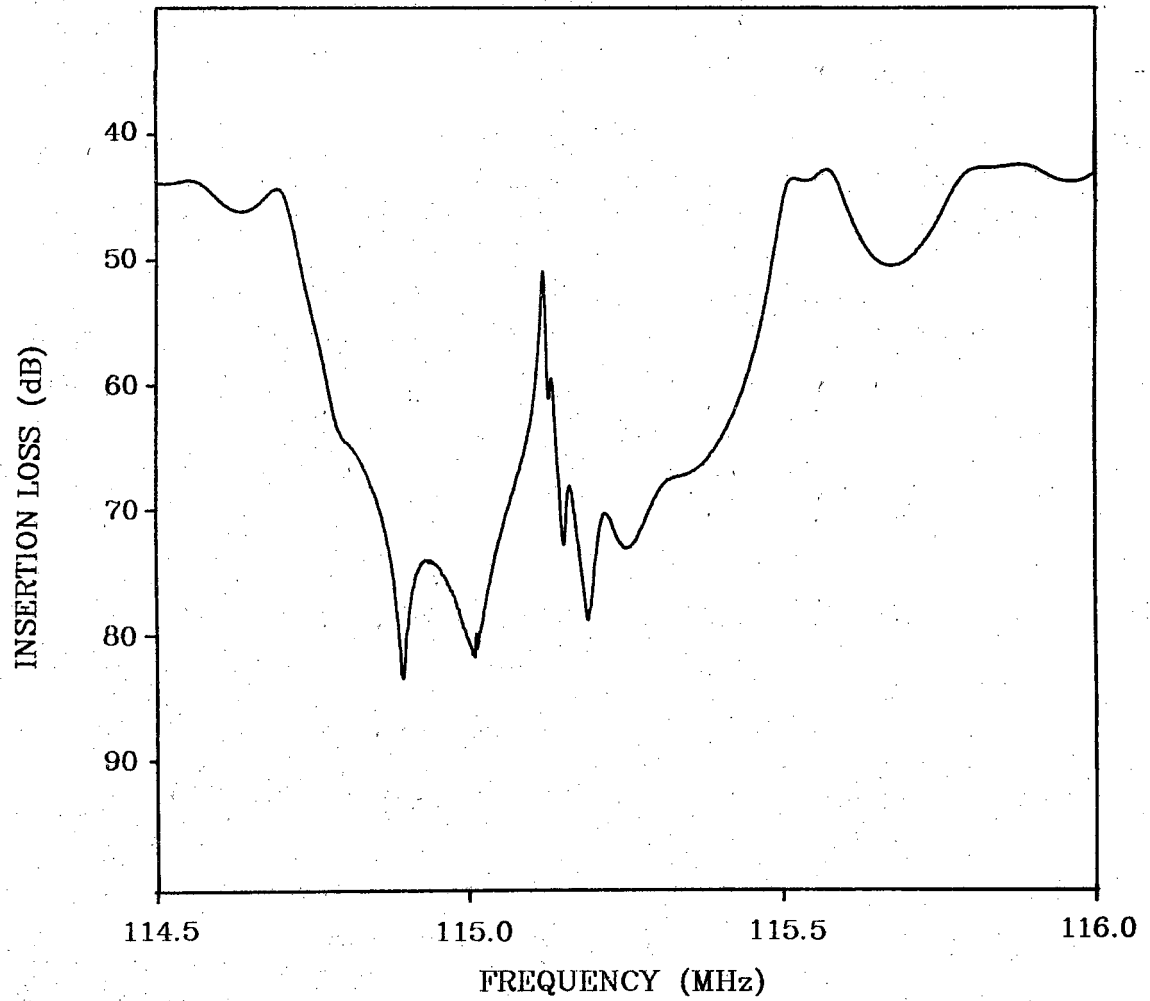
Figure 4.13

Two-port frequency response for an externally coupled ZnO/SiO$_2$/Si SAW resonator.

transmission response plot for a typical internally coupled resonator is shown in Fig. 4.14. For obvious reasons, the internally coupled two-port resonator configuration is of much greater interest for practical signal processing applications and as such, we have applied the above-mentioned changes to the internally coupled structure.

SAW resonators in the configuration shown in Fig. 4.9b have been fabricated for both grooves in SiO_2 and grooves in unoxidized silicon. In both structures the ZnO was chemically etched away from the grating region to form an abrupt step at the edges of the transducer regions; no tapering of the ZnO was attempted. Each reflector array consisted of 400 ion mill grooved sections. Experimental results of Q versus reflectivity per section for limited ZnO internally coupled resonators are shown in Figs. 4.15 and 4.16. In both cases of grooves in SiO_2 and grooves in unoxidized silicon, the maximum Q achieved was below 5000. One would first conclude that perhaps the deeper grooves needed because the lower reflectivity per groove (Fig. 4.10) of both trial configurations caused a severe bulk mode conversion and hence greater power loss. However, the high Q's of the externally coupled resonator configurations quickly discount that as a possibility. The severe degradation of Q is blamed on the abrupt step discontinuity at the edge of the ZnO region which leads to severe bulk wave generation. Several analyses have been performed on the conversion of Rayleigh waves to bulk waves in reflector arrays and at a single shallow groove of finite width. Our interest, however, pertains to a single vertical step and the various reflections which occur at this discontinuity.
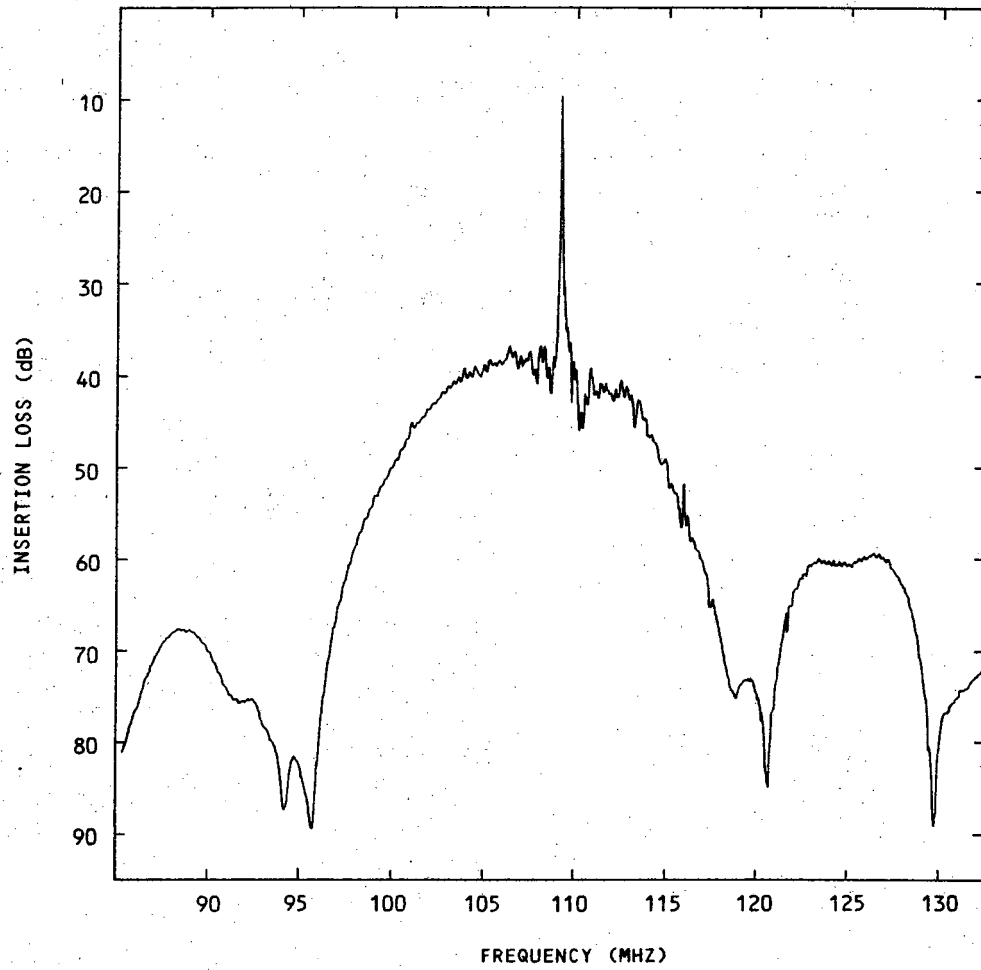
Figure 4.14

Two-port frequency response for an internally coupled ZnO/SiO$_2$/Si SAW resonator employing ion milled groove reflectors.
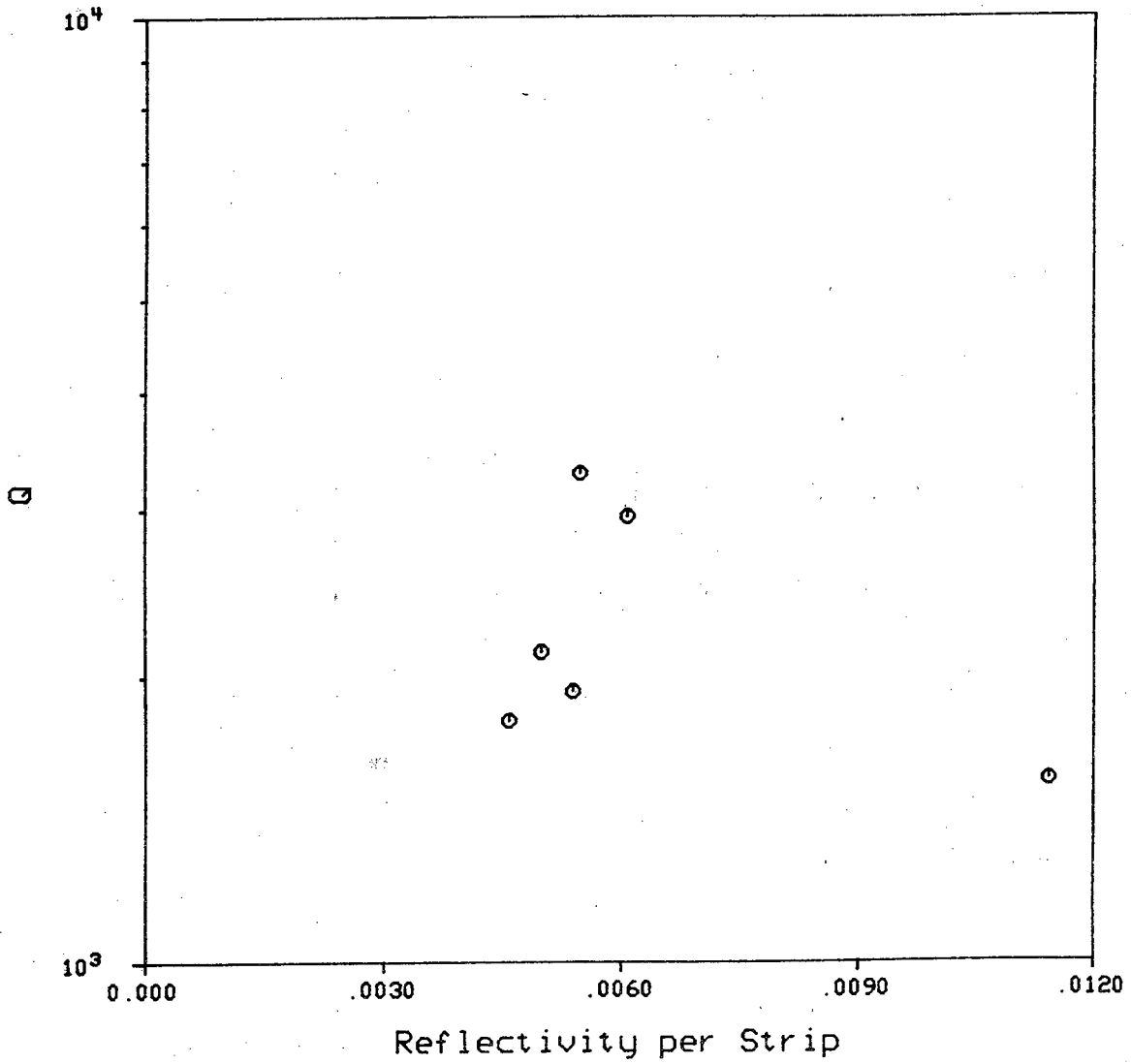
Figure 4.15

Resonator Q vs. reflectivity per strip for limited ZnO internally coupled resonators with grooves etched into SiO_2.
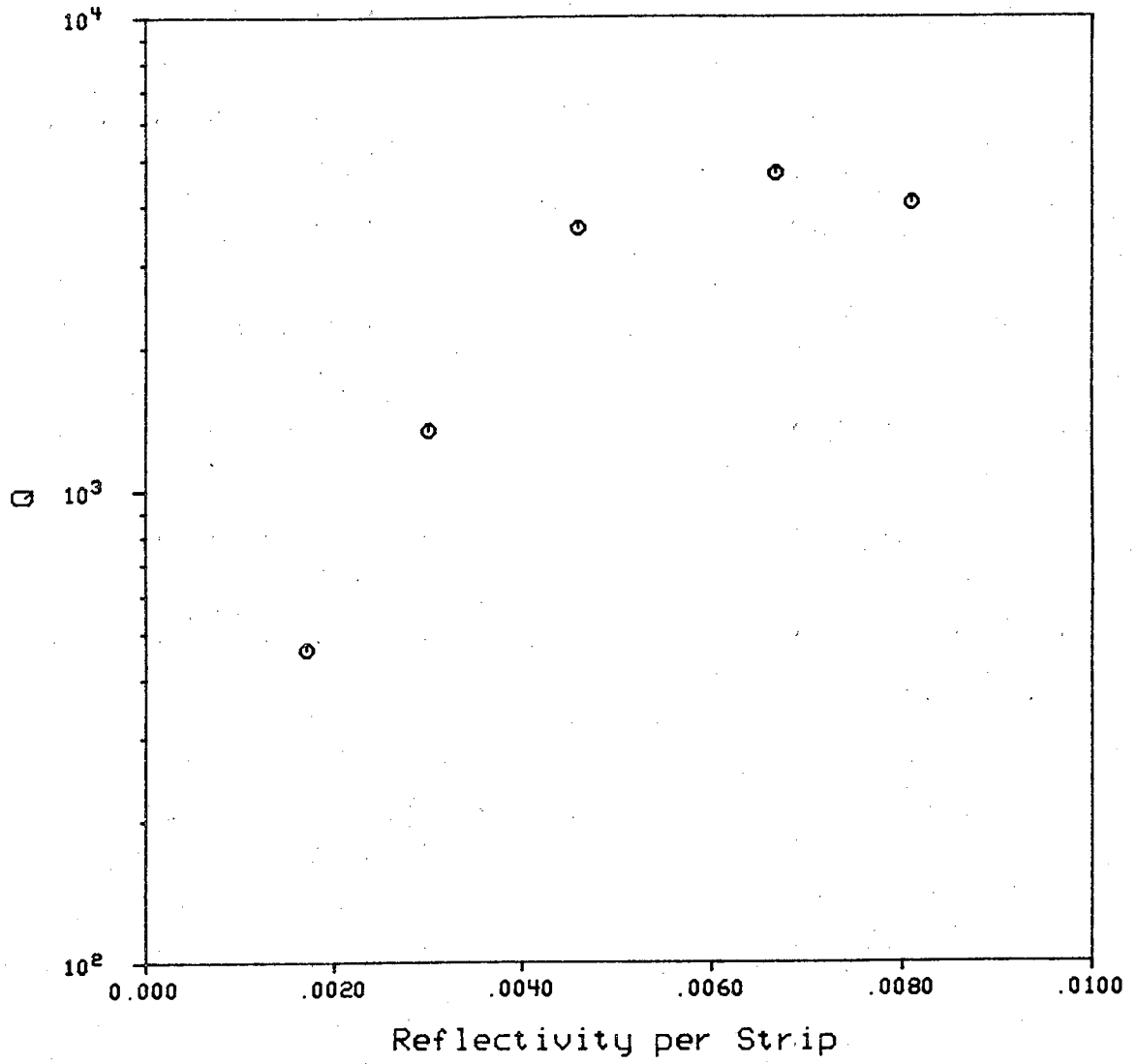
Figure 4.16

Resonator Q vs. reflectivity per strip for limited ZnO internally coupled resonators with grooves etched into unoxidized silicon.

4.5 Recessed ZnO SAW Resonator

Still wanting an internally coupled SAW resonator which exhibits higher Q-values because of the limited ZnO area, we designed an experiment to minimize the mechanical reflection at the edge of the ZnO region. The proposed structure, shown in Fig. 4.17, consists of the same features and dimensions as the internally coupled limited ZnO resonator shown in Fig. 4.9b, but with the ZnO layer recessed into the silicon substrate. The device is fabricated by placing a two mil thick metal mask* atop a silicon substrate on a special aluminum pallet. The mask/substrate/pallet assembly is fastened together by affixing an aluminum shield to the pallet as shown in Fig. 4.18. While all of the layers are in intimate contact, the entire assembly is placed into the ion mill and the silicon is etched to a depth of 8000 Å. After the groove is etched, and without breaking vacuum, a 1000 Å layer of Al is deposited as a shorting plane. The pallet and masks are then placed into the sputtering system and a 7000 Å ZnO film is sputtered, thereby making the ZnO film flush with the silicon surface. At this point, the mask is removed from the substrate and resonators are fabricated as described in Appendix D to yield the devices of Fig. 4.17.

4.5.1 Experimental Results

A series of resonators were fabricated with varying groove depths and Q-values were determined. Results of this experiment are shown in Fig. 4.19 for the recessed ZnO SAW resonators on silicon. The rather disappointing results are shown to behave the same as those of devices fabricated with limited ZnO

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* Moly permalloy (76% Ni, 20% Fe, 4% Mo)
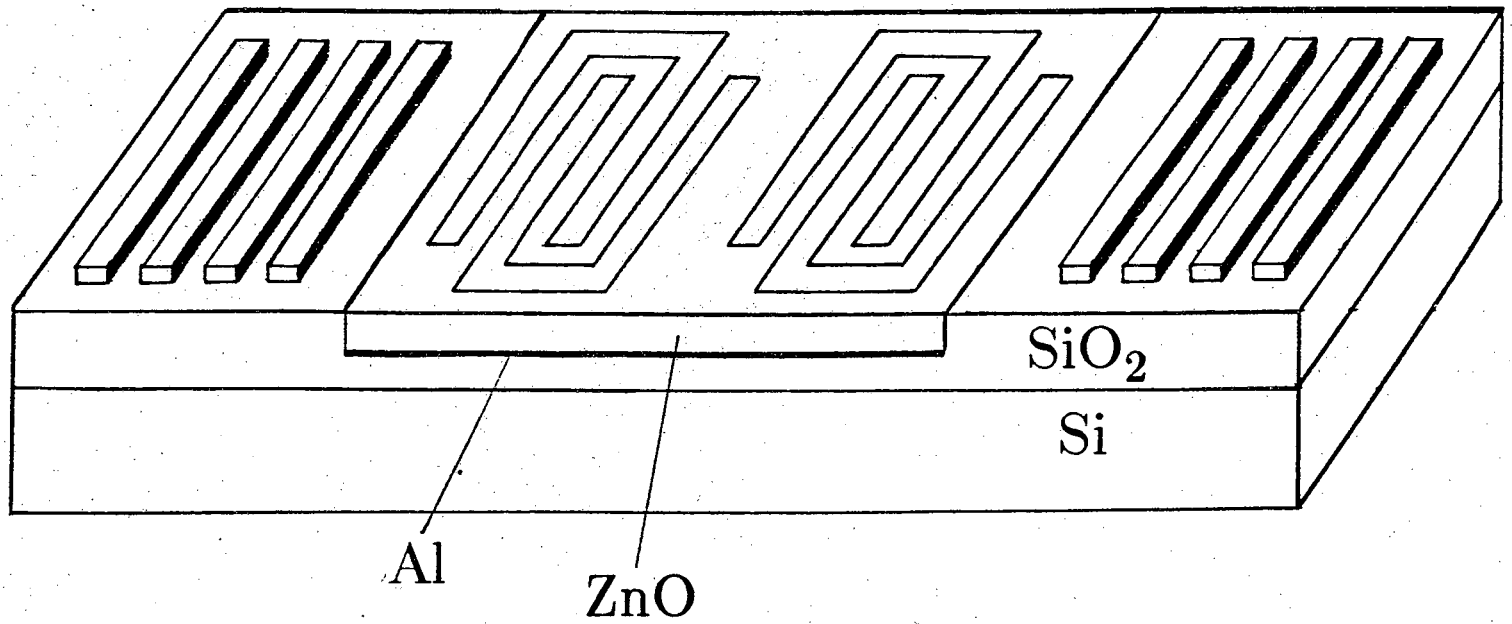
Figure 4.17

Schematic for a recessed ZnO SAW resonator.
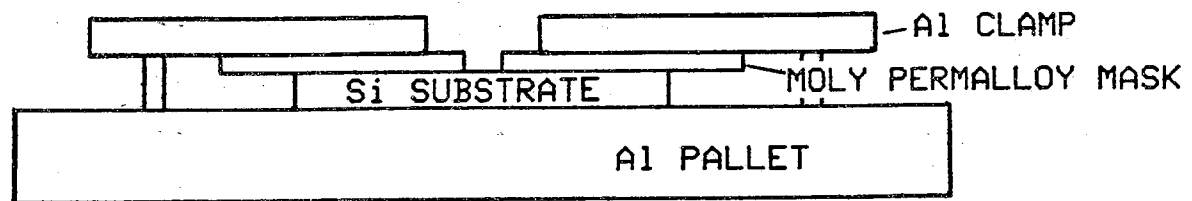
Figure 4.18

Recessed ZnO fabrication assembly.
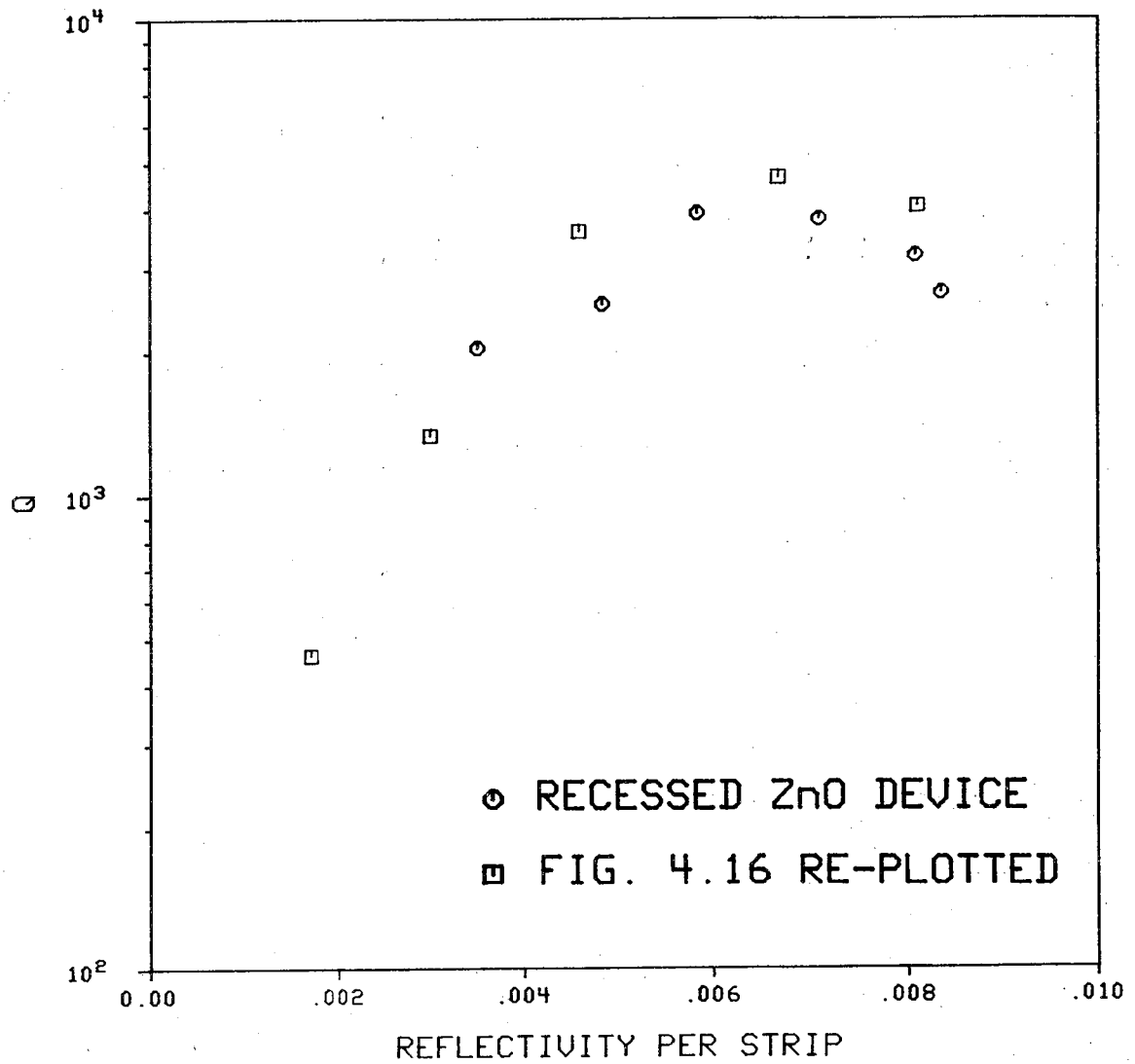
Figure 4.19

Q-value for recessed ZnO resonators for various groove depths. The data of Fig. 4.16 is replotted.

but no recessing of the ZnO. The highest Q-value obtained was 4000 and was achieved for only a modest reflectivity per strip of ~ 0.5%. Increasing groove depth again resulted in a degradation of Q-value. The recessed ZnO structure behaved as if a step existed at the edge of the ZnO.

To examine the edge of the transducer region, we have examined a device with a Dektak step measuring apparatus by dragging a stylus across the vertical ZnO/Si interface. A replica of the step region is shown in Fig. 4.20 for the internally coupled structure. It is apparent that the metal mask approach to recessing the ZnO layer to form a planar structure was unsuccessful. The edge of the ZnO region is seen to taper off over a few wavelengths and become very thin at the edge of the very large silicon barrier. The change in film thickness near the ZnO region edge is most likely due to the altered electric field pattern at the edge of the mask during both ion milling and rf sputtering. The reason for the large ridge at the edge of the silicon is still unexplained. Irrespective of its origin, the step has a severe effect upon the device Q (as shown in Fig. 4.19). Furthermore, because of the very wide gap between the ZnO and silicon regions, the metal mask recessed structure is not a reasonable technique for achievement of the structure of Fig. 4.17.

One possibility for reducing the bulk wave conversion at the step discontinuity is to taper the ZnO layer in a non-recessed structure. In addition to the increased fabrication complexity, however, the design of such a resonator becomes very complicated. Because of the dispersive nature of the layered $ZnO/SiO_2/Si$ system, reflectors in the tapered region would have to be spaced aperiodically to achieve maximum coherent reflection from each array. Additionally, the tapered ZnO layer would comprise a greater surface area of the substrate thereby increasing the propagation loss in the structure.
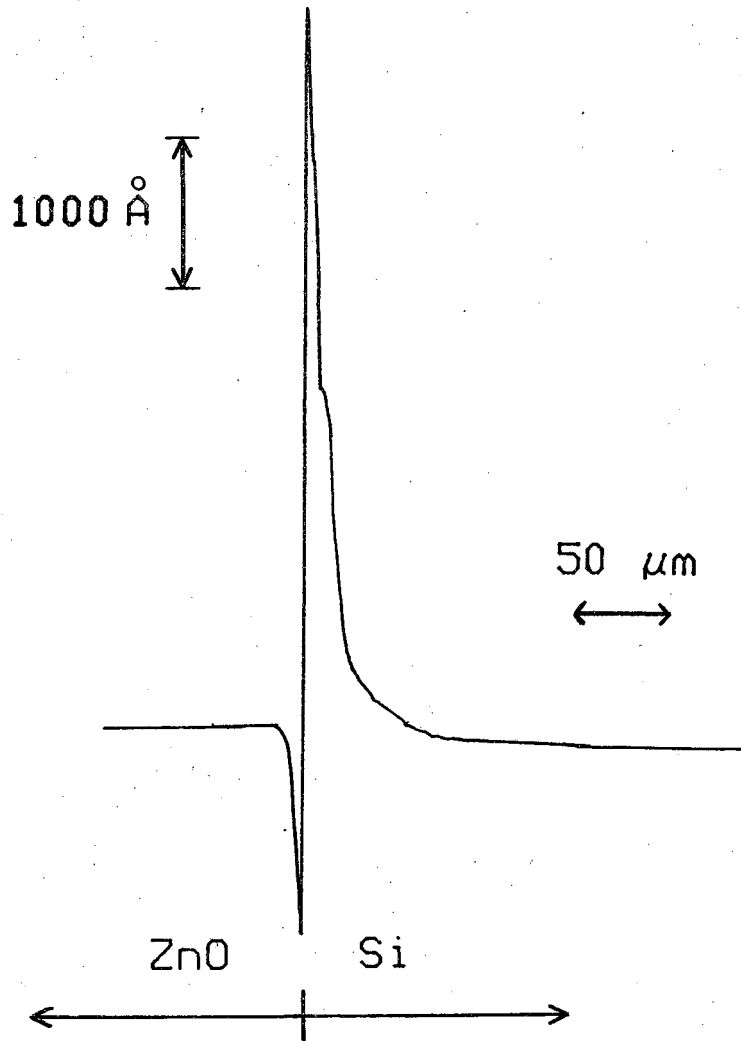
Figure 4.20

Profile of recessed ZnO edge determined by dragging a stylus over the surface.

4.6 Conclusions

We have demonstrated a means by which the Q-values of on-silicon SAW resonators can be enhanced through a minimization of the ZnO film area. Significant improvements were noted in externally coupled configurations but a degradation occurred for internally coupled devices.

The rationale behind fabricating these limited ZnO devices was to improve Q-values so that high frequency SAW resonators could be constructed with reasonable Q-values. At high frequencies, propagation loss in the ZnO film is the major Q-degrading factor and by reducing the area of the device containing ZnO, the device characteristics can be optimized.

We note here that the upper limit for device Q in the internally coupled resonator configuration is 5000 for an abrupt step at the edge of the ZnO. This maximum Q is frequency independent for the same ratio of step height to wavelength. The upper limit on device Q imposed by this step will always be 5000 because all dimensions scale proportionally at different frequencies. At frequencies in the GHz range, then, the Q limit imposed by the step will be far above the achievable Q due to other loss mechanisms in the structure (including propagation loss in the ZnO-less structure). Therefore, one can still benefit from the limited ZnO structure at high frequencies and take advantage of the reduced propagation loss in the regions without ZnO and without concern for the effect of the step discontinuity.

CHAPTER 5

MODE CONVERSION RESONATOR

5.1 Introduction

Most SAW resonators to date have employed Bragg reflection of a single longitudinal mode from periodic gratings of distributed reflectors to form resonant cavities. In addition to single mode Bragg reflection, the layered ZnO/SiO$_2$/Si configuration permits a different means by which wave energy can be confined to form an efficient resonant cavity via mode conversion between different propagating SAW modes. It has been demonstrated[34] that when the ZnO film is of sufficient thickness, the layered structure will support not only the first order Rayleigh mode but also higher order Rayleigh modes. Moreover, in the layered structure, it has been shown[23] that one can efficiently convert between these propagating modes by employing surface perturbations of a particular periodicity.

Recently, Martin et. al[103]. have demonstrated a ZnO-on-Si mode conversion resonator which employs conversion between the Rayleigh mode and the second order Rayleigh mode (or Sezawa mode) for the confinement of energy. In addition to the possibility for enhanced out-of-band rejection offered by this new configuration[89], the positional independence of transducers within the cavity has been demonstrated[104] which has greatly relaxed the previously critical spacing requirements necessary in all SAW resonators.

In this chapter we present a theoretical development of the mode conversion resonator. We first describe the basic device structure and principle of operation, followed by an analysis of the device theory. Prior to drawing conclusions we present experimental results of the mode conversion device to demonstrate the validity of our predictions.

5.2 Structure and Operation

A schematic of a two-port mode conversion resonator is shown in Fig. 5.1. The device consists of two interface[105] transducers, one of Rayleigh type with periodicity λ_R and the other of Sezawa type with periodicity λ_S. The rf diode sputtered ZnO film is 6.5 μm thick, which is of sufficient thickness to support both Rayleigh and Sezawa modes. The reflector array consists of grooves etched into the 1.0 μm SiO$_2$ layer. The periodicity of the grooves (with equal groove and space widths) is d, where d is given by[23,106]

$$k_R + k_S = \frac{2\pi}{d} \quad , \qquad (5.1)$$

at a fixed frequency where k_R and k_S are the Rayleigh and Sezawa wavenumbers, respectively.

A complete qualitative description of the operation of this device has been described elsewhere[89,103] so only a brief outline will be given here with the aid of Fig. 5.2.

Consider the excitation of a Rayleigh wave by the application of a sinusoidal signal to the Rayleigh IDT. The Rayleigh wave will propagate into the mode conversion grating where it will be back-scattered as a Sezawa wave. After traversing the cavity as a Sezawa wave, the wave will be re-reflected by the opposite grating as a Rayleigh wave. Since bi-directional transducers are
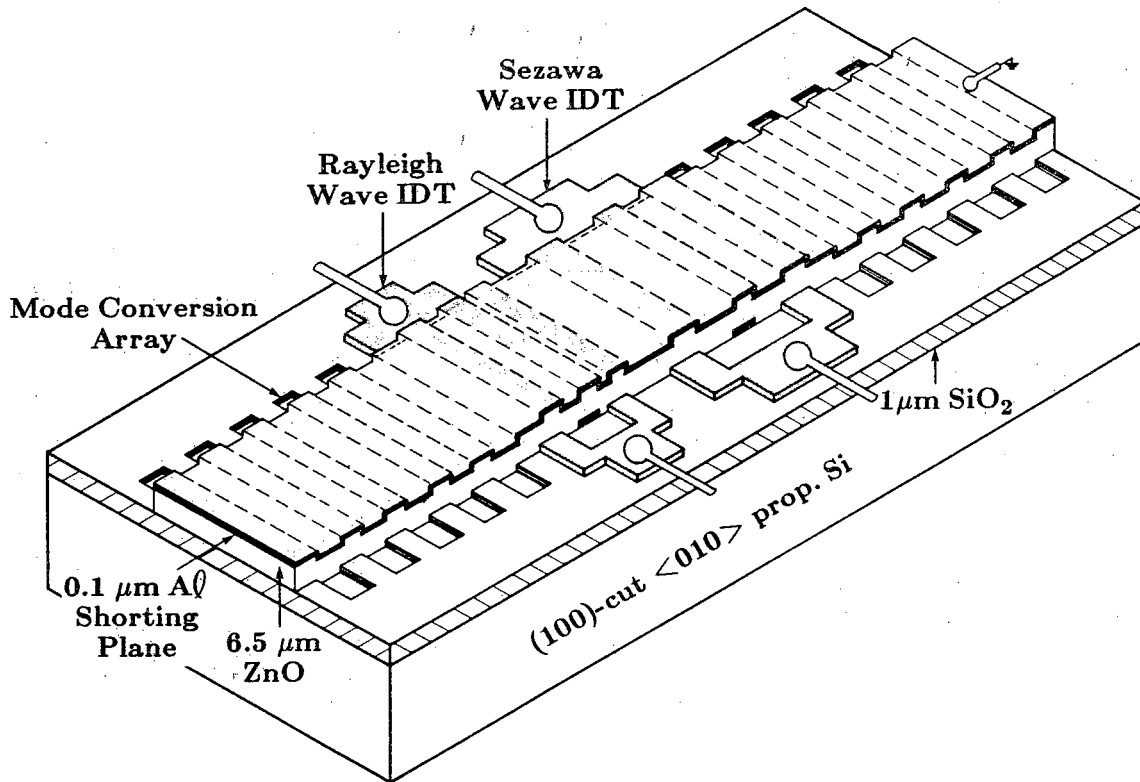
Figure 5.1

Schematic for a two-port mode conversion resonator utilizing interface Rayleigh and Sezawa type transducers.
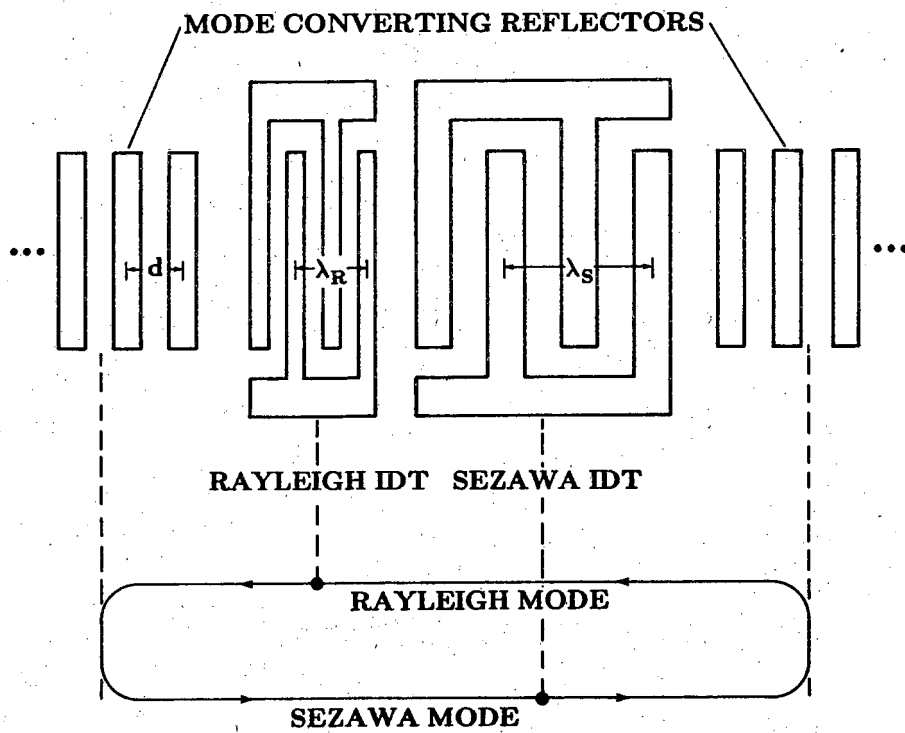
Figure 5.2

Schematic for a mode conversion resonator showing a resonant mode of the cavity.

used, this occurs in both directions such that waves of both types propagate simultaneously in each direction as a result of the excitation by only one transducer. It is the presence of the transducer that gives a definite phase relationship between the two propagating cavity modes. Each of these loops, as a Rayleigh wave in one direction and a Sezawa wave in the other direction is an eigenmode of the cavity. Furthermore, when the total round-trip phase shift of these modes, as a Rayleigh wave in one direction and a Sezawa wave in the other direction, is a multiple of 2π, then each of these modes is a resonant mode of the cavity. As long as no coupling exists between these cavity modes, they will be independent and degenerate. It should be noted that the same conditions could be realized had the Sezawa transducer been used to excite the waves.

It will be shown in this chapter that when the spacing between reflector arrays and the spacing between the transducers of different periodicities is equal to some critical value, a resonant condition is established whereby each transducer couples optimally to a standing wave of the same periodicity. Furthermore, it will be shown that under certain circumstances, the spacing between the transducer and the reflector arrays is non-critical for optimum device performance.

5.3 Analysis

To analyze the SAW mode conversion resonator, first consider a single IDT placed between mode converting arrays as shown in the schematic of Fig. 5.3. By examining the lone transducer one can formulate a method for determining the current in the IDT in the presence of propagating surface acoustic waves. This information, which leads to an expression for IDT

$\dfrac{V}{2}$ $\downarrow$ I

$R_1{}^+ \longrightarrow$

$\longleftarrow S_1{}^-$

Mode Conversion
Reflector Array

$\longleftarrow R_1{}^-$

$S_1{}^+ \longrightarrow$

$R_2{}^+ \longrightarrow$

$\longleftarrow S_2{}^-$

Mode Conversion
Reflector Array

$\longleftarrow R_2{}^-$

$S_2{}^+ \longrightarrow$

$-\dfrac{V}{2}$ $\downarrow$ I

$\longrightarrow$ y

$-l_1$ 0 l_2
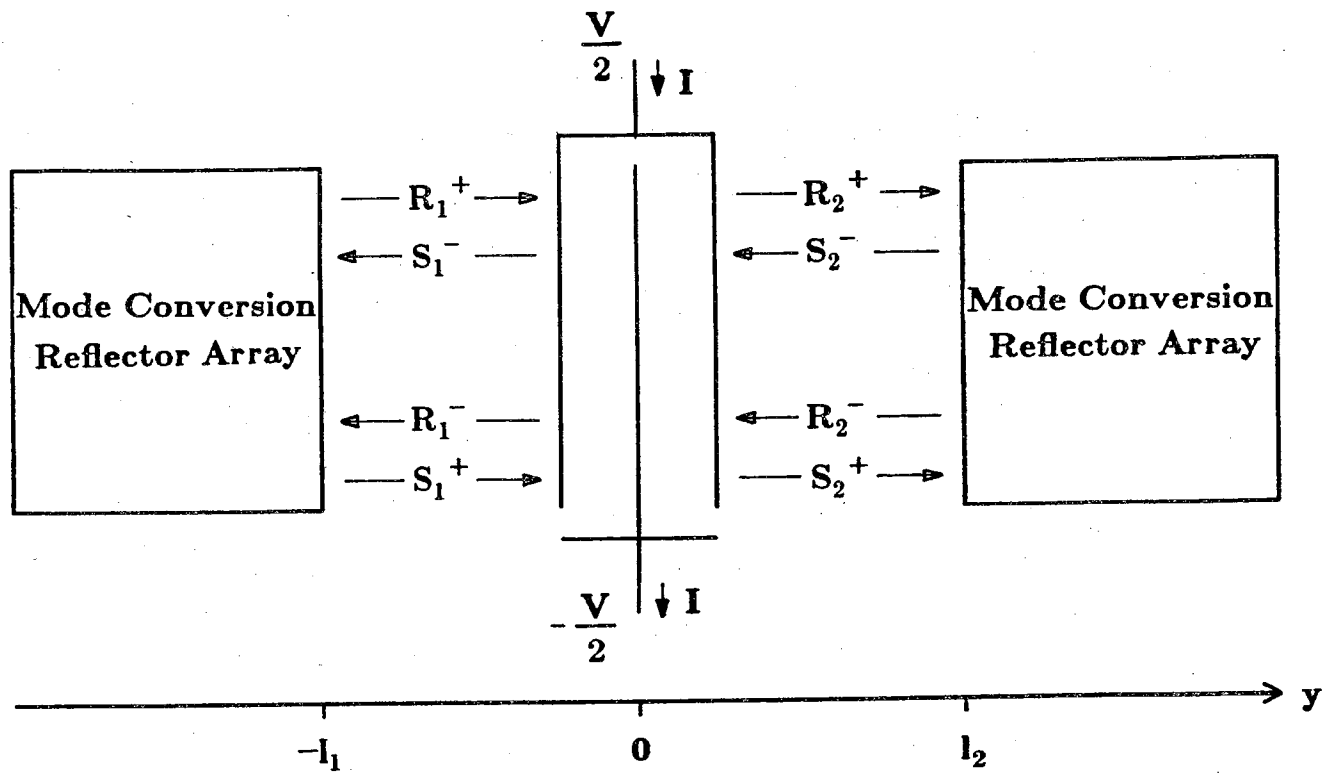
Figure 5.3

A one-port mode conversion resonator formed by two mode converting arrays.

conductance, is readily transferred to the case of the two-port mode conversion resonator (described in the next section).

The transducer can be examined as a linear 3-port device (having two acoustic ports and one electrical port). One can relate the input and output wave potentials to the voltage and current at the electrical port. For simplicity it is assumed that the transducer is symmetric about its center, y_c, so that there is no difference between coupling to propagating waves in the +y or -y directions. Referring to Fig. 5.2, one can write the acoustic wave amplitudes in the cavity as

$$S_2^+(y_c) = S_1^+(y_c) + \mu_S V_T \tag{5.2a}$$

$$R_1^-(y_c) = R_2^-(y_c) + \mu_R V_T \tag{5.2b}$$

$$S_1^-(y_c) = S_2^-(y_c) + \mu_S V_T \tag{5.2c}$$

$$R_2^+(y_c) = R_1^+(y_c) + \mu_R V_T \; . \tag{5.2d}$$

Here R and S represent the Rayleigh and Sezawa wave amplitudes respectively and the numerical subscripts reference a particular side of the transducer. The superscript + or - indicates the direction of propagation.

We are using the traveling electrostatic potential associated with an acoustic wave to denote its amplitude. Thus, in Eq. 5.2, μ_R and μ_S are dimensionless quantities representing the outgoing Rayleigh and Sezawa potentials per volt applied (V_T) to the transducers. The values μ_S and μ_R can be determined by examining the case of an isolated IDT in the absence of a grating such that $R_1^+(y_c) = S_1^+(y_c) = R_2^-(y_c) = S_2^-(y_c) = 0$. Following Martin[28], μ_S and μ_R are given by

$$\mu_S = \frac{jkw}{2} \left| \frac{\Delta v_S}{v_S} \right| \left[\frac{\sin\left(\frac{k_S w}{2}\right)}{\frac{k_S w}{2}} \right] \sum_{n=1}^{N} e^{jk_S y_n} e^{j\phi_n} \qquad (5.3a)$$

$$\mu_R = \frac{jkw}{2} \left| \frac{\Delta v_R}{v_R} \right| \left[\frac{\sin\left(\frac{k_R w}{2}\right)}{\frac{k_R w}{2}} \right] \sum_{n=1}^{N} e^{jk_R y_n} e^{j\phi_n} \quad , \qquad (5.3b)$$

where y_n and ϕ_n are the location and phase of the nth finger relative to the IDT center, w is the finger width, and N is the number of fingers in the IDT. The electromechanical coupling to the Sezawa and Rayleigh modes is represented by $\frac{\Delta v_S}{v_S}$ and $\frac{\Delta v_R}{v_R}$ respectively, and w is the width per IDT finger.

For an IDT placed in the presence of propagating waves one has components of IDT current due to both the potential applied to the IDT and induced by the potentials of the propagating surface acoustic waves. The total current in the IDT is given by

$$I = G_S V_T + G_R V_T + g_{S_+} S_1^+(y_c) + g_{S_-} S_2^-(y_c) + g_{R_+} R_1^+(y_c) + g_{R_-} R_2^-(y_c) \quad (5.4)$$

The terms G_R and G_S represent the radiation conductance of the transducer for Rayleigh and Sezawa waves respectively and V_T is the applied transducer voltage. Here we have not included the purely capacitive current which is independent of the acoustic interaction (assuming weak coupling). The terms g_R and g_S are conductance-type terms which relate the potentials of incoming surface waves to the current induced in the IDT. Due to symmetry, $g_{S_+} = g_{S_-} = g_S$, and $g_{R_+} = g_{R_-} = g_R$ where[28]

$$g_S = -\frac{j\omega C_f}{2}\left[\frac{\sin\left(\frac{k_S w}{2}\right)}{\frac{k_S w}{2}}\right]\sum_{n=1}^{N}e^{-jk_S y_n}e^{-j\phi_n} \tag{5.5a}$$

$$g_R = -\frac{j\omega C_f}{2}\left[\frac{\sin\left(\frac{k_R w}{2}\right)}{\frac{k_R w}{2}}\right]\sum_{n=1}^{N}e^{-jk_R y_n}e^{-j\phi_n} \tag{5.5b}$$

where C_f is the capacitance per finger and w is the finger width. Here again, y_n is the position of the nth finger with respect to the IDT center and N is the number of fingers in the IDT.

We are now in a position to relate the wave potentials outgoing from the IDT to the potentials incident upon the IDT via the reflection coefficients of the reflector arrays, Γ_{1RS}, Γ_{2RS}, Γ_{1SR}, and Γ_{2SR}. The reflection coefficient Γ_{1RS} represents the scattering from the Rayleigh mode to the Sezawa mode by reflector array 1 (Fig. 5.3) and similarly for Γ_{2RS}, Γ_{1SR}, and Γ_{2SR}. The relationships between the wave potentials incident upon an array, and back-scattered from an array (referenced to the IDT center), are given by

$$S_1^+(y_c) = \Gamma_{1RS}R_1^-(y_c)e^{-j(k_R + k_S)(l_1 + y_c)} \tag{5.6a}$$

$$R_2^-(y_c) = \Gamma_{2SR}S_2^+(y_c)e^{-j(k_R + k_S)(l_2 - y_c)} \tag{5.6b}$$

$$R_1^+(y_c) = \Gamma_{1SR}S_1^-(y_c)e^{-j(k_R + k_S)(l_1 + y_c)} \tag{5.6c}$$

$$S_2^-(y_c) = \Gamma_{2RS}R_2^+(y_c)e^{-j(k_R + k_S)(l_2 - y_c)} \quad , \tag{5.6d}$$

where $-l_1$ and l_2 are the edges of the reflector array as shown in Fig. 5.3. In

Eq. 5.6 the array reflection coefficients are referenced to the edge of the reflector array such that

$$\Gamma_{1RS} = \left|\Gamma_{1RS}\right| e^{-j\phi} \qquad (5.7a)$$

$$\Gamma_{1SR} = \left|\Gamma_{1SR}\right| e^{-j\phi} \qquad (5.7b)$$

$$\Gamma_{2SR} = \left|\Gamma_{2SR}\right| e^{-j\phi} \qquad (5.7c)$$

$$\Gamma_{2RS} = \left|\Gamma_{2RS}\right| e^{-j\phi} \qquad (5.7d)$$

where ϕ is the array reflection phase referenced to the edge of the array.

The expression for incident IDT potentials in terms of array scattering coefficients (Eq. 5.6) enables one to rewrite the steady-state Rayleigh and Sezawa potentials inside the mode conversion cavity in terms of the array reflection coefficients, the voltage applied to the IDT used for excitation, and the coupling terms μ_R, and μ_S. Solving Eq. 5.2 subject to Eq. 5.6 one obtains expressions for surface wave potentials incoming to the IDT in terms of the applied IDT voltage, giving

$$R_1^+(y_c) = \frac{\Gamma_{1SR}\left[\mu_S e^{-j(k_R + k_S)y_c} + \Gamma_{2RS}\mu_R e^{-j(k_R + k_S)l_2}\right]e^{-j(k_R + k_S)l_1}V_T}{1 - \Gamma_{1SR}\Gamma_{2RS}e^{-j(k_R + k_S)(l_1 + l_2)}} \qquad (5.8a)$$

$$R_2^-(y_c) = \frac{\Gamma_{2SR}\left[\mu_S e^{j(k_R + k_S)y_c} + \Gamma_{1RS}\mu_R e^{-j(k_R + k_S)l_1}\right]e^{-j(k_R + k_S)l_2}V_T}{1 - \Gamma_{2SR}\Gamma_{1RS}e^{-j(k_R + k_S)(l_1 + l_2)}} \qquad (5.8b)$$

$$S_1^+(y_c) = \frac{\Gamma_{1RS}\left[\mu_R e^{-j(k_R + k_S)y_c} + \Gamma_{2SR}\mu_S e^{-j(k_R + k_S)l_2}\right]e^{-j(k_R + k_S)l_1}V_T}{1 - \Gamma_{1RS}\Gamma_{2SR}e^{-j(k_R + k_S)(l_1 + l_2)}} \qquad (5.8c)$$

$$S_2^-(y_c) = \frac{\Gamma_{2RS}\left[\mu_R e^{j(k_R + k_S)y_c} + \Gamma_{1SR}\mu_S e^{-j(k_R + k_S)l_1}\right]e^{-j(k_R + k_S)l_2}V_T}{1 - \Gamma_{2RS}\Gamma_{1SR}e^{-j(k_R + k_S)(l_1 + l_2)}} \qquad (5.8d)$$

Substituting the expressions for wave potentials in terms of applied voltage from Eq. 5.8 into Eq. 5.4, one can obtain the IDT current in terms of the IDT voltage and the various parameters fixed by the device dimensions. The process just described allows one to calculate the input admittance of an IDT in the presence of propagating surface waves. In the next section we will use this method to analyze the two-port mode conversion resonator.

5.4 The Two-Port Mode Conversion Resonator

In the mode conversion resonator two independent resonant modes are simultaneously present. Each of these independent modes consists of a Rayleigh wave in one direction and a Sezawa wave in the opposite direction. In a two-port mode conversion resonator we couple into the cavity through either the Rayleigh or Sezawa mode and we couple out of the cavity through the other mode.

To analyze the two-port mode conversion resonator we utilize a two-port admittance matrix as follows

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \quad , \qquad (5.9)$$

where the values for I_1, I_2, V_1, and V_2 are referenced as shown in Fig. 5.4. When computing the matrix elements, the coordinate system shown in Fig. 5.4 will be used with the center of IDT 1 at $y_{c_1} = 0$ and the center of IDT 2 at $y_{c_2} = l$. At this point, no restrictions have been placed on the IDT periodicity although we show later the benefit of using IDT's "tuned" to different modes.
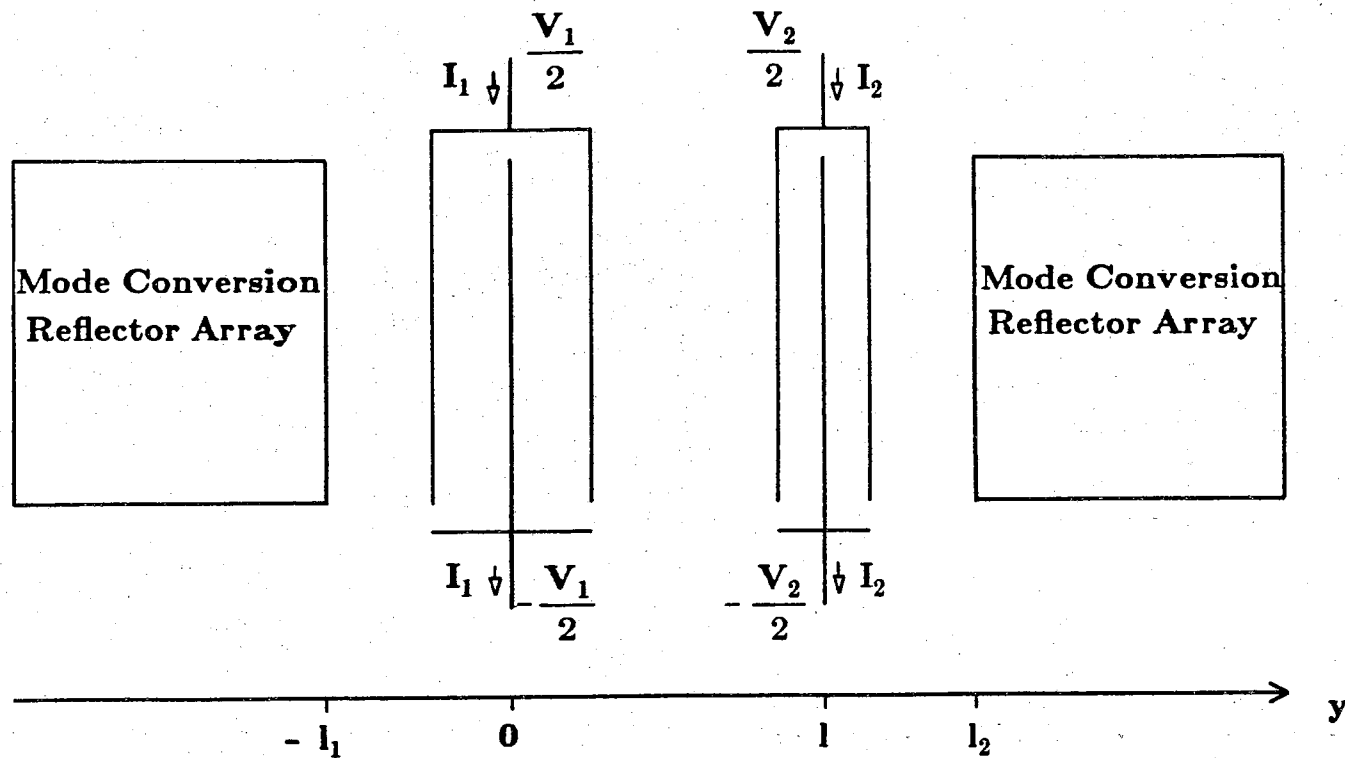
Figure 5.4

A two-port mode conversion resonator with electrical variables indicated.

The admittance matrix components can be evaluated similar to the manner described in the previous section by first obtaining an expression for IDT current in terms of the applied voltage and incoming wave potentials. One can thus evaluate Y_{11} and Y_{22} where

$$Y_{11} = \left.\frac{I_1}{V_1}\right|_{V_2 = 0} \quad , \quad Y_{22} = \left.\frac{I_2}{V_2}\right|_{V_1 = 0} . \qquad (5.10)$$

The transconductance terms Y_{12} and Y_{21} can be calculated by computing the short-circuit current induced on transducer 1 due to an applied voltage on IDT 2 and vice versa, giving

$$Y_{12} = \left.\frac{I_1}{V_2}\right|_{V_1 = 0} \quad , \quad Y_{21} = \left.\frac{I_2}{V_1}\right|_{V_2 = 0} , \qquad (5.11)$$

although only one term need be calculated since reciprocity guarantees that $Y_{12} = Y_{21}$.

To evaluate the admittance matrix elements, one must have expressions for the current in each transducer. In terms of the incident wave potentials and the applied IDT voltage one has, similar to Eq. 5.4,

$$I_1 = (g_{1R}\mu_{1R} + g_{1S}\mu_{1S})V_1 + g_{1R}\left[R_1^+(0) + R_2^-(0)\right] + g_{1S}\left[S_1^+(0) + S_2^-(0)\right] \qquad (5.12a)$$

$$I_2 = (g_{2R}\mu_{2R} + g_{2S}\mu_{2S})V_2 + g_{2R}\left[R_1^+(l) + R_2^-(l)\right] + g_{2S}\left[S_1^+(l) + S_2^-(l)\right] \qquad (5.12b)$$

where the subscripts 1 and 2 on μ and g make reference to IDT 1 and IDT 2 respectively. When computing Y_{11} and Y_{22}, the Sezawa and Rayleigh wave potentials are due to V_1 and V_2 respectively. When computing Y_{12}, however, the wave potentials that induce current in IDT 1 are due to a voltage V_2 applied to IDT 2 and similarly for Y_{21}.

In the two-port mode conversion resonator the admittance elements Y_{11} and Y_{22} are determined by replacing the wave potentials in the current equations of Eq. 5.12 with wave potentials defined in Eq. 5.8 in terms of the proper applied IDT voltage. We follow through this example by calculating Y_{22} which gives,

$$Y_{22} = (\mu_{2R}g_{2R} + \mu_{2S}g_{2S}) \tag{5.13}$$

$$+ g_{2R}\left[\frac{\Gamma_{1SR}\left(\mu_{2S}e^{-j(k_R + k_S)l} + \Gamma_{2RS}\mu_{2R}e^{-j(k_R + k_S)l_2}\right)e^{-j(k_R + k_S)l_1}}{1 - \Gamma^2 e^{-j(k_R + k_S)L_o}}\right]$$

$$+ g_{2R}\left[\frac{\Gamma_{2SR}\left(\mu_{2S}e^{-j(k_R + k_S)l} + \Gamma_{1RS}\mu_{2R}e^{-j(k_R + k_S)l_1}\right)e^{-j(k_R + k_S)l_2}}{1 - \Gamma^2 e^{-j(k_R + k_S)L_o}}\right]$$

$$+ g_{2S}\left[\frac{\Gamma_{1RS}\left(\mu_{2R}e^{-j(k_R + k_S)l} + \Gamma_{2SR}\mu_{2S}e^{-j(k_R + k_S)l_2}\right)e^{-j(k_R + k_S)l_1}}{1 - \Gamma^2 e^{-j(k_R + k_S)L_o}}\right]$$

$$+ g_{2S}\left[\frac{\Gamma_{2RS}\left(\mu_{2R}e^{-j(k_R + k_S)l} + \Gamma_{1SR}\mu_{2S}e^{-j(k_R + k_S)l_1}\right)e^{-j(k_R + k_S)l_2}}{1 - \Gamma^2 e^{-j(k_R + k_S)L_o}}\right] .$$

Calculation of Y_{11} gives the same result as Y_{22} but with l=0 and g_{2R}, g_{2S}, μ_{2R}, and μ_{2S} replaced by g_{1R}, g_{1S}, μ_{1R}, and μ_{1S} respectively. In Eq. 5.13 the subscripts 1 and 2 refer to IDT 1 and IDT 2 respectively as shown in Fig. 5.3. For example μ_{1S} refers to how IDT 1 transmits a Sezawa wave and g_{2R} refers to how IDT 2 receives a Rayleigh wave.

In a similar way the transconductance terms Y_{12} and Y_{21} can be calculated by solving

$$Y_{12} = \frac{I_1}{V_2}\bigg|_{V_1 = 0} \qquad Y_{21} = \frac{I_2}{V_1}\bigg|_{V_2 = 0} \qquad (5.14)$$

We first write the equation for I_1, the short circuit current induced on IDT 1 due to a voltage V_2 applied to IDT 2. The current equation for IDT 1 in terms of the SAW potentials incident on IDT 2 (described by Eq. 5.12) is given by

$$I_1 = g_{1R}\left[R_1^+(0) + R_2^-(0)\right] + g_{1S}\left[S_1^+(0) + S_2^-(0)\right] \quad . \qquad (5.15)$$

Furthermore, we can rewrite the wave potentials incident on IDT 1 in terms of the potentials incoming into IDT 2 to give the short-circuit IDT current

$$I_1 = g_{1R}\left[R_1^+(l)\right]e^{jk_R l} + g_{1R}\left[R_2^-(l) + \mu_{2R}V_2\right]e^{-jk_R l} \qquad (5.16)$$

$$+ g_{1S}\left[S_1^+(l)\right]e^{jk_S l} + g_{1S}\left[S_2^-(l) + \mu_{2S}V_2\right]e^{-jk_S l} \quad .$$

Replacing the SAW cavity potentials as before with those given in Eq. 5.6, one can determine the short-circuit transconductance Y_{12} between IDT's yielding:

$$Y_{12} = g_{1R}\left[\frac{\Gamma_{1SR}\left[\mu_{2S}e^{-j(k_R + k_S)l} + \Gamma_{2RS}\mu_{2R}e^{-j(k_R + k_S)l_2}\right]e^{-j(k_R + k_S)l_1}}{1 - \Gamma^2 e^{-j(k_R + k_S)(l_1 + l_2)}}\right]e^{jk_R l} \qquad (5.17)$$

$$+ g_{1R}\left[\frac{\Gamma_{2SR}\left[\mu_{2S}e^{j(k_R + k_S)l} + \Gamma_{1RS}\mu_{2R}e^{-j(k_R + k_S)l_1}\right]e^{-j(k_R + k_S)l_2}}{1 - \Gamma^2 e^{-j(k_R + k_S)(l_1 + l_2)}} + \mu_{2R}\right]e^{-jk_R l}$$

$$+ g_{1S}\left[\frac{\Gamma_{1RS}\left[\mu_{2R}e^{-j(k_R + k_S)l} + \Gamma_{2SR}\mu_{2S}e^{-j(k_R + k_S)l_2}\right]e^{-j(k_R + k_S)l_1}}{1 - \Gamma^2 e^{-j(k_R + k_S)(l_1 + l_2)}}\right]e^{jk_S l}$$

$$+ \; g_{1S} \left[\frac{\Gamma_{2RS}\left[\mu_{2R}e^{j(k_R + k_S)l} + \Gamma_{1SR}\mu_{2S}e^{-j(k_R + k_S)l_1}\right]e^{-j(k_R + k_S)l_2}}{1 - \Gamma^2 e^{-j(k_R + k_S)(l_1 + l_2)}} + \mu_{2S} \right] e^{jk_Sl}$$

In the same manner one can calculate Y_{21} and the result is the same as for Y_{12} with g_{1R}, g_{1S}, μ_{2R}, and μ_{2S} replaced by g_{2R}, g_{2S}, μ_{1R}, and μ_{1S} respectively, and with $l = 0$.

In this device we have $\mu_{1R}g_{2R} = \mu_{2R}g_{1R}$ and $\mu_{1S}g_{2S} = \mu_{2S}g_{1S}$ resulting from the fact that for a particular mode, the ratio $\frac{\mu}{g}$ is independent of IDT design if the finger lengths are identical[107]. Because of the reciprocal nature of this device, a separate calculation of Y_{21} is unnecessary since reciprocity guarantees $Y_{12} = Y_{21}$.

An interesting aside to the calculation of the transconductance terms Y_{12} and Y_{21} occurs when one determines the transconductance between IDT 1 and IDT 2 outside the mode conversion bandwidth (Γ's are zero) giving

$$Y_{12} = Y_{21} = g_{1R}\mu_{2R}e^{-jk_Rl} + g_{1S}\mu_{2S}e^{-jk_Sl} \quad . \qquad (5.18)$$

This result is particularly interesting because it allows one to compute the delay line response between IDT's in a medium which supports two propagating modes. Furthermore, outside the mode conversion bandwidth, Y_{21} is limited by the cross-coupling terms μ_{2S} and g_{1R} which represent the coupling between the Sezawa IDT (1) and the Rayleigh mode, and the Rayleigh IDT (2) and the Sezawa mode.

Having determined the admittance matrix elements we now may assume (this is done experimentally) that transducer 1 is tuned to the Sezawa mode and transducer 2 is tuned to the Rayleigh mode. This implies $\mu_{1S} \gg \mu_{1R}$, $g_{1S} \gg g_{1R}$, $\mu_{2R} \gg \mu_{2S}$, $g_{2R} \gg g_{2S}$, $G_{1S} \gg G_{1R}$, and $G_{2R} \gg G_{2S}$.

In the vicinity of resonance, Eq. 5.13 and Eq. 5.17 give way to

$$Y_{11} = \mu_{1S}g_{1S} + \mu_{1S}g_{1S}\left[\frac{\Gamma_{1RS}\Gamma_{2SR}e^{-jK(l_1+l_2)}}{1-\Gamma_{1RS}\Gamma_{2SR}e^{-jK(l_1+l_2)}} + \frac{\Gamma_{2RS}\Gamma_{1SR}e^{-jK(l_1+l_2)}}{1-\Gamma_{2RS}\Gamma_{1SR}e^{-jK(l_1+l_2)}}\right] \quad (5.19a)$$

$$Y_{12} = g_{1S}\mu_{2R}\left[\frac{\Gamma_{1RS}e^{-jK(l_1+l)}e^{jk_Sl}}{1-\Gamma_{1RS}\Gamma_{2SR}e^{-jK(l_1+l_2)}} + \frac{\Gamma_{2RS}e^{-jK(l_2-l)}e^{-jk_Sl}}{1-\Gamma_{2RS}\Gamma_{1SR}e^{-jK(l_1+l_2)}}\right] \quad (5.19b)$$

$$Y_{21} = g_{2R}\mu_{1S}\left[\frac{\Gamma_{1SR}e^{-jKl_1}e^{-jk_Rl}}{1-\Gamma_{1SR}\Gamma_{2RS}e^{-jK(l_1+l_2)}} + \frac{\Gamma_{2SR}e^{-jKl_2}e^{jk_Rl}}{1-\Gamma_{2SR}\Gamma_{1RS}e^{-jK(l_1+l_2)}}\right] \quad (5.19c)$$

$$Y_{22} = \mu_{2R}g_{2R} + \mu_{2R}g_{2R}\left[\frac{\Gamma_{1SR}\Gamma_{2RS}e^{-jK(l_1+l_2)}}{1-\Gamma_{1SR}\Gamma_{2RS}e^{-jK(l_1+l_2)}} + \frac{\Gamma_{2SR}\Gamma_{1RS}e^{-jK(l_1+l_2)}}{1-\Gamma_{2SR}\Gamma_{1RS}e^{-jK(l_1+l_2)}}\right] \quad (5.19d)$$

where $K = k_R + k_S$. Additionally, due to symmetry

$$\Gamma_{1RS} = \Gamma_{2RS} = \Gamma_{RS} \quad (5.20a)$$

$$\Gamma_{1SR} = \Gamma_{2SR} = \Gamma_{SR} \quad (5.20b)$$

and we define

$$\Gamma^2 = \Gamma_{RS}\Gamma_{SR} \quad (5.21)$$

We further simplify Eq. 5.19 by letting $(l_1 + l_2)$, the separation between arrays, be L_o yielding

$$Y_{11} = \mu_{1S}g_{1S}\left[\frac{1 + \Gamma^2 e^{-j(k_R+k_S)L_o}}{1 - \Gamma^2 e^{-j(k_R+k_S)L_o}}\right] \quad (5.22a)$$

$$Y_{12} = g_{1S}\mu_{2R}\left[\frac{\Gamma_{RS}e^{-j(k_R + k_S)(l_1 + 1)}e^{jk_S l}}{1 - \Gamma^2 e^{-j(k_R + k_S)L_o}} + \frac{\Gamma_{RS}e^{-j(k_R + k_S)(l_2' - 1)}e^{-jk_S l}}{1 - \Gamma^2 e^{-j(k_R + k_S)L_o}}\right] \qquad (5.22b)$$

$$Y_{21} = g_{2R}\mu_{1S}\left[\frac{\Gamma_{SR}e^{-j(k_R + k_S)l_1}e^{-jk_R l}}{1 - \Gamma^2 e^{-j(k_R + k_S)L_o}} + \frac{\Gamma_{SR}e^{-j(k_R + k_S)l_2}e^{jk_R l}}{1 - \Gamma^2 e^{-j(k_R + k_S)L_o}}\right] \qquad (5.22c)$$

$$Y_{22} = \mu_{2R}g_{2R}\left[\frac{1 + \Gamma^2 e^{-j(k_R + k_S)L_o}}{1 - \Gamma^2 e^{-j(k_R + k_S)L_o}}\right] . \qquad (5.22d)$$

To further simplify the expression of Eq. 5.22 we require that the radiation conductances of the two IDT's are equal outside the mode conversion bandwidth such that

$$\mu_{1S}g_{1S} = \mu_{2R}g_{2R} = G_o \qquad (5.23)$$

Additionally, if we consider two IDT's of different periodicity placed side-by-side next to a mode conversion reflector, reciprocity guarantees

$$\mu_{1S}\Gamma_{SR}g_{2R} = \mu_{2R}\Gamma_{RS}g_{1S} . \qquad (5.24)$$

That is, the transconductance between IDT's when a Sezawa wave (of power p_o) is excited by IDT 1, reflected by the array as a Rayleigh wave, and detected by IDT 2 would be the same as if a Rayleigh wave (also of power p_o) had been launched by IDT 2, reflected by the array as a Sezawa wave, and detected using IDT 1.

The combined result of Eq.'s 5.23 and 5.24 yields

$$\mu_{2R} = \mu_{1S}\sqrt{\frac{\Gamma_{SR}}{\Gamma_{RS}}} \qquad (5.25)$$

which gives the admittance matrix elements in the vicinity of resonance

$$Y_{11} = Y_{22} = G_o \left[\frac{1 + \Gamma^2 e^{-j(k_R + k_S)L_o}}{1 - \Gamma^2 e^{-j(k_R + k_S)L_o}} \right] \qquad (5.26)$$

$$Y_{12} = Y_{21} = G_o \left[\frac{\Gamma \left[e^{-j(k_R + k_S)(l_1 + l)} e^{jk_S l} + e^{-j(k_R + k_S)(l_2 - l)} e^{-jk_S l} \right]}{1 - \Gamma^2 e^{-j(k_R + k_S)L_o}} \right] \qquad (5.27)$$

It should be noted that $Y_{12} = Y_{21}$ even without the condition imposed by Eq. 5.23 which was merely introduced for convenience.

5.4.1 Equivalent Circuit Representation

We now construct an equivalent circuit for the SAW mode conversion resonator as shown in Fig. 5.5a. To optimize device performance at resonance, we desire the shunt elements ($Y_{11} + Y_{12}$, and $Y_{22} + Y_{21}$) vanish, and that Y_{12} and Y_{21} are maximized (Fig. 5.5b). Y_{12} and Y_{21} are given in Eq. 5.27 and, with a slight amount of manipulation, it can be shown that

$$Y_{11} + Y_{12} = Y_{21} + Y_{22} = G_o \left[\frac{\left[1 + \Gamma e^{-jK(l_1 + l)} e^{jk_S l} \right] \left[1 + \Gamma^{-jK(l_2 - l)} e^{-jk_S l} \right]}{1 - \Gamma^2 e^{-jKL_o}} \right] \quad . \qquad (5.28)$$

where $K = k_R + k_S$. From Eq.'s 5.27 and 5.28 above, the desired resonant conditions are realized (i.e., Y_{12} is maximized while $Y_{11} + Y_{12}$ is minimized) when the following equations are satisfied:

$$\Gamma e^{-j[(k_R + k_S)(l_1 + l) - k_S l]} = -1 \qquad (5.29a)$$

$$\Gamma e^{-j[(k_R + k_S)(l_2 - l) + k_S l]} = -1 \qquad . \qquad (5.29b)$$

The above equation requires
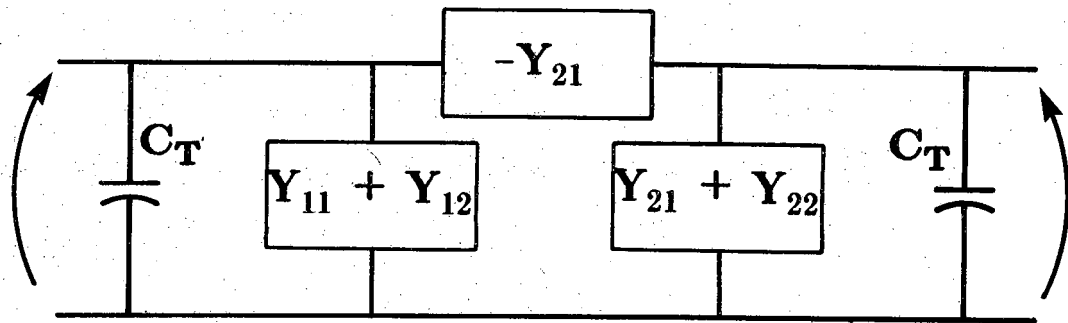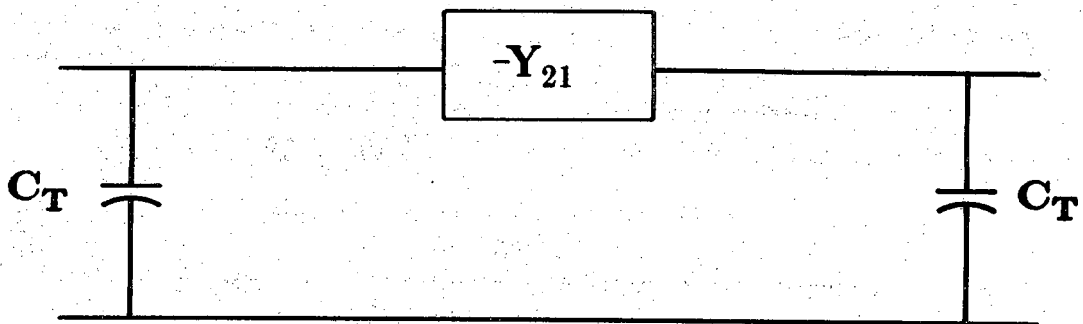
Figure 5.5

(a) Equivalent circuit configuration for a two-port mode conversion resonator. (b) Simplified circuit near resonance.

$$(k_R + k_S)(l_1 + l) - k_S l + \phi = (2n + 1)\pi \tag{5.30a}$$

$$(k_R + k_S)(l_2 - l) + k_S l + \phi = (2m + 1)\pi \quad . \tag{5.30b}$$

Adding Eq.'s 5.30a and 5.30b together and using the mode conversion condition of Eq. 5.1 yields the result

$$L_o = l_1 + l_2 = nd \quad . \tag{5.31}$$

That is, for resonance to occur, the separation between reflectors must be an integer number of array periods. Furthermore, solving Eq. 5.30 for l, the separation between transducers, gives

$$l = \left[m + \left(\frac{l_2 - l_1}{d} \right) \right] \frac{\lambda_R}{2} \quad . \tag{5.32}$$

Thus, we have determined the required reflector array spacing conditions for resonance to occur and also the allowed locations for the IDT's of different periodicity to satisfy the maximum coupling condition.

We note here that the two-port mode conversion resonator employing transducers of different periodicities requires a critical spacing between IDT's dependent upon the placement of the first IDT. However, the first IDT may be placed anywhere between reflector arrays.

5.5 Experimental Results

Mode conversion resonators satisfying the proper spacing requirements have been fabricated in the configuration shown in Fig. 5.1. Interface transducers were used because the structure with an aluminum shorting plane atop the ZnO provides comparable values for Rayleigh and Sezawa electromechanical coupling factors. The (100)-cut, [010]-propagating silicon

substrate was thermally oxidized to a thickness of 1.0 μm. The grooves in the SiO$_2$ layer were ion beam etched to a depth of approximately 1000 Å deep which corresponds to a reflectivity per groove of approximately 1%. At a frequency of 147 MHz, the Rayleigh wave with $\lambda_R = 19.6$ μm and a Sezawa wave with $\lambda_S = 34.9$ μm were coupled by the array of periodicity d = 12.9 μm.

The two-port transmission response of a mode conversion resonator is shown in Fig. 5.6. The Q value for this particular device is approximately 3000, indicating that the mode conversion process is very efficient.

An additional comment about the two-port mode conversion resonator is in order concerning the off-resonant coupling level between the IDT's of different periodicity. It is shown above that the cross-coupling level is of the form

$$Y_{12} = Y_{21} = g_{1R}\mu_{2R}e^{-jk_Rl} + g_{1S}\mu_{2S}e^{-jk_Sl} \qquad . \qquad (5.18)$$

where the terms g_{1R} and μ_{2S} are cross-coupling terms. The mode conversion resonator offers the possibility of enhanced out-of-band rejection by increasing the number of fingers per IDT to reduce the cross-coupling terms. It can be seen from Eq.'s 5.3 and 5.5 that μ_{1R} and g_{2S} will decrease as N_1 and N_2 increase due to the non-coherent addition of phasors arising from coupling to a mode with wavelength λ_R by an IDT having periodicity λ_S, and vice versa.

5.5.1 Spatial Independence

Although the required spacings for proper implementation of the mode conversion resonator have already been derived, it is worthwhile to go back and briefly examine the results. In particular, it is interesting to consider a one-
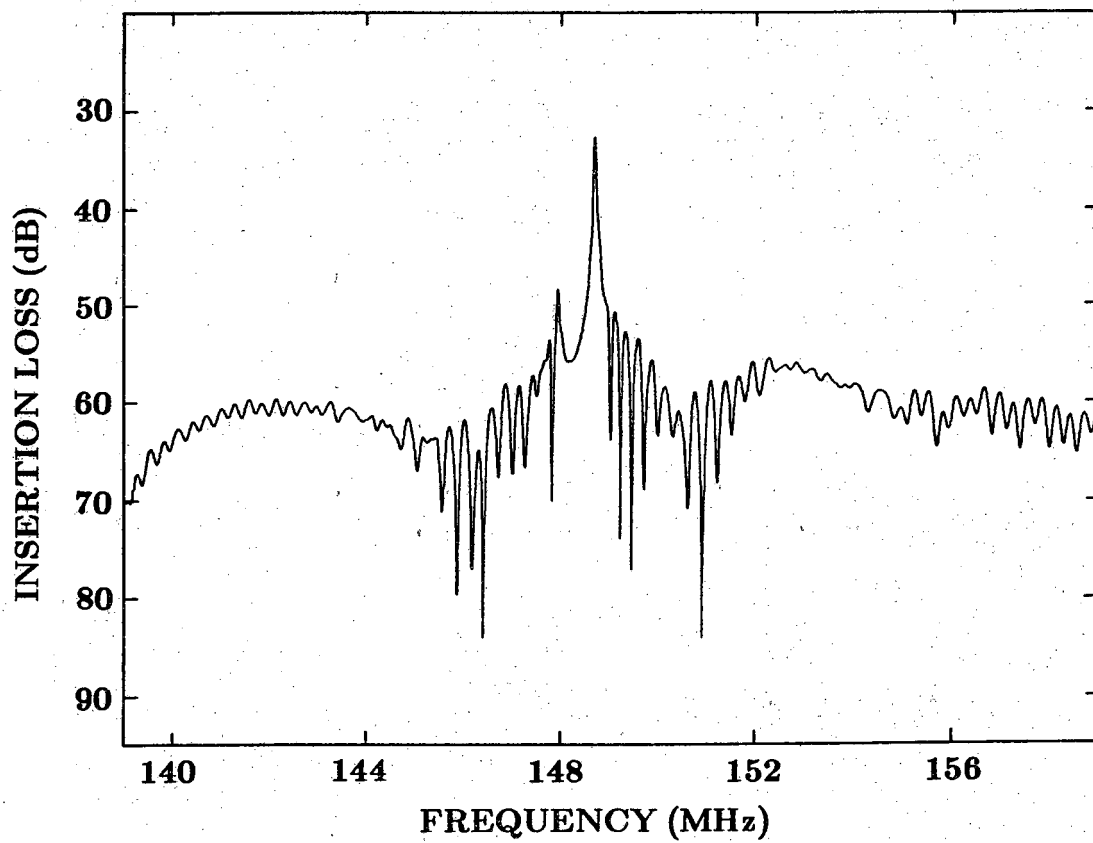
Figure 5.6

Two-port transmission response for a mode conversion resonator employing transducers of different periodicity.

port mode conversion resonator with an IDT of Rayleigh or Sezawa type.

When computing the input admittance for the one-port device, one would obtain the same result as for Y_{11} or Y_{22} in Eq. 5.26 assuming that $\mu g = G_o$ for the single transducer. In a one-port mode conversion resonator then, resonance is satisfied whenever $\Gamma^2 e^{-j(k_R + k_S)L_o}$ is real and positive, and is demonstrated by a significant enhancement in the radiation conductance at the resonant frequency. Thus, resonance will occur whenever,

$$(k_R + k_S)L_o + 2\phi = m\pi \quad . \tag{5.33}$$

Here again, using the mode conversion condition of Eq. 5.1, and the fact that $\phi = 0$ or π, one has $L_o = nd$ where d is the array periodicity; this is the same result for reflector array separation derived for the two-port mode conversion resonator.

For the single-port device considered earlier, the placement of the first (and only) IDT was arbitrary. As a result, as long as the spacing between reflector arrays is an integer number of array periods, the IDT (of either Rayleigh or Sezawa type) can be placed anywhere between reflectors and it will automatically satisfy the maximum coupling condition.

Since placement of an IDT anywhere inside the resonant cavity fixes the location of the standing wave of the same periodicity, one can place another IDT of the same periodicity an integer number of half-wavelengths from the first IDT, thereby coupling optimally to the same standing wave in a two-port configuration. Therefore, as long as the IDT's are of the same periodicity and separated by an integer number of half-wavelengths, the IDT pair can be placed anywhere between the two reflectors and maximum coupling is

guaranteed. Additionally, either a Rayleigh IDT pair or a Sezawa IDT pair may be used for this resonator.

5.5.2 Experimental Results

To demonstrate the positional independence of the resonator response on IDT position, we fabricated both one-port and two-port mode conversion devices with different spacings between transducers and reflector arrays. Both types of devices were fabricated on (100) cut ([100] propagating) silicon substrates. The only changes between devices were the positions of the transducers between reflector arrays. All transducers used were of Sezawa type and had a periodicity of 35.5μm. The transducers for the one-port devices had nine finger-pairs while the transducers used in the two-port devices had five finger-pairs each. For both structures, the reflector arrays consisted of 400 ion beam etched grooves 1300 Å deep with a periodicity of 12.7 μm and a beamwidth of 1.5 mm. For the devices used in this experiment, the transducers and reflector arrays were defined on the top surface of the ZnO rather than at the ZnO/SiO$_2$ interface (Fig. 5.6) because equivalent coupling to both wave types was no longer necessary[103]. The array separation used in all devices was 0.762 mm which corresponds to 60 grating periods.

In the one-port mode conversion resonator we fabricated a series of devices with the transducer position varied by fractions of a Sezawa wavelength from the center of the cavity. The devices fabricated had transducers placed $\dfrac{n\lambda_S}{16}$ from the center of the reflectors with n = 0,1,2,....,7. Results of this experiment can be seen in Fig. 5.7 which shows the measured radiation conductance, G_a,

Figure 5.7

Radiation conductance vs. frequency determined experimentally for one-port mode conversion resonators (right) and computed for conventional one-port resonators (left). In both results the transducer was displaced from the cavity center an amount $\dfrac{n\lambda_s}{16}$ for (a) n=0 (b) n=1 (c) n=2 (d) n=3 (e) n=4 (f) n=6 (g) n=7.
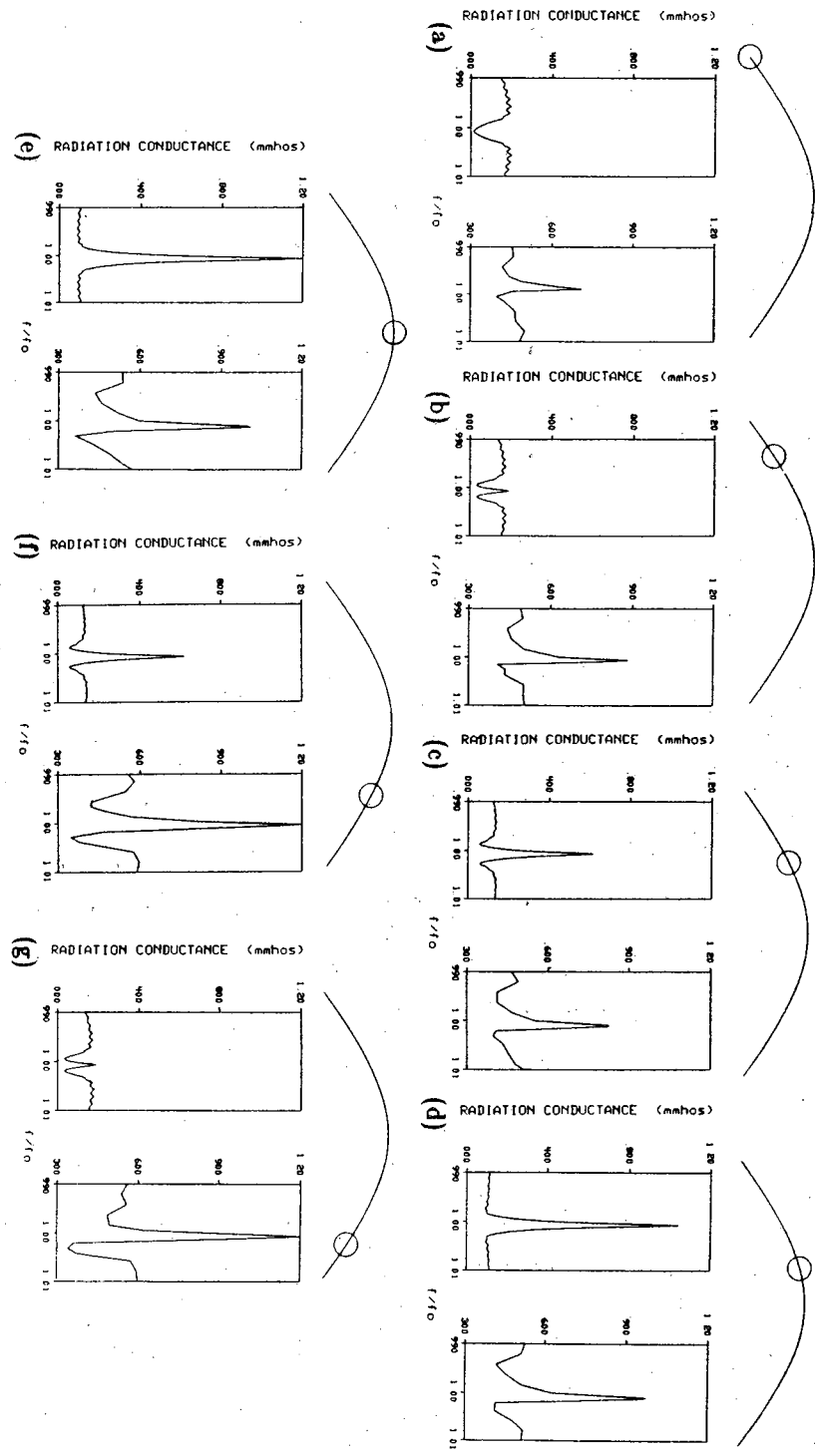
Figure 5.7

for a number of transducer positions for the mode conversion resonator together with computed G_a values for conventional one-port resonators with the same spacings.

As is expected, in a conventional one-port structure with the same spacing, the resonant coupling condition greatly depends on the transducer placement between reflectors. In the mode conversion resonator structure, however, resonance as demonstrated by the enhanced radiation conductance, can be observed for any location of the IDT.

A similar experiment was performed for two-port mode conversion resonators with a fixed spacing of $10\lambda_S$ between centers of identical Sezawa transducers. The midpoint of the pair of transducers was varied from the cavity center by the same fraction as in the one-port experiment; the results are shown in Fig. 5.8. Here again, the calculated response for a conventional device with the same dimensions was computed and plotted alongside the experimental results. It is evident that as the location of the transducer pair is moved within the cavity, there are drastic changes in the response of a conventional device (i.e. resonance and antiresonance) but the results for a two-port mode conversion resonator are almost invariant.

For both one-port and two-port device structures the resonant Q values were in the range 900-1500 but it should be noted that no attempt was made to optimize these resonators but rather to demonstrate the positional independence of the transducer placement. It should also be pointed out that in both one-port and two-port devices, slight variations in the device responses for different spacings are due to the fact that the standing Rayleigh wave pattern is not invisible to the Sezawa IDT's and some coupling will exist which will be different for each spacing chosen. This variation can be minimized by

Figure 5.8

Two-port transmission response vs. frequency determined experimentally for mode conversion resonators (right) and computed for conventional two-port resonators (left). In both devices, the transducer pair was displaced from the cavity center by an amount $\dfrac{n\lambda_s}{16}$ for (a) n=1 (b) n=2 (c) n=3 (d) n=5 (e) n=6 (f) n=7.
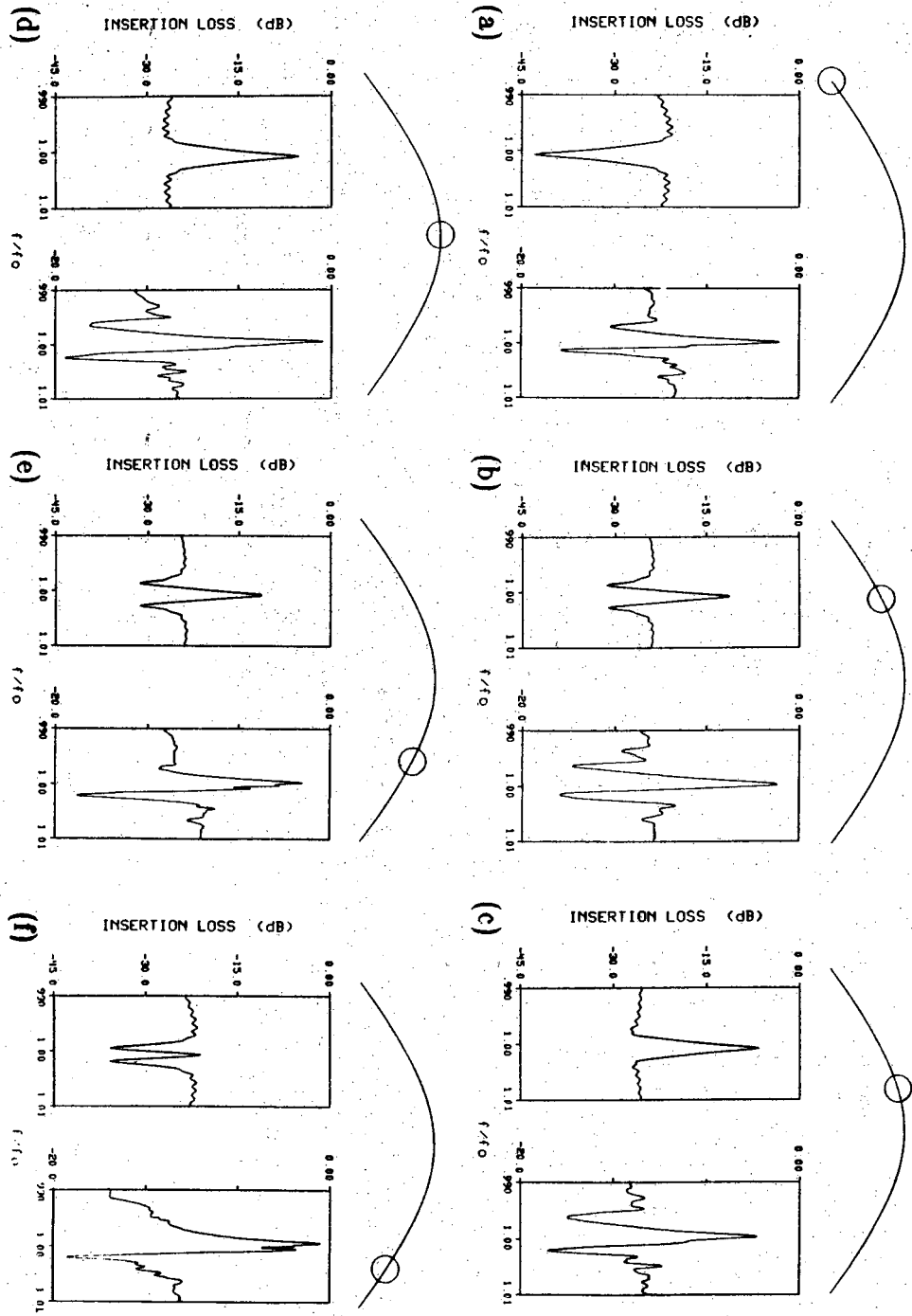
Figure 5.8

increasing the number of fingers per transducer.

CHAPTER 6

CONCLUSIONS AND RECOMMENDATIONS

FOR FURTHER RESEARCH

6.1 Conclusions

The results presented in this report deal with a wide number of devices for use in signal processing applications in the UHF-VHF range. The most significant contributions are the following:

1. Description and implementation of a monolithic SAW memory correlator which utilizes ion implantation for the confinement of signal storage regions. The implant-isolated storage correlator has exhibited a 3 dB storage time more than 10 times longer than any previously reported monolithic memory correlator with the promise of longer storage times if proper precautions are taken.

2. We have predicted and demonstrated a method for determining the potential at the silicon surface associated with a propagating acoustic wave.

3. A simple model has been presented which accurately predicts the charging process occurring in a storage correlator which employs rf writing techniques for its operation. From this model we have demonstrated a means for determining the effective recombination lifetime of inversion layer minority carrier holes behave when injected into a depletion region

of an n-type silicon substrate. Furthermore, our charge storage theory also predicts the charge storage operation for pn diode memory arrays.

In addition to the implant-isolated storage correlator which relies on the acoustoelectric interactions of the propagating SAW potential inside the semiconductor, we have also fabricated improved SAW resonators in a variety of configurations. SAW resonator results are as follows:

4. SAW resonators have been fabricated with ZnO limited to the IDT regions for an externally coupled configuration. Q values in excess of 30,000 have been reported in the externally coupled configuration. Using these devices, estimates of propagation loss have been made for surface acoustic waves on oxidized and unoxidized silicon substrates.

5. Internally coupled limited ZnO SAW resonators have been fabricated in a number of configurations. These prototype devices, along with their externally coupled counterparts will be important in the fabrication of high frequency SAW resonators on silicon where the propagation loss due to the ZnO film is assumed to be the limiting Q factor.

6. A revised theory has been presented for the SAW mode conversion resonator. This theory accurately predicts the positional independence of IDT's in a one-port SAW resonator and has led to the experimental verification of this property. Furthermore, two-port mode conversion resonators were fabricated which demonstrated positional independence of properly separated IDT's. The theory also predicts the separation between IDT's necessary when coupling to the resonator with IDT's of different periodicity.

6.2 Recommendations for Further Research

Recommendations for further research include:

1. The fabrication of an implant-isolated storage correlator with a high quality ZnO film to determine the maximum possible dynamic range.

2. Fabrication of an implant-isolated storage correlator in an attempt to maximize the storage time of the device.

3. Utilization of a gate controlled diode to demonstrate electronic erasure for the implant-isolated correlator.

4. The pursuit of $ZnO/SiO_2/Si$ device characteristics for high frequency applications. With electron beam lithography capability, GHz SAW resonators with ZnO limited to IDT regions can be fabricated and tested.

5. High frequency ZnO-on-silicon research must include a thorough study of the microstructure of ZnO films and a method must be developed for depositing well oriented piezoelectric films which are < 1000 Å thick. ZnO deposition by laser evaporation has been demonstrated elsewhere[108] indicating the possible growth by means of molecular beam epitaxy.

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APPENDICES

Appendix A

Writing Signal Approximation

For a single pulse applied to a storage region one has, after a rectangular pulse of amplitude V_1 and duration Δt_1, a modified surface charge density of Q_1 given by

$$Q_1 = Q_{seq} - C_I V_1 (1 - e^{-\Delta t_1/\tau_R}) \quad . \tag{A.1}$$

If one applies another pulse of amplitude V_2 and duration Δt_2 at some instant immediately after turning off pulse V_1, then the surface charge density is given by

$$Q_2 = Q_{seq} - C_I V_2 + \left[Q_1 - (Q_{seq} - C_I V_2) \right] e^{-\Delta t_2/\tau_R} \tag{A.2}$$

$$= Q_{seq} - C_I V_2 (1 - e^{-\Delta t_2/\tau_R}) - C_I V_1 e^{-\Delta t_2/\tau_R}(1 - e^{-\Delta t_1/\tau_R}) \quad .$$

Similarly, with the application of numerous narrow pulses of amplitudes V_i, one can replicate any time varying signal. If one discretizes the desired signal into uniform increments of duration Δt, one can determine the surface charge density for the application of a signal $N\Delta t$ long by

$$Q_N = Q_{seq} - C_I (1 - e^{-\Delta t/\tau_R}) \left[\sum_{i=1}^{N} V_i e^{-(n-i)\Delta t/\tau_R} \right] \quad , \quad V_i > 0 \quad . \tag{A.3}$$

Furthermore, in addition to the constraint that V_i must be positive, as the storage depletion width expands, only pulses sufficiently large to contribute to

further charge storage are used in the computation of Q_N. That is, pulses incapable of depleting the semiconductor more than its existing deep depletion value do not contribute to signal storage. Referring to Eq. A.2, this requires that we impose the additional constraint that

$$C_I V_i > Q_{seq} - Q_{i-1} \qquad (A.4)$$

for the ith pulse, V_i, to contribute to charge storage. If the inequality of Eq. A.4 is not satisfied, then $Q_i = Q_{i-1}$ because the pulse V_i will have no net effect upon the inversion layer charge. So as a storage region nears saturation, only the maximum portions of each rf cycle will contribute to the stored reference signal and the effective writing time of each cycle decreases.

For completeness we rewrite Eq. A.3 with the proper constraints

$$Q_N = Q_{seq} - C_I(1 - e^{-\Delta t/\tau_R}) \left[\sum_{i=1}^{N} V_i e^{-(n-i)\Delta t/\tau_R} \right] \quad , \quad C_I V_i > Q_{seq} - Q_{i-1} \quad . \qquad (A.5)$$

Appendix B

Electronic Measurement Setups

In measurements performed on the implant-isolated storage correlator, all connections were made with double shielded coaxial cable[*] to reduce spurious rf pickup. Solid-state switches[**] were used in place of the previously preferred double mixer arrangement because of simplicity as well as better isolation. The solid-state switches require a slightly negative ($\sim$ -0.5 V) baseline from the pulse generator (switching signal) for optimum turn-off.

In Fig. B.1 we show the electronic setup for performing degenerate convolution measurements on the implant-isolated storage correlator. In all convolution and correlation measurements, IDT input power levels were kept below 31 dBm to avoid burning out the devices.

The slightly more complex electronic setup for storage correlation is shown in Fig. B.2. Three pulse generators (acoustic, reading, writing) control the correlation function. The reference signal pulse generator is used to control the reference signal duration as well as the correlation periodicity. The reading signal pulse generator has a variable delay function built into it which is important in making storage time measurements. The oscilloscope is triggered

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[*] Alpha Wire Co., Type RG-55 R/U
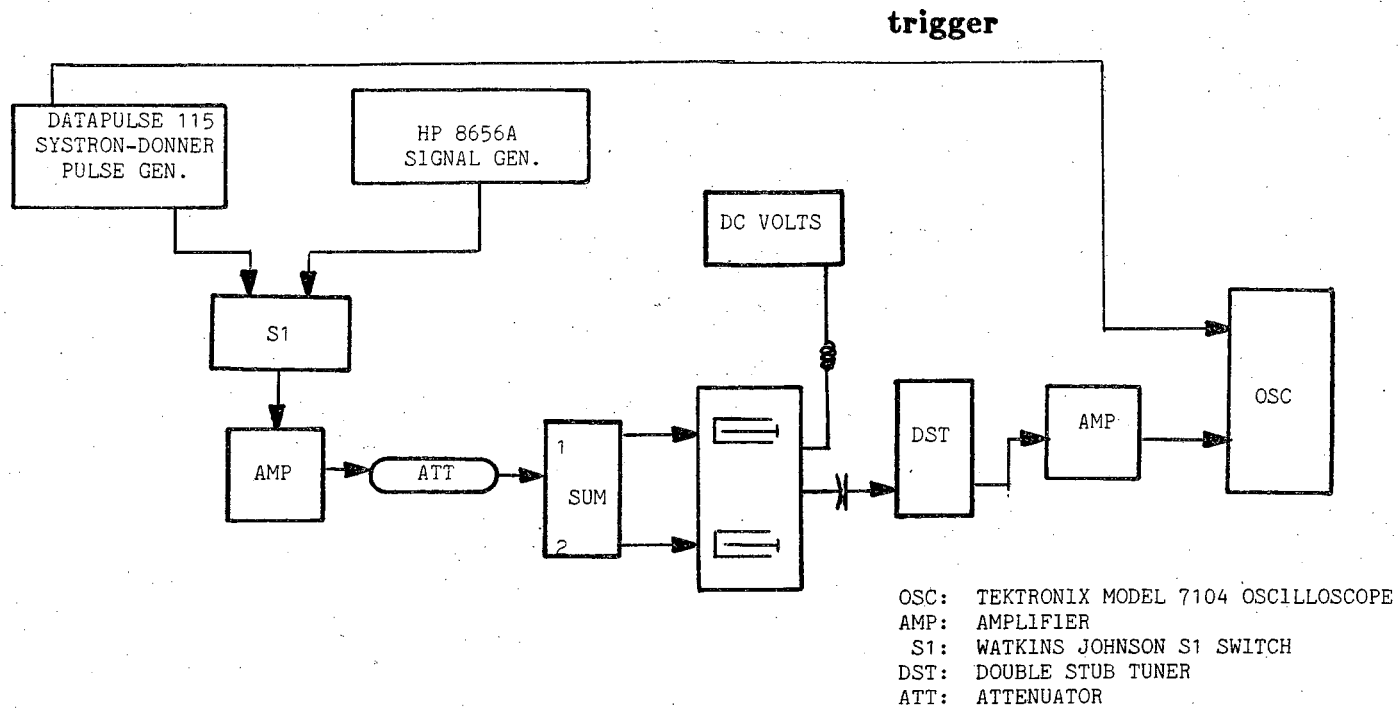[**] Watkins-Johnson model S1

Figure B.1

Electronic setup for degenerate convolution.
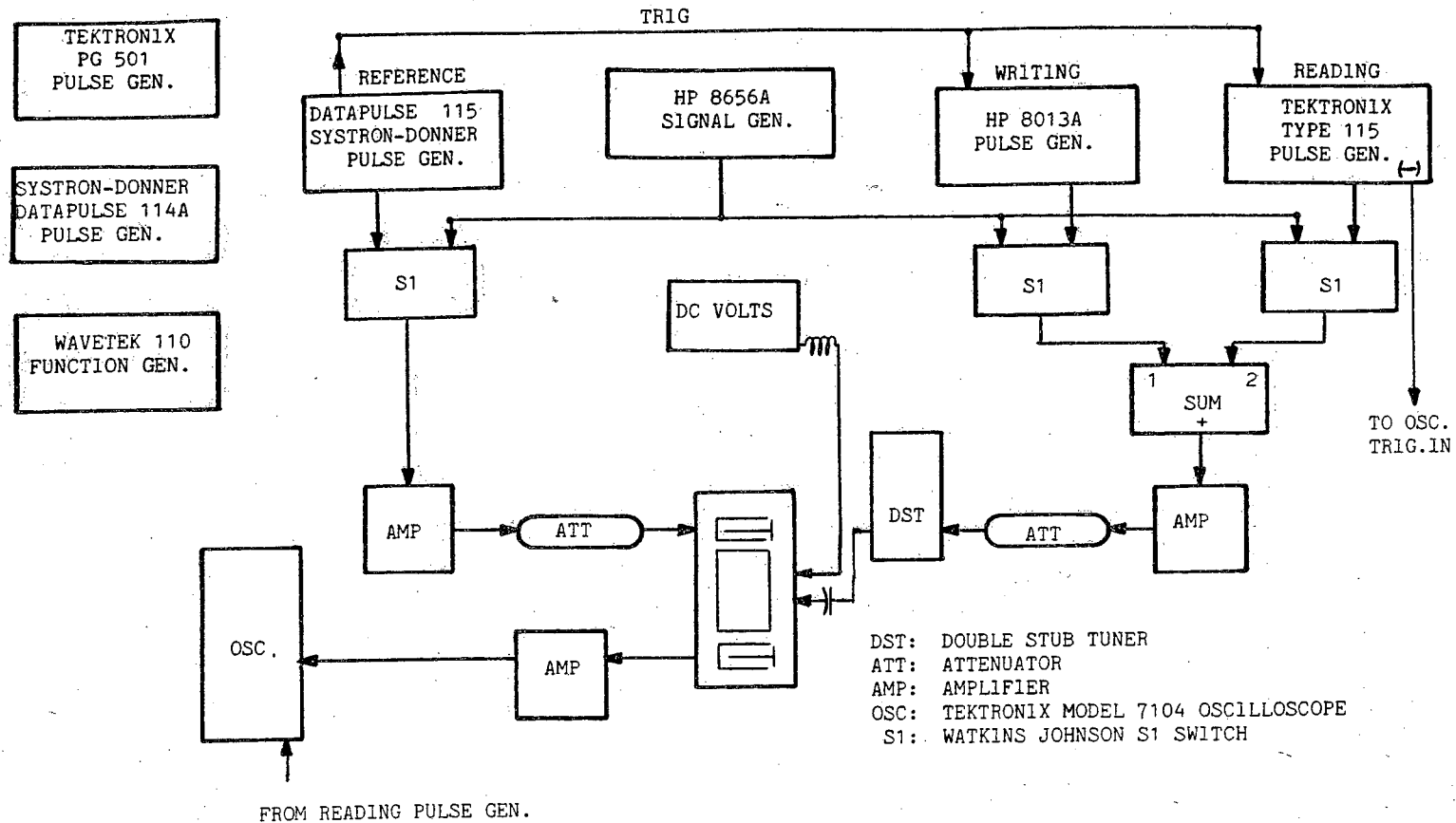
Figure B.2

Electronic setup for the storage correlation experiment.

with the negative output of the read pulse generator.

For the correlation versus number of writes experiment and the storage time experiment, we use the electronic setup shown in Fig. B.3. The Wavetek function generator serves only to govern the periodicity of each cycle. In both correlation output versus number of writes and storage time experiments, it is necessary for the stored signal to go away before taking another measurement (multiple cycles are necessary to obtain a photograph from the oscilloscope). As such, the Wavetek is used because it has a period adjustable to ~10 seconds.

The Datapulse 114A pulse generator sends a constant stream of trigger pulses to a solid-state switch. The Tektronix PG-501 pulse generator, however, allows only a select number of trigger pulses through the switch per cycle. The number of writes is controlled by the rate of the 114A and the pulse width of the PG-501. Each of these trigger pulses activates a write sequence. In this manner, the number of writes per cycle can be controlled very accurately.

To obtain a single readout, one "differentiates" the output of the PG-501 signal using a simple RC network, to detect the trailing edge of the pulse train. The trailing edge pulse then triggers the reading signal generator. In this setup, one can saturate the storage region with numerous writes and then, using the variable delay function of the read pulse generator, observe the correlation output with storage time.
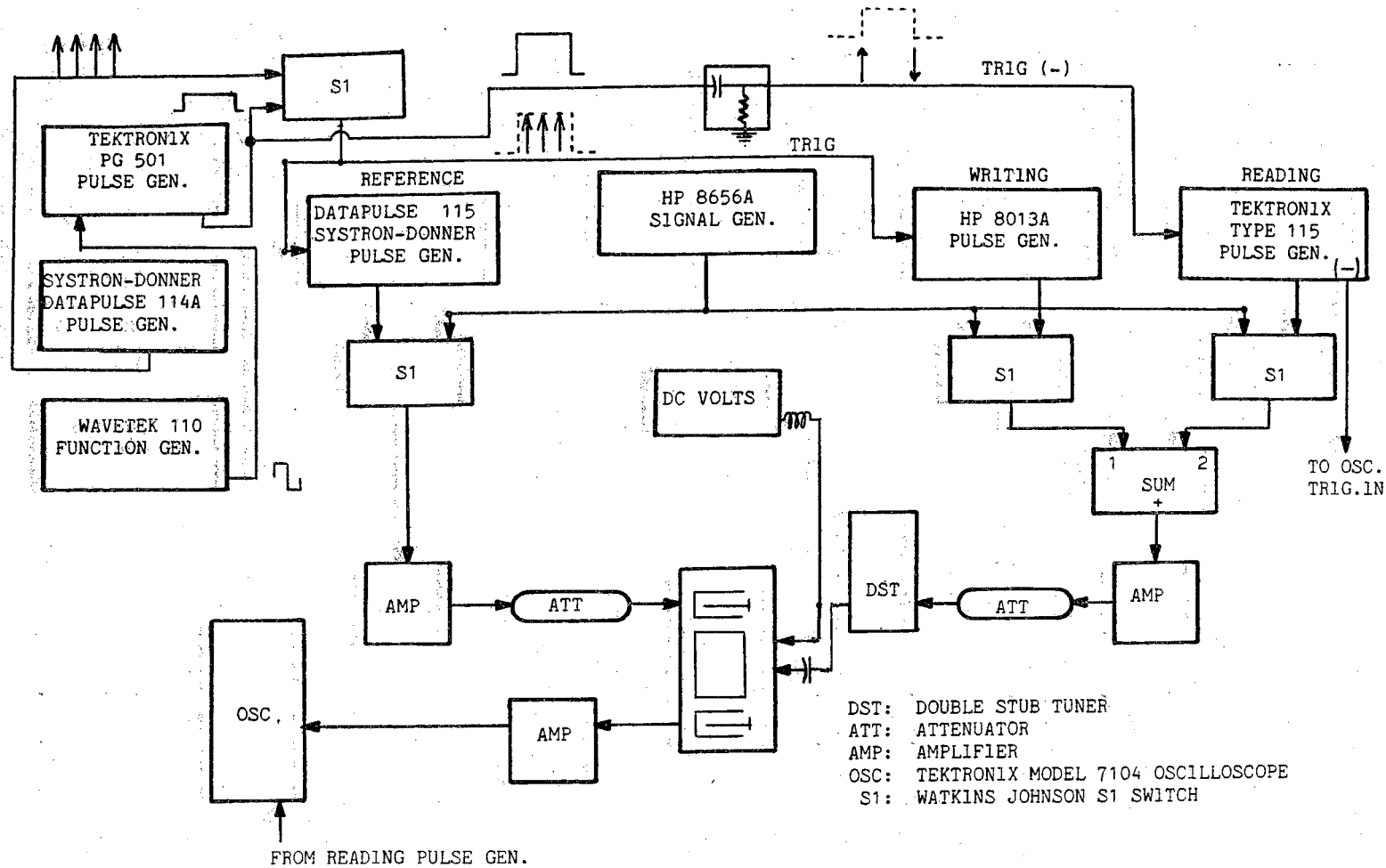
Figure B.3

Electronic setup for determination of correlation vs. number of writes.

DST: DOUBLE STUB TUNER
ATT: ATTENUATOR
AMP: AMPLIFIER
OSC: TEKTRONIX MODEL 7104 OSCILLOSCOPE
S1: WATKINS JOHNSON S1 SWITCH

Appendix C

Pulsed Semiconductor Potential Computation

Under equilibrium inversion bias V_G, one can determine the silicon surface potential from simple MOS device theory. The equilibrium surface potential is given by $V_{S_{eq}}$ where

$$V_{S_{eq}} = -\frac{2kT}{q}U_F \quad . \tag{C.1}$$

U_F is the doping parameter given in Eq. 3.13.

For an applied gate bias V_G one has a condition similar to that shown in Fig. C.1. The silicon is inverted and has a surface inversion layer charge density ρ_s given by Eq. 3.12 and, due to the injecting nature of the ZnO film, an equilibrium charge layer, ρ_o, at the ZnO/SiO$_2$ interface is given by

$$\rho_o = -\rho_s + 2\sqrt{-qN_D\epsilon_s\frac{kT}{q}U_F} \quad . \tag{C.2}$$

From the equilibrium inversion condition as a starting point, consider the application of a negative pulse of amplitude ΔV_G. A negative ΔV_G will instantaneously force the depletion region width to increase thereby deep depleting the semiconductor. We assume that the pulse duration is short compared to the generation lifetime in the depletion region and that no appreciable amount of electrons will be injected into the ZnO film. Thus, application of ΔV_G will not change ρ_s or ρ_o; only the charge on the gate and
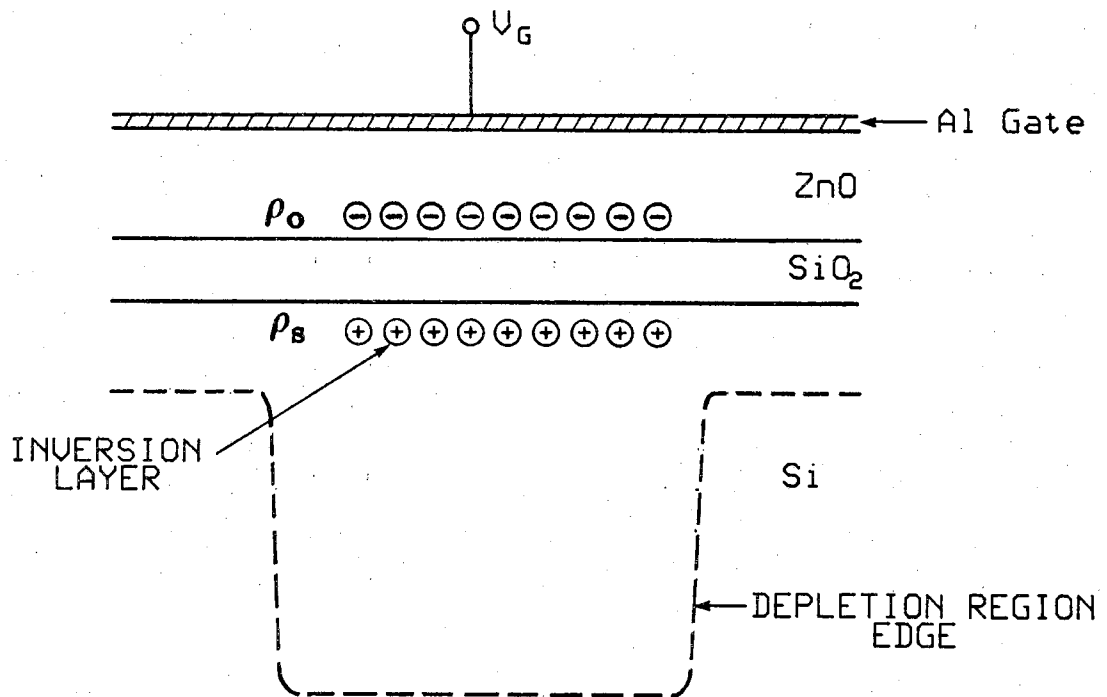
Figure C.1

Inversion condition in a single storage region.

the silicon depletion width will change.

To evaluate the effect of ΔV_G on silicon surface potential, one proceeds exactly as one would for the equilibrium condition by solving Poissons equation in the silicon.

$$\frac{dE'_s}{dx} = -\frac{qN_D}{\epsilon_s} \tag{C.3}$$

$$E'_s = -\frac{qN_D W'}{\epsilon_s} = -\frac{dV}{dx}$$

$$V'_{Si} = -\frac{qN_D}{2\epsilon_s} W'^{\,2} = V_{S_{eq}} + \Delta V_{Si} \quad , \tag{C.4}$$

giving

$$E'_s = \sqrt{-\frac{2qN_D}{\epsilon_s} V'_{Si}} \quad ,$$

where W' is the depletion region width.

We now solve the boundary equations to determine V'_{Si} in terms of $V_G + \Delta V_G$

$$D_{ox} - D'_s = \rho_s \tag{C.5}$$

$$E_{ox} = \left(\frac{\rho_s + \epsilon_s E_s}{\epsilon_{ox}} \right) \quad ,$$

similarly,

$$D'_z = \rho_o + D'_{ox} \tag{C.6}$$

$$E'_z = \left[\frac{\rho_s + \epsilon_{ox}E_{ox}}{\epsilon_z}\right] = \frac{1}{\epsilon_z}\left[\rho_o + \rho_s + \epsilon_s E'_s\right] \quad .$$

The expression for the total gate voltage is given by

$$V'_G = V_G + \Delta V_G = E'_z x_z + E'_{ox} x_{ox} + V'_{Si} \qquad (C.7)$$

Substituting Eq. C.4 and C.5 into Eq. C.6 one obtains

$$V'_G = \frac{x_z}{\epsilon_z}\rho_o + \left[\frac{x_z}{\epsilon_z} + \frac{x_{ox}}{\epsilon_{ox}}\right]\left[\rho_s + \epsilon_s E'_s\right] + V'_{Si} \quad . \qquad (C.8)$$

We note $C_z = \dfrac{\epsilon_z}{x_z}$ and $C_{ox} = \dfrac{\epsilon_{ox}}{x_{ox}}$ represent the per unit area capacitance of

the ZnO layer and SiO$_2$ layer respectively. Similarly, $\dfrac{1}{C_z} + \dfrac{1}{C_{ox}} = \dfrac{1}{C_I}$ where

C_I is the combined insulator capacitance. To obtain V'_G in terms of V_{Si} we

substitute the result of Eq. C.4 to give

$$V'_G = \frac{\rho_o}{C_z} + \frac{\rho_s}{C_I} + \frac{\epsilon_s}{C_I}\left[-\sqrt{\frac{2qN_D}{\epsilon_s}V'_{Si}}\right] + V'_{Si} \quad . \qquad (C.9)$$

Solving for V'_{Si} in terms of V_G one can write $\Delta V'_{Si}$ due to V'_G as

$$\Delta V'_{Si} = V'_{Si} - V_{S_{eq}} = V_d\left[1 + \left\{1 - \frac{\left[\dfrac{\rho_o}{C_z} + \dfrac{\rho_s}{C_I} - V_G - \Delta V_G\right]}{V_d}\right\}^{1/2}\right]^2 + \frac{2kT}{q}U_F \qquad (C.10)$$

where

$$V_d = -\frac{qN_D\epsilon_s}{2C_I^2} \quad .$$

It should be noted that the same procedure outlined above is what is used

in the computation of the surface charge density ρ_s. The calculation of ρ_s is

somewhat simpler, however, because the injecting ZnO layer makes $D_z = 0$.

Furthermore, as expected, $\Delta V'_{Si}$ becomes zero when $C_z \to \infty$ and $\Delta V_G = 0$.

Appendix D

Fabrication Procedures

D.1 Solvent Clean

1. Rinse in acetone (ACE)

2. Heat in ACE until boiling

3. Ultrasonic cleaner in ACE for 3 min.

4. Rinse in trichloroethane (TCA)

5. Heat in TCA until boiling

6. Ultrasonic cleaner in TCE for 3 min.

7. Rinse in ACE

8. Heat in ACE

9. Ultrasonic in ACE for 1 min.

10. Rinse in DI 15 times.

11. Blow dry with zero grade N_2.

D.2 Wafer Clean

For previously unoxidized silicon the cleanup procedure is as follows:

1. Solvent clean (step B.1)

2. Rinse 15 times in DI

3. Leave immersed in ~100 ml DI

4. Add HF acid so ratio of DI:HF is 10:1, agitate for 60 seconds *Do Not Pour Off!*

5. Flood with DI for 60 seconds

6. Rinse 15 times in DI

7. Pour off DI

8. 10 min. in 1:1, H_2O_2:H_2SO_4

9. Rinse 15 times in DI

10. Repeat steps 3 through 6

11. Pour off excess DI, **DO NOT BLOW DRY!**

D.3 Oxidation

1. 1000Å oxidation for correlator.

    900 °C H_2 burn oxidation, 42 min. for (100)-cut Si. TUBE #4.

2. 1.0 μm oxidation

    1100 °C H_2 burn oxidation, 2 1/2 hours for (111)-cut Si. TUBE #4.

3. 3.0 μm SiO_2*

---

* Performed at Fairchild Corp., Palo Alto, CA.

Pyrogenic steam oxidation under 20 atm pressure, 900 °C.

D.4 Cleanup for Recently Oxidized Silicon

1. Solvent Clean (step B.1)

2. Submerge in 1:1, H_2SO_4:H_2O_2 for 10 min.

3. Rinse 15 times in DI

4. Heat 5 min. in DI

5. Rinse in DI 15 times

6. Submerge in 1:1, H_2SO_4:HNO_3 for 10 min.

7. Rinse in DI 15 times

8. Heat 5 min. in DI

9. Rinse in DI 15 times

10. Blow dry using purified nitrogen.

D.5 Ion Beam Metal Deposition

1. Affix clean sample to stage of ion mill* using clips.

2. Rotate stage so samples are parallel to the target** (99.999% Al).

3. Pump chamber (rough to 100 mT, then cryopump) to low 10^{-6} torr pressure range.

4. Fire plasma.

---

* Millatron model, Commonwealth Scientific, Alexandria, VA.
** Cerac Inc., Milwaukee, WI.

Typical Run Parameters:

magnet current: 7.5 A

glow current: 1.5 A

extractor voltage: 300 V

extractor current: 2 mA

cathode current: 15 A

ion source current: 40 mA

ion source (accelerator) voltage: 1500 V

beam current: 15 mA

neutralizer current: 0

chamber pressure: 7.0×10^{-5} Torr

gun pressure: 5.0×10^{-4} Torr

6. Deposit 5 min. with samples covered by shutter.

7 Deposit Al to desired thickness (deposition rate ~ 5Å/mA min of beam current).

8. Stage is rotated throughout deposition for best uniformity.

D.6 Ion Beam Etching

The grooves etched in all resonator configurations are etched using an ion beam. Aluminum, photoresist, and stainless steel shields have all been used for etch masks.

1. Affix clean sample to the water-cooled stage using MUNG II* a heat sink compound.

---

* Commonwealth Scientific, Alexandria, VA.

2. Rotate stage so the argon beam impinges 5 ° from the surface normal.

3. Typical Run Parameters:

> magnet current: 5.0 A
>
> glow current: 1.5 A
>
> extractor voltage: 300 V
>
> cathode current: 15 A
>
> extractor current: 1 mA
>
> ion source current: 25 mA
>
> ion source (accelerator) voltage: 450 V
>
> beam current: 10 mA
>
> neutralizer current: 0
>
> chamber pressure: 9.5×10^{-5} Torr
>
> gun pressure: 5.0×10^{-4} Torr

4. Note that the accelerating voltage is kept below 500 V to avoid baking the photoresist onto the substrate.

D.7 Internally Coupled Limited ZnO Resonator Fabrication

1. Fabricate metal mask for ZnO deposition in IDT regions only.

2. Mount mask and wafer to special pallet using clips.

3. Etch grooves for ZnO using ion mill. Without breaking vacuum, deposit 1000Å Al. Place entire fixture into ZnO sputtering system*.

4. Sputter 0.7μm ZnO. Remove sample from pallet, proceed with resonator fabrication beginning with step #4.

---

* Perkin Elmer model 2400

D.8 Mounting

1. Affix sample to a glass plate using melted black wax. Spin photoresist on the sample and glass slide to protect the samples during dicing. Cut samples apart using a dicing saw**.

2. Remove photoresist by flooding with ACE.

3. Rinse thoroughly in DI.

4. Blow dry using purified nitrogen.

5. Heat glass plate containing samples on a hotplate to loosen individual devices. Place each device into its own teflon beaker.

6. Rinse in TCE.

7. Heat in TCE.

8. Ultrasonic in TCE for 1 min.

9. Solvent Clean (step B.1) (use only 1 min. for each ultrasonic cleaner step).

10. Mount in a flatpack# on an aluminum shiv to raise the device surface to the same level as the connecting leads.

11. Affix shiv to flatpack and device to shiv using silver epoxy##.

12. Bake flatpack and device 1 hour at 120 °C.

13. Ultrasonically bond** the device to the flatpack leads using 1 mil diameter aluminum wire.

** Model 602, Tempress, Los Gatos, CA.
\# Model IP-1065, Isotronics Inc., New Bedford, MD.
\#\# Ablebond 36-2,, Ablestik Laboratories, Gardena, CA.
** Model EMB 1100, Tempress, Los Gatos, CA.

D.9 ZnO Deposition

1. The sample is placed upon a 1/4 inch thick aluminum pallet which has been cleaned by etching in dilute HNO_3 (50:1, DI:HNO_3) and rinsed 20 times in DI. The pallet is sputtered upon for 10 minutes before placing the sample upon the pallet. The sample to be sputtered upon is placed such that the device propagation direction is along the growth rings to ensure constant ZnO thickness along a device. A twenty hour bakeout consists of 14 hours at 150 °C and 6 hours at 300 °C. Two 30 minute presputters are performed with 30 minutes between each before the shutter is opened and the actual sputter is performed. The deposition rate for rf diode sputtered films is typically 100Å/min.

Typical sputtering parameters are as follows:

Substrate temperature: 180 °C

Target: 6" diameter compressed ZnO powder, 6 - 9's purity.

Target-substrate spacing: 30 mm

Gas mixture: 80% Ar : 20% O_2 UHP

Chamber pressure: 10 mTorr

Bias voltage: 900 V

RF power: 100 W

D.10 Pattern Definition

1. Spin AZ 1450J photoresist* 3000 rpm (5000 rpm for correlator grating) for 30 sec.

---

* Shipley Co., Newton, MA.

2. Prebake 25 min. at 90 °C.

3. Expose photoresist in mask aligner[**].

4. Develop photoresist 3:1, AZ developer:DI until pattern develops (~20 sec.). (Develop 1:1, AZ developer:DI for 60 seconds for correlator grating).

5. Rinse 20 times in DI.

D.11 HMDS Treatment

1. Under a fume hood, pour 50 ml hexamethyldisilazane (HMDS) into a 100 ml beaker and place uncovered into a dessicator. *Be Careful!* HMDS is very hazardous.

2. Place oxidized sample into dessicator on filter paper and shield sample with a petri dish top, HMDS may boil when the dessicator is evacuated. Pump exhaust should not be inhaled.

3. Rough dessicator to ~150 mTorr, leave for 5 minutes.

4. Open dessicator under fume hood, remove sample, pump down dessicator.

D.12 SAW Resonator Fabrication

1. Wafer Oxidation

2. Aluminum Deposition

3. ZnO Sputter

4. Al Deposition

[**] Kasper Inst. Inc., Mountainview, CA.

5. Pattern Definition

6. Aluminum Etch

    Sample should remain wet after rinsing developer. Hold sample in tweezers and submerge into alkaline etch solution of:

    750 ml H_2O

    75 g $K_3Fe(CN)_6$

    7.5 g KOH

    For very thin aluminum ($< 500\text{Å}$), dilute etch 1:1 with DI.

7. Rinse in DI 20 times as soon as Al has been etched.

8. Remove photoresist by rinsing in ACE, heating in ACE, ultrasonic in ACE for 1 min. Repeat.

9. Rinse 15 times in DI.

10. Blow dry using zero grade N_2.

11. Define pattern for mask to cover IDT's during grating etch.

12. Etch grooves in ion mill.

13. Remove photoresist and MUNG II

    a. Rinse in ACE

    b. Boil in ACE ~ 10 min.

    c. Ultrasonic in ACE ~ 5 min.

    Repeat step 13 as necessary to completely remove photoresist and MUNG*.

---

* It may be necessary to change beakers due to MUNG II contamination.

14. Mask top surface again to cover IDT's only and repeat steps 6 through 10 to remove any remaining metallization.

15. Cut, clean, mount, bond, and test.

D.13 Externally Coupled Limited ZnO Resonator Fabrication

1. Replace Step #4 of resonator fabrication with

    a. Cover with photoresist and expose a pattern which leaves photoresist in transducer regions only.

    b. Etch away the exposed ZnO using a dilute (100:1, DI:HNO$_3$) nitric acid solution.

    c. Solvent Clean (step B.1).

    d. Evaporate 2000Å aluminum. Return to step #5 of resonator fabrication.

2. After step #11 insert the following:

    Boil in DI water for 10 minutes to form an Al$_2$O$_3$ layer on the grating aluminum. The purpose for the aluminum layer is that alumina etches at a rate approximately four times slower than aluminum,, silicon, and SiO$_2$ which all have comparable etch rates. This is important because deep grooves are necessary to obtain the same reflectivity for grooves etched in ZnO.

D.14 Implant-Isolated Storage Correlator Fabrication

1. Clean bare (100)-cut silicon for oxidation.

2. Grow 1000Å oxide.

3. Spin AZ 1450J photoresist onto top surface of silicon.

4. Strip back oxide using dilute HF acid and a cotton tip swab.

5. Rinse thoroughly in DI.

6. Solvent Clean (step B.1)

7. Perform phosphorus pdep. for back contact.

8. Cover back of sample with black wax and etch top SiO_2 as in step 4.

9. Rinse 15 times in DI.

10. Solvent clean (step B.1)

11. Define pattern from mask align.f (for alignment marks).

12. Etch alignment marks through photoresist in ion mill for 60 minutes.

13. Perform HMDS treatment prior to step 14.

14. Define photoresist pattern for correlator grating.

15. Ion implant phosphorus through photoresist pattern using

$$dose = 8.0 \times 10^{12}/cm^2$$

$$energy = 25 \ KeV$$

Total implant should take longer than 60 seconds for proper results.

16. Solvent clean (step B.1)

17. Perform wafer cleanup for unoxidized silicon. Use only 15 seconds for HF steps and 5 min for H_2O_2:H_2SO_4 step.

18. Grow 1000Å SiO_2.

19 From furnace tube, load the sputtering system immediately. Sputter 1.7 μm ZnO.

20. Deposit 1500Å Al using ion beam deposition.

21. Post metallization anneal, 5 min., 480 °C, N_2 with a 3 minute pull and push in the Marshall Furnace. This anneal is to reduce surface states present at the SiO_2/Si interface.

22. Fabricate test capacitors at this point if desired.

23. Strip Aluminum using phosphoric acid etch.

24. Rinse 20 times in DI.

25. Solvent Clean (step B.1)

26. 1:1, H_2SO_4:H_2O_2 for 10 minutes.

27. Rinse 15 times in DI.

28. Blow dry using purified nitrogen.

29. Ion beam deposit 1200Å aluminum.

30. Define shorting plane metallization in photoresist.

31. Etch aluminum using phosphoric acid etch.

32. Rinse 20 times in DI.

33. Solvent Clean (step B.1).

34. Sputter 1.7 μm ZnO in diode sputtering system.

35. Deposit 1500Å aluminum on ZnO in ion mill.

36. Cover top metallization using photoresist.

37. Strip any back oxide using dilute HF and a cotton tip swab.

38. Rinse 15 times in DI.

    Blow dry using purified nitrogen.

Deposit 2000Å aluminum onto back side of wafer.

39. Solvent clean (step B.1)

40. Define top metallization pattern in photoresist.

41. Cover back aluminum with black wax.

42. Etch top aluminum with alkaline etch for use with ZnO (see resonator fabrication step 6).

43. Clean, cut, bond, test.