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Performance and Reliability of Integrated Solar Thermal Electronics and Devices

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PERFORMANCE AND RELIABILITY OF INTEGRATED SOLAR THERMAL ELECTRONICS AND DEVICES

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Date

PERFORMANCE AND RELIABILITY OF INTEGRATED
SOLAR THERMAL ELECTRONICS AND DEVICES

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of

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This is the dedication.

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TABLE OF CONTENTS

	Page
LIST OF TABLES	vi
LIST OF FIGURES	vii
SYMBOLS	xii
ABBREVIATIONS	xiv
ABSTRACT	xv
1 HIGH TEMPERATURE SELECTIVE SOLAR ABSORBER BASED ON SI SUBSTRATE	1
1.1 Introduction	1
1.2 Methods	6
1.2.1 Structure of selective solar absorber based on Si substrate	6
1.2.2 Simulation of room and high temperatures	7
1.2.3 Fabrication of selective solar absorber	15
1.2.4 Characterization of selective solar absorber	17
1.3 Results and analysis	19
1.3.1 Room temperature emissivity	19
1.3.2 High temperature emissivity	20
1.3.3 Thin Si film selective absorber design and optimization	23
2 SELF-HEALING STRUCTURES TO REDUCE ELECTROMIGRATION FAILURES	30
2.1 Introduction to Electromigration	30
2.2 Method	35
2.2.1 Self-healing structure	35
2.2.2 Fabrication of test lines	36
2.2.3 Characterization: Thermal Reflectance Imaging System	39

	Page
2.3 Results and Analysis	42
2.3.1 Results for electrical polarity 1	42
2.3.2 Results of reverse polarity	52
3 CONCLUSIONS AND FUTURE WORK	59
3.1 High Temperature Selective Solar Absorber Based on Si Substrate .	59
3.2 Self-Healing Structures to Reduce Electromigration Failures	60
LIST OF REFERENCES	63
VITA	69

LIST OF TABLES

Table	Page
2.1 Parameters for different combinations of line width and void/reservoir radius.	35

LIST OF FIGURES

Figure	Page
1.1 The emissivity spectrum of an ideal selective solar absorber which absorbs most light below the cutoff wavelength while suppresses thermal emission of itself. Adopted from C.E. Kennedy [3].	2
1.2 (a) Optimal cutoff wavelength for an ideal selective solar absorber at various solar concentrations and operational temperatures. (b) Maximum thermal transfer efficiency of ideal selective absorber with optimal cutoff wavelengths for different concentration and temperature. Adopted from [4].	3
1.3 (a) schematics of semiconductor/metal selective absorber with bulk Si, Ag back reflector, and front AR coating. (b) Emissivity of selective absorber without front coating (red), with single layer AR coating (green), and with multilayer AR coating and back coating (blue). The thermal transfer efficiency is labeled near each curve. 82% Maximum efficiency is obtained for structures with 4 layer FC and 1 layer BC. The efficiency is calculated under 1000K, 1000 suns, and 1kW/m^2 standard solar intensity. Adopted from Bermel et al [1,4].	5
1.4 Schematic of the structure for selective absorber based on Si substrate. Si_3N_4 serves as front anti-reflection coating which is 215nm. Double side polished $300\mu\text{m}$ Si wafer is chosen to be the selective absorption layer. 300nm Ag is deposited on the back which reflects light back.	6
1.5 (a) reflectance and (b) emissivity for selective absorber with (black) and without (red) front Si_3N_4 anti-reflection coating. The thicknesses of Si_3N_4 , Si, and Ag are 215nm, $300\mu\text{m}$, and 300nm, respectively, in this simulation.	8
1.6 Dependency of the intrinsic free carrier density of Si on temperature.	10
1.7 Simulated absorption coefficient of Si at different temperatures (from 300°C to 800°C) from (a) our model and (b) Roozebooms results [34]. (c) comparison of experiment and simulation of absorption coefficient at different temperature. Adopted from Rogne et al [40].	12
1.8 The real part of the refractive index of Si at 20°C (blue line), 400°C (red line) and 800°C (yellow line).	13

Figure	Page
1.9 Comparison of simulation and experimental results. The sample structure is 1.77mm lightly doped Si. Experimental data is adopted from Sato [22].	14
1.10 Optical microscope pictures of the front surface of the fabricated selective absorber.	16
1.11 Schematic of the direct thermal emission spectrum measurement system. PM is off-axis parabolic mirror, D is the diameter of the mirror, EFL is the effective focus length and FTIR stands for Fourier Transform InfraRed spectrometer.	17
1.12 Measurement (solid lines) and simulation (dashed lines) of the emissivity of selective absorbers with (red lines) and without (black lines) front coating at the room temperature. The thicknesses of Si_3N_4 , Si and Ag are 215nm, $300\mu\text{m}$ and 300nm respectively.	20
1.13 Measurement (solid lines) and simulation (dashed lines) of the emissivity of the selective absorber: (a) without and (b) with a Si_3N_4 AR coating at different high temperatures. The thicknesses of Si_3N_4 , Si and Ag are 215nm, $300\mu\text{m}$ and 300nm, respectively. High spectral selectivity is observed at 473°C in structure with AR coating, with a cutoff wavelength of approximately $1.3\mu\text{m}$	21
1.14 Room temperature emissivity of the selective absorber with Si_3N_4 AR coating after (black line) and before (red line) the high temperature thermal emission measurement.	22
1.15 (a) Emissivity for selective absorbers with different Si thicknesses. Si_3N_4 thickness is 215nm, and the temperature is targeted at 550°C . (b) dependency of efficiency (black line), average absorptance (blue line) and average emittance (red line) on Si thickness. The efficiency is calculated at 100 suns concentrations.	24
1.16 (a) Efficiency for $20\mu\text{m}$ thick Si thin film selective absorber with different Si_3N_4 thickness ranging from 0 to 300nm. The efficiency is calculated under 100 suns and 1000W input solar intensity. (b) Emissivity for selective absorbers with different Si_3N_4 thicknesses. The thicknesses of Si and Ag are $20\mu\text{m}$ and 300nm respectively. The temperature is set at 550°C . . .	25
1.17 Dependence of efficiency on Si_3N_4 thickness for different Si thicknesses under (a) 100 suns, (b) 50 suns, (c) 20 suns and (d) 10 suns. The operating temperature is fixed at 550°C	26

Figure	Page
1.18 Emissivity spectrum for selective absorbers with different Si thicknesses. The thickness of Si_3N_4 is the optimal value, 80 nm. The temperature is set at 550 °C. The F-P interference at Mid-IR is smoothed out for more clear comparison.	27
1.19 Dependency of efficiency on the concentration for different Si thickness. The Si_3N_4 thickness is fixed at 80nm, and the temperature is 550 °C. .	28
1.20 Two dimensional map of the thermal transfer efficiency for different Si thickness under different concentration. Si_3N_4 thickness is fixed at 80nm, Ag is 300nm thick. The targeted temperature is 550 °C.	29
2.1 (a) Schematic of the principle of electromigration. (b) Three major mechanisms of electromigration: (a) grain boundary, (b) bulk diffusion, and (c) surface diffusion. Adopted from Lienig, Jens [47].	31
2.2 Typical voids and hillocks formed by electromigration. Adopted from Lienig, Jens [47].	31
2.3 Typical test results of electromigration. (a) changes of the conductance (red curve) and current (green curve) with gradually increasing voltage. (b) SEM images of the test device before and after the electromigration (EM). A 6nm gap is formed near the cathode pad after the test. Results are adopted from Teresa Esposito, Kim Lewis [54].	32
2.4 Typical results of the distribution of the failure time of many similar devices under electromigration test. The median number of the failure time is found and defined as the lifetime of the device.	33
2.5 Schematics of designed test structures with or without void and/or reservoir.	36
2.6 The designed mask patterns for the fabrication of the devices. (a) Typical serpentine resistor pattern with 5 μm line width. The size of each part is labeled in the figure. (b) Devices with different combinations of width (5, 8 and 10 μm) and radius. The size of black square is around 400 μm ×400 μm for better thermal reflectance imaging.	37
2.7 The work flow for the fabrication of test devices using lift-off process. Typical cross-section of the devices is plotted beside each important fabrication step.	38
2.8 Finished devices at various magnifications, as imaged via optical microscope.	39
2.9 Measured thickness of three different devices using Profilometer (P-7). The resolution of P-7 is within 5nm.	40

Figure	Page
2.10 (a) Schematic of the principle of thermal reflectance imaging (TRI). Input is electrical square wave signal, the temperature and reflectance of the device is changed according to the electrical signal. Images at high and low temperature is taken and made a difference. The differential image shows changes and distribution of the temperature. The inset shows the user interface of the TRI system software. (b) Schematic of thermal reflectance imaging system. A LED light is used to illuminate the device, and a CCD is used to detect the reflected light from the device. A computer synchronizes the triggering of electrical signal and detection of reflection. The current and voltage of the devices the monitored by the oscilloscope using four probe measurement.	41
2.11 Schematic of electrical square wave form applied in the TRI measurement.	42
2.12 (a) Temperature distribution (image No.34) over the whole serpentine test line with structure '5 2 2'. The plus and minus sign in the figure indicates the polarity of the voltage, and the arrow shows the current direction. (b) Change of current (black line) and resistance (blue line) with voltage. .	43
2.13 Changes of temperature distribution over time (from image 34 to 39) near the void (left) and pad (right)	44
2.14 Pictures with high magnification (100×) of void and pad after the test taken by optical microscope. Some little voids are formed near the void, and possible hillock formed at the pad.	45
2.15 Changes of temperature at six different areas around the void with time. The temperature is the average temperature over the selected boxes which are shown in the left. The increasing of image number corresponds to the increasing of time, and each image takes 10 minutes.	46
2.16 Changes of temperature at four different areas around the pad with time. The temperature is the average temperature over the selected boxes which are shown in the left. The increasing of image number corresponds to the increasing of time, and each image takes 10 minutes.	47
2.17 Change of (a) the current and (b) the temperature of void (black line) and pad (red line) with time	47
2.18 Changes of the temperature for the void (black dots) and pad (red dots) with the power I^2R . The dashed lines in the figure are added for guidance only.	48

Figure	Page
2.19 (a) Changes of temperature (black line) and resistance (red line) with time. (b) The dependency of resistance on the temperature. The black dashed line shows the slope of the increasing of resistance due to the temperature with temperature coefficient 0.00429 per °C. The temperature is the averaged temperature of void Box6 which is nearly the average temperature of the whole device.	49
2.20 The change of temperature distribution along a line near the void for images (a) 22 - 24 and (b) 35 - 39. The cross section is shown at the top for reference.	50
2.21 The change of temperature distribution along a line near the pad for images 35 - 39. The cross section is shown at the top for reference.	51
2.22 (a) Temperature distribution (image No.31) over the whole serpentine test line with structure '5 2 2'. The plus and minus sign in the figure indicates the polarity of the voltage, and the arrow shows the current direction. (b) Change of current (black line) and resistance (blue line) with voltage.	52
2.23 Changes of the temperature distribution over time (from image 28 to 32) near the void	53
2.24 Pictures with low (10×) and high (100×) magnification of the whole device (upper part) and the void (lower part) after the test. Taken by optical microscope. The red rectangle shows the zoom-in area of the high magnification near the void. The arrow shows the moving direction of electrons.	54
2.25 Changes of averaged temperature at three different areas around the void with time. The temperature is averaged over the selected boxes which are shown in the left. The increasing of image number corresponds to the increasing of time, and each image takes 10 minutes.	55
2.26 (a) Change of the current with time. (b) Dependency of the temperature for three areas around the void on the power I^2R . The dashed lines in the figure are added for the guidance of the linearity. The data points are all after image 23.	56
2.27 Resistance versus temperature. The red dashed line shows the slope of this relationship predicted by literature: a temperature coefficient of 0.00429 per °C. The black dashed line is added to guide the eye. The temperature is the averaged temperature of void Box3, which is nearly the average temperature of the whole device. The data points are all taken after image 23.	57
2.28 The change of temperature distribution along a line near the void for images 28 - 32. The cross section is shown at the top for reference.	58

SYMBOLS

ϵ	emissivity
α_A	absorptivity
ρ	reflectivity
λ	wavelength of light
n	real part of refractive index
k	imaginary part of refractive index
h	Planck constant
ν	frequency of photon
T	temperature
α	absorption coefficient
α_{BG}	sub-bandgap absorption
α_{FC}	free carrier absorption
α_L	lattice absorption
k_B	Boltzmann constant
n_i	intrinsic free carrier density
η_t	solar thermal transfer efficiency
$\bar{\alpha}$	spectrally averaged absorptivity
$\bar{\epsilon}$	spectrally averaged emissivity
σ	Stefan-Boltzmann constant
C	solar concentration ratio
I	solar intensity
c	light speed in vacuum
$FTIR$	measured FTIR signal
$R(\lambda)$	response function of FTIR

$P(\lambda, T)$	Planck's blackbody function at temperature T
$B(\lambda, T)$	background of FTIR measurement at heater temperature T
A	geometry-dependent constant
$R(\lambda)$	response function of FTIR
J	current density
E_a	activation energy
W	width of test line
r	radius of void/reservoir
t	time
R	resistance of test line

ABBREVIATIONS

CSP	concentrating solar power
TPV	thermophotovoltaic
ARC	anti-reflection coating
S4	Stanford Stratified Structure Solver
IR	infrared
ARC	anti-reflection coating
FTIR	Fourier Transform Infrared
PM	off-axis parabolic mirror
EFL	effective focus length
EM	electromigration
IC	integrated circuits
SEM	scanning electron microscopy
MTTF	median time to failure
TRI	thermoreflectance imaging
UV	ultra-violet

ABSTRACT

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The performance and reliability of solar thermal electrical device is studied. As the key part of solar thermal transfer device, a semiconductor-metal tandem selective solar absorber based on commercially available Si wafer is fabricated and measured at high temperatures. High selectivity of the devices is obtained at temperature as high as 473°C , and the structure is demonstrated to be mechanically and thermally stable at elevated temperature (up to 500°C). Increased free carrier absorption and lattice absorption of Si is observed at high temperatures, which rises thermal reradiation dramatically. To mitigate this effect, thin Si film-based selective absorber is designed and optimized which shows high thermal transfer efficiency (60-70%) over a wide range of solar concentration (20-100 suns). The simple structure combined with the mechanical and thermal stability enables the low-cost Si substrate-based selective solar absorber to find wide applications in solar thermal energy conversion system. One of the main causes of the electronic device failure, electromigration, is investigated experimentally aiming at elongating the lifetime of the integrated circuit. A novel self-healing structure is proposed, and the test device is fabricated by lift-off process and characterized using thermal reflectance imaging technique. Failure due to electromigration is observed in the experiment, and the introduction of reservoirs is expected to realize a self-healing of the interconnect, which will lead to more reliable and long-lifetime electronic system.

1. HIGH TEMPERATURE SELECTIVE SOLAR ABSORBER BASED ON SI SUBSTRATE

1.1 Introduction

The efficiency of power conversion from solar to some other usable form of energy is a key factor in the economic feasibility of processes that harvest solar energy. While technologies like photovoltaics and solar thermal can be used to achieve power conversion, both have their respective theoretical and practical performance limits. These limits are due to losses inherent to converting across a broad range of the electromagnetic spectrum. However, it is important to observe that these limits do not have the same origin or fundamental form. For medium- to high-energy photons, particularly below 1 eV, it can in fact be most effective to use thermal conversion, especially if one is confined to a single photovoltaic bandgap. However, for low-energy photons, it is best not to absorb them at all, to help suppress infrared reradiation. A selective solar absorber allows one to cleanly discriminate between these wavelength ranges.

Solar thermal energy conversion has been widely studied and played important role in many applications, such as solar thermophotovoltaic (TPV) systems [1, 2] and concentrating solar power (CSP) systems [3]. Efficient thermal conversion of sunlight requires high solar absorptance and low reradiation at a certain operational temperature. This requirement can be fulfilled by a selective solar absorber, which absorbs most sunlight below a cutoff wavelength, along with low emissivity above the cutoff, as illustrated in Fig. 1.1. The selectivity helps the absorber utilize most useful solar energy with low thermal energy losses to reradiation. An ideal selective solar absorber absorbs most sunlight below a cutoff wavelength, while also exhibiting

low emissivity above the cutoff. This design will have high efficiency in converting sunlight into usable heat, even when operating at high temperatures.

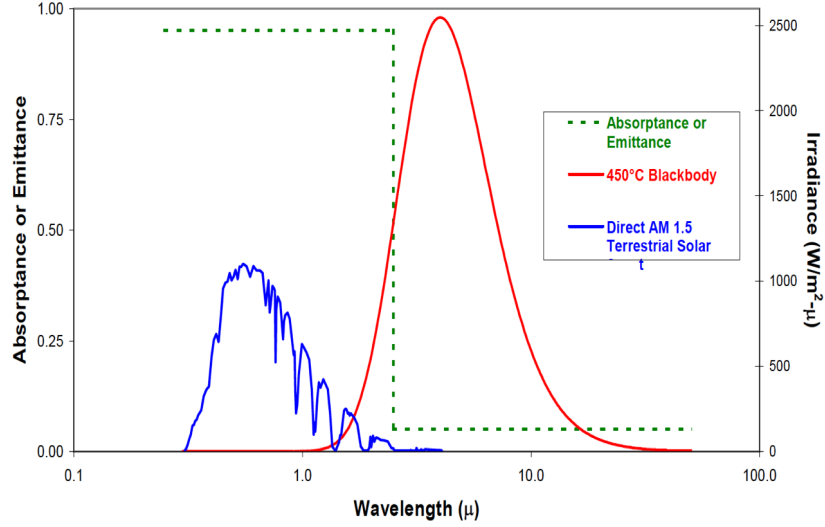


Fig. 1.1. The emissivity spectrum of an ideal selective solar absorber which absorbs most light below the cutoff wavelength while suppresses thermal emission of itself. Adopted from C.E. Kennedy [3].

According to Planck's law of blackbody radiation, the peak wavelength of a blackbody spectrum increases inversely with temperature. Therefore, the large difference between the solar surface temperature (around 5500°C) and much lower practical operational temperature of most solar thermal system allows a wide design space for the cutoff wavelength. Depending on the exact system temperature and solar concentration, the optimal cutoff may vary for different situations [4]. To determine the best cutoff wavelength, a thorough study has been conducted by prior researchers [4], as shown in Fig. 1.2(a). For higher concentration and lower temperature, the optimal cutoff increases gradually to around $3.5\mu\text{m}$. In contrast, the opposite conditions lead to shorter cutoff wavelength. This is because for higher concentration, the thermal emission becomes less important, and the longer the cutoff, the more sunlight the selective absorber will absorb. Also, for high temperature, the peak of thermal re-radiation shifts towards shorter wavelength which shifts the cutoff wavelength in

the same direction. According to Fig. 1.2 (b), the efficiency is at its maximum for high concentrations and low temperatures. However, as demonstrated by the Carnot theorem, the overall efficiency limit of a heat engine generally increases with higher operational temperature [4]. In this sense, there is a trade-off between solar thermal transfer efficiency and heat utilization efficiency, and thus a finite optimal temperature will exist for a given set of circumstances. Thus, in practical device designs, operating temperature should be optimized to obtain maximum overall system efficiency.

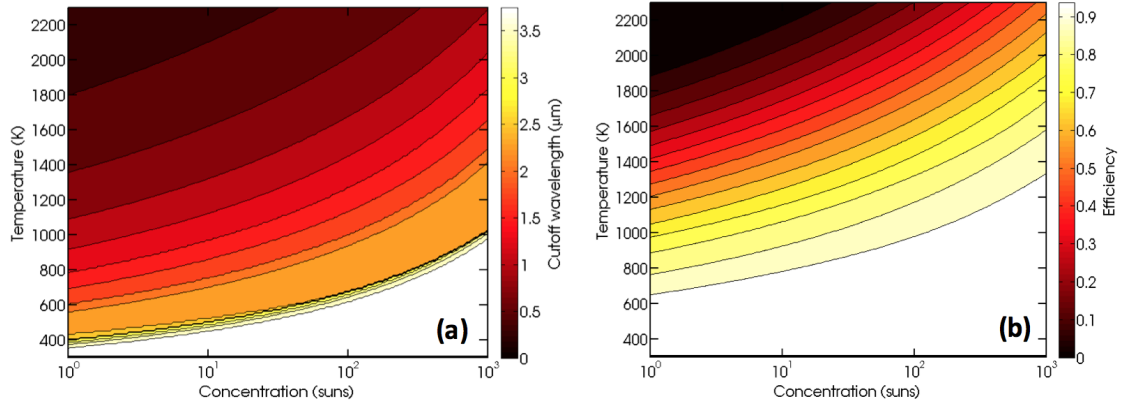


Fig. 1.2. (a) Optimal cutoff wavelength for an ideal selective solar absorber at various solar concentrations and operational temperatures. (b) Maximum thermal transfer efficiency of ideal selective absorber with optimal cutoff wavelengths for different concentration and temperature. Adopted from [4].

For a practical selective solar absorber, apart from high selectivity, mechanical and thermal stability are often required for many applications, such as solar TPV system which operates at high temperatures ($T \geq 500^\circ\text{C}$) for high overall energy conversion efficiencies [5]. In this sense, a design and optimization of the selective solar absorber that properly accounts for these additional factors is critical in improving the performance of experimentally-relevant solar thermal conversion systems.

Many structures have been proposed and studied for selective solar absorbers, such as metal-dielectric composite coatings [6], semiconductor-metal tandems [7–9], metamaterial surfaces [10–12], and metallic photonic crystals [13–18]. Among them,

the semiconductor-metal tandem selective solar absorber has been demonstrated to possess high thermal transfer efficiency both in simulation [1] and in experiment [7,9]. Since semiconductor materials absorb most photons with energies above the bandgap and are transparent to those below the bandgap energy, they naturally possess strong spectral selectivity. Depending on the practical requirements, a wide variety of semiconductor materials have accordingly been utilized for selective solar absorbers, such as silicon (Si) [9], germanium (Ge) [19], and lead sulfide (PbS) [20]. According to Kirchoff's law, the emissivity ϵ equals absorptivity α_A in thermodynamic equilibrium, which can be expressed by reflectivity for opaque objects; that is, $\epsilon(\lambda) = \alpha_A(\lambda) = 1 - \rho(\lambda)$ [3]. By placing a metal as the back reflector, long wavelength light passing through the semiconductor will be reflected back by the metal layer, which reduces thermal emission [21]. Since most semiconductor materials have a high refractive index, a front anti-reflection (AR) coating is needed for efficient absorption of sunlight. Compared with other selective solar absorber structures, the semiconductor-metal tandem is both low-cost, easy to fabricate, and mechanically stable, which could facilitate its wide application and adoption.

In recent work, Bermel *et al.* [1] have performed a thorough numerical study of selective absorbers made from semiconductor-metal tandems. As shown in Fig. 1.3(a), bulk crystalline Si is used to selectively absorb sunlight, silver is used as the back reflector, and front AR coating (single layer and multi-layer) is optimized globally. It is seen clearly from Fig. 1.3(b) that there is a sharp cutoff around $2.3\mu m$ for all structures. The addition of a single-layer AR coating increases the efficiency from 56% to 71%, while the further optimized 4-layer AR coating gives 82% solar thermal transfer efficiency. These results are sufficient to justify a follow-up investigation with an experimental component.

In this work, a semiconductor-metal tandem selective solar absorber based on commercially available and inexpensive Si wafer is fabricated and characterized at a range of high temperatures. The structure is shown in Fig. 1.4, which includes both a Si_3N_4 AR coating (215 nm) and a Ag back reflector (300 nm). High selectivity of

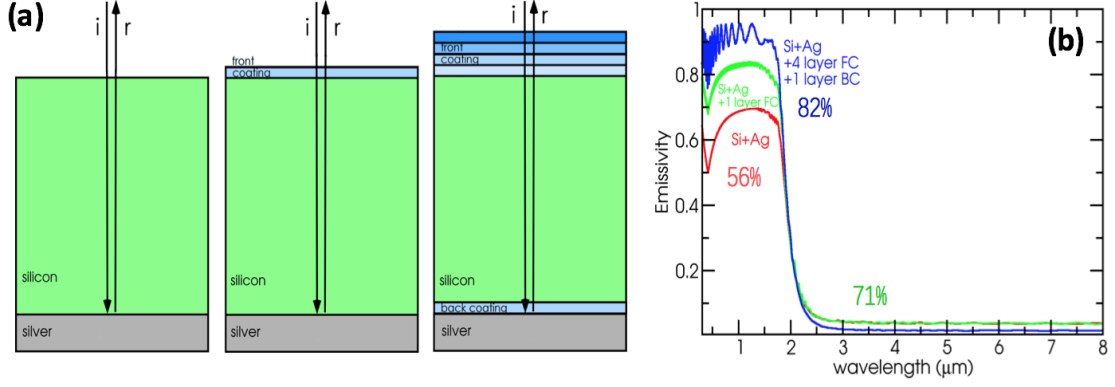


Fig. 1.3. (a) schematics of semiconductor/metal selective absorber with bulk Si, Ag back reflector, and front AR coating. (b) Emissivity of selective absorber without front coating (red), with single layer AR coating (green), and with multilayer AR coating and back coating (blue). The thermal transfer efficiency is labeled near each curve. 82% Maximum efficiency is obtained for structures with 4 layer FC and 1 layer BC. The efficiency is calculated under 1000K, 1000 suns, and $1\text{kW}/\text{m}^2$ standard solar intensity. Adopted from Bermel et al [1, 4].

the devices is observed at temperature as high as 473°C . Additionally, the structure is demonstrated to be thermally stable at elevated temperatures (up to 500°C). However, due to the increased free carrier absorption of Si [22] at high temperature, thermal re-radiation rises dramatically, which limits the maximum temperature the selective solar absorber can operate at. To mitigate this effect, thin Si film-based selective absorbers are designed and optimized, which show the high thermal transfer efficiency at a wide range of low solar concentration. Additionally, as demonstrated by Yi Cui *et al.* [23], thin Si film substrates exhibit excellent mechanical stability and flexibility, which could further improve the feasibility and practicability of a selective solar absorber based on thin Si film substrates.

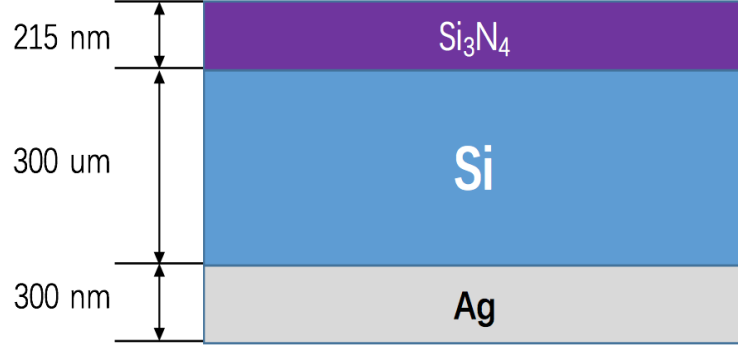


Fig. 1.4. Schematic of the structure for selective absorber based on Si substrate. Si_3N_4 serves as front anti-reflection coating which is 215nm. Double side polished $300\mu\text{m}$ Si wafer is chosen to be the selective absorption layer. 300nm Ag is deposited on the back which reflects light back.

1.2 Methods

1.2.1 Structure of selective solar absorber based on Si substrate

The structure of the selective absorber is illustrated in Fig. 1.4. The selectivity of this structure is primarily provided by Si, which absorbs photons with energies above the bandgap, and relatively few photons with energies below the bandgap. Since the bandgap of Si matches the middle of the solar spectrum, it has been previously demonstrated to serve as a good selective absorber material [7,9]. Photons that are not absorbed by the Si are reflected back by Ag effectively. According to Kirchhoff's law, this reduces the reradiation of light that are below the Si bandgap, which suppresses total emission of Si at high temperature.

To increase the absorption of desirable higher energy photons in the solar spectrum, an anti-reflection front coating is needed, since the refractive index difference is large for Si and air, which makes it fairly reflective. Previous researchers have successfully optimized the front coating for selective absorber [1]. Based on their work, 215 nm Si_3N_4 is used as front coating, for a transmission peak around 550 nm.

1.2.2 Simulation of room and high temperatures

We establish a model based on the Stanford Stratified Structure Solver (S4) [24, 25] that can simulate the reflection of our designed selective absorber at both room temperature and high temperatures. The model must capture the material properties, particularly the real and imaginary parts of the refractive index, n and k , respectively. This model should be accurate across this entire temperature range to achieve the best match with experiment. As for Si_3N_4 , its n and k spectra are obtained directly from previous experimental work done by Kischkat *et al.* [26]. Since Si_3N_4 is very thin, has a large bandgap, and there is little extant data available for Si_3N_4 at high temperatures, we assume its optical property remains unchanged at within our temperature range. In the same way, the complex refractive index of Ag refers to the study of Rakić *et al.* [27] and is assumed to be independent of temperature. This is probably a less accurate assumption, but is less critical at high temperatures, as will be demonstrated below.

Since Si is relatively thick and has been demonstrated to have strong temperature dependence [22, 28, 29], we have to pay particular attention to the modeling of Si. At room temperature, much experimental study has been done on Si [30, 31]. Here, we combine work from Green and Keevers [32], Salzberg and Villa [33] and Bermel *et al.* [1]. Based on this data, the reflection of the designed selective absorber has been simulated, as illustrated in Fig. 1.5(a). According to Kirchhoff's law, the emissivity of the selective absorber is calculated and shown in Fig. 1.5(b).

From the simulation results, it can be seen that there is a sharp cutoff of emissivity around $1.1\mu\text{m}$, which is the bandgap of Si at room temperature. This cutoff makes the selective absorber effectively absorb a great deal of sunlight, while simultaneously suppressing re-emission of light below the cutoff energy, which has the potential to result in a relatively high solar thermal transfer efficiency. Also, it shows that the front coating increases the absorption of light around 550nm to nearly 100%, right at the peak of solar spectrum. This enables the selective absorber to have relatively high

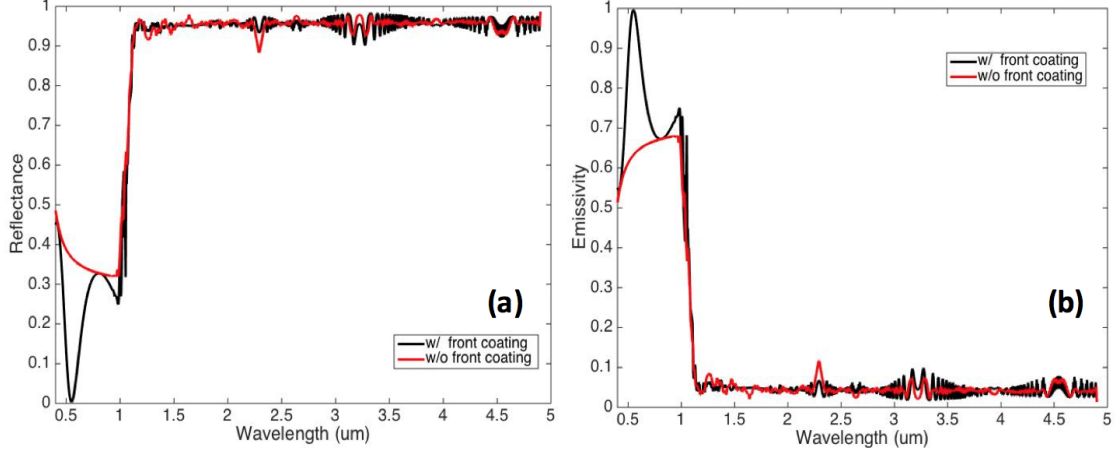


Fig. 1.5. (a) reflectance and (b) emissivity for selective absorber with (black) and without (red) front Si_3N_4 anti-reflection coating. The thicknesses of Si_3N_4 , Si, and Ag are 215nm, $300\mu\text{m}$, and 300nm, respectively, in this simulation.

absorptance of sunlight. In addition, the fluctuation of the reflection or emissivity at infrared is due to the Fabry-Pérot cavity formed by the front and back surface of the double side polished Si substrate. However, this phenomenon will not be observed in practical measurements, because of the finite spectral resolution of our measurement setup.

In terms of the optical properties of Si at high temperatures, we refer to the thorough review of silicon's complex refractive index at different high temperatures performed by Roozeboom [34], which gives semi-empirical equations for calculation. Jellison and Modine [35] also performed extensive study on optical property of Si between $0.4 - 0.84\mu\text{m}$ and $25 - 490^\circ\text{C}$. They found an empirical equation for the imaginary part of the refractive index k that can fit well with the experimental results for this range, given by:

$$k(h\nu) = k_0(h\nu)\exp(T/T_0(h\nu)), \quad (1.1)$$

where:

$$k_0(h\nu) = -0.0805 + \exp[-3.1893 + 7.946/(E_g^2 - (h\nu)^2)], \text{ and} \quad (1.2)$$

$$T_0(hv) = 369.9 - \exp(-12.92 + 5.509hv) \quad (1.3)$$

In these equations, h is Planck's constant, $E_g = 3.648$ eV, T is in $^{\circ}\text{C}$ and energy is in unit of eV. Experimental results also demonstrate the validity of the empirical equations up to 700°C [34].

As for longer wavelengths, such as the mid-infrared, the absorption of Si mainly contains three parts corresponding to three different mechanisms, namely: interband absorption, free carrier absorption and lattice absorption, which can be captured as a linear sum of absorptivities, given by [34, 36]:

$$\alpha = \alpha_{BG} + \alpha_{FC} + \alpha_L. \quad (1.4)$$

Here, α is the absorption coefficient of Si which correlates with k accordingly to $k = \alpha\lambda/4\pi$ [36]. The interband absorption dominates at shorter wavelengths, which is related with the sub-bandgap phonon-assisted absorption of Si. Macfarlane *et al.* [37] gives a thorough study, and establishes an empirical model to describe the band edge absorption of Si [37]. They associate absorption with the emission and absorption of four different phonons, which can be written as:

$$\alpha_{BG}(hv, T) = \sum_{i=1}^4 [\alpha_{ia}(hv, T) + \alpha_{ie}(hv, T)], \quad (1.5)$$

where:

$$\alpha_{ia}(hv, T) = \frac{F_i(hv - E_g(T) + k_B\theta_i)}{hv[\exp(\theta_i/T) - 1]}, \text{ and} \quad (1.6)$$

$$\alpha_{ie}(hv, T) = \frac{F_i(hv - E_g(T) - k_B\theta_i)}{hv[1 - \exp(\theta_i/T)]}, \quad (1.7)$$

which corresponds to the absorption and emission of phonons, respectively. In these equations, $\theta_1 = 212\text{K}$, $\theta_2 = 670\text{K}$, $\theta_3 = 1050\text{K}$, $\theta_4 = 1420\text{K}$, k_B is Boltzmann's constant, T is in K, energy is in eV, and function F_i in $\text{eV} \cdot \text{cm}^{-1}$. The bandgap E_g and F_i functions are expressed explicitly as:

$$E_g(T) = 1.155 - 4.73 \times 10^{-4}T^2/(635 + T),, \text{ and} \quad (1.8)$$

$$F_1(x) = \begin{cases} 0.504\sqrt{x} + 392(x - 0.0055)^2 & x \geq 0.0055 \\ 0.504\sqrt{x} & 0 \leq x \leq 0.0055 \\ 0 & x \leq 0 \end{cases} \quad (1.9)$$

$$F_2(x) = \begin{cases} 18.08\sqrt{x} + 5760(x - 0.0055)^2 & x \geq 0.0055 \\ 18.08\sqrt{x} & 0 \leq x \leq 0.0055 \\ 0 & x \leq 0 \end{cases} \quad (1.10)$$

$$F_3(x) = \begin{cases} 536x^2 & x \geq 0 \\ 0 & x \leq 0 \end{cases} \quad \alpha_{3a} \text{ only, and} \quad (1.11)$$

$$F_4(x) = \begin{cases} 988x^2 & x \geq 0 \\ 0 & x \leq 0 \end{cases} \quad \alpha_{4a} \text{ only} \quad (1.12)$$

Based on these empirical equations, we can calculate the α_{BG} and thus the imaginary refractive index k of Si at different temperatures.

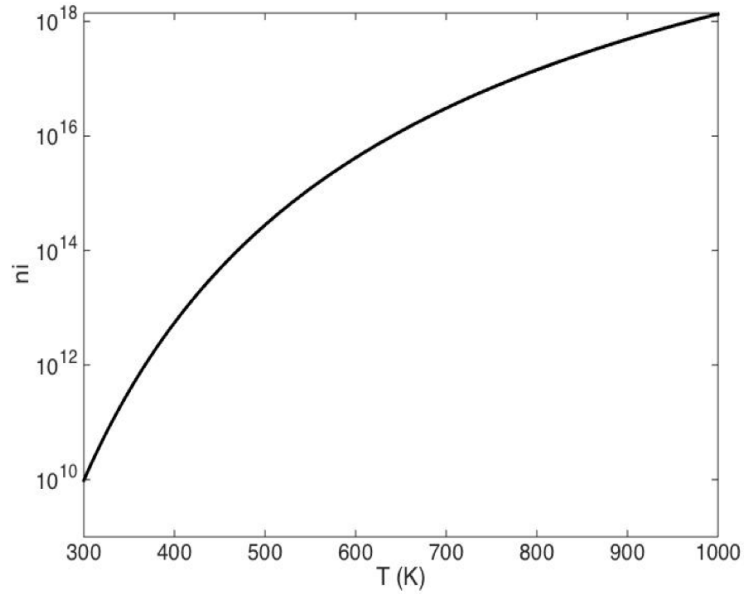


Fig. 1.6. Dependency of the intrinsic free carrier density of Si on temperature.

Since the intrinsic free carrier density n_i of Si increases exponentially with temperature, as shown in Fig. 1.6, when $T \geq 500$ K, n_i is even larger than the extrinsic

doping of a commercial lightly-doped Si wafer. As temperature increases further, Si enters the intrinsic region, and sees its density of free carriers increase by orders of magnitude. This effect in turn increases the free carrier absorption dramatically with temperature, as has been demonstrated by Sato [22].

In order to calculate the free carrier absorption coefficient, Vandenabeele and Maex [38, 39] have measured the emissivity of Si at 1.7 - 3.4 μm at different temperatures, and developed an empirical equation that fits well with experimental data, given by:

$$\alpha_{FC} = 4.15 \times 10^{-5} \lambda^{1.51} T^{2.95} \exp(-7000/T), \quad (1.13)$$

where T is the temperature in K, λ is in μm and α_{FC} is in cm^{-1} . Experiments performed by Rogne *et al.* demonstrated the validity of the above equation from 1 - 9 μm up to 800 $^{\circ}\text{C}$ [40], as shown in Fig. 1.7(c). Since free carrier absorption at high temperature increases the emissivity of Si in the infrared, it also increases thermal re-radiation, thus degrading the selectivity of selective absorbers based on Si. Also, the dependence of intrinsic free carrier on temperature is fundamental to the semiconductor material; it is difficult to eliminate this effect. Thus, we should minimize the impact of intrinsic free carrier absorption by properly modeling it and then optimizing the design of the selective absorber.

The last thing that should be considered is the lattice absorption of Si at high temperature. It is assumed to be temperature-independent. It can be calculated from the simulation results of Roozeboom [34] by subtracting from 300 $^{\circ}\text{C}$ data. Therefore, we have all the needed formulas and data to properly simulate the absorption coefficient of Si from 1 - 10 μm at arbitrary temperatures, as shown in Fig. 1.7.

From the above figures, it is clear that our model of Si closely matches the literature, which indicates that we can use it to simulate the performance of Si-based selective absorbers at high temperature. Also, as mentioned above, the model generates a good fit with experimental results [Fig. 1.7(c)], which enhances its validity.

In addition to the imaginary refractive index k discussed above, we need to take into account the dependency of the real part of refractive index n on temperature.

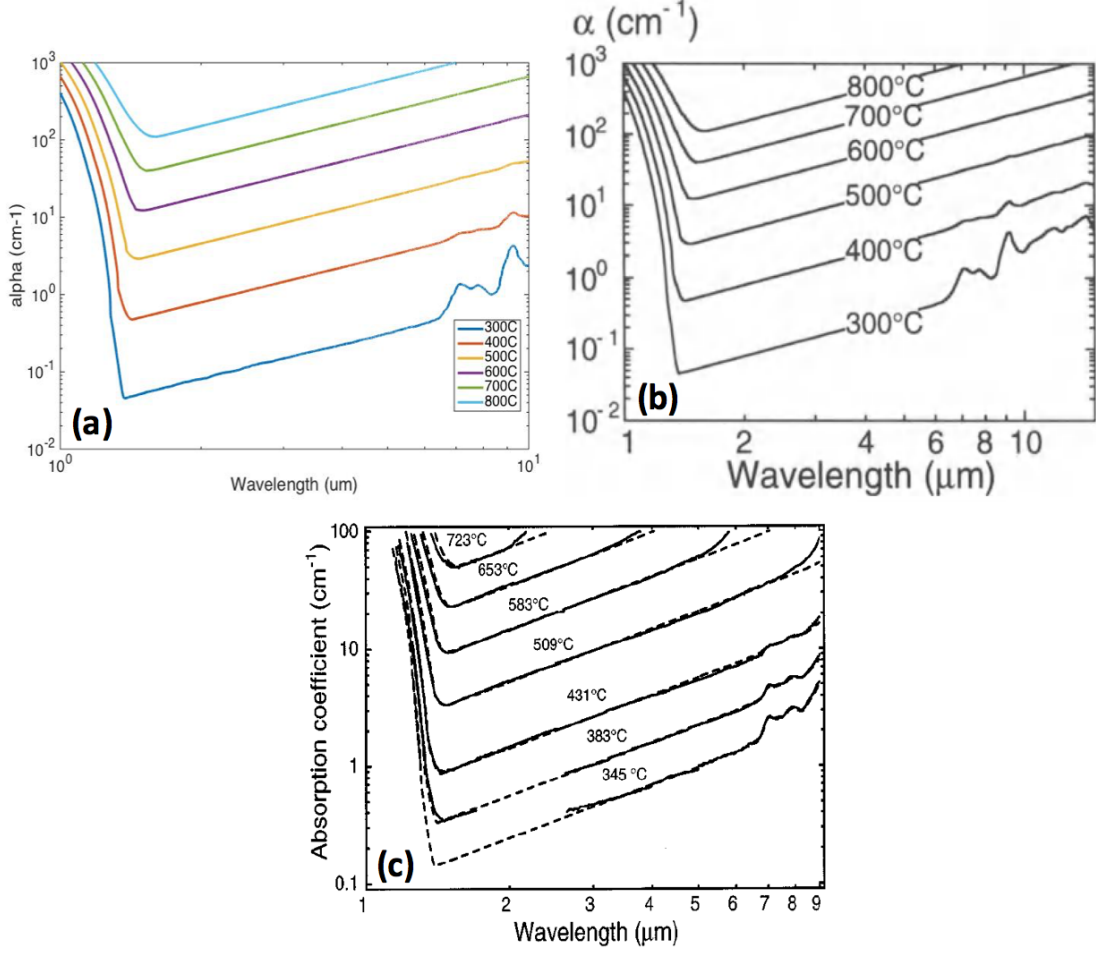


Fig. 1.7. Simulated absorption coefficient of Si at different temperatures (from 300 °C to 800 °C) from (a) our model and (b) Roozebooms results [34]. (c) comparison of experiment and simulation of absorption coefficient at different temperature. Adopted from Rogne et al [40].

From Jellison and Modines work [35], an empirical formula can be used to model n at different temperatures from 0.4 - 1 μm .

$$n(h\nu, T) = \sqrt{4.386 - 0.00343T + (99.14 + 0.062)/(E_g^2 - (h\nu)^2)} \quad (1.14)$$

where E_g is 3.652eV, T is in °C and energy is in eV. As for infrared part, Li provides the following relevant formula:

$$n(\lambda, T) = \sqrt{\epsilon_r(T) + \frac{L(T)}{\lambda^2}(A_0 + A_1T + A_2T^2)}, \quad (1.15)$$

where:

$$\epsilon_r(T) = 11.4445 + 2.7739 \times 10^{-4}T + 1.705 \times 10^{-6}T^2 - 8.1347 \times 10^{-10}T^3, \text{ and } (1.16)$$

$$L(T) = \exp(-3\Delta L(T)/L_{293}), (1.17)$$

where $A_0 = 0.8948$, $A_1 = 4.3977 \times 10^{-4}$, $A_2 = 7.3835 \times 10^{-8}$. T is in unit K and wavelength is in μm . The coefficient $\Delta L(T)/L_{293}$ is:

$$\Delta L(T)/L_{293} = -7.1 \times 10^{-4} + 1.887 \times 10^{-6}T + 1.934 \times 10^{-9}T^2 - 4.544 \times 10^{-13}T^3 (1.18)$$

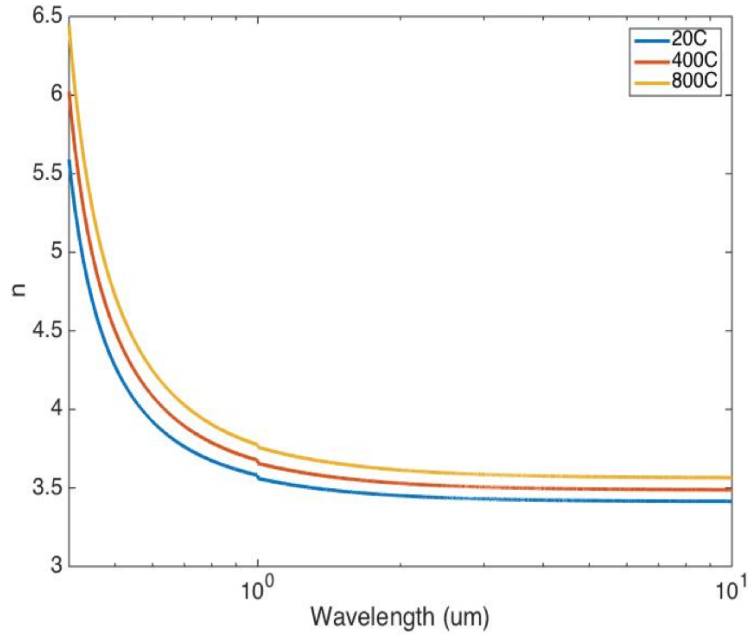


Fig. 1.8. The real part of the refractive index of Si at 20 °C (blue line), 400 °C (red line) and 800 °C (yellow line).

From the above equations, we can calculate the n spectrum for Si at different temperatures, as shown in Fig. 1.8. These result shows that n only has a little dependence on temperature, and increases gradually with T .

Since we now have both real and imaginary parts of the refractive index of Si over a wide range of wavelength and temperature, we can then simulate the reflectance

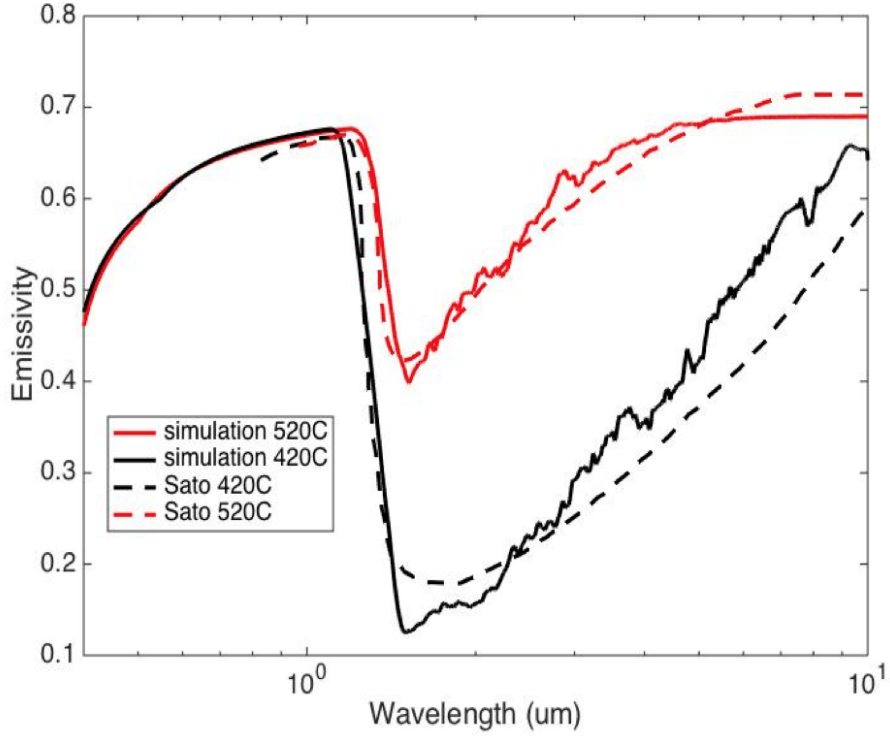


Fig. 1.9. Comparison of simulation and experimental results. The sample structure is 1.77mm lightly doped Si. Experimental data is adopted from Sato [22].

of the selective absorber using the S4 simulation tool [24, 25]. We first use this to verify the full model by comparing with experimental results from Sato [22]. They measured the emissivity of 1.77mm thick Si sample at different high temperatures. We established a similar structure in S4, and compared with experiment, as shown in Fig. 1.9. From the comparison, we see that the simulation matches well with the experimental results, except for some small deviations at long wavelengths. This may be caused by the difference between the specification of actual sample and simulated structure, such as doping, thickness and/or surface roughness. Thus, the established model can be used to compare with our room and high temperature measurement and to design and optimize selective absorber structure.

Finally, to examine and compare the performance of the designed selective absorbers, the solar thermal transfer efficiency η_t is utilized as the figure of merit. It is defined and calculated as follows [1]:

$$\eta_t = \bar{\alpha} - \frac{\bar{\epsilon}\sigma T^4}{CI}, \quad (1.19)$$

where σ is the Stefan-Boltzmann constant, T is the temperature of selective absorber in unit K, C is the solar concentration ratio, I is the solar intensity which is usually 1000 W/m^2 [1]. $\bar{\alpha}$ is the spectrally averaged absorptivity of the device, given by:

$$\bar{\alpha} = \frac{\int_0^\infty d\lambda \epsilon(\lambda) dI/d\lambda}{\int_0^\infty d\lambda dI/d\lambda} \quad (1.20)$$

where $dI/d\lambda$ is the spectral light intensity of the sun per unit wavelength under standard test conditions [1] and $\epsilon(\lambda)$ is the calculated or measured emissivity of the selective surface. $\bar{\epsilon}$ is the average emittance, and is given by:

$$\bar{\epsilon} = \frac{\int_0^\infty d\lambda \epsilon(\lambda) / \lambda^5 [\exp(\frac{hc}{\lambda k_B T}) - 1]}{\int_0^\infty d\lambda / \lambda^5 [\exp(\frac{hc}{\lambda k_B T}) - 1]} \quad (1.21)$$

where h is Planck's constant and k_B is Boltzmann's constant. With the figure of merit defined above, we can then estimate the efficiency of the designed structure and fabricated devices, and compare it with other selective absorbers in the literature.

1.2.3 Fabrication of selective solar absorber

The selective absorber is fabricated from a standard Si wafer, which is a double side polished, lightly doped, N-type, 2 inch wafer with around $300\mu\text{m}$ thickness (Pure Wafer). Ag is first deposited on the back of the Si wafer using CHA evaporator. A relatively thick Ag (around 300nm) is evaporated in order to reduce the risk of islanding effect of Ag at high temperature [7], which would decrease the reflection of light. The deposition rate is 1.5 \AA/s , which is monitored and controlled by a quartz crystal monitor in the CHA electron beam evaporator housed in the Birck Nanotechnology Center of Purdue University.

A 215nm Si_3N_4 anti-reflection coating (ARC) is finally sputtered on the front of the Si substrate using PVD sputtering, a magnetron sputtering system with unheated stage (custom built by PVD Products for Birck Nanotechnology Center). The sputtering is performed using an AC power supply operating at 100 W, with chamber pressure at 5 mTorr with a flow rate of 15 sccm Ar gas. In addition, the sample stage is rotated at 7 rpm for more uniform deposition. The total duration of the sputtering is around 86 minutes. The deposited Si_3N_4 thickness is measured and calibrated by spectroscopic ellipsometry (Filmetrics). After the fabrication of the whole wafer, it is then diced into many $1.1\text{cm} \times 1.1\text{cm}$ small samples that can be well fit into the measurement of room temperature reflection and high temperature emissivity.

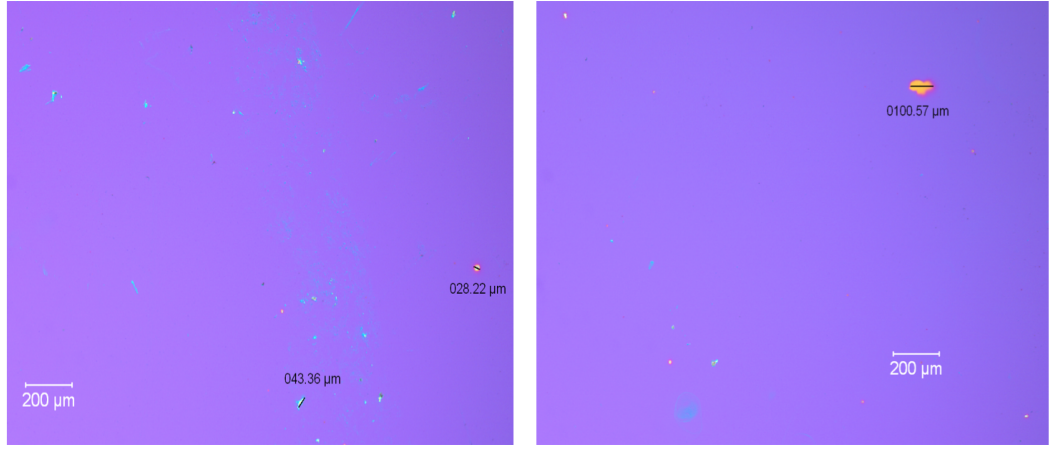


Fig. 1.10. Optical microscope pictures of the front surface of the fabricated selective absorber.

The surface of the fabricated selective absorber has a dark blue color, as shown in Fig. 1.10, which is consistent with the absorption of most visible light. There are a few defects visible on the surface, which may be caused by the surface roughness of the Si wafer and/or the attachment of little particle on the wafer surface. However, these small defects have little influence on the overall optical performance of the selective absorber, as demonstrated by the following reflectance and emissivity measurement.

1.2.4 Characterization of selective solar absorber

The room temperature reflectance of the selective absorber is measured by a Lambda 950 spectrophotometer with an integrating sphere (Labsphere). The measurement range is limited to $0.5 - 2.5\mu\text{m}$, but it is enough for room temperature characterization. The direct high temperature thermal emissivity spectrum measurement is illustrated in Fig. 1.11. The sample is placed in a vacuum chamber and heated by the heater through conduction. The emitted light is collected and guided by the Cu tube, transmitted through a CaF_2 window, reflected by three off-axis parabolic mirrors (PM 1, 2, and 3, Edmund Optics) to a Fourier Transform InfraRed (FTIR) spectrometer with a mercury cadmium telluride detector and KBr beam splitter (Thermo Fisher Nicolet 670). The vacuum chamber is kept at low pressure (10^{-7}mTorr) during the measurement.

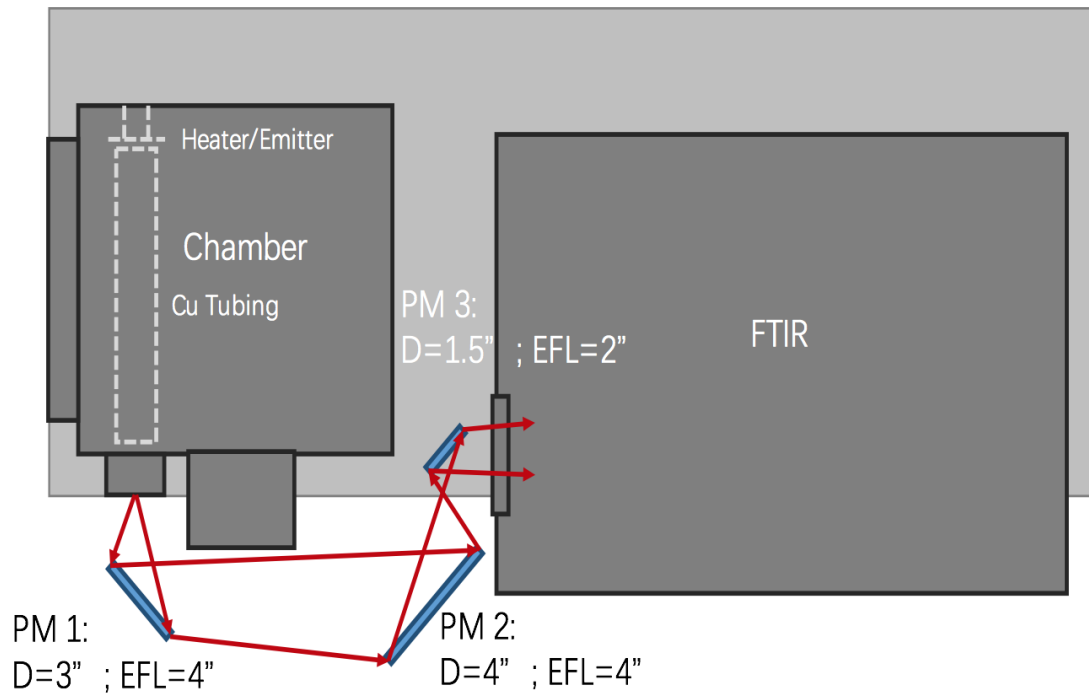


Fig. 1.11. Schematic of the direct thermal emission spectrum measurement system. PM is off-axis parabolic mirror, D is the diameter of the mirror, EFL is the effective focus length and FTIR stands for Fourier Transform InfraRed spectrometer.

The surface temperature of the sample is measured by a type-K thermocouple, which is attached to the sample's surface directly by high temperature paste (Ultra-temp 516). As for the FTIR measurement, 100 scans are used to achieve a high signal-to-noise ratio through most of the spectrum. During this time, the detector is maintained at low temperature (77K) by frequently adding liquid nitrogen to the FTIR in order to maximizing detectivity of small signals. A carbon nanotube sample is used as a relevant blackbody reference, which has been demonstrated by measuring its ultra-low reflectance at room temperature.

The emissivity spectrum of the selective absorber is calculated according the calculation method by F. Marquier et al [41], which uses a blackbody as a reference, while taking the background emission into account. The measured FTIR of the sample is expressed as following [41]:

$$FTIR_s(\lambda, T_s, T_{sh}) = R(\lambda)[\epsilon(\lambda, T_s)P(\lambda, T_s) + B(\lambda, T_{sh}) + \rho(\lambda, T_s)P(\lambda, T_R)], \quad (1.22)$$

where T_s , T_{sh} , T_R are the temperatures of the sample, the heater and room temperature respectively. $\rho(\lambda, T_s)P(\lambda, T_R)$ is the reflection of the room background by the sample surface. $R(\lambda)$ is the response function of the FTIR itself, $B(\lambda, T_{sh})$ is the background which is related to the temperature the heater, and $P(\lambda, T)$ is Planck's blackbody equation:

$$P(\lambda, T) = \frac{2hc^2}{\lambda^5} \frac{1}{\exp(\frac{hc}{\lambda k_B T}) - 1} \quad (1.23)$$

where h is Planck's constant, k_B is Boltzmann's constant, and c is the speed of light. $\rho(\lambda, T_s)$ is the reflectivity of the emitter at temperature T_s . According to Kirchhoff's law of thermal radiation, $\rho(\lambda, T_s) = 1 - \epsilon(\lambda, T_s)$. Thus, the equation (1.22) reduces to:

$$FTIR_s(\lambda, T_s, T_{sh}) = R(\lambda)\{\epsilon(\lambda, T_s)[P(\lambda, T_s) - P(\lambda, T_R)] + B(\lambda, T_{sh}) + P(\lambda, T_R)\} \quad (1.24)$$

In order to eliminate the background $B(\lambda, T_{sh})$ and $P(\lambda, T_R)$, a Mo cap deposited with Ag (which has very low emissivity) covers the sample room window, which is

kept around room temperature. Then the FTIR at similar heater temperature is measured, which is:

$$FTIR_R(\lambda, T_R, T_{sh}) = R(\lambda)[B(\lambda, T_{sh}) + P(\lambda, T_R)]. \quad (1.25)$$

Then, by subtraction, we have:

$$FTIR_s(\lambda, T_s, T_{sh}) - FTIR_R(\lambda, T_R, T_{sh}) = R(\lambda)\epsilon(\lambda, T_s)[P(\lambda, T_s) - P(\lambda, T_R)]. \quad (1.26)$$

Similarly, we can follow the same procedure for a blackbody reference but with nearly unit emissivity, $\epsilon_B(\lambda, T_B) \approx 1$. Then we find:

$$FTIR_B(\lambda, T_B, T_{Bh}) - FTIR_R(\lambda, T_R, T_{Bh}) = R(\lambda)[P(\lambda, T_B) - P(\lambda, T_R)] \quad (1.27)$$

By dividing Eq. (1.26) by Eq. (1.27) and doing simple algebra, we can finally calculate the emissivity of the selective absorber as:

$$\epsilon(\lambda, T_s) = \frac{FTIR_s(\lambda, T_s, T_{sh}) - FTIR_R(\lambda, T_R, T_{sh})}{FTIR_B(\lambda, T_B, T_{Bh}) - FTIR_R(\lambda, T_R, T_{Bh})} \frac{P(\lambda, T_B) - P(\lambda, T_R)}{P(\lambda, T_s) - P(\lambda, T_R)} \quad (1.28)$$

1.3 Results and analysis

1.3.1 Room temperature emissivity

The room temperature reflection and emissivity of the fabricated sample has been measured and calculated first, as shown in Fig. 1.12. They are also compared with the simulation in the same figure. The range can only be measured between 0.5-2.5 μm in this spectrometer, which fortunately is enough for temperature characterization. As indicated by Fig. 1.12, the experiment fits well with the simulation results, which means the devices are fabricated as expected. Therefore, the thickness of Si_3N_4 is most likely around 215nm at room temperature. Also, the simulation has been validated further, which increases our confidence in guiding future measurements and device design.

Overall, the results are consistent with our expectations that the ARC should increase the absorption of photons with energies above the cutoff. Also, there is a

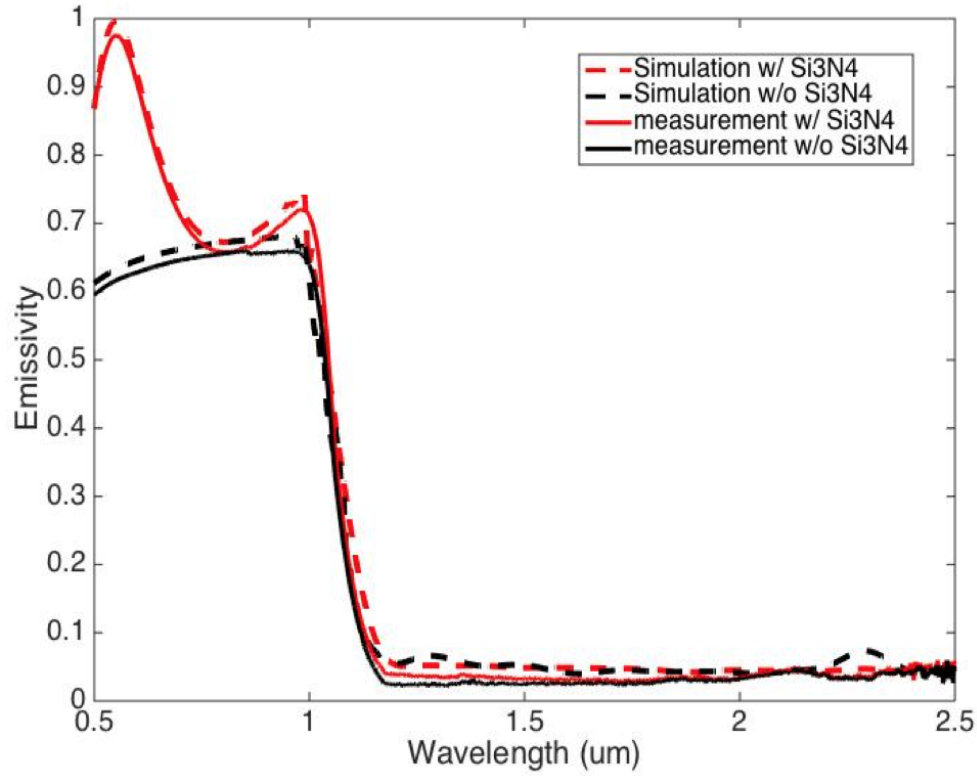


Fig. 1.12. Measurement (solid lines) and simulation (dashed lines) of the emissivity of selective absorbers with (red lines) and without (black lines) front coating at the room temperature. The thicknesses of Si_3N_4 , Si and Ag are 215nm, 300 μm and 300nm respectively.

sharp cutoff of emissivity observed around 1.1 μm , which makes the selective absorber effectively absorb most solar light, while suppressing re-radiation below the cutoff energy. Thus, this structure has potentially high solar thermal transfer efficiency.

1.3.2 High temperature emissivity

The emissivity of the selective absorber with and without Si_3N_4 AR coating at different high temperature is measured using the direct thermal emission measurement system described above, as shown in Fig. 1.13. The measurement shown in the figure is modified by taking the error of the thermocouple temperature measurement into

account, which is 2% in our case. For example, for the 468+25 °C curve in Fig.1.13 (a), 468 °C is actually the measured value from the thermocouple, plus 25 °C, is the temperature gradient generated by the thermocouple contact resistance. After this modification, the measured and simulated emissivity match each other, thus verifying the consistency of the model and the measurement system. However, there is still a small discrepancy between the theory and experiment [e.g., 520+15 °C in Fig. 1.13(b)]. This is mainly due to the area difference between the sample and the blackbody .

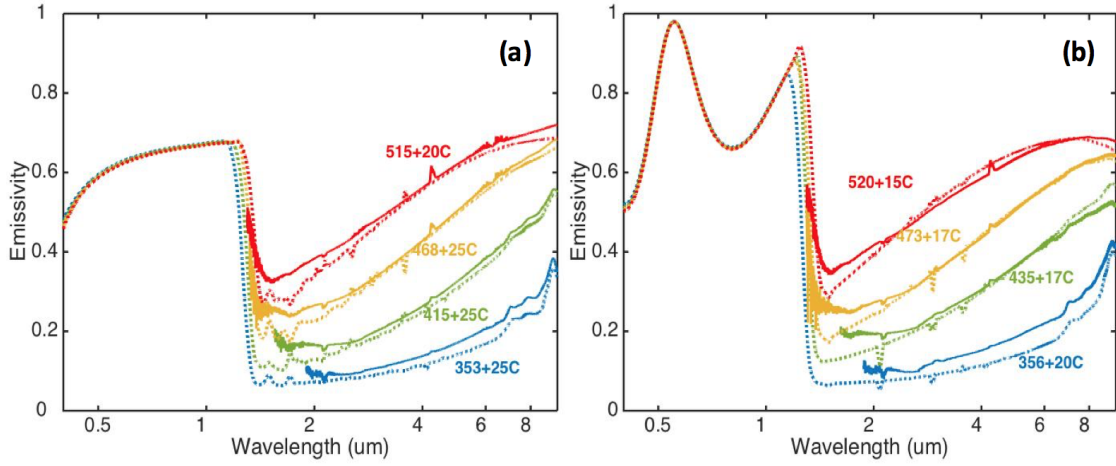


Fig. 1.13. Measurement (solid lines) and simulation (dashed lines) of the emissivity of the selective absorber: (a) without and (b) with a Si₃N₄ AR coating at different high temperatures. The thicknesses of Si₃N₄, Si and Ag are 215nm, 300μm and 300nm, respectively. High spectral selectivity is observed at 473 °C in structure with AR coating, with a cutoff wavelength of approximately 1.3μm.

The structure with the AR coating shows increased light absorption above the cutoff, which is insensitive to temperature. The cutoff wavelength redshifts to longer wavelength with increased temperature, due to the reduction of the Si bandgap with temperature. Thus, the absorption gradually increases as we increase the temperature. As for longer wavelength, the emissivity increases dramatically with temperature, which is both predicted by the model and measured in the experiment. This is

mainly due to the free carrier absorption of Si as it enters the intrinsic region at high temperature [22]. Also, the lattice absorption peaks around 6 - 9 μm is observed at relatively low temperature [353+25 $^{\circ}\text{C}$ and 356+20 $^{\circ}\text{C}$ in Fig. 1.13(a) and 1.13(b)], which is also seen in simulation. The increased absorptivity of Si at high temperature limits the highest temperature the selective absorber can maintain selectivity. Nonetheless, the Si-based solar selective absorber shows good selectivity when the temperature is below 473 $^{\circ}\text{C}$ for samples with a Si_3N_4 AR coating.

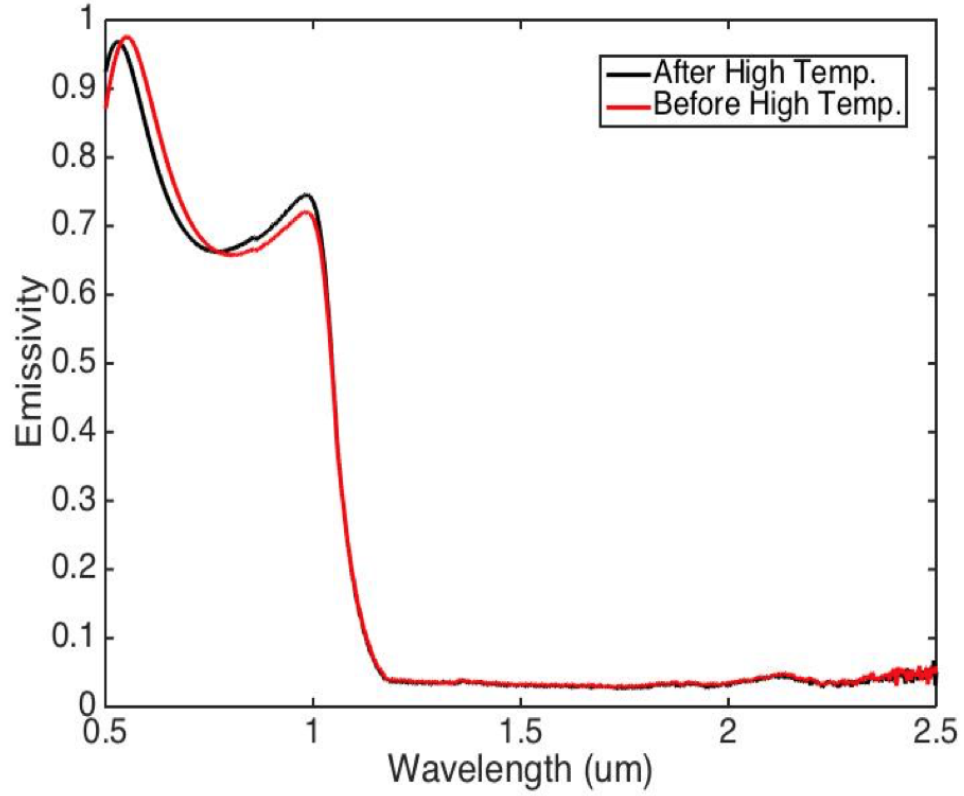


Fig. 1.14. Room temperature emissivity of the selective absorber with Si_3N_4 AR coating after (black line) and before (red line) the high temperature thermal emission measurement.

After the measurement of samples at high temperature, the room temperature reflection is remeasured to determine whether any significant structural changes or failures occur at high temperatures. As shown in Fig. 1.14, there is only a slight discrepancy of the emissivity spectra of these samples before and after high temper-

ature measurements. The difference may be due to the surface non-uniformity of Si_3N_4 front coating deposition of the fabricated sample, which shifts the spectrum in different areas of the sample. Also, it may be caused by the change of the thickness of Si_3N_4 during high temperature, but the change is very modest, and acceptable for solar thermal absorption applications. In addition, the spectrum below the cut-off remains unchanged, indicating that Ag is not destroyed by the high temperature characterization procedure. The same measurement is performed for many other samples both with and without Si_3N_4 AR coating, which shows similar results. Very modest if any changes in the samples are observed after high temperature exposure, which demonstrates the fundamental thermal stability of this Si-wafer based selective absorber architecture.

1.3.3 Thin Si film selective absorber design and optimization

As illustrated by both simulations and experimental results, the selective absorber suffers from strong free carrier absorption at high temperatures, which increases the emissivity of light below the cutoff and thus decreases the overall thermal transfer efficiency. To mitigate this problem, one possible solution is to reduce the thickness of the Si substrate. Fortunately, as demonstrated by Yi Cui [23], when the thickness of a Si wafer is below $10\mu\text{m}$, it possesses excellent mechanical stability and bendability, as counter-intuitive as this behavior may seem. In this way, the selective absorber based on thin film Si substrate may not only exhibit higher efficiency, but high flexibility which has wider potential applications. Thus, in this section, the design and optimization of thin Si film selective absorber is described, to pave the way for future experiments.

At first, the selective absorber with different Si thicknesses is simulated and analyzed in order to examine the influence of Si thickness. As shown in Fig. 1.15(a), the emissivity below the cutoff decreases rapidly with Si thickness, which indicates that free carrier absorption is suppressed effectively by a thin-film Si layer. However, in

the same time, the absorption of light right above the cutoff also degrades gradually, since ultra-thin-film Si structures cannot absorb all photons above the bandgap energy. Thus, there exists a trade-off between suppressing free carrier absorption and absorbing photons above the cutoff as much as possible.

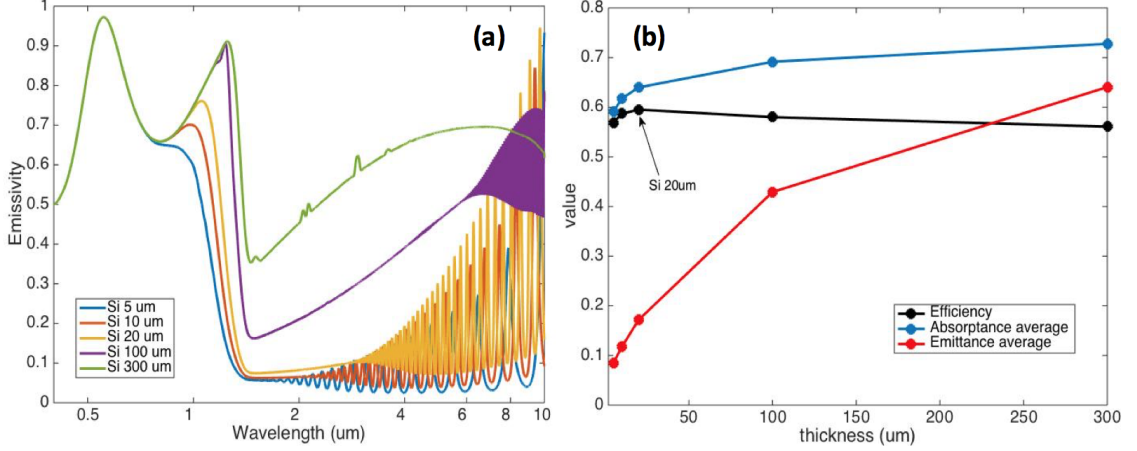


Fig. 1.15. (a) Emissivity for selective absorbers with different Si thicknesses. Si_3N_4 thickness is 215nm, and the temperature is targeted at 550 °C. (b) dependency of efficiency (black line), average absorptance (blue line) and average emittance (red line) on Si thickness. The efficiency is calculated at 100 suns concentrations.

Because of this trade-off, there is an optimal Si thickness that produces the highest efficiency, as shown in Fig. 1.15(b). As the Si thickness decreases, both the average absorptance and average emittance decreases, but emittance decreases faster than absorptance. It turns out that a 20 μm Si thickness exhibits the highest efficiency, which is around 60%. Since the efficiency for all thicknesses is calculated under 100 suns, which decreases the weight of average emittance to a large extent in calculating efficiency, it seems like the difference of efficiency between thick and thin Si thickness is very little. However, as we will show in the following analysis, thin Si film selective absorber is much less sensitive to concentration than thick Si. Therefore, this allows us to reduce the concentration while not destroying the efficiency, which will

benefit practical applications where solar concentrations will not always reach their theoretical limits throughout the course of years in the field.

Since the optimal Si thickness has been found above, the silicon nitride thickness is then varied to find out the best value for thin Si film selective absorber [42]. The dependency of efficiency on Si_3N_4 thickness (Fig.1.16 (a)) indicates that 80nm Si_3N_4 front coating generates the highest efficiency, which is 71.43%. We can see more clear from the emissivity spectrum for different Si_3N_4 thicknesses in Fig. 1.16(b) that 80nm Si_3N_4 (red line) covers more area of the spectrum region above the cutoff than 215nm thickness (purple line).

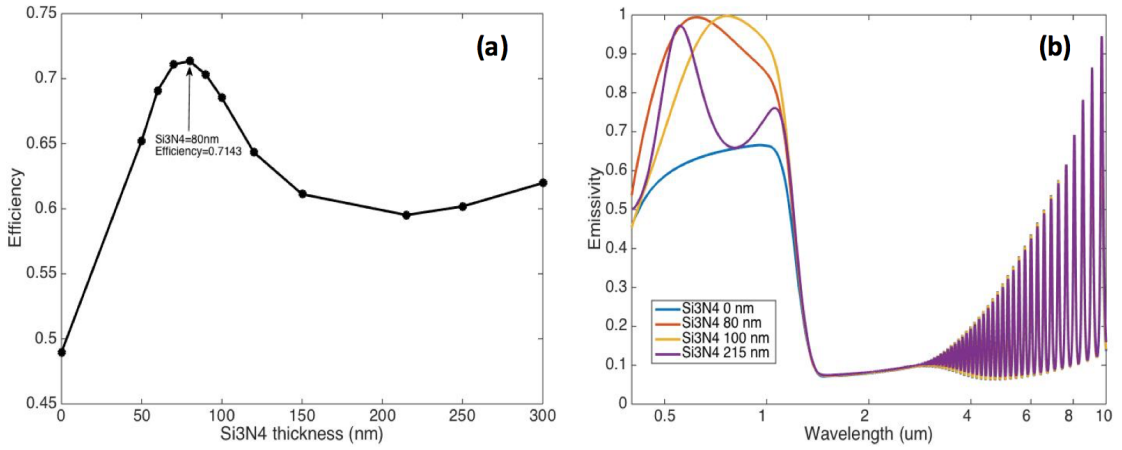


Fig. 1.16. (a) Efficiency for $20\mu\text{m}$ thick Si thin film selective absorber with different Si_3N_4 thickness ranging from 0 to 300nm. The efficiency is calculated under 100 suns and 1000W input solar intensity. (b) Emissivity for selective absorbers with different Si_3N_4 thicknesses. The thicknesses of Si and Ag are $20\mu\text{m}$ and 300nm respectively. The temperature is set at 550°C .

The optimization is repeated for other Si thicknesses, which shows similar optimal Si_3N_4 thicknesses. Also, different concentrations are considered to examine the sensitivity of efficiency to the concentration. The results are all summarized in Fig. 1.17. From these results, we can draw the following conclusions: (i) the optimal Si_3N_4 thicknesses are all around 70-80nm for different Si substrate thicknesses and

does not change with the concentration; (ii) the thinnest Si selective absorbers will be less sensitive to concentration, since their spectrally-averaged emissivity is lower; thus, (iii) for different concentrations, there will be a different optimal Si thickness – as concentration goes down, the optimal Si thickness decreases; and finally, (iv) for concentration as low as 20 suns, the maximum efficiency for 5 μm Si thickness can still be 60%.

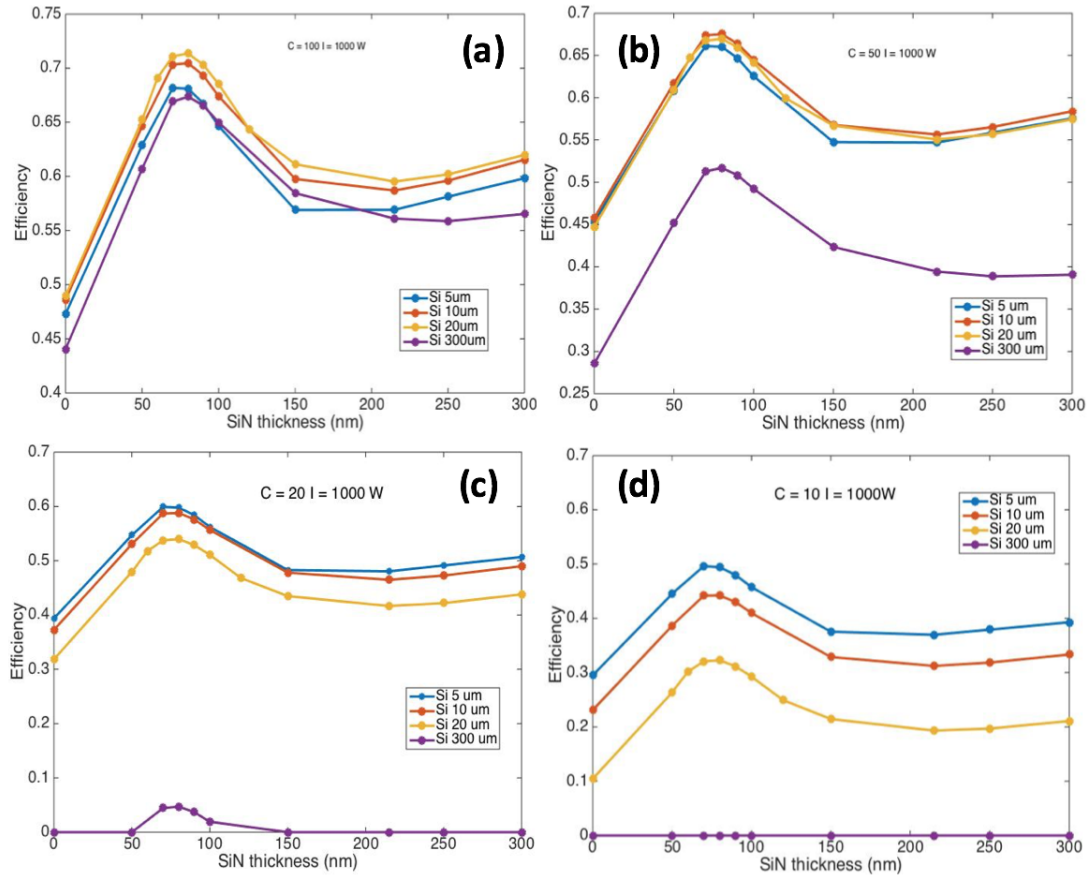


Fig. 1.17. Dependence of efficiency on Si_3N_4 thickness for different Si thicknesses under (a) 100 suns, (b) 50 suns, (c) 20 suns and (d) 10 suns. The operating temperature is fixed at 550 °C.

Since the optimal Si_3N_4 thickness for different Si thickness is around 80 nm, the emissivity spectrum for different Si thicknesses is plotted together with 80 nm Si_3N_4 in Fig. 1.18. The emissivity below the cutoff is effectively suppressed for thin Si

films. Although the absorption of photons right above the cutoff energy is decreased in the same time, it is compensated by the suppression of thermal re-radiation, which enables the selective absorber to remain at a high thermal transfer efficiency across a large range of concentrations. In addition, the cutoff maintains a sharp cutoff across all Si thicknesses.

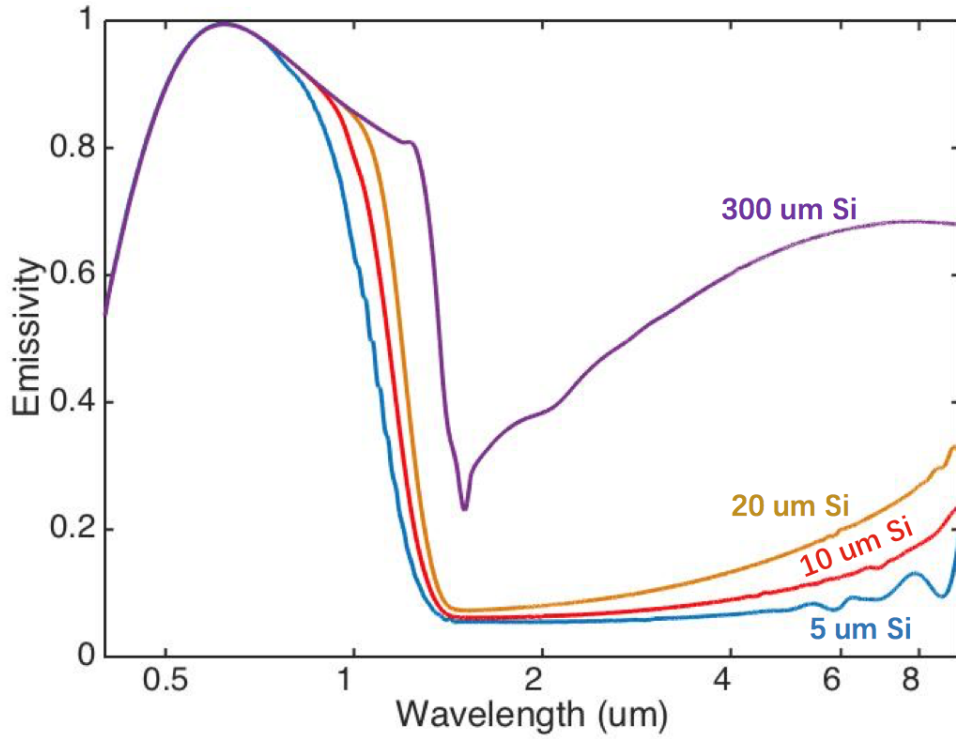


Fig. 1.18. Emissivity spectrum for selective absorbers with different Si thicknesses. The thickness of Si_3N_4 is the optimal value, 80 nm. The temperature is set at 550 °C. The F-P interference at Mid-IR is smoothed out for more clear comparison.

The dependence of η_t on a broad range of solar concentration values is illustrated in Fig. 1.19. As expected from previous results and analysis, thinner Si layers are less sensitive to the concentration such as 5 μm , which maintains around 65% efficiency across a large range of concentrations. As solar concentration decreases, the optimal Si thicknesses reduce gradually from 20 μm , to 10 μm , and finally, to 5 μm .

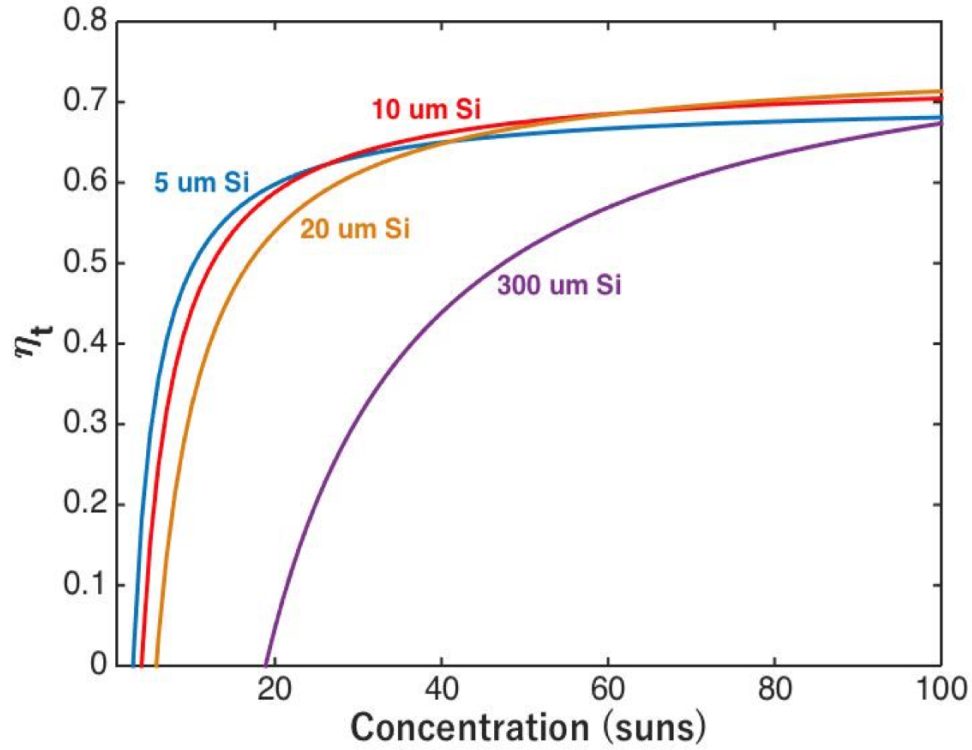


Fig. 1.19. Dependency of efficiency on the concentration for different Si thickness. The Si_3N_4 thickness is fixed at 80nm, and the temperature is 550 °C.

To capture these effects more generally, a contour plot in Fig. 1.20 presents thermal transfer efficiency as a function of a broad range of Si thicknesses and solar concentrations. For high concentrations (≥ 50 suns), the efficiency is higher for thick Si, and insensitive to Si thicknesses greater than $8\mu\text{m}$. As the concentrations go down, the optimal Si thicknesses decrease gradually, and are sub- $10\mu\text{m}$ ($4 - 8\mu\text{m}$). For Si thicknesses below $4\mu\text{m}$, it is much less sensitive to the concentration, probably due to the low spectrally-averaged emissivity. In all cases, as one would expect, the maximum efficiency always drops with reduced concentration.

Additionally, as demonstrated by Yi Cui's group [23], when the Si substrate is thinner than $10\mu\text{m}$, it exhibits excellent mechanical stability and flexibility. In this case, $10\mu\text{m}$ Si thin films may be more suitable for achieving high efficiencies with

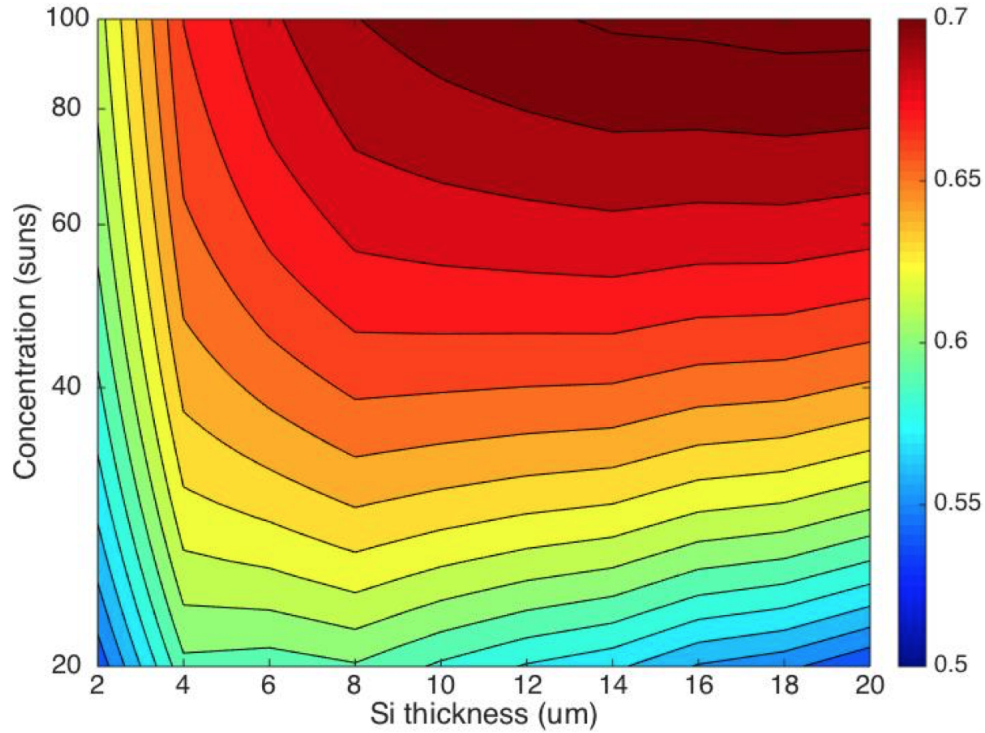


Fig. 1.20. Two dimensional map of the thermal transfer efficiency for different Si thickness under different concentration. Si_3N_4 thickness is fixed at 80nm, Ag is 300nm thick. The targeted temperature is 550 °C.

mechanical flexibility. In conclusion, the optimal 80nm Si_3N_4 thickness, combined with a 10 μm -thick Si thin film selective absorber, has the potential to generate high efficiency (around 67%) under moderate concentrations. At the same time, its excellent flexibility commends it to a wider variety of applications. Therefore, the simple structure, the mechanical stability, relatively easy and reliable fabrication and high efficiency makes the thin Si film selective absorber more competitive and useful. This line of investigation should be pursued aggressively in future experimental research.

2. SELF-HEALING STRUCTURES TO REDUCE ELECTROMIGRATION FAILURES

2.1 Introduction to Electromigration

Following Moore’s law, the feature size of today’s integrated circuits (IC) has been getting smaller and smaller. As a consequence, the current density has increased to the extent that it may reduce the reliability of IC systems. In the context of renewable energy, this is particularly relevant in parts such as micro-inverters, which have been identified by several major companies (Toshiba, Enphase) as a weak link in these systems. One of the key degradation mechanisms observed in this context, called Electromigration, has recently drawn much attention from researchers and IC designers [43–46]. As shown in Fig. 2.1, as electrons move from the cathode to the anode, they collide with metal ions and transfer momentum to individual atoms, moving them in the direction of the electron wind. This electron-associated force can be so large under high current density that it will overcome the confinement of the crystalline lattice, as well as the electric field from the anode to the cathode [47]. There are mainly three kinds of paths in which atoms can move: grain boundaries, in the bulk, and on the surface, as illustrated in Fig. 2.1(b). Among these, grain boundaries generally dominate, thus causing most electromigration [47]. Because of this phenomenon, the distribution and orientation of grain boundaries greatly influence electromigration [48–50].

Under the collision force from electrons, atoms in the interconnect wires suffer from gradual displacement, which forms hillocks and voids at grain boundaries (Fig.2.2). These defects may cause severe problems for the circuits, such as the fracturing of interconnects via large voids, and short circuits due to hillock formation.

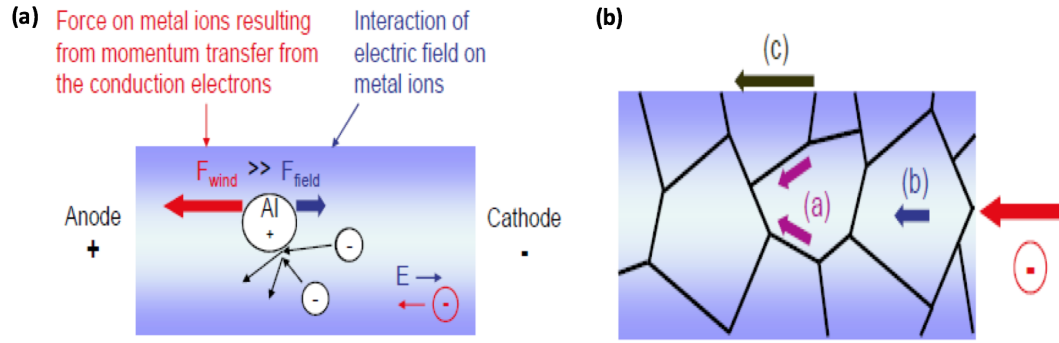


Fig. 2.1. (a) Schematic of the principle of electromigration. (b) Three major mechanisms of electromigration: (a) grain boundary, (b) bulk diffusion, and (c) surface diffusion. Adopted from Lienig, Jens [47].

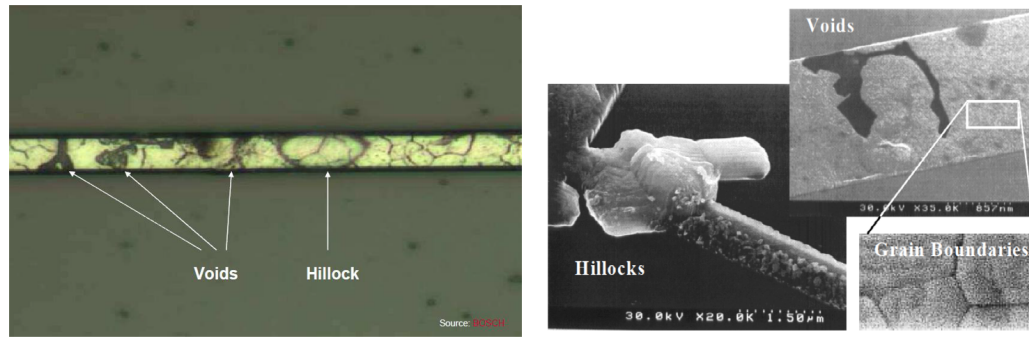


Fig. 2.2. Typical voids and hillocks formed by electromigration. Adopted from Lienig, Jens [47].

Due to the serious damage caused by the electromigration, they have been widely studied by many researchers [51–53]. To study electromigration in the lab in a reasonable amount of time, extremely high voltages and current densities have been applied to nanodevices under test in prior work [54]. As shown in Fig. 2.3(a), the voltage is gradually increased, and the current and conductance are monitored accordingly. At the beginning, the current increases linearly and the conductance stays constant. However, when the voltage is beyond a critical value, the current and conductance drops to zero suddenly, which suggests that the test line has broken abruptly. Also, right before this happens, the conductance decreases gradually, which may be due to

the formation of microvoids in the device in or close to the critical current path. Fig. 2.3(b) clearly shows the ultimate results of electromigration: a 6nm gap is formed near the cathode end, which is often observed in many electromigration studies [44, 46].

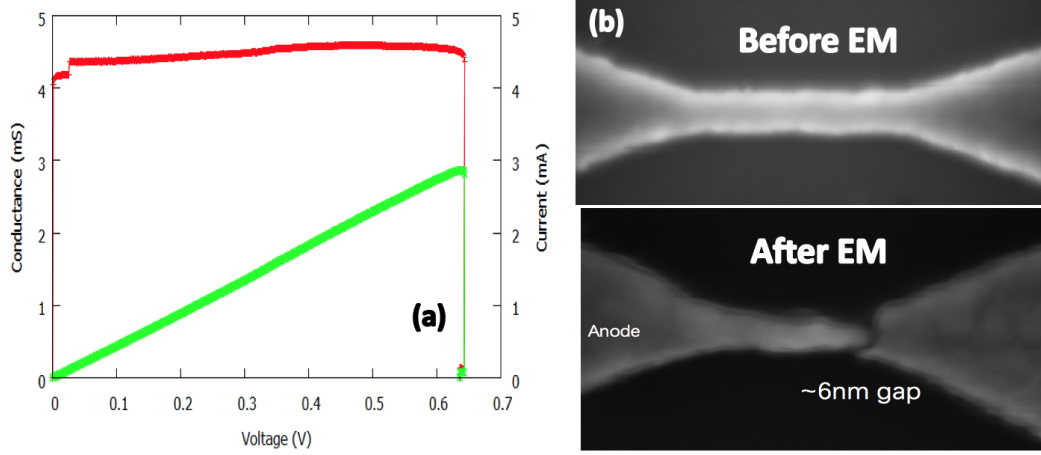


Fig. 2.3. Typical test results of electromigration. (a) changes of the conductance (red curve) and current (green curve) with gradually increasing voltage. (b) SEM images of the test device before and after the electromigration (EM). A 6nm gap is formed near the cathode pad after the test. Results are adopted from Teresa Esposito, Kim Lewis [54].

To analyze electromigration quantitatively, the EM lifetime is defined as an evaluation parameter for electromigration. The median time to failure (MTTF) is used and defined as follows: under certain condition (e.g. constant current density), 50% of devices will fail after the time MTTF, or equivalently, one device will have a 50% probability of failing after the MTTF time has elapsed. In fact, MTTF is the median lifetime of a set of identical devices [45]. Therefore, to measure MTTF, many devices are tested in the same way, and their time to failure is recorded, as shown in Fig. 2.4.

Based on the experimental results, a semi-empirical equation, Black's equation, has previously been proposed and used to calculate the MTTF of a interconnect due to the electromigration degradation [55–58]. It is given by:

$$MTTF = \frac{A}{J^n} \cdot e^{E_a/k_B T}, \quad (2.1)$$

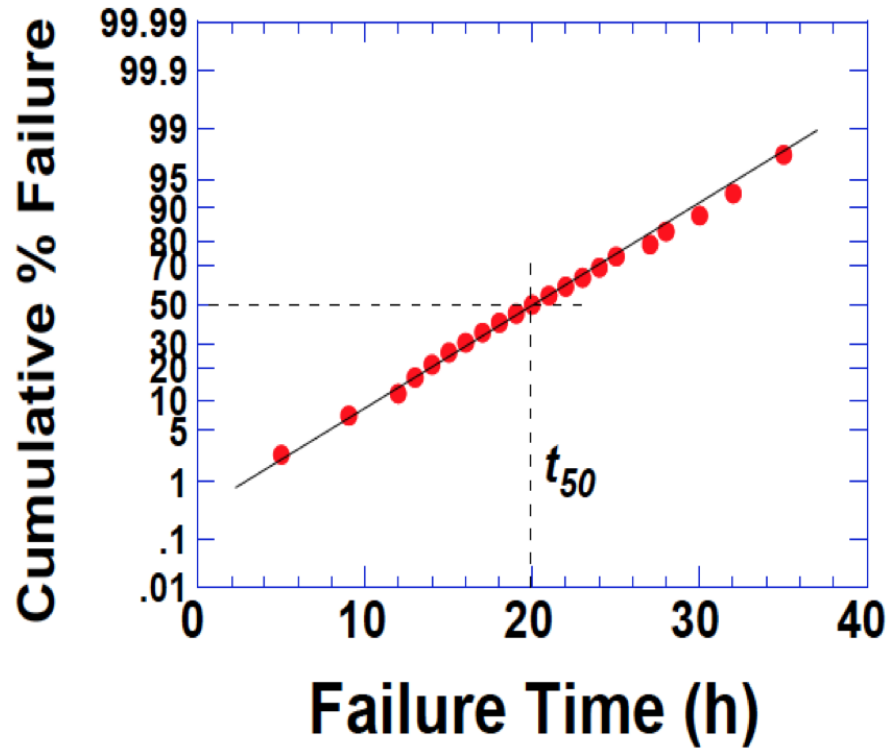


Fig. 2.4. Typical results of the distribution of the failure time of many similar devices under electromigration test. The median number of the failure time is found and defined as the lifetime of the device.

where A is a geometry-dependent constant, J is the current density in the interconnect, n is the exponent of the current density (usually equals 2), E_a is the activation energy of metal atoms, k_B is Boltzmann's constant, and T is the temperature of the device (in unit K). As illustrated by Black's equation, the lifetime is inversely proportional to the current density to some power, since the electron force will be higher for increased current density. Additionally, if the temperature increases, the lifetime will drop exponentially. Finally, metals with the highest activation energies will experience the longest lifetimes.

Many concepts to reduce the risk of electromigration damage have been previously investigated. For example, researchers have utilized physical designs and optimized circuit designs to reduce the current density [59–61], and some have designed novel ar-

chitectures to mitigate electromigration [62, 63], or copper doping in Al film to reduce electromigration risk [64, 65]. There are some special effects of the electromigration that also need to be considered in real device design and EM study. First of all, when the width of the wire is narrow enough, it will form bamboo-like grain boundary structures, which protect the atoms from moving with the electron wind [47, 66, 67]. This effect may potentially increase the lifetime of the device. Also, when the length of the interconnect is short (10 - 100 μm), a mechanical stress gradient will be established along the line, which helps atoms move along the opposite direction of the electrons. This effect may compensate the displacement caused by the electromigration, thus preventing the formation of voids [47, 68–70]. In addition, the reservoir effect, which elongates the lifetime of an interconnect by placing extra material source near potential voids, has been widely studied and utilized for electromigration mitigation [71, 72].

In this work, we propose a self-healing structure, aiming at refilling voids to improve the reliability of interconnects. By placing a material reservoir near the spots of potential void formation, it functions to refill the void and increases the lifetime of the test lines. Interconnect lines with voids and reservoirs are designed and fabricated using the lift-off process to study electromigration and demonstrate the self-healing effect. The material we mainly focus on in this study is aluminum, which is commonly used in integrated circuits, and known to be susceptible to electromigration [53, 73].

To precisely analyze the change and distribution of temperature over the interconnect, we utilize the thermal reflectance imaging (TRI) technique [74–76]. By gradually increasing the voltage over time, the test lines suffer from increasing rates of electromigration, due to the ever-larger current densities they experience. The progression of failure of these interconnect are identified by measuring their resistance using four probe measurements. Based on these tests, we can estimate the lifetimes of each kind of devices, the causes of electromigration, and the efficiency and functionality of the reservoirs.

According to our study and experiments, the introduction of reservoirs is expected to realize a self-healing of the interconnect, which will lead to more reliable

and long-lifetime electronic system. The failure of the device is found to depend on the symmetry of the interconnect, which may provide guidelines for practical circuit design and reservoir optimization. In short, this self-healing structure may provide us with the ability to relieve degradation from electromigration to increase the lifetimes of long interconnect channels.

2.2 Method

2.2.1 Self-healing structure

To improve the reliability of interconnects, we propose a self-healing structure, aiming at refilling voids, as shown in Fig. 2.5 (structure 3). By placing a material reservoir near the areas of potential void formation, it has the greatest potential to refill them efficiently. We design and fabricate different types of interconnect lines with voids and reservoirs to demonstrate this self-healing effect. Structure 1 has no void and no reservoir, which serves as control. Structure 2 has one void but no reservoir, while structure 3 has one void and one reservoir near the void. Each structure has different combinations of line widths W and void and reservoir radii r , as shown in Table 2.1.

Table 2.1
Parameters for different combinations of line width and void/reservoir radius.

W (μm)	5		8		10	
r (μm)	1	2	1.6	3.2	2	4

The material we mainly focus on is aluminum, which is commonly used in integrated circuits and susceptible to electromigration [53, 73]. To generate a reasonable resistance matched to the range and resolution of our voltage source, the interconnect length is designed to be 1.25mm. However, this length makes it difficult to observe the whole device at high magnification in the following characterization setup. Thus,

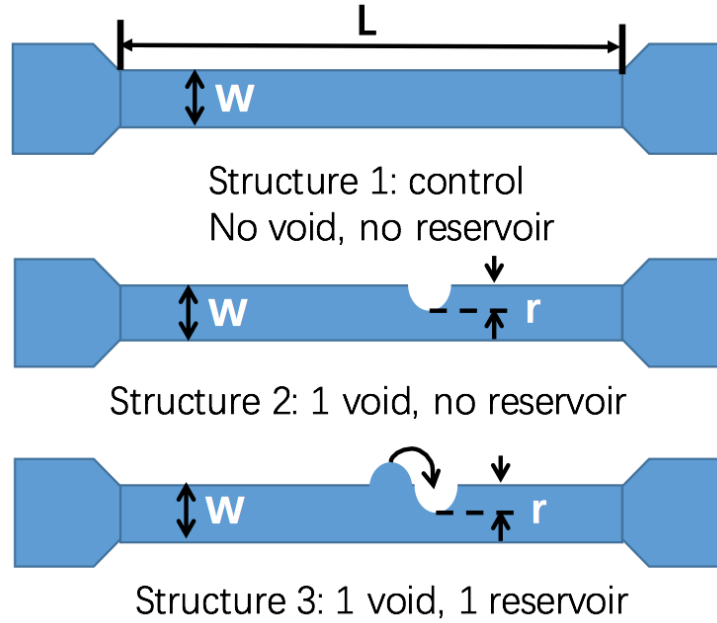


Fig. 2.5. Schematics of designed test structures with or without void and/or reservoir.

we design serpentine-shaped resistors via a mask pattern, as shown in Fig. 2.6. Fig. 2.6(a) is a typical serpentine pattern with $5\mu\text{m}$ line width and without void, which contains two same resistors. The upper one has a label '5 0', which indicates a $5\mu\text{m}$ line width with 0 void/reservoir. For other kinds of labels, such as '5 2 2', 5 means $5\mu\text{m}$ line width, the middle number 2 means the radius of the void/reservoir is $2\mu\text{m}$, and the last number 2 means there is one void and one reservoir (in contrast with only '1' void structure). Fig. 2.6(b) shows the final array of devices with different line width and void/reservoir radius. The black square can fit into the thermoreflectance imaging system with good resolution.

2.2.2 Fabrication of test lines

The lift-off process is used for the fabrication of the metal serpentine resistors is summarized in Fig. 2.7. At first, the patterns are transferred from the mask to the

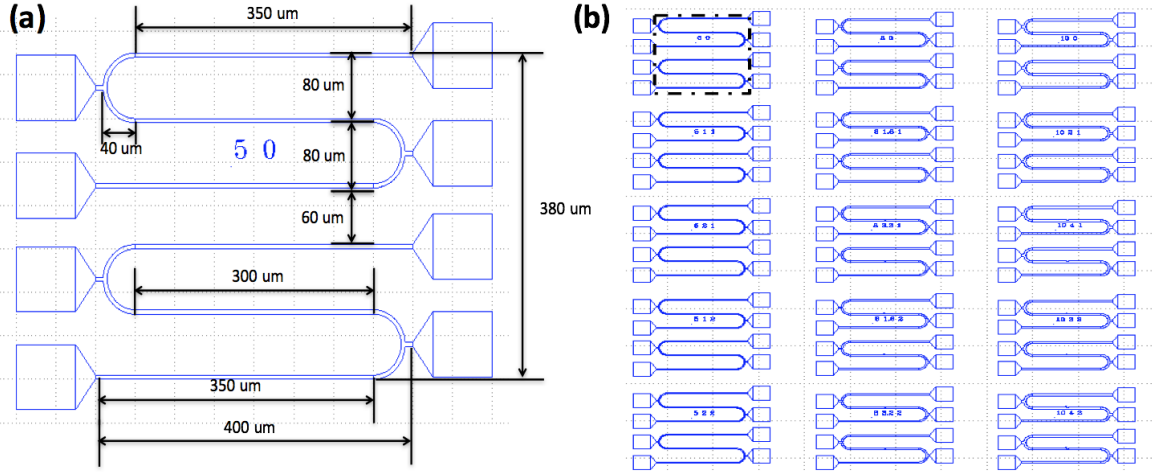


Fig. 2.6. The designed mask patterns for the fabrication of the devices. (a) Typical serpentine resistor pattern with $5\mu\text{m}$ line width. The size of each part is labeled in the figure. (b) Devices with different combinations of width (5, 8 and $10\mu\text{m}$) and radius. The size of black square is around $400\mu\text{m} \times 400\mu\text{m}$ for better thermal reflectance imaging.

photoresist by the standard photolithography process, using the following procedures: (1) the standard Si wafer (Double side polished, 4 inch, $\langle 100 \rangle$ direction) with 200nm SiO_2 (dry thermal oxidation) on top is cleaned by soaking in Acetone, Methanol, IPA in ultrasonic water each for 5 minutes; (2) the wafer is then dried by nitrogen and prebaked on hotplate at 120°C for 5 minutes; (3) $1.8\mu\text{m}$ positive photoresist (AZ 1518) is applied to the wafer using a G3 Wafer Spinner (step 1: 500 rpm, 5 s; step 2: 4000 rpm, 45s); (4) the wafer is soft-baked on a hotplate at 90°C for 5 minutes to harden the photoresist; (5) the pattern is transferred from the mask to photoresist by exposing the wafer under the mask using the UV light in the mask aligner (Suss MA 6 Mask Aligner), the exposure time is 13s; (6) the exposed photoresist is developed in the developer (AZ 340 : ultra-pure water (1:4)) for 10 - 12 s (the time should be controlled strictly, since over-development will destroy the smallest feature, $1\mu\text{m}$

void), then the developed wafer is rinsed in ultra-pure water for several seconds and dried by nitrogen.

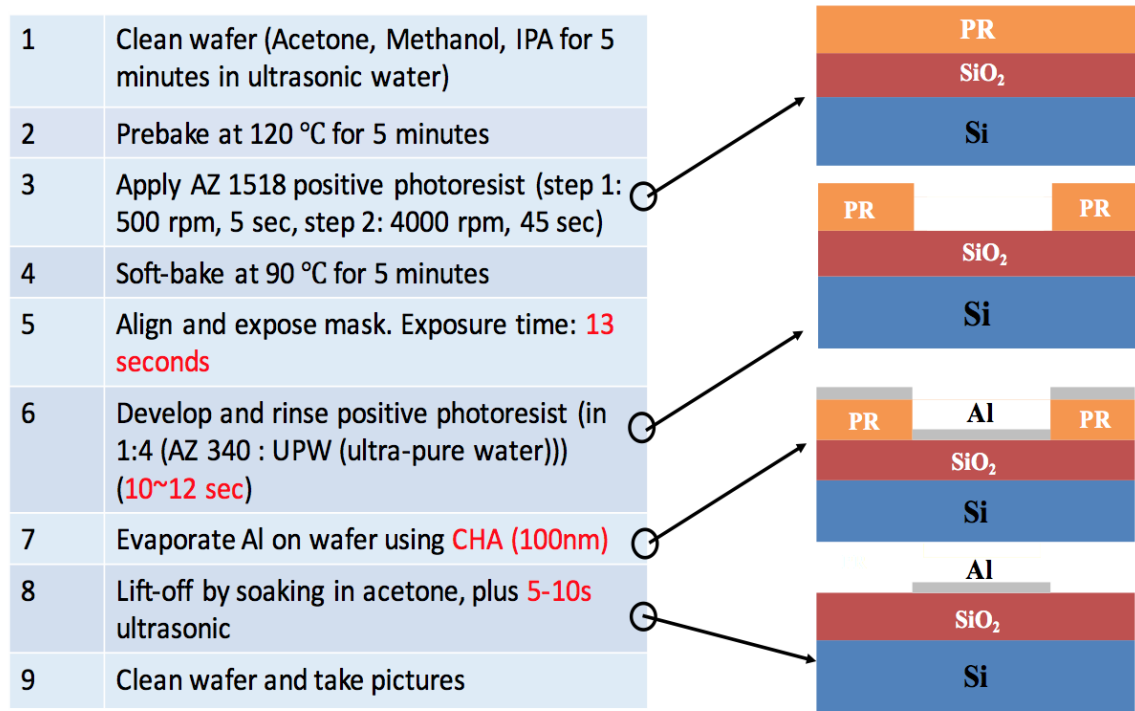


Fig. 2.7. The work flow for the fabrication of test devices using lift-off process. Typical cross-section of the devices is plotted beside each important fabrication step.

Next, 100nm Al is deposited on the wafer using e-beam evaporation (CHA e-beam evaporator). The deposition rate is $3\text{\AA}/\text{s}$. After Al deposition, the sample is soaked in Acetone until all the Al deposited on the photoresist is peeled off. During the soaking, the beaker that contains the wafer is placed in ultrasonic water bath for 5 - 10s which helps to lift-off the unwanted metal. Finally, the wafer is cleaned in Methanol and water for a while, and then dried by nitrogen.

Fig. 2.8 shows the pictures of the final fabricated devices taken by optical microscope. As indicated by the figure, the shape and size of devices are within the parameters that we designed and expected. The voids and reservoirs with different

radii are defined correctly by the fabrication, and have clearly resolved features. The line widths are slightly smaller than designed, which may be due to the diffraction of the UV light during the exposure step. The thickness of the resistors is also measured using profilometer (P-7), as shown in Fig. 2.9. The thickness of the devices is around 110nm, which is a little bit higher than designed value, but this discrepancy appears to only have a negligible influence on our final results.

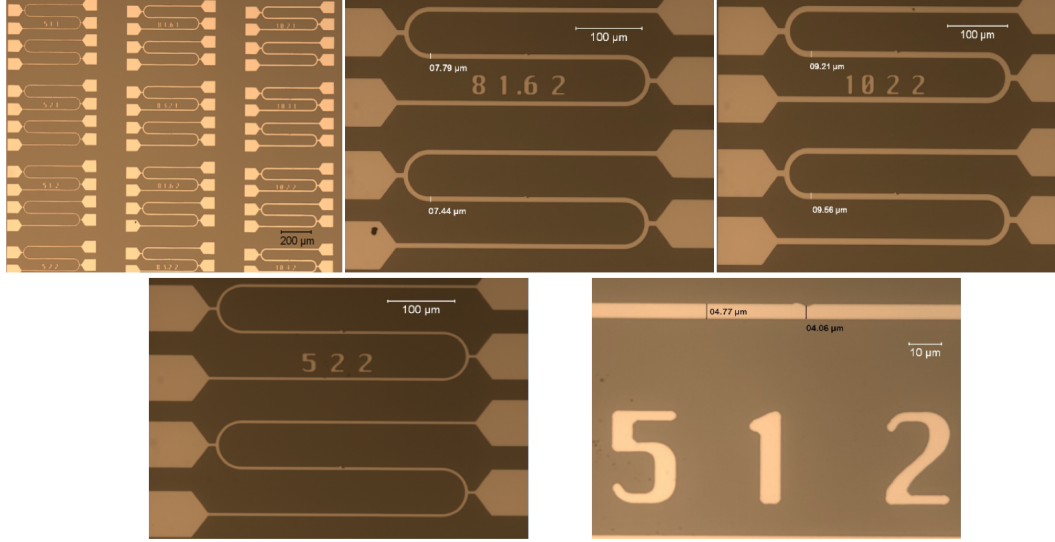


Fig. 2.8. Finished devices at various magnifications, as imaged via optical microscope.

2.2.3 Characterization: Thermal Reflectance Imaging System

The test devices are characterized using Thermal Reflectance Imaging (TRI) system [74] to analyze the change and distribution of temperature over the whole device. The main principle of TRI is illustrated in Fig. 2.10(a). An electrical square wave signal is input into the test line, and the temperature of the device is increased accordingly, which in turn changes the reflectance of the metal resistors. By taking pictures of the devices at the peak and valley of the reflectance function using CCD,

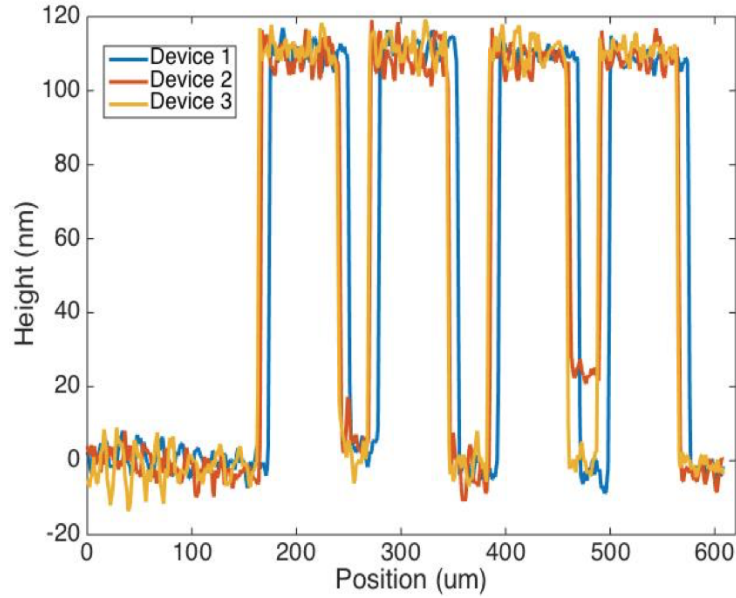


Fig. 2.9. Measured thickness of three different devices using Profilometer (P-7). The resolution of P-7 is within 5nm.

the changes and distribution of the temperature over the test line can be calculated by making difference of these two pictures.

Figure 2.10(b) shows a schematic of the TRI system, which includes signal generation, illumination, detection, electrical measurement systems. Electrical square wave signals are triggered and applied to the device under test. At the same time, the voltage and current (and thus resistance) of the devices is measured using four probe measurements, and fed into the oscilloscope for monitoring. These device are illuminated by a LED, and the reflected light is detected by the CCD of an optical microscope. Triggering and detection are synchronized by the computer software to ensure that the images at the peak and valley of reflectance are measured correctly. Due to the thermal expansion of the objective of optical microscope and mechanical vibration of the sample, the image of the device may sometimes be out of focus, particularly over long measurement times. To eliminate this problem, a movable stage controlled by a motor is used to maintain focus automatically.

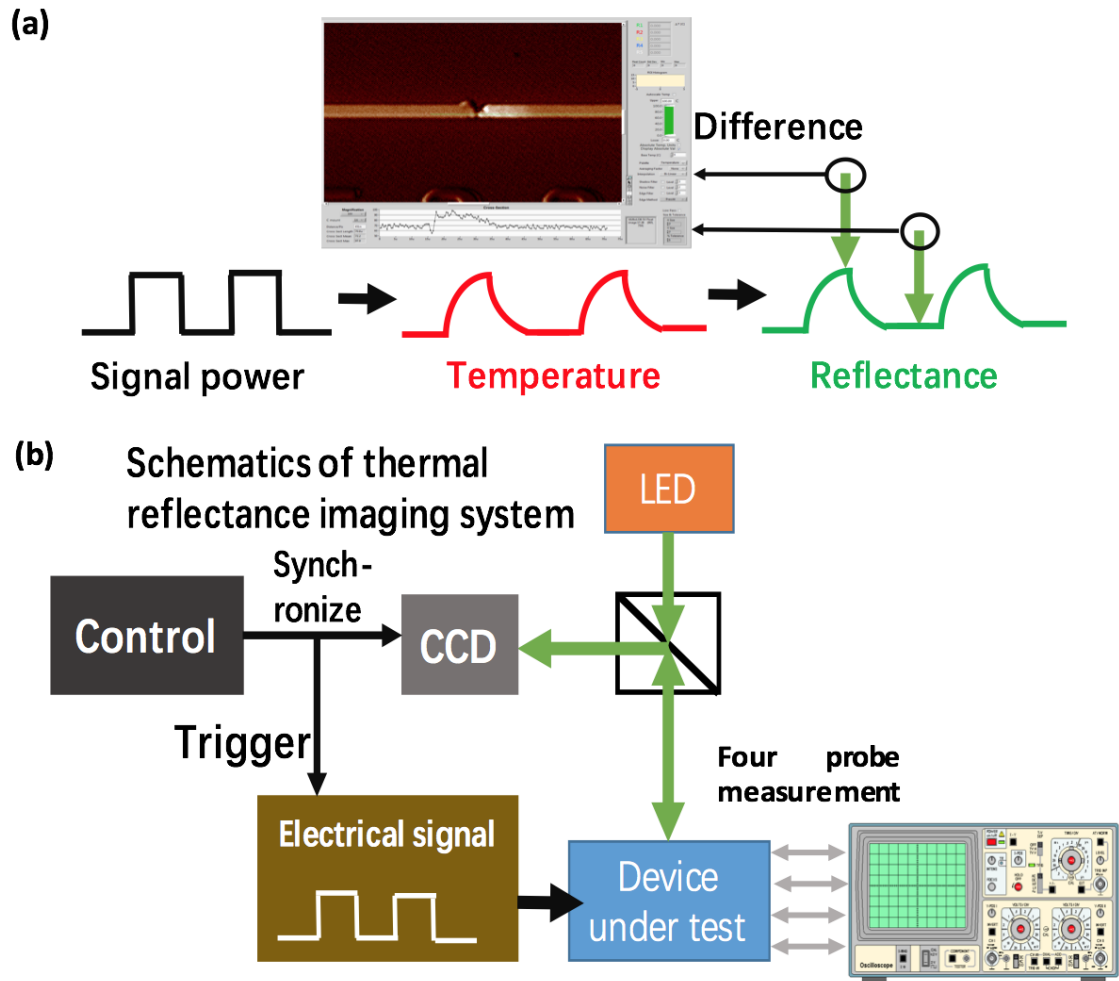


Fig. 2.10. (a) Schematic of the principle of thermal reflectance imaging (TRI). Input is electrical square wave signal, the temperature and reflectance of the device is changed according to the electrical signal. Images at high and low temperature is taken and made a difference. The differential image shows changes and distribution of the temperature. The inset shows the user interface of the TRI system software. (b) Schematic of thermal reflectance imaging system. A LED light is used to illuminate the device, and a CCD is used to detect the reflected light from the device. A computer synchronizes the triggering of electrical signal and detection of reflection. The current and voltage of the devices the monitored by the oscilloscope using four probe measurement.

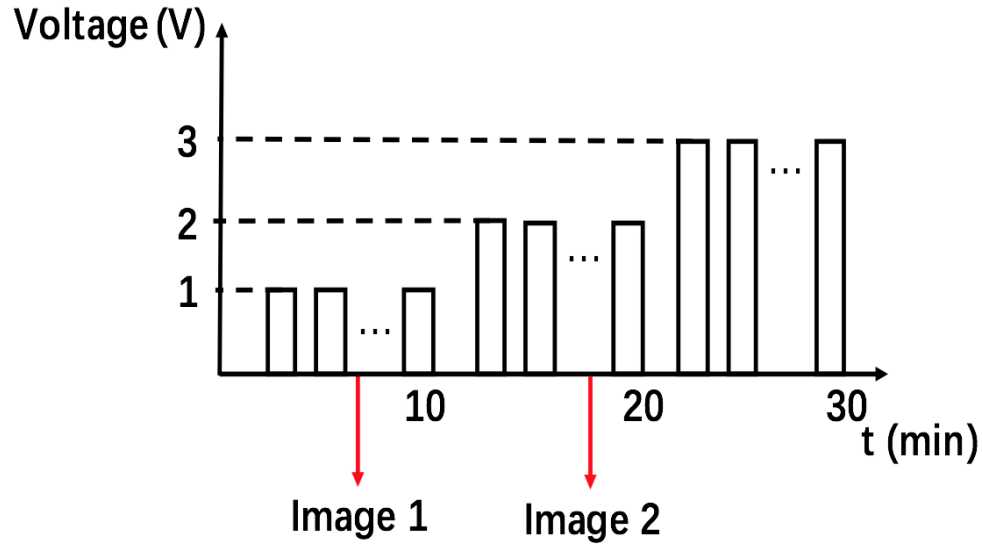


Fig. 2.11. Schematic of electrical square wave form applied in the TRI measurement.

As for the square wave form used in the characterization: a 1ms periodicity with 10% duty cycle is chosen for better thermal imaging. To get images with high quality and good signal to noise ratios, every single thermal image is taken by averaging all the images in a 10-minute duration window. The magnitude of the square pulses can also be controlled arbitrarily. The voltage is thus increased linearly to a high enough value to cause electromigration on the test line after a reasonable amount of time (on the order of minutes to hours).

2.3 Results and Analysis

2.3.1 Results for electrical polarity 1

The structure '5 2 2' ($5\mu\text{m}$ line width, $2\mu\text{m}$ void/reservoir radius, with void and reservoir) is tested in the TRI setup by increasing the current gradually from 0A to 0.12A (using current source), as shown in Fig. 2.12. Positive voltage is applied on the upper contact pad. One thermal image is generated for each current magnitude,

and total 41 images are produced in this test. The figure shown in Fig. 2.12(a) corresponds to image No.34, which illustrates the typical temperature distribution over the whole device. The temperature near the void is higher than other places on the test line, due to the higher current density near the neck of the void, as expected. As shown in Fig. 2.12(b), the resistance increases gradually with the voltage, which is partially due to the self-heating of the structure. Increasing the temperature with Joule heating will thus also increase the resistivity of Al, particularly on an insulating SiO_2 substrate. The corresponding temperature coefficient for Al is 0.00429 per $^\circ\text{C}$. The electromigration, such as the formation of little voids will increase the resistance as well. We will obtain further insight into this phenomenon in later analysis. Additionally, when the current increases beyond 0.12A, the test line is broken at the lower pad (with negative voltage), and no current can flow through the device.

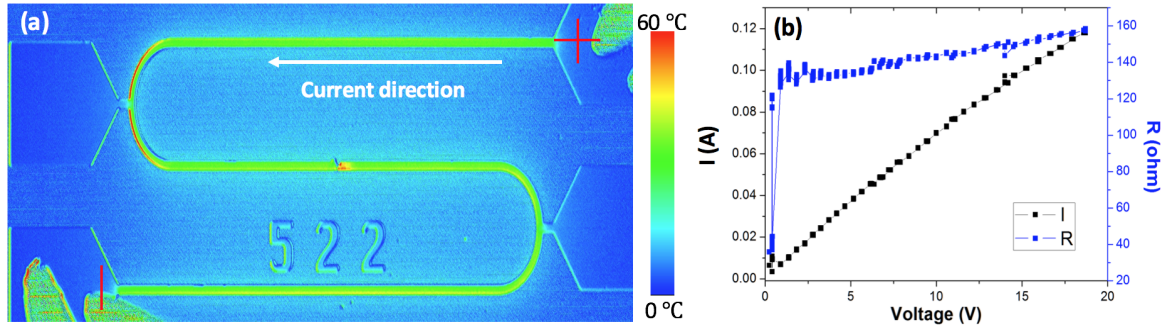


Fig. 2.12. (a) Temperature distribution (image No.34) over the whole serpentine test line with structure '5 2 2'. The plus and minus sign in the figure indicates the polarity of the voltage, and the arrow shows the current direction. (b) Change of current (black line) and resistance (blue line) with voltage.

Qualitatively, the changes of the distribution of temperature over time is illustrated in Fig. 2.13. In terms of the void, the areas with high temperature (red area) spread out gradually from the void, and the average temperatures decrease. This

behavior arises from the formation of little voids near the void, which reduces the effective reflectance. After image 38, the test line is broken, so no current flows. Thus, the temperature shown in image 39 is dramatically reduced. One interesting thing found is that there forms a hotspot near the pad right before the device fails, and, as mentioned above, the test line finally breaks at the padm but not the void. Thus, even though the void has higher temperature than the contact pad, it survives for a longer time, which may be due to the self-healing effect.

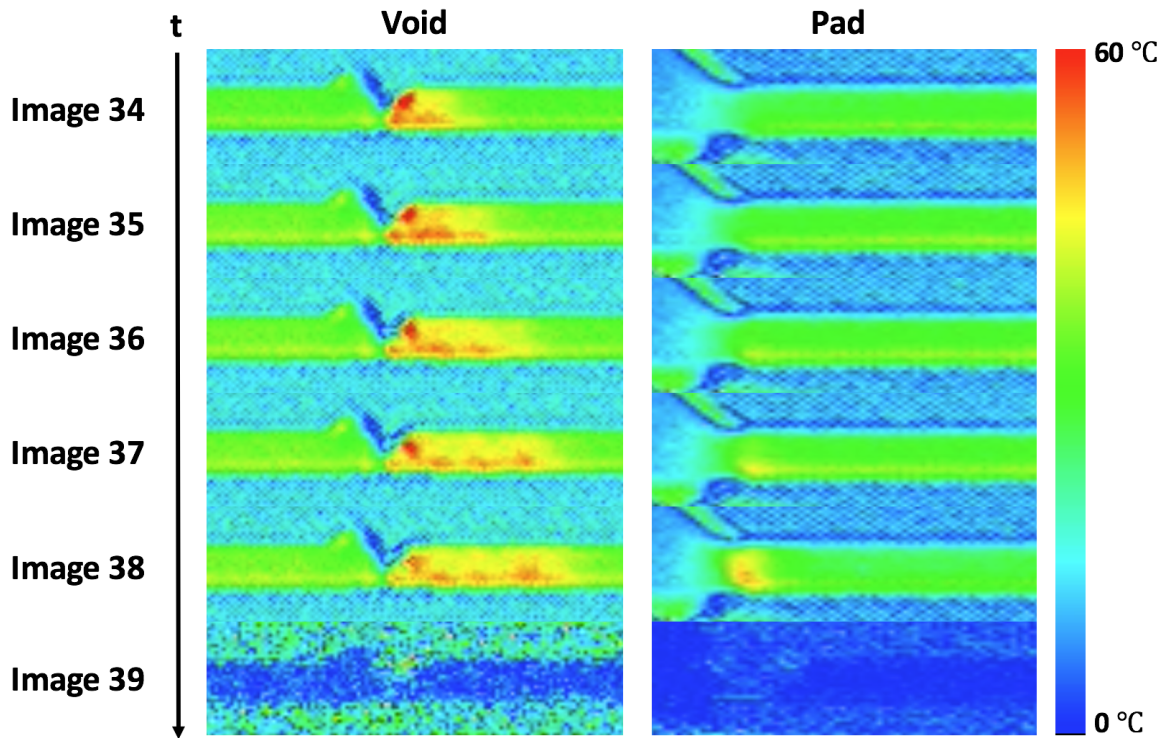


Fig. 2.13. Changes of temperature distribution over time (from image 34 to 39) near the void (left) and pad (right)

Optical images of the device after the testing are taken at high magnification (100 \times), as shown in Fig. 2.14. Some little voids are formed only at the right of the void. These voids actually reduces the effective reflectance of areas around them which is reflected in the decreasing of temperature in the experiment as mentioned

above. The picture of the pad clearly shows the broking, and hillock-like structure is formed on the line.

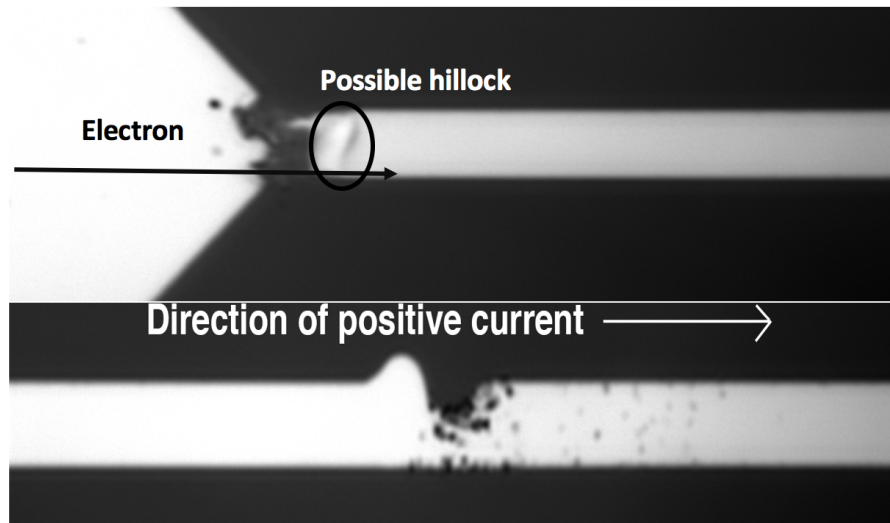


Fig. 2.14. Pictures with high magnification ($100\times$) of void and pad after the test taken by optical microscope. Some little voids are formed near the void, and possible hillock formed at the pad.

To analyze the results quantitatively, the changes of temperature with time is illustrated in Fig. 2.15 for the void. Six areas around the void is selected, and the average temperature over them is calculated. The temperatures of them all increase with time before image 35. However, boxes closer to the void increase faster due to higher current density. Right before the break down of the device (image 39), their temperatures all decrease quickly. In this scenario, the temperature of box that is closer to the void reduces earlier. According to the above conclusion that the reduction of the temperature is due to the formation of little voids, the voids first form near Box1 and then gradually evolve to the right (from Box2 to Box4). In this case, the reduction of the temperature may become a sign that predict the degradation of the device due to the electromigration. As for Box 5 and 6, they nearly overlap with each other since they are on the line that is far away enough from the void. Thus, the temperature of them may be regards as the average temperature of the whole device.

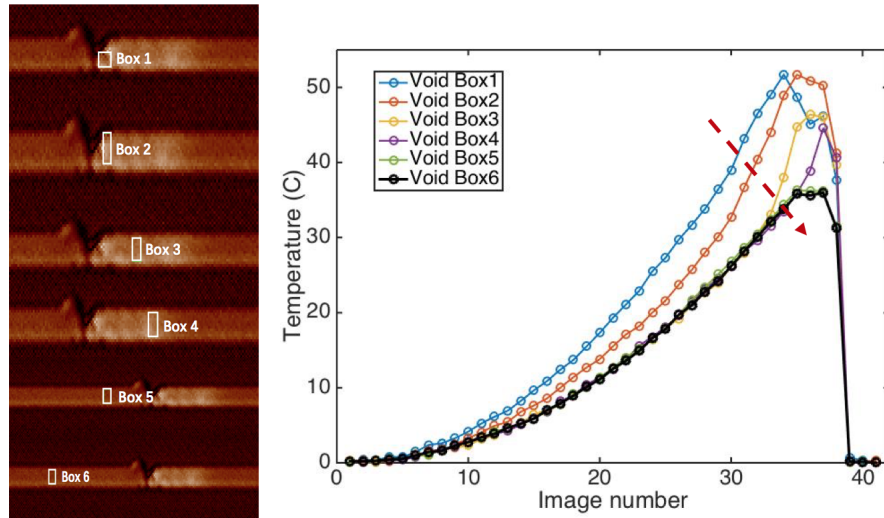


Fig. 2.15. Changes of temperature at six different areas around the void with time. The temperature is the average temperature over the selected boxes which are shown in the left. The increasing of image number corresponds to the increasing of time, and each image takes 10 minutes.

In terms of the case for the pad, we can get similar results as shown in Fig.2.16. However, the temperature is smaller than that around the void. Interestingly, for Box2 which is right on the hotspot, its temperature first is smaller than the areas on the line that is far away from the hotspot (Box 3 and 4). But its temperature increases dramatically right before the break down, and reaches the maximum point at image 38. The relatively high temperature finally causes the disconnection between the contact pad and the line. As indicated in Box1 (blue line), the temperature on the pad is much smaller than that on the line.

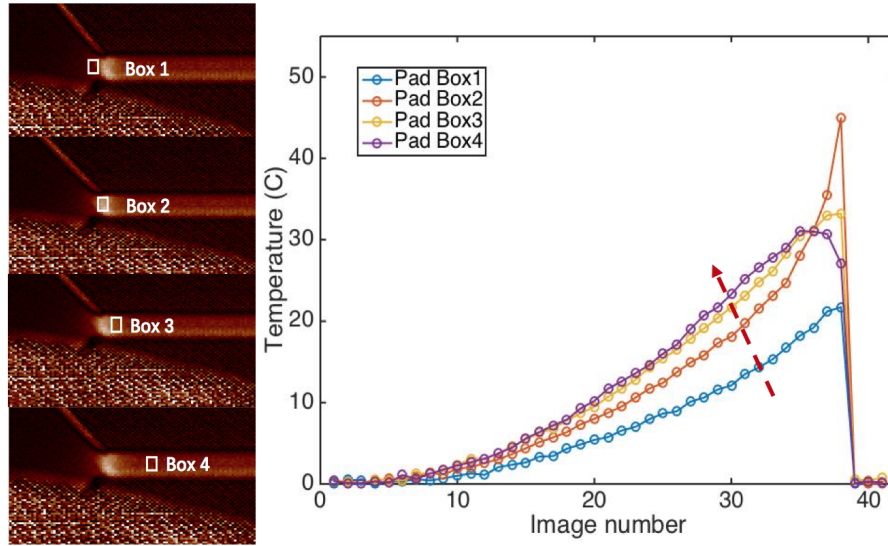


Fig. 2.16. Changes of temperature at four different areas around the pad with time. The temperature is the average temperature over the selected boxes which are shown in the left. The increasing of image number corresponds to the increasing of time, and each image takes 10 minutes.

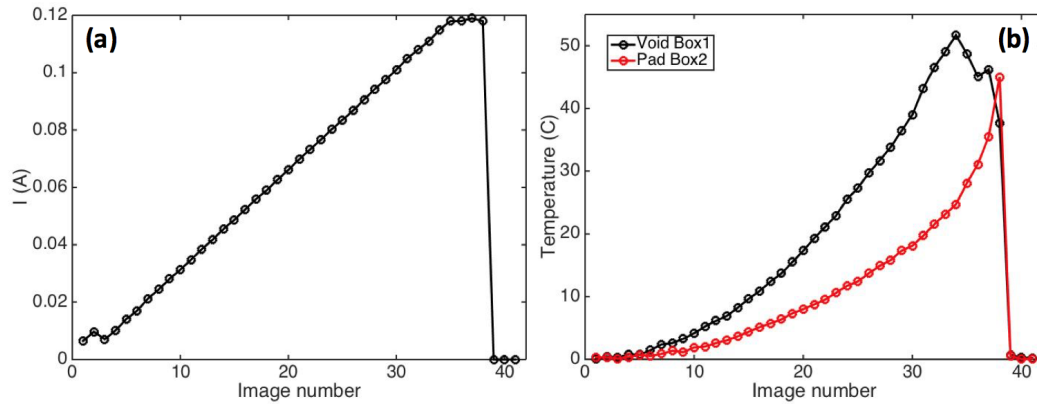


Fig. 2.17. Change of (a) the current and (b) the temperature of void (black line) and pad (red line) with time

To get more details into the reasons about the changes of temperature, Fig. 2.17 shows the correlation between the current and the change of temperature with time. The current increases linearly, but one should notice that, after image 35 the current

reaches maximum value limited by current source, and keeps constant afterwards. But the temperature of void drops down after image 35, which indicates the formation of little voids around the void. Intriguingly, the temperature of void and pad increases nearly quadratically which may relate with Joule heating, I^2R . To examine the relationship between Joule heating and the actual temperature of the device, they are plotted together in Fig. 2.18. As expected, the temperature increases nearly linearly with Joule power. However, there is little deviation which may be caused by the electromigration. Especially, when the current is constant, the void temperature drops dramatically in stead of keeping constant value. In contrast, the pad temperature increases exponentially. Also, the curves for void and pad have different slope, possibly because they have different local resistance. The void which has narrower width may have higher local resistance, while the pad is much bigger and the resistance is lower.

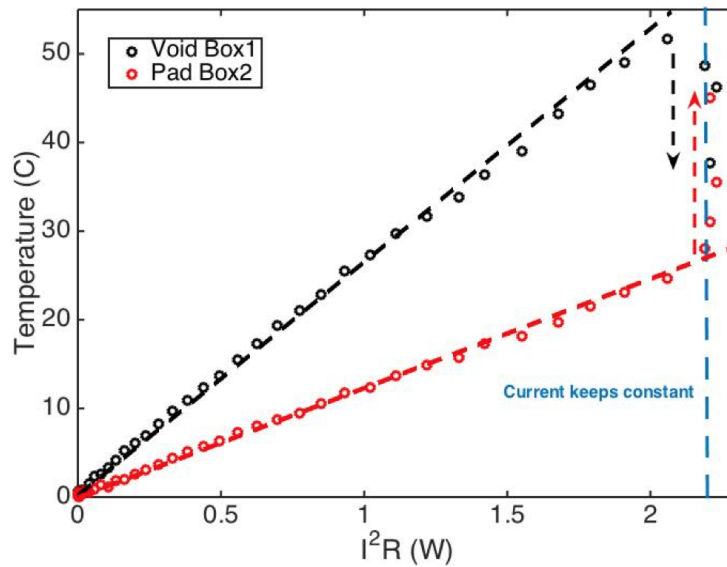


Fig. 2.18. Changes of the temperature for the void (black dots) and pad (red dots) with the power I^2R . The dashed lines in the figure are added for guidance only.

As the temperature of the test line increases, its resistivity will increase as 0.00429 per $^{\circ}\text{C}$. Fig. 2.19 shows the correlation between resistance and temperature. After

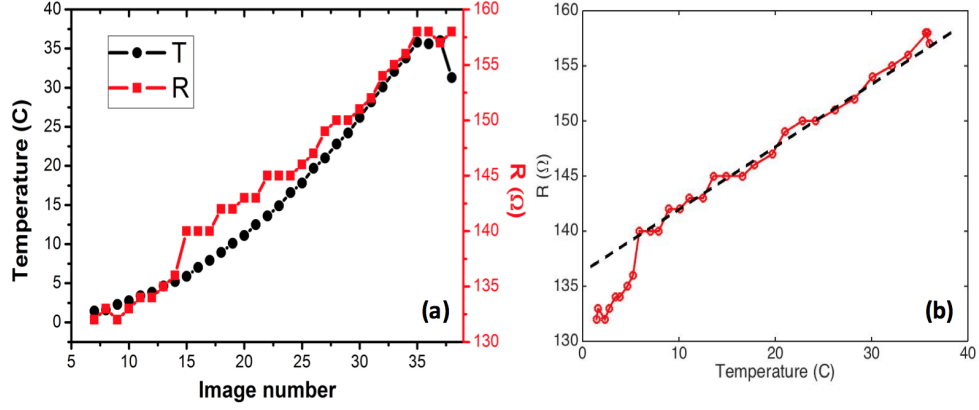


Fig. 2.19. (a) Changes of temperature (black line) and resistance (red line) with time. (b) The dependency of resistance on the temperature. The black dashed line shows the slope of the increasing of resistance due to the temperature with temperature coefficient 0.00429 per $^{\circ}\text{C}$. The temperature is the averaged temperature of void Box6 which is nearly the average temperature of the whole device.

image 35, the current (and thus the Joule heating power) keeps nearly constant, so the temperature and resistance also have little change. As shown in Fig. 2.19(b), the increasing of resistance nearly follows the rate of resistivity increasing due to Joule heating. Thus, the change of resistance is mainly caused by the Joule heating.

From the changes of the temperature distribution over a line near the void (Fig. 2.20), we can see that initially (image 22 - 24) the temperature increases gradually due to Joule heating, and the temperature at the void is bigger than that on the line by over 10°C . However, after image 35, the temperature slowly goes down, and there is even a temperature dip at the void. This may be potentially caused by the formation of little voids due to the electromigration, since the temperature would otherwise keep constant under static current. Also, the difference of temperatures between the void and other places on the line gradually reduces, and the high temperature regions starts to spread out to wider area which we have seen previously (Fig. 2.13).

As for the changes of temperature around the pad, something is found, as shown in Fig. 2.21. From image 35 to 37, the temperature on the line far away from the hotspot does not change, while that around the hotspot increases gradually. For image 38

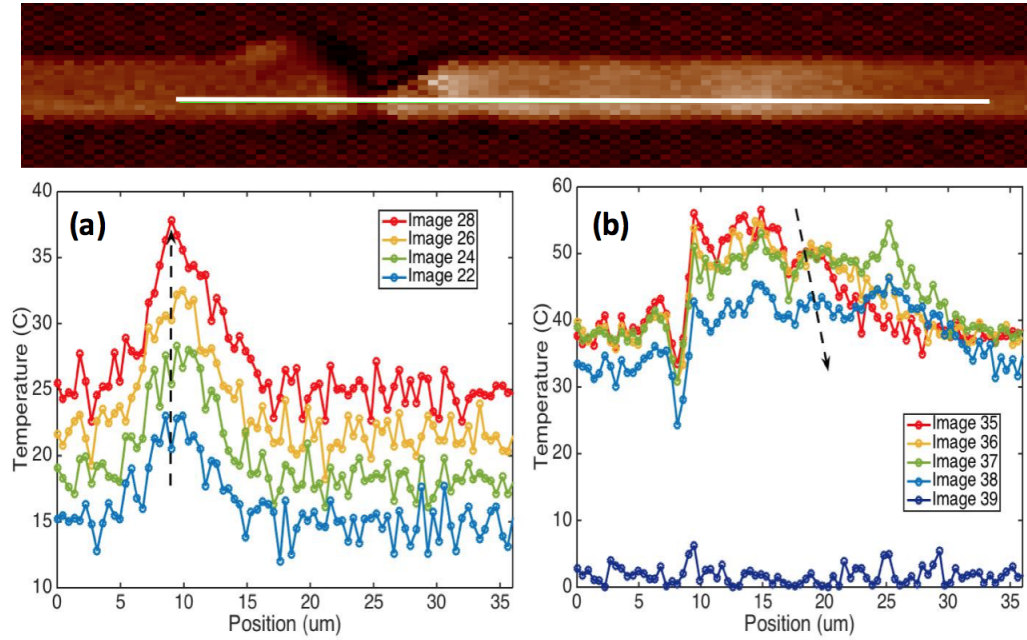


Fig. 2.20. The change of temperature distribution along a line near the void for images (a) 22 - 24 and (b) 35 - 39. The cross section is shown at the top for reference.

(right before the device failure), the temperature of the hotspot increases to nearly 50°C , and the temperature on the line decreases a little bit. The temperature on the pad is always much smaller compared with that on the hotspot, which generates high temperature gradient. One possible reason about the break-down at the pad is that, since the temperature and current density on the hotspot is much bigger than that on the contact pad, the electromigration rate at the hotspot is larger. Also because the contact pad connects to the cathode of the circuit, electrons move from left to right. Therefore more atoms leave the hotspot than that come in, which leads to a net atoms flux moves out of the hotspot. Gradually, the contact pad is disconnected with the test line which causes device failure. This may also explains why the failure is often observed at the cathode pad rather than the anode [44]. As for the anode end, the temperature gradient leads to the net atoms flux towards the contact pad which even tightens the connection between the pad and the test line.

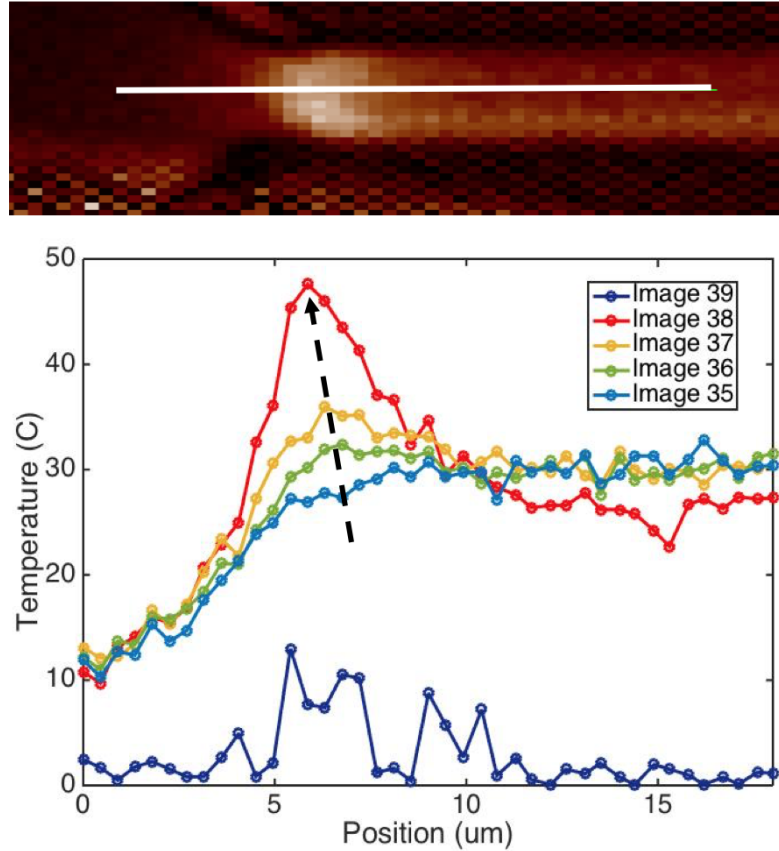


Fig. 2.21. The change of temperature distribution along a line near the pad for images 35 - 39. The cross section is shown at the top for reference.

In conclusion, the formation of voids due to the electromigration is observed which is reflected in the decreasing of the temperature around the void. The increasing of the temperature and resistance of the device is mainly caused by Joule heating. Finally, the test line fails at the cathode contact pad which is frequently observed in electromigration experiment. The failure is found to be mainly due to the high temperature gradient between the pad and the interconnect.

2.3.2 Results of reverse polarity

Due to the asymmetry of the '5 2 2' structure, it is necessary to examine the influence of the other polarity. Also, this will help us find out whether the device will all fail at cathode pad. In this scenario the positive voltage is biased at the lower pad as shown in Fig. 2.22. The temperature around the void is also much higher than other places, and the high temperature at the upper edge of the line is due to the fabrication defects which leaves large voids. Since the probe tip is disconnected with the contact pad when the voltage is around 9V during this experiment, after reconnecting the probe tip, there leaves a zig-zag distortion on the I-V curve (Fig. 2.22 (b)). If we ignore the defect, the resistance increases gradually with voltage which has been shown to be mostly due to the Joule heating. After 14 V, the device failure happens at the void in this time. The discrepancy between previous test may help us get deep insight into the essence of the device failure and electromigration. Fig. 2.23 qualitatively shows the changes of the temperature near the void over time. The hotspot locates near the right of the void and gets bigger and bigger with higher magnitude as time goes on. After image 31, the interconnect breaks as shown in image 32.

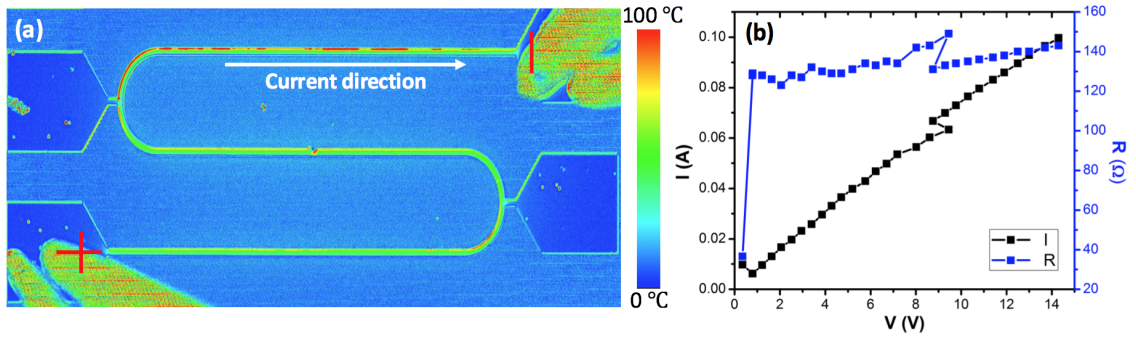


Fig. 2.22. (a) Temperature distribution (image No.31) over the whole serpentine test line with structure '5 2 2'. The plus and minus sign in the figure indicates the polarity of the voltage, and the arrow shows the current direction. (b) Change of current (black line) and resistance (blue line) with voltage.

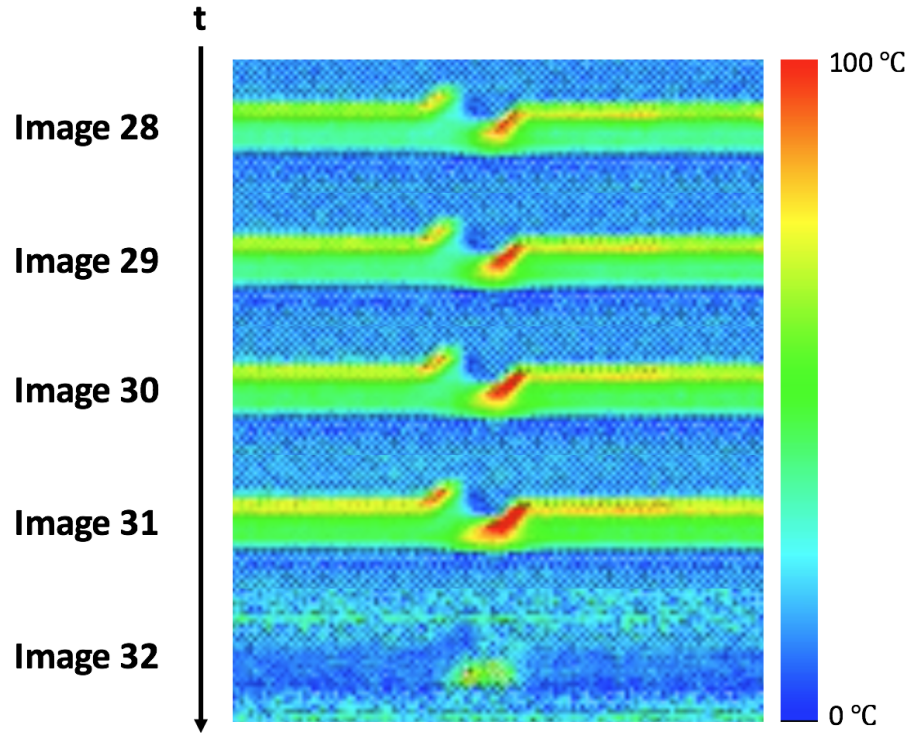


Fig. 2.23. Changes of the temperature distribution over time (from image 28 to 32) near the void

The device actually fails very quickly at the beginning of the averaging of image 32. After the break-down, the temperature on the breaking edges kept high and decreases gradually which leads to high averaged temperature at break-down point (image 32). The pictures of the device after the failure is taken by optical microscope as illustrated in Fig. 2.24. Different from previous study, there is no visible voids formed near the void. But there is a hillock at the right edge of the void which is similar to the results of cathode pad. Intriguingly, the hillocks are all formed at the downstream of the electron flow. In addition, there are no visible defects formed elsewhere along the test line.

Quantitatively, the change of temperature with time around the void is shown in Fig. 2.25. Three areas are picked around the void. Box 1 and 2 are right near the hot spot, and the Box 3 is on the test line and far away from the void which represents the

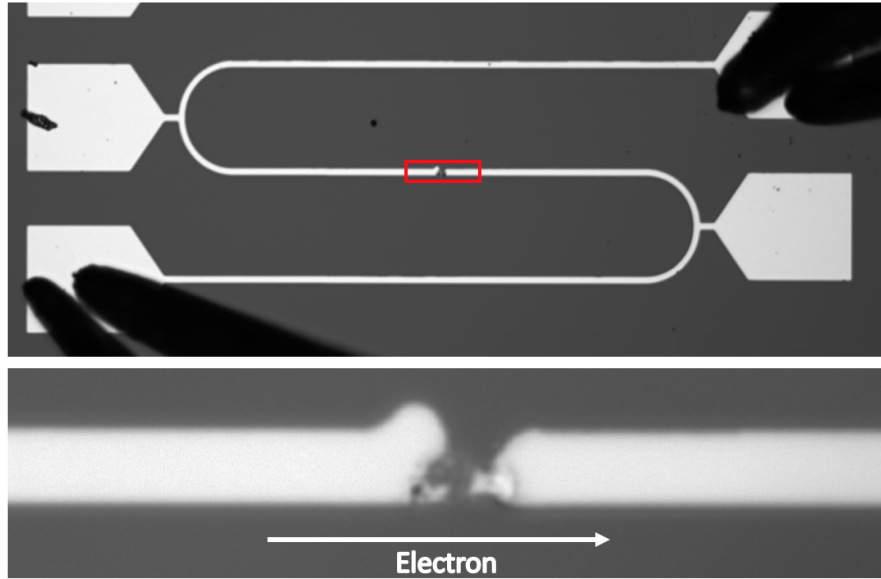


Fig. 2.24. Pictures with low ($10\times$) and high ($100\times$) magnification of the whole device (upper part) and the void (lower part) after the test. Taken by optical microscope. The red rectangle shows the zoom-in area of the high magnification near the void. The arrow shows the moving direction of electrons.

average temperature of the whole device. As expected, the temperatures of them all increase with time, and the temperature around the void (red line) is much higher than that of the other places on the line (black line). Also, the temperature keeps increasing without dropping before the failure, with the maximum temperature reaching as high as 90°C . This is much different from previous experiment, since no little void is formed near the large void. Also, the failure voltage (14 V) is lower than previous one (18 V), which means the device fails much faster and time is not long enough for the formation of little voids.

The relationship between the temperature and the Joule heating power shown in Fig. 2.26 indicates the main cause of temperature increasing. The current in this time increases linearly with time and does not saturates which is expected from the output of the current source in the experiment. From Fig. 2.26(b), the temperature of the whole device (Box3, black dots) increases linearly with Joule heating as predicted by

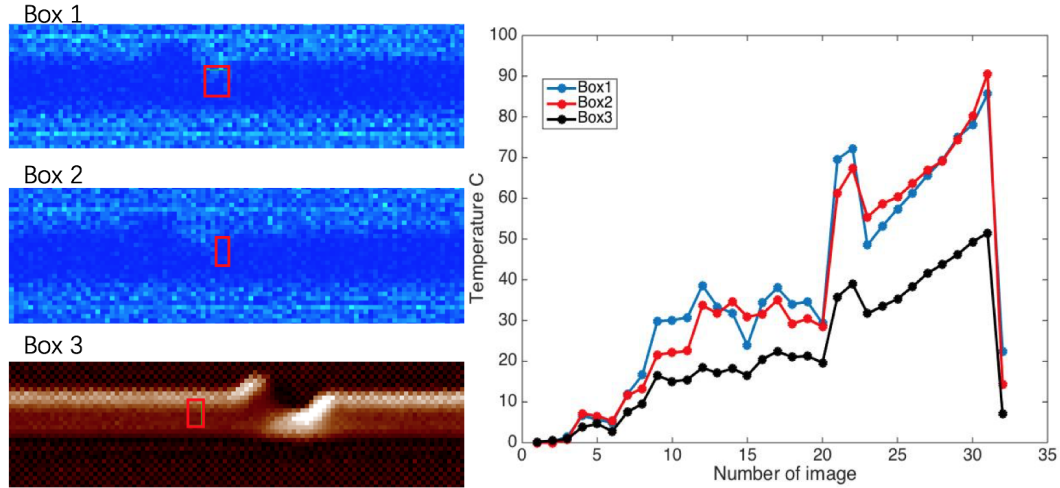


Fig. 2.25. Changes of averaged temperature at three different areas around the void with time. The temperature is averaged over the selected boxes which are shown in the left. The increasing of image number corresponds to the increasing of time, and each image takes 10 minutes.

the theory. However, for the temperature near the void, there is some discrepancies. The temperature of Box1 (right below the void) increases also linearly but with a little bit higher slope. This may be due to the higher local resistance around the void which has nearly half width compared with the bulk line. As for Box2, it first increases linearly, but has large deviation at the end two points. The maximum deviation can be as large as 10°C . The much faster increasing of temperature for Box2 is similar to the hotspot near the cathode pad, which may need further investigation. One possible reason may be because the local resistance increases much faster than the global resistance which increases the Joule heating power.

To figure out the causes for the increasing of the resistance, the dependency of the resistance on the temperature is illustrated in Fig. 2.27. As shown in the figure, the resistance increases nearly linearly with the temperature following the black dashed line. However, compared to the slope of the resistivity of Al with respect to temperature expected from the literature (0.00429 per $^{\circ}\text{C}$), the actual rate at which resistance increases is slightly lower. One possible reason is that Box3 is somewhat closer to the

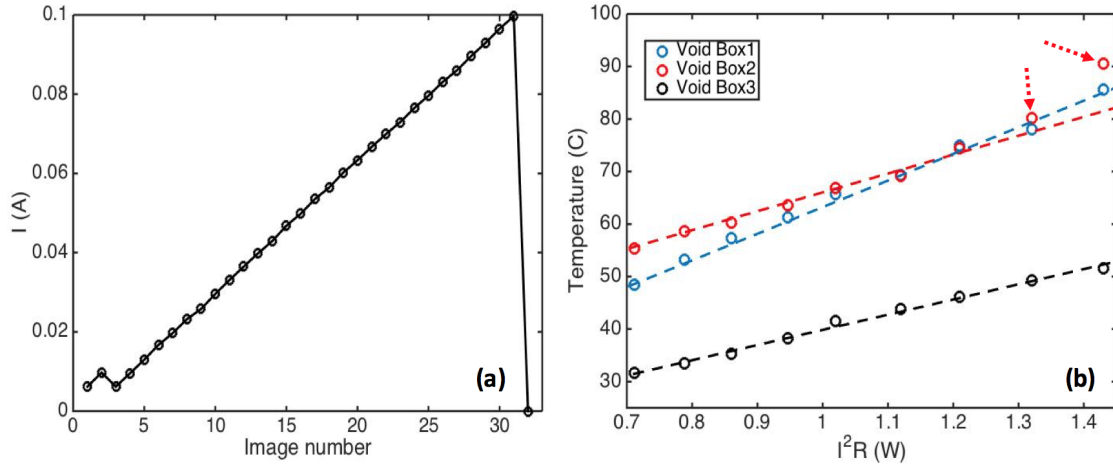


Fig. 2.26. (a) Change of the current with time. (b) Dependency of the temperature for three areas around the void on the power I^2R . The dashed lines in the figure are added for the guidance of the linearity. The data points are all after image 23.

void, which has a temperature greater than the actual whole device temperature. In this sense, the main cause for the resistance increase is still temperature related. It appears that Joule heating increases the temperature and thus the resistance of the whole device.

From the change of temperature distribution along a line around the void in Fig. 2.28, the temperature both on the void and the test line increases gradually. As expected, the maximum temperature of the void is nearly 70°C greater than that on the line, which produces a high temperature gradient. As mentioned in the last section, the temperature gradient leads to a net atom flux that leaves the area around the void. This phenomenon accelerates the breakdown of the void. Interestingly, even after the failure of the device (image 32), the temperature around the void is still significantly greater than that of the ambient, since it was strongly heated, and takes a long time to cool down.

In conclusion, for the reverse polarity case, the device fails at the void, possibly due to the large temperature gradient around the void. The discrepancy between these two polarities is related with the relative position of the reservoir and void,

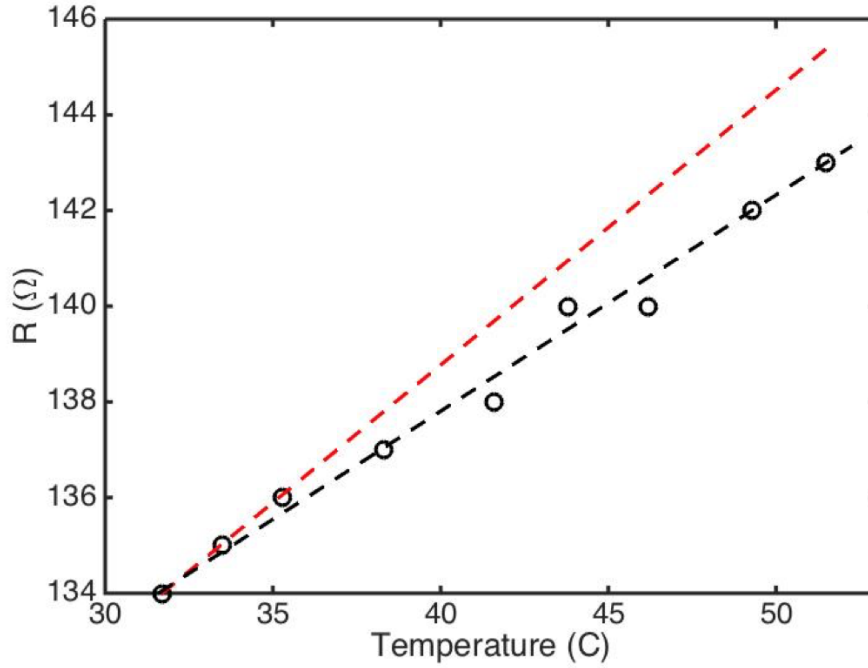


Fig. 2.27. Resistance versus temperature. The red dashed line shows the slope of this relationship predicted by literature: a temperature coefficient of 0.00429 per °C. The black dashed line is added to guide the eye. The temperature is the averaged temperature of void Box3, which is nearly the average temperature of the whole device. The data points are all taken after image 23.

which makes the void easier to break down for one polarity than for the other. Joule heating is still the main cause of the increasing of the temperature and resistance in the test line, until electromigration becomes strongly evident near the very end. Still, further tests on more devices need to be performed to reproduce and extend the conclusions drawn from our initial results.

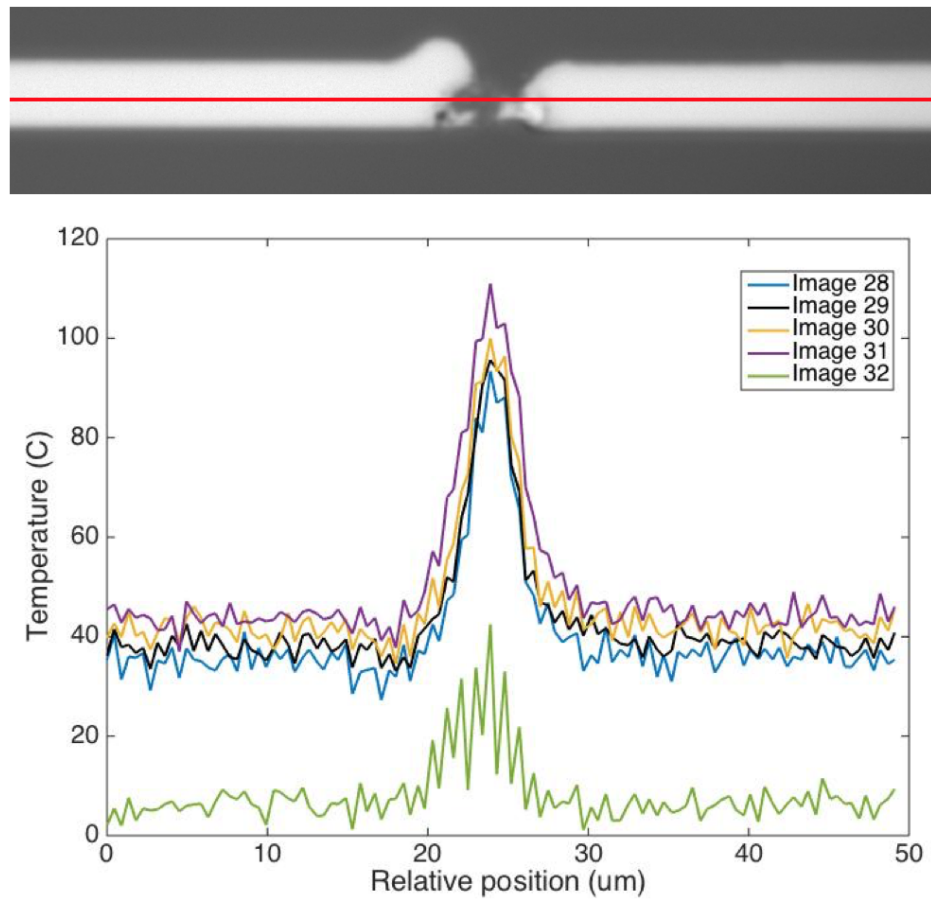


Fig. 2.28. The change of temperature distribution along a line near the void for images 28 - 32. The cross section is shown at the top for reference.

3. CONCLUSIONS AND FUTURE WORK

3.1 High Temperature Selective Solar Absorber Based on Si Substrate

Creating selective solar absorber systems using simple, stable structures capable of surviving high temperatures is essential for widespread adoption of efficient, high-temperature solar thermal technologies. In this thesis, semiconductor-metal tandem selective solar absorbers based on commercially available Si wafers have been fabricated using well-known sputtering and evaporation techniques. They are characterized both at room temperature using a spectrophotometer, and then at high temperatures by a custom-built Direct Thermal Emission Spectrum Measurement System. The fabricated devices show sharp selectivity with cutoff wavelength around $1.1\mu\text{m}$ at room temperature, as expected for a double-side polished intrinsic silicon wafer. The Si_3N_4 AR coating introduced substantially increases the absorption of visible and near-infrared solar photons with an absorption peak around 550nm. As predicted by our model, high selectivity of the devices is obtained at temperature as high as 490°C , and the structure is demonstrated to be mechanically and thermally stable even at slightly higher temperatures (up to 535°C). Increased free carrier absorption and lattice absorption of Si is observed at elevated temperatures, which rises thermal re-radiation dramatically.

To mitigate thermal re-radiation experienced at high temperatures, a thin Si film-based selective solar absorber has been computationally designed and optimized. As Si thickness decreases, the thermal emission reduces dramatically which increases the solar thermal transfer efficiency. However, thickness must be at least several microns to maintain sufficient absorption of visible and near-infrared photons. An optimal Si_3N_4 thickness is found to be 80nm and demonstrated to be insensitive to the Si thickness and solar concentration. Thinner Si layers, due to their lower thermal

emission, also have the distinct advantage that they are less sensitive to the solar concentration. In this way, the optimal Si thickness decreases at lower concentrations. A device with sub- $20\mu\text{m}$ Si thin film is predicted to exhibit high efficiency (60-70%) at a wide range of solar concentration (20 - 100 suns). As demonstrated by Yi Cui *et al.* [23], thin-film Si substrates exhibit excellent mechanical stability and flexibility. Therefore, combining a simple thin-film Si structure with mechanical and thermal stability could enable a wide range of applications in solar thermal energy harvesting and conversion systems.

In the future, the Si thin film based selective absorber merit further investigation in both simulation and experiments. From a computational perspective, future studies could include further global optimization, higher-temperature designs, and multi-layer anti-reflection coating design and optimization. Experimentally, it would be appropriate to fabricate the selective absorber using thin Si film substrate as in Yi Cui's recent work [23], and then to characterize it both at room and high temperatures. The mechanical stability and reliability of the selective absorber after multiple high temperature cycles should also be studied. As part of this goal, new refractory metal material such as Ta, W, and Pt should also be considered and tested. Also, multi-layer AR coatings should also be fabricated and studied, if simulation results indicate a significant net benefit is expected.

3.2 Self-Healing Structures to Reduce Electromigration Failures

In applications where high current density is present, such as microinverters for solar energy, abrupt failure of the integrated circuits can occur from electromigration. To mitigate these challenges, a self-healing utilizing reservoir effect structure has been proposed and investigated in this thesis. A test device with serpentine structure has been designed and fabricated using lift-off process. It is characterized by a thermal reflectance imaging system originally developed by our collaborators, which has very high spatial and temperature resolution.

Since the self-healing structure is asymmetric, two opposite electrical polarities have been studied here. For the first polarity, as expected, the temperature around the void is higher than elsewhere, due to its high current density. However, for the pad, its temperature increases gradually but forms a hotspot right before the breakdown of the device. An increase in temperature and resistance of the device is found to be caused by Joule heating. The formation of electromigration nanovoids in a cluster around the artificial void is also observed. However, perhaps surprisingly, the device fails at the neck between the cathode contact pad and the test line. The failure around the cathode pad may be explained by the high temperature gradient between the pad and the interconnect, which causes net atom flux leaving the hotspot [44].

In testing with the reverse polarity, the device fails at the void, probably due to the large temperature gradient between the void and the test line. The discrepancy between these two polarities is related to the relative position of the reservoir and void and the direction of the electron wind, which makes the void significantly easier to break down at one polarity than the other. Of course, Joule heating is still the main cause of temperature and resistance increases throughout the device. However, sharp deviations of the temperature beyond the Joule heating are observed right before the device break-down, which may be related with the formation of nanovoids around the artificial void.

In the future, additional tests on more devices with both polarities need to be performed to confirm the conclusions drawn above. Other structures of particular interest include devices without void and reservoir, devices with only a void and no reservoir, as well as devices with different line width and void radius. This will help quantify the influence of line width and void radius, the reservoir effect, and the temperature gradient. Moreover, a high-throughput study of the devices using only electrical measurements to collect Weibull statistics is required to obtain definitive insight into the mechanisms of electromigration and reservoir effects in this class of devices. Such work would allow for a more quantitative understanding, by deter-

mining the precise dependence of the mean time to failure on current density and activation energy in each case.

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VITA

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