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Is approved by the final examining committee:

SAEED MOHAMMADI
Co-chair

CHEN YANG
Co-chair

LUIS M. KRUCZENSKI

KENNETH P. RITCHIE

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DESIGN, COMPACT MODELING AND CHARACTERIZATION OF NANOSCALE DEVICES

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of

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of

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LIST OF ABBREVIATIONS

FE	Field Emission
FEA	Finite Element Analysis
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
FEA	Field Emitter Array
FN tunneling	Fowler-Nordheim Tunneling
SOA	Safe Operating Area
FBSOA	Forward Bias Safe Operating Area
LB technique	Langmuir-Blodgett Technique
TCAD	Technology Computer-Aided Design
SEM	Scanning Electron Microscope
ALD	Atomic Layer Deposition
RIE	Reactive Ion Etching
DRIE	Deep Reactive Ion Etching
BOE	Buffered Oxide Etch
CMP	Chemical-Mechanical Planarization
HF	Hydrogen Fluoride
CMOS	Complementary Metal Oxide Semiconductor

SOI	Silicon on Insulator
BOX	Buried Oxide
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	N-channel MOSFET
BSIM	Berkeley Short-channel IGFET Model
DIBL	Drain Induced Barrier Lowering
RF	Radio Frequency
NVT	Nano-Vacuum Tube
IC	Integrated Circuit
VS	Virtual Source
GSG	Ground-Signal-Ground
S-parameter	Scattering Parameter
Y-parameter	Admittance Parameter
Z-parameter	Impedance Parameter
NF	Noise Figure
PSD	Power Spectral Density
M/NEMS	Micro/Nanoelectromechanical Systems
DLV	Doppler Laser Vibrometer
AM	Amplitude Modulation

ABSTRACT

Shen, Yanfei. Ph.D., Purdue University, December 2016. Design, Compact Modeling and Characterization of Nanoscale Devices. Major Professor: Saeed Mohammadi.

Electronic device modeling is a crucial step in the advancement of modern nanotechnology and is gaining more and more interest. Nanoscale complementary metal oxide semiconductor (CMOS) transistors, being the backbone of the electronic industry, are pushed to below 10 nm dimensions using novel manufacturing techniques including extreme lithography. As their dimensions are pushed into such unprecedented limits, their behavior is still captured using models that are decades old. Among many other proposed nanoscale devices, silicon vacuum electron devices are regaining attention due to their presumed advantages in operating at very high power, high speed and under harsh environment, where CMOS cannot compete. Another type of devices that have the potential to complement CMOS transistors are nano-electromechanical systems (NEMS), with potential applications in filters, stable frequency sources, non-volatile memories and reconfigurable and neuromorphic electronics.

In this work, a compact scalable nonlinear RF MOSFET model for NMOS transistors in a standard 45nm CMOS SOI technology is presented. This model employs a simple nonlinear core known as the Virtual Source (VS) model and adds parasitic elements

around it to accurately simulate the RF performance of NMOS transistors up to 40GHz. The traditional long-channel thermal noise model is replaced by a combined shot-thermal noise model for the first time to accurately predict the noise behavior of these short-channel transistors up to 40GHz. The model parameters are extracted from DC, S-parameter and noise measurements across different bias conditions and for different device dimensions to achieve a scalable nonlinear model.

In addition to CMOS modeling, silicon nanowire field emitter arrays, which yield large current densities with high reliability and low turn-on voltages are designed, and implemented. An electro-thermal simulation is performed to obtain the parameters that optimize the device performance. The silicon emitter arrays are fabricated using a self-assembled technique for the first time. Silicon nanowire FEAs fabricated with this technique are dense (~75% fill factor), highly repeatable and reproducible, and low-cost. An ungated two-terminal device and a gated vacuum transistor are fabricated in this technology and are characterized.

Various CMOS integrated NEMS resonators are fabricated and characterized. A compact model for double-clamped CMOS Silicon on Insulator (SOI) NEMS devices is constructed and implemented. The model covers both linear and nonlinear characteristics of nanoscale single gated and double gated resonators made of silicon beam of different sizes and gaps. This model can also capture the hardening or softening effects, Duffing-type response and hysteresis responses, that are observed in such devices.

CHAPTER 1. INTRODUCTION

1.1 Introduction

For novel nanoscale devices, integration with CMOS is an essential step that facilitates such advanced devices to transition from research-grade technology into the consumer market. There are generally two paths to design CMOS integrated devices. One way is to fabricate the devices first and then try to make them CMOS compatible. The other way is to design devices directly on a CMOS chip. Once the devices are made CMOS compactible, they can benefit from enormous infrastructure available for CMOS electronic manufacturing and can quickly gain high reliability and low cost status available in CMOS, leading to their good commercial prospective. After devices are ready for commercial use, there is a second complication that needs to be addressed. In an integrated circuit, there are sometimes millions or even billions of devices with different sizes and operating conditions. These devices have different parameters, which lead to different electrical performance. The decision in what type of device to use and what parameters may provide optimal performance can be addressed by device modeling. There are basically two types of device models; The FEA (finite element analysis) based models utilized in TCAD device simulation, suitable for process as well as single device level simulation to predict different real-world physical effects such as heat, vibration,

flow, EM wave, etc. They utilize the very fundamental physics principles, ranging from the very general, like Maxwell Equations or Bernoulli's Principle to the very specialized functions, such as Fowler-Nordheim tunneling equation for field emission tunneling. They employ the boundary conditions, which are set by a user, divide the whole geometry into smaller meshes and solve the physics based equations consistently for all meshes. The finer the meshes are, the more accurate the simulation is, and the more time it will take to run the simulation. Typically, this type of simulation is very computational intensive. So only a single device or a few very simple devices are acceptable at a fair accuracy if the simulation runs on a single computing platform. A few commercialized simulators are Synopsis Sentaurus TCAD, COMSOL Multiphysics, Ansys HFSS and so on. Circuit simulations, which usually composed of a dozen to millions of sophisticated electrical devices, sources, passive components, however, cannot rely on TCAD simulations as they are very inefficient in solving such a big problem. Therefore, a so-called compact model for each of the devices is needed to speed up the simulation with a reasonable accuracy.

Compact model is the bridge between devices and circuits. While partially physics based, most compact models utilize a set of empirical or semi-empirical mathematical equations to describe the device characteristics for circuit simulators. The compact model takes in the terminal input and generates terminal output information, which is based on the electrical behavior of the device, but can be extended to other characteristics such as mechanical motion, stress and heat. A simple example is an ideal resistor with resistance R. A simple mathematical function to describe the behavior would be $I = V/R$, where I is the current in the resistor when a voltage V is applied. The compact model takes in the

terminal voltage of the resistor (*V*) and output the current flowing through it (*I*). The device behavior described by compact model could be multi-domain correlated. For example, in a simple micro-cantilever as shown in Figure 1.1, mechanical domain and electrical domain are combined. The deflection of the micro-cantilever will induce the resistance change in the beam, which could be sensed by electrical instrument. If a gate is present, the electrical force between the gate and cantilever will drive the beam and the beam deflection will change the capacitance, which will further change the electrical forcing between the two. Therefore, a good compact model is able to take in the terminal information, combine the inherent dynamics to predict electrical or mechanical behavior accurately.

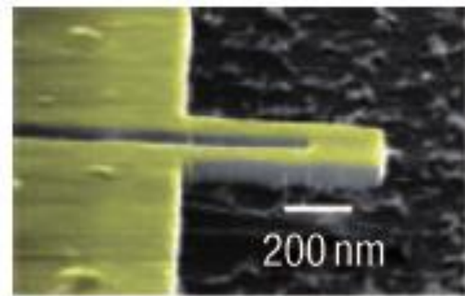

Figure 1.1. A single crystal SiC epilayer cantilever for mass sensor [1]

As modern nano-scale devices are becoming more and more sophisticated as the dimensions are getting smaller, compact models are becoming more complex since a number of physics-based phenomena need to be considered. Modern state-of-the-art MOSFET compact models usually have several hundred of parameters to take care of

various physical effects, such as short-channel effect, narrow-width effect, channel length modulation, drain-induced barrier lowering (DIBL), etc.[2].

After the compact model is developed, the circuit simulator takes all the compact models for each of the elements and the inter-connection information to solve the circuit equations iteratively using Newton-Raphson or a similar method. The circuit equations are Kirchhoff's Voltage Law (KCL) and Kirchhoff's Current Law (KVL). A good compact model needs to have the following properties,

(1) Accurate for a wide range of parameters

(2) Physics based

(3) Computationally simple

(4) Smooth enough: continuous, differentiable, even second order differentiable

Finally, a compact model needs to have good parameter initializations and limits to ensure convergence in a circuit simulation.

1.2 Compact Modeling of 45nm CMOS SOI Transistors

A comprehensive deep submicron MOSFET model that captures DC, RF and noise characteristics of transistors is of great importance for circuit designers and several such models have already been fully or partially developed [3]–[7]. Modern mainstream transistor compact models are composite type models, which take an accurate DC core model to describe the drain current characteristic and a terminal charge model for low frequency analog simulations. In order to predict high frequency (HF) behavior, an equivalent circuit is constructed and various technology-related parasitic elements are

added around the DC core model. These parasitic elements are extracted from experimental data for different geometries and biases.

Figure 1.2 is a typical example of modern transistor model. The bottom circuit in the left figure is the equivalent circuit model, which consists of a core transistor model, taking care of the drain current information and intrinsic parasitic elements, such as the overlapping capacitances, C_{gs}, C_{gd}, C_{ds}, output conductance g_{ds}, etc. and several peripheral extrinsic parasitic elements (both resistive and inductive) such as L_G, R_G, L_S, R_S, R_D, L_D, etc., which cannot be neglected at high frequency operation.

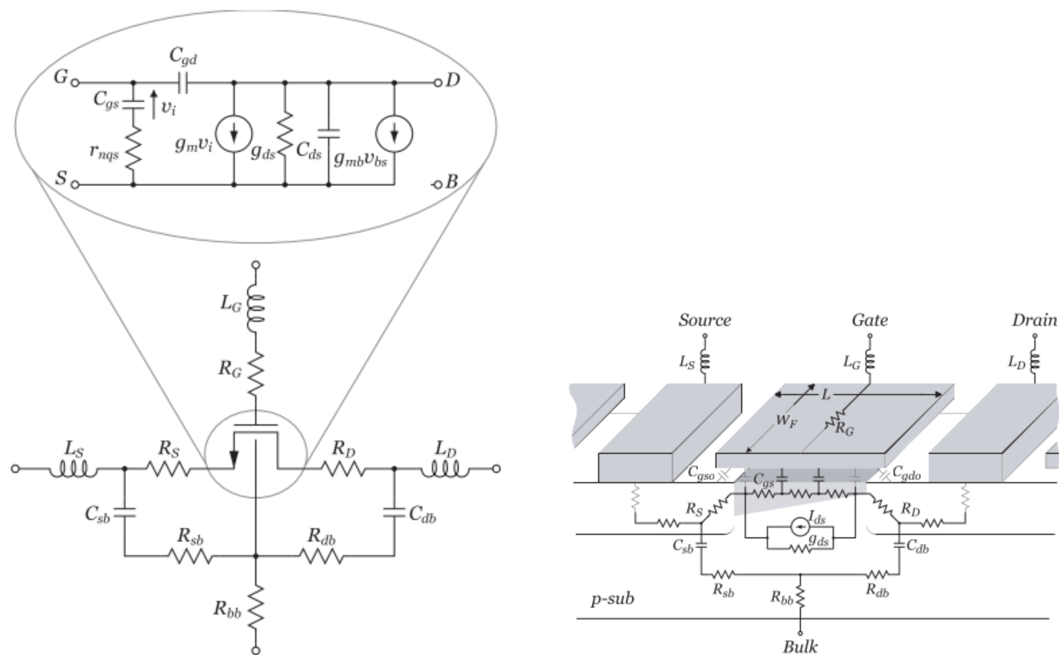

Figure 1.2. Equivalent circuit model of modern NMOS transistor [8]

The origins of the various parasitics in a single finger layout of a CMOS transistor is also shown Figure 1.2. Almost all mainstream MOSFET models provide the core part of the

model as shown in the top left figure of Figure 1.2, while semiconductor manufacturing foundries characterize their own external parasitics for their own technology and add them to these core models to achieve a complete non-linear transistor model.

Most current state-of-the-art transistor models are equivalent circuit based as discussed above. The differences are in the approaches that they employ to describe the DC model and charge model. In particular, how much physical phenomena are captured in the model may vary. Most of the models were intended for digital and low frequency applications so they often fail to capture the RF behavior accurately. With more attention towards the wireless communication market, the model vendors are forced to extend their models for HF applications. The widely used transistor models such as BSIM, and Phillips MOS Model have been shown to accurately predict the drain current behavior for deep submicron devices [3][4]. However, they usually employ hundreds of parameters to achieve such accuracy, which makes the parameter extraction process very tedious. Yet they fail to accurately capture the RF and noise behavior of modern sub-100-nm CMOS transistors. The new surface-potential-based PSP model formerly developed at the Pennsylvania State University and Philips (now at Arizona State University and NXP Semiconductors Research) has been supported by the Compact Modeling Council (now Compact Model Coalition in Si2) as the next standard model. It is a combined product of MOS Model 11 [4] and SP [9], both of which are based on charges calculated from surface potential [2]. The virtual source (VS) model has its advantage in reducing the number of parameters down to below twenty, while maintaining the accuracy of predicting non-linearity at DC, especially for short channel transistors, where semi-ballistic transport takes place [6][10]. The model, however, is still in infancy with

unproven accuracy for non-linear RF behavior and no apparent advantages in prediction of the noise behavior at high frequencies.

Various work on MOSFET small signal modeling has been reported [11]–[14]. For many RF applications such as RF power amplifiers, mixers, and oscillators, however, the capability of the model to predict the large signal and intermodulation distortions is important. Several work on MOSFET nonlinear model has also been reported [15]–[19].

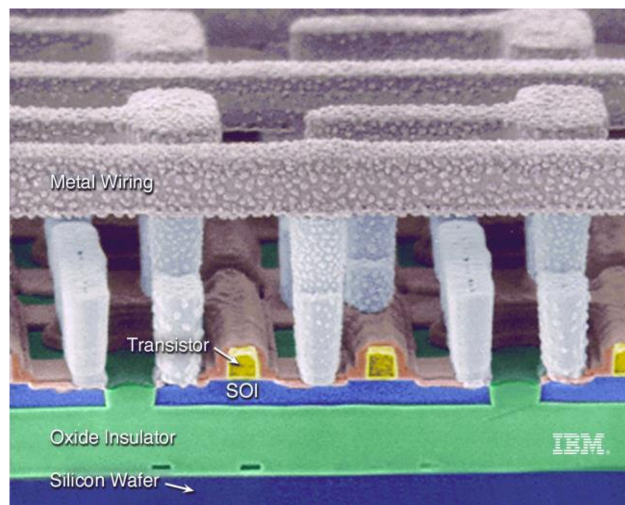

Figure 1.3. A SEM image from IBM of one finger of CMOS SOI transistor [20]

Nevertheless, few deal with nonlinear RF modeling of MOSFETs with channel lengths below 65 nm and also on silicon-on-insulator (SOI) technology. CMOS SOI technology usually offers 20-35% better performance compared to its bulk CMOS counterparts [21], because of the elimination of junction capacitances and substrate loss. Also for power applications, the presence of the Buried Oxide (BOX) layer helps the device to sustain larger voltage swing, which may lead to high output power. Figure 1.3 is a SEM image of one finger of a CMOS SOI transistor. Only a few work has been devoted to CMOS SOI

transistor modeling [13], [22]–[24]. Most are either dealing with small-signal models or are purely empirical based. Large signal circuit design has been purely relying on the models provided by semiconductor manufacturing foundries, which are developed for digital and low-frequency analog circuits, and lack the accuracy to predict RF and microwave behavior.

Accurate MOSFET noise model requires deep understanding of device physics and accurate noise source identification. Most existing MOSFET noise models are thermal-noise based, which consider the noise originated from the finite channel resistance, induced gate noise, correlation between gate and channel noise and various parasitic resistances [25]–[29]. Reference [30] adds the source-bulk junction and drain-bulk junction shot noise to the channel thermal noise. The latter two noise sources, under normal biasing condition of the transistor, are very small, as these junctions are reversed biased. Classical long channel thermal noise model is not able to fully capture the noise for nanoscale transistors, especially when the channel length scales down to below 100 nm. Compromises have been made to fit the need, however, not only does the classical long channel model fail to capture the fundamental physics, but also, as the device channel length scales down further, the model requires even more revisions. Lastly, reference [31] proposed that for short channel MOSFETs, the shot noise induced by the random nature of electron injection from the source through the potential barrier into the channel dominates the drain current noise compared to the thermal channel noise induced by electron random scattering in the channel. This model, unfortunately, has not been tested and verified.

In summary, an accurate CMOS SOI transistor modeling will require the model to have the following properties:

(1) Physics based accurate drain current model

(2) Accurate HF small signal and large signal model

(3) Accurate nonlinear and intermodulation distortion

(4) Scalability and bias dependence

(5) Accurate HF noise prediction

In this thesis, a comprehensive NMOS transistor model that covers drain current, high frequency nonlinear behavior, and a new combined shot-thermal noise is presented in the following sections.

1.3 Cold Cathode Technology

Cold cathode field emission has numerous vacuum microelectronic applications including plasma displays [32], electron guns for high power microwave sources [33], spacecraft neutralizer [34], scanning electron microscopes and so on. The mechanism for electron emission from a surface by applying a large electric field is called field emission. Recently, a field emission based vacuum channel MOSFET has been reported [35]. Figure 1.4 lists the applications of field emitters and the corresponding difficulty levels. Thermionic emission demands active cooling, a problem that has hindered the integration of thermionic electron guns into microsystems. In comparison to thermionic emission, field emission requires no cooling, thus may be suitable for integrated circuit applications. For a cold cathode to emit electrons, a substantially large electric field is often required to overcome the work function of the material used. To reduce the voltage

required between the two electrodes, sharp tips are usually used in almost all field emission applications. Tremendous amount of work has been devoted to conical shape field emitter arrays, known as Spindt arrays, for which the top sharp tip reduces the required voltage level and the large body would be able to provide sufficient amount of electrons and also helps to cool the device at the same time [34][36]. The problem associated with this type of devices is, however, the non-uniformity in tip sharpness due to fabrication variations. Typically, sharper tips are turned on earlier and conduct more current under the same bias, when compared to dull tips. This phenomenon leads to more heat generation for sharper tips, which in turn, causes them to burn easily. In order to mitigate the non-uniformity in tip current for longevity, a large feedback resistor, which acts as a current regulator, has been added in series with the emitter [37].

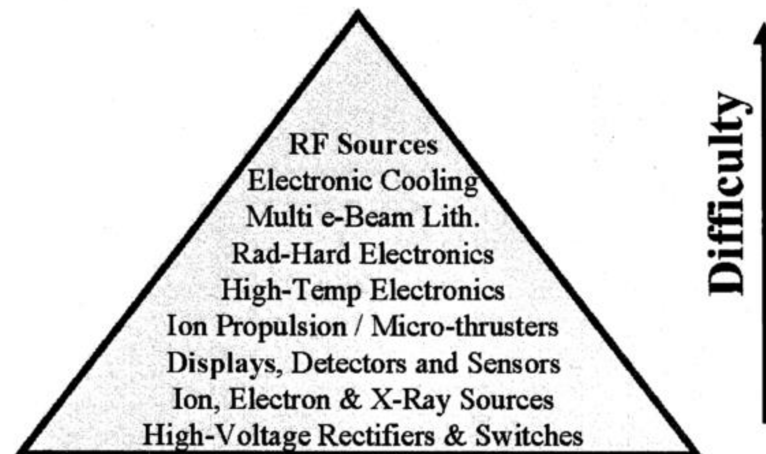

Figure 1.4. Difficulty level of various applications of field emitters[36]

This approach is not promising since the total emission current is limited to a fairly low number of field emitters as they continue to burn while their current is shifted to other

tips. A silicon pillar structure made with a low-doped semiconductor to achieve uniformity of emission current has been previously proposed [38]. Moreover, different materials are used as electron source, including carbon nanotubes (CNTs) [39]–[42], zinc oxide (ZnO) [43], and silicon carbide (SiC) [44]. The problem with all these implementations is that not only are they are still early stage research projects and far from integration, but also they have no current control mechanism, which may cause the device to fail rapidly. In this thesis, a field emitter electron source with vertical silicon nanowire array structure is proposed that addresses the problems of previous work. By taking advantage of current saturation mechanism in high aspect ratio semiconductor structure, the emission current can be readily limited and uniformity of emission is expected. Also, by reducing the doping level, the saturation voltage can be lowered to a few tens of volts for sharp tips and small gaps. A comprehensive device TCAD simulation has been conducted to achieve the optimal parameters for the design of the nanoscale electron field emitter. Two main failure mechanisms have been considered: thermal runaway and ion bombardment. Approaches to avoid both mechanisms are evaluated [34]. By utilizing the Langmuir-Blodgett (LB) experiment, a self-assembled mechanism to achieve low-cost and high density field emitters has been established. In this technique, instead of using electron beam lithography, a single compact layer of silica particles is deposited and used as a mask for etching of silicon nanowires. This way of fabrication yields a very dense array of nanowires, which will lead to high current density at a very reduced cost. Moreover, a new packaging process is proposed. Details of simulation, optimization and fabrication of these devices are discussed in Chapter 3.

1.4 Nano-Electro-Mechanical (NEM) Systems

Micro/Nanoelectromechanical systems (M/NEMS) are gaining great momentum and interest for a variety of applications such as extremely high sensitivity mass sensors [1], mechanical switches [45], mechanical memories[46], tunable filters [47] and oscillators [48]. One reason is the maturity of fabrication and their commercialization. Consequently, several MEMS devices have been used in our daily lives, such as accelerometers and pressure sensors in cars, different type of sensors in phones, etc. [49]. The other reason is that they possess an inherently high quality factors and can provide narrow bandwidth operation compared to their electrical counterparts. Moreover, mechanical devices, when scaled down to nanometer dimensions are usually more energy efficient, which is a good advantage for mobile computing. Most commercialized mechanical devices are MEMS devices. When compared to their micro-scale counterparts, the nano-scale mechanical devices offer even better performance in most cases and are more sensitive if used as a sensor. The main problem is that they suffer from process variations and are still considered research-grade devices. The other challenge is that these nano-scale devices are difficult to integrate reliably because mechanical parts are more fragile as dimensions shrink down. Also, nano-scale devices are more challenging to characterize as the output signal is usually very weak and various damping sources such as surface effects may become more prominent.

Regarding NEMS devices, two different goals are pursued in this thesis. One is to design CMOS-compatible NEMS devices based on already commercialized CMOS technologies. These NEMS devices are then post-processed using a simple microfabrication technology in the cleanroom to release the mechanical parts. These

devices are then characterized with various methods for different purposes. Barniol group has done some pioneering work for CMOS-compatible MEMS device mostly based on 0.35 μm and 0.13 μm CMOS technologies and has proven the concept [50]–[54]. A more advanced technology, namely GlobalFoundries 45 nm CMOS SOI technology, has been used to pursue alternative designs for different applications. Further details are illustrated in Chapter 4.

The other goal of pursuing NEMS technology is to construct a system-level compact model for nano-scale NEMS resonators. Not only does the model capture the mechanical behavior of the device, it also accounts for the detailed coupling between the mechanical and electrical behavior of the system. Furthermore, it takes into account the various parasitic elements, which are important for these nano-scale devices. Chapter 4 provides further details on this subject.

CHAPTER 2. COMPACT MODELING OF 45NM CMOS SOI TRANSISTORS

2.1 Introduction

Nanoscale CMOS technology is an excellent platform for implementing single-chip systems because of its low manufacturing cost and integration capability with digital circuits [55]. Cutoff frequency f_T and maximum oscillation frequency f_{MAX} of advanced nanoscale Metal Oxide Semiconductor Field Effect Transistor (MOSFET) have surpassed 200 GHz mark, enabling microwave and mm-wave circuit operation [56]. Implementing microwave and mm-wave circuits with first time success remains elusive due to limited accuracy of the available device models on conductive Si substrates. Accordingly, comprehensive deep sub-100 nm MOSFET models that accurately capture DC, RF (including nonlinear) and noise characteristics of transistors are of great demand. Device modeling requires the knowledge and expertise in several distinct areas including mathematical modeling, device physics, high frequency and microwave measurement, electro-thermal analysis, noise analysis, programming, and statistics. Several MOSFET models have already been fully or partially developed [3]–[6]. The widely used BSIM model employs hundreds of parameter - many of them empirical - to capture linear and nonlinear RF and noise behavior of modern submicron MOSFET devices. Extraction of so many parameters is cumbersome and has led to the development of many BSIM models with insufficient accuracy. The surface potential based Phillips MOS Model

utilizes fewer empirical parameters compared to BSIM model. With over 200 parameters to be extracted, however, the model development is still an enormous challenge given the short time to market for advanced CMOS technologies. Another MOSFET model is the so-called virtual source (VS) model, which uses about ten parameters to describe the nonlinear DC performance of short-channel transistors. This model assumes a semi-ballistic transport mechanism inside nanoscale channels of MOSFETs, leading to a good modeling accuracy [6][10]. The VS model, however, has to be supplemented with bias and geometry dependent parasitic resistances, capacitances, and inductances to become suitable for deployment at high frequencies. To date, the VS model with high frequency capability has been demonstrated for GaN FETs [57]. This model, however, is still unproven for predicting the nonlinear RF to mm-wave behavior of MOSFETs. Furthermore, it has no apparent advantage in predicting the noise behavior of nanoscale MOSFETs at high frequencies over other available MOSFET models.

Compared to nonlinear DC modeling, the nonlinear RF modeling of transistors is more challenging due to bias and geometry dependence of some of the parasitic elements in the RF model. Small-signal modeling is a shortcut in developing RF models and helps capturing the high frequency behavior of transistors under small-signal excitation and under a particular bias condition with good accuracy. Various MOSFET small-signal models have been reported [11]–[14]. The main drawbacks in utilizing small-signal models are that the model cannot capture device nonlinearity and is only valid for particular device geometries and at particular bias conditions under small-signal excitation. Thus, the small-signal model fails to predict the large-signal behavior of RF power amplifiers, mixers, and oscillators, where device bias and gain may change under

applied RF signal and device nonlinearity. Furthermore, even for low-power RF circuits such as low noise amplifiers, weak nonlinearities including third order intermodulation distortions cannot be envisaged by the small-signal model. Several MOSFET nonlinear RF models have been reported [15]–[19]. Nevertheless, few deal with nonlinear RF modeling of MOSFETs with channel lengths below 65 nm and none addresses the intricacies of CMOS SOI modeling. To date, RF to mm-wave circuit designers have been mostly relying on digital models provided by semiconductor manufacturing foundries, which are mainly developed for digital and relatively low frequency analog circuit applications. These models have insufficient accuracy to predict RF and microwave behavior of linear and nonlinear devices and circuits.

MOSFET noise modeling requires a good understanding of device physics in order to identify various noise sources across the device. Most existing MOSFET noise models are based completely upon thermal noise. Such models presume that the noise originates from several thermal noise sources including a finite channel resistance, induced gate noise correlated to the channel noise, and various parasitic resistances [25]–[29]. The induced gate noise is introduced to explain the extra gate noise of MOSFETs at high frequencies as the device dimensions scale down. The induced noise model is incorporated more or less in the same manner among van der Ziel long-channel model, the BSIM 6 model, and Phillips MOS 11 model [3][4][58]. They share the same noise topology, in which, two correlated noise sources, i.e. the channel noise (the current noise flowing from the drain to the source terminal) and the induced gate noise (the current noise flowing from the gate to the source terminal), are incorporated [4][25][59]. Several other modifications to the classical long-channel noise model have been introduced.

Reference [30] adds the source-bulk junction and drain-bulk junction shot noise to the channel thermal noise in an attempt to capture the extra noise seen in sub-micron MOSFETs. Moreover, for noise, high frequency and high power applications, the distributed gate resistance effect of multi-finger MOSFETs has been introduced. Due to difficulty in its implementation, instead of using a lumped RC model, this effect has been most commonly modeled by a lumped gate resistor with a modified empirical resistance value [60][61][62]. The distributed gate resistance depends on the MOSFET layout and can be avoided if short transistor finger widths are employed in multi-finger RF transistor structures.

Despite all the modification made to the classical long-channel thermal noise model of MOSFETs, it still fails to fully capture the noise of nanoscale transistors, especially when the channel length scales down below 100 nm. On the other hand, for ultra short-channel MOSFETs with ballistic transport, it has been proposed that shot noise induced by the random nature of electron injection from the source contact through the potential barrier and into the channel dominates the drain current noise [31]. Therefore, the thermal channel noise induced by the random thermal motion of electrons in the channel of transistors operating in ballistic transport regime can be ignored. While this shot noise model fits the noise behavior of ultra short-channel MOSFETs investigated by device simulation, the model is not experimentally verified as no comparison to measured noise data has been provided [28]. Additionally, current sub-100 nm MOSFETs are still semi-ballistic transport devices and the aforementioned shot noise model is not expected to completely capture their noise behavior. It only seems logical that a combined shot-thermal channel noise model, which would integrate the classical long-channel noise

model and the shot-channel noise model together be utilized to accurately predict the noise behavior of the semi-ballistic transport devices.

2.2 Virtual Source (VS) Based DC Modeling

Since the explosion of mobile communication and computing, CMOS SOI technology has been in the forefront of technology platforms for applications such as microprocessors, embedded DRAM, transceivers and low-power devices [21]. Compared to its bulk CMOS counterpart, CMOS SOI provides between 20% to 35% performance gain or reduced power dissipation. The technology has been widely used in RF circuit design due to its low power dissipation, improved RF isolation, transistor stacking capability and the possibility of utilizing high resistivity and low-loss substrates [63][64]. The reasons for the performance gain of CMOS SOI devices over conventional bulk CMOS devices are: (*i*) significant reduction of transistor and passive element areal capacitances, (*ii*) reduced transistor short channel effects (SCE), (*iii*) improved transistor subthreshold slope, and (*iv*) the capability of using high resistivity substrate to reduce the losses and improve the self-resonance frequency of passive components. There are two types of SOI devices, namely, partially-depleted (PD) SOI and fully depleted (FD) SOI. In FD-SOI, the device layer thickness is smaller than the depletion thickness of source and drain contacts, leading to fully depleted body at threshold. There is no possibility of employing a body contact to the transistor in these devices and they behave similar to bulk CMOS devices, *i.e*. no kink effect (sudden increase in the output conductance for large drain-source voltage V_{ds}) is observed. One of the main drawbacks of FD-SOI technology is its large-scale manufacturability, especially at sub-100 nm nodes. It has been proven difficult to control the parameters responsible for device depletion thickness

to guarantee that the body is depleted under all biasing conditions across all device dimensions. PD-SOI, on the other hand, has a device layer thickness at least twice larger than the maximum depletion thickness, leading to the formation of a neutral region beneath the depletion region. Compared to the bulk CMOS and their FD-SOI counterparts, PD-SOI MOSFETs exhibit anomalous behavior such as kink effect, and reduction of threshold voltage V_T with an increase of V_{ds} for devices without substrate contacts (floating body configuration) [63]. The VS model employed in this work is developed for PD-SOI CMOS transistors, but currently does not capture kink effect. Additionally, several other mechanisms including breakdown mechanisms (source-drain reach-through, source-drain breakdown and gate oxide breakdown), low-frequency noise, lifetime and statistical variations of various device parameters are not employed at this time. While all these mechanisms are important and will be implemented in future modeling efforts, the current model is proven to have excellent accuracy for these 45 nm NMOS transistors, as long as the applied gate-source voltage V_{gs} and drain-source voltage V_{ds} remain below the safe transistor operating voltage in this technology (V_{safe} = 1.2 V). Note that although the VS model was originally developed for bulk MOSFETs, it has been applied to GaN HEMTs and Carbon Nanotube FETs with good accuracies, achieved by tweaking DC model parameters [65][66]. Through matching with measured data, it has been shown that the VS model is very robust in predicting the DC characteristics of NMOS transistors with different widths investigated in this work.

As the channel length becomes comparable to the electron mean free path in the channel, the classical drift-diffusion transport model fails [10]. Under this condition, MOS transistors feature semi-ballistic transport in the channel, where the classical drift-

diffusion based transport model fails [10]. By employing only a few physical parameters, the virtual source VS model is able to capture the output characteristics of modern short channel CMOS devices to a good accuracy. In the VS model, the normalized drain current is calculated as the product of the channel charge density (Q_{x0}) and the virtual source velocity (v_{x0}) at the top of the energy barrier at the source [6], where the gradual channel approximation applies [6].

$$\frac{I_d}{W} = Q_i(x_o) \cdot v_{x_o} \cdot F_{sat} \tag{2.1}$$

where $F_{sat} = \frac{V_{ds}/V_{dsat}}{\left(1+\left(\frac{V_{ds}}{V_{dsat}}\right)^{\beta}\right)^{1/\beta}}$. The channel charge density is given by an empirical function given by

$$Q_i(x_o) = nC_{inv}\phi_t \ln\left(1 + \exp\left(\frac{V'_{GS}-(V_T-\alpha\phi_t F_f}{n\phi_t}\right)\right) \tag{2.2}$$

where n is subthreshold coefficient, V'_{GS} is series resistance corrected voltage between gate and source and α is a fitting parameter. V_T is DIBL corrected threshold voltage. F_f is inversion function given by

$$F_f = \frac{1}{1+\exp\left(\frac{V'_{GS}-(V_T-\alpha\phi_t/2}{\alpha\phi_t}\right)} \tag{2.3}$$

Figure 2.1. illustrates the VS model fit into the measured data. An excellent fit for I_d-V_{ds} curves is observed.

The VS model has ten input parameters: gate capacitance under strong inversion C_{inv}, threshold voltage V_T, subthreshold swing SS, drain-induced barrier lowering parameter $DIBL$, series contact resistances R_s and R_d, effective channel length L_{eff}, carrier low-field effective mobility μ, carrier velocity v_{x_o} at the virtual source x_o, and two fitting

parameters α, β. Details of extraction of these parameters are provided in [6]. In short, the gate capacitance and effective channel length are extracted from the foundry design manual. Series contact resistances, threshold voltage, *DIBL*, *SS*, carrier mobility, and carrier velocity at the VS are extracted from the measured data. Empirically, α is set to be 3.5 while β is set to be 1.8 for NMOS transistors. The VS parameter values for the NMOS transistors investigated in this work are extracted from the dc behavior and are listed in Table 2.1.

Table 2.1. Extracted VS Parameters

Parameters	NMOS	Notes
L_g (nm)	40	Channel length
L_{ov}	12	Total overlap channel length
C_g (μF/cm^2)	2.625	Gate capacitance
R_s (Ω·μm)	153	Series contact resistance
DIBL (mV/V)	156	Drain-induced barrier lowering
SS (mV/dec)	97	Subthreshold swing
v_{xo} (cm/s)	9.1e6	Electron velocity at virtual source
μ (cm^2/V·s)	144	Mobility
α	3.5	Fitting parameter
β	1.8	Fitting parameter

Compared to its bulk counterpart, CMOS SOI devices present a relatively low thermal conductivity to the substrate due to a thin yet considerable buried oxide layer with low thermal conductivity under the active region. For RF transistors operating under high DC and/or RF powers, the temperature in the active region rises considerably. Higher temperature in the channel leads to higher scattering, higher noise and device

performance deterioration. In order to capture this phenomenon, a self-heating module is added to the VS model as described below.

$$\Delta T = \frac{R_{th}}{\tau}\int_0^{\tau} V_{ds} I_{ds} dt, \quad T_{junc} = T_{amb} + \Delta T \tag{2.4}$$

$$v_x = v_{x_o}(1-\eta\Delta T), \quad \mu = \frac{\mu_o}{1+\theta\dfrac{\Delta T}{T_{amb}}}, \tag{2.5}$$

where both θ and η are fitting parameters. τ is the period of the RF signal or the interval over which the heat dissipation is calculated and dt is an infinitesimal time increment. T_{amb} is the ambient temperature and T_{junc} is the elevated junction temperature due to self-heating. Parameters v_{xo} and μ_o are the initial VS velocity and carrier mobility at ambient temperature. R_{th} is the thermal resistance, assumed to be constant with modest temperature changes and may be calculated according to [67],

$$R_{th} = \frac{1}{2W}\left(\frac{t_{box}}{k_{ox}k_d t_{si}}\right)^{\frac{1}{2}} \tag{2.6}$$

where W is the transistor width, t_{box} is the thickness of buried oxide, t_{si} is the silicon body thickness, k_{ox} and k_d are the silicon dioxide and source/drain (n+ silicon) thermal conductivities, respectively. Note that thermal capacitance, which is a measure of how quickly the device warms up or cools down when power increases or decreases is not modeled. The above self-heating model takes into account virtual source velocity and mobility degradations due to the temperature rise ΔT caused by the self-dissipated power according to (2.5).

An accurate DC model is the very foundation of the high frequency nonlinear transistor model. It not only requires to have an accurate prediction of the drain current, but also both transconductance and output conductance must be modeled with good

accuracies in order to predict both linear and nonlinear high frequency behavior of the transistor.

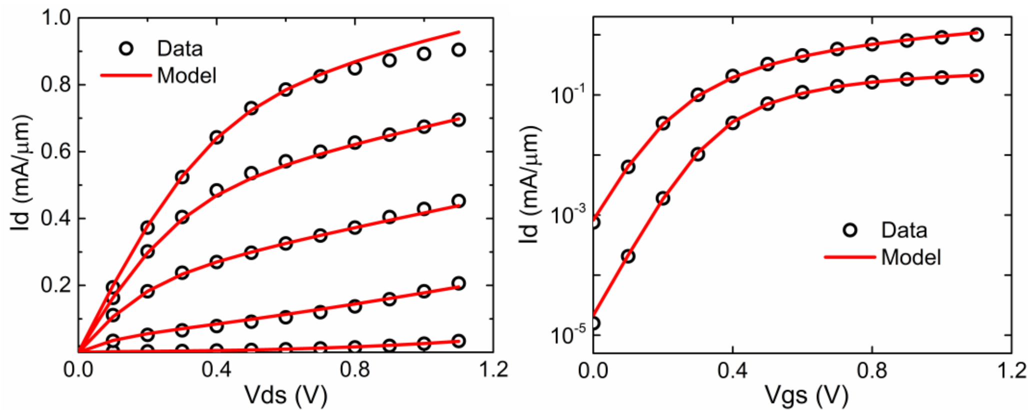

Figure 2.1. Accuracy of the developed VS model with self-heating effect (red curves) *vs*. measured DC data (open symbols) for two DC characteristics: (a) Drain current vs drain-source voltage (I_d-V_{ds} characteristics), when gate-source voltage V_{gs} varies from 0.2 V to 1.0 V in steps of 0.2 V; (b) Drain current vs. gate-source voltage (transfer characteristics) when V_{ds} = 0.1 V (lower currents) and V_{ds} =1.1 V (higher currents)).

2.3 Nonlinear RF Modeling

2.3.1 Equivalent Circuit Based RF Model

A simple equivalent circuit based MOSFET RF model has been developed for MOSFET transistors in this technology as shown in Figure 2.2 (a). It consists of the core nonlinear VS model with included self-heating, intrinsic parasitic capacitances C_{gs}, C_{gd}, C_{ds} (enclosed by the blue box in Figure 2.2) and extrinsic parasitic elements (C_{pg}, C_{pd}, L_g, R_g, L_d, R_d, L_s, R_s) originated from interconnections, vertical interconnects (VIAs), RF pads and transistor layout parasitics. All these parasitic elements have been extracted from the measured S-parameter data. The measured transistors have multi-finger layout

with 1 μm finger width and 40 nm effective finger length and number of fingers ranging from 42 to 336. The S-parameters were measured up to 40 GHz using Keysight E8361A PNA with INFINITI GSG RF probes. Moreover, the open de-embedding patterns were measured and used to eliminate the parasitic parallel capacitances associated with the pads (C_{pg}, C_{pd}). Note that, unlike the small-signal equivalent circuit model, this model is built upon a physics based DC model, rather than empirical transconductance and output conductance extracted from measured S-Parameter data.

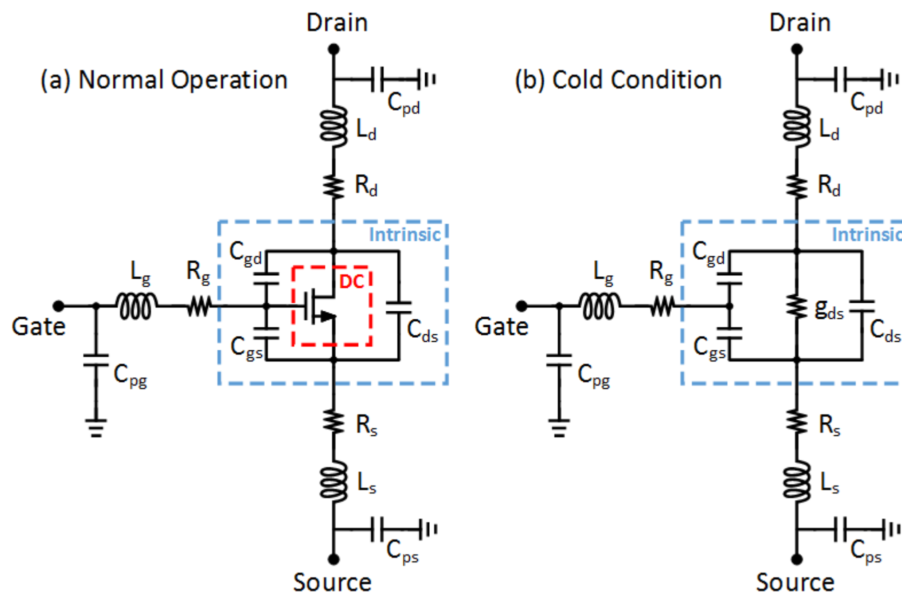

Figure 2.2. Nonlinear equivalent circuit model of NMOS transistors under (a) normal operation and (b) cold bias condition. The DC characteristics is given by VS model (inside the red box). Elements inside the blue box are denoted as intrinsic elements whereas those outside of the box are extrinsic elements.

2.3.2 Extrinsic Parameter Extraction

Most extrinsic elements (with the exception of R_g, R_d and R_s in Fig. 2.2 (a)) originate from the intermediate metal layers and the pads of MOSFET test structures and should not be taken into account when developing the nonlinear scalable RF model. The extrinsic parameters are bias independent but are functions of pad and interconnect geometries and their metallization structure. The extrinsic parasitic elements should be accurately extracted in order to obtain accurately extracted intrinsic parasitic elements discussed in the following section. The gate and drain parallel capacitances are extracted from an open de-embedding pattern that is fabricated on the same chip. Next, extrinsic parasitic inductances and resistances are extracted. Various extraction techniques have been developed for different technologies [12]–[14], [68]. Among them, techniques presented in [12] and [13] have been found to be most effective for this short-channel CMOS SOI technology. Under cold bias condition (V_{ds} = 0 V and I_{ds} = 0 A), the transistor operates in the linear regime and the equivalent circuit of the transistor simplifies to the one shown in Fig. 2.2 (b). During the extraction of extrinsic parameters, reference [13] utilized the fact that channel conductance in the linear regime is proportional to the overdrive voltage ($V_{gs} – V_t$) and this assumption has been verified for the NMOS transistors investigated in this work. By utilizing Z-parameters and equations developed in [13], all series parasitic elements may be extracted with a simple linear regression. The extracted extrinsic parameters are shown in Table 2.2.

Table 2.2. Extracted extrinsic parameter values for different sizes of transistors

Width (μm)	42	84	168	336
C_{pg} (fF)	13.65			
C_{pd} (fF)	12.11			
L_g (pH)	32.13	30.33	35.32	35.41
L_d (pH)	32.24	23.37	31.55	35.72
L_s (pH)	45.22	41.26	39.76	38.40
R_g (Ω)	25.78	14.15	5.9	2.95
R_d (Ω)	2.62	2.47	2.01	2.08
R_s (Ω)	0.36	0.34	0.69	0.85

2.3.3 Intrinsic Parameter Extraction

The intrinsic parameters were extracted from intrinsic Y-parameters, which can be obtained from the measured S-parameter by performing the following steps,

(1) converting the measured S-parameter (pads included) to extrinsic Y-parameter (Y^{ext});

(2) subtracting extrinsic parallel capacitances from extrinsic Y-parameter (Y^{ext}) to obtain intermediate Y-parameter (Y');

$$[Y'] = [Y^{ext}] - \begin{bmatrix} j\omega C_{pg} & 0 \\ 0 & j\omega C_{pd} \end{bmatrix}$$

(3) converting the intermediate Y-parameter (Y') to intermediate Z-parameter (Z')

(4) subtracting extrinsic series resistances and inductances from the intermediate Z-parameter (Z') to obtain intrinsic Z-parameter (Z^{int})

$$[Z^{int}] = [Z'] - \begin{bmatrix} R_g + R_s + j\omega L_g + j\omega L_s & R_s + j\omega L_s \\ R_s + j\omega L_s & R_d + R_s + j\omega L_d + j\omega L_s \end{bmatrix}$$

(5) converting intrinsic Z-parameter (Z^{int}) to intrinsic Y-parameter (Y^{int}).

With the intrinsic Y-parameter (Y^{int}), the intrinsic elements can be extracted according the following equations:

$$C_{ge} = -\frac{imag(Y_{12}^{int})}{\omega}$$

$$C_{gs} = \frac{imag(Y_{11}^{int} + Y_{12}^{int})}{\omega}$$

$$C_{ds} = \frac{imag(Y_{22}^{int} + Y_{12}^{int})}{\omega}$$

$$R_{ds} = \frac{1}{real(Y_{21}^{int})}$$

$$g_m = real(Y_{21}^{int})$$

C_{gsi} and R_i were extracted from the intrinsic Y_{11}^{int} as

$$Y_{11}^{int} = j\omega\left(C_{gse} + C_{gd} + \frac{C_{gsi}}{1+\omega^2 R_i^2 C_{gsi}^2}\right) + \frac{\omega^2 R_i C_{gsi}^2}{1+\omega^2 R_i^2 C_{gsi}^2} \quad (2.7)$$

Thus, C_{gsi} and R_i were extracted from linear fitting of the following equation at low frequency as shown in Figure 2.3.

$$\frac{1}{real(Y_{11}^{int})} = R_i + \frac{1}{R_i C_{gsi}^2} \cdot \frac{1}{\omega^2} \quad (2.8)$$

Figure 2.4 depicts extracted intrinsic elements *vs.* frequency for a 42 μm wide transistor (42 fingers with finger width of 1 μm and effective finger length of 40 nm) biased at gate-source voltage V_{gs} = 0.9 V, and drain-source voltage V_{ds} = 0.9 V following the above extraction procedures. The fact that these intrinsic elements are constant over a broad frequency range of interest indicates the physical accuracy of the model. The same extraction technique has been applied to transistors with different sizes (84 μm, 168 μm,

and 336 μm wide NMOS transistors with 84, 168, and 336 fingers, respectively, each with finger width of 1 μm and effective finger length of 40 nm) under different biasing combinations. V_{gs} is varied from 0 V to 1.2 V in steps of 0.3 V and V_{ds} is varied from 0 V to 1.2 V, also in steps of 0.3 V. The extracted intrinsic parameters g_m and R_{ds} are compared with dI_{ds}/dV_{gs} and the reciprocal of dI_{ds}/dV_{ds} from the nonlinear VS model and tossed out in favor of the nonlinear and scalable VS model. In Figure 2.5 (a), the extracted intrinsic transconductance g_m (open circles) of an 84 μm wide transistor is compared with dI_{ds}/dV_{gs} from the VS model (solid curves) as functions of gate-source voltage V_{gs}, when drain-source voltage V_{ds} is a parameter. Similarly, in Figure 2.5 (b), the output resistance R_{ds} (open circles) of an 84 μm wide transistor is compared with the reciprocal of dI_{ds}/dV_{ds} from the VS model (solid curves) as functions of drain-source voltage V_{ds}, when gate-source voltage V_{gs} is a parameter. Similar observations are made for other transistor sizes. Therefore, the two comparisons show close match between the transconductance and output resistance and their respective VS values, which is an indication of VS model accuracy.

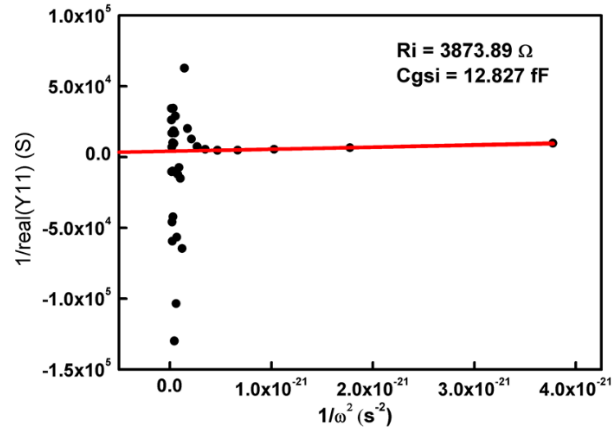

Figure 2.3. Linear fitting of 1/real(Y_{11}) to $1/\omega^2$ at low frequency region to extract R_i and C_{gsi}

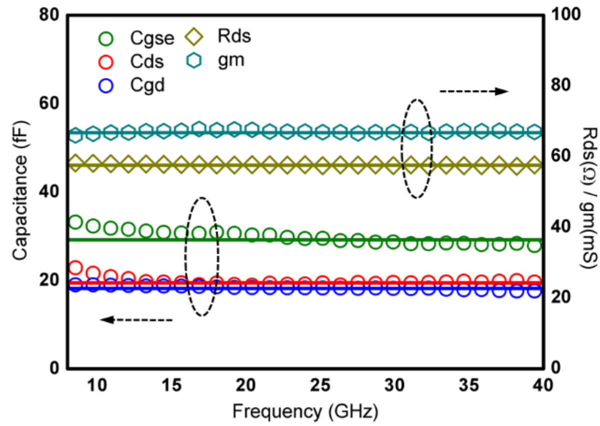

Figure 2.4. Frequency dependence of the extracted intrinsic elements, C_{gse}, C_{ds}, C_{gd}, R_{ds}, and g_m for a $42\mu m$ transistor biased at $V_{gs} = 0.9$V, $V_{ds} = 0.9$V

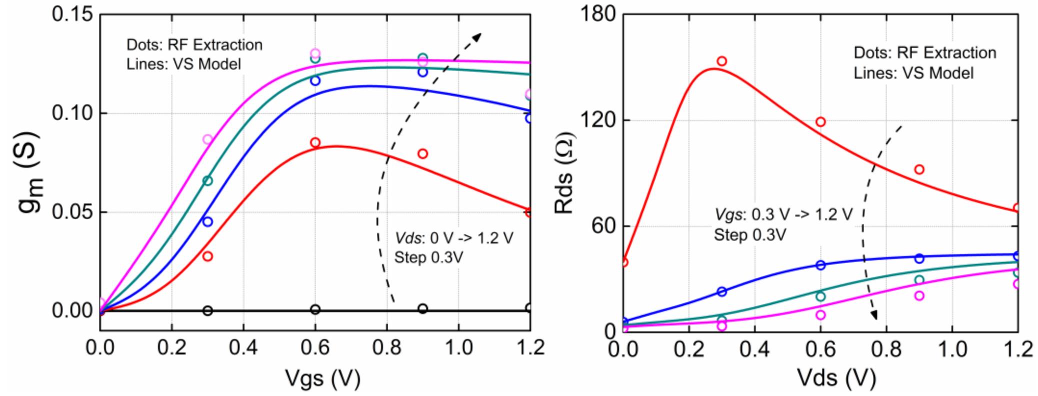

Figure 2.5. Accuracy of the VS model demonstrated by comparison to the extracted intrinsic parameters: (a) g_m and (b) R_{ds} for different bias conditions for an 84 µm wide transistor. Extracted intrinsic parameters g_m and R_{ds} are tossed out in favor of the scalable VS model.

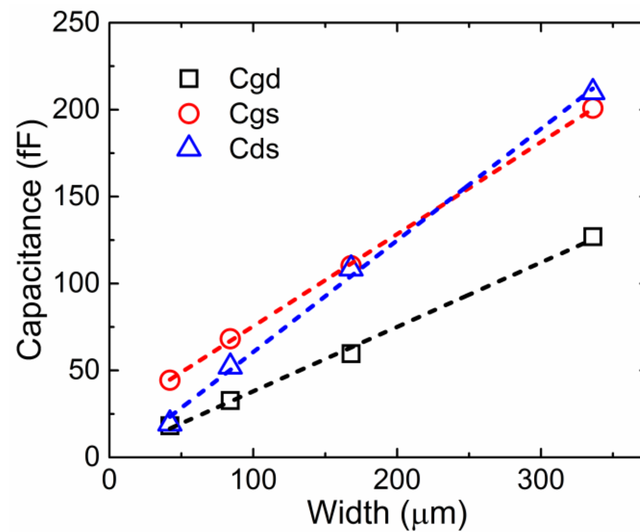

Figure 2.6. Intrinsic capacitances as functions of transistor width at V_{gs} = 0.9 V and V_{ds} = 0.9 V.

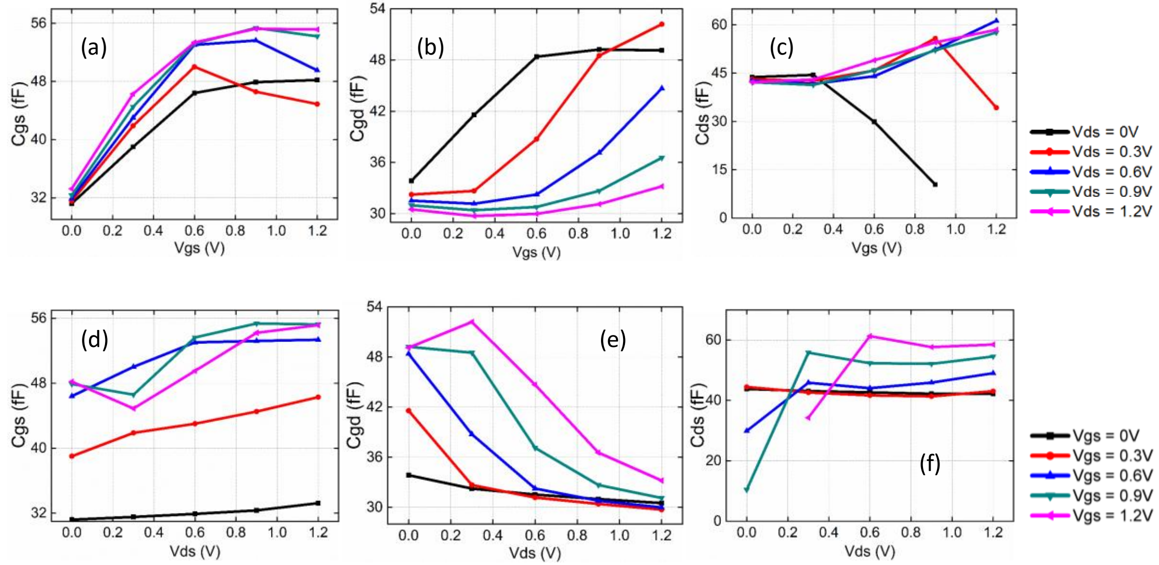

Figure 2.7. Bias dependence of extracted intrinsic elements (a)(d) C_{gs}, (b)(e) C_{gd}, and (c)(f) C_{ds} as functions of drain-source voltage V_{ds} and gate-source voltage V_{gs} for an 84 µm wide transistor.

Scalability is an essential part of a compact transistor model as it enables circuit designers to optimize the circuit performance by choosing the optimal transistor size. Figure 2.6 depicts the scalability of the extracted intrinsic capacitances C_{gs}, C_{gd}, and C_{ds} for transistor widths ranging from 42 µm to 336 µm. As these parasitic capacitances are mostly the overlapping and fringing capacitances among different terminals, they have linear dependences on the transistor width. An empirical approach has been taken to model the size dependency (scalability) of the three intrinsic parasitic capacitances. Six fitting parameters (the slope and the Y-axis intersection of each curve in Figure 2.6) have been extracted. Intrinsic elements for transistors with other sizes not measured here are extrapolated from these values. Figure 2.7 shows the gate-source and drain-source bias dependence of the three intrinsic capacitances (C_{gs}, C_{gd} and C_{ds}) for an 84 µm wide

transistor. In Figure 2.7 (a)-(c), the drain-source voltage is a parameter whereas the gate-source voltage is swept and in Figure 2.7 (d)-(f), the gate-source voltage is a parameter while the drain-source voltage is swept. Again, similar trends are observed for transistors with different width.

2.3.4 S-parameter Simulation

The developed MOSFET scalable model is put to a simple verification test. The S-parameters of an 84 μm NMOS transistor combined with extrinsic parasitic elements that represent interconnect test structure and the pads are calculated using Cadence SpectreRF and compared with the measured S-parameter values for the same transistor under different bias conditions. Figure 2.8 shows such comparison when gate-source voltage is fixed, while drain-source voltage is varied (V_{gs} = 1.2 V, V_{ds} = 0 V, 0.3 V, 0.6 V, 0.9 V, 1.2 V). Figure 2.9 depicts the comparison for a fixed drain-source voltage, while gate-source voltage is varied (V_{ds} = 1.2 V, V_{gs} = 0 V, 0.3 V, 0.6 V, 0.9 V, 1.2 V). An excellent match among measured and simulated S-parameter values up to 40 GHz and for all biasing conditions is observed. Moreover, similar trends are observed for other transistor sizes, demonstrating the accuracy of the scalable nonlinear model to predict the small-signal RF performance of transistors with different sizes.

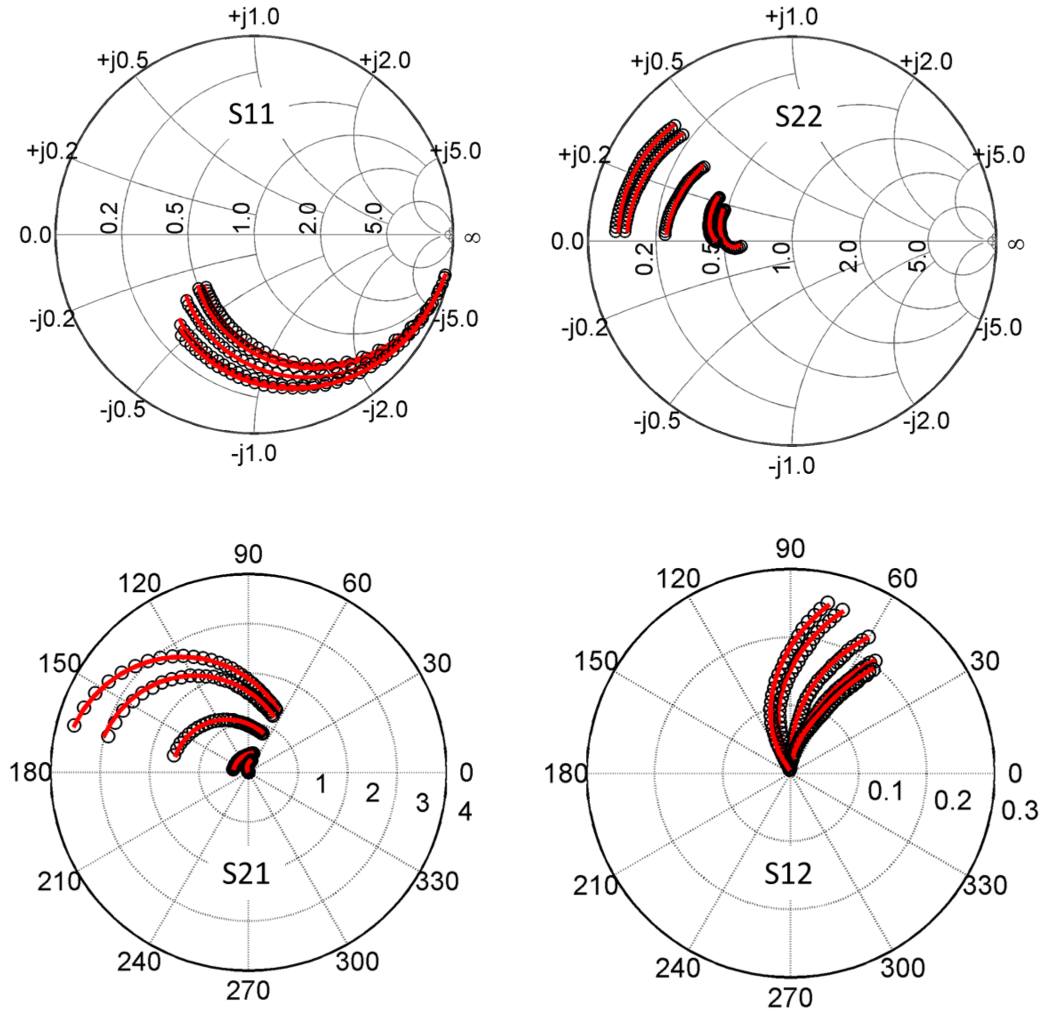

Figure 2.8. Comparisons of measured (open symbol) and simulated (solid line) S-parameters for different V_{ds} (0.0V, 0.3V, 0.6V, 0.9V, 1.2V) and V_{gs} = 1.2V for 84μm transistor.

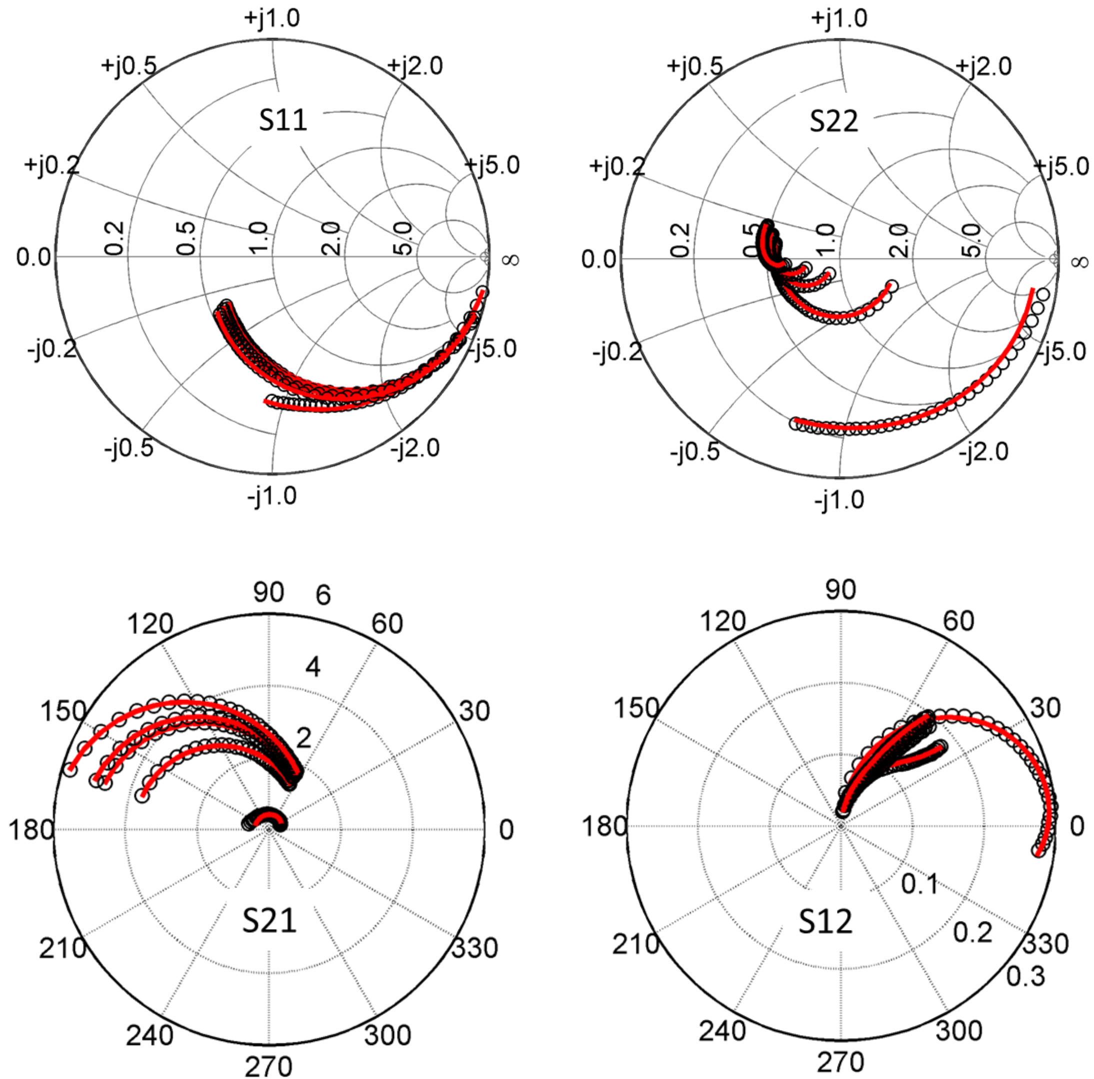

Figure 2.9. Comparisons of measured (open symbol) and simulated (solid line) S-Parameters for different V_{gs} (0.0V, 0.3V, 0.6V, 0.9V, 1.2V) and V_{ds} = 1.2V for 84μm transistor.

2.4 Noise Behavior of nm-Scale Transistors

The next step in the model development is to add noise capability to the existing nonlinear model. According to classical high frequency noise models, the noise sources

in a MOS transistor originate from thermal noise associated with access resistances and channel resistance as shown in Figure 2.10 (a) ($\overline{i_D^2}$, $\overline{i_G^2}$, $\overline{i_S^2}$, and $\overline{i_{Ch}^2}$). The thermal noise of physical resistors within the transistor can be described by a current noise source in parallel with the resistor R with a noise power spectral density $4kT\Delta f/R$. The absolute temperature T is set to the junction temperature of the device according to the self-heating module of the nonlinear transistor model. For $\overline{i_G^2}$, in addition to the thermal gate noise stemmed from the physical gate resistance, an induced gate noise is introduced to the classical model of sub-micron MOSFETs with very thin gate oxide to capture the noise due to the coupling between the potential fluctuations in the channel and the overlaying gate through gate-oxide capacitance [58]. On the other hand, for channel thermal noise, while some circuit simulators such as SPICE use the model $\overline{i_{Ch}^2} = 4\gamma k_B T g_m$ (where g_m is the transconductance at the DC operating point, not valid for the linear region), the most widely used channel noise model is the one derived by van der Ziel given by,

$$\overline{I_d^2} = 4\gamma k_B T g_0 \tag{2.9}$$

where g_0 is the output conductance at V_{ds} = 0 V (linear region). γ is the so-called channel noise parameter and is equal to 2/3 in saturation and 1 in linear region for long channel devices [25]. This noise model describes the noise behavior of long-channel transistors well. The model, however, tends to underestimate the channel noise for short-channel transistors [69]. In an attempt to explain the excess noise of short-channel transistors, the

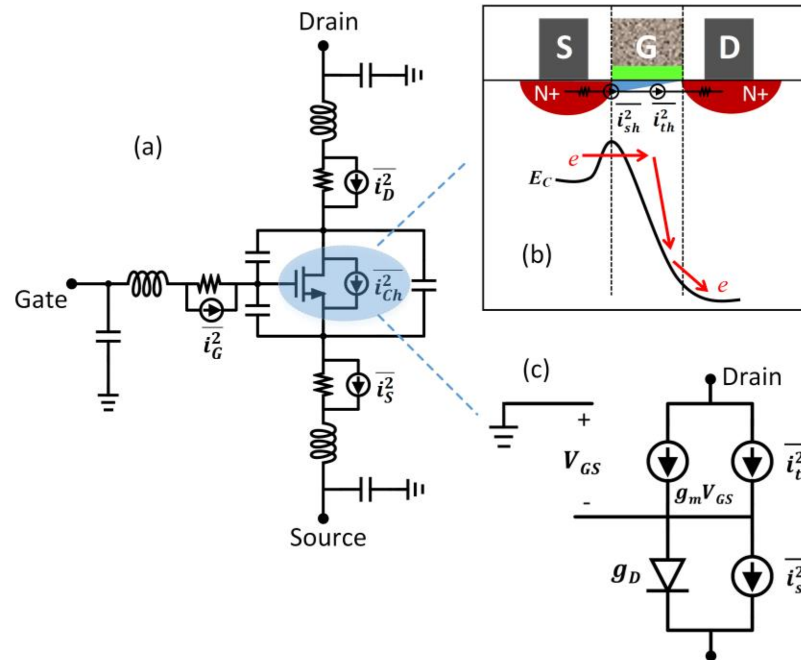

Figure 2.10. (a) Equivalent noise circuit model of a MOSFET with various noise sources. (b) The inset depicts the noise mechanisms in the channel for short-channel MOSFETs. (c) Circuit diagram of the combined channel noise model.

excess noise has been attributed to the elevated electron temperature at the drain [70]. Unfortunately, the electron temperature based noise model is shown to be in contradiction with simulation results [71]. On the other hand, the existing long-channel noise model has been adopted by most model developers through assigning a larger channel noise parameter γ that is no longer constant and changes with both bias and device dimensions to accommodate larger than expected noise of short-channel MOSFETs. While such a modification is convenient, it does not capture the noise of the short-channel device accurately, especially as the drain-source voltage or the lattice temperature of the device changes. Extraction of such empirical parameter γ to fit to all measured noise data is also very challenging.

Reference [31] points out that classical thermal channel noise model is based on drift-diffusion transport theory, which fails to predict the transport behavior of short-channel devices with ballistic transport. Therefore, in [31] the channel noise has been attributed to the shot noise induced by random injections of electrons from the source terminal to the channel, whereas the thermal noise in the channel has been completely eliminated. The current noise spectral density of the channel has been described by $2k_sqI$ following the shot noise model in vacuum tubes (which are ballistic devices). According to the model, as the injection of electrons alter the field near the source in the space-charge region, the probability for the following electron injection is reduced, leading to the introduction of a shot noise suppression factor k_s ($k_s < 1$). The shot noise model of short-channel MOSFET with the assumption of ballistic transport has been compared with device simulation data. Unfortunately, to the best of authors' knowledge, no verification of the noise model with measured noise performance has been provided since.

The shot noise model is built upon the ballistic transport theory, in which the electrons, after tunneling into the channel, are pumped into the drain immediately without any scattering. Given the doping density of the channel of NMOS transistors in this 45 nm CMOS SOI technology, the electron mean free path is roughly 7 nm [72]. Therefore, each electron encounters, on average, 5-6 scattering events in the channel before arriving at the drain (Effective channel length is 40 nm). This assumption ignores the fact that the transport occurs at Si-SiO_2 interface, which may impact the number of scattering events experienced by each electron. Therefore, it is only logical to devise a MOSFET noise model for such semi-ballistic devices that has contributions from both thermal and shot

noise. Therefore, the effective channel noise spectral density can be described through the following equation,

$$\overline{i_{Ch}^2} = \overline{i_{sh}^2} + \overline{i_{th}^2} \tag{2.10}$$

in which, $\overline{i_{sh}^2} = 2k_s qI$ is the shot noise term used to describe the noise associated with the tunneling of electrons at source-channel barrier, and $\overline{i_{th}^2}$ is the thermal noise generated by thermal agitation of electrons in the channel given by (2.9) with γ of 2/3 in saturation and 1 in linear region. Note that the correlation between the two noise sources $\overline{i_{sh}^2}$ and $\overline{i_{th}^2}$ is ignored as the two noise mechanisms are spatially separated. The model is depicted in the schematic shown in Figure 2.10 where the noise equivalent circuit model is constructed over the high frequency nonlinear model. The combination of the shot and thermal channel noise models not only predicts the drain current noise accurately, but it also captures the undying physics very well. Note that an accurate high frequency equivalent circuit model is the premise to constructing the noise model. The noise sources consist of the thermal noise from three access resistors for the three terminals of the device, *i.e.* $\overline{i_D^2}$, $\overline{i_G^2}$, $\overline{i_S^2}$ and the combined shot-thermal noise from the channel, *i.e.* $\overline{i_{Ch}^2}$, given by (2.10). By matching to the measured noise data, it has been experimentally found that there is no need for accounting for the induced gate noise or distributed gate resistance, at least for the transistor geometries measured in this work. As a result, to model the noise, a single parameter k_s, which is not bias, geometry or frequency dependent is used to match the model to all the measured noise data.

The high frequency noise characteristics of a two-port system can be represented by

$$NF = NF_{min} + \frac{R_n}{G_s}\left|Y_s - Y_{opt}\right|^2$$

$$= NF_{min} + \frac{4R_n}{Z_0}\frac{\left|\Gamma_{opt}-\Gamma_s\right|^2}{\left|1+\Gamma_{opt}\right|^2(1-|\Gamma_s|^2)} \quad (2.11)$$

where NF is the noise factor (also termed as noise figure when reported in decibels) at a given source impedance Γ_s. NF_{min} is the minimum noise factor. Γ_{opt} is the source reflection coefficient for minimum noise factor and Z_0 = 50 Ω is the characteristic impedance of the system. R_n is the equivalent noise resistance, which is a measure of how fast the noise figure degrades as the source reflection coefficient deviates from its optimum value Γ_{opt}. An accurate NF prediction requires an accurate modeling of four noise parameters: NF_{min}, R_n, and complex Γ_{opt}. The equivalent circuit S-parameter and noise parameters (NF_{min}, R_n, and Γ_{opt}) were calculated by SpectreRF simulation. Figure 2.11 is the comparison between the measured S-parameters and simulated S-parameters based on this model and the one based on the foundry model (post-layout simulation) for an 84 μm transistor biased at V_{gs} = 0.5 V, V_{ds} = 1.0 V in the frequency range of 8 to 40 GHz. As can be seen, this model demonstrates a much better accuracy for predicting S-parameters, which is a necessary requirement for predicting the noise behavior.

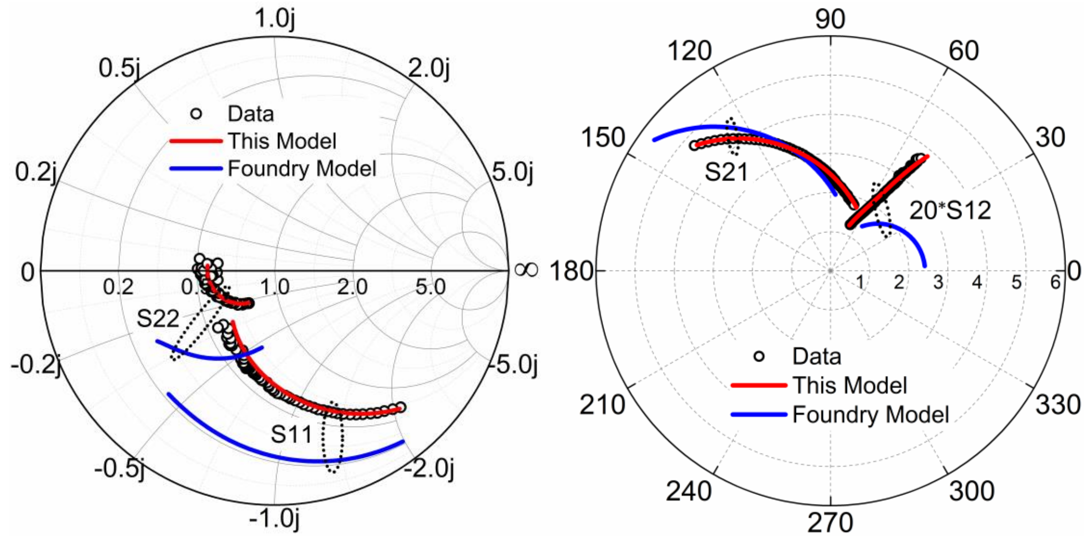

Figure 2.11. Comparison of measured (symbols) and simulated S-parameters by this model (red lines) and the foundry model (blue lines) for an NMOS transistor with a width of 84 µm at bias V_{gs} = 0.5 V and V_{ds} = 1 V.

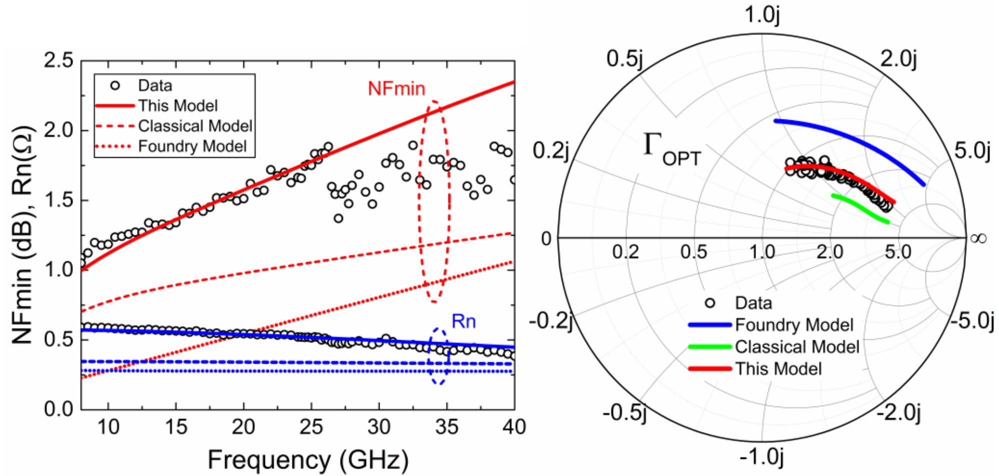

Figure 2.12. Measured (open symbols) and simulated (lines) noise parameters with three different noise models: (a) NF_{min} and R_n as functions of frequency and (b) Γ_{OPT} plotted on a Smith impedance chart for an NMOS transistor with a width of 84 µm at bias V_{gs} = 0.5 V and V_{ds} = 1 V. Note that, the mismatch in NF_{min} at frequencies between 26 and 40 GHz is due to the measurement issues as it appears in all the noise data.

Figure 2.12 shows the simulated noise parameters, *i.e.* NF_{min}, R_n, and Γ_{opt} by three different models (the one developed in this work, the classical ideal long-channel thermal noise model with γ of 2/3, and the post-layout foundry model) compared to the measured data. The foundry model and the classical model both underestimate the minimum noise figure by ~ 1 dB and ~ 0.5 dB, respectively, as they attribute the channel noise to the finite channel resistance, whereas the shot noise at the source terminal is not considered. Moreover, the classical channel noise model and the foundry model predict that the equivalent noise resistance is almost flat within the broad range of frequencies, which is in contradiction with the measured data. Additionally, the foundry model and the classical model underestimate the equivalent noise resistance, which means that a small mismatch of the source impedance leads to a large discrepancy in the overall noise figure. Inaccuracy in the optimal reflection coefficient prediction observed by both the foundry model and the classical model shown in Figure 2.12 (b) leads to erroneous impedance matching of noise sensitive circuits *e.g.* low noise amplifiers (LNAs). Compared to the foundry model and the classical thermal model, the model developed in this work delivers a much more accurate prediction of all the noise parameters, leading to accurate noise figure predications for all impedance values across the Smith chart. Note that in the frequency range between 26 to 40 GHz, an abrupt drop of NF_{min} is observed in the measure data for all measured transistors (different sizes) and under different bias combinations. As the noise figure cannot decrease or fluctuate with increased frequency, the observed trend of NF_{min} between 26 to 40 GHz are likely due to a measurement-related issue, which is still under investigation. Such measurement-related issues were much less severe for R_n, and Γ_{opt} measurements.

With respect to the device operating region, classical thermal noise model predicts that the noise spectral density should decrease from linear region with $\gamma = 1$ to saturation region with $\gamma = 2/3$, which is in direct contradiction with the observed trend of the extracted noise spectral density shown in Figure 2.13. The extracted channel noise follows shot noise trend but is smaller in values.

Figure 2.14 shows the noise behavior as a function of channel length when devices scale down to near ballistic limit. There are two critical lengths (L_{c1} and L_{c2}). Above L_{c2}, the thermal noise dictates the output noise while below L_{c1}, the shot noise dominates the output noise. In between these two critical channel lengths, the channel noise should be described by the combined shot-thermal noise.

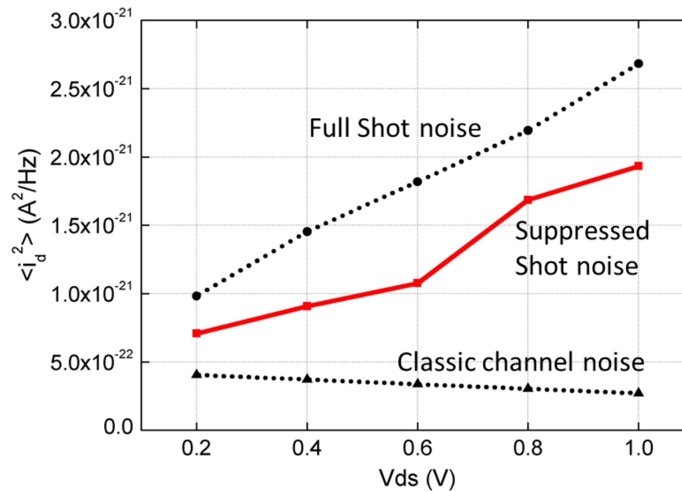

Figure 2.13. Comparisons of different channel noise models as a function of V_{ds}, V_{gs} is kept at 0.5V for 42µm transistor

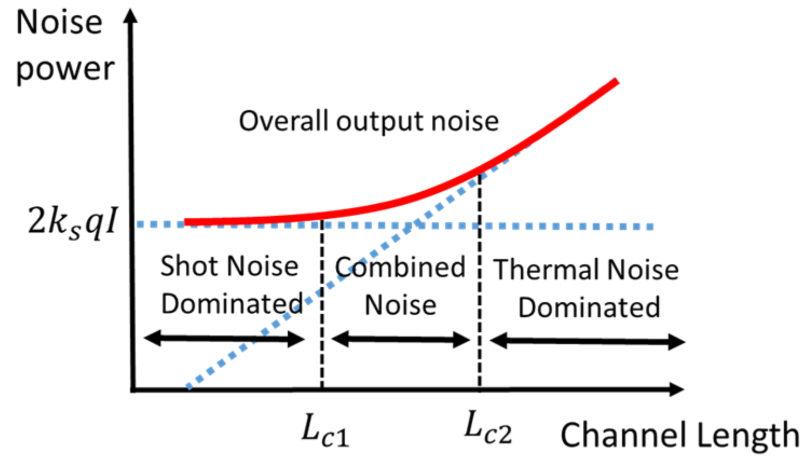

Figure 2.14. Relation between shot noise, thermal noise with the overall output noise as a function of channel length

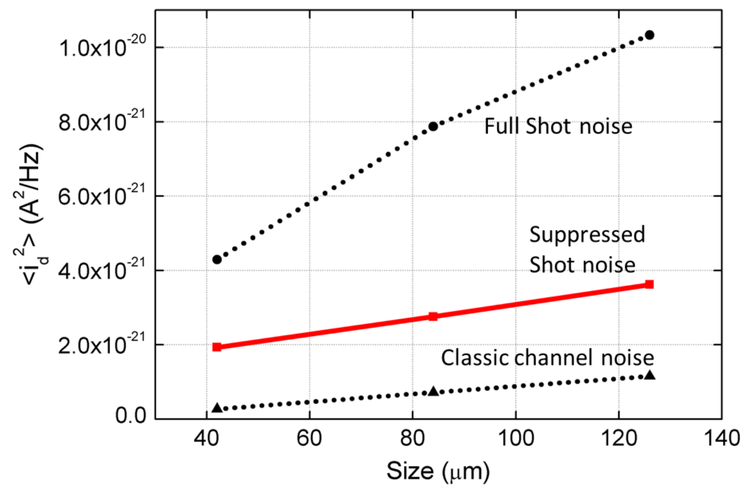

Figure 2.15. Comparison of different channel noise models for transistors of different sizes, bias condition: $0.5V_{gs}$, $1.0V_{ds}$

2.5 Model Validation

In order to further verify the model accuracy, two different circuits, namely a triple-stacked power amplifier cell [73] and a two-stage microwave low noise amplifier (LNA) have been implemented and their measured performance is compared against simulated data based on the transistor model developed in this work. The triple-stacked power cell, which can be used to construct power amplifiers, is used to verify the power performance and nonlinearity of this model, whereas, the two-stage LNA has been used to verify the high-frequency noise model developed in this work.

Figure 2.16 (a) shows the circuit schematic of the triple-stacked power amplifier cell, which consists of three 126 μm wide transistors, with the bottom transistor in common-source configuration with external bias applied through a bias tee and two common-gate transistors that are self-biased from an output bias-tee. Three power measurements at three frequencies, 2 GHz, 10 GHz, and 24 GHz have been conducted using a Keysight 83640L CW signal generator as the power source and a Keysight N8488A power sensor connected to a power meter. The circuit is also simulated using SpectreRF with a foundry-supported process design kit (PDK) and also with the transistor model developed in this work in combination with models of passive devices (inductors and capacitors) from the post-layout extraction. The simulated and measured output power as a function of input power (P_{out}-P_{in}) for each measured frequency are shown in Figure 2.16 (b) and present a close agreement between the measured data and our model. Excellent prediction of the linear output power and $P_{1\mathrm{dB}}$ (1 dB compression point) indicates the accuracy of the nonlinear model of the transistor. Note that the foundry model overestimates the output power and $P_{1\mathrm{dB}}$ by 1 to 3 dB.

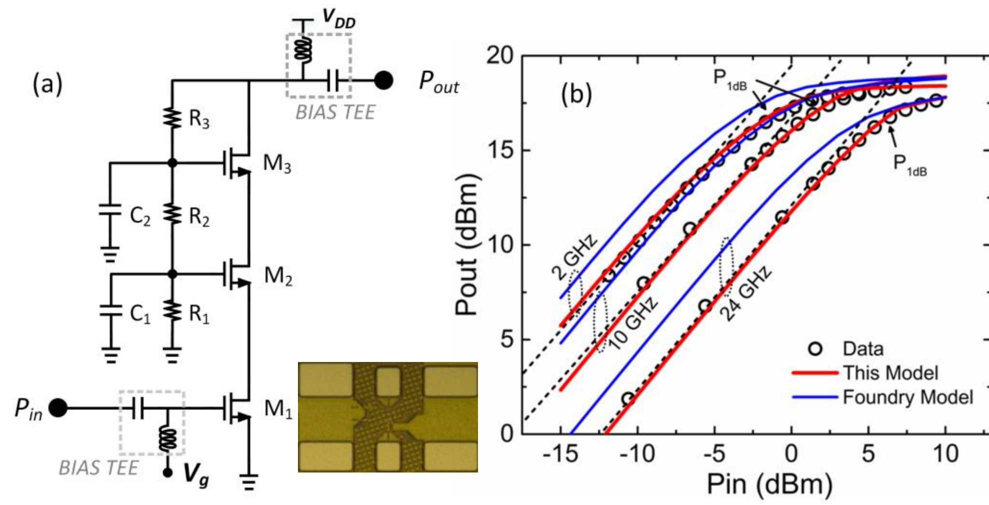

Figure 2.16. (a) The circuit schematic of a triple-stack power amplifier cell. All transistors are 126 μm wide. (b) The comparison among measured and simulated output powers of the triple-stack power cell at three different frequencies: 2 GHz, 10 GHz, 24 GHz.

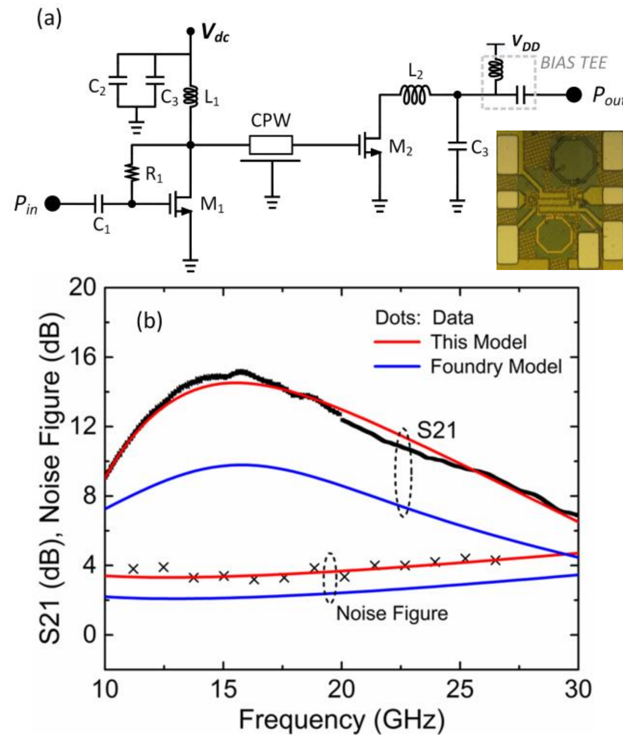

Figure 2.17. (a) The circuit schematic of a two-stage microwave LNA. The first stage uses a 126 µm wide transistor while the second stage has an 84 µm wide transistor. (b) The comparison between measured and simulated S_{21} and Noise Figure of the LNA (50 Ω source impedance) vs. frequency. Noise data was only available up to 26.5 GHz.

The circuit schematic of the two-stage LNA is depicted in Figure 2.17 (a). The LNA consists of two common-source stages with a 126 µm wide transistor in the first stage and an 84 µm wide transistor in the second stage. The gain and noise figure at 50 Ω input impedance have been measured using a Keysight N8975A Noise Figure Analyzer with INFINITI GSG RF probes. The S-Parameters of the LNA are also measured using a Keysight E8361A PNA. Moreover, the circuit is simulated using SpectreRF with both the foundry-supported PDK and the transistor model developed in this work in combination with models of passive devices (inductors and capacitors) from the post-layout extraction. Figure 2.17 (b) depicts comparison among the simulated and measured forward gain S_{21}

and noise figure at 50 Ω input impedance of the LNA. A close agreement between the measured data and simulated data based on this model is observed for both gain (S_{21}) and noise figure from 10 to 30 GHz (Noise data to 26 GHz). The simulated circuit performance based on the foundry PDK underestimates both gain (by as much as 5 dB) and noise figure (by about 1.3 dB).

2.6 Conclusion

A new comprehensive and scalable NMOS transistor model for a standard 45 nm CMOS SOI technology has been developed and its accuracy has been verified through comparison with measured data. This nonlinear RF model employs a core VS model to simulate nonlinear DC characteristics, and is supplemented with self-consistent heating effect to capture the effect of high DC and/or RF power dissipation of large multi-finger transistors on the SOI substrate. The model captures the underlying transport theory to accurately predict drain current and its derivatives with respect to gate-source and drain-source voltages. Various device and interconnect related parasitic elements have been added to the model and are extracted from the measurement for transistors with different widths operating under various biases to achieve a nonlinear model for all regions of operation. Compared to the existing foundry model, this model maintains a much better accuracy through the comparison of simulated and measured small-signal S-parameters.

A new combined shot-thermal channel noise model that predicts the high frequency noise behavior of NMOS transistors has been developed. Through the combination of suppressed shot noise and ideal long-channel thermal noise, the model developed in this work is capable of capturing the device physics and achieving a better noise behavior

prediction compared to its counterparts. It is found that induced gate noise model and distributed gate resistance model are not required to capture the noise behavior of these transistors. The developed noise model uses only one fitting parameter (shot noise suppression factor k_s) and overcomes the limitations of most existing thermal-noise based models which have difficulty predicting the noise of sub-100 nm channel length transistors and a model based on pure shot channel noise developed for ballistic transport devices.

The model accuracy is confirmed through the comparison with the measured data of two microwave integrated circuits. A triple-stack power amplifier cell and a two-stage LNA were designed, implemented and measured. The close agreement between the measured and simulated output power, gain, and noise figure of these circuits indicates that the model is ready for practical RF and microwave circuit design.

Effects such as gate oxide breakdown, drain-source reach-through, kink effect observed in PD-SOI transistors, gate distributed resistance, low-frequency noise, device lifetime and statistical variations of device parameters have not been modeled in this work. While this work has focused on 45 nm NMOS SOI transistors, many of the techniques and ideas described here may be applicable to other CMOS and CMOS-SOI devices and even III-V FETs.

CHAPTER 3. COLD CATHODE TECHNOLOGY

3.1 Introduction

Before the transistor revolutionized the world, the vacuum tubes dominate the fields of computing and communication. However, there are several fundamental shortcomings for the vacuum tube devices in early- and mid-1900s, such as their large size, power hungry and hot operation, which often led to their early failure. These drawbacks were not resolved and presented a significant disadvantage compared to recently discovered transistors in early 1950s. Transistors with the possibility of integration leading to integrated circuits eventually replaced vacuum tubes in most computing and communication platforms. Figure 3.1 is a typical picture of the vacuum tube device. There are three terminals, cathode, anode, and control grid, which operate in a similar way to the source, drain, and gate terminals of a MOSFET. The whole structure is inside of a vacuum tube. When a voltage is applied to the anode, an electrical field will present at the cathode. If the electrical field is large enough such that the electrons at the cathode can overcome the surface potential, the electrons will tunnel through the vacuum to the anode and the current flows from the anode to the cathode. The control grid functions as a gate. It reduces the threshold voltage when a positive voltage is applied and shuts off the current flow when a negative voltage is applied. As can be seen, the vacuum tube device operates pretty much the same way as modern MOSFETs. Despite all the afore-

mentioned drawbacks of vacuum tube technology, it has two apparent advantages that make them superior to the modern CMOS transistor technology, namely the ballistic transport and the high power characteristics. Compared to the solid channel in the MOSFET, the channel of this device is vacuum. So the transition time will be much shorter compared to MOSFETs of the same scale, which suffer from scattering and are governed by drift-diffusion transport for long channel devices or semi-ballistic for shot channel devices. Shorter transition time means higher operating frequency. In fact, it has been shown that modern vacuum tube devices, with a similar channel length compared to MOSFETs, can operate up to THz frequency range, much above microwave frequencies that MOSFETs can operate and below infrared frequencies where operation is amenable to infrared and optical technology. Therefore, these vacuum devices can comfortably fill this THz gap of the electromagnetic spectrum.

The most mainstream implementation of modern vacuum tube technology is based on silicon field emitter arrays (FEAs). While tremendous progress has been made in advancing the technology, there are still several obstacles that prevent Si FEAs from commercial deployment. First, due to process variations, it has been impractical to achieve uniformity across the individual emitters of a silicon field emitter array. Non-uniformity of these FEAs causes variations in length and sharpness across the emitters which leads to some of the devices to emit larger currents while others may have less or no current at all. Emitter tips with very high currents may heat up excessively and burn out due to joule heating. The second reason for these silicon FEAs devices not to become commercially available is their short lifetime due to possible thermal runaway, and ion bombardment, which will be discussed in details in the following sections. Finally,

current FEA devices require a high operation voltage (~1,000 V) and have a low current density and fall short in integration and mass production due to fabrication incompatibility with mainstream Si technologies.

In this thesis, a new vacuum transistor based on silicon FEAs is proposed as shown in Figure 3.2. In this structure, several techniques are utilized to overcome the above mentioned shortcomings of modern silicon FEAs. For example, non-uniformity is addressed by adapting a simple but novel current limiting mechanism that results in current density uniformity across FEA tips despite difference in their shape, length or sharpness. Short lifetime is tackled by careful engineering design of the device parameters. Low current density and high fabrication cost are mitigated by utilizing a new fabrication technique, based on Langmuir-Blodgett (LB) self-assembled deposition. The detailed discussions on these techniques are presented in the following sections. Table 3.1 shows the comparison among the old vacuum tube technology, the modern CMOS technology, and the new proposed vacuum transistor technology. As can be seen, the new proposed vacuum transistor technology resolves almost all the drawbacks of the old vacuum tube technology and achieves a comparable performance and integration capability compared to the modern CMOS technology with presumed advantages of operating at higher frequencies and higher powers.

3.2 Physics

Field emission is associated with the electrons tunneling through a surface barrier, which follows the Fowler-Nordheim (FN) equation described below, where tunneling

occurs from the conduction band of the non-conducting region to the vacuum energy level. The basic version of the equation valid for flat metallic surfaces is shown below:

$$J_{FN} = AE^2 e^{(-\frac{B}{E})} \tag{3.1}$$

where J_{FN} is the electronic current density, E is the electric field at the vicinity of the field emitter, and A and B are physical constants, which are $1.23 \times 10^{-6}\ \mathrm{A/V^2}$ and $2.37 \times 10^{8}\mathrm{V/cm}$, respectively.

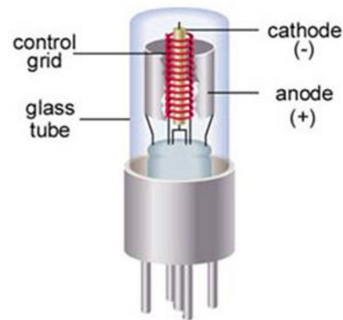

Figure 3.1. A typical three-terminal vacuum tube device.

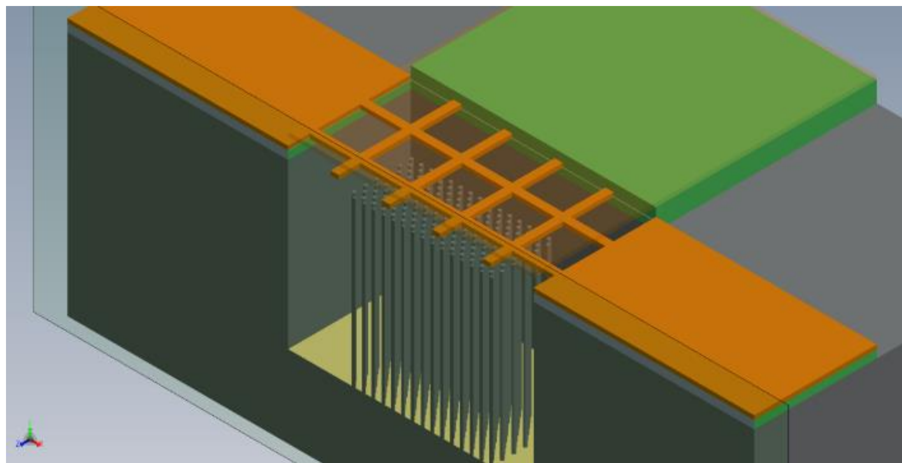

Figure 3.2. The proposed silicon FEAs as a vacuum transistor.

Table 3.1. A comparison among the old vacuum tube technology, the modern CMOS technology and the new proposed vacuum tube technology.

	Old vacuum tube technology	**Modern CMOS technology**	**New vacuum tube technology**
Operation speed	~ 100kHz	~ 100GHz	~ 1THz
Mechanism	Thermionic emission	Solid channel	Field emission
Channel length	~ cm to mm	10nm	A few nm
Transport	ballistic	semi-ballistic	ballistic
Temperature	hot	cold	cold
Size	large	small	small
Power	5 W - MW	0.1 - 5 W	~5 - 50 W
Integration	Low level (17,468 in 167 m^2)	High (billions in cm^2)	high
Cost	expensive	cheap	cheap
Reliability	unreliable	reliable	reliable

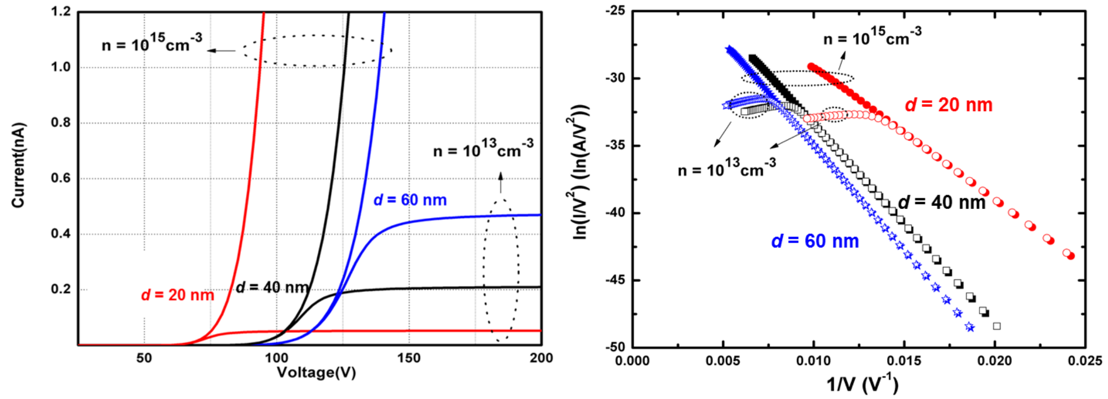

Figure 3.3. (Left) Field emission characteristics of a single silicon nanowire with different diameters and doping densities demonstrating current regulation. (Right) the corresponding FN plot.

Silicon pillar structure as the emitters has been reported as a current limiter to improve the uniformity [38][74] and reliability [75]. These designs utilized FEAs with μm level dimensions of the tips and high doping densities, which prevented them from achieving reliabilities of typical MOSFET devices. The field emitter arrays based on vertical nanowire structure with much smaller dimensions (~nm) will give rise to better current regulation due to the high aspect ratio and tiny cross section area. Borrowing the idea from the operation of MOSFETs, the drain current will saturate after the drain voltage goes above the overdriven voltage. Similarly, the current of the nanowire reaches a saturated state as electric field strength increases beyond a critical value. Any further increase of the electric field strength leads to only slight increment in emission current due to the channel length modulation effect, the same phenomena observed in short-channel MOSFETs. From the drift-diffusion theory, the saturation current is simply given by $I_{sat} = Anev_s$, where A is the cross-sectional area, e is the electron charge, n is the carrier concentration, and v_s is the saturation velocity ($\sim 10^7 \mathrm{cm/s}$ for silicon). This

current-source behavior will help protect the nano-tips from drawing high currents estimated by the Fowler-Nordheim equation and eventual burning out. The current-source behavior also facilitates improved reliability characteristics. As can be seen from the saturation current equation, $I_{sat} = Anev_s$, the current can be well controlled by tuning the carrier concentration. Figure 3.3 (left) shows the emission characteristics with a good control over emission current per tip as the carrier concentration is decreased by a factor of 100. By tuning the applied voltage, almost all the lightly doped tips with diameters ranging from 20 nm to 60 nm can emit current with a nearly constant current density. The heavily doped tips, however, saturate at a very high current, in the regime that the tips may burn out due to Joule heating. Figure 3.3 (right) is the corresponding FN plot. The linear relation for tips doped at density of $1 \times 10^{15}\text{cm}^{-3}$ verifies the current is from field emission without any current control mechanism present. The negative slopes become positive at high voltage for tips doped at density of $1 \times 10^{13}\text{cm}^{-3}$ demonstrating a good control over current due to the saturation mechanism.

3.3 Failure Mechanisms

There are two main mechanisms that will cause the silicon nano-tips to fail. The first one is thermal-related failures including thermal burnout and thermal runaway. The other mechanism is due to the bombardment of ionized residue, which is a result of the presence of atoms in the vacuum that are ionized by high energy electrons.

3.3.1 Thermal Stability

A good control of current leads to a better control of the temperature profile across the array. There are two main temperature restrictions need to be considered. First, the device

needs to operate below the silicon melting point (~1414 ºC). Given the dimensions and operating conditions of SI FEAs, it has been shown that the two heating mechanisms, namely joule heating and Nottingham effect, do not provide enough energy to

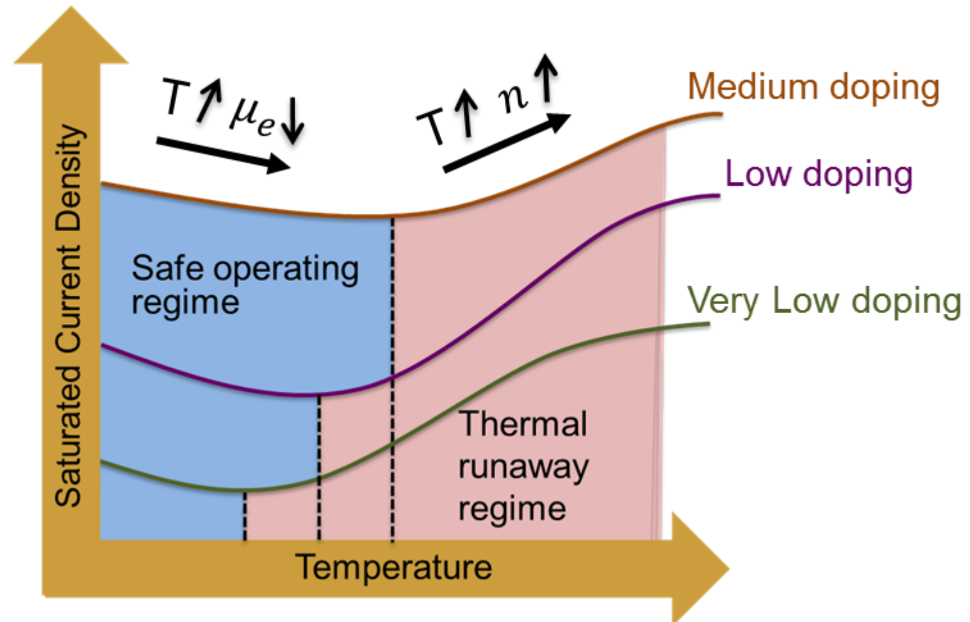

Figure 3.4 FEAs saturated current density as a function of temperature for different doping levels. Safe Operating Area (SOA, blue region) is where the current density negatively depends on the temperature while Thermal runaway area is where current density positively depends on temperature.

trigger a direct failure [76]. The other thermal restriction is the positive feedback thermal runaway, which is already known in power bipolar transistors as the Forward Bias Safe Operating Area (FBSOA) [77]. In fact, for lowly doped semiconductor devices, the conduction occurs in two stages with respect to temperature. At initial stage when temperature is below a certain critical temperature (T_c), temperature increment leads to more scattering of carriers with lattice structure and ionized centers. As a result, the mobility of electrons will decrease. Therefore, in this so-called mobility dominated

transport regime, the current decreases as the temperature increases. However, by further increasing the temperature, more electrons will be invoked from the valance band to the conduction band, giving rise to an increment of intrinsic carrier concentration. In this carrier density dominated region, which occurs beyond the critical temperature (T_c), the current increases as the temperature increases. Higher current will generate more joule heat and the temperature will go even higher. This positive feedback causes a local heating of the device at one or few emitter tips and will eventually cause a fatal failure to the device as illustrated in Figure 3.4.

To extract the safe operating area (SOA) of field emitter arrays, a heat transfer simulation was conducted using COMSOL Multiphysics. Joule heating was considered as the heat source while two main channels for heat outflow were considered: (1) heat

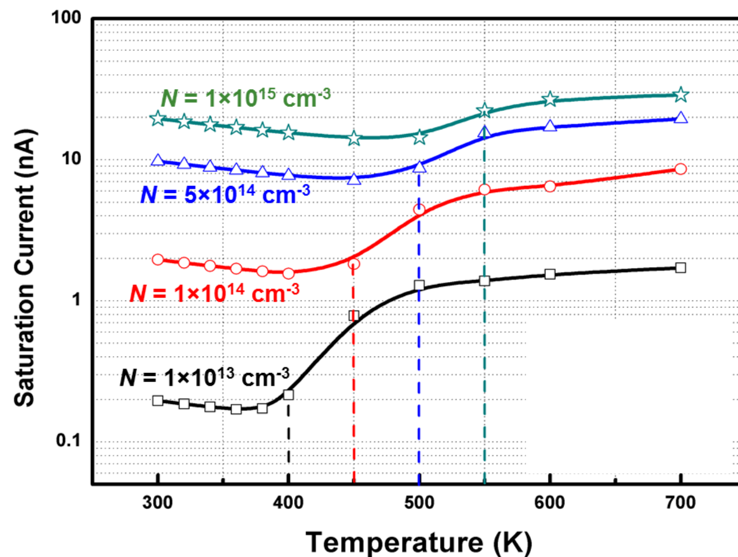

Figure 3.5. Simulation result of saturation current as a function of temperature for different carrier concentrations.

radiation from the surface to the ambient vacuum and (2) thermal conduction through the substrate, which is the dominant heat sinking mechanism in this case. As can be seen from Figure 3.5, the saturation current initially decreases with the ambient temperature and increases after surpassing the critical temperature. This behavior is distinct for different carrier concentrations. The critical temperature between the mobility dominated region and the carrier density dominant region is 400K, 450K, 500K, and 550K for carrier concentrations $1 \times 10^{13}\text{cm}^{-3}$, $1 \times 10^{14}\text{cm}^{-3}$, $5 \times 10^{14}\text{cm}^{-3}$ and $1 \times 10^{15}\text{cm}^{-3}$, respectively. The device should operate below these critical temperatures to avoid thermal runaway. Although this is for nanowires with 40 nm diameter and 3 μm in length, same principle also applies to other dimensions.

3.3.2 Ion Bombardment

Emitted electrons from the nanowire will ionize the residue gas molecules in the chamber, which under the electric field will be sputtered onto the tips causing them to degrade [78]. This ion sputtering will increase the surface roughness of the tip apex. In other words, the phenomenon leads to more microscopically sharp sites on the tip apex. These sharp tiny sites, termed as nanoprotrusion [34], induce a highly concentrated electric field and emit more currents, leading to their burn out. This mechanism can also explain the different fluctuation modes observed in [79].

The velocity (v_{ion}) of the ionized gas molecules that reach the tip apex from the anode can be estimated as:

$$v_{ion} = \sqrt{\frac{2qV}{m_{ion}^*}} \qquad (2.2)$$

where q is the charge of the ionized gas molecule, V is the applied voltage and m_{ion}^{*} is the effective mass of the ion. By reducing the gap between the collector and the tip apex, the voltage required for current emission could be reduced, which would mitigate the ion bombardment. On the other hand, the rate of ion bombardment per unit time can be estimated as:

$$e_i = \alpha n_i \frac{\Omega}{4\pi} S \tag{3.3}$$

where α is the probability of gas molecules being ionized per unit time, n_i is the number density of residual gas molecules, Ω is the solid angle that the tip sees the anode and S is the volumn of the sphere centered at the tip apex with a radius equal to the gap between the collector and the tip apex. α is estimated to be 0.02 when the energy of the hitting electron is 200 eV and it will increase as the energy of the hitting electrons increases [79]. Thus, reducing the gap distance and higher vacuum environment would greatly improve the reliability of the tips.

3.4 Silicon Nanowire Field Emitter Arrays

3.4.1 Simulation

Several parameters can be adjusted to avoid the above mentioned failure mechanisms and enhance the longevity of the tips and maximize the emission current at the same time. To extract the optimized parameters, a comprehensive field emission simulation was conducted using Synopsys Sentaurus software. By self-consistently solving the coupled Poisson equation, carrier continuity equations and the FN equation, the transport

properties under various ambient environment were obtained for a single silicon nanowire with different dimensions.

Three device parameters, namely diameter, length, and carrier concentration, were adjusted for the purpose of obtaining the highest saturation emission current as well as the most effective cooling. The increment of diameter will lead to the increase of thermal conductivity as well as the power dissipated under the saturation regime. The length increase will bring about a decrease of thermal conductivity but an increase in the dissipated power. As carrier concentration increases, the thermal conductivity does not change much while the power dissipated under saturation increases significantly.

Figure 3.6 (left) shows the final steady-state temperature for a single nanowire with different lengths and carrier concentrations when operating under velocity saturation regime. The diameter is $40\ \mathrm{nm}$. The dashed lines represent the critical temperatures, which separate two distinct conduction mechanisms, for different carrier concentrations. As can be seen, the critical temperatures put strong restrictions on the carrier concentration. The only acceptable parameters for Si field emitters are nanowires with a carrier concentration of $1 \times 10^{13}\ \mathrm{cm}^{-3}$ and length below 3 μm. Figure 3.6 (right) shows the steady-state temperature and emission current for devices with different radii and lengths. The carrier concentration is $1 \times 10^{13}\ \mathrm{cm}^{-3}$ and the dashed line is the corresponding critical temperature. As the aspect ratio has to be maintained at least to $50:1$ to ensure the saturation effect [80], the largest diameter is $40\ \mathrm{nm}$, which will give largest possible emission current of $0.2\ \mathrm{nA/tip}$.

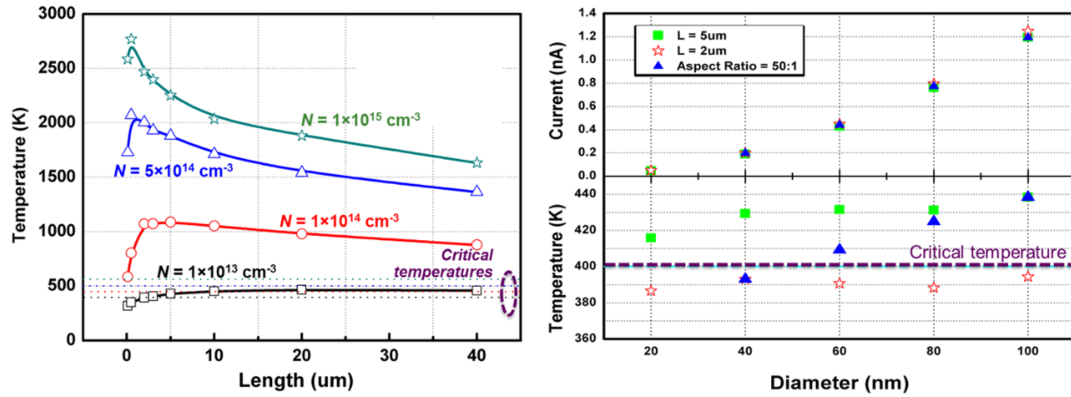

Figure 3.6. (Left) Temperature as a result of operating silicon nanowire field emitters under saturation regime as a function of nanowire length. Dashed lines show the critical temperatures for different doping densities. (Right) Temperature (bottom) as a result of operating silicon nanowire field emitters under saturation regime as a function of diameter and the corresponding current single nanowire (top).

In conclusion, the optimal parameters for silicon nanowires to operate as field emitters under the thermally stable saturation regime are: diameter of 40 nm, length of 2 μm and carrier concentration of $1 \times 10^{13} \text{cm}^{-3}$. This parameter combination will give a current of 0.2 nA per tip.

3.4.2 Design and Fabrication

Two types of silicon nanowire arrays were fabricated. The first one is an ungated two-terminal silicon FEA. The other one is a gated three-terminal silicon FEA. The ungated two-terminal silicon FEAs were fabricated as below. The silicon nanowire array was fabricated using a top-down fabrication approach as depicted in Figure 3.7. First, a thin layer (30 nm) of Al_2O_3 was deposited and patterned using photolithography on top of a low-doped silicon substrate (N type, <100>, 320-480 Ω·cm) to define field emitter active area. Then, a monolayer of silica (SiO_2) nanoparticles with 200 nm average diameters

were deposited using a Langmuir–Blodgett (LB) deposition technique. Parameters of LB deposition were optimized to achieve a very dense film with few defects. A thinning process was performed on the silica nanoparticles by using a dry etching of SiO_2 for 15 and 30 sec. As a result, small spaces (20-50 nm) among the nanoparticles were created as shown in the inset of Figure 3.8. The extra space is essential for the following Si etching process as it allows the plasma to reach Si. A deep reactive ion etching (RIE) of Si was performed with silica particles used as a masking layer. As a result, long Si nanowires with an approximate length of 1.5 – 2 μm were created as shown in Figure 3.8. While the average distance of Si nanowires is set by the diameters of silica nanoparticles (~200 nm), the diameters of Si nanowires depend on the thinning process of silica nanoparticles and dry etching conditions of silicon. The silica nanoparticles were removed using Buffered Oxide Etch (BOE). A commercial 40 μm PET film was used as a spacer between the silicon nanowires and the top anode metal. However, to reduce the gap further, a 10 μm SU-8 was deposited and patterned, to form an alternate approach for the spacer between the Si nanowires and the top Anode metal. The final shape of the nanowire can be well controlled by both silica thinning process as well as the Si dry etching process. In Figure 3.9, the left figure of type (I) sample is achieved by using a thinning process that lasted 15 sec, leading to sharper tips compared to the right figure of type (II) sample achieved with 30 sec of silica thinning process.

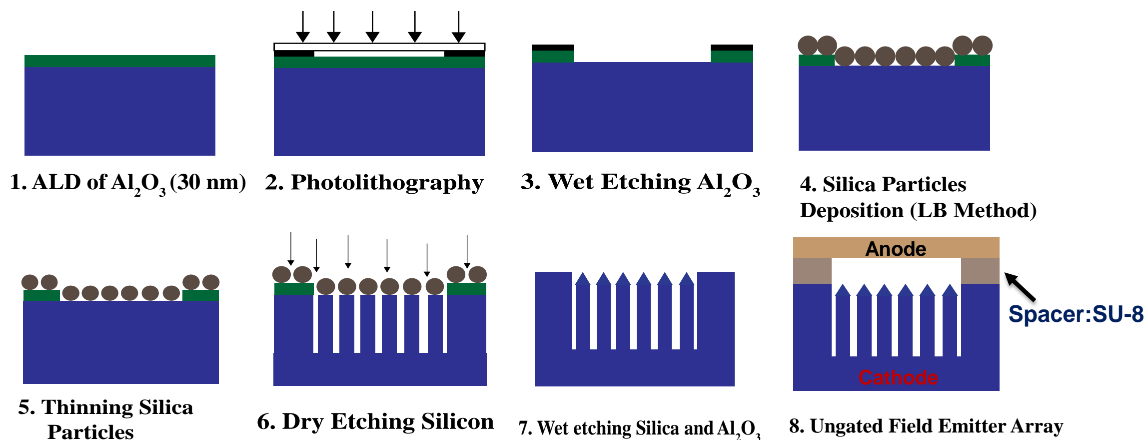

Figure 3.7. The fabrication process of silicon FEAs

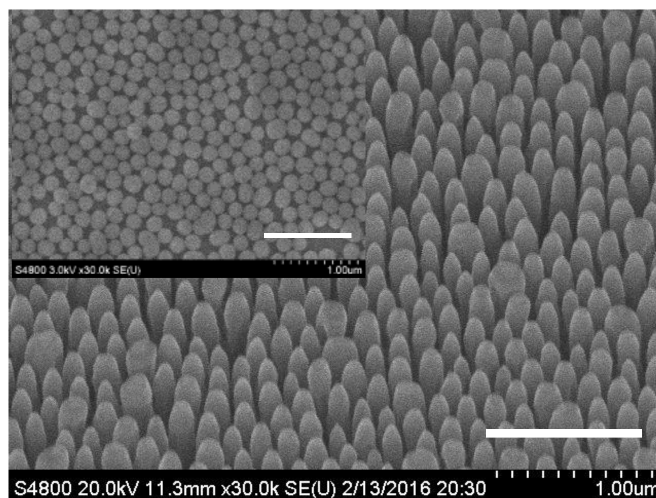

Figure 3.8. An SEM image of the silicon FEA. The inset is an SEM image of silica particles deposited on top of silicon wafer by LB process. The white bars are 1µm in length.

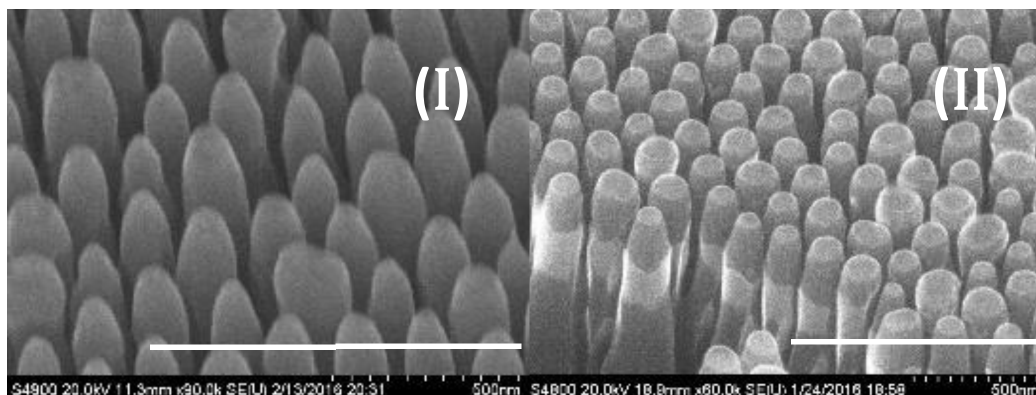

Figure 3.9. Two SEM images of silicon FEA with different tip curvatures. Type (I) sample was achieved by using 30s thinning time of silica particles while Type (II) was thinned for 15s. The white bars are 1μm in length.

The gated three-terminal silicon FEAs were fabricated in a similar way as the ungated devices with some modifications and steps to the process as follows. In the above ungated two-terminal silicon FEAs, after the silica particles were remove by BOE, a 1 μm layer of SiO_2 is deposited onto the wafer to act as a spacer between the cathode and the gate terminal. Then the SiO_2 was planarized. Nickel and Aluminum metals with a thickness of 150 nm and 100 nm were deposited onto the SiO_2 with the gate pattern layer on the photomask using an e-beam evaporator. An SEM image of the patterned metal gate is shown in Figure 3.10 (left). Then, another dry etch step was performed to expose silicon nanowires. The top anode was fabricated with glass, on which metals Nickel and gold with thickness of 100 nm and 70 nm, respectively, were deposited. Then, a layer of SU-8 with a thickness of 5-10 μm was deposited onto the glass. This step is followed by a photolithography development step to open a window of the SU-8 layer such that the metal anode is exposed. The final anode structure with SU-8 spacer is depicted in Figure 3.10 (right).

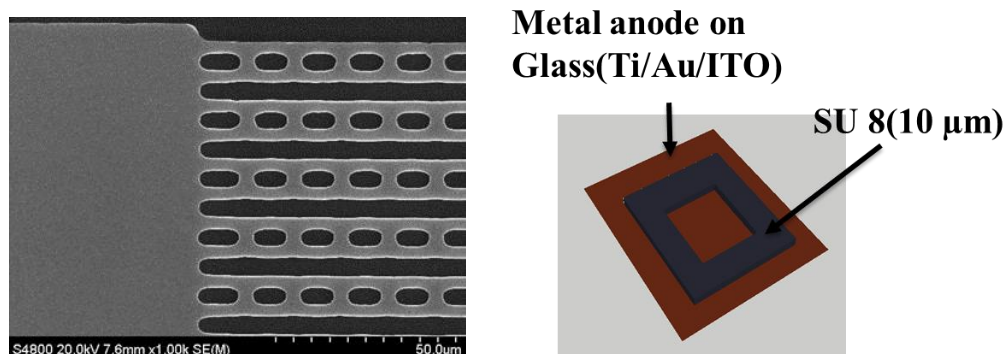

Figure 3.10. (Left) The fabricated Nickel/Aluminum pattern on top of wafer used as the gate in three-terminal silicon FEAs. (Right) The metal anode of the three-terminal FEAs with a 10 μm SU 8 acting as a spacer between the gate and anode.

After the wafer with the gate and the glass with the anode fabricated, the two pieces were affixed together with an optical glue followed by a 5-minute exposure to UV light. The final sample was then mounted on a printed circuit board with the three terminals soldered to form electrical connections to the measurement system.

3.4.3 Device Characterization

The measurements for ungated two-terminal devices were performed inside a vacuum system at a vacuum level of 10^{-7} to 10^{-8} torr. A voltage was applied between the substrate (Cathode) and the top Anode metal (molybdenum) while emission current was measured by a pico-ampere meter. The gap between the tip of Si nanowires and the anode is set by the thickness of the PET film (nominal 50 μm). Figure 3.11 depicts the measurement result for three Type I samples (30 sec of thinning process). The turn-on voltage is around 400V. Although only three samples are shown here, the process is highly repeatable. The

inset of Figure 3.11 is the corresponding Fowler-Nordheim (FN) plot. Figure 3.12 is measured FN plots for various samples. The samples are from two categories: one with 30 sec silica thinning time (Type I), and the other with 15 sec (Type II). Two different FN slopes are observed. Sharp FEA tips fabricated using the 30 second silica thinning process have a slope of 3.2 $A/kV \cdot cm^2$. Tips fabricated with only 15 second of silica thinning process are not as sharp and achieve an FN slope of 8.4 $A/kV \cdot cm^2$. This observation is consistent with FN theory in which, the slope is inversely proportional to the field enhancement factor. Sharper tips have a larger field enhancement factor, thus a smaller slope. The red curves correspond to a FEA device with a small effective emission area of 10^{-5} cm^2, thus they have lower current than the blue curves that correspond to devices with an active emission area of 0.02 cm^2. However, the current density FN plots with different areas are similar, as shown in the figure.

In order to further reduce the turn-on voltage, the PET film was replaced by a 10 µm SU-8 spacer that was deposited and patterned on the sample. An active window is defined by the deposited SU-8 spacer. Figure 3.13 depicted the measured emission characteristics of a sample with an active area 250 µm by 250 µm. The turn-on voltage is about 20 V with a current density of 1.6 A/cm^2 at an electric field of 8 V/µm. To be best of the author’s knowledge, this value is the highest current density ever reported for silicon FEAs in literature. Table 3.2 is a comparison of the measured current density between the device in this work and the published works.

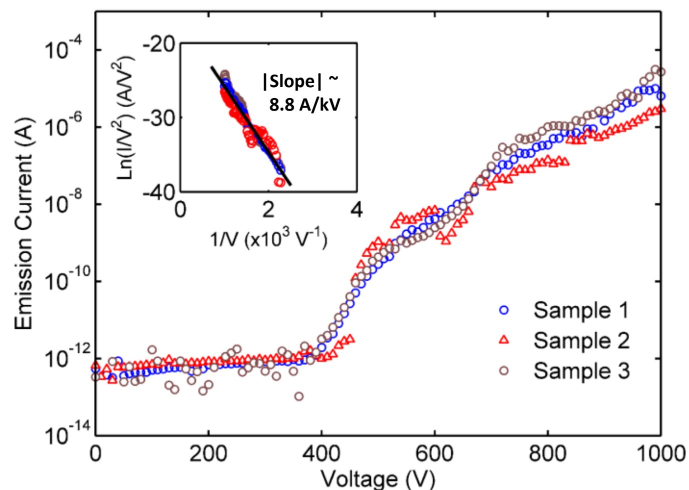

Figure 3.11. Measurement result of ungated two-terminal silicon FEA for different samples. The inset is the corresponding FN plot. The solid line is fit to the data. All three are Type (I) samples in Figure 3.9.

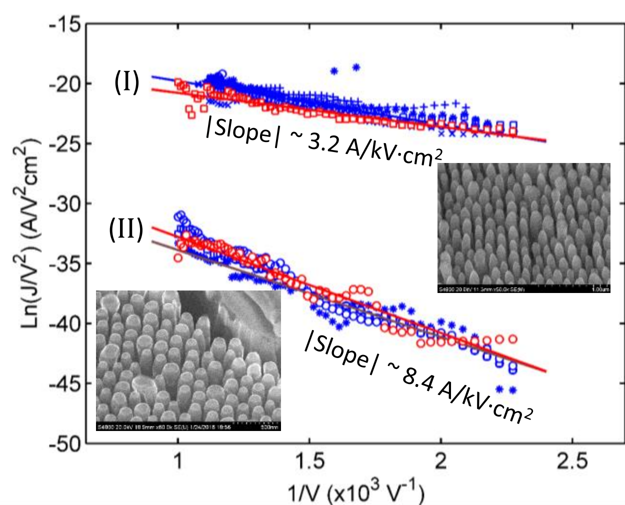

Figure 3.12. FN plots of various silicon FEAs. The solid lines are fit to the data. Type (I) and (II) curves correspond to samples in Figure 3.9, respectively.

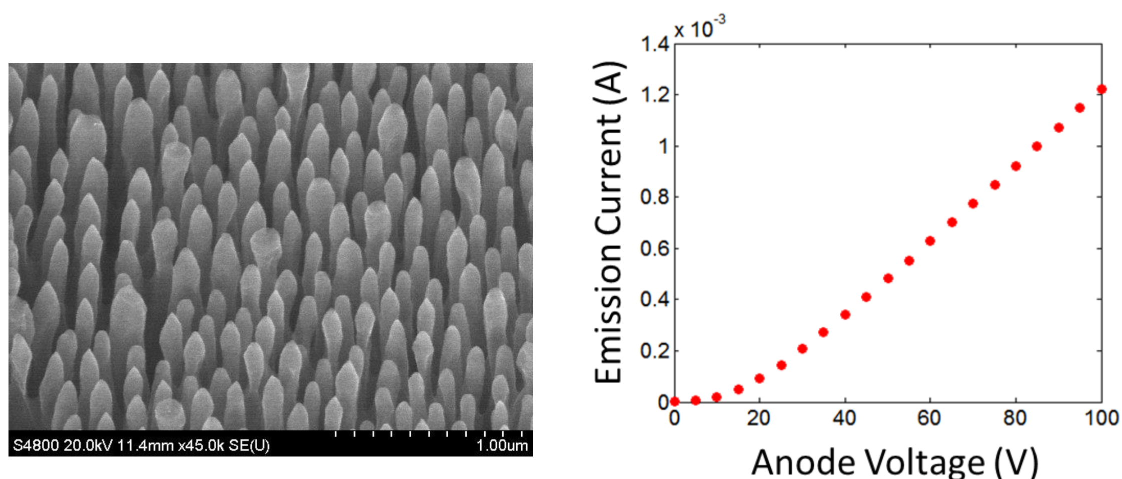

Figure 3.13. (Left) An SEM image of silicon FEAs with tips thinned further to 50 nm in diameter on average. (Right) The measured IV characteristics with a 10 µm SU-8 spacer showing an improved turn-on voltage of 20 V and a current density of 1.6 A/cm^2 at 8 V/µm.

Table 3.2. A comparison of field emission measurement results between the device in this work with other published works.

Reference	**Current Density**	**Dimensions**	**Gap**	**Material**
[44]	0.4 A/cm@14 V/µm		1 mm	SiC
[74]	200 uA/ cm^2@40 V/µm	100 nm	25 µm	Si
[38]	480 mA/cm^2@64 V/µm	1 um	25 µm	Si
[81]	10 µA/cm^2@16 V/µm	45 nm	25 µm	MWCNTs
[43]	1 mA/cm^2@4.7 V/µm			ZnO
[82]	70 mA/cm^2@5 V/µm			CNT
This work	**1.6 A/cm^2@8 V/µm**	**50-70 nm**	**10 µm**	**Si NW**

The gated three-terminal FEAs were measured in the same measurement system with the same vacuum level. A fixed voltage was applied to the gate and the substrate was grounded while the anode was ramped from 0 to 400 V in steps of 5 V. This sweep was repeated for different fixed gate voltages. The measurement result is shown in Figure 3.14. As can be seen from the figure, the emission current is well controlled by the gate voltage. With a higher gate voltage, more electrons will be absorbed by the gate such that less electrons reach the anode metal leading to a decrease in the emission current level. For a gate voltage of 25 V in the current configuration, no current is registered at the anode. Figure 3.15 depicts the corresponding FN plot.

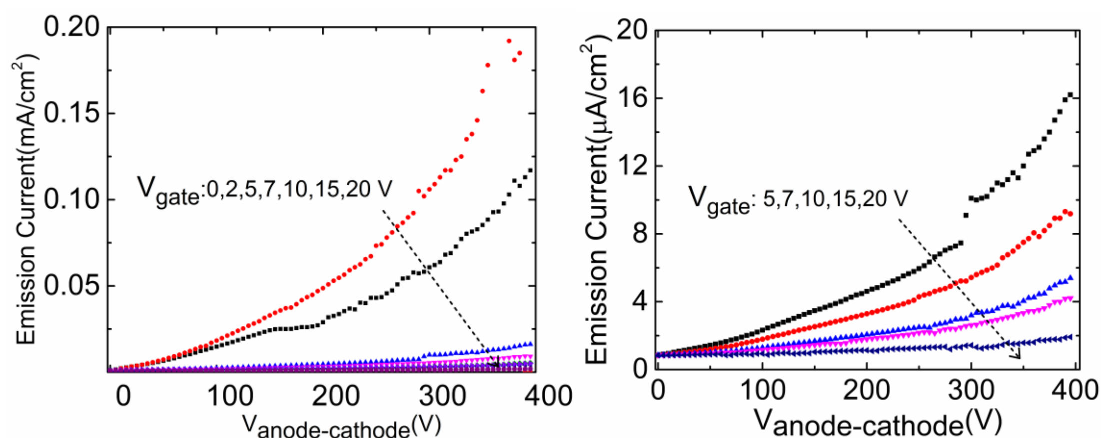

Figure 3.14. The measured IV characteristics of the gated three-terminal FEAs. The right figure is a zoom-in of the left figure with gate voltages of 0 V and 2 V omitted.

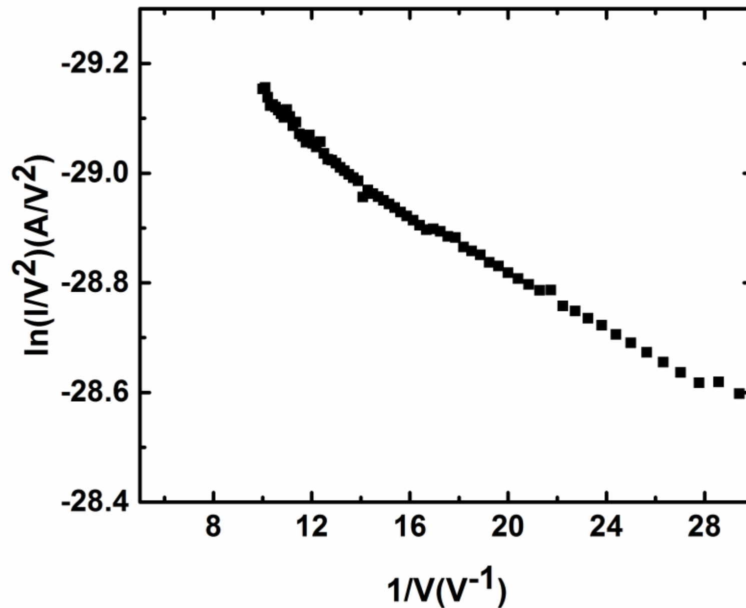

Figure 3.15. FN plot of the measured IV characteristics of the gated three-terminal FEAs.

3.5 Conclusion

In this section, vacuum devices based on silicon FEAs were presented. The proposed solution overcomes various obstacles that current silicon based FEAs suffer from. A new self-assembly technique, LB deposition, has been introduced to fabricate silicon FEAs without using e-beam lithography, leading to very low-cost fabrication of such devices. Silicon nanowire FEAs fabricated with this technique are dense (~75% fill factor), highly repeatable and low-cost. By utilizing thinning of silica particles during the fabrication, the structure and the corresponding emission characteristics are tuned. Furthermore, a comprehensive TCAD simulation was performed to extract the optimal device parameters, such as channel length, width and carrier concentration. With such optimized parameters, the FEAs can achieve thermal stability and achieve the highest possible current density.

The ungated two-terminal FEAs and gated three-terminal FEAs were fabricated and characterized in a vacuum system. A record high current density of 1.6 A/cm^2 has been achieved. Also emission current modulation was demonstrated with a meshed gate structure in the three terminal FEAs. The idea of current control through the current saturation mechanism of each individual silicon nanowire has been investigated. In fact, the high current density of 1.6 A/cm^2 achieved is the outcome of the current limiting mechanism of the sharper tips. This current limiting mechanism can be further proved with a lifetime measurement, which will be left for the future work as discussed in the last chapter of this thesis.

CHAPTER 4. NANO-ELECTRO-MECHANICAL SYSTEMS

4.1 Introduction

In this chapter, two main topics about nano-electromechanical systems (NEMS) are addressed. In the first section, two types of NEMS systems based on CMOS platform are investigated. Optical and electrical characterization techniques are performed on these devices that are fabricated using the GlobalFoundries 45 nm CMOS SOI technology and are post-processed using a recently developed technology at Purdue [83]. In the second section, the compact modeling of double-clamped double-gated silicon NEMS resonators is discussed.

4.2 CMOS NEMS Resonator Characterization

4.2.1 Metal Grid Plate NEMS Resonator

A metal grid plate was designed as a mechanical structure on the CMOS platform and was post-processed as depicted in the inset of Figure 4.1. The mechanical part was designed with the metal layers on GlobalFoundries 45nm CMOS SOI technology and was further released with a wet etching post-processing recipe such that the body of the mechanical part is released while the two ends are anchored. The plate is made of copper with dimensions of 5.40 μm (Length)×4.82 μm (Width)×136 nm (Thickness). Below the copper is the silicon substrate, which acts as a bottom gate that can couple to the metal plate. The left figure of Figure 4.1 depicts the characterization diagram. The device was

driven by an AC signal generated by a signal generator. An additional DC bias was applied to the plate to enhance the electrical forcing between the silicon substrate and the device. A Doppler Laser Vibrometer (DLV), which can detect pico-meter level displacement, was used to characterize the out-of-plane motion of the device. The right figure of Figure 4.1 shows the measured frequency response of the displacement when both DC and AC excitations are present. A clear resonant peak was observed at around 11 MHz. This peak is consistent with different AC and DC excitation configurations as shown with different symbols. The resonant peak only appeared in the released plates verifying the mechanical vibration of the plate.

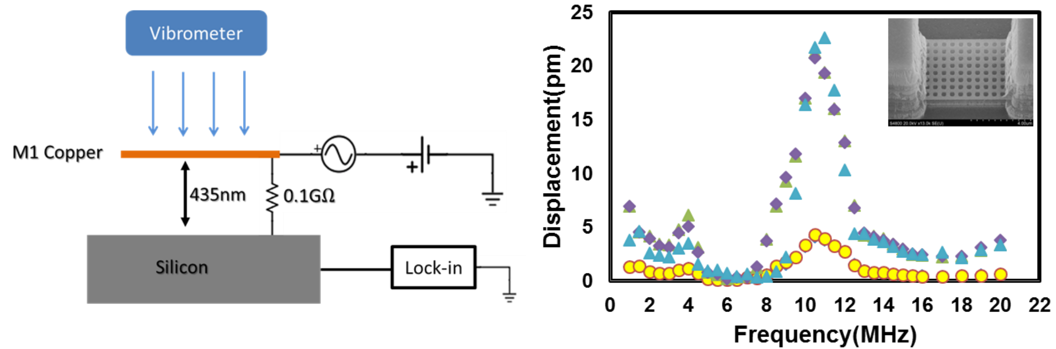

Figure 4.1. (Left) The testing scheme of post-processed metal grid mechanical resonator. (Right) DLV optical measurement result of the metal grid resonator. Different symbols are results with different AC and DC excitation configurations. (Inset) An SEM of the resonator with dimensions: 5.396μm×4.82μm×136nm

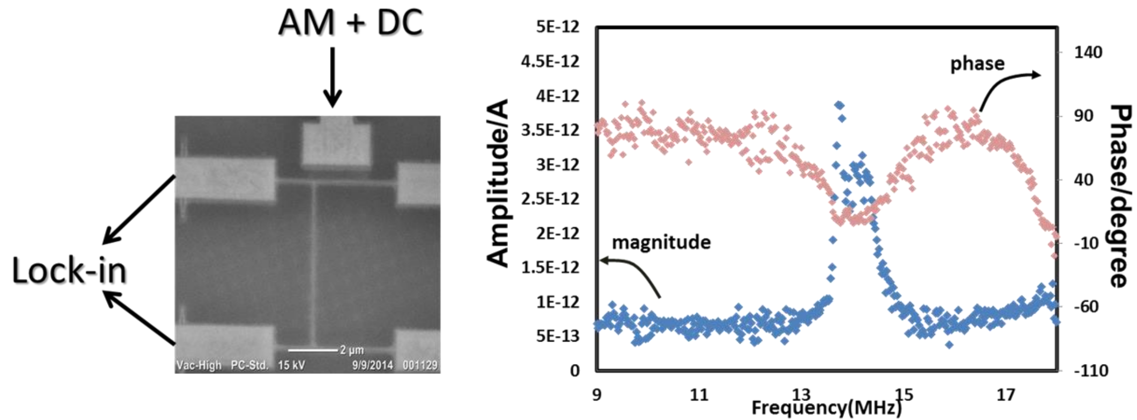

Figure 4.2. (Left) An SEM image of the H-shape resonator and the testing scheme. AM: amplitude modulated signal, Lock-in: lock-in amplifier. (Right) The corresponding measured frequency response.

4.2.2 H-shape Resonator

The second CMOS-NEMS resonator designed, post-processed and characterized is an H-shape resonator as depicted on the left SEM image of Figure 4.2. The resonator was anchored at four ends while a vertical beam lies in between the two parallel horizontal beams. Also, a side gate is placed close to one of the horizontal beams, which can be used either to drive the entire structure or to sense the vibration. The H-shape resonator is also a metal beam made of copper. The measurement diagram is shown in the left figure of Figure 4.2. The beam has a width of only 70 nm. An electrical driving and electrical sensing method was adopted as follows. An amplitude modulated (AM) AC signal with a DC bias was applied to the gate while a lock-in amplifier was used to detect the electrical response of the beam. The signal generator, which was used to generate the AM signal was configured such that the modulation index (m) is 0.5 and the modulation frequency f_m is 1 kHz, while the carrier frequency f_c was swept around the frequency range of

interest, which is around the natural frequency of the device. The lock-in amplifier was configured to measure the signal at 1 kHz. This measurement technique filtered out most of the feedthrough signals such that the weak signal coming from the resonator was much less noisy and had no background signal. The measurement result is shown as the right figure of Figure 4.2. Two adjacent peaks with about a 60 degree phase change were present indicating that different resonant modes were induced, which was expected from the simulation result. However, due to the process variation and the error caused by the dimension measurements, the measured result does not match the simulation result quantitatively.

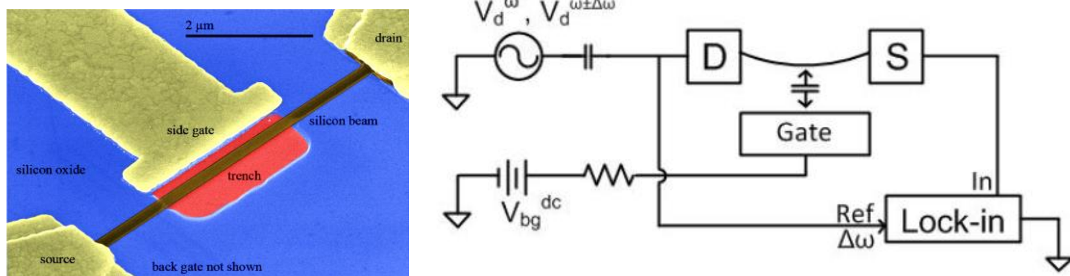

Figure 4.3. (Left) An SEM picture of a representative silicon resonator [84]. (Right) Diagram of the measurement setup [85]

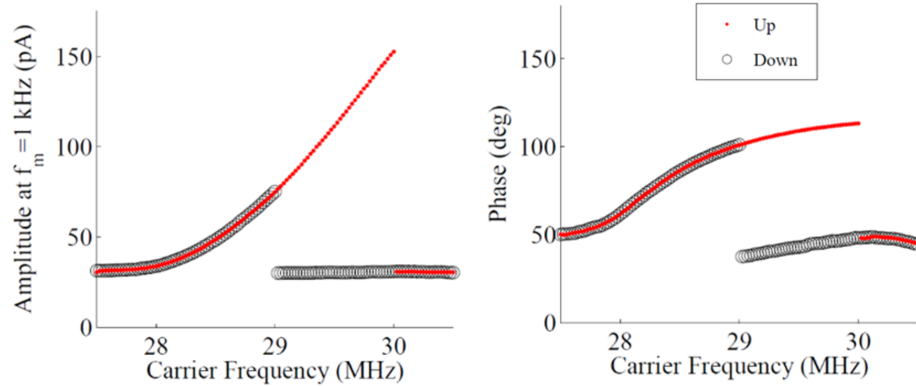

Figure 4.4. Measured magnitude (left) and phase (right) frequency response of the double-clamped silicon resonator [86]

4.3 Compact Modeling of Double-Clamped Silicon Resonators

4.3.1 Experimentation and Characterization

A double-clamped double-gated silicon resonator on SOI platform, which was fabricated and characterized in [84], was modeled. The structure of the resonator is shown in the left picture of Figure 4.3 and the measurement setup is shown in the right figure. The measurement setup is very similar to the previous setup that was used for the H-shape resonator characterization, except that three-terminal measurement was used here. An AM signal was applied to the drain (D) terminal. A lock-in amplifier was used at the source terminal to measure the current at the modulation frequency. A DC bias was applied to the gate. Figure 4.4 is the measured magnitude and phase frequency response of the device. Detailed discussions about the fabrication and characterization of this device are in [84]. In the following sections, a physics based compact model about this device is presented.

4.3.2 Mechanical Equation of Motion

The beam mechanical equation is based on classical Bernoulli-Euler beam model with residual tension, N_1, and midplane stretching [86]

$$\rho A\,\ddot{y}(x,t) + c\dot{y}(x,t) + EI\,y''''(x,t) - \left[N_1 + \frac{EA}{2L}\int_0^L {y'}^2(x,t)\,dx\right] y''(x,t) = F(t) \tag{4.1}$$

where L, w and h are the length, width, and thickness of the beam. ρ is the mass density. E is the modulus of elasticity for the material. $y(x,t)$ is the deflection of the beam at time t and a distance along the beam, x. c is the specific viscous damping coefficient. $I = \frac{1}{12}wh^3$ is the moment of inertia for out-of-plane motion.

4.3.3 Forcing Model

Electrostatic force between the beam and gate per unit length can be described by:

$$F_{pp}(x,t) = \frac{\epsilon_0 w V_{gap}^2(x,t)}{[g - y(x,t)]^2} \tag{4.2}$$

where $V_{gap}(x,t)$ is the instantaneous potential difference between the gate and the beam at some distance along the beam, x. g is the nominal gap size. Equation (4.2) is used to describe the force between two surfaces with uniform gap and potential difference. For deflected beams, the electrostatic forcing through an improved capacitance model can be written as:

$$F = \frac{1}{2} V_{gap}^2 \frac{\partial C}{\partial y} \tag{4.3}$$

where C is the capacitance between the beam and the gate. The forcing model is expanded in a Taylor series around $z = 0$, keeping terms up to z^3. The final forcing equation is,

$$F(t) = \frac{\epsilon_0 w V^2(t)}{90 g^5} [f_0 + f_1 z(t) + f_2 z^2(t) + f_3 z^3(t)] \quad (4.4)$$

where the geometric parameters f_0, f_1, f_2 and f_3 are defined in table 2.

4.3.4 Capacitance Modulation

During operation, the beam and gate act as a variable capacitor, allowing AC current flow through them. Following the above discussion, the capacitance could be described as,

$$C(t) = \frac{\epsilon_0 L}{g} [L + k_1 z(t) + k_2 z^2(t) + k_3 z^3(t)]$$

The charge at time t is

$$Q(t) = C(t) V_{gap}(t)$$

The current is given by

$$i(t) = \frac{dQ}{dt}$$

$$i_{cap}(t) = \dot{C}(t) V_{gap}(t) + C(t) \dot{V}_{gap}(t)$$

This is the current contribution from the variable capacitance with the gate.

4.3.5 Piezoresistive Effect

The resistance of the beam will change when the beam deflects, which will contribute to the total current. The axial strain from mid-plane stretching is

$$\epsilon(t) = \frac{1}{2L} \int_0^L \left[\frac{\partial y(x,t)}{\partial x}\right]^2 dx = 2.44 \left[\frac{z(t)}{L}\right]^2$$

Table 4.1. Coefficients – Dimensional Form [86]

Coefficient	Expression
B_0	$\rho A \int_0^L \phi^2 \,\mathrm{d}x$
B_1	$c \int_0^L \phi^2 \,\mathrm{d}x$
B_2	$EI_b \int_0^L \phi'''' \phi \,\mathrm{d}x - S_r w h \int_0^L \phi'' \phi \,\mathrm{d}x$
B_3	$\frac{EA}{2L} \int_0^L \phi'^2 \,\mathrm{d}x \int_0^L \phi'' \phi \,\mathrm{d}x$
f_0	$45 g^3 \int_0^L \phi \,\mathrm{d}x$
f_1	$g^2 \left[90 \int_0^L \phi^2 \,\mathrm{d}x - 2g^2 \left(15 \int_0^L \phi'' \phi \,\mathrm{d}x + g^2 \int_0^L \phi'''' \phi \,\mathrm{d}x \right) \right]$
f_2	$135 g \int_0^L \phi^3 \,\mathrm{d}x + g^3 \left(-15 \int_0^L \phi'^2 \phi \,\mathrm{d}x + 3g^2 \int_0^L \phi''^2 \phi \,\mathrm{d}x + 4g^2 \int_0^L \phi''' \phi' \phi \,\mathrm{d}x \right) + 2g^3 \left(-15 \int_0^L \phi'' \phi^2 \,\mathrm{d}x + g^2 \int_0^L \phi'''' \phi^2 \,\mathrm{d}x \right)$
f_3	$180 \int_0^L \phi^4 \,\mathrm{d}x - 30 g^2 \int_0^L \phi'^2 \phi^2 \,\mathrm{d}x - 30 g^2 \int_0^L \phi'' \phi^3 \,\mathrm{d}x + 48 g^4 \int_0^L \phi'' \phi'^2 \phi \,\mathrm{d}x$
f_c	$\frac{\epsilon_0 w V^2(t)}{90 g^5}$
κ_1	$\frac{1}{g} \int_0^L \phi \,\mathrm{d}x$
κ_2	$\frac{1}{g^2} \int_0^L \phi^2 \,\mathrm{d}x + \frac{1}{3} \int_0^L \phi'^2 \,\mathrm{d}x + \frac{g^2}{45} \left(\int_0^L \phi''^2 \,\mathrm{d}x + 2 \int_0^L \phi''' \phi' \,\mathrm{d}x \right)$
κ_3	$\frac{1}{45 g^3} \left(45 \int_0^L \phi^3 \,\mathrm{d}x + 6 g^4 \int_0^L \phi'' \phi'^2 \,\mathrm{d}x + 15 g^2 \int_0^L \phi'^2 \phi \,\mathrm{d}x - g^4 \int_0^L \phi''^2 \phi \,\mathrm{d}x - 2 g^4 \int_0^L \phi''' \phi' \phi \,\mathrm{d}x \right)$

With the transverse and shear stresses neglected, the beam resistance could be described as

$$R_{beam}(t) = R_0[1 + \epsilon(t)G_R]$$

where $R_0 = \frac{\rho_r L}{wh}$ is the nominal beam resistance, G_R is the resistance gauge factor given by,

$$G_R = 1 + 2\nu + E\pi_L$$

which accounts for both geometric effects, $1 + 2\nu$ (ν is Poisson's ratio) and piezoresistive effects, represented by $E\pi_L$. π_L is the effective longitudinal piezoresistive coefficient, which has a dependence on crystal orientation and other parameters such as doping and temperature. With all these effects accounted, the final beam resistance equation can be described as,

$$R_{beam}(t) = \frac{\rho_r L}{wh}\{1 + 2.44\left[\frac{z(t)}{L}\right]^2 (1 + 2\nu + E\pi_L)\}$$

which depends on the beam deflection.

4.3.6 Equivalent Circuit Representation

Figure 4.5 is the equivalent circuit representation of the beam and the measurement setup. There are variable capacitors between gates and beam and piezoresistors for each half of the beam. The equations that describe the variable capacitances and beam piezoresistances can be found above. When the device operates, there will be two AC currents flowing into the source, one from the drain, the other from the gate. These currents are modulated by how the beam deflects and both contribute to the output current.

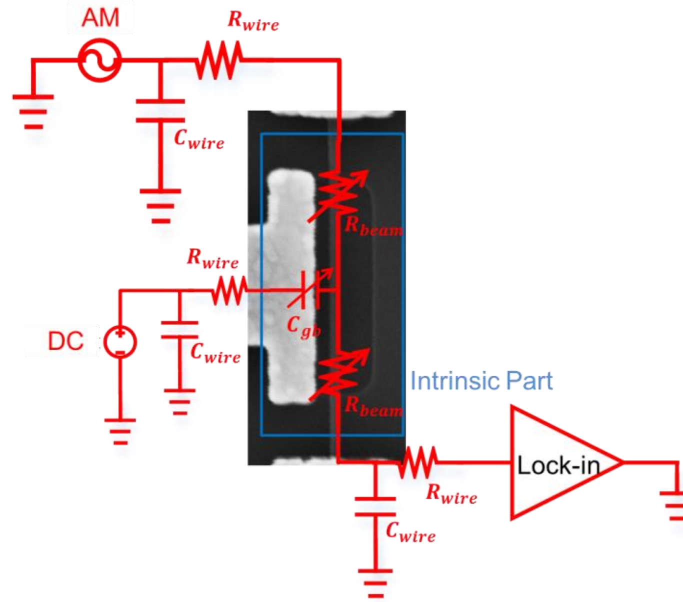

Figure 4.5. Equivalent circuit representation of the beam and measurement setup

4.3.7 Simulation

Figure 4.5 shows the experimental testing circuit as well as the simulation testbench circuit. An AC signal (modulated or not) is applied to the drain of the beam while the source is connected into a lock-in amplifier. A DC voltage is applied to the gate. Various parasitic are considered here, including the wire capacitance, wire resistance, contact resistance, leakages and so on. Output current/voltage at the lock-in amplifier is measured.

For the circuit simulation, spectreRF harmonic balance solver is used. For this simulation that requires high accuracy, a conservative accuracy is set. Also, in the simulator option, the relative tolerance (reltol), voltage absolute tolerance (vabstol) and current absolute tolerance (iabstol) is set to be 10^{-8}. To help the convergence, the transient-aided HB (tstab) is set to be 10^{-4}s.

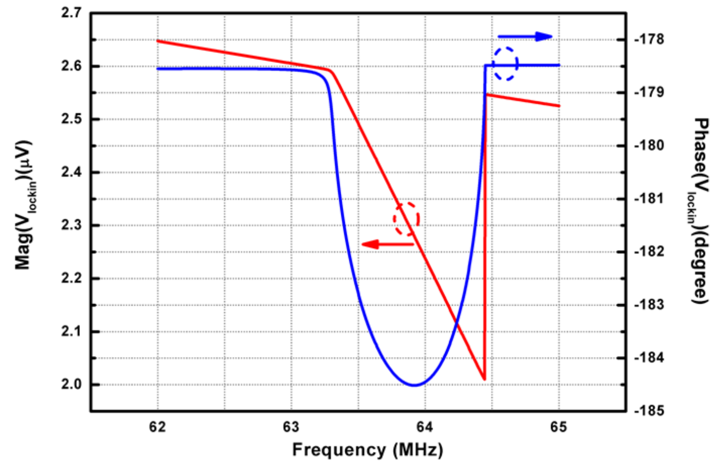

Figure 4.6. Frequency response of the beam driven by a single-tone excitation. Red line is the magnitude. Blue line is the phase.

4.3.7.1 Single-tone excitation

This is a test of the system driven by a single tone AC excitation. Beam dimension is 4 μm in length, 110nm in thickness, 180nm in width while the gap between the beam and gate is 144nm. Figure 4.6 is the frequency response under a 40 mV_{rms} AC excitation and 6V DC back gate bias. This simulation is to measure the output voltage across resistor of the lock-in amplifier under different sweeping frequencies. A clear resonant peak and phase change is observed at 64.4 MHz.

4.3.7.2 Multi tone simulation

This is a test of the system driven by an amplitude modulated (AM) AC signal. Beam dimension is 5.9 μm in length, 110 nm in thickness, 180 nm in width while the gap between the beam and gate is 144nm. Figure 4.7 is the frequency response. The

modulation factor (M) is 0.5 and the modulation frequency is 1kHz. The amplitude of the carrier signal is $40\ mV_{rms}$. 6V DC is applied to the back gate. The simulation is to measure the output current under the modulated frequency 1kHz, while the carrier frequency is swept around the natural frequency. Also, under this excitation condition and bias condition, strong nonlinearity and hysteresis start to emerge.

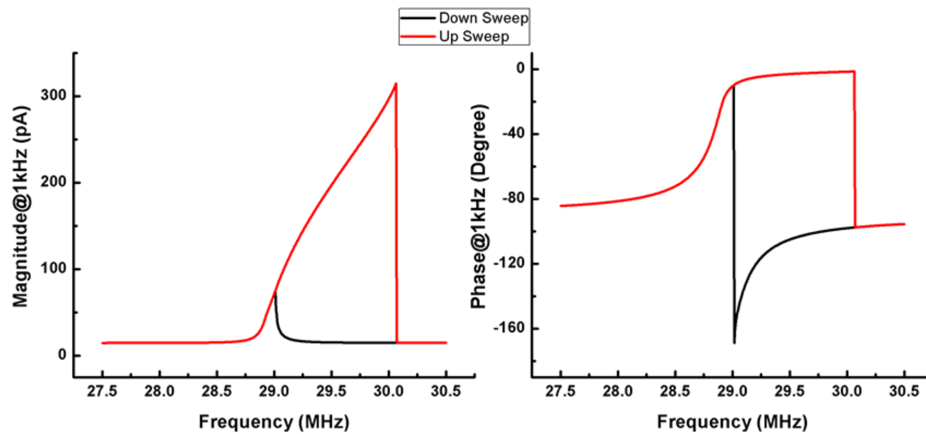

Figure 4.7. Frequency response of the beam under an amplitude modulation excitation. Frequency response of magnitude (left) and phase (right) of the output current at modulated frequency 1kHz. Red curves are the response when the carrier frequency is up-swept while the black curves is down-swept

4.4 Conclusion

Two types of CMOS integrated NEMS resonators were designed, fabricated and characterized using optical and electrical characterization techniques. The results indicated promising future for NEMS integration within the CMOS platform. Also, a compact model for double-clamped silicon nanoresonator is constructed. The model covers capacitive modulation and piezoresistive effect, which are the two dominant

effects in nanoresonators. This model is also able to capture various linear and nonlinear behaviors and hysteresis effect, which may be critical in some practical applications.

CHAPTER 5. FUTURE WORK

5.1 Process Design Kit (PDK)

A comprehensive NMOS model that predicts DC, RF and noise behavior on the GlobalFoundries 45 nm CMOS SOI platform has been completed. In the future, there are several aspects that need to be addressed as follows.

1) Extend this NMOS model to cover more physical effect, such as kink effect, various breakdown mechanisms, such as source-drain reach-through, source-drain breakdown and gate oxide breakdown, low-frequency noise, lifetime and statistical variations of various device parameters;
2) Extend the NMOS model to predict the PMOS behavior;
3) Construct the models for passive elements, such as resistors, inductors, capacitors, coupled lines, and transmission lines, etc.
4) Construct a process design kit (PDK) for this technology based on the compact models on active and passive devices;
5) Further verify the accuracy, efficiency, performance of the PDK models through a more complex RF systems design.

5.2 High Frequency Nano-Vacuum Tube Devices

In this thesis, an integrated silicon FEA-based vacuum transistor has been demonstrated for the first time. A low-turn on voltage of 20 V and a high current density of 1.6 A/cm^2 have been achieved. However, with proper tip sharpening, an ideal current saturation with a current density of 16 A/cm^2 is expected with a low turn-on voltage of less than 5 V. This level of current density and the aforementioned individual current control through current saturation mechanism need to be verified. In the future, the high resistivity substrate needs to be replaced with a highly doped substrate with a low-doped cap layer such that the current control only appears at each individual silicon nanowire and not in the bulk of the substrate. Also, a comprehensive lifetime study should be performed for devices that demonstrate such current saturation mechanism.

The aim of vacuum transistor was to achieve a high current density device for high frequency and high power transistor application. Furthermore, CMOS-integration is a key advancement for this device to enter the market. Similar devices have been designed on the GlobalFoundries 45 nm CMOS SOI platform as shown in Figure 5.1 (left). The silicon emitter tips have a dimension of 140 nm by 140 nm. The device was post-processed to release the silicon emitters as depicted in Figure 5.1 (right). Through post-processing, the tips can be further thinned down to less than 10 nm. Also, two layers from the CMOS Back-End-of-Line (BEOL) were used as the gate and anode electrodes. The DC and high frequency characterizations are yet to be performed on these devices. Given the device dimensions in this technology, a rough estimate of a cut-off frequency 1.2 THz and maximum oscillation frequency of 2.2 THz may be achievable. Also, this device is expected to deliver 10-100 Watts at ~100 GHz.

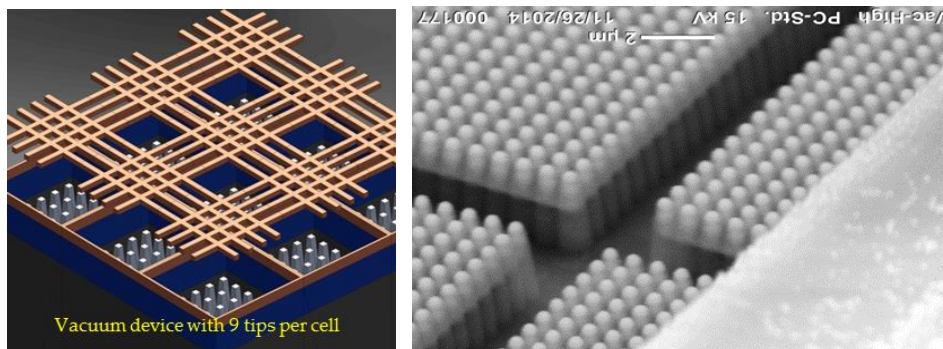

Figure 5.1. Vacuum transistors implemented on the GlobalFoundries 45 nm CMOS SOI platform (left) and an SEM image of the device after post-processed to release the silicon emitters (right).

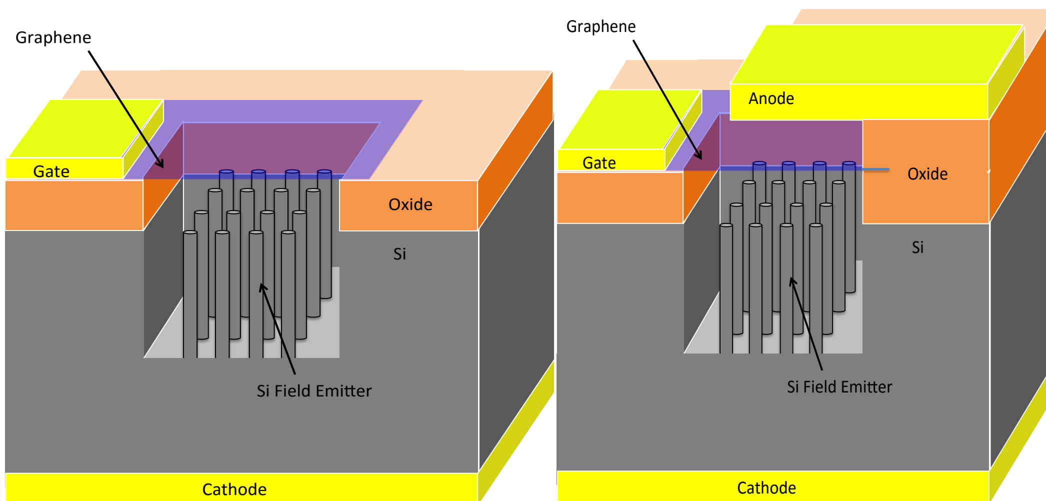

Figure 5.2. Implementation of silicon FEAs with transparent monolayer graphene gate before placing anode (left) and after adding anode (right).

Another direction to pursue is to replace the metal mesh gate with a transparent Graphene gate as depicted in Figure 5.2. Free-standing suspended Graphene has been

demonstrated to be largely transparent to and unaffected by an electron beam with an energy of 30 keV. Compared to its metal counterpart, Graphene gate will have a much higher anode collection efficiency, leading to a higher cut-off frequency and maximum oscillation frequency.

5.3 Future Nano-Electromechanical Sensing Systems

For the future research on NEMS devices, there are two directions that can be pursued, namely experimentation and modeling. In the experimentation part, a more complex mass sensing system or signal processing system can be designed on this CMOS platform. For example, a brand new type of NEMS resonators was designed as shown in Figure 5.1. In this design, a number of double-clamped resonators acting as band-reject resonators and filters work to null undesired frequencies of a receiver module. In addition to these resonators, an output amplifier that mimics the receiver and shows a flat gain for the frequency range of interest, such that very weak signals can be detected was designed as shown in Figure 5.2. For the characterization, an AC signal will be applied to the middle of a transmission line in between the resonators and a DC bias will be applied to the resonators. After the beams are released with the above simple post-processing fabrication steps, an electrical force between the transmission line and the resonator will be induced by both the AC signal and DC signal applied to the beams. Some portion of the AC power at the frequencies of resonance of these beams will be passed through the coupling capacitors with the beams. So a notch-type response at the resonant frequency is expected at the output of the amplifier. Also, a series of resonators with different dimensions along the transmission line were carefully designed and engineered such that

some of them have close resonant frequencies, which will lead to their interaction as a multi-pole filter. Another flexibility in terms of tuning is the inherent resonant frequency shift due to the spring softening/hardening effect caused by the DC bias. The band-reject resonators together with a well-designed low noise amplifier makes a mechanical RF front end receiver, which will have much higher quality factor compared to its electrical alternatives. Furthermore, this level of CMOS integration helps with the advancement of SoC integration. Such studies provide us with the opportunity to investigate the signal processing application of the device.

With regards to the modeling effort, the current compact model of the double-clamped resonator only predicts the behavior in a qualitative sense. In the future, this model can be extended to a quantitative matching as in the final circuit design scenario, where the qualitative analysis is not enough. Also, the current model aims at silicon-based resonators. A model that can predict the behavior of metal resonators is crucial for the CMOS applications. Effects, such as spring softening/hardening effect, piezoresistive effect, etc, will need to be modified in modeling of such devices.

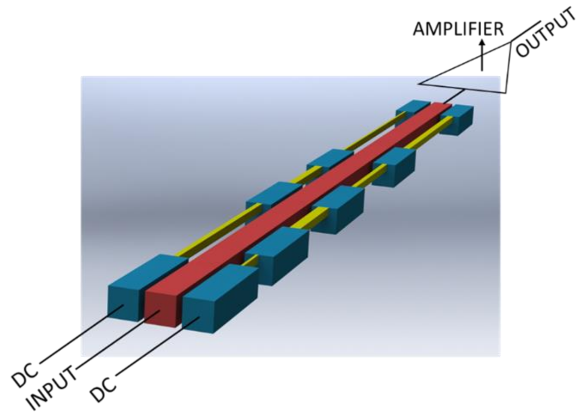

Figure 5.3. A diagram showing the transmission line resonators with testing scheme. The yellow parts are the resonators with different dimensions. The red line is the input line for the amplifiers. The blue boxes are the anchors for the resonators.

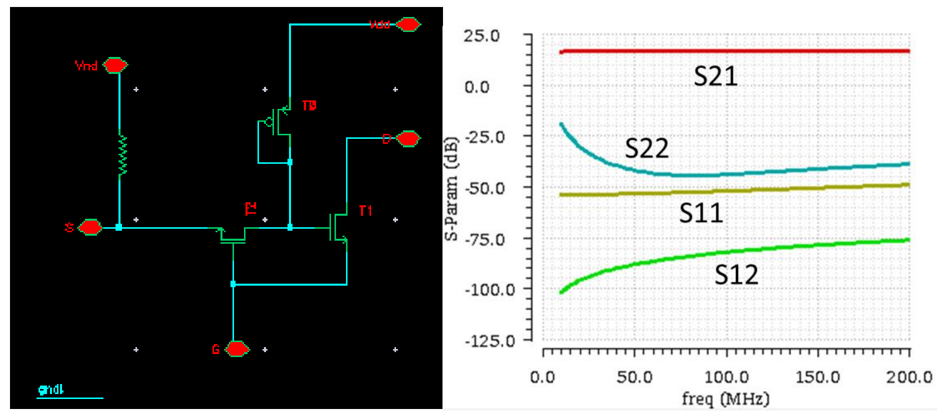

Figure 5.4. Circuit schematic of an output amplifier for the nano-resontors (left) and simulated S-parameters of the amplifier (right).

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VITA

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Yanfei Shen received his Bachelors of Science in physics from University of Science and Technology of China in 2010, a Masters in Science in physics from Purdue University, West Lafayette, IN in 2013, a Masters in Science in computer science from Purdue University, West Lafayette, IN in 2016, and Ph.D. degree in physics from Purdue University, West Lafayette, IN, in 2016. His research interests include compact modeling of nanoscale devices, nanoscale device simulation, high frequency characterization and modeling.