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From Process to Circuits: New Perspectives to Solar Cell Design

Elif Selin Mungan
Purdue University

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MUHAMMAD A. ALAM, Co-Chair

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FROM PROCESS TO CIRCUITS:
NEW PERSPECTIVES TO SOLAR CELL DESIGN

A Dissertation

Submitted to the Faculty

of

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To my dearest coauthor in life, without whom this PhD wouldn’t be possible.

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ABSTRACT

Mungan, Elif Selin. Ph.D., Purdue University, May 2015. From Process to Circuits: New Perspectives to Solar Cell Design. Major Professors: Kaushik Roy and Muhammad Ashraful Alam.

As the demand for cheap and clean energy sources increased over the last two decades, solar cells have proven to be strong candidates against the fossil fuels. From an economic perspective, in order to replace fossil fuels, it is required to reduce the cost of solar cells. This can be achieved by depositing thinner absorber layers under low process temperatures, yet these efforts lead to poorer efficiency values. Addressing such trade-offs and providing solutions to this problem have been the main objectives of this study.

In this research, we have approached the aforementioned problem from two distinct approaches. The first one is to look at the correlation between the fabrication conditions and the performance of the cell, while the second one is to investigate the interaction between the solar cell and the power conditioning circuitry. Following our first approach, we started from the deposition conditions of thin films and addressed their effects on the efficiency of the solar cells made out of these films. Using numerical simulations, we were able to identify the effect of various changes in the copper indium gallium diselenide (CIGS) and CdTe solar cells due to deposition conditions. Within the context of our second approach, we demonstrated that the performance of a polycrystalline Si based energy scavenging system can be improved, provided that the optimization for the solar cell and the power conditioning circuitry is done simultaneously. Finally, these approaches were combined to study the effects of process conditions on the device, circuit and system levels.

1. INTRODUCTION

1.1. The Need for a Green Energy Source: Photovoltaics

Since the early 20th century, the amount of CO_2 released to the atmosphere increased as a byproduct of industrialization process all over the world. This excess CO_2 led to the greenhouse effect, which increased the surface temperature of Earth. With the increase in the fossil fuel consumption, the increase in surface temperature has taken a steeper slope in the last 50 years [1]. This alarming fact underlined the need for alternative energy resources with no or minimum carbon footprint. In addition, fossil fuels are limited resources and the increasing demand for oil reduces the energy independency of the nations while causing conflicts all over the world. From the possible options, sun is the most promising candidate to replace the fossil fuels given the fact that only 0.4% of US land covered with solar cells would be enough to generate the nation's energy demand [2]. Yet, in order to replace fossil fuels, the cost of the generated electricity should be low as well. Even though the solar module prices dropped 57% in the last 10 years [3], the levelized cost of solar energy ($/kWh) is still higher than that of fossil fuels [4].

As the first and widely used photovoltaic (PV) technology, single-crystalline Si (c-Si) solar cells generally employ high temperature processes and thick Si layers (~400μm) to absorb the whole spectrum of sunlight [5]. In order to reduce the cost of a solar cell, one can reduce the amount of material used or the process temperature during the fabrication. The first approach led to thin film solar cells, which required highly absorptive materials such as CIGS and CdTe to collect all of available the photons. On the other hand, the second approach affected the crystallinity of the materials and led to usage of amorphous, microcrystalline and polycrystalline materials. Although they might not be single-crystalline, thin film solar cells demonstrated efficiency values comparable

to that of c-Si technology as shown in Fig. 1.1. Yet, to compete with a mature technology like c-Si, a deep understanding of these materials is required. Therefore, the focus in this research has been the mechanisms limiting the efficiencies of thin film solar cells, specifically solar cells made out of polycrystalline Si (poly-Si), CdTe and CIGS.

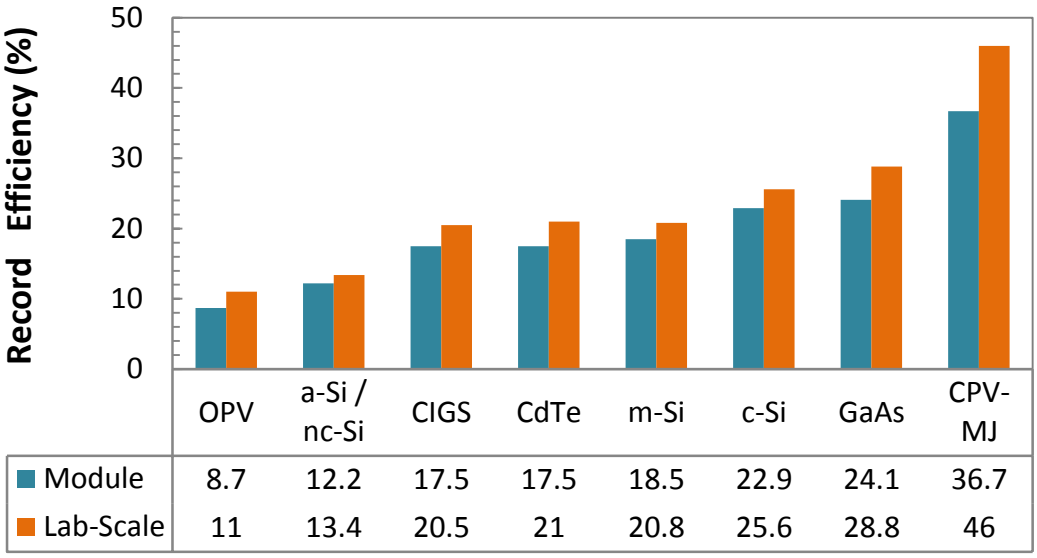


Fig. 1.1 Best lab-scale cell (orange) and typical module level (blue) efficiencies for various solar cell technologies as of 2015. (Data is courtesy of Green et al. [6])

Organic PV (OPV), amorphous and nanocrystalline Si tandem cells (a-Si/n-Si),copper indium gallium diselenide (CIGS), multicrystalline Si (mc-Si), single-crystalline Si (c-Si), and concentrator PV (CPV) with mulit-junctions (MJs)

1.2. Fundamentals of Photovoltaics

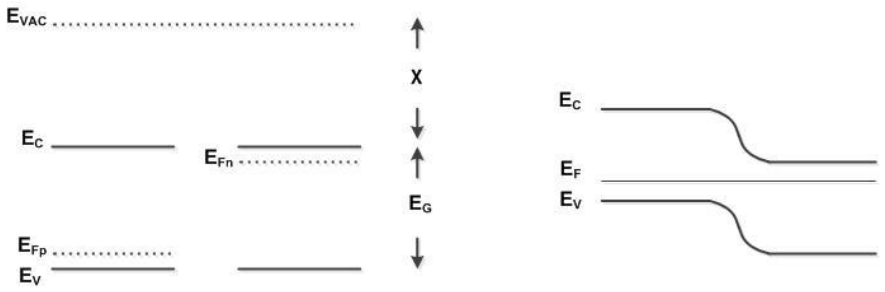
1.2.1. Photovoltaic Effect

The solar cells make use of the photovoltaic effect to convert the sun's energy to electricity. The photons coming onto a semiconductor excites an electron from the valence band to the conduction band, leaving a hole behind. Thus, an electron-hole pair is generated which can be collected at contacts in the presence of an electric field. Yet, all photons in the sun's spectrum might not be collected. In order for a photon to excite an electron, it should have energy larger than the bandgap of the absorber material which limits the efficiency of a solar cell. For instance, photons with energies smaller than

1.1eV cannot be collected with a single c-Si cell. In addition, the conduction band minima (E_C) and the valence band maxima (E_V) of Si do not have the same momentum which makes Si an indirect bandgap material. Because of this bandgap structure, the excitation of an electron from valence band requires the presence of a phonon to occur. Therefore, this event is less likely to happen in Si compared to the direct bandgap materials with aligned E_C and E_V such as CIGS and CdTe.

1.2.2. Solar Cell Configurations and Band Diagrams

The electric field required to collect the generated electron-hole pairs in a solar cell is generally provided by the built-in voltage of a pn or p-i-n junction. Depending on the electron affinities of materials forming the junction (χs), a homojunction or a heterojunction can form. For instance, polycrystalline Si solar cells are homojunctions (see Fig. 1.2) while CdTe and CIGS solar cells are preferred to be heterojunctions. Since CdTe and CIGS materials are generally p-type materials and are hard to dope, they are coupled with n-type CdS layers which create the heterojunction. In this study, the CIGS solar cells are assumed to be Type I heterojunctions with fully overlapping bandgaps and a positive conduction band offset (ΔE_C) (see Fig. 1.3.b), whereas the CdTe solar cells are assumed to be Type II heterojunctions with staggered bandgaps and a negative ΔE_C (see Fig. 1.3.d).



(a) (b)

Fig. 1.2 The band diagrams of p and n-type materials before and after they form a homojunction

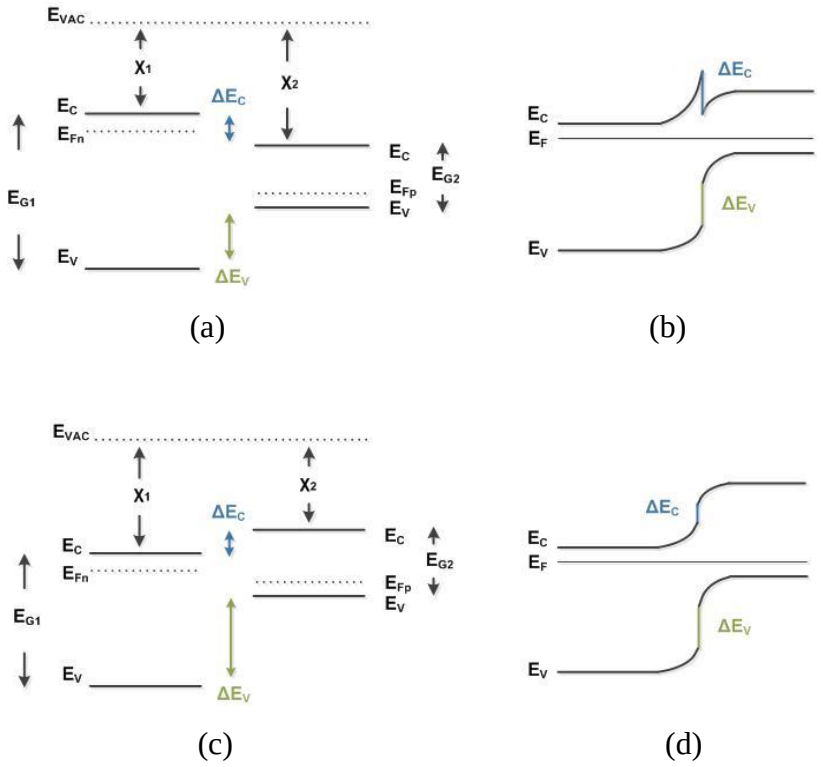


Fig. 1.3 The band diagrams of p and n-type materials before and after they form: a Type I heterojunction (a, b) and a Type II heterojunction (c, d)

1.2.3. Carrier Transport in Solar Cells

In a polycrystalline homojunction pn diode, the relationship between the charges in a device and the electric field is given by the Poisson equation:

$$\nabla.(\epsilon\nabla\varphi) = -q(p - n + N_D + N_A) - \rho_{Trap} \tag{1.1}$$

where ϵ is electrical permittivity, φ is electrostatic potential, p, n, N_D, N_A are densities of holes, electrons, ionized donors and acceptors, and ρ_{Trap} is the charges at the traps within the device. In non-equilibrium conditions (under bias and/or illumination), the quasi Fermi levels for electrons and holes (F_n, F_p) split in the bandgap and determine the carrier densities as:

$$n = n_i e^{(F_n - E_i)/kT} \tag{1.2}$$

$$p = n_i e^{(E_i - F_p)/kT} \tag{1.3}$$

where n_i, E_i and k are the intrinsic carrier density, intrinsic Fermi level and Boltzmann constant. The diode current can be determined from the slope of F_n and F_p which gives the following transport equations for electrons:

$$J_n = \mu_n \mathrm{n} \nabla F_n \tag{1.4}$$

$$= q\mu_n n \nabla \varphi + qD_n \nabla n \tag{1.5}$$

where q, μ_n and D_n are the charge, mobility and diffusion constant of electrons. The Equation (1.4) can be extended to be Equation (1.5) in which the carrier transport is described by two competing processes, namely, drift and diffusion mechanisms consecutively. Similar expressions can also be written for hole current density:

$$J_p = q\mu_p \mathrm{p} \nabla \Phi_p \tag{1.6}$$

$$= q\mu_p p \nabla \varphi - qD_p \nabla \mathrm{p} \tag{1.7}$$

The change in the number of carriers in a diode over time is given by the following continuity equations:

$$\frac{dn}{dt} = \frac{1}{q} \nabla . J_n - R_n + G_n \tag{1.8}$$

$$\frac{dp}{dt} = \frac{1}{q} \nabla . J_p - R_p + G_p \tag{1.9}$$

where R and G terms stand for recombination and generation rates within the diode. The R term can contain multiple recombination mechanisms. For indirect bandgap materials such as c-Si, Auger recombination mechanisms dominate while it is the radiative recombination mechanism for direct bandgap materials like GaAs [7]. On the other hand, the efficiencies of polycrystalline solar cells are limited by the Shockley-Read-Hall recombination (SRH) occurring at their defective regions or surfaces [8]. In steady state, dn/dt term in Eq. (1.8) becomes zero which leads to the equation for the DC condition.

It should be noted that these sets of equations are valid for homojunctions. Attention should be paid while dealing with heterojunctions since modifications are required to accommodate the change in the ϵ value and the abrupt potential change from one material to another [9].

1.2.4. Figure of Merits and Compact Model

The transport equations set in Section 1.2.3 can be solved to determine the current of a pn diode in dark (I_{dark}) and it can be superposed with the generated current under illumination at short circuit conditions (I_{Light}) to obtain the I-V characteristics of a solar cell. If the series resistance is negligible, the I-V characteristic in the first quadrant is given by:

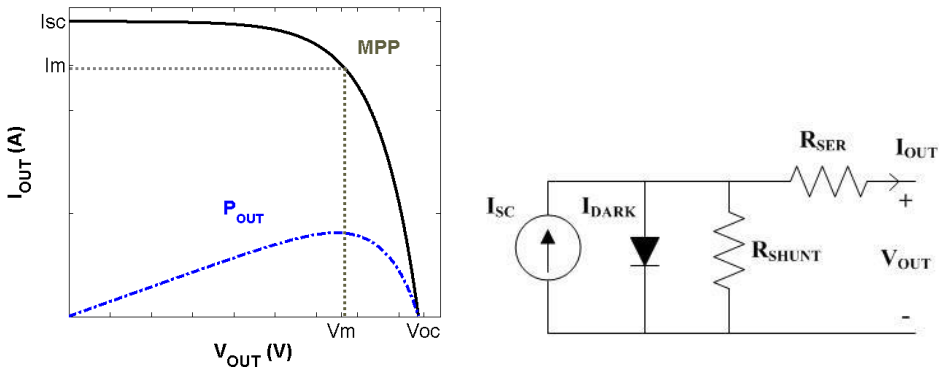
$$I = I_{Light} - I_{\ Dark} \tag{1.10}$$

$$= I_{Light} - I_0(e^{qV/nkT} - 1) \tag{1.11}$$

where I_0 is the reverse saturation current, n is the ideality factor of the diode and V is the applied voltage at the output of the solar cell. A sample I-V curve of a solar cell under illumination is illustrated in Fig. 1.4.a. This I-V curve can be modeled with the compact model shown in Fig. 1.4.b. The model employs a current source to indicate the light generation in the device. A diode in reverse polarity to the current source stands for the I_{dark}. In addition, this model indicates two parasitic resistances within the device. The first of those is the series resistance (R_{ser}) that is due to the resistance of the material between front contacts, the sheet resistance of contacts or recombination in the bulk of the absorber. The second resistance, shunt resistance (R_{sh}), indicates the low resistance paths that might have formed between front and back contacts during the deposition. Both resistances are undesired for a high efficiency solar cell since they reduce amount of power delivered to the load. If these parasitic effects are included, Equation (1.11) would become [10]:

$$I = I_{Light} - I_0\left(e^{\frac{q(V+IR_{Ser})}{nkT}} - 1\right) - \frac{V+IR_{Ser}}{R_{Sh}} \tag{1.12}$$

Although this compact model and the related superposition principle holds for thick c-Si solar cells, it generally is not a good fit for thin film solar cells since recombination modeled in I_{dark} gets strongly coupled with generation mechanism and becomes voltage dependent [11].



(a) (b)

Fig. 1.4 Current-voltage and power-voltage characteristics (a) and the compact model (b) of a solar cell.

The performance of a solar cell is determined by four figure of merits shown in Fig. 1.4.a, namely, short circuit current (I_{SC}), open circuit voltage (V_{OC}), fill factor (FF) and efficiency (η). The first of these terms, I_{SC}, indicates the current of the diode at short circuit condition (V=0) under illumination. Since I_{dark} goes to 0 at V=0, I_{SC} is found to be equivalent to I_{Light} from the superposition method in Equation (1.11). If the carrier collection occurs mainly diffusively, I_{SC} would be given by:

$$I_{SC} = qG(L_e + L_p) \tag{1.13}$$

where Le and L_p are the diffusion lengths of electrons and holes.

The second figure of merit, V_{OC}, is the voltage applied on the solar cell for which the I_{Light} is equal to the I_{dark} and thus the net current is 0. If the net current (I) is equated to 0 in Equation (1.11), V_{OC} can be written as:

$$V_{OC} = \frac{nkT}{q} \ln\left(\frac{I_{SC}}{I_0}\right) + 1 \tag{1.14}$$

As it can be observed from Fig. 1.4.a, the power that can be extracted from a solar cell increases as V is increased. Once it reaches the maximum power point (MPP), the power declines due to lack of output current. This maximum point indicated by maximum point current and voltage (I_m,V_m) is the ideal biasing point of a solar cell and determines

the FF and η. FF indicates the importance of parasitic resistances and can be determined by the ratio :

$$FF = \frac{I_m V_m}{I_{SC} V_{OC}} \tag{1.15}$$

The final and most important figure of merit, η, indicates the efficiency of the solar cell while converting the incoming solar power (P_S) to electrical power (P_E).

$$\eta = \frac{P_E}{P_S} = \frac{I_m V_m}{P_S} = \frac{I_{SC} V_{OC} FF}{P_S} \tag{1.16}$$

In solar cell design, the main goal is to improve the efficiency of the device. To achieve this goal, one can improve the absorption via reducing the reflection on the front surface, introducing direct bandgap materials or higher carrier lifetimes to increase the carrier collection at short circuit condition and therefore the I_{SC}. If a higher V_{OC} is desired, one can work with larger bandgap materials that would create a larger built-in voltage. Yet, since the number of photons that can excite an electron in the semiconductor reduces as the bandgap increases, there is an optimum bandgap (~1.35eV for a single junction [12]). Reducing the R_{ser}, (by reducing the recombination in the bulk) or increasing R_{sh} (by introducing buffer layers that stop diffusion of metals during contact annealing) improves the FF and therefore the η.

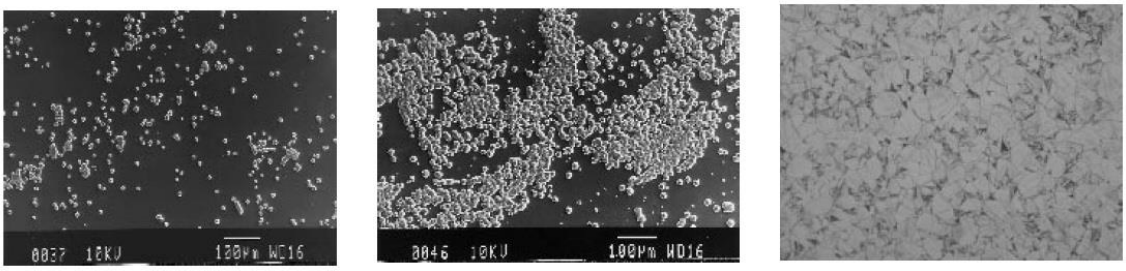
2. EFFECTS OF PROCESS CONDITIONS ON THE EFFICIENCY OF CHALCOGENIDE SOLAR CELLS

2.1. Process Technologies for Thin Film Polycrystalline Solar Cells

2.1.1. Polysilicon Solar Cells

Due to its usage in integrated circuits, various fabrication processes have been studied for polycrystalline Si material. For fabrication of solar cells two different approaches can be taken in general. The first approach would be the deposition of the material in one step. As shown in Fig. 2.1, the direct deposition approach starts on a clean substrate. Later on, initial particles stick to the surface and start the nucleation process. Later on, the incoming particles stick to regions close to these nucleation centers. By the time the surface is filled, each nucleation center will have a crystal formed around them which are called as “grains”. For this method, the control of the initial nucleation phase is critical since the size of the initial nuclei determines the size of the crystals inside the material. If the initial nuclei radius is too small, then the grains grow to be small too. On the other hand, if the initial nuclei are few and large in size, it will be harder to obtain a continuous film [13].

To avoid the problem of controlling the initial nucleation phase, a second approach can be taken in which the material is deposited on a high quality thin film called as the “seed”. The seed layer can be made by laser annealing of an amorphous Si layer (Excimer laser annealing (ELA) [14], sequential lateral solidification (SLS) [15]) or by using metals to induce nucleation sites (metal induced lateral crystallization (MILC) [16]) which would lead to larger grain sizes (GrSs). These processes are widely used for thin film transistor (TFT) fabrication, yet they get less feasible with an increase in film thickness. Thus, for solar cell fabrication these processes are generally used to form the seed layer and the rest of deposition is done with another epitaxial method.



(a) (b) (c)

Fig. 2.1 Nucleation (a) and growth (b) process of polycrystalline Si fabricated with atmospheric pressure CVD. Grains would be seen as in (c) under a microscope [17]. Copyright © by John Wiley & Sons [1]

There is a wide range of epitaxial methods that can be used to deposit the bulk of the solar cell. From these methods, chemical vapor deposition (CVD) works well with the seeding approach. The deposition process for this method involves the chemical reactions between the different gases (precursors) and the surface at high temperatures (around 800 to 1200 C°). Generally silane (SiH_4) precursor is used for polycrystalline Si deposition. A uniform film can be achieved using this method and when it is used with direct deposition approach, the microstructure in Fig. 2.1.c can be obtained.

2.1.2. Polycrystalline CIGS Solar Cells

The highest efficiencies for CIGS solar cells are obtained with the co-evaporation process technology. In this technology, all elements in the compound are evaporated simultaneously. Three variations of this approach are illustrated in Fig. 2.2. The main difference between these processes is the change in the Cu flux and substrate temperature during the deposition. Bilayer and 3-stage processes make use of the fact that Cu rich process step provides larger GrSs. In [18], Cu_xSe formation during growth is claimed to enlarge the grains and make the film more uniform. On the other hand in the bilayer process, the film is made Cu-rich at the first step and Cu-poor at the second. By doing this, excess Cu_xSe layer can be turned into CIGS and a relatively uniform Cu

[1] From Poortmans & Arkhipov, Thin Film Solar Cells Fabrication, Characterization and Applications, 1st Edition. Copyright © 2006 by John Wiley & Sons, Inc. Reprinted by permission of John Wiley & Sons, Inc.

composition can be achieved throughout the device. In 3-stage process an initial Cu-poor layer is incorporated along with additional Ga grading which introduces a second bandgap grading in the device due to the change in the mole fraction of Ga in the film.

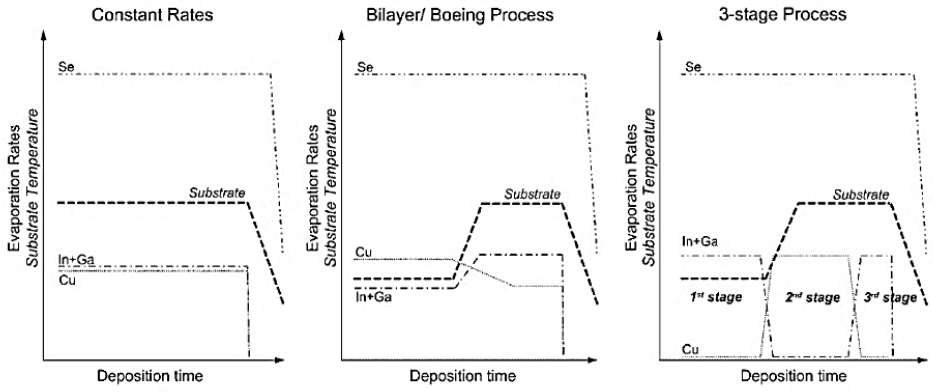
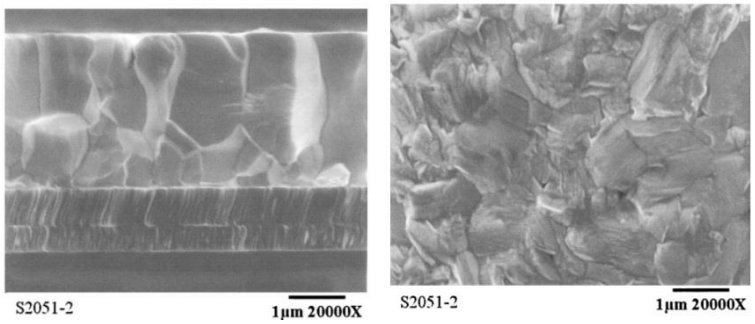


Fig. 2.2 Three variations of co-evaporation process used for CIGS solar cells [19]. Copyright © by John Wiley & Sons [2]



(a) (b)

Fig. 2.3 Cross-section (a) and top view (b) of the CIGS sample fabricated with 3-stage process [20]. Copyright © by John Wiley & Sons [3]

[2] From Romeo et al., Development of Thin-film Cu(In,Ga)Se2 and CdTe Solar Cells, Progress in Photovoltaics, Vol. 12, Iss. 2-3. Copyright © 2004 by John Wiley & Sons, Inc. Reprinted by permission of John Wiley & Sons, Inc.

[3] From Ramanathan et al., Properties of 19.2% Efficiency ZnO/CdS/CuInGaSe2 Thin-film Solar Cells, Progress in Photovoltaics Vol. 11, Iss. 4. Copyright © 2003 by John Wiley & Sons, Inc. Reprinted by permission of John Wiley & Sons, Inc.

In Fig. 2.3, the microstructure of the CIGS films fabricated with 3-stage process indicate the high quality of the material. The sizes of the individual crystals are significantly larger (~um) compared to other process technologies.

2.1.3. Polycrystalline CdTe Solar Cells

There are two variations of the same method that provide the highest efficiencies for CdTe solar cells [21]. The method is based on the evaporation of the substrate material (~600C), which can be CdTe compound or a stoichiometric mixture of Cd and Te onto a substrate that is spaced very close (mm to cm) to the source. If the chuck of the substrate is kept at a slightly lower temperature (~450C), the process is called close space sublimation (CSS). If the material transport is sustained by an inert gas, it is called as vapor transport deposition (VTD). An illustration of the deposition chamber for CSS is provided in Fig. 2.4 [21].

Another important aspect of the CdTe deposition is the post-treatment of samples with $CdCl_2$. The samples are annealed at temperatures from 300 to 600 C° in Cl-O ambient and an increase in the GrS is observed as in Fig. 2.5 [22]. For samples fabricated at lower temperatures, this increase would be more dramatic.

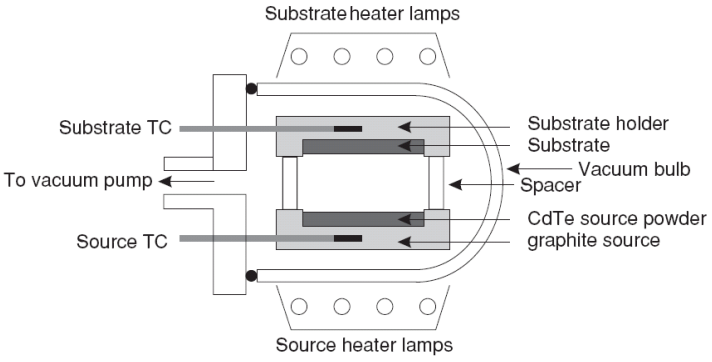


Fig. 2.4 Deposition setup for close space sublimation (CSS) process [21]. Copyright © by John Wiley & Sons [1]

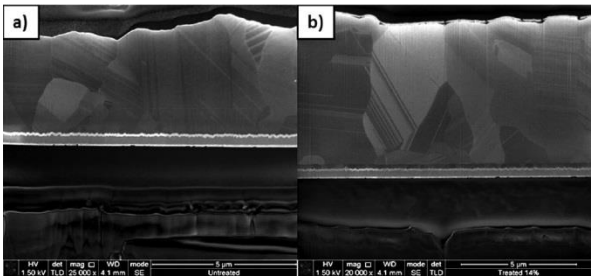


Fig. 2.5 The cross-section of CdTe samples fabricated with CSS process. Before and after $CdCl_2$ treatment [22]. Copyright © by John Wiley & Sons [4]

2.2. Grain Boundaries

As their name indicates, polycrystalline materials have multiple crystalline sections called as "grains". Each of these grains has a different crystallographic orientation and the regions (generally planes) where these sections meet are called as grain boundaries (GBs) as shown in Fig. 2.6.

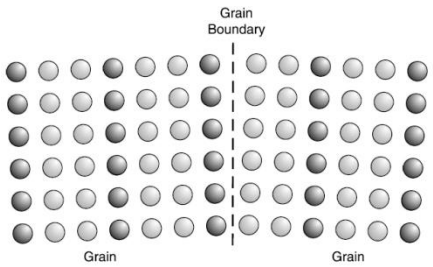


Fig. 2.6 Grain boundaries as planar defects [23]. Copyright © by John Wiley & Sons [5]

There are several ways that a GB can form. The simplest possibility is to have a grain that is rotated around an axis on a plane parallel to the GB plane. This type of GB is called as the tilt GB. On the other hand, if the rotation axis is perpendicular to the boundary plane, the twist GBs are formed.

[4] From Major et al., Focussed ion beam and field emission gun–scanning electron microscopy for the investigation of voiding and interface phenomena in thin-film solar cells, in Progress in Photovoltaics, vol. 20, Iss. 7. Copyright © 2012 by John Wiley & Sons, Inc. Reprinted by permission of John Wiley & Sons, Inc.

[5] From Tilley, Extended Defects, Defects in Solids. Copyright © 2008 by John Wiley & Sons, Inc. Reprinted by permission of John Wiley & Sons, Inc.

The misorientation between the grains is generally indicated with the rotation angle (θ). Depending on the value of θ, the GBs are categorized to be low or high angle. In the case of a tilt GB, if the GB is low angle, it can be described as an array of edge dislocations which are the discontinuities in the crystal structure. The distance between the edge dislocations (D) is given by:

$$D = \frac{b}{2\sin(\theta/2)} \approx \frac{b}{\theta} \tag{2.1}$$

where b is the Burgers vector, which indicates the direction and magnitude of the misorientation. As θ grows larger, D reduces such that the dislocations overlap and become indistinguishable for high angle GBs. The transition from low to high angles generally occur around θ = ~15° [24].

2.2.1. Grain Size Measurement Techniques and Distribution

A polycrystalline material's quality is generally measured by its average GrS. Therefore, there are several ways to measure this figure of merit. The simplest method is lineal intercept technique [25], which includes drawing a line on the micrograph of the film and counting the number of grains that line intercepts (N_L). The mean lineal intercept would be the average distance between GBs and would be expressed as:

$$\bar{l} = \frac{L}{N_L M} \tag{2.2}$$

where L is the length of the drawn line and M is the magnification magnitude. This procedure should be repeated for multiple lines to obtain a statistically sound value.

The second method is devised by American Society of Testing and Material (ASTM) which includes counting the number of grains in 1 inch^2 samples which are magnified at 100x. The number of grains (N) is converted to the standardized GrS number (n) using:

$$N = 2^{(n-1)} \tag{2.3}$$

Once n is found, the user can refer to the sample charts prepared by ASTM and determine the average GrS of the sample.

Besides average GrS, the distribution of the measured GrSs is an important data for polycrystalline materials. Based on this data, one can comment on the growth process and do performance variation analysis. Experimentally observed GrS distributions do

generally have a tail which is due to the change in GrS and number during the film growth as shown in Fig. 2.7. Starting from the initial distribution at t=0 (f_1) the distribution grows to be f_2 over time and two simultaneous mechanisms in grain growth is illustrated in this figure. First, the grains in range R_1 can grow due to a diffusion-like process given that there is a concentration gradient at the GB. On the other hand, the grains in range R_2 can either increase or decrease due to a field dependent mechanism caused by a driving force such as the change in GB curvature [26].

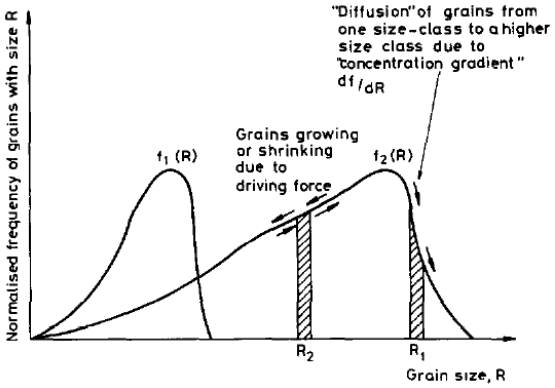


Fig. 2.7 The change in the GB size distribution tail over time [26]. Copyright © by Elsevier [6]

Historically, the GB size distributions are fitted with lognormal distribution, yet it is not found to be a good fit universally. In [26], it is found that the two mechanisms mentioned above causes a distribution peak sharper than lognormal which is more in line with the experimental data.

Although the theoretical works are mainly done on single-element metals, the GrS distributions for alloys and compounds follow a similar trend and data are readily available for CdTe and CIGS materials [27] [28]. Fig. 2.8.a indicates an increase in the average GrS with CSS CdTe film thickness. The distributions of the GrSs observed from the top of the sample at two different film thicknesses are provided in Fig. 2.8.b. These distributions are found to be Rayleigh distributions [27].

[6] Reprinted from Acta Metallurgica, Vol. 3, Iss. 3, Atkinson et al., Theories of Normal Grain Growth in Pure Single Phase Systems, Pages 469-491, Copyright (1988), with permission from Elsevier.

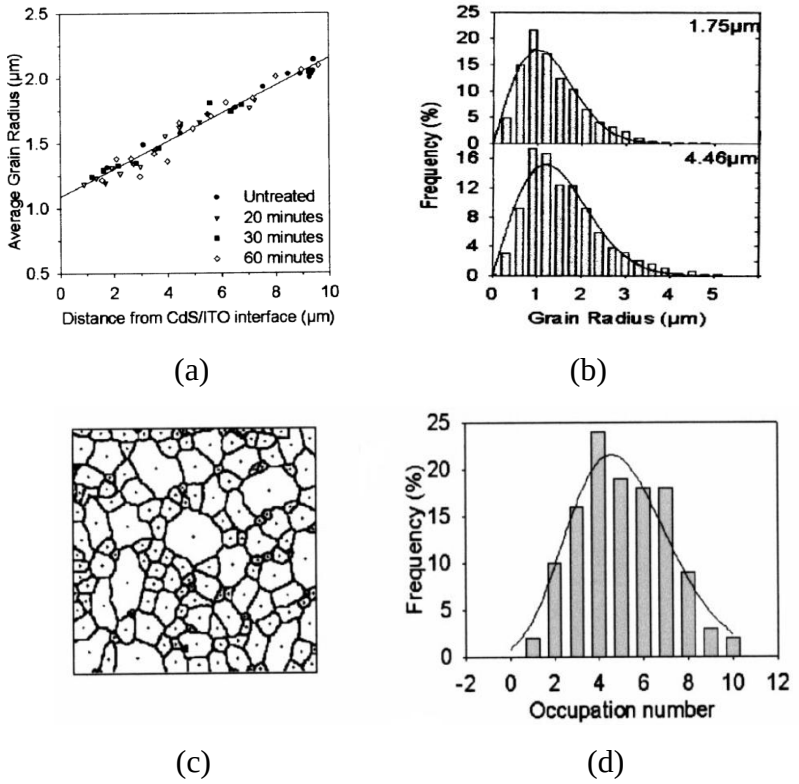


Fig. 2.8 The average grain size of *CSS* CdTe films with respect to measurement depth (a) and the grain size distributions of the films at two different depths (b). An illustrative top-view image of CdTe film (c) and the distribution for the number of grain centroids in a given area (d) [27]. Copyright © by Elsevier [7]

Instead of measuring the GrS, one can look into the number of grains in a given area. In Fig. 2.8.d, the distribution for the number of grain centroids in a given area is shown for the same CdTe sample. This distribution is fitted with a Poisson distribution indicating that the occurrence of grains in an area is a random-like process. The GrS distribution for CIGS reported in [28] differs from the CdTe sample discussed previously and follows a lognormal distribution. In addition, the deposition temperature is found to affect the distribution such that the mean GrS shifts to larger values at higher temperatures as the variation in GrS increases.

[7] Reprinted from Thin Solid Films, Vol. 361-362, Cousins et al., Grain structure of CdTe in CSS-deposited CdTe/CdS solar cells, Pages 253-2571, Copyright (2000), with permission from Elsevier.

2.2.2. Effects of Grain Boundaries on Device Performance

Since GBs are considered to be arrays of dislocations, they tend to trap free carriers. Based on the type of defects, these traps can be charged which changes the potential near the GB position. If the trap is acceptor-like, it would be neutral when unoccupied and it would be negatively charged when occupied by an electron. On the other hand, if the trap is donor-like, the unoccupied trap would be positively charged, while the occupied trap would be neutral. These traps are generally represented with an energy level in the bandgap and act as the recombination centers. In a real material, it is possible to have multiple traps with different energy levels. In that case, one can define a neutral energy level which indicates the net charge along that GB [29]. For instance for the band diagram in Fig. 2.9, the positively charged donor-like traps are compensated by negatively charged acceptor-like traps which resulted in a negative charge along the GB. To maintain the charge neutrality, the energy band at GB position bend upwards, leading to an energy barrier that limits the carrier transport in this n-type material. This barrier affects the subthreshold slope in TFTs, while its effects are rather complex in solar cells and will be discussed in the following sections.

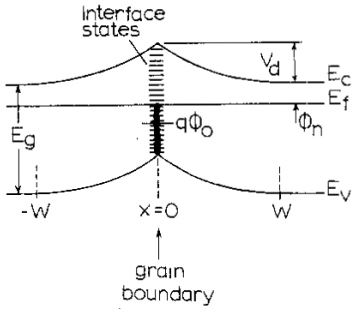


Fig. 2.9 The band diagram of a negatively charged GB in an n-type semiconductor [29]. Copyright © by IEEE [8]

Although the atomic forces exist over the GBs, the atoms along them are loosely connected to each other. These unsatisfied bonds create a surface energy along the GB. For high angle GBs, this energy is higher. Due to this surface energy, GBs are

[8] © 1977 IEEE. Reprinted with permission from Card et.al, Electronic Processes at Grain Boundaries in Polycrystalline Semiconductors Under Optical Illumination, IEEE Transactions on Electron Devices, 1977.

chemically more active than the bulk of the grains [30] which leads to the gettering of impurities along the GBs [31]. The dislocations on the GBs generally attract impurities like metals which might be useful in some cases. The passivating properties of Na along the GBs would be a good example. In [32] it is claimed that for polycrystalline CIGS, following the procedure in [32] , Na acts as a catalyzer during the adsorption process of O_2 which takes the place of the Se vacancies and passivates these defects. On the other hand, the Cu diffusion along the GBs from the back contact to the front of the device in a CdTe solar cell is found to be degrading the reliability of the product over time [33].

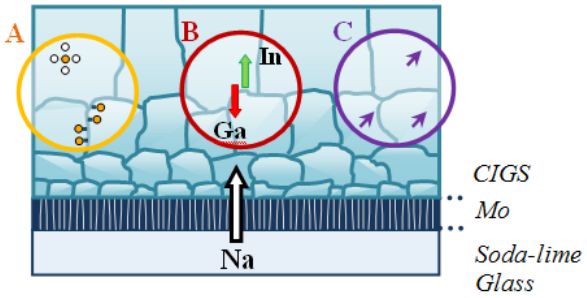


Fig. 2.10 Experimentally observed changes in CIGS due to Na diffused from the substrate: (A) Increased carrier density, (B) Ga segregation and (C) Change in crystal orientation [34]. Copyright © by IEEE [9]

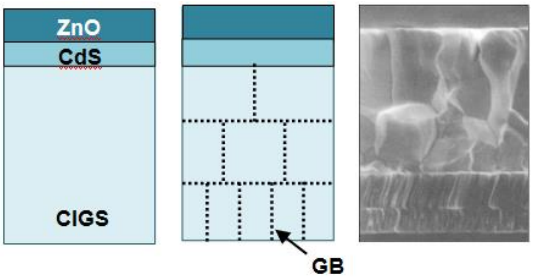
2.3. Effects of Na on the Efficiency of CIGS Solar Cells

As it is discussed in Section 1.1, CIGS and CdTe are promising materials for high performance thin film photovoltaics. Therefore in the following sections, CIGS and CdTe solar cells are going to be taken under investigation. Particularly for this section, the relationship between the CIGS cell performance with its Na content is going to be studied. It has been experimentally observed that Na diffusing from the soda-lime glass substrate causes an increase in the CIGS cell efficiency [35] . Yet, there is not a consensus on a mechanism that explains how Na affects the cell efficiency.

In literature, Na is observed to (a) increase the carrier density [36] [37], (b) cause segregation of Ga towards the Mo back contact [38] [39], (c) increase the number of

[9] © 2013 IEEE. Reprinted with permission from Mungan et.al, Modeling the Effects of Na Incorporation on CIGS Solar Cells, IEEE Journal of Photovoltaics, 2013.

<112> oriented grains [40] [41] (see Fig. 2.10). Given that these observations can occur simultaneously in a real device, it would be hard to distinguish the effects of one from the others. Therefore, the numerical simulation framework in Section 2.3.1 is proposed to investigate each observation and their potential effects on the efficiency of the CIGS cell.



(a) (b) (c)

Fig. 2.11 Single-crystalline (a) and polycrystalline (b) structures used in the simulations. (c) SEM image of the CIGS solar cell in Fig. 2.3.a [34]. Copyright © by IEEE [9]

2.3.1. Simulation Framework

The simulation framework required to study the effects of Na incorporation is constructed in a commercial 2D/3D device simulator called Sentaurus [42]. Within this framework, TCAD models are developed for a single-crystalline and a polycrystalline CIGS solar cell as in Fig. 2.11. Both models are composed of CIGS, CdS and ZnO layers as the absorber, buffer and window layers respectively. Both devices are set to be 1 μm-wide, whereas the thickness of each aforementioned layer is 3 μm, 50 nm and 200 nm respectively. The material parameters are adopted from [43]. For instance, the bandgap of CIGS is chosen to be 1.15eV and the affinity difference between CIGS and CdTe is assumed to be 0.3 eV. CIGS absorber is set to be p-type with a doping level of $2x10^{16}$ cm^{-3} and its bulk trap density is fixed to be 10^{14} cm^{-3}. The simulations are conducted under standard terrestrial solar spectrum (AM 1.5), whereas 5% and 80% reflectance are assumed at the front and back contacts of the device. The polycrystalline model is formed by placing GBs in the single-crystalline model. Idealized Manhattan geometry is employed to model the grains in the polycrystalline model in Fig. 2.11.b and the GrSs are enlarged towards the CdS layer to make the model similar to the SEM image of the real-life device in Fig. 2.11c [20].

Table 2.1 Parameters used to model GB trapped charge density (N_T) [a] and surface recombination velocity (s_R) [b] with different trap models [34]. Copyright © by IEEE [9]

Trap energy level (E_T), trap density at shallow and midgap energy levels (N_{TS} and N_{TM}), capture cross section for electrons and holes (σ_e, σ_h), conduction and valence band edge energies (E_C, E_V).

	E_T (eV)	N_{TS} (cm^{-2})	σ_e (cm^2)	σ_h (cm^2)
Neutral	Midgap	0	10^{-18}	10^{-18}
Acceptor	E_V+0.1	$4.5x10^{11}$	10^{-18}	10^{-18}
Donor	E_C-0.2	$4.5x10^{11}$	10^{-18}	10^{-18}

[a]

s_R (cm/s)	E_T (eV)	N_{TM} (cm^{-2})	σ_e (cm^2)	σ_h (cm^2)
10^3 -10^6	Midgap	10^4 -10^7	10^{-8}	10^{-8}

[b]

The GBs are modeled with defective interfaces. Following Ref. [43], four possible trap types are considered to model those defects: (a) neutral traps, (b) acceptor-like traps, (c) donor-like traps with no valence band discontinuity, and (d) neutral traps in a valence band shifted region. For charged traps, recombination velocity (s_R) and trapped charge density (N_T) of a GB is studied independently from each other. s_R is considered to be determined by midgap trap states with large capture cross-sections (σ), whereas N_T is controlled by the shallower trap states with small σs. The last trap type mentioned above is considered to be due to the Cu depletion around the GB region [44]. Therefore, it is modeled with a 20 nm-wide region around a neutral GB and only the valence band energy (E_V) of the material in this region is shifted down by 0.2 eV. As in Table 2.1, the trap density of shallow traps (N_{TS}) is chosen to be $4.5x10^{11}$ cm^{-2} since it is the worst case scenario for a device with the parameters selected in this section. N_{TS} values higher than

$4.5x10^{11}$ cm^{-2} create a highly inverted region around the GB that limits the number of holes and therefore the recombination at the GB [43].

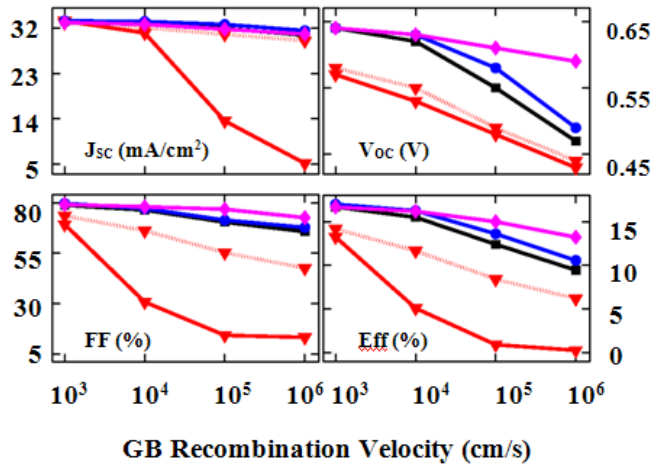
σ for electrons and holes (σ_e, σ_h) at shallow traps are assumed to be 10^{-18} cm^{-2} so that they create an energy barrier at the GB but do not contribute to the carrier recombination (s_R < 10 cm/s). On the contrary, 10^{-8} cm^{-2} is used for σ_e, and σ_h of midgap traps and their trap density (N_{TM}) is varied to keep s_R between 10^3-10^6 cm/s. This reduction in trap density towards the midgap is considered to be a valid assumption since it is observed to be common for various materials [45].

2.3.2. Analysis of Possible Improvement Mechanisms

In this subsection, the aforementioned changes in the CIGS absorber layer with Na incorporation are going to be replicated in the simulation environment and their effects on the CIGS cell performance is going to be investigated independently.

2.3.2.1. Observation 1: Increase in the Carrier Density

As the first observation to be studied, the increase in the carrier density is replicated in the simulation environment using the polycrystalline structure in Fig. 2.11.b. The performance of this structure is evaluated for various GB models and s_Rs to explore how much GB passivation can improve the cell performance. As the results in Fig. 2.12 indicate, the degradation in the cell performance is worst for GBs with donor-like traps with no discontinuity in the valence band (solid red line with triangles). This observation can be explained by the downward band bending at the GB position as shown in in Fig. 2.13.a. Due to the positive charges at the GB in a p-type CIGS, a downward band bending (E_{GB}<0) that attracts minority carriers (electrons) occurs in the device. As more minority carriers are attracted to the GB, electron and hole concentrations get closer to each other and SRH recombination at the GB is increased. This increase in the GB recombination is found to cause a significant reduction in performance metrics (short circuit current density (J_{SC}), V_{OC}, FF and efficiency) as shown in Fig. 2.12.



(◆) *Neutral trap in a valence band shifted region (ΔE_V=0.2eV)*

(●) *Acceptor-like traps*

(■) *Neutral traps*

(▼) *Donor-like traps with $N_{TS} = 4x10^{11}$ cm^{-2}*

(▼) *Donor-like traps with $N_{TS} = 4.5x10^{11}$ cm^{-2}*

Fig. 2.12 Performance of a polycrystalline CIGS solar cell with respect to GB recombination velocity (s_R) and GB model [34]. Copyright © by IEEE [9]

Since there is no band bending for neutral GBs, the GB recombination remains low and performance degradation with s_R is subtle (black squares in Fig. 2.12). As for the GBs with acceptor-like traps (blue circles in Fig. 2.12), the GB is charged negatively which leads to an upward band bending (E_{GB}>0). Therefore, the minority carriers are repelled from the GB and the recombination at the GBs is minimized. Finally, for the GBs modeled with neutral traps in a valence band shifted region (magenta diamonds in Fig. 2.12), the band diagram looks like Fig. 2.13.b. The holes are repelled from the region due to the barrier at the valence band, whereas electrons are not affected. Provided that the shift in the valence band (ΔE_V) is large enough, the region around the GB can be inverted to the extent that the recombination is limited by the number of holes at the GB. The ΔE_V due to Cu depletion in CIGS can go up to 0.4 eV [44]. The results for this type GBs in Fig. 2.12 are obtained for a ΔE_V of 0.2 eV which is found to be large enough to reduce the GB recombination significantly.

The results in Fig. 2.12 can be used to estimate a possible improvement in CIGS cell performance due to GB passivation. For instance, if the trap type at a GB with an s_R of 10^5 cm/s changes from donor-like traps to neutral traps, its efficiency can improve by ~11%. On the other hand, if the N_{TS} of donor-like traps at the GB is low, the improvement margin would be lower as well. For this purpose, results for a second N_{TS} are provided Fig. 2.12 (dotted red line with triangles). If the N_{TS} was $4x10^{11}$ cm^{-2}, the improvement margin would have reduced to 4%. From a different perspective, only the midgap trap states could be passivated which would reduce the s_R. If GB s_R is improved from 10^6 cm/s to 10^3 cm/s, the efficiency of a device whose GBs are modeled with donor-like traps and $N_{TS} = 4.5x10^{11}$ cm^{-2} (solid red line with triangles in Fig. 2.12) can improve by ~13%. Note that, in this analysis s_R and N_T are isolated from each other. Yet, an annealing process might reduce the trap densities related to both s_R and N_T which would further improve the efficiency.

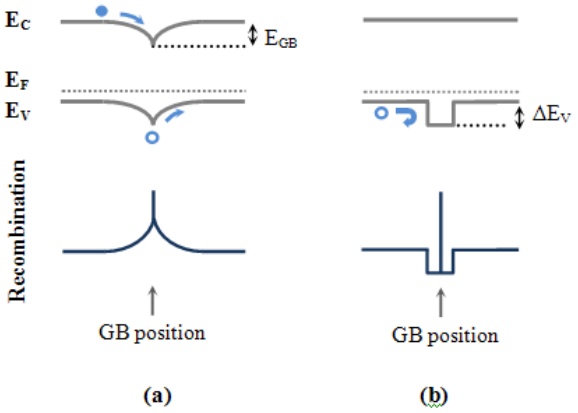


Fig. 2.13 Energy band diagrams and recombination rates at GBs modeled with: (a) Donor-like traps with no valence band discontinuity (b) Neutral traps within a valence band shifted region [34]. Copyright © by IEEE [9]

2.3.2.2. Observation 2: Change in Ga Distribution

As the second change in the CIGS material properties with Na incorporation, Ga segregation towards the Mo back contact is investigated in this subsection. In the presence of Na, the interdiffusion between Ga and In decreases and Ga diffuses towards

the back of the device. Since Ga concentration ([Ga]) determines the bandgap of CIGS, this leads to the double graded band diagram in Fig. 2.14 [38], [39]. To explore the impact of this change, the mole fraction of Ga within the single-crystalline and polycrystalline CIGS cell structures in Fig. 2.11.a and Fig. 2.11.b is graded. For ease of comparison, $N_{TS}=4x10^{11}$ cm^{-2} is used in this part of the study. The optical material parameters and dependence of the CIGS bandgap on [Ga] is taken from [46] and [47].The E_V of CIGS is kept fixed and the change in the bandgap is reflected only to electron affinity. [Ga]/[Ga+In] ratio is set to be 0.3 and 0.5 at the CdS/CIGS and CIGS/Mo interfaces respectively [20]. Afterwards, the ratio is varied at 500 nm away from the CdS/CIGS junction (minimum bandgap point in Fig. 2.14). The formula of the CIGS is assumed to be $CuIn_{(1-x)}Ga_xSe$ for this analysis.

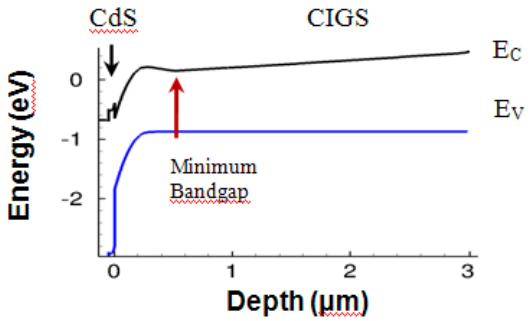
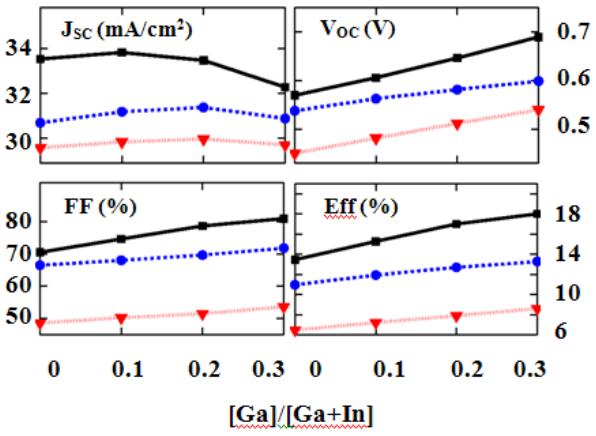


Fig. 2.14 Energy band diagram of the double graded single-crystalline CIGS solar cell [34]. Copyright © by IEEE [9]

As shown in Fig. 2.15, the performance of both single-crystalline and polycrystalline cells are found to be reduced as the Ga mole fraction (and therefore the bandgap) is reduced at the minimum bandgap point. The reduction in Ga leads to smaller effective bandgap for CIGS (thus reduces the V_{OC}) and increases the absorption (thus increases the J_{SC}) of the cell. The reduction in V_{OC} is found to be more pronounced which causes the reduction in the efficiency. In polycrystalline cells, the V_{OC} is already suppressed by the GB recombination. Hence, the reduction in efficiency with the reduction in [Ga]/[Ga+In] is subtle for the polycrystalline structures. If existence of Na reduces [Ga]/[Ga+In] from 0.3 to 0.2 as in [20], the efficiency is expected to be reduced by 1% for single-crystalline

cell. For a polycrystalline cell, this reduction would be 0.58% or 0.71%, if its GBs are modeled with neutral traps or donor-like traps respectively.



(▬) *Single-crystalline*
(●) *Polycrystalline with neutral traps*
(▼) *Polycrystalline with donor-like traps & $N_{TS}=4x10^{11}$ cm^{-2}*

Fig. 2.15 Performance of a double graded CIGS solar cell with respect to the Ga concentration at the minimum bandgap point [34]. Copyright © by IEEE [9]

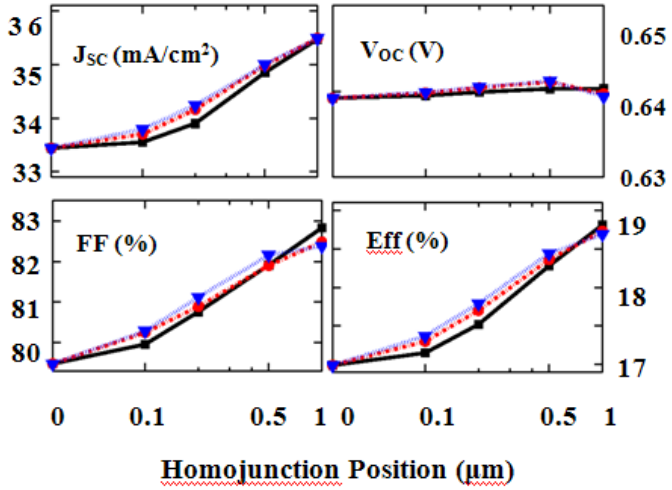
2.3.2.3. Observation 3: Change in Crystal Orientation

The increase in the number of <112> oriented grains with Na incorporation [40] [41] can affect the CIGS in two different ways: (a) the Cd diffusion from the CdS layer into CIGS is reduced for <112> oriented grains [48], (b) crystalline order and therefore the mobility of CIGS might increase. In the following subsections, the effects of these two methods on the performance of the CIGS solar cell are explored.

2.3.2.3.1 Reduced Cd Doping from CdS Layer

To observe the effect of Cd diffusion into the CIGS layer, an n-type CIGS layer is created between the n-type CdS and p-type CIGS layers while keeping the cell thickness fixed. Afterwards, the performance of the single-crystalline CIGS cell is monitored for different Cd doping depths and concentrations. The results in Fig. 2.16 demonstrate an increase in J_{SC} and FF due to the improved electric field introduced by the homojunction in CIGS layer. Given that the efficiency of the CIGS cell increases with Cd doping and

<112> oriented grains allow less Cd diffusion, the CIGS cell would suffer from an efficiency loss due to Na incorporation. Fortunately, this loss would be around 0.5% since a typical homojunction depth is around 80 nm [49].



(■) $N_{Cd}=10^{16}$ cm^{-3} (●) $N_{Cd}=5x10^{16}$ cm^{-3} (▼) $N_{Cd}=10^{17}$ cm^{-3}

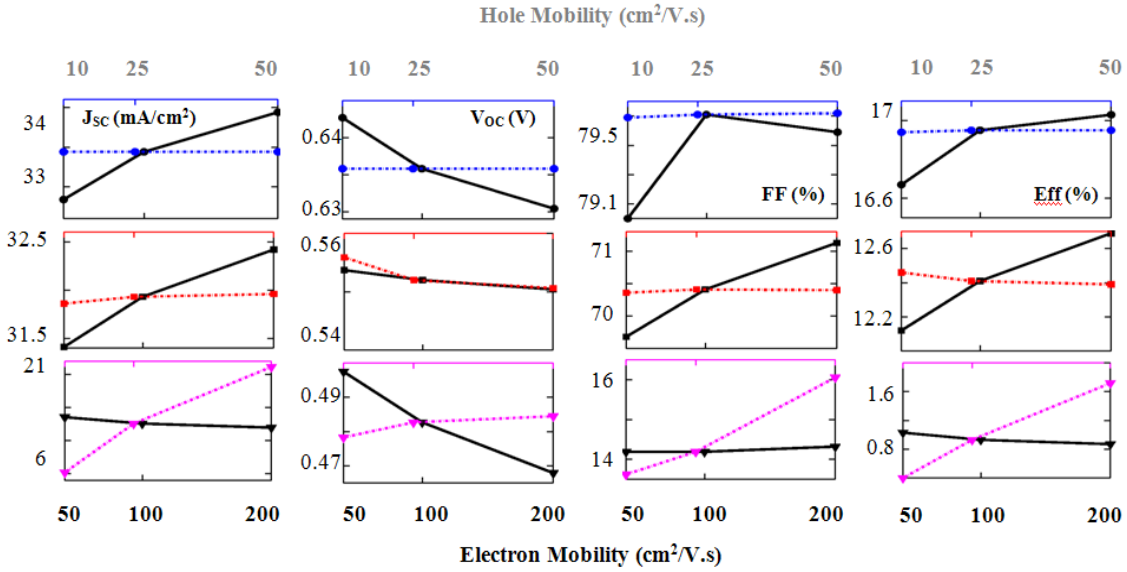
Fig. 2.16 Performance of CIGS solar cell with respect to homojunction position and doping density (N_{Cd}) of the Cd diffused n-type CIGS layer [34]. Copyright © by IEEE [9]

2.3.2.3.2 Increase in the mobility

As a possible consequence of the increase in the <112> oriented grains, the mobility of the CIGS layer might increase with Na incorporation. To investigate the extent of improvement that can be obtained with higher mobility values, mobility values for electrons (μ_e) and holes (μ_p) are varied for both single-crystalline and polycrystalline CIGS models. Two models are considered for the GBs of the polycrystalline structure: (a) neutral traps and (b) donor-like traps with $N_{TS}=4.5x10^{11}$ cm^{-2}. In both cases, the GB s_R is fixed to be 10^5 cm/s and the results of this analysis are reported in Fig. 2.17.

As the results in Fig. 2.17 show, effect of μ_p on the efficiency of a single-crystalline cell (first row in Fig. 2.17) is minimal since the absorber length is already shorter than the diffusion length for holes. On the other hand, when the mobility of the minority carriers (μ_e) is increased, an increase in carrier collection, J_{SC} and efficiency is observed. When neutral GBs are implemented in the device structure (second row in Fig. 2.17), the

efficiency trend remained similar. A slight reduction in V_{OC} is observed as μ_p is increased. This change in trend is found to be due to an increase in hole density and therefore an increase in recombination at the inverted GB in the depletion region. The reduction in V_{OC} is found to be more prominent for higher s_Rs.



(●) *Single-crystalline cell*
(■) *Polycrystalline cell with neutral traps*
(▼) *Polycrystalline cell with donor-like traps & N_{TS}=4.5x10^{11} cm^{-2}*

Fig. 2.17 Performance of CIGS solar cell with respect to electron mobility (solid black lines) and hole mobility (dashed colored lines) [34]. Copyright © by IEEE [9]

Once donor-like traps with the N_{TS} of 4.5x10^{11} cm^{-2} are placed into the GB (third row in Fig. 2.17) instead of neutral traps, the trend is found to be reversed. For this GB model, the holes are repelled from the GB, whereas the electrons are attracted to it (see Fig. 2.13.a). Hence, when μ_p is increased, hole concentration decreases at already inverted GB regions. This mechanism further reduces the GB recombination and improves J_{SC} along with the efficiency. On the other hand, increasing μ_e increases the electron concentration at the GB, causing higher GB recombination and lower efficiency.

Overall, the change in performance metrics with respect to the mobility values is found to be very small. The maximum amount of improvement in efficiency is found to

be limited to 1.44% for a realistic improvement in the mobility values. That is why change in crystal observation is considered to be not the dominant cause for the increase in CIGS cell efficiency with Na incorporation.

2.3.3. Discussion

The aim of this work was to investigate how Na might be improving the CIGS solar cell efficiency and test possible mechanisms using the proposed simulation framework. It should be noted that the parameters used in this work are collected from various works in the literature and therefore the results are not specific for a technology. On the other hand, the simulation framework proved itself to be a valuable tool to gain insight to this problem, test characterization experiments, debug and optimize any process.

The results obtained in the previous sections indicate the improvement in cell efficiency might be mainly due to the passivation of GBs. The efficiency can improve by ~11% when donor-like traps are neutralized by Na. On the other hand, the effects of Ga segregation and increase in the <112> oriented crystals on the cell efficiency are found to be limited to 1-2%. Of course these numbers are dependent on the process parameters and will be different for different CIGS processes. Regardless, the simulation framework can be utilized for any process.

2.4. Effects of Deposition Pressure on the Efficiency of Close Space Sublimation Deposited CdTe Solar Cells

For CSS-deposited CdTe films, changing the deposition chamber pressure is a powerful method to control the average GrS of the deposition process [50]. As Fig. 2.18 indicates, the average GrS increases from 1 μm to 6 μm as the N_2 gas pressure in the chamber is changed from 2 Torr to 200 Torr [51]. In this section, the results of this change in thin film morphology will be investigated. First, the effect of GrS distribution on the efficiency variation of a small scale (~mm^2) CdTe solar cell will be studied. Afterwards, a comprehensive study of the CSS-CdTe solar cells from process to module design will be conducted.

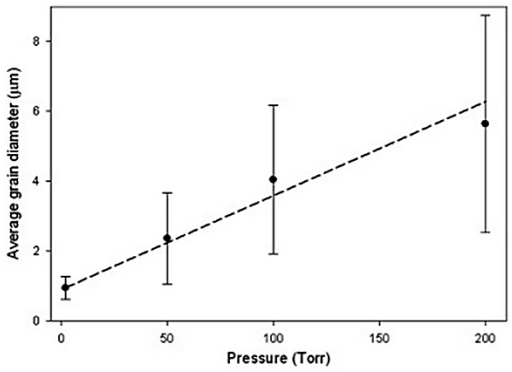


Fig. 2.18 Relation between the average GrS of a CSS-deposited CdTe thin film and the deposition pressure [51]. Copyright © by Elsevier [10]

2.4.1. Change in Grain Size Distribution and Performance Variation

Imperfections in the semiconductor fabrication process leads to variations in the final product's performance. For the CSS-deposited CdTe process with an average GrS of 1µm in [51], the efficiency values vary from 1% to 7%. In this section, the contribution of GrS distribution to this variation is going to be investigated.

As the first step to achieve this goal, a micron-scale, multi-level numerical model is proposed to study the effect of GBs and average GrS on the efficiency of CdTe solar cells. The results are calibrated with the experimental data in [51] and the efficiency trends are explained using this model. Afterwards, the length-scale is extended by compact modeling micron-scale cells with different GrSs and connecting these cells together in a SPICE platform. An experimental GrS distribution is implemented to a millimeter-scale cell using this approach and the implications of the GrS on the efficiency variation are studied.

2.4.1.1. Numerical Model for Micron-Scale Solar Cells

The numerical model for the small scale CSS CdTe solar cells is designed in a commercial 2D and 3D drift-diffusion solver, Sentaurus [42]. Two 2D models are

[10] Reprinted from Solar Energy Materials and Solar Cells, Vol. 94, Iss. 6, Major et al., Control of grain size in sublimation-grown CdTe, and the improvement in performance of devices with systematically increased grain size, Pages 1107-1112, Copyright (2010), with permission from Elsevier.

prepared with the geometries shown in Fig. 2.19.a and Fig. 2.19.b. The structure Fig. 2.19.a is used to model the effects of average GrS. On the other hand, the structure Fig. 2.19.b is prepared to study the impact of GrS distribution. Both of them employ CdTe, CdS and SnO_2 layers as their absorber, buffer and window layers. The thicknesses of these layers are set to be 6 µm, 500 nm and 150 nm respectively based on the dimensions in [50]. The baseline material parameters such as doping profiles, mobility and bandgap values are adopted from [52].

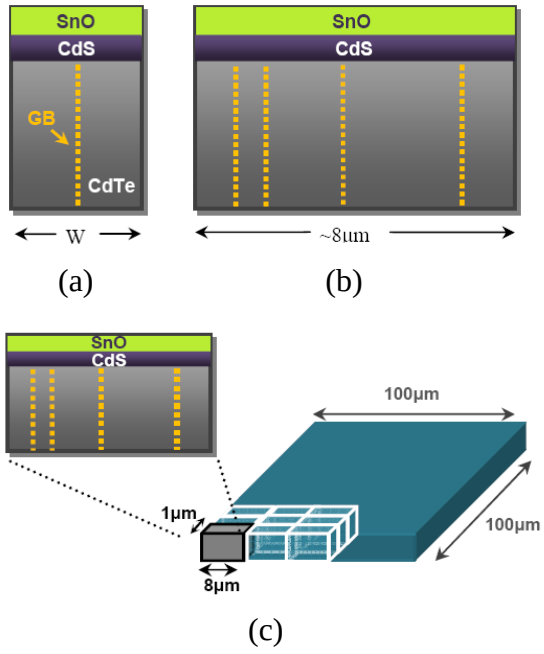


Fig. 2.19 Structures used to model the micron-scale solar cell [with uniform GrS (a) and random GrS (b)] and millimeter-scale cell (c) [53]. Copyright © by IEEE [11]

The GBs on the other hand are modeled as 2 nm-wide defective regions between single-crystalline grains and the defects are modeled as single level donor-like traps. The E_T used in the model is obtained from an admittance spectroscopy study done on a similar CSS CdTe solar cell [54] by the same research group conducted the work in [50] and [51]. The admittance spectroscopy study indicates three E_Ts for the GBs that are at

[11] © 2013 IEEE. Reprinted with permission from Mungan et.al, Bridging the Gap: Modeling the Variation due to Grain Size Distribution in CdTe Solar Cells, Proceedings of IEEE Photovoltaic Specialists Conference (PVSC), 2013.

0.17, 0.43 and 0.89 eV above E_V. In this work, the traps at 0.89eV are assumed to be related to the mid-gap trap states within the single-crystalline grain regions. On the other hand, the traps at 0.17eV are associated with the CdTe doping and the recombination due to this energy level is assumed to be negligible. Hence, the trap energy level related to the GBs is chosen to be 0.4 eV above E_V.

Capture cross section for electrons (σ_e) in the traps are modified to satisfy the $s_R=\sigma_e N_T v_T$ relationship for different N_T and s_R combinations used in Section 2.4.1.3. Here, the thermal velocity (v_T) is assumed to be 10^7 cm/s and the capture cross section for holes (σ_h) is assumed to be 2 orders smaller than that of majority carriers due to less attraction of holes to ionized donor trap states [52]. It should be noted that by taking this approach, s_R and N_T are coupled using a single E_T unlike the approach in [43]. In that approach, one E_T close to the band edge is used to model the effect of N_T and another E_T is used to model the effect of s_R of a GB (see Section 2.3.1).

2.4.1.2. Compact Model for Millimeter-scale Solar Cells

A millimeter scale solar cell is composed of smaller subcells that have grains with varying sizes. The sizes of its grains determine the performance of a subcell while the GrS distribution determines the ratio between the high and low performing subcells. To model the effects of GrS distribution, initially the GrSs and therefore the positions of GBs in a micron-scale subcells are determined based on an experimental GrS distribution. Afterwards, 100 subcells are simulated using the framework in Section 2.4.1.1. SPICE compact model parameters of these simulated subcells are extracted using the "four points" technique in [55] and these parameters are fitted into empirical distributions to model the performance variation in micron-scale. Finally, random subcells are picked based on these empirical distributions and their SPICE models are connected to make up a 100 µm x 100 µm cell using the approach in [56] (see Fig. 2.19.c). Afterwards, Monte Carlo simulations are conducted. The sheet resistance of the SnO_2 layer and the metal contacts in these simulations are taken to be 0.1 Ω/sq and 10 Ω/sq respectively.

2.4.1.3. Effect of Average Grain Size on Cell Efficiency

Before proceeding to the performance variation problem, one should know the effect of average GrS on the efficiency of the micron-scale solar cell. This knowledge can be obtained using the simulation framework proposed in Section 2.4.1.1 and can be used to explain the change in performance with respect to average GrS trend observed in [51]. There, the authors claim that increasing the ambient N_2 pressure in the deposition chamber from 2 Torr to 200 Torr leads to an increase in GrS from 1μm to 6μm due to the reduction in the initial nucleation density. This increase in GrS manifests itself in higher solar cell efficiencies, as shown with ▷ symbol in Fig. 2.20, but this improvement saturates for samples with average GrSs larger than 3 μm.

For this part of the study, the change in the performance of the CdTe solar cell is hypothesized to be due to the change in GrS only and the experimental results are aimed to be replicated in the simulation environment. For this purpose, the GrS is assumed to be uniform and GBs are assumed to be vertical and periodic as shown in Fig. 2.19.a, whereas the width of the device is set to be the average GrS. Also, the parameter set determined in Section 2.4.1.1 is assumed to be fixed and independent of the GrS. To determine the GB properties that will be used to reproduce the experimental results, the s_R and N_T parameters are varied and the results in Fig. 2.20 are compared with the data from [51]. The best match between the simulation and experimental data was obtained for an s_R value of 10^6 cm/s and N_T value of 10^{12} cm^{-2}(solid magenta triangles in Fig. 2.20).

Similar to the experimental observations, the results in Fig. 2.20 indicate an increase in cell efficiency as the GrS increases and the improvement in efficiency saturates for GrSs larger than 2.3μm. As the GrS gets larger, the depletion region of the GBs takes up a smaller portion of the device and recombination at the GBs significantly reduces. The cell performance is mainly limited by the bulk trap density within the grain and the Schottky barrier at the back of the device for devices with grains larger than 2.3μm. On the other hand, for devices with smaller GrSs, continuous GB depletion regions form around the junction that bring the energy bands down and lead to an energy barrier for electrons towards the back of the device. The electrons stopped by this barrier recombine at the CdTe/CdS junction at a higher rate.

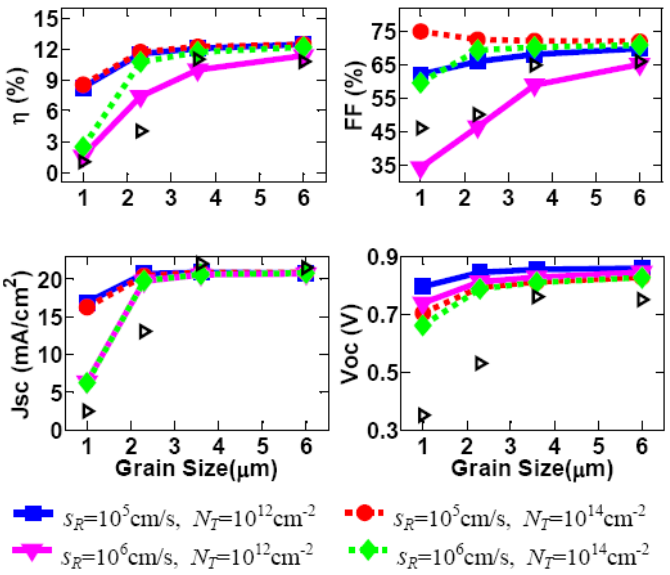


Fig. 2.20 Performance of simulated micron-scale cells with different GB recombination velocities (s_R) and GB trap densities (N_T). ["▷" indicates the data from Major et al. in [51]] [53]. Copyright © by IEEE [11]

Secondly, it is observed that the performance of the CdTe degrades as s_R increases. On the other hand, this observation is not valid for N_T. It is found that the results obtained for the N_T value of 10^{14} cm^{-2}, shown with green diamonds in Fig. 2.20, demonstrates higher fill factor (FF) and efficiency (η) values compared to the N_T value of 10^{12} cm^{-2}, shown with magenta triangles in Fig. 2.20. Similar to the observation done in [43] , the N_T = 5.10^{18} cm^{-3} value is found to be inverting the region around the GB such that number of holes limits the recombination at the GB. Therefore, increasing N_T leads to less number of holes and recombination at the GB.

2.4.1.4. Effect of Grain Size Distribution on Cell Efficiency Variation

To study the effect of GrS distribution on the efficiency of CSS CdTe cell, an experimental GrS distribution is chosen from [27] and fitted to the Rayleigh distribution shown in Fig. 2.20. The solar cell sample that provided this distribution was annealed for 20 minutes and the measurement was done 1.68 μm away from the CdS/ITO interface.

To accommodate multiple GBs in the simulation framework, the width of the structure is kept close to 8 μm (see Fig. 2.19.b). x=0 position is chosen as the starting point and a random number based on this Rayleigh distribution is generated to determine the distance of the first GB from the starting point. More random numbers are generated to determine the distance of the next GBs from the previous ones until the width of the device becomes greater than 8 μm. To satisfy the periodic boundary conditions, the sizes of the first and last grains are halved. Afterwards, following the framework explained in Section 2.4.1.1, 100 micron-scale subcells with random GrSs based on this distribution are simulated with the GB parameters of $s_R=10^6$ cm/s and $N_T=10^{12}$ cm^{-2}.

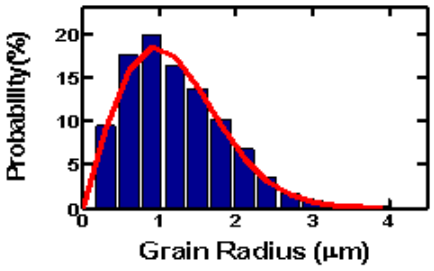


Fig. 2.21 The grain size distribution of the randomly generated structures used to simulate the variation in cell efficiency (blue bars) and the fitting distribution from [27] (red line) [53]. [Data is courtesy of Cousins et al.[7]] Copyright © by IEEE [11]

In line with the experimental results, the results for micron-scale solar cells in Fig. 2.22 indicate significant variation for all performance metrics and emphasize the importance of GrS distribution on the performance variation at the micron scale. On the other hand, when these micron-scale devices are connected in parallel to make up a millimeter-scale solar cell, the variation is found to be diminished (see Fig. 2.23). The subcells with smaller GrSs are found to be not affecting their neighboring subcells with larger GrSs considerably and therefore the averaging effect is observed at millimeter-scale. It should be noted that this outcome is opposite of what is observed for shunts with a heavily skewed distribution in a module [57]. Therefore, it can be concluded that the variation in cell efficiency observed in [51] cannot be due to the GrS distribution.

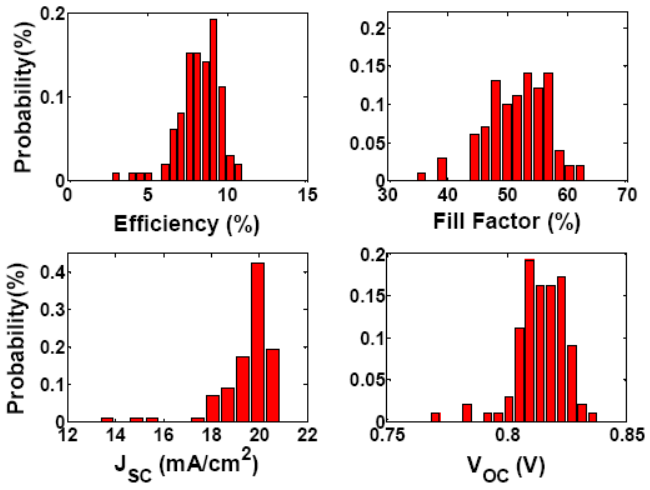


Fig. 2.22 The variation results from μ–scale TCAD simulations [53]. Copyright © by IEEE [11]

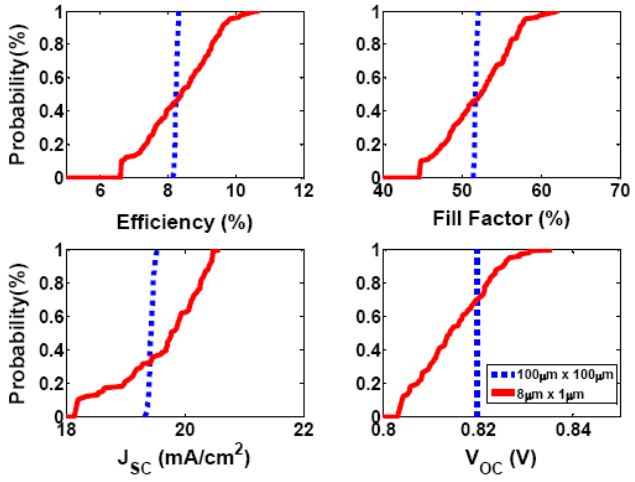


Fig. 2.23 The empirical cumulative distribution functions of the Monte Carlo simulation results for micron-scale and millimeter-scale CSS CdTe cells [53]. Copyright © by IEEE [11]

2.4.2. Modeling Close Space Sublimation Deposited CdTe Solar Cell Technology from Process to Module Design

In the previous section, the performance of a solar cell technology was tried to be understood by studying millimeter-scale solar cells and the effects of the process

parameters on their performance. Yet, a technology has many more design layers and the final product is generally a meter-scale module. The design of the final product involves: (a) design of a deposition process that is low cost and creates less number of defects, (b) obtaining knowledge on the semiconductor device physics of a lab-scale (~cm) device to use it for characterization and improve the performance and (c) design of a module that is reliable and high performance. There are efforts to improve the cell performance from these different aspects, yet improving an early design stage, i.e. process quality, does not necessarily indicate a proportional improvement in the performance of a module-scale solar cell. For instance in Fig. 2.20, increasing the GrS from 4 μm to 6 μm does not improve the performance of the lab-scale solar cell in [51]. In addition, the performance of a module-scale cell fabricated with this process is unknown. Most technologies have a significant gap between the lab-scale and module-scale cell efficiencies as shown in Fig. 1.1. Therefore, it is difficult to determine the potential of this process in the market. Hence, there is a need for a multi-scale, hierarchical model that can predict the performance of each design level and covers the design process from process end to the module end. To answer this need, in this section, the connection between these different design levels are going to be made with the end-to-end model illustrated in Fig. 2.24.

The proposed end-to-end model is composed of three levels: material, device and module. The material model in Fig. 2.24.a simulates the growth process of a polycrystalline material and determines the final microstructure deposited at specific process conditions. On the second layer of the hierarchy, the microstructure obtained from the material model is reconstructed in the absorber layer of a lab-scale solar cell and its performance is studied with the device model in Fig. 2.24.b. At the topmost module level in Fig. 2.24.c, the compact models of the lab-scale cells are connected together with series and shunt resistance elements to make up a meter-scale solar cell module. Using this hybrid end-to-end model, one can obtain deeper understanding of the effects of process changes on the performance of lab-scale and module-scale solar cells. This knowledge can be used to further improve cell performance and reliability at various levels of the design process.

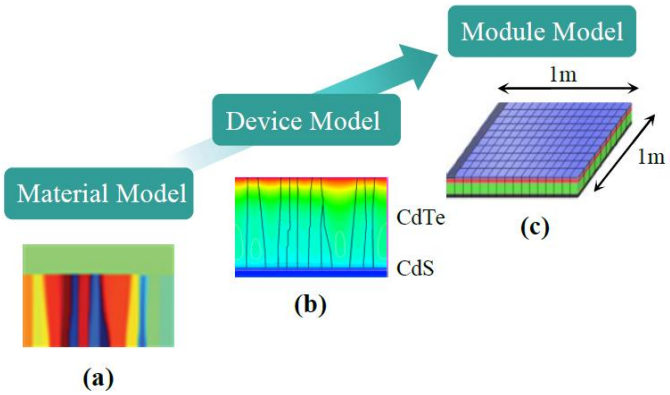


Fig. 2.24 Setup of hierarchical end-to-end model of CSS CdTe solar cell technology [58]. Copyright © by IEEE [12]

The experimental data in [51] are used to calibrate the proposed end-to-end model for the CSS CdTe solar cell technology. In the following sections, the material model will be used to model the change in thin film GrS with respect to N_2 pressure during deposition first. Then, the simulated microstructure will be transferred to the device model and the limiting factors on the lab-scale device performance are going to be investigated. Finally, the module level model will be used to estimate the performance of a meter-scale CSS CdTe solar cell module.

2.4.2.1. Material Model

The growth of CSS thin films is a complex process. The grains in the polycrystalline film go through nucleation, growth and coarsening stages during the deposition [59], whereas the average GrS of the deposited film is determined by the process conditions such as deposition temperature, pressure and duration. The material model used in this section is developed by Wang et. al. [60] and it models two significant features of polycrystalline film growth: (a) growth of grain nuclei as a function of time via a level set model (LSM), (b) change in the crystal orientation of grains during growth via a phase

[12] © 2014 IEEE. Reprinted with permission from Mungan et.al, From Process to Modules: End-to-End Modeling of CSS-Deposited CdTe Solar Cells, IEEE Journal of Photovoltaics (JPV), 2014.

field model (PFM). This model neglects process details such as deposition chamber's geometry or temperature distribution [61]. Yet, it should be noted that to the best of the authors' knowledge there is no theoretical work that takes the CSS deposition process in complete detail.

2.4.2.1.1 Modeling the Grain Growth Process

The LSM method used to model grain growth is essentially a well-known method [62] that was previously used to keep track of the change in the interface over time for processes like etching [63]. The technique is popular due to its ability to track changes in the interfaces with sharp edges and its ability to model impinging and detaching of those interfaces.

In LSM method, the interface between the gas and solid interface is determined by a scalar $\varphi(\vec{x},t)$ function that is a function of position and time. Negative values of $\varphi(\vec{x},t)$ would define the deposited solid regions, whereas positive values define the evaporated source material in gas state and $\varphi(\vec{x},t)=0$ indicates the solid-gas interface. The interface is tracked by:

$$\frac{d\varphi(\vec{x},t)}{dt}=\sum_{i=1}^{3}\frac{\partial\varphi}{\partial x_i}\frac{\partial x_i}{\partial t}+\frac{\partial\varphi}{\partial t}=0 \tag{2.4}$$

and the gradient of $\varphi(\vec{x},t)$ is set as 1 ($|\nabla\varphi|=1$). Eq. (2.4) can be simplified to:

$$\frac{d\varphi}{\partial t}+\vec{v}.\nabla\varphi=0 \tag{2.5}$$

where

$$\vec{v}=v_n\frac{\nabla\varphi}{|\nabla\varphi|}=\Gamma\Omega\frac{\nabla\varphi}{|\nabla\varphi|} \tag{2.6}$$

$\vec{v}$ in Eq. (2.5) refers to the local velocity of the interface while v_n is its normal velocity. As it is indicated in Eq. (2.5), v_n depends on the deposition rate (Γ) and the molar volume (Ω) [62]. Γ is determined by the difference between the gas pressure of the evaporated source material (P_g) and the local pressure at the curved grain surface (P_γ) by [64]:

$$\Gamma = K_n(P_g - P_\gamma) \tag{2.7}$$

$$K_n = 1/\sqrt{2\pi MRT_e} \tag{2.8}$$

where K_n is the Knudsen constant that takes molar mass (M), gas constant (R) and the source temperature (T_e) into account. P_γ can be calculated using the Gibbs-Thomson relation [65]:

$$\mu_V(\kappa) - \mu_V(\infty) = \gamma\kappa\Omega = RTln(P_\gamma/P_\infty) \tag{2.9}$$

where $\mu_V(\kappa)$ is the chemical potential of a vapor with a curvature κ and $\mu_V(\infty)$ is the chemical potential of a flat surface. γ indicates the energy of the surface between gas and solid regions and P_∞ stands for the vapor pressure of a flat surface.

2.4.2.1.2 Modeling Crystal Orientation of Grains

To model the change in the crystal orientation of the grains during growth, a PFM model is employed that solves the Helmholtz free energy equation for the solid phase (F_S) [66] :

$$F_s = \int_V [g(\Psi)s|\nabla\theta| + h(\Psi)\frac{\varepsilon^2}{2}|\nabla\theta|^2]\, dV \tag{2.10}$$

where Ψ is the solid-gas phase field order parameter that defines the solid and gas phases, ($\Psi=1$ for solid and $\Psi=0$ for gas phase) [60] and $g(\Psi)=h(\Psi)=\Psi^2$. θ stands for the grain orientation [66] while s and ε are the first and second order coupling strengths between Ψ and $\nabla\theta$ respectively.

Assuming that the vapor deposit that transforms into solid attains the same grain orientation with the grain it is attached to, the Allen-Cahn equation [67] can be used to model the grain coarsening process as follows:

$$\frac{\partial\theta}{\partial t} = -p(\Psi)M_n^s\frac{\partial F_s}{\partial\theta} \tag{2.11}$$

where $p(\Psi) = \Psi^2$ and

$$M_n^s = -1/(q(\nabla\theta).\tau_\theta.\Psi^2) \tag{2.12}$$

Based on the definition in [66], q would be close to infinity and $\nabla\theta$ would be zero inside the grain. On the other hand, $q(\nabla\theta)$ would be 1 and $\nabla\theta$ would be non-zero at the GB. Here, τ_θ corresponds to the inverse mobility. Substituting Eq. (2.12) into Eq. (2.11), one can obtain the final version of the equation for the grain orientation kinetics:

$$q(\nabla\theta)\tau_\theta\Psi^2\frac{\partial\theta}{\partial t} = p(\Psi)\nabla.(h(\Psi)\varepsilon^2\nabla\theta + g(\Psi)s\frac{\nabla\theta}{|\nabla\theta|}) \tag{2.13}$$

2.4.2.1.3 Calibration of the Simulation Framework

In this subsection, the simulation framework defined in Sections 2.4.2.1.1 and 2.4.2.1.2 is used to simulate the microstructures of the CSS CdTe thin films deposited under 2, 50, 100 and 200 Torr pressure. Based on the initial coverage ratios provided in Table 2.2, a set of semi-spherical nucleation islands are placed on a 50 μm-wide sample. The diameters of these islands are assumed to have a Gaussian distribution, with a mean value as in Table 2.2 and a standard variation of 0.1 μm. After this initial setup, the material simulations are run and the cross-sections of the CSS CdTe films deposited under different pressures are obtained as in Fig. 2.25. Afterwards, the GrSs measured from the top-view of the films are plotted against the experimental data in Fig. 2.26 and good agreement is observed between the experimental data in [51] and the simulation results. The results in Fig. 2.25 and Fig. 2.26 indicate that as the deposition pressure increases, larger and fewer grains are obtained and the surface roughness of the CdTe film increases.

Table 2.2 Material Model Simulation Parameters. Copyright © by IEEE [12]

Pressure (Torr)	Initial GrS (μm)	Initial Coverage (%)	Final GrS(μm)
2	0.64	80	1.16
50	1.18	68	2
100	1.94	58	3.3
200	2.92	52	6.13

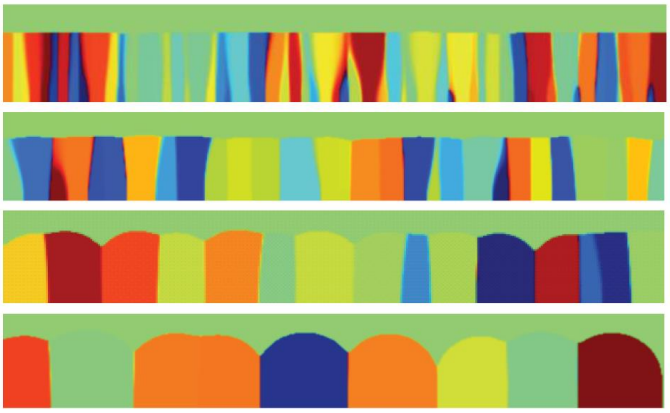


Fig. 2.25 50 μm x 6 μm CSS CdTe thin films deposited under different chamber pressures [Top to bottom: 2, 50, 100 and 200 Torr] [58]. Copyright © by IEEE [12]

This trend can be explained by the increase in the Gibbs free energy of formation with deposition pressure. The radiuses of the initial islands need to grow larger than a critical radius (r^*) so that they can form the nuclei and r^* increases with pressure (P) as follows:

$$r^* = -\frac{2\gamma}{\Delta g_v + P} \tag{2.14}$$

where ∇g_v is the chemical free energy of transformation from gas to solid phase for the bulk. As r^* increases fewer islands can become nuclei which results in larger and fewer grains. Finally, it should be noted that due to lack of experimental γ data for CdTe, γ and the initial GrS parameters are obtained empirically based on Eq. (2.14) to reconstruct the experimental data.

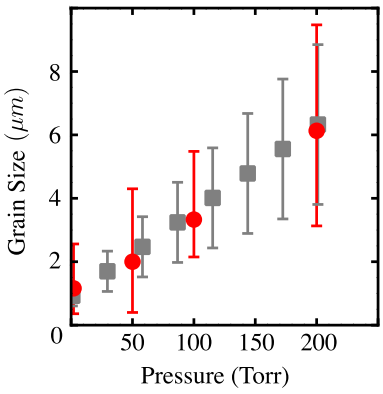


Fig. 2.26 CSS-CdTe grain size as a function of chamber pressure (simulation data: ● , experimental data from Major et al. in [51]: ■) [58]. Copyright © by IEEE [12]

2.4.2.2. Device Model

In this section, the performance of the lab-scale solar cells made from the CdTe thin films simulated in Section 2.4.2.1 (see Fig. 2.25) are going to be determined. The study will start with understanding the effects of average GrS on the lab-scale cell efficiency, specifically understanding the sharp reduction in the V_{OC} observed for cells with small GrSs in Fig. 2.20. Understanding the loss mechanisms in a lab-scale CdTe solar cell will be the last part of this study at the device level.

The performance of lab-scale polycrystalline CSS CdTe solar cells are studied via the 2D TCAD model proposed in Section 2.4.1.1. In this section, two different GB geometries are employed: (a) ideal and vertical GBs placed average GrS away from each other, (b) synthetic GBs whose positions are extracted from the microstructures in Fig. 2.25 via image processing techniques. The structures with ideal GBs are illustrated in Fig. 2.19.a where Fig. 2.27 illustrates the structures with synthetic GBs. In Fig. 2.27, the device is modeled to have a superstrate configuration in which CdTe layer is deposited on the glass substrate precoated with SnO_2 and CdS layers. Due to this configuration, the GBs are more closely spaced at CdS/CdTe junction compared to the CdTe/back contact interface.

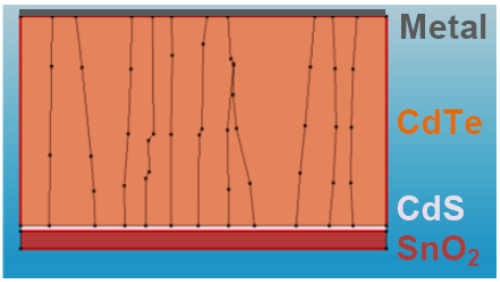


Fig. 2.27 Device structure with synthetic GBs for CSS CdTe solar cells deposited under 2 Torr pressure. [Device dimensions are 10 µm x 6 µm] [58]. Copyright © by IEEE [12]

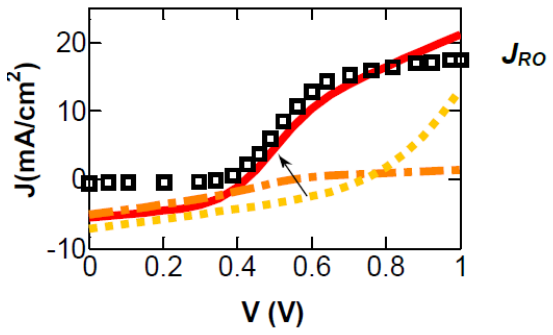
2.4.2.2.1 Effects of Grain Size on the Efficiency of Ideal Microstructures

In Section 2.4.1.3, the change in the lab-scale CSS CdTe solar cell's performance with deposition pressure was tried to be explained with the change in the average GrS of the process. This approach could explain the first increasing and then saturating performance of the cells with respect to the GrS. Yet, the steep reduction in the V_{OC} observed for samples with small GrSs indicated the existence of a secondary limiting process (see Fig. 2.20). To investigate this secondary process, additional data from [51] is studied for a sample deposited under 2 Torr pressure (see Fig. 2.28).

The experimental J-V curve shown with black squares in Fig. 2.28 saturates around 0.6V instead of increasing continuously which is a phenomenon called as "roll-over" in literature [52]. This phenomenon indicates the possibility of having a high energy barrier at the back contact (Φ_B) that can explain the sharp reduction in the V_{OC}. Since GBs are highly chemically active regions, it is possible for samples with small GrSs to have secondary phases forming at the back of the device that would create this high Φ_B [68].

The results obtained with the parameter set that provided the best fit in Section 2.4.1.3 for a structure with periodic GBs ($s_R=10^6$ cm/s, $N_T=10^{12}$ cm^{-2}, $\Phi_B=0.4$eV), do not indicate roll-over within the voltage range of interest (see the yellow dotted line in Fig. 2.28). On the other hand, the dash dotted orange line indicating a roll-over effect can be obtained for a Φ_B of 0.7eV. Yet, the increase in Φ_B should be accompanied with an increase in N_T to explain the high current density at the roll-over point (J_{RO}). A higher N_T increases the number of positively charged traps along GB and lowers the energy barrier

for electrons flowing from CdS to CdTe side and thus increases J_{RO} (see red solid line in Fig. 2.28). Given this explanation, one can replicate the J-V curves for the samples with average GrS smaller than 3 μm with the parameter Set A (Φ_B=0.4eV, N_T =10^{12} cm^{-2}) from Section 2.4.1.3, whereas the samples with average GrS larger than 3μm can be replicated with the parameter Set B (Φ_B=0.7eV, N_T =10^{13} cm^{-2}) as shown in Fig. 2.29.



(···) Φ_B=0.4eV, N_T =10^{12} cm^{-2} (–·) Φ_B=0.7eV, N_T =10^{12} cm^{-2}
(—) Φ_B=0.7eV, N_T =10^{13} cm^{-2} (□) Major et al. [51]

Fig. 2.28 Dependency of light J-V curve and the roll-over current (J_{RO}) of CSS CdTe solar cells on back contact barrier (Φ_B) and GB trap density (N_T). (Experimental data courtesy of Major et al. [51]) [s_R= 10^6 cm/s] [58]. Copyright © by IEEE [12]

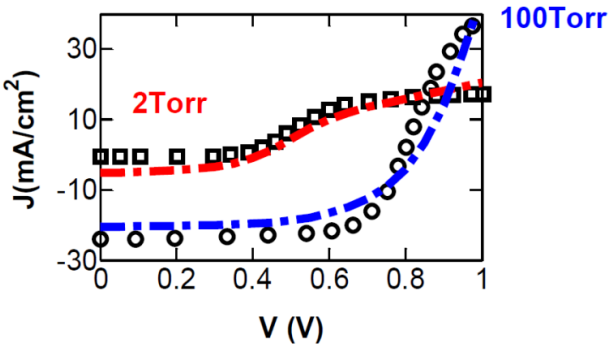
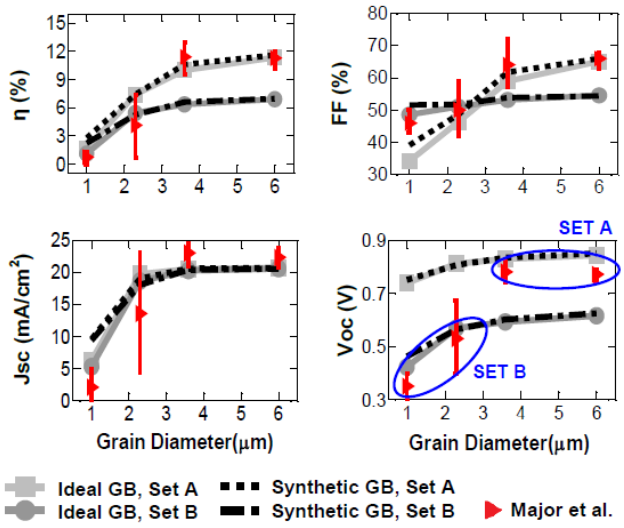


Fig. 2.29 Reconstruction of light J-V curves of CSS CdTe solar cells deposited under 2 Torr and 100 Torr pressures. (Simulation results: (dash-dotted lines), experimental data: (□,○) courtesy of Major et al. [51]) [58]. Copyright © by IEEE [12]

2.4.2.2.2 Effects of Grain Size on the Efficiency of Ideal Microstructures

The two parameter sets used in the previous subsection were determined for the ideal GB model that assume all the grains in the solar cell have the same GrS, which is equal to the average GrS of the process. Yet, the microstructures shown in Fig. 2.25 indicate a non-uniform distribution of GrSs and the effects of this distribution are investigated in this section. For this purpose, the synthetic GBs extracted from Fig. 2.25 are embedded in the simulation structures and the results in Fig. 2.30 are obtained.

As it can be observed from Fig. 2.30, the simulation results for the synthetic and ideal structures agree well for samples with GrSs larger than 1μm. For cells with GrSs smaller than or equal to 1 μm, the synthetic GB model is found to be producing better results (especially in J_{SC} and FF) from the ideal GB model due to occasional large grains occurring throughout the film.



Set A: Φ_B*=0.4eV,* s_R*=10^6 cm/s,* N_T*=10^12 cm^-2,*

Set B: Φ_B*=0.7eV,* s_R*=10^6 cm/s,* N_T*=10^13 cm^-2*

Fig. 2.30 Performance metrics of CSS CdTe Solar Cells modeled with ideal GBs (solid lines) and synthetic GBs (dashed lines) versus experimental data (Courtesy of Major et al. [51]). [58]. Copyright © by IEEE [12]

A second conclusion that can be drawn from Fig. 2.30 is that for devices with grains smaller than 3 μm, the experimental results agree well with simulation results obtained

for a high Φ_B (Set B). On the other hand, the results indicate a lower Φ_B (Set A) for devices with grains larger than 3 µm. Therefore, the change in performance metrics of a CSS CdTe solar cell with deposition pressure should be modeled with the change in average GrS along with the change in the back contact properties and GB passivation.

2.4.2.2.3 Loss Mechanisms for a CSS CdTe Solar Cell

For polycrystalline solar cells, the non-radiative recombination at GBs is a significant limiting factor on their cell efficiencies. Yet, there are other loss mechanisms occurring simultaneously that should be taken into account. The experimental data in [51] indicates that increasing GrS from 4 µm to 6 µm does not improve the cell performance. Hence, a secondary loss mechanisms should be playing an important role in this regime. Therefore, in this section a breakdown of the loss mechanisms in a polycrystalline CSS CdTe solar cell with respect to GrS is going to be made.

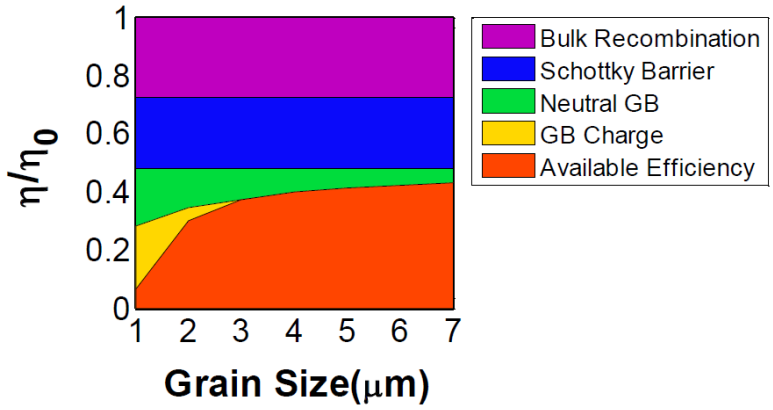


Fig. 2.31 Breakdown of loss mechanisms observed in polycrystalline CSS CdTe solar cells. (The results are normalized with respect to efficiency of an ideal cell (η_0)) [58]. Copyright © by IEEE [12]

To achieve this goal, the simulations are started with an ideal CdTe solar cell with ohmic contacts and efficiency of (η_0). The initial structure did not have any recombination, and loss mechanisms are implemented step-by-step. Midgap bulk traps defined in [52] are introduced first which is followed by the Schottky Barrier at the back contact (Φ_B=0.7eV). Afterwards, neutral GBs with few charges along them (s_R= 10^6

cm/s, $N_T = 10^7$ cm^{-2}) are implemented and finally donor-like GBs with parameters from Set B ($s_R = 10^6$ cm/s, $N_T = 10^{13}$ cm^{-2}) are included in the model. At each step, the impact of the most recently included loss mechanism is recorded and the efficiency values are normalized with respect to η_0 to attain to Fig. 2.31.

The results in Fig. 2.31 demonstrate that the recombination in the bulk of the CSS CdTe solar cells and the efficiency loss due to Schottky barrier causes the efficiency of the cell to be reduced by half. For cells with grains smaller than 3 μm, the neutral GBs reduce the efficiency and this reduction can be further enhanced by adding charges along the GBs. For cells with grains larger than 3 μm, the depletion region along the charged GB is found to be not affecting the cell efficiency. It should be underlined that the devices are modeled with parameter Set B in this section, therefore the loss in real devices due to Schottky Barrier (blue bar in Fig. 2.31) should be expected to be less for GrSs larger than 3 μm.

2.4.2.3. Module Model

For all solar cell technologies, moving from lab-scale production to module production means a reduction in efficiency values due to series and shunt resistances (R_{SER} and R_{SHUNT}) in the module [69]. Furthermore, the parasitic shunts cause variation on the module efficiency that can be described by a lognormal distribution for different PV technologies [70]. To study these phenomena in module level, the PV module is treated as a 2D network of lab-scale cells connected with contact sheet resistances [71]. The dimensions of the module are assumed to be same with the First Solar modules in [72] which are 0.56m x 1.16m and the contact resistances are chosen to be 10Ω/sq and 0.5Ω/sq for Sn0 and contact metal layer respectively. Each lab-scale cell with a 1 cm^2 area is placed in an array of 56 rows and 116 columns to make up the thin film module in Fig. 2.32. A random R_{SHUNT} value based on the lognormal distribution in [69] is assigned to these unit cells and Monte Carlo simulations are conducted in HSPICE circuit simulator to determine the performance of the module level CSS CdTe solar cell efficiency.

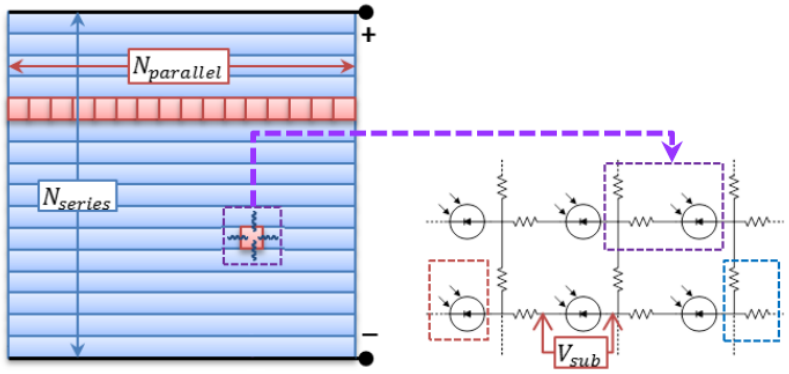
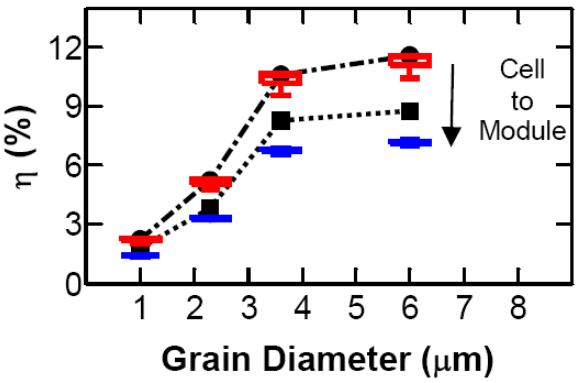


Fig. 2.32 Module model configuration and its equivalent circuit representation [58]. Copyright © by IEEE [12]

To investigate the performance change in CdTe solar cells when the device dimensions are changed from lab-scale to module-scale, device level simulation results are compared with module level simulation results. As the starting point, a lab-scale device with synthetic GBs are simulated with the parameter Set A for GrSs larger than 3 µm and with parameter Set B for GrSs smaller than 3 µm (dash-dotted line in Fig. 2.33). Afterwards, R_{SHUNT}s are added to the device simulations and the maximum variation in the lab-scale cell's performance is observed to be 1.2% (top boxplots in Fig. 2.33). At the third step, the lab-scale cells without R_{SHUNT}s are connected in a module configuration and the efficiency values are found to be reduced by 0.5 to 2.8 % due to the effect of R_{SER}. This amount of reduction is found to be agreeing well with the efficiency gaps reported in [6]. Finally, the R_{SHUNT} is included into the module-level simulations and the performance is found to be further reduced by 1-2% and the variation is found to be significantly reduced to 0.4% (~5% of the median V_{TH}). These small variation values are found to be due to the large size of the module. Since the number of shunts is also increased significantly (~10^4), and the impact of shunts in their neighboring regions is limited due to the contact resistance [73], non-local effects of the shunts diminish and performance loss is averaged.



(▪▪) 1 cm^2 cell without R_{SHUNT} (▫) 1 cm^2 cell with R_{SHUNT}

(▪▪▪) 0.65 m^2 module without R_{SHUNT} (▫) 0.65 m^2 module with R_{SHUNT}

Fig. 2.33 Change in the efficiency of CSS CdTe solar cell as the cell size is changed from lab-scale (1 cm^2) to module-scale (0.65 m^2) [58]. Copyright © by IEEE [12]

2.4.2.4. Looking Across Design Levels

After looking at the CSS CdTe solar cell design process at material, device and module levels one can clearly see the points to improve at each design step that would improve the final product's performance. At the material level this would be the improvement of GrS. The device design step indicates the importance of the Schottky barrier at the back contact. Therefore, more attention should be paid to contact formation during the material design step. In addition, increasing the GrS does not guarantee an increase in the module efficiency. Although the efficiency of a lab-scale device can increase to 11.6% due to larger average GrS, the final product's efficiency will be mainly limited to 6.8% due to R_{SER} and R_{SHUNT} limitations.

To sum up, the end-to-end model proposed in this section enables researchers to treat the design process as a whole and identify the bottlenecks. Without a big picture similar to the one provided here, it would be easy to waste valuable research resources by focusing on non-critical parts of the problem. Finally, this method can be used to obtain understanding and solve problems for any solar cell technology.

3. MODELING AND CO-OPTIMIZATION OF POLYCRYSTALLINE SILICON SOLAR CELLS AND POWER CONDITIONING CIRCUITRY FOR ENERGY SCAVENGING APPLICATIONS

3.1. Micro-scale Energy Scavenging Concept

Many electronics applications rely on the user or a service provider to replace the power source of a system once the battery's lifetime runs out. On the other hand, for many wearable electronics and wireless sensor network applications frequent replacement of battery is not a viable or an economically sound option. The system might be employed in a remote location (i.e. space weather visualization [74]), there might be large number of nodes and therefore large number of batteries to be replaced (i.e. agricultural management [75], structural condition assessment [76]) or simply it might be an inconvenience for the user (i.e. patient monitoring [77]). Micro-scale energy harvesting has emerged as a solution to this problem. It enables the system to replenish its power source with the energy harvested from its surrounding. This energy might be in forms of solar, thermal, piezoelectric or RF energy [78]. From these options, solar energy stands out with its high energy potential for indoor (~$\mu W/cm^2$) and outdoor (~mW/cm^2) applications [79]. The aforementioned problems often set unique constraints on the energy scavenging system which emphasize low power, small form factor and low cost.

The flow chart in Fig. 3.1 illustrates the working principles of a wireless sensor node powered by scavenged solar energy. A solar cell (photovoltaic cell) is employed to scavenge the solar energy and its output voltage (V_{PV}) is converted by the DC/DC power converter to the voltage required by the application unit (V_{VDD}). The application unit in Fig. 3.1 is composed of a sensing and a communication unit that transmits the sensed data to a central processor. A control circuitry is required to make sure that solar cell is operated at its optimum biasing point under different light irradiances throughout the day and year. The control circuitry achieves this goal by adjusting the input resistance of the

power converter to change the load of the solar cell. To avoid the large area requirement of a topology with an inductor, the power converter topology is chosen to be a linear charge pump for this work. Therefore, the control unit matches the input resistance of the power converter to the solar cell by regulating the switching frequency (f_{SW}) of the switches in the charge pump. The scavenged energy is stored in an energy buffer (e.g. a supercapacitor or a rechargeable battery) and provided to the application unit when the system is operational. Such systems are generally not operational all the time. The duty cycles can be as low as 1% which reduces the power consumption of the system [79].

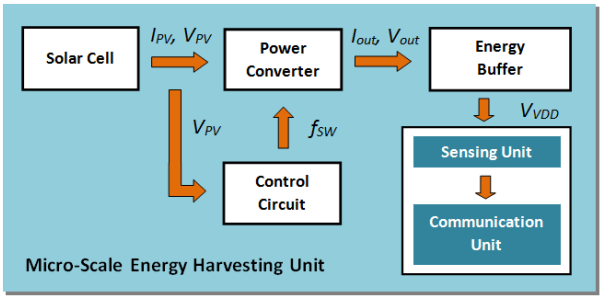


Fig. 3.1 Building blocks of a wireless sensor node powered by scavenged solar energy

Due to the large number of nodes required to implement a wireless sensor network, each node is required to be compact, low power and low cost. To reduce the cost of a node the system designed in this chapter is envisioned to be fabricated with low temperature polycrystalline Si (LTPS) process technology. LTPS utilizes lower deposition temperatures that reduce the energy consumption during fabrication. In addition, due to the low deposition temperature, the system can be manufactured on low cost flexible or glass substrates which will further reduce the cost. Since the whole system (including the solar cell and the peripheral circuitry) is aimed to be integrated on the same substrate with the same process technology, it is expected to be more compact as well. On the other hand, the system is expected to suffer from performance loss due to defective GB regions formed in the thin film. Therefore, there is a need to assess the feasibility of an LTPS wireless sensor node.

To achieve this goal, an end-to-end modeling approach is adopted. The simulation framework is built starting from the device level. At this level, the polycrystalline Si TFTs are modeled as the building blocks of the peripheral circuitry and a polycrystalline Si solar cell compatible with the TFT process is proposed as the transducer. At a higher level of abstraction, the results of device models are employed in circuit simulations and each circuit is studied in isolation. At the system level, the units illustrated in Fig. 3.1 are put together to study the interactions between the units and the performance of the overall system. Finally, the effects of the process parameters on the performance of the overall system are investigated.

By following such a holistic approach, the aim of this work is to provide more control over the process and more options to improve the system performance. This approach shines light on design trade-offs that is not visible for the conventional approach in which the building blocks are studied in isolation.

3.2. Thin Film Transistor Modeling

TFTs are metal oxide semiconductor field effect transistors (MOSFETs) that are fabricated on polycrystalline materials. They are widely used for display applications because of their low cost [80]. Due to the large number of GBs in the channel, the threshold voltage (V_{TH}) of a TFT is generally high (around 2.5V [81]) which increases the power consumption of the device. To solve this problem in [82] a very narrow TFT is proposed. In this work, the channel length of the TFT (L_{CH}) is set to be 200 nm, which is the average GrS of the ELA process in [81]. By doing that, the possibility of having more than 1 GB in the channel is reduced significantly and the V_{TH} is reduced to ~0.5V, which is very close to that of single-crystalline MOSFETs. Yet, the Si thickness of the proposed device is found to be too thin and therefore unfeasible for the TFT process that aims for low cost applications, whereas the observed short channel effects make this device a poor choice for analog applications.

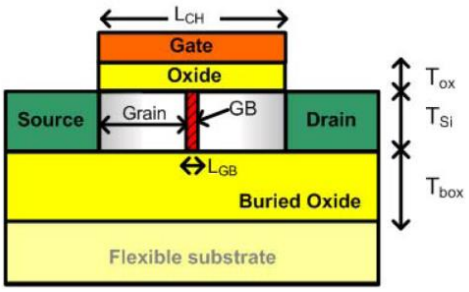


Fig. 3.2 The device structure of the modeled TFT [83]. Copyright © by IEEE [13]

Hence, methods to improve the performance of the proposed TFT device (see in Fig. 3.2) are investigated in this section [83] [84]. For this purpose, the effect of GB position on the V_{TH} of the TFT is studied first. The oxide thickness (T_{OX}) and Si thickness (T_{Si}) are chosen to be 10 nm and 20 nm consecutively, whereas buried oxide (BOX) thickness (T_{BOX}) is varied between 10 and 50 nm. On the other hand, the doping concentrations for p-type channel and n-type source and drain are set to be 10^{15} cm^{-3} and 5.10^{20} cm^{-3} consecutively. The polycrystalline structure is reconstructed in Sentaurus by placing 4 nm-wide highly defective regions between c-Si grains. The recombination in GBs is modeled with traps at 4 different energy levels (E_Ts) within the bandgap. The deep level traps are placed 0.05eV above and below the mid-gap, whereas their trap density (N_T) is set to be 10^{12} cm^{-2}. On the other hand, the band tail trap states are placed 0.02 eV away from both conduction and valence bands and they are assigned a trap density two orders of magnitude higher than N_T (10^{14} cm^{-2}). The capture cross-sections of these traps are assumed to be 10^{-15} cm^2 and equal for both holes and electrons [82]. The GBs are assumed to be unidirectional and their directions are set orthogonal to the current since this orientation is more detrimental on the cell performance than the parallel to the current direction [85].

As the first step of this analysis, the position of a single GB within the channel is varied and the drain current versus gate voltage (Id-Vg) curve of the transistor is looked into. The results in Fig. 3.3 indicate that the leakage current of the TFT increases as the

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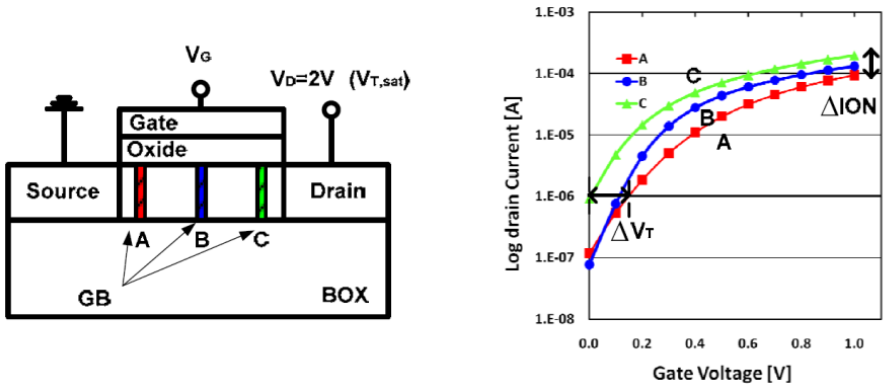
GB occurs closer to the drain since its effect on the source to channel energy barrier will be minimum. Because of the same reason, the saturation current of a TFT with a GB close to drain would be higher than a TFT with a GB close to source.



(a) (b)

Fig. 3.3 2D TFT device structure with a GB at different locations in the channel (a) and the corresponding Id-Vg curves (b) [83]. Copyright © by IEEE [13]

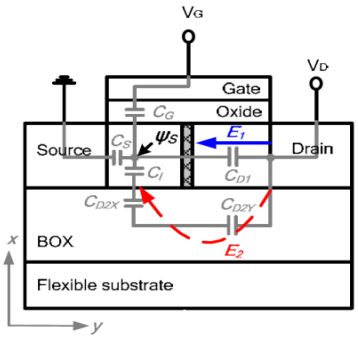


Fig. 3.4 Capacitive network that determines the energy barrier between source and the channel [83]. Copyright © by IEEE [13]

As the second step to this study, the analog performance of the proposed TFT is aimed to be improved. In terms of analog performance, the focus of this study is kept limited to output resistance (R_O) of the transistor since it determines the gain of an operational amplifier that can be designed with this TFT. Given that R_O of the TFT in Fig. 3.2 is heavily affected by drain induced barrier lowering (DIBL), emphasis is placed on this 2D effect. DIBL roots from the electric field due to the drain voltage (V_D) that

lowers the energy barrier between source and channel. The potential profile in the channel is affected by V_D via Si and BOX as shown in Fig. 3.4.

This effect can be modeled with a capacitive network as shown in Fig. 3.4 and the capacitance values can be represented as:

$$C_g = \varepsilon_{OX} \frac{W_{TFT} L_{CH}}{T_{OX}}, \qquad C_i \approx \varepsilon_{Si} \frac{W_{TFT} L_{CH}}{T_{Si}} \tag{3.1}$$

$$C_{d1} \approx \varepsilon_{Si} \frac{W_{TFT} T_{Si}}{l}, C_{d2x} \approx \varepsilon_{BOX} \frac{W_{TFT} L_{CH}}{T_{BOX}}, \; C_{d2y} \approx \varepsilon_{BOX} \frac{W_{TFT} T_{BOX}}{l} \tag{3.2}$$

$$C_{d2} = C_i || \, C_{d2x} || C_{d2y} \tag{3.3}$$

where W_{TFT} is the width of the transistor while l is the distance of the observed point from the drain, and C_{d2} is the parallel combination of C_i, C_{d2x} and C_{d2y}. The permittivity values of gate oxide, Si and BOX are given by ε_{OX}, ε_{Si}, ε_{BOX} consecutively. The surface potential in this case is given by:

$$\psi_S = \frac{C_g}{C_\Sigma} V_{gs} + \frac{C_{d1}}{C_\Sigma} V_{ds} + \frac{C_{d2}}{C_\Sigma} V_{ds} \tag{3.4}$$

where C_Σ is the series combination of C_g, C_{d1}, C_{d2} and C_S.

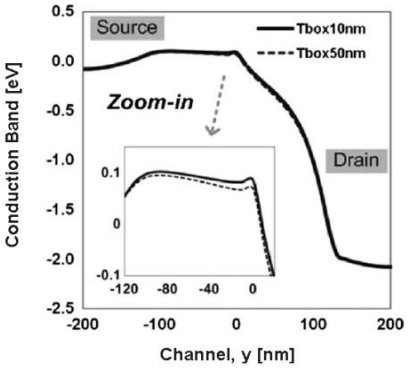


Fig. 3.5 Reduction in DIBL effect for thicker BOX thickness (T_{BOX}) observed at the conduction band diagram of the proposed TFT (V_{GS} = 1 V and V_{DS} = 2 V [84]). Copyright © by IEEE [14]

[14] © 2011 IEEE. Reprinted with permission from Kim et.al, Thin-BOX Poly-Si Thin-Film Transistors for CMOS-Compatible Analog Operations, IEEE Transactions on Electron Devices, 2011.

For L_{CH} values larger than T_{BOX}, C_{d2y} tends to be smaller than C_{d2x} and thus dominates the C_{d2} term. Therefore, when the T_{BOX} is reduced, C_{d2} value reduces, leading to reduced DIBL as shown in Fig. 3.5 and a larger R_O.

3.3. Thin Film Transistor Process Compatible Polysilicon Solar Cell Model

Once the TFT model is in place, the initial 2D solar cell model is built and optimized in Sentaurus. It would be desired for all devices to have the same thickness so that both the solar cell and the peripheral circuitry of the wireless sensor system can be fabricated on the same substrate. Yet, this brings forwards two challenges. First of all, Si is an indirect bandgap material. Therefore, a Si solar cell requires a thick absorber layer (~400 μm [5]). This problem can be tolerated for the wireless sensor node applications since the system is operated for short periods of time (see Section 3.1). Yet, the power output of the solar cell should be determined and optimized accurately. Secondly, during the contact formation of a very thin solar cell, there is a possibility for the contact metals to diffuse into the material via GBs and shunt the device [86]. Thus, instead of a vertical current flow, a horizontal current flow is proposed for the solar cell used in this work (see Fig. 3.6).

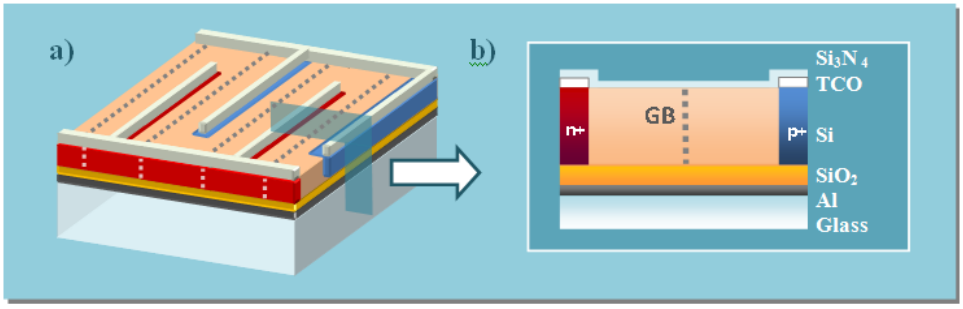


Fig. 3.6 The top view (a) and cross section (b) of the proposed polycrystalline Si solar cell structure.

Following the same design idea used for TFTs in Section 3.2, the distance between the highly doped contact regions of the proposed cell (W_{SC}) is set to be the average GrS of the fabrications process to improve the cell performance. That is why the W_{SC} is chosen to be 200 nm as it is the average GrS of the ELA process in [81]. The SiO_2 and

glass layers are set to be 50 nm and 1 μm-thick respectively. The work function of transparent contacts (TCOs) is determined as 4.45 eV [87]. They are assumed to be transparent and their s_R is set to be 10^5cm/s. The width of the contacts is chosen to be 50 nm and the contact resistance is modeled with Schottky barrier resistance model in [88].

Before starting the optimization process, n+, p, and p+ regions are doped 10^{18}, 10^{15} and 10^{18} cm^{-3} respectively and the Al layer at the bottom is omitted. Mobility is modeled to be doping dependent [89] and bandgap narrowing is also taken into account [90]. The recombination at GBs is modeled as in Section 3.2 while SRH and Auger recombination is calculated throughout the sample. For SRH, the crystalline Si parameters (10^{-4} s for electron and hole lifetimes) are employed, whereas 10^{-30} cm^6/s is used as Auger recombination coefficient for electrons and holes. Finally, the simulations are conducted under AM 1.5 illumination conditions.

3.3.1. Optimization of the Single-crystalline Structure

Before studying the polycrystalline structure and the effects of GBs on the performance of the solar cell, the device's optical properties and doping profile are optimized for a single-crystalline structure in the following sections.

3.3.1.1. Optical Enhancement of the Proposed Structure

As it was discussed in Section 3.3, thick absorber layers are required for Si solar cells and the optical generation within a 100 nm-thick polycrystalline Si layer is very limited. Hence, the efficiency values that can be obtained for a polycrystalline Si solar cell without any light trapping mechanism are low. That is why two light trapping mechanisms are implemented into the proposed cell structure in this section.

The structure in Fig. 3.6.b is simulated without the Al layer as the reference cell which does not have any light trapping schemes. Afterwards, a Si_3N_4 antireflective coating (ARC) is placed on top of the cell and an Al layer at the back of the device consecutively. The ARC layer's thickness is optimized to be 46 nm for the device under investigation and the results are reported in Table 3.1. Both methods are found to be improving mainly J_{SC} and therefore the efficiency of the cell. ARC achieves this by

reducing the reflection of the incoming light on the front surface while the Al layer increases the reflection and the optical length of the device.

Table 3.1 The effects of light trapping mechanisms on the 100 nm-thick solar cell [91]. Copyright © by IEEE [15]

	Jsc (mA/cm^2)	**Voc (V)**	**Efficiency (%)**
Without light trapping	2.63	0.5516	1.17
With only 46 nm ARC	4.16	0.5634	1.89
With only Al reflective layer	3.97	0.5622	1.8
With Al reflective layer and 46 nm ARC	5.5	0.5706	2.52

3.3.1.2. Optimization of the Doping Profile

As a second method, the performance of the proposed cell can be improved by optimizing the doping profile of the structure. Generally, a high internal electrical field is desired to make sure the generated carriers are collected before recombining in the bulk or at the GBs. This can be achieved by highly doping the n+ and p+ regions, yet high doping levels are associated with additional loss mechanisms. Hence, an optimum doping profile exists for the structure.

During the doping optimization process, the lightly doped p region's doping concentration is fixed to be $10^{15}cm^{-3}$. The doping levels of n+ and p+ regions are assumed to be same and their values are varied between 10^{17} cm^{-3} and 10^{21} cm^{-3}. As it can be observed from Table 3.2, the best efficiency for the single-crystalline structure is obtained when the doping density of n+ and p+ regions is 10^{19} cm^{-3}. The contact resistance is found to be reducing the efficiency for doping values smaller than 10^{19} cm^{-3}.

[15] © 2011 IEEE. Reprinted with permission from Mungan et.al, 2D Modeling and optimization of excimer laser annealed thin film polysilicon solar cells, Proceedings of 37th IEEE Photovoltaic Specialists Conference (PVSC), 2011.

On the other hand, for doping values higher than 10^{19} cm^{-3}, the doping dependent mobility values are reduced. Bandgap narrowing also reduces the carrier generation in the areas under contacts leading to a decrease in J_{SC}. Finally, Auger recombination becomes prominent for very high doping values (10^{21} cm^{-3}) and causes a reduction in V_{OC}.

Table 3.2 Performance metrics for different doping concentrations [91]. Copyright © by IEEE [15]

Doping (cm^{-3})	**Jsc (mA/cm^{-2})**	**Voc (V)**	**FF (%)**	**Efficiency (%)**
10^{17}	5.52	0.528	71.21	2.07
10^{18}	5.5	0.571	80.38	2.52
10^{19}	5.47	0.604	82.82	2.73
10^{20}	5.37	0.608	82.92	2.71
10^{21}	4.09	0.543	81.36	1.81

3.3.2. Effects of a Single Grain Boundary on the Device Performance

Once the single-crystalline model for the proposed solar cell is finalized, a GB is placed into the structure. First, the change in solar cell performance due to existence of GB is investigated for different T_{Si}s and N_Ts. Later on, the sensitivity of the cell performance to the GB position is explored.

3.3.2.1. Effects of Device Thickness and Grain Boundary Trap Density

The performance of a single-crystalline solar cell can significantly change once a GB exists within the device. This change is mainly dependent on the number of GBs, T_{Si} and N_T at the GB. To explore the effects of these variables, a single GB is placed in the middle of the device and its performance is compared to that of a single-crystalline solar cell in this section.

The analysis is started with the investigation of T_{Si}'s effect on the performance of a single-crystalline and a polycrystalline-Si solar cell. As the results in Fig. 3.7 indicate, the

efficiency of a single-crystalline solar cell increases in a non-linear fashion with T_{Si}. A similar trend is observed for the polycrystalline structure with a single GB with an N_T of 10^{12} cm^{-2}. Yet, the efficiency values are found to be significantly lower compared to the single-crystalline cell. In addition, the efficiency of an 800 nm-thick polycrystalline cell is marginally higher than a 400 nm-thick one. Therefore, 400 nm is determined to be a good choice for T_{Si} since it would keep the cost of the polycrystalline device low while maintaining the efficiency. By doing that, the TFT process limitations on T_{Si} can also be satisfied.

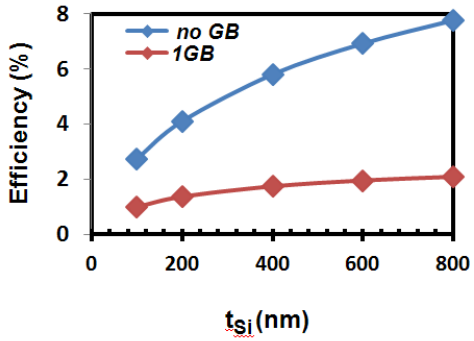


Fig. 3.7 Dependence of cell efficiency on device thickness for a single–crystalline cell (no GB) and a cell with a single GB (1GB) [91]. Copyright © by IEEE [15]

Table 3.3 Impact of trap density (N_T) on the polycrystalline cell performance [91] . Copyright © by IEEE [15]

N_T (cm^{-2})	Jsc (mA/ cm^{-2})	Voc (V)	FF (%)	Efficiency (%)
$2x10^{11}$	5.467	0.3917	64.01	1.37
10^{12}	5.465	0.307	58.97	0.99

The significant reduction in performance due to the presence of a GB, observed in Fig. 3.7, can be alleviated by reducing the N_T of the GB. The reduction in N_T can be achieved by passivation methods such as plasma hydrogenation [92]. The results in Table 3.3 demonstrate the extent of a possible performance improvement if the N_T is reduced from 10^{12} cm^{-2} to $2x10^{11}$ cm^{-2}. Reducing N_T improves the performance in two aspects.

First, the s_R of the GB reduces. Secondly, the energy barrier at the GB reduces due to the reduction in the number of available positions for charges to be trapped along the GB. This reduction in GB recombination results in higher V_{OC} and FF for the polycrystalline Si solar cell.

3.3.2.2. Effects of GB position

In a real device, the GBs can occur anywhere with random distances between them. Now that the number of GBs in the device can be reduced by keeping the W_{SC} small, one would wonder if there is a sweet spot for a GB to be placed such that it would be very detrimental. To answer this question, a single GB is placed within the p region of the solar cell and its position is varied from n+ region to p+ region. The normalized J_{SC}, V_{OC} and efficiency values of these devices with GBs at different positions are illustrated in Fig. 3.8.

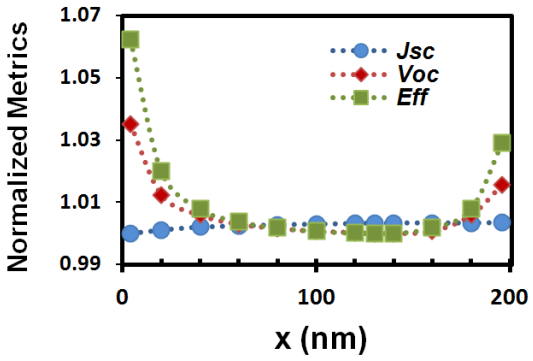


Fig. 3.8 Change in the performance metrics of the proposed solar cell with respect to the position of a single GB [The results are normalized with respect to the minimum value for that metric] [91]. Copyright © by IEEE [15]

The SRH recombination rate is maximized where the number of electrons and number of holes (n and p) are equal. Confirming this expectation, the results indicate that the recombination at open circuit condition is maximized (and V_{OC} is minimized) at 130 nm away from the n+ region. This point is where n and p are equal to each other in a single-crystalline cell. Moving away from this sweet spot, either n or p reduces and hence

the recombination rate drops. On the other hand, the energy barrier at GB location plays a limiting role for short circuit conditions. The sign and number of the net charges along the GB change with respect to the GB position. As GB gets closer to the n+/p junction, n trapped at the GB becomes larger than trapped p. Therefore, the barrier height increases while the J_{SC} decreases. Overall, the efficiency is found to be following the V_{OC} trend and the amount of variation is observed to be small.

3.3.3. Effect of Multiple Grain Boundaries on the Device Performance

Since the W_{SC} of the proposed device is chosen to be 200 nm, the possibility of having more than one GB is reduced significantly for a process with an average GrS of 200 nm. Even though this fact limits the V_{TH} of the TFT device and the recombination in the solar cell, it forces a restriction on the lithography process. Such restrictions are generally overcome by employing more advanced technologies that might introduce an increase in the process cost. To avoid such a cost, a wider W_{SC} might be more favorable. Yet in that case, the probability of having multiple GBs increase. Thus, an optimization for the W_{SC} would be required.

As possible W_{SC}s, 250 nm and 350 nm are chosen for the initial optimization process. Since the chosen values are narrower than 400 nm, the possibility of having 3 GBs is considered to be low. Hence, the maximum number of GBs that can occur within the device is assumed to be 2 for this analysis. To estimate the worst case scenario, 2 GBs are placed in the lightly doped p region of the solar cell and the distance between the GBs is fixed to be 200 nm. When the position of the first GB (and therefore the second GB) is varied, the GB recombination is found to be maximized when the GBs are placed equidistant from the n+/p and p/p+ junctions. It is observed that when the GBs are placed in that fashion, both GBs collect carriers effectively instead of one being favored.

3.3.3.1. Effect of Device Width

In this section, the performance of the proposed solar cell structure is evaluated for different W_{SC}s in the presence of different number of GBs. The design space is explored for various W_{SC}, T_{Si} and N_T combinations. For each W_{SC}, efficiency values for possible

number of GBs that can occur within the device are reported in Table 3.4. In each case, the GBs are placed at positions they are most detrimental to the efficiency of the cell. The results for this analysis indicate the performance of a 350 nm-wide device performs slightly better than 200 and 250 nm-wide samples when there is no GB or there is a single GB in the device. Yet, unlike the 200 nm-wide sample, 350 nm-wide sample has a higher possibility of having 2 GBs. In that case, the performance of the 350 nm-wide sample is slightly lower than a 200 nm-wide sample with a single GB.

Table 3.4 Efficiency of the proposed TFT process compatible solar cell [91]. [15]

Solar cell width (W_{SC}), polycrystalline Si thickness (T_{Si}), trap density (N_T) and number of GBs present within the device (0GB, 1GB and 2GBs)

EFFICIENCY (%)

		W_{SC} = 200 nm		**W_{SC} = 250 nm**			**W_{SC} = 350 nm**		
	Nt (cm^{-2})	**0GB**	**1GB**	**OGB**	**1GB**	**2GBs**	**OGB**	**1GB**	**2GBs**
T_{Si} = 100 nm	**$2x10^{11}$**	2.73	1.37	2.76	1.41	1.27	2.79	1.46	1.34
	10^{12}	2.73	0.99	2.76	1.02	0.8	2.79	0.97	0.83
T_{Si} = 400 nm	**$2x10^{11}$**	5.79	2.47	5.83	2.54	2.28	5.9	2.66	2.42
	10^{12}	5.79	1.73	5.83	1.79	1.51	5.9	1.89	1.57

The increase in the performance with W_{SC} is due to the decrease in the ratio between highly doped contact regions to the lightly doped intrinsic region. Since the contact regions are highly doped, the losses associated with it such as lower mobility, higher Auger recombination and bandgap narrowing degrades the cell's performance. Therefore, for a wider device with long carrier lifetimes, increasing W_{SC} increases the cell performance. On the other hand, as W_{SC} gets wider the probability of the generated carriers recombining before they are collected increases. Therefore, an optimum width

exists for the proposed device's W_{SC} depending on its carrier lifetime. Since c-Si parameters are employed for the grains and the explored W_{SC} values are small compared to the diffusion length of the carriers, the performance of the simulated device is found to be often improving with W_{SC} for the range of values investigated here.

The only instance where 250 nm-wide cell outperforms the 350 nm-wide cell is found to occur when the device have a T_{Si} of 100 nm and a single GB with an N_T of 10^{12} cm^{-2}. This reversal in the trend can be explained as follows. The performance of the 350 nm-wide cell is observed to be limited by the energy barrier at a GB close to the n+ region. For T_{Si}=100 nm case, the generation rate is limited, whereas the negative charge along this GB is maximized. Since the thicker samples have higher generation rates, p at the GB position is higher. This increase reduces the number of net trapped charges and the energy barrier at the GB. Hence, J_{SC} and efficiency is improved for thicker samples. Similarly for samples with N_T =2.10^{11} cm^{-3} GBs, the energy barrier remains low and the general trend stands valid.

3.3.4. Estimation of a Centimeter-scale Cell Efficiency

In the previous sections, the worst cases for the proposed polycrystalline-Si cell are investigated. That is to say, if the W_{SC} of the device is 350 nm, the whole 1 cm^2 cell is assumed to be composed of unit cells with two GBs. In reality, some of the unit cells are going to have no GBs, where some of them will have one, two or more GBs depending on the GrS distribution. Therefore, the efficiency of a 1 cm^2 cell is expected to be different than a unit cell with two GBs.

To estimate this efficiency, SPICE models are extracted for unit cells with different number of GBs. The shunt and series resistance components of the solar cell SPICE model (see Fig. 1.4.b) are omitted due to the size of the cell (1 cm^2). Afterwards, the probability of having a specific number of GBs (P_{GB}) in a unit cell is calculated based on the formalism in [93]. Assuming the unit cell's depth is 1 μm, the number of unit cells required to build the 1 cm^2 cell (N_{UC}) is calculated. Later on, the number of unit cells with a specific number of GBs in them is calculated by multiplying P_{GB} with N_{UC}. Finally, these unit cells with different number of GBs are connected in parallel to make up the SPICE model of the 1 cm^2 cell.

Following the aforementioned procedure, the efficiency of a 1 cm^2 cell with a 400 nm T_{Si} is calculated. The results for 200 and 350 nm-wide devices with $2x10^{11}$ cm^{-2} and 10^{12} cm^{-2} N_Ts are illustrated in Fig. 3.9. In general, as the average GrS of the process increases the possibility of having a GB within the device reduces. This change leads to a higher V_{OC} and efficiency values close to that of a single-crystalline cell. Secondly, the performance of the 350 nm-wide device is found to be less than 200 nm-wide one. Yet, the reduction is found to be marginal. Thus, increasing the W_{SC} to 350 nm to reduce the cost of this technology would be a sound decision.

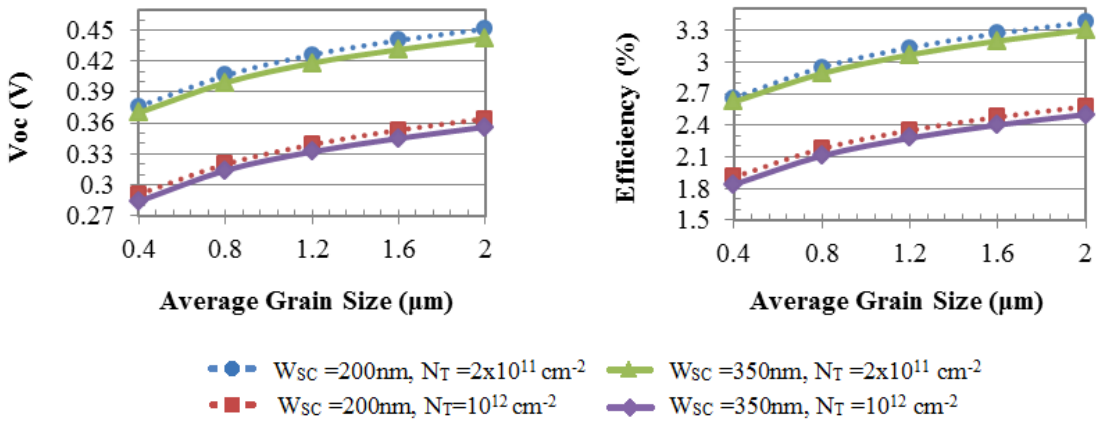


Fig. 3.9 The open circuit voltage (V_{OC}) and efficiency of a 1 cm^2 polycrystalline Si solar cell with respect to the average grain size [91]. Copyright © by IEEE [15]

3.4. Effects of Process Parameters on Device, Circuit and System Levels in a Polysilicon Based Energy Scavenging System

In this section the modeling and optimization efforts in the previous sections are going to be put together with circuit and system modeling efforts under one simulation framework. This framework will be used to study the impact of process parameters on the performance of a micro-scale energy harvesting system. During the design process of an energy scavenging system, the first step involves modeling the effects of deposition process on the performance of devices to be used. Therefore, there is a need for device level models that can translate the quality of the material to the performance of the solar

cell and the TFTs. In order to obtain the maximum power from the solar cell, a second layer of design procedure should be applied that involves the design and optimization of the power converter circuitry that acts as the load of the solar cell. At the last step, the solar cell and the circuitry should be co-optimized to provide the optimum results. The proposed simulation framework that can capture these steps would prove to be valuable since it can provide physical insight to every design step. Finally, although the following work employs polycrystalline Si as the substrate material, the simulation framework can be extended to other materials.

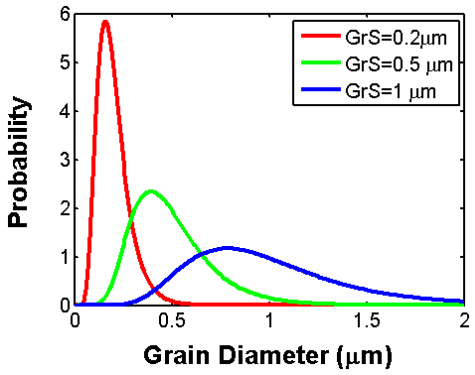


Fig. 3.10 Lognormal grain size (GrS) distributions of processes with different average GrSs

3.4.1. Process Parameters

In this work, the whole energy scavenging system is envisioned to be deposited with the same technology and therefore a change on the process parameters, namely GrS distribution and GB trap density (N_T) would affect the system at multiple levels. For the process in question, N_T is chosen to be 10^{18} cm^{-3} and 5.10^{18} cm^{-3} (3D equivalent of 10^{12} cm^{-2} and 2.10^{11} cm^{-2} values in Section 3.3.2.1). The GrS distributions are set to be lognormal with average GrSs of 0.2, 0.5 and 1 μm while the standard deviation of the associated normal distribution is set to 0.4 μm. The GrS distributions of these processes are plotted in Fig. 3.10.

3.4.2. Effects of Process Parameters on the Performance of Thin Film Transistors

The process parameters would affect the power conditioning unit via the change in the TFT performance. For instance, the GrS distribution determines the number of GBs in a TFT. Due to the varying number of GBs occurring at random positions in a TFT, V_{TH} might have a wide spread distribution. To estimate this distribution, the TFT model in Section 3.2 is modified and 100 samples are simulated to demonstrate the statistical nature of the problem. The results in Fig. 3.11 and in Fig. 3.12 are obtained for an n-type TFT (nTFT) and a p-type TFT (pTFT) with L_{CH}=0.5 μm. Other parameters used in the simulations are listed in Table 3.5 and the V_{TH} values are determined as the gate to source voltages that provide 10^{-8} A/μm current for a drain to source voltage of 50 mV.

Table 3.5 TFT Device Simulation Parameters

Channel Length (L_{CH}), Si and SiO_2 thicknesses ($T_{Si\ TFT,}$ T_{OX}), doping concentrations for source and drain regions (N_S, N_D), pTFT Body Doping (N_{Dbody}), nTFT Body Doping (N_{Abody})

Parameter	Value
L_{CH}	500 nm
$T_{Si\ TFT,}$ T_{OX}	50 nm, 15 nm
N_S, N_D	10^{20} cm^{-3}
N_{Dbody}	10^{15} cm^{-3}
N_{Abody}	10^{17} cm^{-3}

In both Fig. 3.11 and Fig. 3.12, the number of samples with the minimum V_{TH}s (0.14 V for pTFT and 0.75 V for pTFT) increase as the GrS is increased, indicating that the probability of not having a GB inside the channel increases as the GrS increases. For the process with $N_T = 5.10^{18}$ cm^{-3}, the gap between the minimum and maximum V_{TH}s of the process technology is significantly higher than the process with $N_T = 10^{18}$ cm^{-3}. The results indicate that the process variation problem observed for $N_T = 5.10^{18}$ cm^{-3} case can be alleviated by choosing a GrS larger than the L_{CH} (e.g. GrS = 1μm) so that samples with GBs within can be limited.

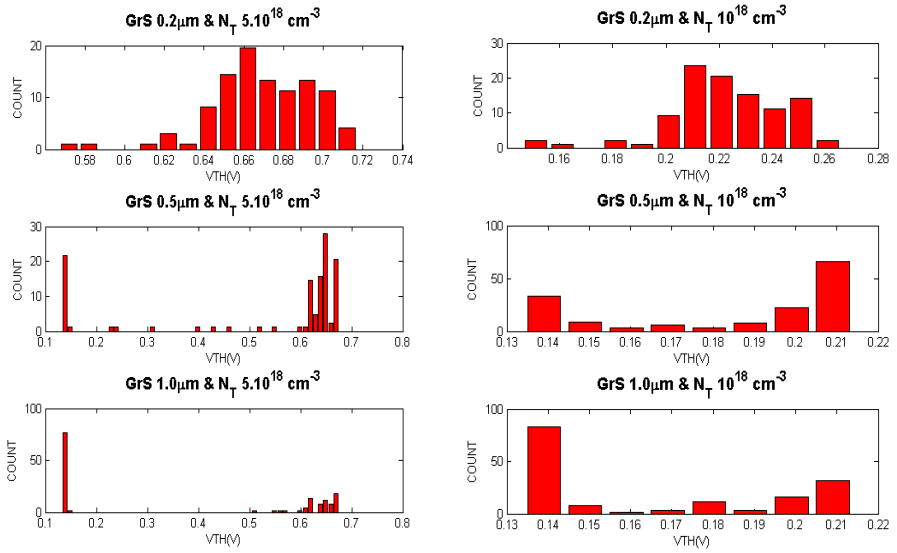


Fig. 3.11 Threshold voltage (V_{TH}) distribution of nTFTs for different trap densities (N_Ts) and grain sizes (GrSs)

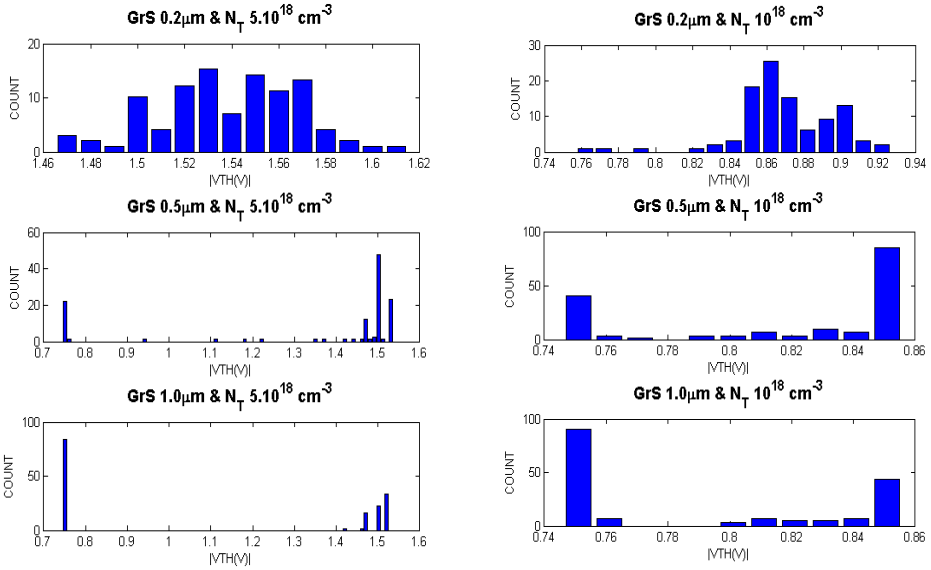


Fig. 3.12 Threshold voltage (V_{TH}) distribution of pTFTs for different trap density (N_Ts) and grain sizes (GrSs)

Another observation that can be made on Fig. 3.11 and Fig. 3.12 is the non-Gaussian shape of the V_{TH} distribution for GrS=0.5 μm and $N_T = 5.10^{18}$ cm^{-3}. At first sight, one might argue the shape of the distribution is due to the lack of data. Yet, what is observed here is the quantization of the possibilities of having a single-crystalline TFT or a polycrystalline TFT with 1 or 2 GBs. Surely, this distribution would be valid if only the GB position and N_T are the reasons for the variation. In reality, there will be other effects due to the non-ideal nature of the TFT process, such as non-uniform $T_{OX,}$ that will modify the distribution shape.

Due to the multimodal nature of these distributions, it is decided to use two V_{TH}s to define a distribution: one for single-crystalline devices and another one for the polycrystalline devices. To see what V_{TH} value would be a good representation of a polycrystalline Si process with a certain N_T and average GrS, a boxplot of each distribution (without the single-crystalline samples) is plotted. The representative V_{TH}s for polycrystalline Si devices are determined as the medians of the boxplots illustrated in Fig. 3.13 and Fig. 3.14. The representative V_{TH}s are found to change marginally for processes with different GrSs. Therefore, a single V_{TH} value is used for TFTs with different GrSs in this work. Since the representative V_{TH} of GrS = 0.2 μm is the highest, it is selected as the value to be used in circuit simulations (see Fig. 3.7). Finally, Level 62 RPI polycrystalline Si SPICE models are extracted for devices with the representative V_{TH}s.

Table 3.6 V_{TH} Values Used for TFTs in Circuit Simulations

	sC	**N_T =10 ^{18} cm^{-3}**	**N_T =5x10 ^{18} cm^{-3}**
nTFT	0.14 V	0.22 V	0.67 V
pTFT	0.75 V	0.87 V	1.54 V

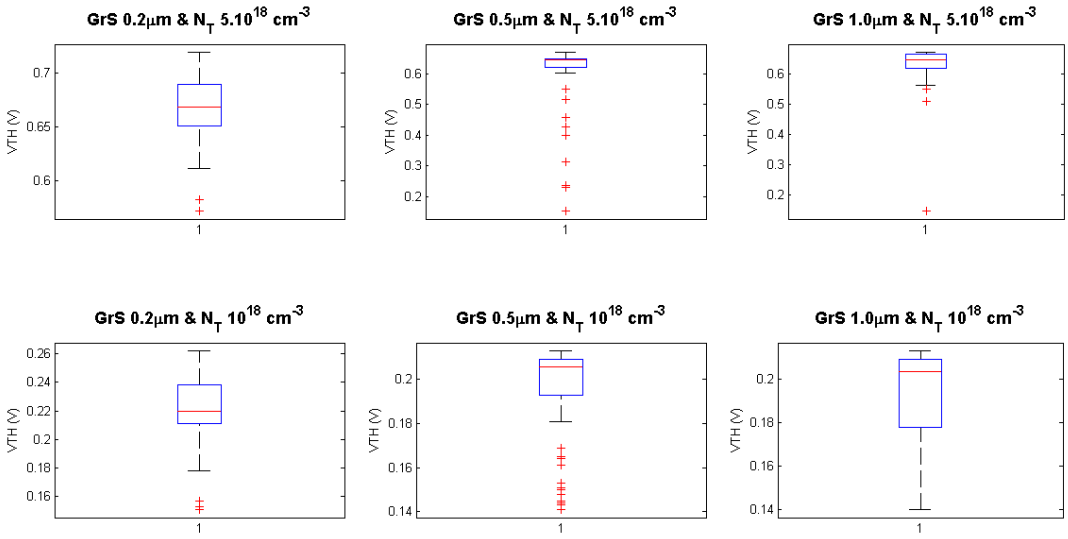


Fig. 3.13 Boxplot of threshold voltages for nTFTs with different trap densities (N_Ts) and grain sizes (GrSs)

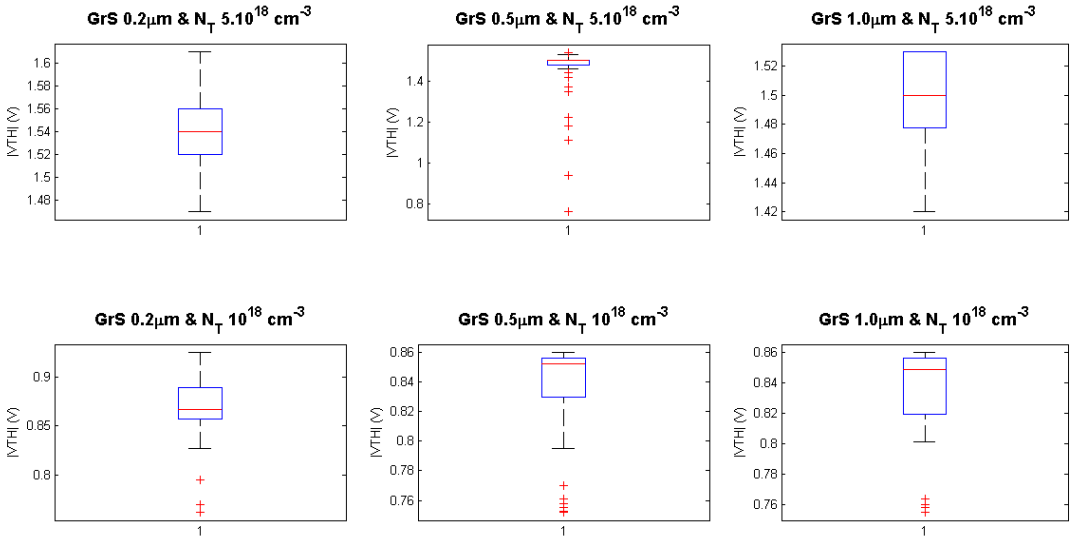


Fig. 3.14 Boxplot of threshold voltages for pTFTs with different trap densities (N_Ts) and grain sizes (GrSs)

For the purpose of comparison, the Id-Vd and Id-Vg curves of the devices with these representative V_{TH}s are plotted in Fig. 3.15. From the performance of the devices, it is evident that nTFT outperforms the pTFT. The main reason behind this high V_{TH} of pTFT

is found to be due to the work function of Al gate. In addition, the midgap traps cause the subthreshold slope to be gentle (pseudo subthreshold slope [94]) which is observed to increase the V_{TH} of pTFTs even further. As pTFTs are required to design a linear charge pump, they are expected to be the limiting factor for the performance of the power converter circuitry. Since the application unit of the system is assumed to have the power requirements of the TELOS wireless node [95], 2.4 V is required to operate the system. Therefore, the V_{TH} of the pTFT is desired to be no more than 1.5 V. The values in Table 3.5 are selected to satisfy this condition and T_{OX} is scaled in an iterative fashion for the same purpose. Finally, the results in Fig. 3.15 indicate the effect of GBs with $N_T = 10^{18}$ cm^{-3} on the TFT performance is found to be very small.

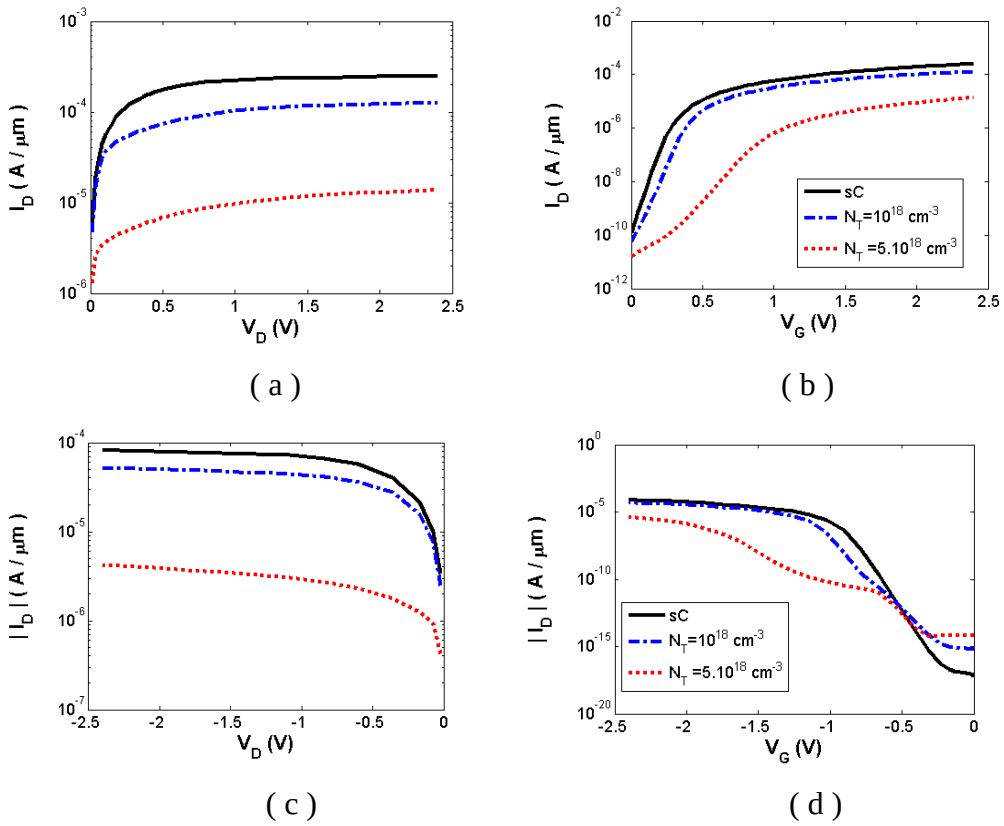


Fig. 3.15 Id-Vd (|Vg|=2.4V) and Id-Vg curves (|Vd|=2.4V) of nTFT (a-b) and pTFT (c-d) [source is grounded]

3.4.3. Effects of Process Parameters on the Performance of Solar Cells

As the power source of the system on glass, the solar cell device structure in Fig. 3.6 was previously proposed in Section 3.3. W_{SC} was assumed to be equal to the average GrS of a process such that the maximum number of GBs that can occur in the channel would be limited to 1. Yet, this would require very small process features, which would increase the process complexity and cost. To study further trade-offs between cost and performance, the simulation framework is modified such that it can simulate the performance of a device with multiple GBs (for different W_{SC}s and T_{Si}s) in a faster fashion. This is achieved by solving the 1D drift-diffusion equations in MATLAB using the Newton's iteration scheme [96] for the structure in Fig. 3.6.b. The fast nature of the simulation framework is utilized to conduct large-scale simulations that can take random GB positions and number of GBs into account. The GBs are modeled as in Section 3.2, whereas the dimensions and doping profile of the simulated device are summarized in Table 3.7. The mobility and lifetimes of the carriers are assumed to be concentration dependent [89] [97]. Yet, mechanisms like Auger recombination, bandgap narrowing and Schottky barrier contact resistance are not taken into account in this model.

Table 3.7 Parameters used to model the solar cell of micro-scale energy scavenging system

Doping concentrations for n+, p, p+ regions (N_{D+},N_A,N_{A+}), width of p region (W_{SC}), width of contact region (W_{CNT}); Si, Si_3N_4,SiO_2 thicknesses (T_{Si}, T_{Si3N4}, T_{SiO2}).

Parameter	Value
$\mathbf{N_{D+}}$,$\mathbf{N_A}$,$\mathbf{N_{A+}}$	10^{18}, 10^{15}, 10^{18} cm^{-3}
W	0.2 -0.8 μm
$\mathbf{W_{CNT}}$	50 nm
$\mathbf{T_{Si}}$	0.2 -0.8 μm
$\mathbf{T_{Si3N4}}$, $\mathbf{T_{SiO2}}$	46 nm, 50 nm

To be able to embed the generation profile into the device simulator, the optical generation rate (G) at a specific depth (y) of a polycrystalline Si solar cell with a thickness of T_{Si} is modeled as follows [98]:

$$G(y) = A(t_{Si})\, e^{-\alpha(T_{Si})y} + B(T_{Si})\, e^{-\beta(T_{Si})y} + C(T_{Si}) \tag{3.5}$$

$$X(T_{Si}) = X_1 + X_2 T_{Si} \tag{3.6}$$

$$C(t_{Si}) = C_1 + e^{C_2 + C_3 T_{Si}} \tag{3.7}$$

where A, B, α, and β functions in Eq. (3.5) have the form of Eq. (3.6) and the C function has the form of Eq. (3.7). The X_1, X_2, C_1, C_2, and C_3 terms in Eq. (3.5) and Eq. (3.6) are fitting parameters. These parameters are extracted by fitting Eq. (3.5) to the optical generation profiles of polycrystalline Si solar cells obtained from numerical simulations done in Sentaurus. The numerical simulations are conducted under AM 1.5 illumination for 0.2 to 0.8 µm-thick polycrystalline Si solar cells and the results are illustrated in Fig. 3.16. Even though Eq. (3.5) is an empirical fit, its terms carry physical significance. The first and second terms model the absorption of photons with short and long wavelengths, while the third one is a correctional term due to the reflection at the Al layer.

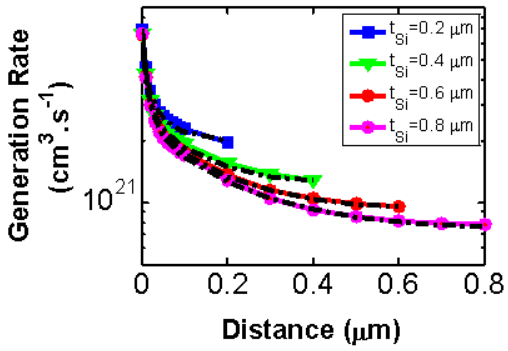


Fig. 3.16 Generation profiles for the proposed device obtained with the empirical model (colored solid lines) and numerical model (black dashed lines) [98]. Copyright © by ACM [16]

[16] Reprinted with permission from Mungan E. S., "Modeling, design and cross-layer optimization of polysilicon solar cell based micro-scale energy harvesting systems", Proceedings of International Symposium on Low Power Electronics and Design (ISLPED), © 2012 ACM. http://doi.acm.org/10.1145/2333660.2333693

Once the simulation framework is established, its results in Fig. 3.17 are compared to the 2D simulation results obtained for the same structure in Sentaurus. Although there are slight mismatches between the MATLAB and Sentaurus models due to the 2D effects, the results are found to be agreeing well with each other. In general, a continuous increase in the efficiency of the cells is observed with increasing T_{Si}. Similar to Section 3.3.2.1, the improvement rate is dampened for cells with GBs. The performance of the device is found to be rapidly degrading with the presence of a single GB (unlike the TFTs in Fig. 3.15), whereas the second GB is found to be not as destructive as the first one.

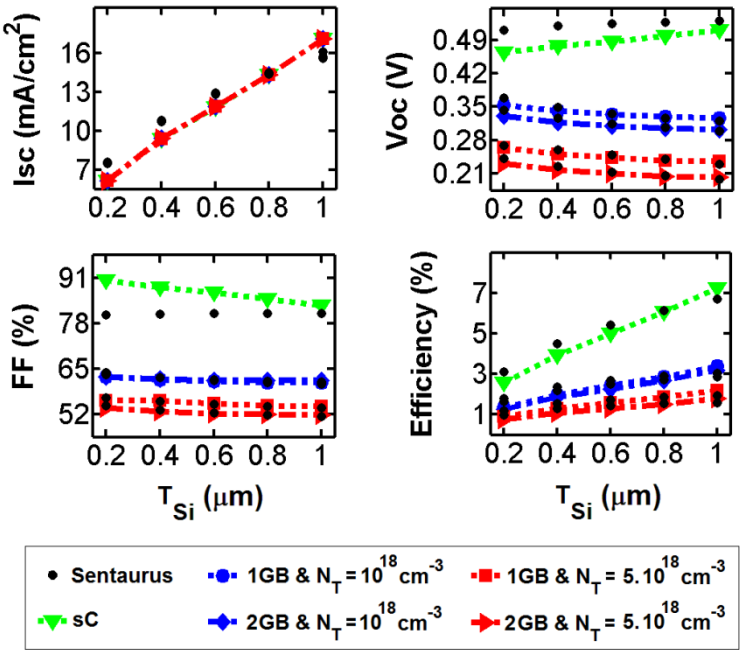


Fig. 3.17 Comparison between 1D MATLAB model and 2D Sentaurus results for the proposed solar cell for the cases when there is no GB (sC), 1 GB at $W_{SC}/4$ distance away from the n+ region (1GB) and 2 GBs placed $W_{SC}/4$ distance away from the n+ and p+ regions (2GB) [W_{SC}=200 nm]

The results in Fig. 3.17 are obtained for a W_{SC} of 200 nm. When the study is extended for multiple W_{SC}s and carrier lifetimes, the results in Fig. 3.18 are obtained. Similar to the results obtained in Section 3.3.3.1, the efficiency of the cell is found to increase with W_{SC} for samples with long lifetimes ($\tau_n=10^{-5}$ s, $\tau_p=3.10^{-6}$ s [97]) and high

mobility values. Yet, when τ_n is low ($\tau_n = \tau_p = 10^{-9}$ s) or there is a GB in the device, the generated carriers are recombined before they reach to the contacts for longer widths. Therefore, an optimum W_{SC} value exists for those cases. This value is observed to be ~0.8 µm for 1GB cases (when GB is at $W_{SC}/4$ distance away from the n+ region) while it is ~1.4 µm for the single-crystalline sample with low τs.

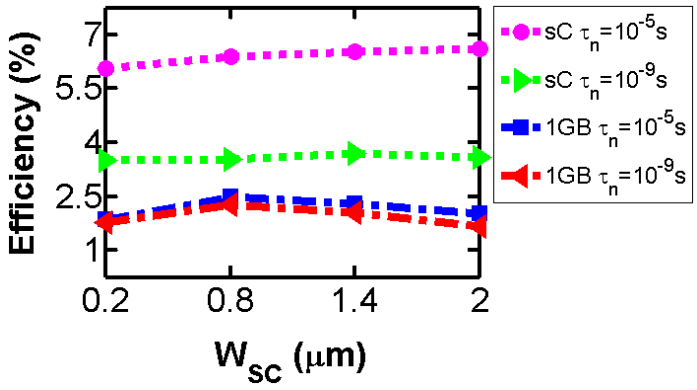


Fig. 3.18 Width dependency of the proposed solar cell's efficiency for different lifetimes and cases when there is no GB (sC) and 1 GB at $W_{SC}/4$ distance away from the n+ region (1GB) [T_{Si}=0.8 µm]

Once the 1D simulation results are calibrated for micron-scale devices, the results are extrapolated for a 1 cm^2 device. For this purpose, the GBs are assumed to occur only along the direction perpendicular to the current flow. Then, the GBs are placed randomly in 100 micron-scale cells based on the lognormal distributions in Fig. 3.10. Later on, the simulated unit cells are connected in parallel to make up a 1 cm^2 sample using the method in Section 3.3.4 and the results are plotted in Fig. 3.19.

In Fig. 3.19.a, it is shown that wider devices, which are prone to have multiple GBs, have lower efficiencies when T_{Si} =0.8 µm. On the other hand, having less probability of containing a GB, does not necessarily guarantee a high efficiency when T_{Si} =0.2 µm. To further analyze this trend, the unit cell efficiency distributions are provided in Fig. 3.19.b to e. The distributions indicate the W_{SC}=0.8 µm samples perform better compared to W_{SC}=0.2 µm samples when they are single-crystalline or when they have one GB (in line with the results in Fig. 3.18 and Section 3.3.3.1). On the other hand, W_{SC}=0.8 µm

samples can have two GBs. These competing mechanisms create the change in the trend observed for different T_{Si}s.

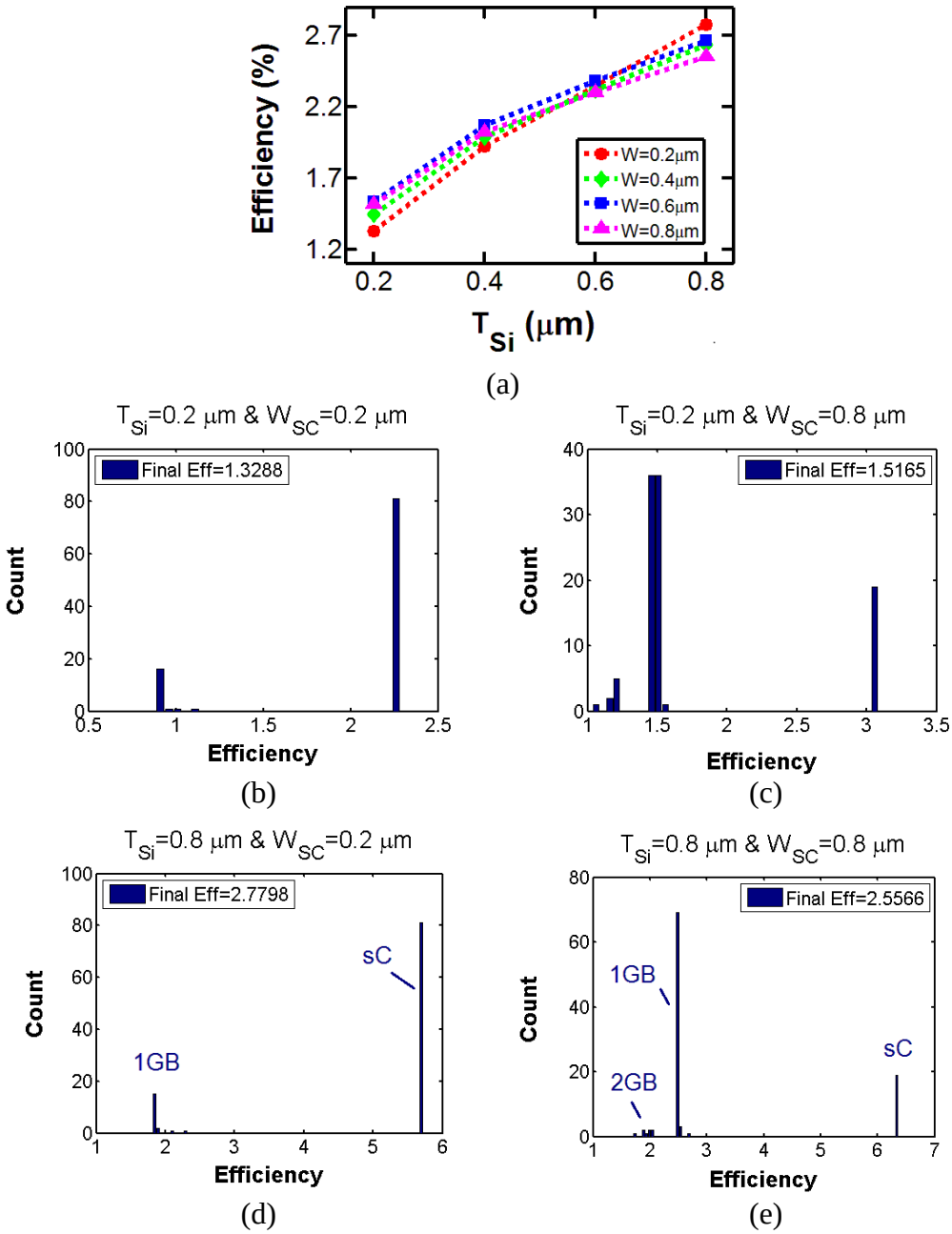


Fig. 3.19 Efficiency of a 1 cm^2 solar cell (a) and efficiency distributions for its unit cells (b-e) for different W_{SC}s and T_{Si}s [N_T=5.10^{18} cm^{-3} , average GrS=1μm]

A second observation that can be drawn from Fig. 3.19 is that reducing W_{SC} reduces the possibility of having a GB in a unit cell to less than 20% when W_{SC}=0.2 µm and average GrS=1 µm. Yet, the final efficiency of the 1 cm^2 cell is limited by the worst performing unit cells since the current density of the worst performing cell is degraded in an exponential fashion as shown in Fig. 3.20.

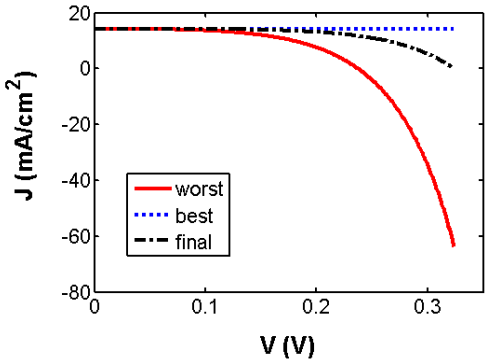


Fig. 3.20 J-V curves under illumination for best and worst unit cells and the final 1 cm^2 cell. [W_{SC}=0.2 µm, T_{Si}=0.8 µm, average GrS=1 µm]

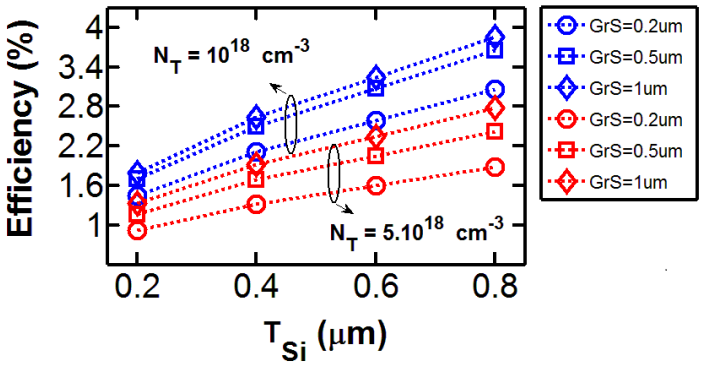


Fig. 3.21 Impact of GrS and N_Ts on the efficiency of the proposed 1 cm^2 solar cell. [W_{SC}=0.2 µm]

On the other hand, the impact of average GrS on the efficiency of a 1 cm^2 cell with a fixed W_{SC} (0.2 µm) and different N_Ts can be observed in Fig. 3.21. When the results in Fig. 3.21 are compared to those in Fig. 3.17, the efficiency values for devices processed with an average GrS of 0.2 µm are found to be similar to the polycrystalline results in

Fig. 3.17. The efficiencies in general improve with increasing the GrS especially for thicker samples. Yet, the performances of these polycrystalline cells are found to be far from the single-crystalline results in Fig. 3.17, which can be explained by the previous observation done on Fig. 3.20.

3.4.4. Effects of Process Parameters on the Power Conditioning Circuit

Due to the low output voltage of a single solar cell, it is required to interface the cell with a power conditioning circuit so that the output voltage can be increased to the requirements of the system. As shown in Fig. 3.1, the solar cell is interfaced with a power conditioning unit that is composed of a DC/DC power converter and a control unit. The power converter topology for this work is chosen to be a linear charge pump [99] illustrated in Fig. 3.22 [98]. Unlike its inductive alternatives (i.e. boost or buck converters), the charge pumps are more cost-effective since they do not employ inductors that take up large space on the chip.

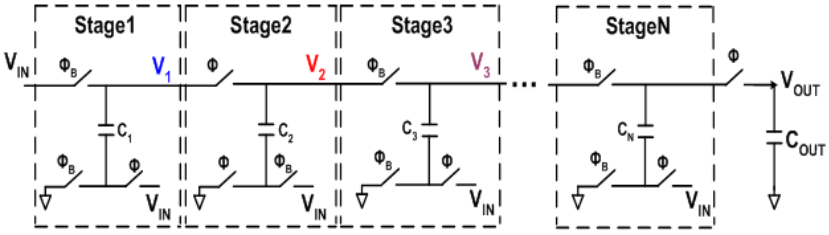


Fig. 3.22 N-stage linear charge pump with gate control [98]. Copyright © by IEEE [16]

The linear charge pump illustrated in Fig. 3.22 is composed of N stages, which are synchronized by two non-overlapping clocks (Φ and Φ_B). When Φ_B is high, C_1 is charged to V_{IN} and this charge is transferred to the next stage when Φ is high. For an ideal system V_1 is boosted to a voltage of $2V_{IN}$. For V_2 this voltage would be $3V_{IN}$ and therefore N^{th} stage's output voltage would be $(N+1)V_{IN}$. Given that the equivalent resistance of a switched capacitor is:

$$R_{EQ} = \frac{V}{I} = \frac{V}{Q/t} = \frac{V}{CVf_{SW}} = \frac{1}{Cf_{SW}} \tag{3.8}$$

The output current of the N-stage linear charge pump is:

$$I_{OUT} = \frac{f_{SW} C}{N}[(N+1)V_{in} - V_{out}] \tag{3.9}$$

where f_{SW} is the switching frequency of the switches. On the other hand, the input current for an ideal charge pump can be stated as:

$$I_{IN} = (N+1)I_{OUT} \tag{3.10}$$

Note that the input of the power converter is also the output of the solar cell. During the day or throughout the year, the solar irradiance changes significantly. Thus, the operating point that a solar cell should be biased at (to maximize the power delivered to the load) changes as well. The control unit regulates the operating point by changing the f_{SW} and therefore I_{IN} (and the input resistance) of the power converter. There are various methods to determine this maximum operating point for a solar cell. From those, VCO [100] or hill-climbing [101] based methods are preferred because of their accuracy and low power consumption.

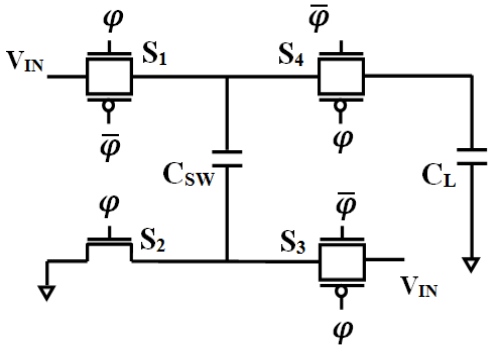


Fig. 3.23 Single stage charge pump topology

As mentioned before, the aim of this study is to be able to power a system similar to the TELOS wireless sensor node [95], which requires 2.4 V as its supply voltage. As the first step of the analysis, the performance of TFTs designed in Section 3.4.2 are investigated in a single stage charge pump as in Fig. 3.23. The setup is prepared with ideal non-overlapping clocks and input voltage source in Cadence environment. The switching capacitance (C_{SW}) is chosen to be 500pF while the output load capacitance (C_L) is 1µF. Since the output voltage is 2.4V and the number of stages is 1, the input voltage is

required to be higher than 1.2V so that it can sustain 2.4V at the output capacitance. Therefore the input voltage is set to 1.3V and the f_{SW}s between 1 to 40 MHz are investigated.

As it can be observed from Fig. 3.24, the performance of the power conditioning unit is affected by the process parameters and the transistor width (W_{TFT}) significantly. The black dash-dotted line indicates the expected performance of a charge pump with an ideal switch for which the I_{OUT} is determined by the equivalent resistance of the switching capacitance as in Eq. (3.9). Yet, as the frequency increases, R_{EQ} decrease and after a critical frequency (f_c) the on-resistances of the TFT switches dominate the output resistance of the power converter. This high frequency performance is referred as the fast switching limit (FSL) in the literature [102]. In this work, the f_c values are determined as the frequency for which I_{OUT} deviates from the ideal performance by 10%. Given this description, the polycrystalline TFT with $N_T = 5.10^{18}$ cm^{-3} and W_{TFT}=0.5 mm in Fig. 3.24 has an f_c of 1 MHz, whereas f_c moves to 4.6 MHz for W_{TFT}=5 mm. On the other hand, the f_c for the TFT with $N_T = 10^{18}$ cm^{-3} is at 8.9 MHz for W_{TFT}=0.5 mm, which is very close to the f_c for the single-crystalline TFT at 9.6 MHz.

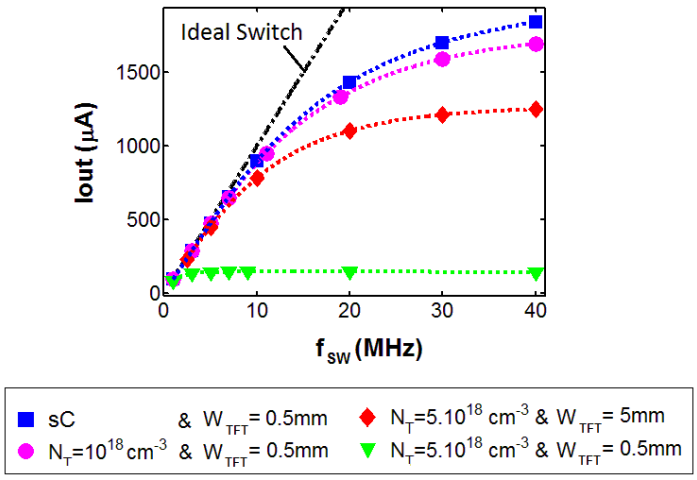


Fig. 3.24 Output of a single stage linear charge pump for different TFT models

These results give a practical insight to the design of the power converter. First of all, the maximum f_{SW} of the circuit employing TFTs with $N_T = 5.10^{18}$ cm^{-3} is going to be

limited. Solar cells with high output currents would require a higher range of f_{SW}s. Therefore, designing with this TFT model would be a challenge. One can increase C_{SW} size to reduce the frequency range of the operation at the expense of the area. Another solution would be to increase W_{TFT} to reduce the on-resistance of the transistor but it should be remembered that the larger the transistor, the larger the power required to drive them would be and the circuit might have problems like clock feedthrough [103]. Therefore, there would be a limit to improvements in performance using this approach. Note that the results in Fig. 3.24 are taken for ideal clocks and the switching power loss is not taken into account.

The second insight that can be drawn from Fig. 3.24 is the improvement in the performance of the TFT with GB once the N_T is reduced. The performance of the N_T $=10^{18}$ cm^{-3} TFT is found to be very similar to that of single-crystalline case similar to what is observed in the I-V curves of the TFTs in Fig. 3.15.

3.4.5. Effects of Process Parameters on the Energy Scavenging System

3.4.5.1. System Optimization

Once the performance of the power converter is characterized, the solar cell SPICE model is introduced at the input of the converter instead of the ideal voltage source and an inverter chain buffer is designed to drive the transistors' gates as in Fig. 3.25. In order to minimize the switching loss, the number of stages in the power converter is limited to 1 and the rest of the simulations are carried out with this setup in Cadence environment. Previously in [104] a voltage controlled oscillator (VCO) based control unit was proposed for a similar system. Since the power consumption of the VCO is found to be small compared to the switching loss at the gate driver, the VCO is omitted in this work. Thus, f_{SW} is provided by an ideal voltage source to the input of the gate driver. Finally, a capacitor is utilized as the energy buffer and the voltage supply of the gate driver is provided from the V_{OUT} on this capacitor. Hence, the net I_{OUT} values to be reported in this subsection are less than what is originally harvested from the solar cell.

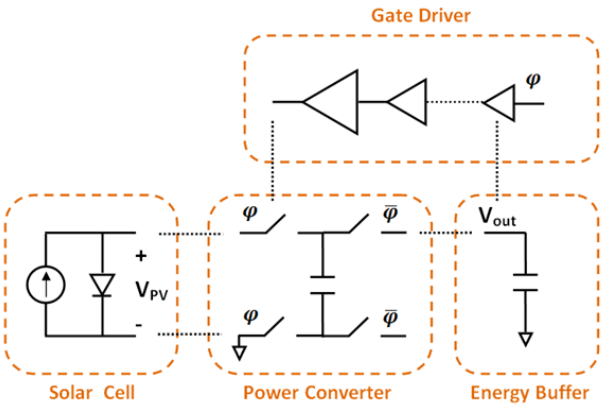


Fig. 3.25 Schematic of the energy scavenging system

The system illustrated in Fig. 3.25 is designed and optimized using the method in Fig. 3.26 to provide predetermined power and area requirements. Three processes with the parameter sets in Table 3.8 are considered for the rest of this work. These cases are named as the "Best", "Average" and "Worst" processes due to their performances. The results obtained for these processes are compared to show how much the system performance is affected by the change in process conditions.

Taking an end-to-end approach, the design process in Fig. 3.25 is started from TFT design. Initially, the V_{TH} required to satisfy the system requirements is determined and then the device is modeled using the method in Section 3.4.2. This step is followed by the solar cell design as it is described in Section 3.4.3. To increase the output voltage of the solar cell, the 1 cm^2 solar cell is divided into M regions and these regions are connected in series. The optimum number of M is investigated by monitoring the output power of the system (P_{OUT}) for various M values as the W_{TFT} and f_{SW} is optimized for each M value. If the system requirements cannot be met, the framework provides several options to enhance the system performance. One can make improvements in the device level and redesign TFT or solar cell for better performance. As another option, one can focus on the circuit side and optimize the number of stages in the power converter as well.

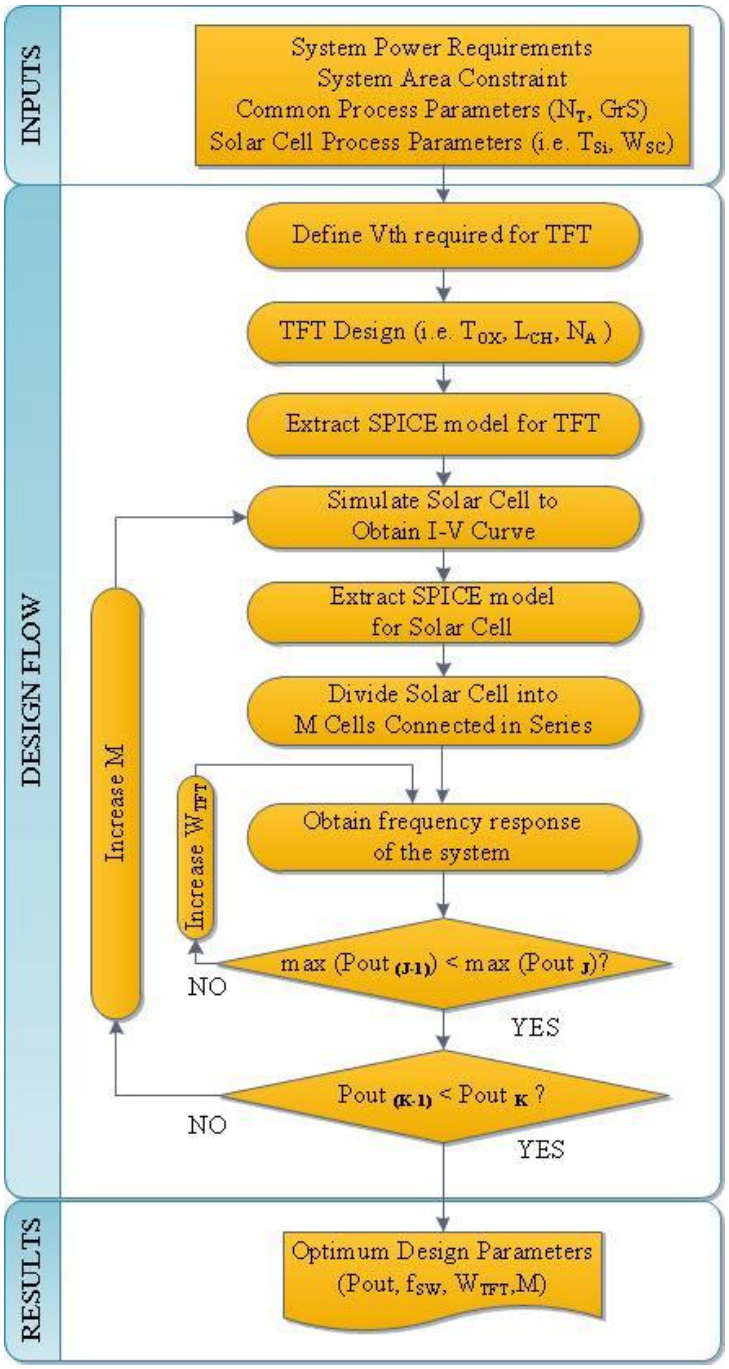


Fig. 3.26 Micro-scale energy scavenging system design flow

Table 3.8 Processes used to determine the impact of process parameters on the performance of the micro-scale energy scavenging system.

Trap density (N_T), average grain size (GrS) of the process, solar cell Si thickness (T_{Si}) and width of the solar cell (W_{SC})

Process Name	**N_T (cm^{-3})**	**GrS (µm)**	**T_{Si} (µm)**	**W_{SC} (µm)**
Worst	5.10^{18}	0.2	0.2	0.2
Average	5.10^{18}	1	0.8	0.2
Best	10^{18}	1	0.8	0.2

As it is discussed in the previous section, the performance of the power converter circuit employing the TFT model with $N_T = 5.10^{18}$ cm^{-3} improves with W_{TFT}. Yet, once the transistors are driven by a buffer employing the same technology, the switching loss comes into picture and an optimum W_{TFT} needs to be determined for optimum system performance.

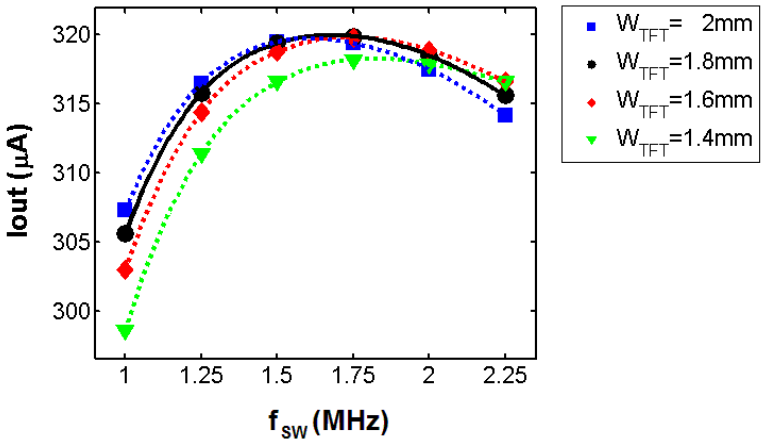


Fig. 3.27 System net output current for different W_{TFT}s fabricated with the "Worst" process. [M=7]

Fig. 3.27 indicates the change in the system performance with respect to W_{TFT} for the "Worst" process parameters. From the results it can be observed that the on-resistance of the W_{TFT}=1.4 mm transistor limits the current driving capability of the transistor. On the

other hand, even though the W_{TFT} =2 mm device can provide more current at low frequencies, the switching loss in the buffer limits the system I_{OUT} at high frequencies due to the dynamic power consumption relation ($P_{SW}=CV_{DD}^2f$). Therefore, the maximum I_{OUT} for this optimization process (I_{MAX}) is obtained for W_{TFT} =1.8 mm and f_{SW} = 1.75MHz respectively for a 1 cm^2 solar cell with M=7.

To determine the optimum M for all processes, the W_{TFT} optimization procedure is repeated for various M values for systems to be fabricated with the "Best", "Average" and "Worst" processes. As it can be observed from Fig. 3.28, each cell requires a minimum M value to provide a non-zero I_{OUT}. For M values smaller than the indicated starting values, the output voltage of the solar cell is not enough to maintain the system V_{OUT}=2.4 V with a single stage power converter. That is why the "Worst" solar cell requires higher Ms. To put into perspective, the V_{OC} of the "Best" and "Worst" processed 1 cm^2 solar cells with M=1 are 0.413V and 0.267V consecutively.

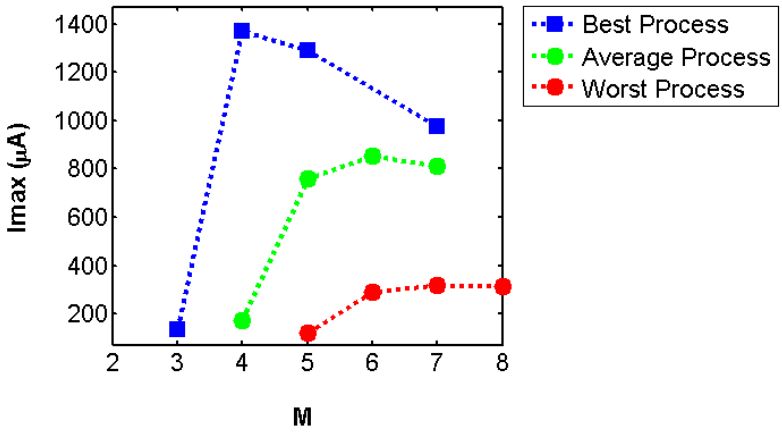


Fig. 3.28 Best possible output current (I_{MAX}) of the energy scavenging system with respect to M for different processes

As the second observation from Fig. 3.28, optimum M values for "Best", "Average" and "Worst" processes are found to be 4, 6 and 7, whereas the power conversion efficiencies of the system for each case are determined to be 89%, 86% and 78% consecutively. For array configurations with small M values, V_{OC} would be small but the I_{OUT} would be high. Hence, higher f_{SW}s are required to obtain the maximum available

output power (see Eq. (3.9) and Eq.(3.10)). Yet, since P_{SW} also increases with frequency, a lower f_{SW} might provide more system I_{OUT}. Besides P_{SW}, the required f_{SW} might be higher than the f_c which would also reduce the I_{OUT}. Using a lower f_{SW} means I_{IN} of the power converter would be lower. Thus, the optimum operating point of the solar cell when it is connected to the power conditioning unit (V_{SYS}, I_{SYS}) would be different than the maximum power point of the solar cell (V_M, I_M). As for array configurations with larger M values, V_M increases as I_M decreases. On the other hand, the on-resistances of the non-ideal switches are found to increase with V_{PV} due to lower overdrive voltages and asymmetric performance of the nTFT and pTFT (see Table 3.6). Hence, I_{OUT} and P_{OUT} reduces.

3.4.5.2. Case Study 1: Increasing the GrS

In Fig. 3.11 and Fig. 3.12 it is shown that the possibility of having a GB within the TFT for processes is reduced with larger GrSs. So if one can improve the GrS, it would be possible to improve the system's performance. Although increasing GrS would also improve the performance of the solar cell, it is assumed to be small for the "Worst" process with T_{Si}=0.2 µm (see Fig. 3.21). Hence, the solar cell model used to generate the following results is kept the same for this case study. The following analysis indicates the contribution of the improvement in the TFT performance to the overall system performance.

For the "Worst" process, the TFT model has $N_T = 5.10^{18}$ cm^{-3} and an average GrS of 0.2 µm (see Table 3.8). As it was demonstrated previously in Fig. 3.27, I_{OUT} of the "Worst" process is maximum when W_{TFT}=1.8 mm and f_{SW}=1.75 MHz (also shown with red squares in Fig. 3.29). If the GrS is improved, the TFTs would have a higher probability of being single-crystalline. Hence, the change in the system performance is simulated by changing the TFT model from polycrystalline to single-crystalline while keeping W_{TFT} fixed.

Initially, the gate driver (and therefore the switching loss) is kept out of the analysis and ideal clocks are used to drive the power converter. The results of this setup illustrated in Fig. 3.29 indicate that I_{OUT} can be improved marginally by 6% (20 µA) if the TFT

model is switched from polycrystalline to single-crystalline. In the next step, the gate driver is included in the design and the change in system performance is monitored. At this point, two comparisons can be made to determine how much improvement can be obtained by increasing the GrS: (a) iso-area and (b) iso-performance. For the iso-area comparison, W_{TFT} of single-crystalline TFT is kept the same with the optimum value for polycrystalline W_{TFT} (1.8 mm) and the blue star curve in Fig. 3.29 is obtained. As it can be seen from this curve, at low frequencies I_{OUT} of the system is much higher than polycrystalline TFTs can provide. Yet, as the frequency goes up, the switching loss in the gate driver dominates due to the higher on-current of the single-crystalline transistors and the system's net I_{OUT} reduces. The improvement in this iso-area case is limited to 6µA but the real advantage of the single-crystalline TFT model becomes visible in the iso-performance comparison. For the iso-performance comparison, the single-crystalline TFT driven by ideal clocks is scaled down to W_{TFT} = 90 µm that would match the I_{OUT} of the polycrystalline TFT with W_{TFT} = 1.8mm. Once the gate drivers are included back into the analysis, the results shown with the black circle curve in Fig. 3.29 are obtained. The results indicate an 18 µA increase in I_{OUT} and 6% increase in P_{OUT} due to reduced switching loss, in addition to the 20 times reduction in the circuit area.

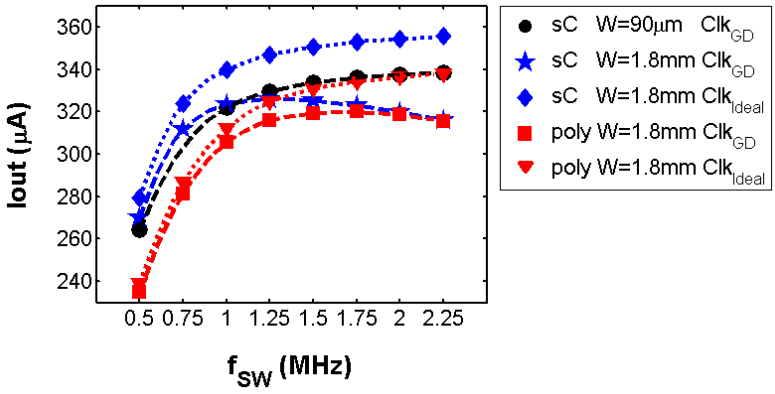


Fig. 3.29 System performance improvement due to increase in the GrS and change in the TFT model from polycrystalline (poly) to single-crystalline (sC) [Clock is provided from a gate driver (Clk_{GD}) or an ideal voltage source (Clk_{Ideal})]

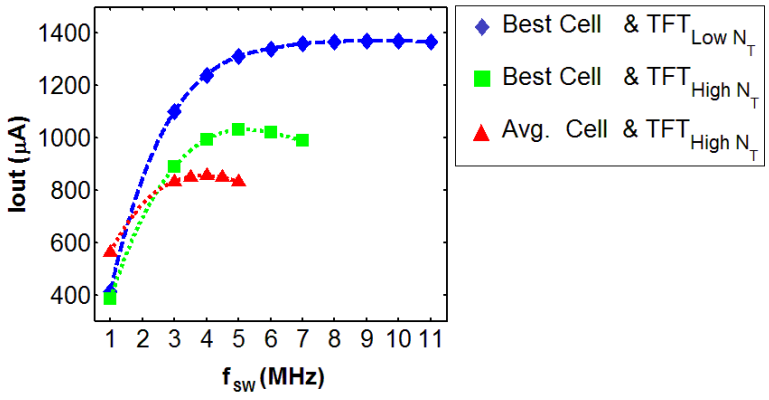


Fig. 3.30 Improvement in system performance due to the increase in N_T of the "Average" process

$TFT_{Low\ NT}$: TFTs with $N_T = 10^{18}\ cm^{-3}$, $TFT_{High\ NT}$: TFTs with $N_T = 5.10^{18}\ cm^{-3}$

3.4.5.3. Case Study 2: Decreasing the N_T

If one was to improve the N_T value of the process, she would move from the "Average" process to the "Best" process. In that case there would be an improvement in the solar cell performance along with the TFT performance. The maximum available output power of the solar cells would improve by 1082 µW, whereas the improvement in the energy scavenging system's P_{OUT} would be 1222 µW. To analyze the impact of TFT performance improvement on the system performance, a step by step approach is taken and the results are shown in Fig. 3.30. Initially, the system is designed with the "Average" process that is to say both solar cell and the TFT are modeled with parameters from Table 3.8 (red triangles in Fig. 3.30). Afterwards, the solar cell fabricated with the "Best" process is interfaced with peripheral circuitry implemented with high N_T TFTs ($N_T = 5.10^{18}\ cm^{-3}$). The results illustrated with green squares in Fig. 3.30, indicate I_{OUT} improves by 148 µA and P_{OUT} improves by 355µW by just changing the solar cell process. On the other hand, in real life both solar cell and the TFT should be fabricated with the same process. Therefore, the N_T used for TFTs should be for the "Best" process ($N_T = 10^{18}\ cm^{-3}$) and the system I_{OUT} trend should look like the blue diamond curve in Fig. 3.30. In this setup, the system P_{OUT} improves by 867 µW due to the improvement of the N_T of the TFT process. Given this breakdown of improvements in the system

performance, one can conclude that the improvement in proposed solar cell's performance is significant, yet TFT performance limits the amount of harvested power.

3.4.6. Looking Across Design Levels

Throughout this chapter, the feasibility of an integrated LTPS micro-scale energy harvesting system is investigated using an end-to-end modeling approach. The design of the system is started from device level and taken up to the system level. At the device level, poly-Si TFTs and solar cells are studied in detail. The effect of GB properties and locations are investigated along with the effect of GrS distribution of the process on the proposed TFT's and solar cell's performances. Solar cells are found to be more sensitive to the presence of a GB. As for TFTs, it is shown that GrSs larger than the L_{CH} are required to alleviate the variation problem due to narrow channel. The devices are designed keeping the system requirements in mind, whereas at the circuit level the designs are made to accommodate the shortcomings of the devices. As an example, the TFT is designed to have a V_{TH} lower than 1.5 V to satisfy the 2.4V supply voltage requirement of the system and a single stage power converter is used to minimize the switching loss due to the large gate capacitances of wide TFTs. At the system level, it is shown that the optimum operating point of a solar cell can change when it is connected to the power conditioning circuitry due to the loss mechanisms within the circuitry. Finally, the effects of process parameters on the system performance are evaluated. For a process with high N_T ("Worst" process), increasing the average GrS is found to reduce the circuit area by 20 times. On the other hand, if the N_T is decreased for a specific process (e.g. moving from "Average" process to "Best" process) the possible improvement in system performance is found to be limited by the TFT performance. Overall, the proposed simulation framework is proved to be a valuable tool to design, debug and improve systems including but not limited to an LTPS micro-scale energy scavenging system.

4. SUMMARY

The research efforts explained in this thesis have focused on two main topics. As the first topic discussed in Section 2, the effects of the deposition conditions on the performance of chalcogenide solar cells are investigated. Within this context, two polycrystalline materials, namely CIGS and CdTe have been studied. For CIGS, the effects of the Na on the cell performance are looked into. From the various hypothesizes in literature, it is shown that the passivation of the GBs have the highest impact on the efficiency of the small-scale solar cells [34]. For CdTe, the effect of deposition pressure on the efficiency of a lab-scale and a module-scale solar cell are investigated using the proposed end-to-end model. During this study, statistical analysis and compact modeling methods are employed to show that the variation observed for the small-scale solar cells are averaged out at larger-scales [53]. It is also shown that a possible improvement in a lab-scale cell's performance is not guaranteed to improve the module performance proportionally due to the parasitic resistances [58].

The second research topic discussed in Section 3 is aimed for low cost and low power energy scavenging systems which would employ polycrystalline Si solar cells as the energy scavenging unit and polycrystalline Si TFTs to implement functionalities for power conditioning (power converter, MPPT) and application (sensors, RF transceivers) units. To achieve this goal, a polycrystalline Si TFT model is proposed for improved analog performance [83] [84] along with a polycrystalline Si solar cell that is compatible with TFT process [91]. Finally, an LTPS micro-scale energy harvesting system is put together and the effects of material parameters are investigated on device, circuit and system level performance. The results indicate the system operating conditions are heavily affected by the process parameters and loss mechanisms at device and circuit levels.

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VITA

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Elif Selin Mungan received her B.S. degree in electronics engineering from Sabanci University, Istanbul, Turkey in 2008 and her M.S. and Ph.D. degree in electrical and computer engineering from Purdue University, West Lafayette, IN in 2010.

Her current research interests are silicon and non-silicon device modeling for low cost - low power flexible electronics applications such as TFTs and solar cells from the device/circuit co-design point of view.

Mrs. Mungan was the recipient of Sakip Sabanci Encouragement Scholarship for her academic excellence from 2005 to 2008 and the IEEE MTT Society Undergraduate Scholarship for her thesis work in 2008.

PUBLICATIONS

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[1] E. S. Mungan, Y. Wang, S. Dongaonkar, D. R. Ely, R. E. García, M. A. Alam, "From Process to Modules: End-to-End Modeling of CSS-Deposited CdTe Solar Cells," , Journal of Photovoltaics (JPV), vol. 4, iss. 3, pp. 954-961, 2014.

[2] E.S. Mungan, S. Dongaonkar and M. A. Alam, "*Bridging the Gap: Modeling the Variation due to Grain Size Distribution in CdTe Solar Cells*," accepted to IEEE Photovoltaic Specialists Conference (PVSC) 2013.

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[5] E.S. Mungan and K. Roy, "*2D Modeling and Optimization of Excimer Laser Annealed Thin Film Polysilicon Solar Cells*" accepted for IEEE Photovoltaic Specialists Conference (PVSC)**,** 2011.

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