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Towards Single-Chip Nano-Systems

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TOWARDS SINGLE-CHIP NANO-SYSTEMS

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This dissertation is gratefully dedicated to my beloved wife and 2 boys for their patience, and my parents, who raised me and taught me to never stop trying to reach for a higher goal.

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ABSTRACT

Pajouhi, Hossein. Ph.D., Purdue University, December 2016. Towards Single-Chip Nano-Systems. Professor: Saeed Mohammadi.

Important scientific discoveries are being propelled by the advent of nano-scale sensors that capture weak signals from their environment and pass them to complex instrumentation interface circuits for signal detection and processing. The highlight of this research is to investigate fabrication technologies to integrate such precision equipment with nano-sensors on a single complementary metal oxide semiconductor (CMOS) chip. In this context, several demonstration vehicles are proposed. First, an integration technology suitable for a fully integrated flexible microelectrode array has been proposed. A microelectrode array containing a single temperature sensor has been characterized and the versatility under dry/wet, and relaxed/strained conditions has been verified. On-chip instrumentation amplifier has been utilized to improve the temperature sensitivity of the device. While the flexibility of the array has been confirmed by laminating it on a fixed single cell, future experiments are necessary to confirm application of this device for live cell and tissue measurements. The proposed array can potentially attach itself to the pulsating surface of a single living cell or a network of cells to detect their vital signs.

Next, a fabrication process has been developed to integrate arrays of electron field emitters within a CMOS SOI chip. The proposed integration technology enables engineered electrodes with uniform tip shapes and highly controlled electrode distances.

Field emission experiments from both vertical and horizontal nano-tips within a CMOS chip is demosntrated.

A fabrication approach based on engineering the CMOS substrate has also been developed to improve the characteristics of electronic components and circuits. By transferring or removing the silicon substrate of a CMOS SOI chip, the loss of Si substrate has been eliminated, leading to improved performance of two circuit demonstration vehicles. In the first example, a high performance wideband RF power amplifier (PA) is presented with the substrate transferred to Aluminum Nitride (AlN). In the second case, improved performance of an integrated rectifier and antenna (Rectenna) without silicon substrate is presented.

Finally, post-processing techniques to integrate nano-fluidic channels and nanoelectromechanical systems (NEMS) on a CMOS chip have been developed. For applications in integrated nano-fluidic channels, post-processing recipes to fabricate both horizontal and vertical channels have been proposed, which may facilitate future single biomolecule detection and characterization. For integrated NEMS, different nanobeams have been fabricated in a standard CMOS SOI technology, with a focus on the development of different suspension methods. Proposed techniques to fabricate NEMS devices may find applications in precision mass sensing, gyroscopes and electromechanical filters.

Nano-sensors integrated with CMOS offer a pathway to overcome several challenges, including low detection bandwidth, low signal-to-noise ratios, and low yield and reproducibility. Solving these challenges will propel integrated nano-systems into the commercial market.

1. INTRODUCTION

1.1 Introduction to Nano-Sensors and Systems

Nano-sensor is referred to a device, which conveys information from a nano-scale environment and transforms it to the macroscopic world. Various advanced nano-sensors exist in nature. For example, the sense of smell is functionalized by receptors, which enable the detection of nano-scale molecules. Certain fish takes advantage of nano-sensors to detect surrounding microscopic vibrations, and some plants are equipped with miniature light detectors.

Inspired by nature, nano-sensors are being developed rapidly, which has led to a global research effort. Better understanding of nano-scale phenomenon in recent years has offered prospects for a wide range of applications for nano-sensors. Nanoelectromechanical systems (NEMS), based on resonating nano structures, have demonstrated precise environmental monitoring capabilities [1], [2]. By taking advantage of electron field emission from nano-tips, under specific conditions, vacuum gauges have been developed [3]. Nanophotonics and nano-opto-electromechanical systems (NOEMS) have demonstrated applications in optical biosensing [4]. Chemically-modified nanoparticles have significantly improved the performance of gas sensors and ion-selective electrodes [5]. Nano-pore and nano-fluidic technology have enabled the detection and analysis of DNA molecules [6] and three-dimensional nano-pillars have facilitated intracellular electrical recording of single cells [7].

Despite the progress in reserach, nano-sensor technology is still not mature enough for commercialization. Advancement in nano-fabrication techniques is an important aspect that may enhance nano-sensor capabilities and performance.

1.2   Introduction to CMOS Technology

The Complementary Metal Oxide Semiconductor (CMOS) process is the standard way of fabricating transistors. A combination of n-type and p-type transistors, fabricated in complementary metal oxide semiconductor (CMOS) technology, has various applications in implementing digital and analog circuitries as currently being used in microprocessors, memories and many interface systems. For digital applications, CMOS transistors come in a symmetrical pair of n-type and p-type transistors, which helps lower their power consumption. As all devices presented in this thesis are fabricated in a standard CMOS silicon-on-insulator (SOI) platform, a brief overview of CMOS fabrication steps are presented in this section. Although standard CMOS processing includes simultaneous fabrication of pairs of n-type and p-type transistors, here the main steps to fabricate an n-channel transistor are presented, as the complementary p-channel transistor processing follows similar steps.

The process starts with generation and patterning of a thick oxide layer on the surface of p-type silicon (Figures 1.1(b,c)). The oxide layer, namely field oxide, is patterned to define regions in which the transistors are going to be built. In the next step, a high quality oxide layer is formed by means of thermal oxidation and a polysilicon layer is deposited on the entire surface (Figures 1.1(d,e)), which will be used as the gate oxide and gate electrode, respectively. The high resistivity of the polysilicon will be altered by doping it to either \ n-type or p-type in a following step. Next, a selective etching which defines the MOS transistor gate region (Figures 1.1(f,g)) is performed. A high-concentration impurity doping is introduced through ion implantation to dope the poly-Si gate and form the source and drain junctions in a self-aligned process (Figure 1.1(h)).

With the transistor fabrication completed, the back end of process (BEOP) starts, which includes the processing of metallization interconnects, vias and dielectric layers. An insulating layer of SiO_2 covers the surface (Figure 1.1(i)) of the transistors and small openings are etched through the insulating layer to expose source, drain and gate contacts (Figure 1.1(j)). Then, contact windows are filled with vertical interconnect (via) metal

(Figure 1.1k) and patterned to form electrical contacts to the transistor terminals (Figure 1.1(l)). CMOS interconnection layers are normally fabricated as a stack of several layers, on top of the CMOS transistors. Metal paths are isolated from each other by means of intermediate oxide or low-K dielectric layers. Vertical interconnections are formed by etching holes in the corresponding intermediate oxide layers, followed by metal deposition to fill the holes. The process involves sequential metal depositions, pattering and etching, electroplating and chemical-mechanical polishing (CMP). Finally, contact pad metallizations are deposited and a passivation layer is applied to coat the circuit and isolate it from environmental factors such as free ions, humidity and chemical solutions that may affect the performance of the transistor. Adopting the well-established CMOS process for the fabrication of nano-sensors can pave the way to create reliable and reproducible nano-devices and nano-systems.
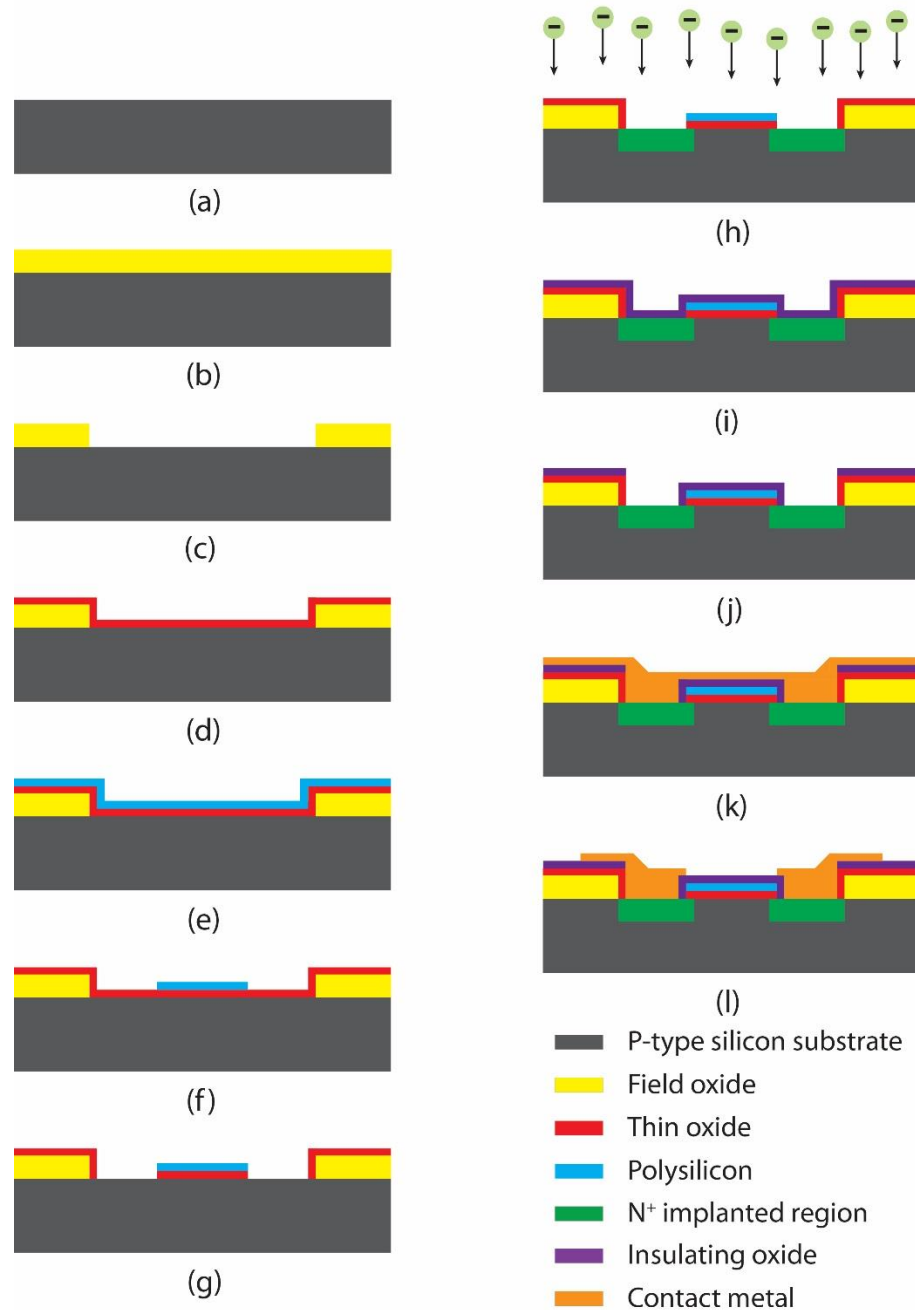
Figure 1.1. Schematic of the main processing steps to fabricate a n-channel MOS transistor on a p-type silicon substrate. (a) P-type silicon substrate. (b) Oxidation of the silicon substrate. (c) Selective etching of the field oxide. (d) High-quality oxide deposition. (e) Polysilicon deposition. (f,g) Selective etching of the thin oxide and polysilicon. (h) Doping the silicon surface. (i) Deposition of the insulating oxide. (j) Selective etching to open contact

windows. (k) Metal evaporation. (l) Patterning and etching of the metal layer to form the contacts.

The possibility of mixing nano-sensors with CMOS circuits, has opened up a new paradigm in designing sensors and electronic circuits and systems. Figure 1.2 demonstrates a simple schematic of the proposed sensor and CMOS integration. Having the sensor on the same chip with the CMOS transistor enables on-chip control over the sensor, as well as data acquisition and data processing [8]. Detected signals at the nano-scale are often weak and can be masked by induced noise and undesired couplings. Figure 1.2 demonstrates a brief overview of how CMOS integration may enhance system performance by reducing parasitic elements of the circuit (parallel capacitor and series resistor). Additionally, improved sensitivity can be achieved by taking advantage of integrated amplifiers. The improvement is due to the fact that the instrumentation noise is significantly reduced (hence the signal-to-noise ratio can be improved) by the availability of on-site amplification at the output of the nano-sensor device.
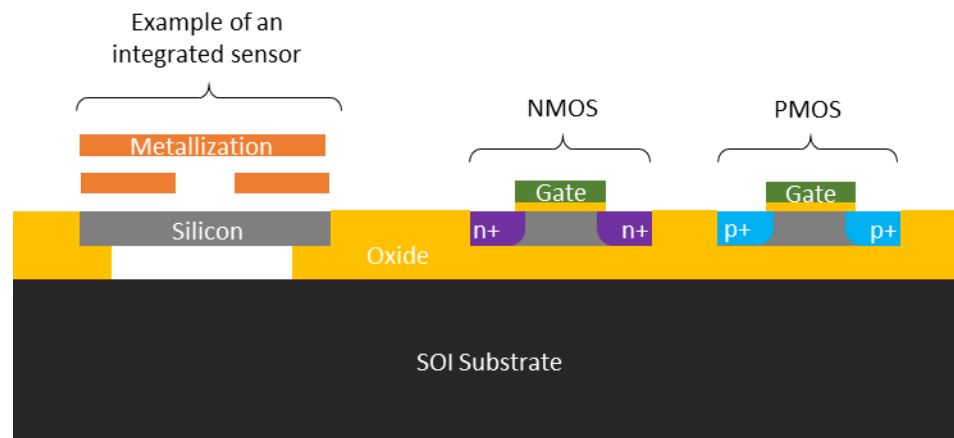
Figure 1.2. Simplified schematic of sensor and CMOS integration

In addition to signal-to-noise ratio improvement, the measurement bandwidth can be significantly increased by reducing the output capacitance of the device and reducing the series resistance of interconnects. Increased measurement bandwidth leads to signal

detection at very high frequencies, a characteristic that is desirable for single biomolecule detection. According to the simplified schematic in Figures 1.3(c,d), the bandwidth is limited by the parasitic capacitance in the detection circuit. In this figure, R_e and C_p represent the output resistance and the detection circuit parasitic capacitance of the nano-sensor, respectively. $1/(R_eC_p)$ roughly determines the bandwidth of the system. CMOS integration significantly lowers the parasitic capacitance (C_p), and hence facilitates high measurement bandwidths.
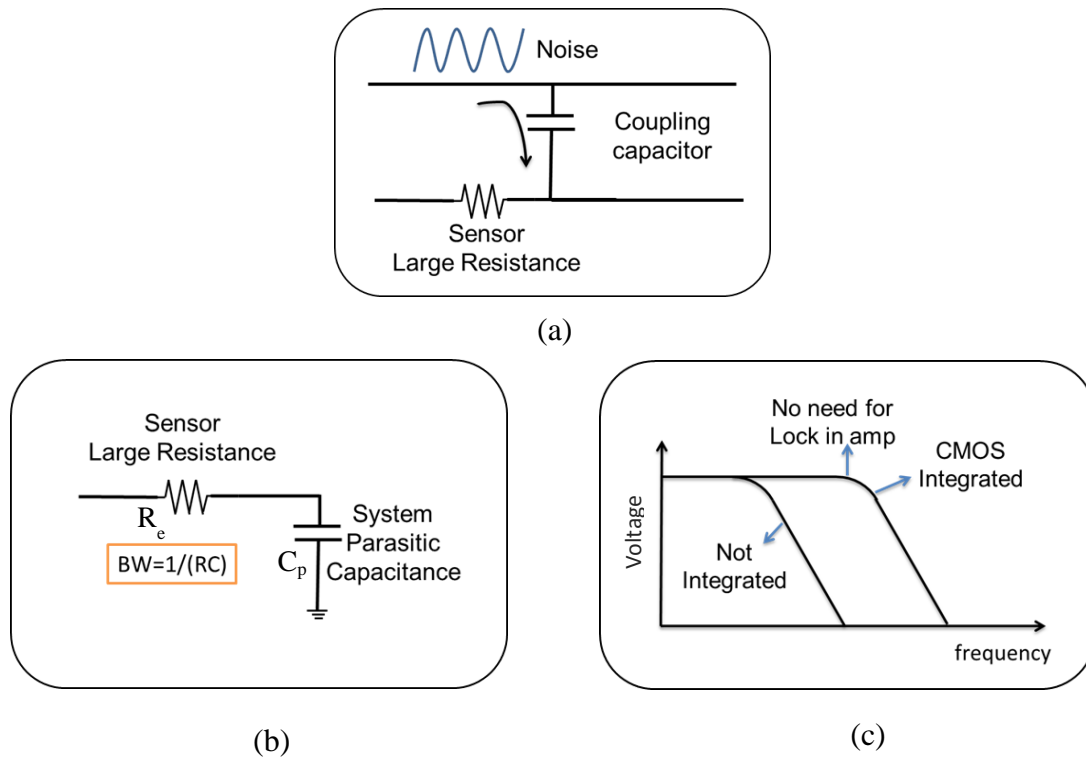
Figure 1.3. Schematic demonstrating how CMOS improves weak signal measurements by (a) reducing undesired couplings and (b,c) by increasing the bandwidth.

Improved nanofabrication techniques have led to many advancements in nano-sensor technology. Despite these improvements, sensor reliability is yet to be enhanced and the production cost is yet to be reduced to make systems based on nano-sensors suitable for

widespread applications. Through the integration of sensor and CMOS, one can exploit the well-developed fabrication technique of CMOS devices for nano-sensors. Moreover, the cost and size of CMOS integrated devices are significantly reduced while their sensitivity and specificity are improved. An already commercialized example of such technology is imaging sensor arrays integrated with electronics. CMOS image sensors improve the image quality via the on-chip amplification and processing of detected signals. Integrated gyroscopes [8] and RF capacitive systems [9] are other examples of such technology. Table 1.1 summarizes the advantages that CMOS integration offers to the sensors.

Table 1.1. Summarizing the advantages of CMOS integration

Advantages from an engineering perspective:	Advantages from a commercialization perspective:
Reduced undesired coupling	Low-cost production
Increased bandwidth	High-volume batch fabrication
No need for external instrumentation	Implemented with high yield based on established technologies
Accurate	
System integration	Compact
Fabrication reproducibility	Mass production in short time frame
Post-processing with no photolithography steps	

1.3   Sensor-CMOS Integration Techniques

Different techniques to fabricate and integrate sensors on a CMOS chip have been previously reported. Basically, a nano-system integrated on a CMOS chip consists of three different parts: (i) Active CMOS transistors; (ii) CMOS metallization which forms interconnect lines and passive inductors and capacitors; (iii) The integrated sensor. All previously reported integration approaches are common in having these three parts, however, the fabrication sequence may vary among these approaches [10].

In each approach, the following concepts may help determining its advantages and disadvantages. First, the process sequence should be developed in a way that the fabrication of each part has minimum impact on the fabrication of the other two parts. For example, high-temperature procedures can only be performed during the initial steps of CMOS transistor fabrication and not during the latter stages of sensor fabrication, as they may influence the performance of CMOS transistors. Secondly, fabrication with a minimum number of lithography steps is desired, as each step of lithography adds cost to the system and may have a negative effect on the production yield. If sensors are being fabricated as post-processed devices, it is ideal not to use lithography for their fabrication all together. Lastly, vertical stacking of the components may help save chip area and lead to more compact systems leading to lower cost [11].

If sensors are defined prior to the fabrication of CMOS transistors, sensor fabrication can include a high-temperature process, such as poly-silicon deposition. The pressure sensor introduced in reference [12] is an example of this procedure. In this work, first the sensor is defined in a trench below the surface of the wafer. Then, the trench is filled with oxide and nitride in order to protect the device in the CMOS transistor fabrication stage. While, this approach integrates sensors and CMOS circuits together, it is not compatible with standard low-cost CMOS fabrication. Alternatively, CMOS transistors may be defined prior to the integrated sensor. The advantage here is that standard CMOS processing can be carried out without any additional consideration related to the sensor fabrication stage. However, the thermal budget of the fabricated CMOS transistors imposes limitations to the thermal budget of the sensor fabrication process. Digital micro mirrors, utilized in overhead projectors, are an example of this approach [8]. For these devices, an oxide layer is deposited on the CMOS circuitry, in order to protect the transistors in the micromachining stage. The device is completed through the deposition and patterning of interconnect metallization at the end.

CMOS transistors and sensors may be fabricated simultaneously. In this approach, the processing is optimized for minimum degradation in both sensors and CMOS transistors. For the pressure sensor explained in reference [13], CMOS layers are used to integrate the sensor on the same level as the transistors. In the above approaches, the

fabrication of CMOS metallization is carried out at the very last step of the processing, after defining the transistors and sensors. On the other hand, an alternative fourth method exploits CMOS metallization towards the fabrication of sensors. In this method, although the sensor is partially defined in the CMOS transistor fabrication step, it is completed after the CMOS metallization step. A post-CMOS processing step is required in order to completely define the sensor. References [14] and [15] are examples of the fourth approach.

1.4 Introduction to CMOS Post-Processing

Post-CMOS processing refers to steps performed after the CMOS process is completed, in order to monolithically integrate the micro/nano structures on the CMOS chip.   The objective of this thesis is to utilize the CMOS metallization for sensor fabrication using post-CMOS processes without adding any lithography. A typical post-processing may include multiple sequences of vertical and lateral etchings. Normally, the process starts with anisotropic plasma etching (vertical etching) of a stack of CMOS dielectric layer. This vertical etching step exposes the buried sacrificial layer on the chip and facilitates the lateral etching for the next step. For the next processing step, a lateral etching method should be chosen, which is suitable for etching the sacrificial layer. This step is optional and is typically used to make a horizontal air trench or fluid channel within the CMOS BEOL layers. In order to prevent the sensor (or pads) from being damaged during post-processing, multiple protection layers may be required. The number of vertical/lateral etchings steps increases by increasing the number of required protective layers.

Limited thermal budget is a major point that should be considered during the post-processing. While the CMOS active components can withstand high temperatures, the resistance of the metal interconnect degrade when exposed to high temperatures. For example, low stress polysilicon needs to be annealed at 900 $^{\circ}$C, which should be precluded from being used in post-processing. Examples of the common processing approaches that can be performed at temperatures below 400 $^{\circ}$C (so can be used as a post-processing step) are reactive ion etching (RIE), Electron beam evaporation, plasma

enhanced chemical vapor deposition (PECVD), atomic layer deposition (ALD), sputtering and electroplating processes.

1.5   Project Description and Thesis Outline

The goal of this research is to come up with fabrication techniques to integrater nano-sensors in a CMOS platform. Fabrication procedures presented here may lead to higher level of nano-sensor integration with analog and digital circuits. Most of the post-processing technologies proposed in this Thesis utilize chips fabricated in a standard 45 nm CMOS SOI technology. The technology offers CMOS transistors and eleven metallization layers on a SOI substrate. The minimum poly-silicon gate size is 45 nm. All metallization layers except for the top layer are formed with Copper. The very top metal layer commonly used for pads is made of Aluminum. The minimum dimension of the lowest metal layer (M1) is 70 nm, and the minimum poly-Silicon width is 40 nm. Several physical design rules impose limitations on different aspects of the nanostructure design. Following these Design Rules, a layout of the device is drawn using Cadence software. The layout of nano-devices along with other circuits and test structures is "taped out" to the foundry for chip fabrication. In-house post-processing steps are then completed in the cleanroom to form the micro/nano structures. Figure 1.4 illustrates the side view schematic of the CMOS layers stack used in this technology.
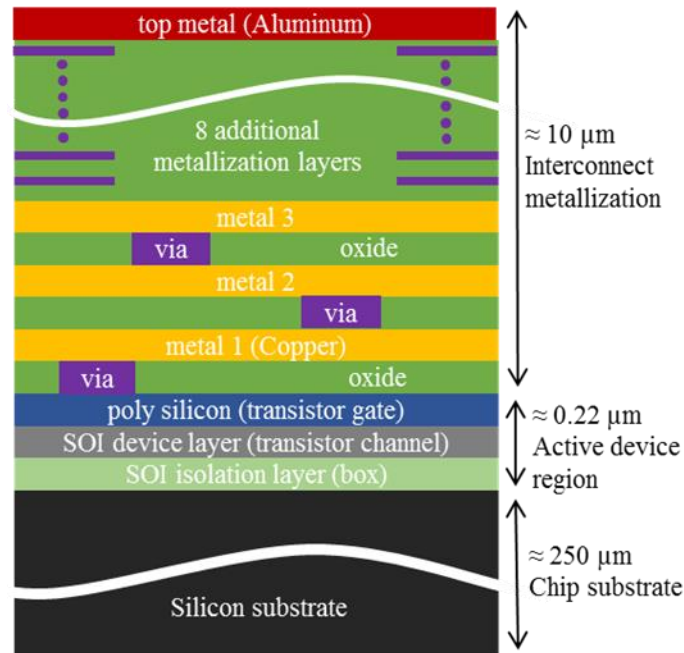
Figure 1.4. Cross-sectional view of the layers in the utilized 45 nm CMOS Silicon-on-Insulator (SOI) technology.

The organization of the rest of this dissertation is as follows. Chapters 2 elaborates on the fabrication and thermal characterization of fully-integrated flexible micro-electrode arrays (MEAs) which can potentially be used for the characterization of single cells and neurons. Chapter 3 presents integrated, vertically and laterally oriented, nano-tips, which operate as electron field emitters. Chapter 4 introduces post-processing approaches for engineered CMOS substrates. Chapter 5 proposes post-processing techniques for applications in integrated nanoelectromechanical systems and fluidic nanochannels. Chapter 6 summarizes the research related to integrating nano-sensors and CMOS devices, with a focus on the fabrication techniques, and its potential for future integrated systems.

2. FLEXIBLE CMOS MICROELECTRODE ARRAYS WITH APPLICATIONS IN SINGLE CELL CHARACTERIZATION

2.1 Introduction

Biological sensing at the micro- and nano-scales facilitated by high performance electrodes leads to a better understanding of single cell behavior [16]. A variety of such electrodes have been developed to record electrical activities of beating cells, using both intracellular [7], [17]–[19] and extracellular [20] techniques. A planar high-density microelectrode array (MEA) is one example of the electrodes utilized in an extracellula

in-vitro measurement for interfacing to neurons [21]. Moreover, nanoscopic probes, such as nano-pillar electrode arrays [19], [22] are extensively used for intracellular action potential measurement of individual neurons [17]. The weak nature of biological signals combined with the three-dimensional moving surfaces of cells and tissues demand tight integration of an array of flexible electrodes with electronic amplifier circuits to enhance the recovery of such signals.

While novel flexible electronic sensors with improved sensitivities have been developed, they still require a number of leads coming out of the sensor array and in some cases require external instrumentation amplifiers for signal recovery. Such designs not only lead to a loss of the overall sensitivity and reduced measurement bandwidth, but also demand complex integration and packaging approaches [23]. At the cellular level, three-dimensional kinked nanowire FETs have been proposed for single-cell action potential recording [7]. The kinked nanowire based designs have achieved high sensitivity at the sensor level, but require external amplifiers with associated path loss and undesired coupling, compromising their overall sensitivity. At the tissue level, three-dimensional flexible circuits on deformable sheets that bend according to the curvatures of tissues, provide interface for in-vivo characterization [24]–[26]. While these techniques have utilized simple integrated electronics, they can benefit from large scale integration in order to reduce the distance among array sensors, further reducing the number of leads coming out of the array (analog multiplexing) and enhancing the detected signals, as achieved by analog and digital signal processing and amplification.

Previously reported flexible electronic circuits are based on either thinned-down Si flakes that can bend at a few millimeter radius to prevent damage [27], or transferred-printed silicon micro-islands [28]–[30], presumably characterized with low yield as device density increases [31]. In this work, an ultra-flexible microprobe array based on CMOS ultrathin membranes is fabricated. The array can be easily laminated on micron-size curved surfaces such as the surface of a single cell, and is equipped with very dense electronics. To demonstrate the functionality of complex electronics on the array, CMOS temperature sensors and instrumentation amplifiers for precision single cell thermometry

are implemented and tested. The operating conditions of CMOS transistors utilized as temperature sensors are optimized to enhance the measurement sensitivity.

Cell temperature is an indicator of cellular processes such as cell division, metabolism and enzyme reaction [32]. For example, precision cell thermometry can identify cancer cells that are characterized with slightly higher temperatures than normal cells [33]. Additionally, the temperature across a single cell is not constant and is slightly elevated around mitochondrion due to their high metabolism. While accurate in-vivo measurement of temperature across a cell is important, understanding the behavior of a cell demands other sensors such as potential and pH sensors to be integrated within the flexible sensing platform. Such a flexible microelectrode array with integrated sensors and electronic amplifiers will become an instrumental tool for understanding the cell behavior without disturbing its environment.

2.2   Motivation

Rethinking the electrodes used in biological sensing is essential to further advance our knowledge of bio-species such as single cells at nano-scale level. Although flexible and stretchable microelectrode arrays for sensing the surface of organs and tissues have been previously reported, none are small enough to operate at the cellular level. The proposed technology to fabricate micro-electrode arrays within a CMOS platform is considered an advancement over the previous reports in that it has the potential to address the demand for sensing very weak biological signals from the three-dimensional moving surfaces of cells. The distance between the cell and the microelectrode array plays a major role in limiting the voltage amplitude captured by the microelectrode [34]. This limitation emphasizes the importance of the microelectrode array being placed as close as possible to the cell. Consequently, closely attaching the microelectrode array to the cell will lead to a more robust signal recording. The technology to fabricate a perforated MEA has been developed to address this limitation by apply negative pressure to assigned openings in the substrate, enhancing the contact between the microelectrode and the cells [34]. Perforated MEA is mostly suitable for tissue slices and not dissociated cultured cells. MEAs based on carbon nanotubes [35], [36], metal nano-pillars [37] and

nano-cavities [38] are among other approaches that enhance the cell/electrode interface and consequently lower the contact impedance.

2.3 Design

A standard 45 nm CMOS Silicon-on-Insulator technology that brings about reliability, reproducibility and large integration capability is utilized in this work. In the first step of this research, the layout of the device (Figure 2.1(e)) was designed in Cadence software. After the chip fabrication, the devices were completed using in-house post CMOS processing techniques. In this design arrays of 4×4 ultrathin CMOS islands interconnected by meandered copper (Cu) metals were transfer-printed to host substrates or cells, bypassing the yield-limiting obstacles of previously reported for transfer-printing of complex circuits [31]. As shown in Figures 2.1(a,b), each island of the array is 19×19 μm^2 with a thickness of about 10 μm (A stack of a 220 nm Silicon-on-Insulator (SOI) layer and a ~10 μm thick interconnection/oxide layer on top). The array is surrounded by four 90×90 μm^2 pads. Each island is interconnected with 12 corrugated copper wires, of which only four are connected to the input/output (I/O) pads. An alternative design with finer (70 nm metal width) and fewer corrugated interconnects (4 wires for each Si island) is implemented as well. The microelectrode array can be scaled to much smaller dimensions, enabling characterization of several test points across the surface of a single cell with a diameter of a few μm.
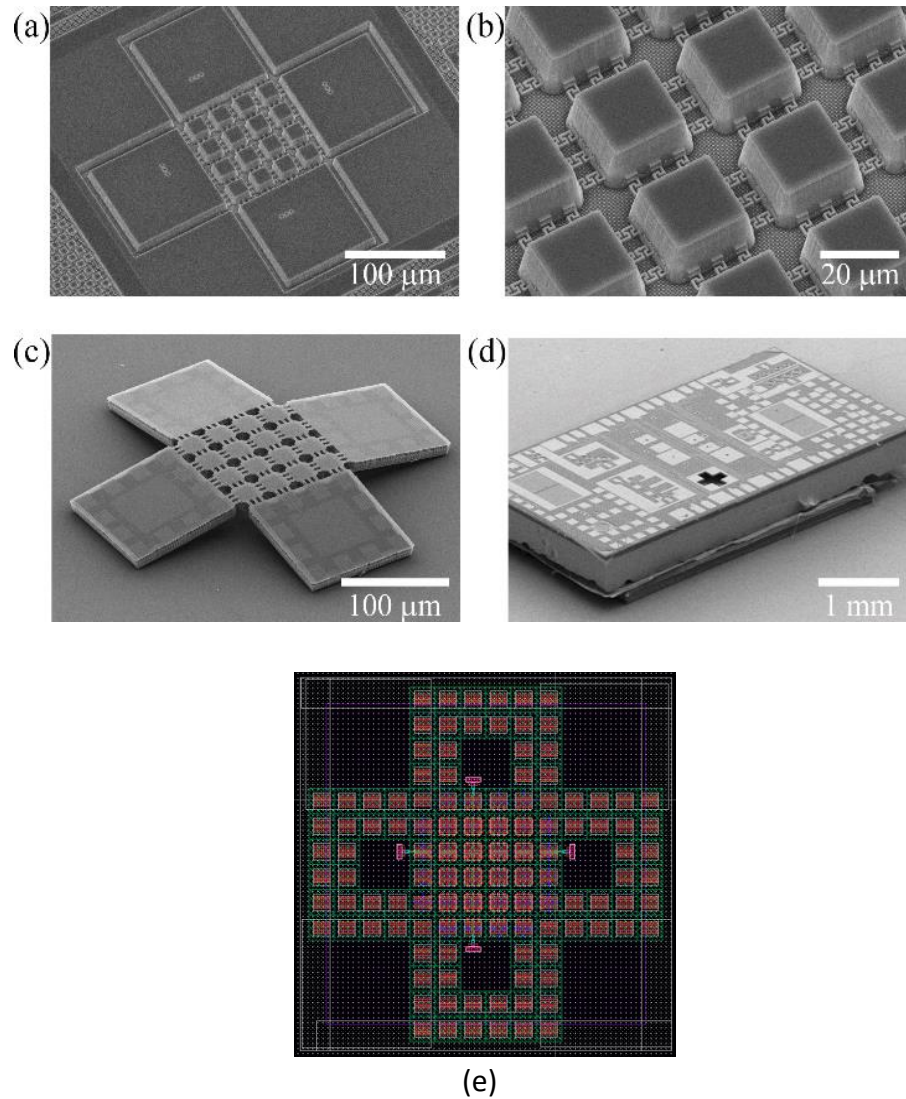
Figure 2.1. SEM images of the microprobe array being etched and released during a post-CMOS processing technology. (a) The microarray structure on a CMOS SOI chip. (b) Microarray islands after the plasma etch and before the release. (c) Released microarray dielet. (d) Chip after the release of the microarray dielet. One can see a small black spot in the chip. That is the empty location of the microelectrode array after the dielet being released. (e) Layout of the device, designed in Cadence software.

High density interconnect is achieved through utilizing a commercial 45 nm CMOS Silicon-on-Insulator technology with eleven layers of metallization. Figure 2.2 illustrates

the schematics for different layers in the utilized CMOS technology. In this particular process, eleven layers of interconnect metallization are available on top of the SOI wafer. The metal layers become thinner as they get closer to the device layer with the closest metal layer with a thickness of only 136 nm. Metallization with different thicknesses are isolated from each other by thin layers of oxide and high-K dielectric, but can be connected by vertical interconnects (vias). With a multitude of interconnection layers inside each island, integration of dense circuits such as amplifiers and signal processing circuits within each island is feasible. The integration of sensor and amplifier enables high signal-to-noise ratios and enhanced sensitivity. Figures 2.2(a,b,c) illustrates the dense interconnects buried inside each island.

2.4   Fabrication

CMOS islands are formed in a post-CMOS processing technology [39], [40] based on a one-step dry isotropic etching without a need for lithography. The top Aluminum metallization layer in the CMOS process serves as a built-in mask to form Si islands inside an Inductively Coupled Plasma (ICP) etcher. Ultrathin (~10 μm thick) CMOS micro-islands are then suspended using a Xenon di-fluoride (XeF_2) gas that etches the silicon substrate underneath the array. The sidewalls are protected with a thin layer of Al_2O_3 formed by atomic layer deposition, which also provides electrical isolation. Parameters such as pressure and gas duty cycle have been optimized to achieve high fabrication yield by taking an infrared (IR) microscope image after each etching cycle. Figure 2.3 summarizes the post-processing steps and provides a cross sectional schematic of the islands and their interconnecting metals. Details of the post-processing recipe are provided in Appendix A.1.

(a)

(b)

(c)
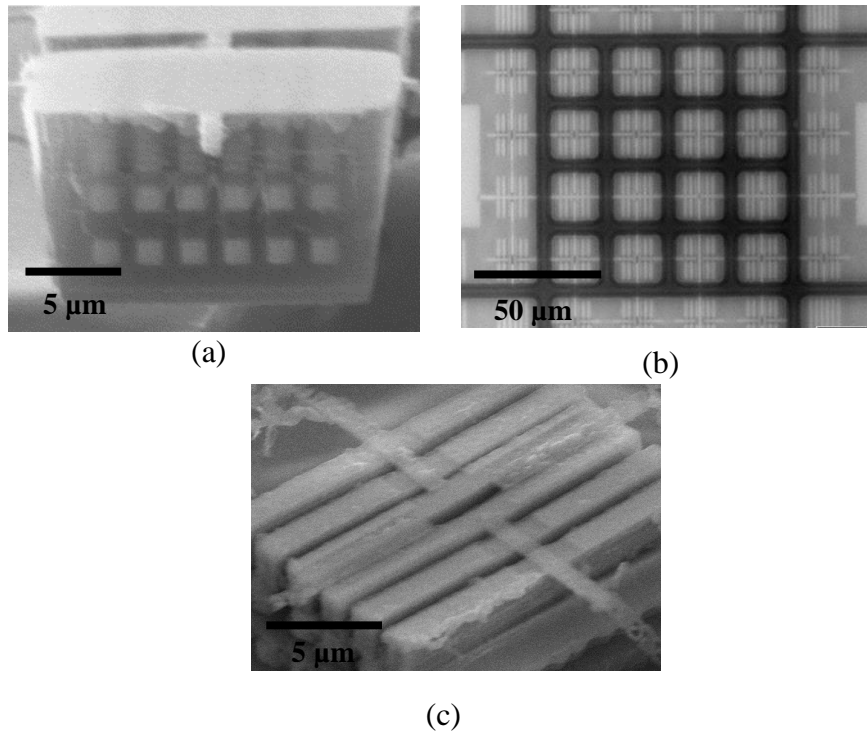
Figure 2.2. Complementary Metal Oxide Semiconductor (CMOS) layers and high density interconnects: (a) SEM micrograph of an island, illustrating several layers of interconnections. The device layer is located at the top of this image. (b) An IR microscope image illustrates dense metal interconnectors within each island. This large capacity of interconnections enables signal amplification and data processing along with the sensors, leading to higher signal-to-noise ratios and more accurate measurements. (c) SEM micrograph shows the dense stack of interconnectors inside each islands. The surrounding oxide was etched using Buffer Oxide Etchant (BOE) in order to take this picture, but the BOE etching is not part of the post-CMOS processing.
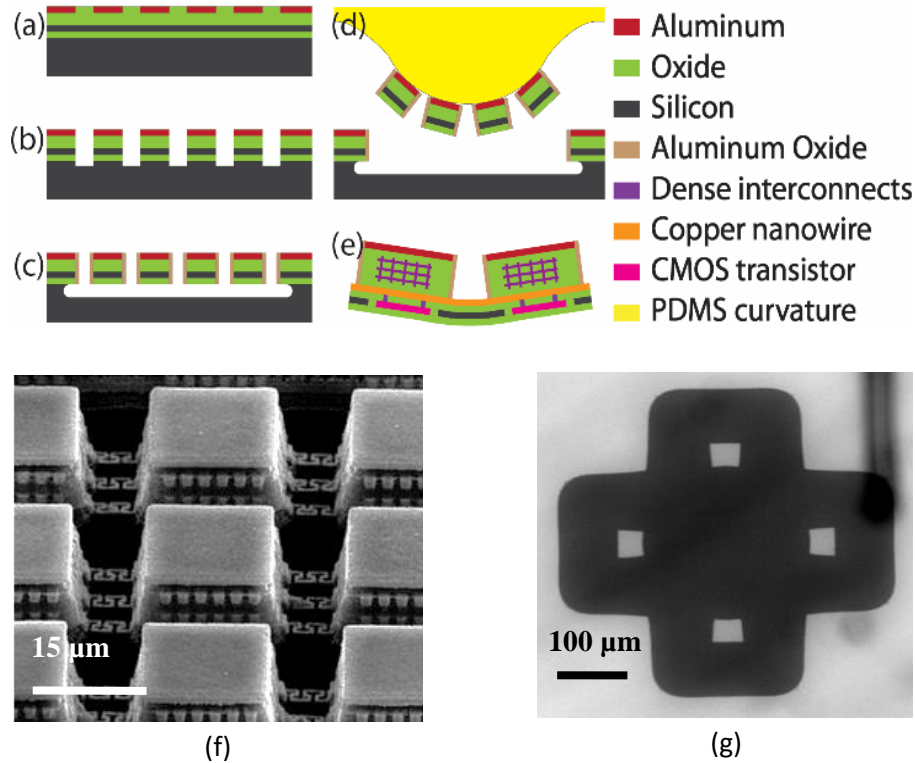
Figure 2.3. Fabrication process flow: (a) CMOS chip after fabrication in the foundry. (b) Anisotropic dry etching using ICP. A combination of CHF_3 and CF_4 gasses, with flow rates of 40 sccm and 10 sccm, respectively, have been used in a Panasonic E620 setup, at 1 Pascal chamber pressure. Radio Frequency (RF) coil and bias powers were set to 700 Watts and 250 Watts, respectively. (c) Aluminum oxide deposition followed by ICP anisotropic etching and XeF_2 isotropic etching. The SOI Oxide layer (buried oxide) served as intrinsic etch-stop to protect the island from the bottom. (d) Transferring the array using PDMS transfer-printing technique. (e) Zoomed-in schematic of two cells of the array and the nanowire interconnects. (f) SEM micrograph of the suspended array, after the XeF2 etching step. (g) An IR microscope image of the array taken from the back side of the chip. Four micropillars (small squares) hold the array suspended in air. The IR microscope image helped in characterizing the fabrication process parameters such as pressure and gas duty cycle.

The two bottom copper layers in the CMOS technology are used to form the meandered interconnects, with widths of 400 nm and thickness of ~800 nm for the two

metal layers and the low-K dielectric layer between them. The top copper layer serves as a mask in the isotropic etching process while the bottom copper layer acts as the conductive media among sensors/circuits and I/O pads. The meandered geometries provide excellent flexibility [41]. On the other hand, thinning down the islands to 10 μm of dielectric/metallization layer and only a 220 nm

(a)

(b

(c)

(d)
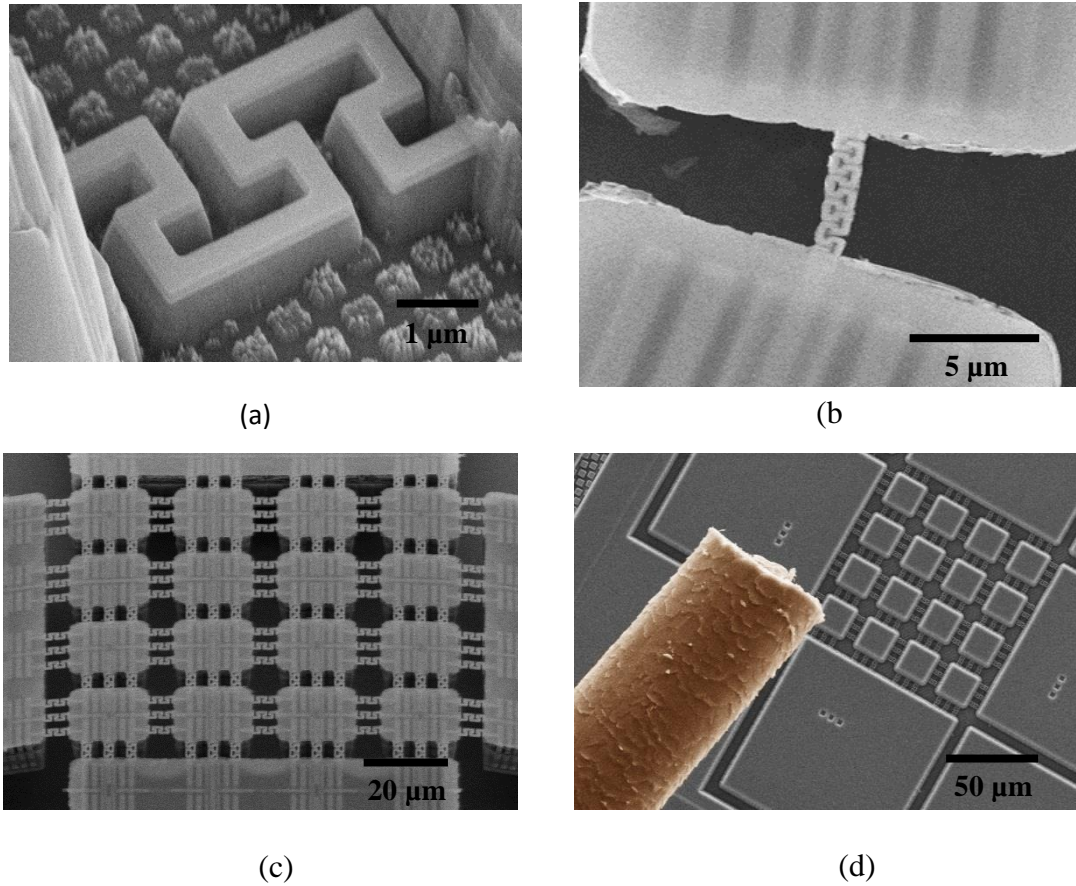
Figure 2.4. (a) An SEM image of a single corrugated interconnect metallization. (b) An SEM image showing flexibility of a corrugated nanowire after suspension. (c) An SEM micrograph that illustrates all of the channels through which the islands are interconnected. By introducing analog multiplexer circuits inside each island (not done in this work) multiple sensor port measurement can be achieved. (d) A comparison between a human hair and the array size. The corrugated wires are designed to give enough flexibility to the array to cover very small micro curvatures.

Silicon-on-Insulator layer reduces the stress and leads to minimal strain bending and enhanced flexibility [42]. Figure 2.4 illustrates several SEM micrographs of the meandered interconnections. In an initial attempt, a micromanipulator setup was used inside the SEM in order to study the array under strain. This experiment setup was replaced by a more advanced method, as explained in the next section.

2.5   Mechanical Characterization

The flexibility of the array was experimentally tested by applying a gentle force to the suspended array, using a computer controlled tip as illustrated in Figures 2.5(a,c). A Klocke Nanorobotics manipulator inside a FEI Nova 200 dual beam FIB/SEM (Focused Ion Beam) setup was used for this purpose. While a bending radius of 560 μm was achieved, the experiment was limited by concerns about damage to the tip of the manipulator.
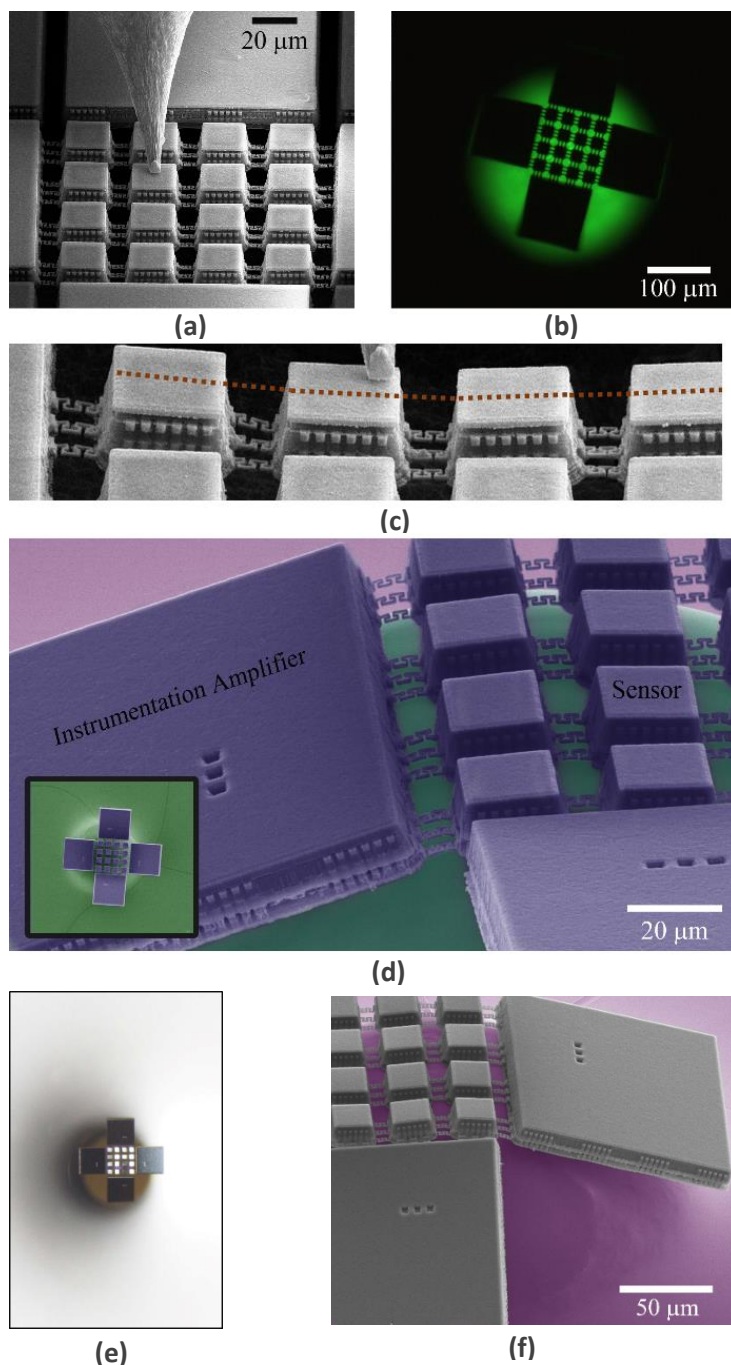
Figure 2.5. (a) An SEM micrograph that illustrates the microelectrode array inside the FIB vacuum chamber. The tip is located on the surface of a micro island. (b) A fluorescent microscope image of the array laminating on a 220 µm fluorescent micro-bead. (c) An SEM image that illustrates the bent array under the Nanorobotic tip force. (d) A false color SEM image of the microprobe array transfer-printed on a fluorescent microsphere. The inset

illustrates a false color SEM image of the microprobe array transfer-printed on a fluorescent microsphere from a top view. (e) An optical microscope image of the array being transferred onto a micro-bead. (f) A false color SEM image of the microelectrode on a PDMS concave micro-curvature.

Polydimethylsiloxane (PDMS) was used as a soft stamp to pick up the microprobe array and transfer-print it onto a planar or concave host substrate. An in-house micromanipulator setup was built to bring the microprobe array close to the host concave substrate. As the interconnections and active Si islands are monolithically integrated, they all transferred in one step. Consequently, no alignment was necessary during the transfer-printing process, which facilitated much higher yield of complex circuits in comparison to competing technologies [31]. Figures 2.5(b,d) show a 220 μm diameter fluorescent microsphere coated with a thin PDMS layer (50 μm) used as a host substrate for the transfer printing procedure. Conformal wrapping of the microelectrode onto a concave hemispherical fluorescent surface demonstrates the flexibility of the array with an extremely small bending radius. The CMOS sensors exhibited no change in their DC electrical performance after transferring.

A similar experimental method was also developed to transfer cells onto the surface of a microelectrode array. Figure 2.6 illustrates optical and SEM images of a fixed mouse female germline stem cell transferred onto the microarray using a micro-tweezer. The operation mechanism of the micro-tweezer is reported elsewhere [43], [44]. The stem cell was fixed in a 2.0% Gultaraldehyde in 0.1 mol Cacodylate buffer pH 7.4 solution prior to transferring (Figures 2.6(a,b)). Figure 2.6d illustrates the false color SEM picture of a microelectrode array over fixed mouse ova. The extreme flexibility of the microelectrode array combined with the ability to transfer-print it on to a curved surface facilitates extracellular recording of cell temperature and other vital signs.
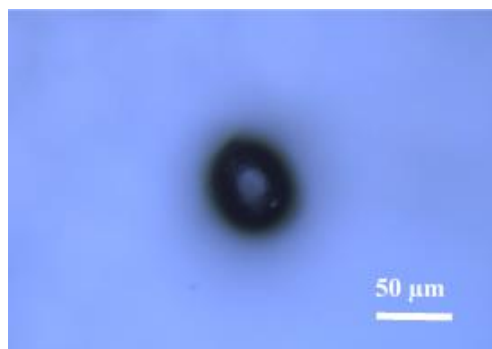
(a)
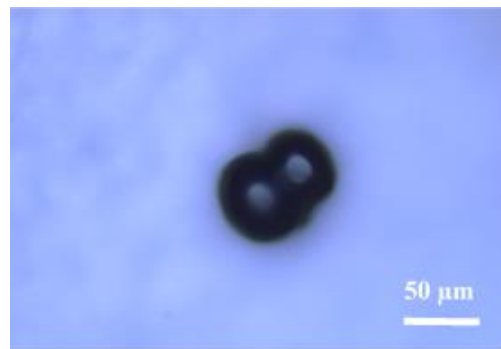
(b)
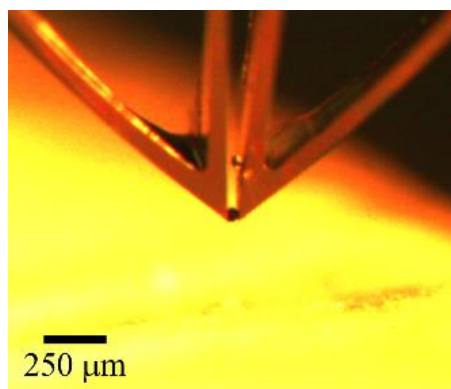
(c)
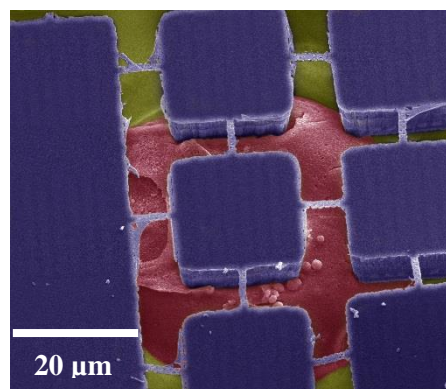
(d)
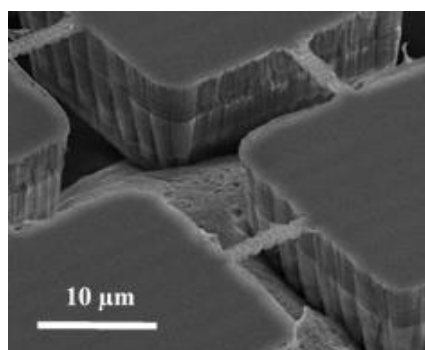
(e)
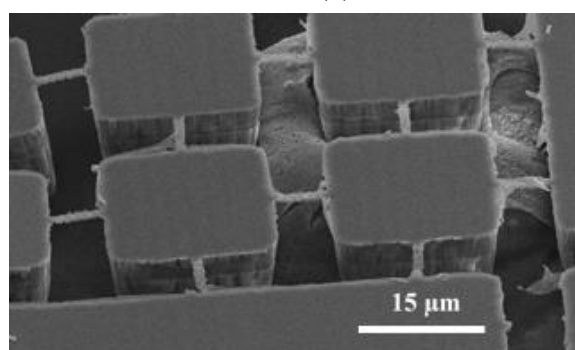
(f)
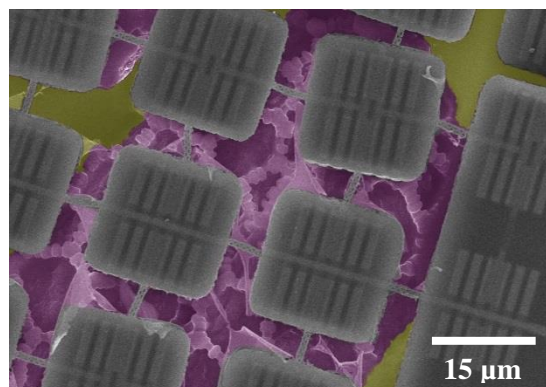
(g)

Figure 2.6. Transferring the array onto fixed cells and flower pollen: (a,b) An optical microscope image of a mouse female germline stem cell and a two cell embryo, after preparation, fixation and dehydration. (c) An optical image illustrating the cell manipulation onto the microelectrode array using a micro-tweezer. (d) An SEM image of the microelectrode array covering a mouse female germline stem cell. (e,f) An SEM micrograph of the array over the cell. (g) A false color SEM micrograph of the microelectrode array covering a dried flower pollen (Lily pollen) for demonstration.

2.6   Electrical Characterization

In order to confirm the adaptability of the microelectrode array to the real cell environment, we have conducted electrical measurements with a suspended microelectrode array under mechanical strain when it is in a wet environment. A packaging process has been developed for this purpose. The process starts with top anisotropic etching of the SiO_2 illustrated in Figure 2.3(b), followed by the wirebonding of the sensor to a punched PCB board to be able to make electrical connections (Figure 2.7(a)). The next step was to spin coat a very thin layer of PDMS on the surface of the chip. Then, a small hole was made on the backside of the chip using a XeF_2 silicon dry etching technique (Figures 2.7(b,c)). The hole was filled with Cell Culture Media that resembles the real condition of cell measurement. A custom made micromanipulator setup (Figures 2.7(d,e,f)) was used to move a small pin (Figure 2.7(g)) in the vertical direction, in order to gently deflect the suspended microelectrode array. The entire setup was placed under an optical microscope in order to facilitate alignments and imaging of the experiment.
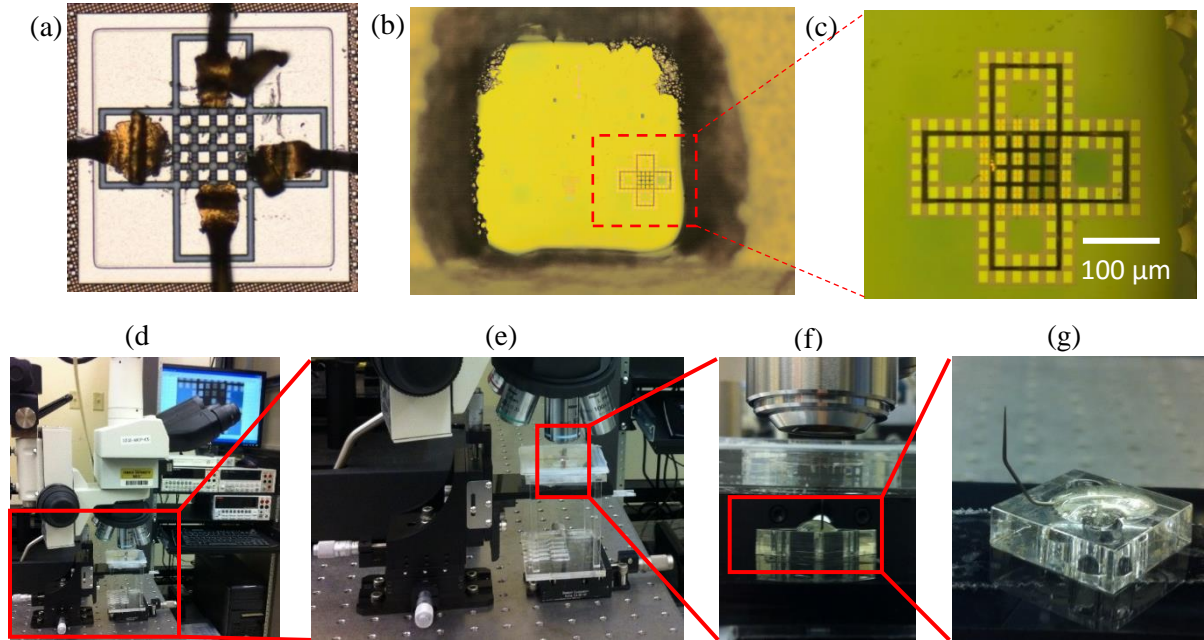
Figure 2.7. (a) An optical microscope image of the chip after wirebonding. (b,c) An optical microscope image of the backside of the chip, after a window has been opened on the silicon substrate. The back side of the microelectrode array is revealed after using XeF_2 silicon dry etching. (d,e,f,g) The experimental setup used for gentle deflection of the microelectrode under wet conditions. (d) Optical microscope (e) two micromanipulators (f) microscope lens (g) pin.

Figure 2.8(a) illustrates the schematic of the setup used for this experiment. Figure 2.8(d) illustrates the electrical measurement of the sensor in dry/wet, and also in relaxed/strained, conditions. Figures 2.8(b,c) illustrate the optical microscope image of the array before and after being deflected in the setup described above. Note that the operation of the transistor is independent of the environment the sensor is located in. Figure 7(e) may be used to explain the observed behavior. This schematic illustrates the position of the sensor (transistor) inside the island. The deflection of the entire array does not cause any bending of the individual islands. Instead, the meandered wires deflect to accommodate for the displacement. Consequently, the deflection of the entire array does not affect the behavior of the transistor inside the island. The length of the transistor is about 1/20 of the length of the island, which enables the positioning of the transistor in a

protected and well passivated location inside the island. Figure 2.8(f) illustrates the islands on a PDMS concave shape. One can see the islands does not bend under any mechanical strain applied to the array.
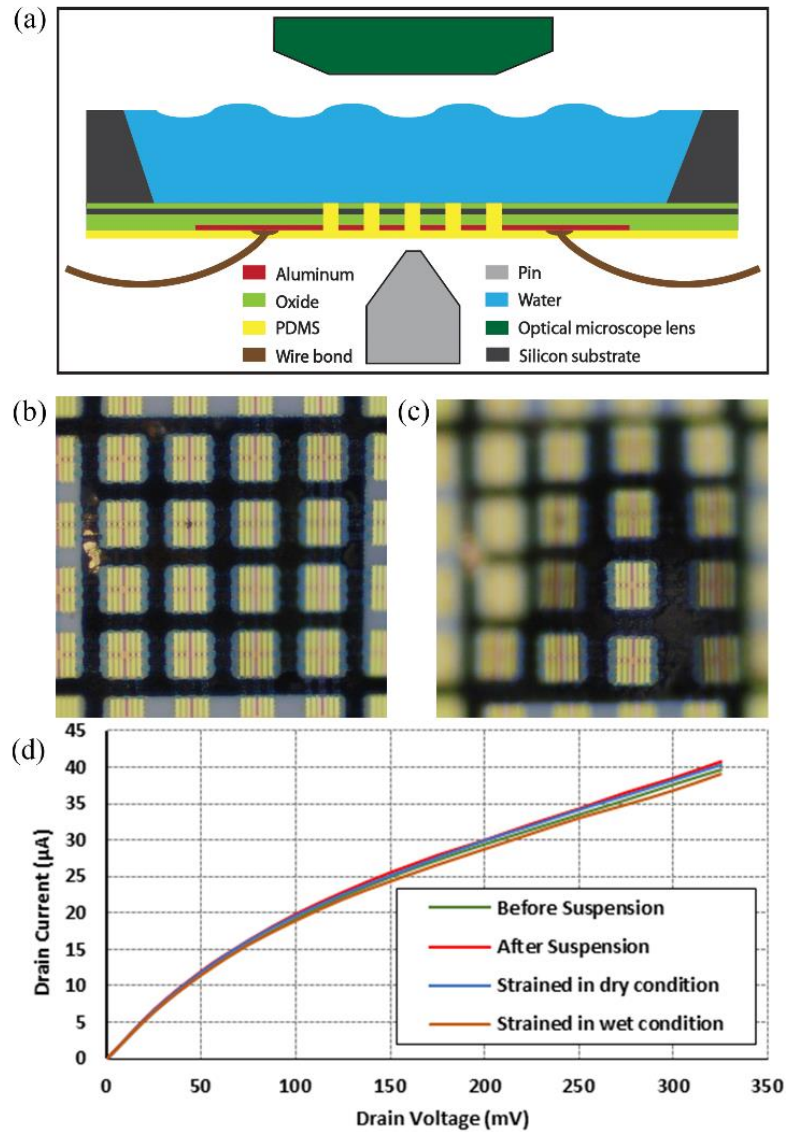
Figure 2.8. (a) A schematic of the microelectrode array under strain and in wet condition. (b,c) An optical microscope image of the backside of the chip exposed after using XeF$_2$ silicon dry etching, after a window has been opened on the silicon substrate. (d) An experimental measurement of the FET's drain current versus drain voltage under different conditions.

2.7   Temperature Sensing

A promising application of the microelectrode array is in single cell thermometry. CMOS temperature sensors can have high temporal resolution (fast response). In our experiment, the thermometer is based on buried CMOS transistors inside the islands. Note that in this experiment no live cell was used and only the thermometer was calibrated. The DC electrical characteristics of CMOS transistors change by temperature variation. The CMOS sensor was calibrated using a hotplate by monitoring the CMOS transistor drain current as the temperature of the hotplate changes in the range of 35 °C to 40 °C. First, the thermo-reflectance imaging microscopy [45] was used to confirm that the array elements are thermally isolated (Figure 2.9(a)). The thermal isolation facilitates reading the temperature variation across a cell (or cells) without any influence from the environment (microelectrode array thermal path).

To achieve maximum temperature sensitivity, the operation of the transistor was simulated under different biasing conditions to identify the most sensitive biasing region to temperature changes as illustrated in Figure 2.9(b). This behavior enabled us to exploit the linear dependence of drain current to temperature changes. Simulation was performed using Cadence virtuoso software. The drain-source current of the transistor was plotted for varying temperatures between 35 to 40 ^{o}C (with steps of 0.01 ^{o}C), under different gate-to-source (V_{gs}) and drain-to-source (V_{ds}) biasing conditions (between 0-1 V, with steps of 0.01 V). Consequently, the gate-to-source and drain-to-source voltages of the transistor were set to 400 mV and 300 mV, respectively, to achieve maximum temperature sensitivity at a relatively small current to avoid self-heating effects. Figure 2.9(d) illustrates an average increase in the drain current of 370 nA/^{o}C.
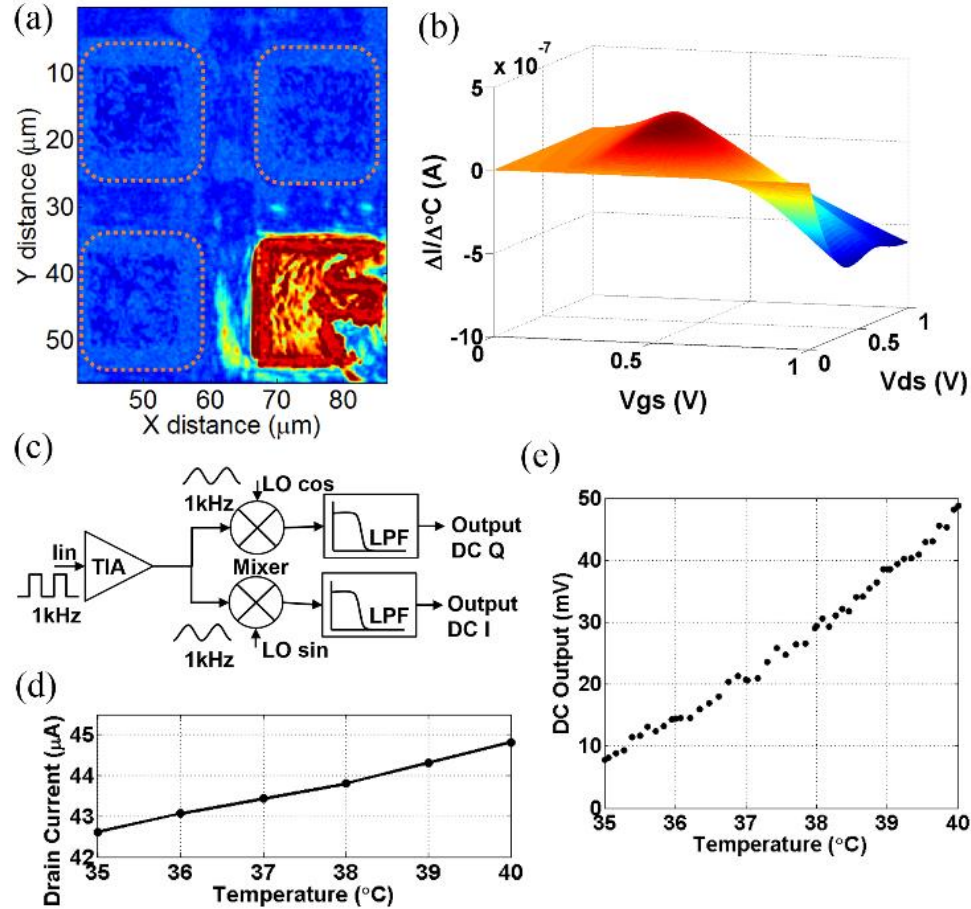
Figure 2.9. (a) A thermal micrograph of four different islands, captured using a non-contact thermo-reflectance technique. In this image, the bottom right island is selectively heated up to evaluate thermal leakage between islands. (b) Computer modeling (Cadence virtuoso simulation) of the transistor indicating the most sensitive bias operation mode with respect to temperature. (c) A simplified schematic of the on-chip instrumentation amplifier design with an input transimpedance amplifier (TIA) and in-phase and quadrature mixers. (d,e) The measured temperature of the sensor in one of the islands (d) without lock-in amplifier in 1 $^{\circ}$C steps and (e) with the integrated CMOS lock-in amplifier in 0.1 $^{\circ}$C steps.

Figure 2.9(c) shows a simplified schematic of the on-chip instrumentation amplifier, namely a lock-in amplifier implemented in the 45 nm CMOS SOI process by another student. The circuit is designed based on a trans-impedance amplifier (TIA) and two

quadrature differential phase mixers. Transistor sizes were chosen to achieve small flicker noise. Figure 2.9(e) shows the output voltage of the lock-in amplifier versus temperature. With an output voltage reading standard deviation of 425 μV, a temperature sensitivity of 0.15 ^{o}C was measured in this proof-of-concept design. Figure 2.10 illustrates the schematic of the integrated instrumentation amplifier.
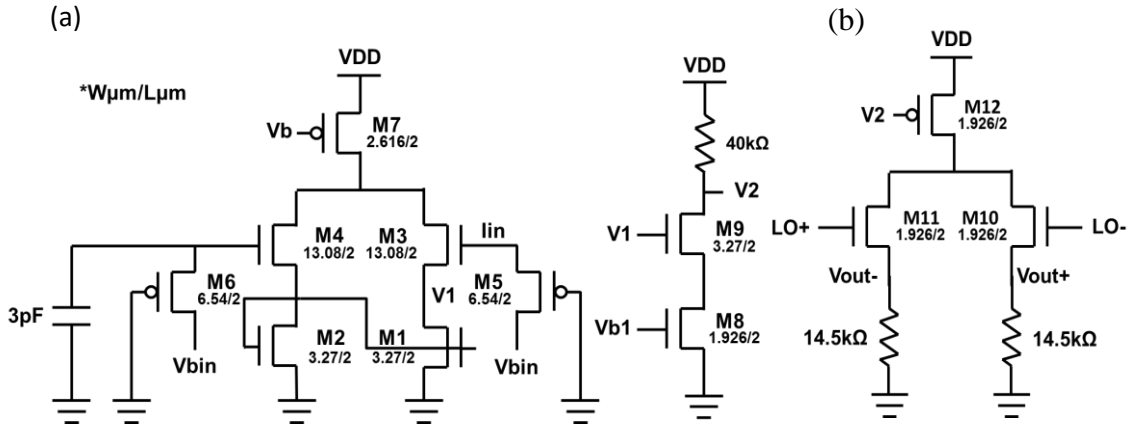
Figure 2.10. On-chip instrumentation amplifier implementation: The circuit is designed with an on-chip (a) trans-impedance amplifier (TIA) and (b) two on-chip quadrature differential phase mixers. Transistor sizes were chosen to achieve small flicker noise. Bias voltages are listed below: $V_b = 800$ mV, $V_{b1} = 600$ mV, $V_{bin} = 730$ mV.

2.8 Summary

In summary the technology to fabricate an ultra-flexible thermometer array based on ultrathin CMOS islands interconnected and held together with meandered Cu metals is demonstrated. Unlike current extracellular recording techniques that are performed by electrodes from a distance of about 100 μm from the cell [16], the proposed technology enables the development of microelectrode arrays that can conform to the cells, and have the potential to facilitate an unprecedented access to "cellular information". The monolithic nature of silicon membranes and their meandered interconnections bypass the yield limitations of existing transfer-printed circuits [31]. The proposed technology for the fabrication of flexible microelectrode array has the potential to enable simultaneous measurements at several sites, with direct contact to the cell surface. The use of a

standard CMOS process and a simple post-processing technology that does not use any lithography combined with a one-step transfer-printing method has facilitated an important milestone for future flexible and stretchable electronics. The proposed technology may find a variety of applications including precision single-cell characterization, flexible multi-functional sensing systems sensory skins, and smart wound therapy. These applications have emerged from the flexible nature of the device that yields conformal coverage of micro-curvatures combined with highly reliable and flexible complex integrated circuits achieved by the developed microprobe array.

2.9   Future Work

In the next generation designs, multiple sensors including action potential and pH sensors will be included in each island. Moreover, the dimensions of each island will be reduced further to suit single-cell and neuron measurements. Sensing various sites of the surface of live cells using the proposed device is another future directions, which will provide researchers with unprecedented information about the cellular behavior. Furthermore, in-vivo applications are possible by configuring the proposed device as a "neuro-prosthetic". An alternative design with pn junctions in each island can function as a sensitive neuro-biosensor An integrated wireless telemetry module with on-chip power scavenging is currently being developed and will be eventually integrated with the proposed MEAs.

3. LATERAL AND VERTICAL CMOS INTEGRATED FIELD EMITTERS

3.1 Introduction

Electron emission refers to a phenomenon in which free electrons are emitted from a surface into vacuum under specific conditions. Four different methods are known for electron emission, which are listed in the following: (i) thermionic emission; (ii) photoelectric emission; (iii) secondary electron emission; and (iv) field emission. In thermionic emission, electrons are ignited from the surface of cathode by gaining enough thermal energy from an external heat source. In this method the emission current can be controlled by tuning the heating power of the cathode and can achieve long-term stability without any problem. However, in some cases high temperature working conditions result in the outgassing or even evaporation of the cathode material [3]. High power consumption is another disadvantage of this method. On the other hand, photoelectric emission needs high energy UV light or laser beam sources for electron emission, and can only generate a small number of free electrons, leading to the low efficiency of this technique In the third method, secondary electrons are emitted from the surface as a result of an incident between externally energized particles and the primary electrons on the surface.

Field emission is a technique, in which a strong electric field applied to the surface ignites the electrons from the cathode to the anode electrode [46]. The field emission process can operate at room temperature, hence lower power consumption can be achieved as opposed to thermionic emission. Moreover, the response time is extremely fast and it does not need thermal radiation or UV light as an external source. Also, there is a low probability of chemical reaction between the cathode material and the

surrounding gas. The performance of the emitter array; however, is sensitive to the operating environment [47]. In low vacuum working conditions, the ionized gas molecules strike the emitter and may cause damages to the surface [48]. Also, field emitters require micro- and nano-protrusions, which leads to high production cost. Table 3.1 lists different electron emission techniques and their advantages and disadvantages.

Table 3.1. A comparison between the deferent electron emission methods

Method	Advantages	Disadvantages
Thermionic emission	Can achieve long-term stability by tuning the heating power	High temperature may result in outgassing or even evaporation of the cathode material
		High power consumption
Photoelectric emission	Applications in photo cells and solar panels	Needs high energy UV light or laser beam sources
		Generates a small amount of free electrons
Secondary electron emission	Applications in electron beam microscopies	Needs external high energy particle generation
Field emission	Operate close to room temperature	Performance sensitive to the operating environment
	Lower power consumption	Higher production cost
	Fast response time	
	No need for thermal radiation or UV light external sources	
	Low probability of cathode chemical reaction	

In field emission, a high electric field increases the probability of quantum mechanical tunneling through the surface energy barrier of a metal. As a result of applying a very high electric field, the potential ramp between the Fermi level and the vacuum level deforms, leading to a small potential barrier (Figure 3.1). Consequently,

electrons with energies near the Fermi level can tunnel through this barrier and ultimately emit into vacuum.
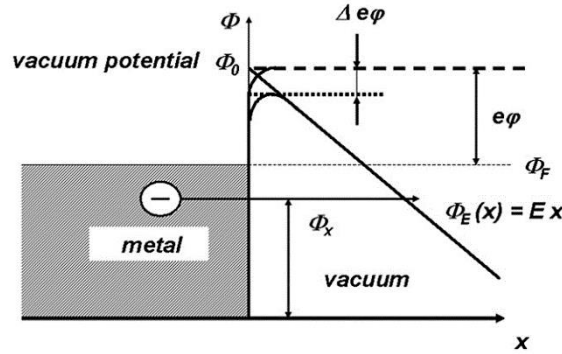
Figure 3.1. Simplified potential model for the field emission of metals (Figure from reference [3])

Neglecting the Schottky effect, the field emission current density can be described by the Fowler-Nordheim (F-N) Equation [3]:

$$J = \frac{q^3 \, E^2}{17.6\pi^2 \, \hbar\emptyset} exp(\frac{-4\sqrt{2m}.v(y).\emptyset^{1.5}}{2q\hbar.E}) \tag{3.1}$$

where J is the current density, E is the electric field, q is the electron charge, $\emptyset$ is the metal work function, m is the electron mass and $\hbar$ is the reduced Planck constant. Function $v(y)$ expresses the effect of Schottky barrier lowering on the probability of electrons escaping the surface in a simplified form. Parameter y is the ratio of Schottky barrier lowering to the metal work function. The function $v(y)$ and parameter y are given by the following Equations [49]:

$$v(y) = 0.95 - y^2 \tag{3.2}$$

$$y = \frac{1}{\emptyset} \sqrt{\frac{Eq^3}{4\pi\varepsilon_0}} \tag{3.3}$$

The geometry of the emitter plays a major role in enhancing the electric field, hence the emission current density with a given anode-cathode voltage. Geometrical parameters include: (i) cathode tip sharpness; (ii) cathode aspect ratio; (iii) gaps between the cathode electrodes and (iv) distance between the anode and cathode. The field enhancement factor (β) describes the relation between the above mentioned parameters and the electric field:

$$\beta = \frac{E \cdot d}{V_{(anode-cathode)}} \qquad (3.4)$$

where d is the distance between the tip of the cathode and anode and V is the anode-cathode voltage. The electric field E is perpendicular to the surface of the tip at any point on the tip. The larger the β, the higher the field enhancement, and therefore, the lower the emission turn-on voltage. According to Equation 3.1, the metal work function $\emptyset$ is another crucial parameter to modify the field emission property. An ideal electron source should have a small value of $\emptyset$. Additionally, a material with high melting point and excellent thermal conductivity is preferred. For practical applications, a large number of inexpensive and easy to process tips are required.

Electron emission technology has found variety of commercial applications. Devices such as flat panel displays [50], [51] were successfully integrated to demonstrate moving color images. Field emission based x-ray sources have provided images of biological samples [52], [53]. Taking advantage of microelectromechanical system (MEMS), novel miniaturized field emitter-based pressure sensors have also been proposed [3]. Vacuum channel transistors, diodes and triodes have found applications in vacuum micro and nanoelectronics [54]–[56]. Developed electron guns have found applications in high power microwave sources [57], [58] and also field electron spectroscopy and microscopy. Moreover, presented gas discharge tubes may find applications for protecting telecommunications against power surges [59].

Field emitter nanostructures have exploited a wide range of materials, including metals, silicon, carbon, diamond, etc. Metallic nanowires, such as gold, silver, copper, nickel, and molybdenum have demonstrated excellent performance due to their low work

function (∅) and high thermal and electrical conductivity [49], [60]–[67]. However, they cannot operate at very high temperature conditions as they deform and melt. Silicon field emitters take advantage of the well-established fabrication techniques offered by the semiconductor industry. This capability enables the fabrication of tip geometries ranging from cones to wedges to pyramids, with high aspect ratios [68]–[70]. Also, the silicon technology facilitates the integration of sophisticated current control circuits with the field emitters on the same substrate [71]. However, it has been demonstrated that silicon-based emitters are subject to oxidization which affects their emission performance [3].

Carbon nanostructures, such as carbon nanotubes, carbon nanoparticles and graphene have also been investigated as field emitters. Small tip radii, high aspect ratios, high melting points and high mechanical and chemical stability are among the advantages for carbon nanotube based devices. However, the random orientation of nanotube and nanowires leads to unstable emission currents. Moreover, weak electric and thermal contact between the substrate and carbon nanotubes are still problematic [72]. Extra processing, such as supplementing carbon nanotubes with low work function metals, has been demonstrated to improve their local electric field properties, and hence field emission properties [73]–[75]. Metal-based tips have been shown to be more durable in comparison with carbon nanotube field emitters [76]–[78]. Diamond is a material of negative electron affinity, which has also been investigated as a material for field emitters [79].

One of the main challenges in realizing the long term durability of field emitters is the inability to achieve uniform nanowires [80]. Various technologies have been used for the fabrication of field emitter arrays. These techniques include: Focus Ion Beam (FIB) [49], electron beam lithography (EBL) [81]–[83], synthesis of carbon nanotubes (CNTs) [72]–[74], [84] and electrochemical processing [66], [85], [86]. These fabrication techniques are unable to control the sharpness, length and orientation of the tips well, hence, the concentration of the electric field will not be uniformly distributed among the nanowires. As a result, the nanowires don't emit uniformly at a given applied anode-cathode voltage. Therefore, some of the tips fail earlier due to higher current conduction,

which causes thermal stress. This process continues in a chain until the array is burnt out, which is known as a catastrophic failure [80].

Utilizing the CMOS process for field emitters addresses the reliability obstacle mentioned above by making engineered tips, and taking advantage of a well-developed fabrication process [70], [71]. CMOS field emitters offer the following advantages: (i) Uniform tips guarantee homogeneous emission, leading to reliable and durable devices; (ii) Miniaturization of the distance between electrodes (cathode, anode and gate) leading to low turn-on voltages; (iii) Monolithic integration with electronic circuits, which facilitates active current controlling; (iv) Small operating currents; (v) The fabrication process does not require lithography, leading to reduced cost.

3.2   Fabrication and Experiment

In this work, we take advantage of CMOS technology to integrate field emission tips on the CMOS substrate. The fabrication process starts with the CMOS transistor fabrication on a silicon on insulator substrate. This step performed by a semiconductor manufacturing foundry is followed by BEOL process, which includes several layers of metal on top of the Si wafer, which facilitates the interconnection between the underlying electronic components. All metals are surrounded by SiO_2 or low-K dielectric polymers, which keeps them electrically isolated from each other. CMOS metallization layers are exploited to fabricate uniform field emitters through designing electrically connected islands of copper to serve as nano-tips. The 3D metal nanowire tips are formed after in-house post-processing, using anisotropic etching of SiO_2 in an inductively coupled plasma chamber. The CMOS top metal (Aluminum) serves as a protective layer against plasma over the chip. Figure 3.2 summarizes the fabrication process of both vertical and lateral nanowires presented in this work. Post-processing recipe is provided in Appendix A.2.
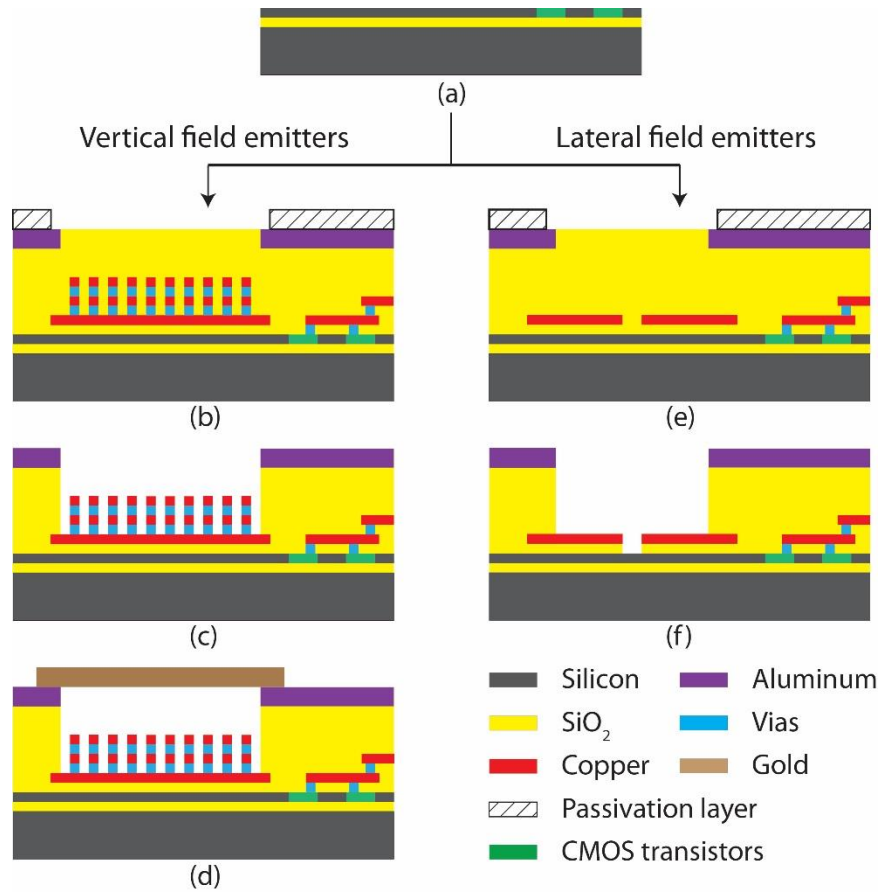
Figure 3.2. Schematic of the steps involved in the fabrication of vertical and lateral copper nano-tips. (a) The CMOS transistors are fabricated on the silicon substrate. (b,e) Multiple copper and tungsten metal layers are fabricated to shape the nano-tips and also to serve as CMOS interconnections. (c,f) Anisotropic dry etching of SiO_2 is used to reveal the nanowires. (d) Nano-tips in presence of externally fabricated anode.

Three different types of devices have been designed, fabricated and experimentally tested. The functionality of two orientations of vertical and lateral nanowires have also been investigated. Field emission parameters and relative emission durability have been evaluated for all devices. For the measurement, post-processed CMOS chips were loaded into a vacuum chamber and tested at 3.5×10^{-8} Torr. A Kepco power supply was used as the DC source, and a Keithley 6485 was used as a precision current picometer and

automatic data acquisition was conducted by a computer. Figure 3.3 illustrates the measurement setup.
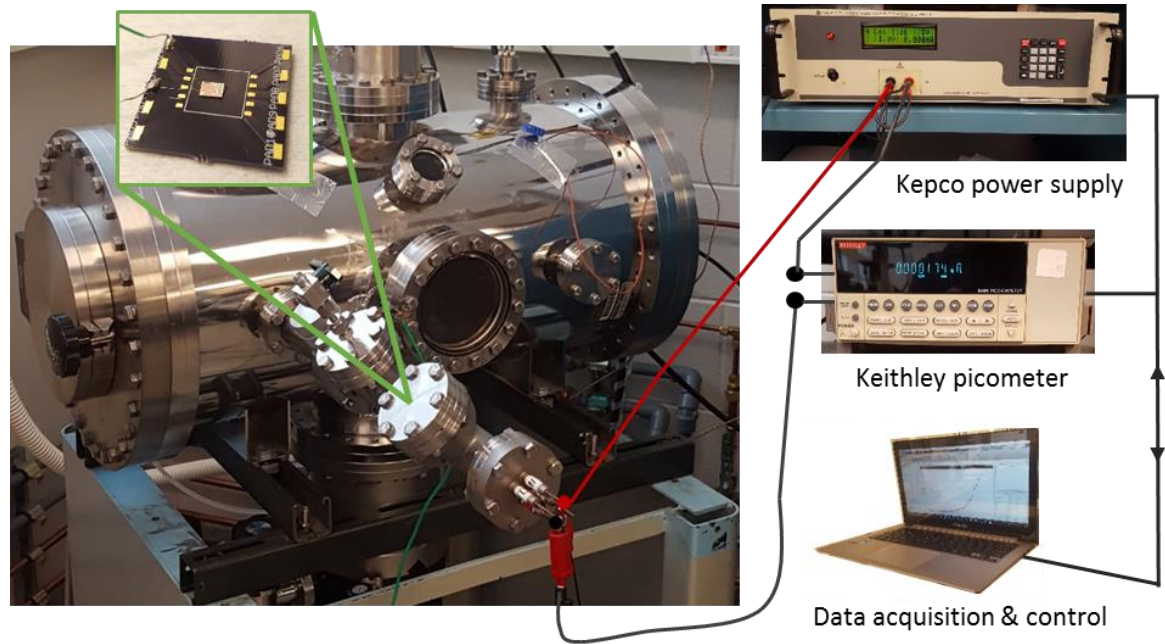
Figure 3.3. Experimental measurement setup, illustrating the vacuum chamber and utilized measurement equipment.

Device number 1 was designed in a 130 nm bulk CMOS technology, in which vertically standing nanowires were formed using two stacked copper layers (M2 and M3) and their relative tungsten via layers. Vertically oriented nanowires are suitable for applications such as displays and technologies requiring an electron gun [50]–[53]. Figure 3.4 illustrates an SEM image of the uniform CMOS nanowire array. The anode-cathode distance in this design is 17 μm and the radius of the tips is around 150 nm. Figure 3.4(d) depicts CAD simulation (using Comsol Multiphysics software) of the electric field distribution around the nanowires, when a 30 V potential is applied across the cathode and anode electrodes. The anode-cathode gap was assumed ideal vacuum, and the anode and cathode materials were chosen to be gold and copper, respectively. The simulation results showed uniform distribution of the electric field among nanowires

(with maximum electric field of 5.55 x 10^6 V/m), with no proximity effect across the neighboring nano-tips.

(a)

(b)

(c)

(d)
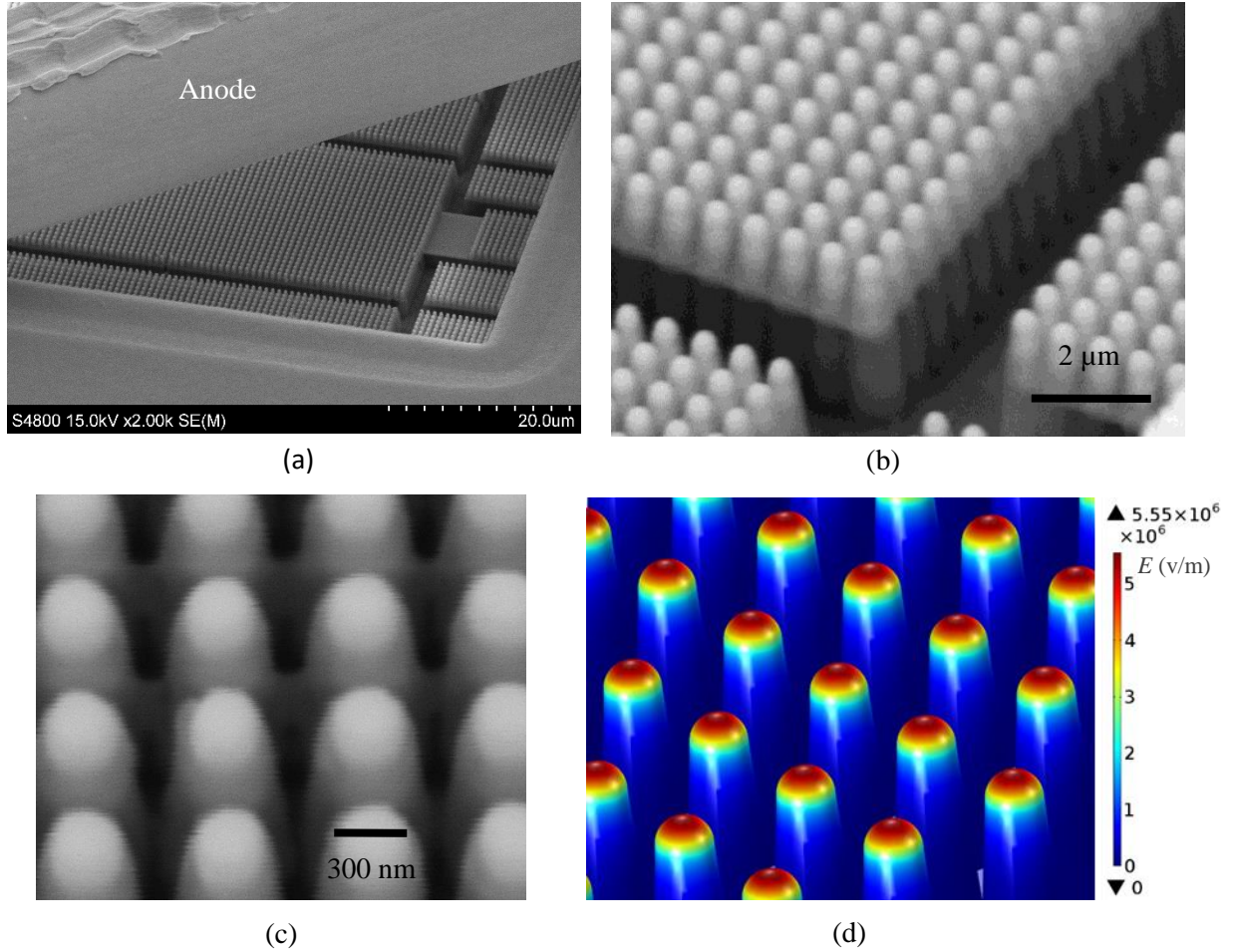
Figure 3.4. (a,b,c) SEM micrograph of the vertically oriented nanowire array (device number 1). (d) CAD simulation for the electric field distribution for an anode-cathode voltage of 30 V.

Figure 3.5 illustrates the experimental data related to the device number 1. In the current-voltage plot (Figure 3.5(a)), one can see a rise in the current above 12 V, due to the initiation of the Fowler-Nordheim tunneling process. The error bars show a maximum standard deviation of 29.38 pA, after repeating the measurement five time on the same device. To examine the current-voltage data more closely, the corresponding Ln (I/V^2)

versus (1/V) plot is depicted in Figure 3.5(b). The field enhancement factor (β) is calculated according to the following equations:

$$\beta = \frac{-b * \emptyset^{1.5} * d}{S} \tag{3.5}$$

$$b = constant = 6.85 * 10^7 \ \left(\frac{V}{cm \,.(eV)^{1.5}}\right) \tag{3.6}$$

where $\emptyset$ is the metal work function in eV, d is the anode-cathode distance and S is the slope of the F-N plot. Considering the copper metal work function of 4.5 eV and $d = 17$ µm, a value of ~6000 is estimated for β. The stability of the field emission is crucial for practical applications. The field emission current has been monitored for several hours, at a fixed voltage of 14 V. Figure 3.5(c) illustrates lifetime measurement for the proposed device. The lifetime measurement shows a standard deviation of 32 fA from the average in a duration of 12 hours, which is ±4.1% of the operating current.
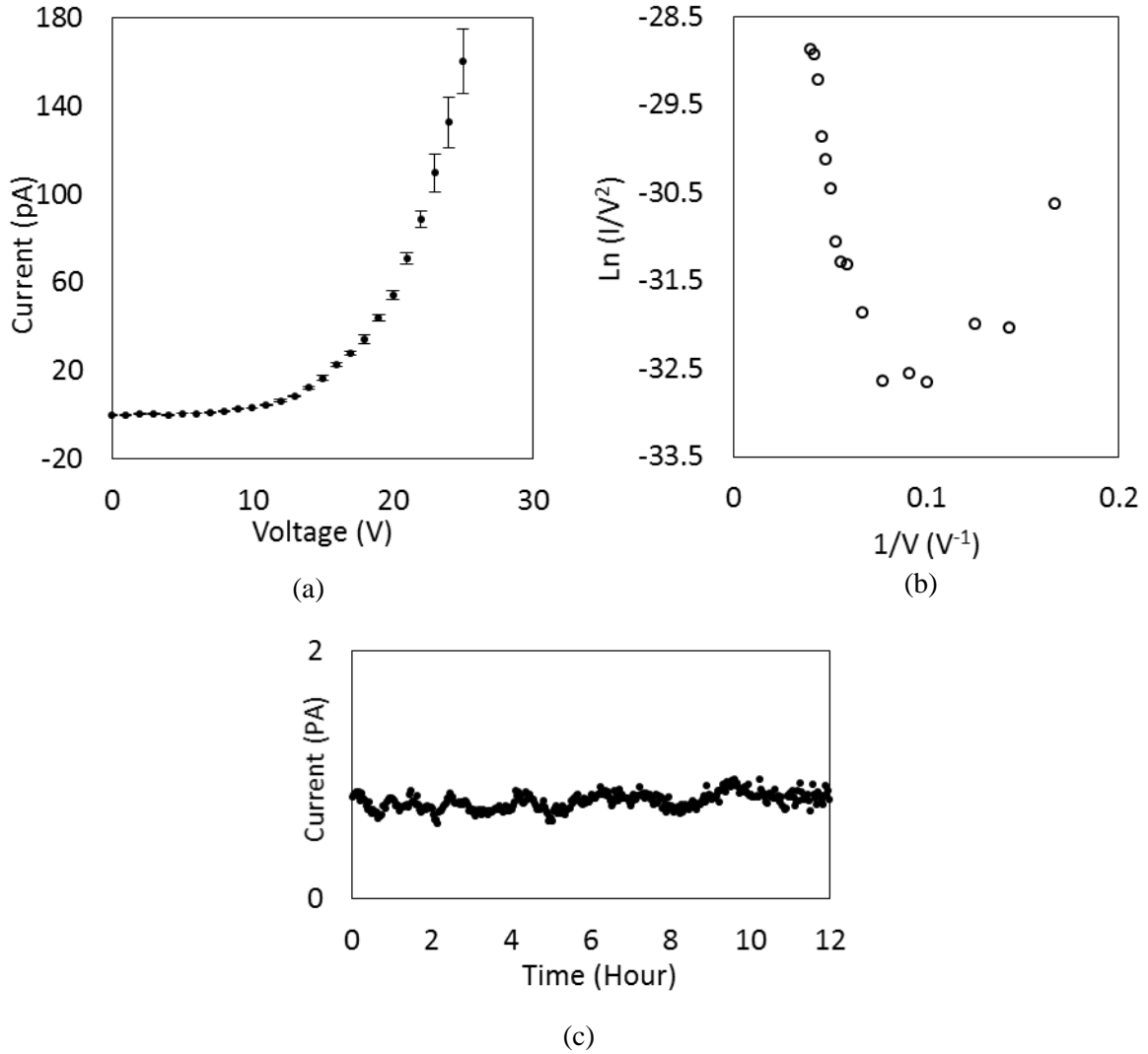
Figure 3.5. Experimental result for device number 1. (a) The emission current as the result of sweeping voltage. (b) The corresponding Fowler-Nordheim plot. (c) A long term current measurement at an anode-cathode voltage of 14 V.

Device number 2 was designed with 26 pairs of lateral nano-tips in a row and was fabricated in the same 130 nm bulk CMOS technology. The distance between the anode and cathode tips was 320 nm, with a tip radius of 150 nm, and nanowire length of 1 μm. The space between two adjacent nanowires is 750 nm. CAD analysis were performed (Figure 3.6(c)) for electric field distribution on the nano-structure, under conditions close

to the real measurement environment. Comsol Multiphysics software was used for the simulation. The anode and cathode materials were both chosen to be copper inside a vacuum environment. A maximum electric field of 1.98×10^8 V/m was obtained at the tip of nanowires. The magnitude of the electric field dropped by 123% at the point between the two neighboring nano-tips, which illustrates a small proximity effect in this design. In this device, the anode and cathode were fabricated on the same substrate, so there was no need for a separate anode and consequently, no need for alignment. Lack of alignment requirement is a clear advantage in terms of the simplicity of the fabrication. In contrast with the vertical nano-tips, the proposed lateral nanowires are composed of copper only. In general, lateral field emission devices may be suitable for radio frequency applications [87], due to small distance between the electrodes (anode and cathode), leading to small transit times [88]. Figure 3.6 illustrates the SEM image of the device.

(a)

(b)

(c)
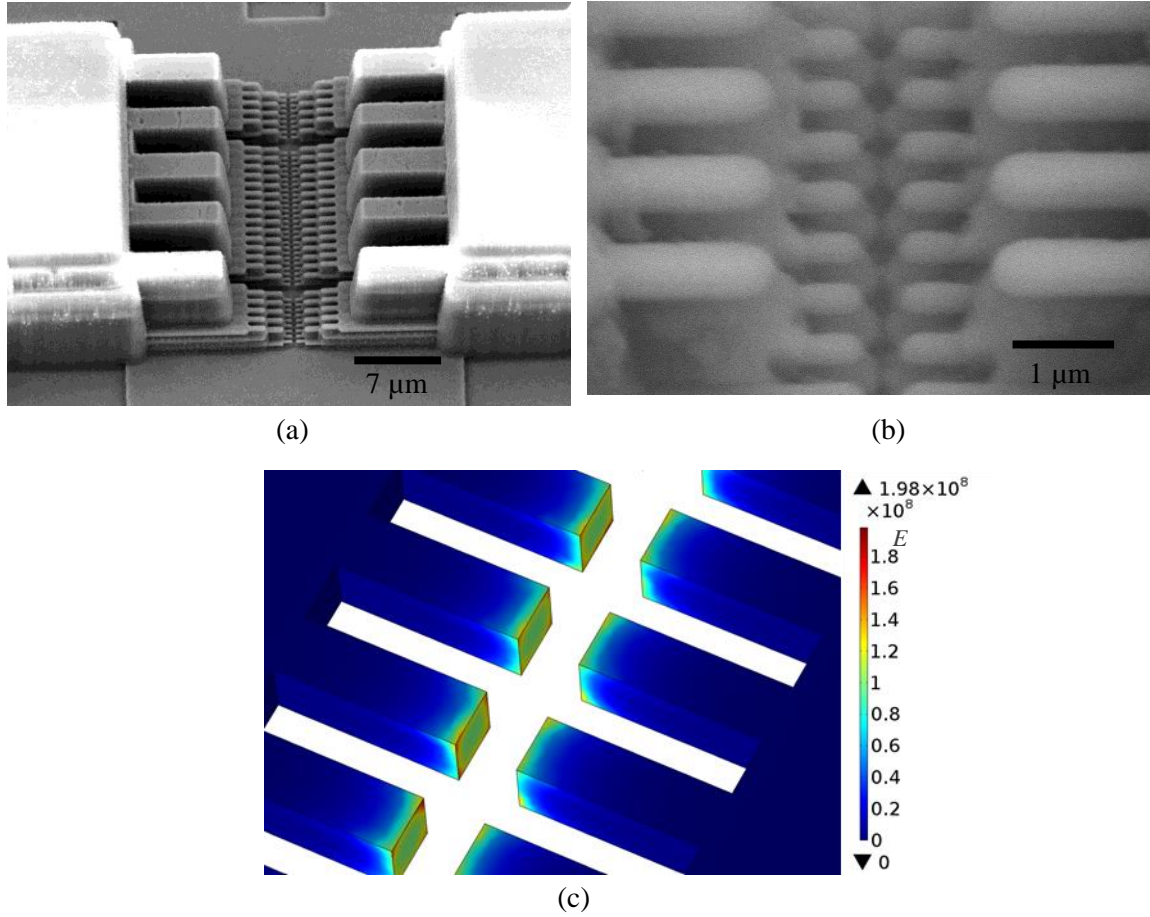
Figure 3.6. (a,b) An SEM micrograph of the laterally-oriented nanowire row (device number 2). (c) A CAD simulation of the electric field distribution for an anode-cathode voltage of 30 V.

Figure 3.7 illustrates the measurement results obtained for device number 2. Two different field emitters, namely devices *a* and *b*, were separately fabricated and tested. At a sufficiently high electric field across the electrodes, the field emission with a turn-on voltage of 8 V was observed as illustrated in Figure 3.7(a). Each device was measured five times and the error bars in Figure 3.7a illustrate the maximum standard deviation of 0.48 nA and 0.24 nA for devices *a* and *b*, respectively. The negative slope parameter of the device was achieved using the F-N plot, illustrated in Figures 3.7(b) and 21(c). The corresponding value for β was calculated using Equation 3.5. An average field enhancement factor $\beta = 780$ was achieved for this device. The durability of the devices

has been validated by performing lifetime measurement, as depicted in Figure 3.7d. The lifetime measurement shows a standard deviation of 30 fA from the average in a duration of 12 hours, which is as small as ±1.8% of the operation current (Deviations of ±1.2% has been reported by other groups [89]).

(a)

(b)

(c)

(d)
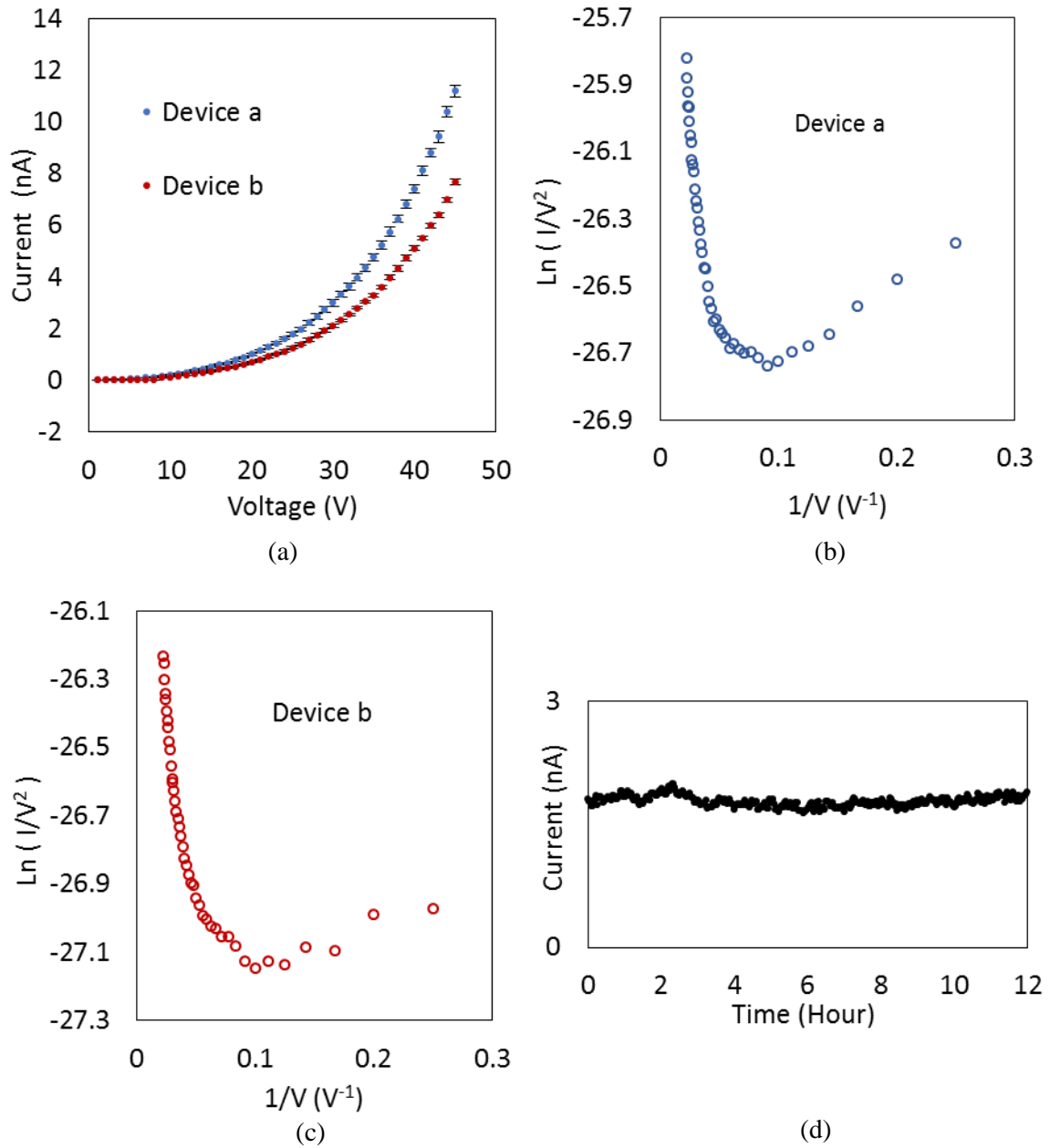
Figure 3.7. Experimental results obtained from device number 2. (a) The emission current as the result of sweeping the voltage for two different devices.

(b,c) The corresponding Fowler-Nordheim plots. (d) A long term current measurement obtained at an anode-cathode voltage of 26 V.

Device number 3 was designed in a standard 45 nm CMOS SOI technology, which enables the fabrication of finer tips, with a lower anode-cathode distance. Closer electrodes in such lateral field emitters enables lower turn on voltage and higher current density. As illustrated in Figure 3.8, the dimension of the cathode electrode becomes very fine as it gets closer to the anode. This feat has been achieved by fine dimensions of the lower metal layers of this CMOS technology. The tip radius is only 60 nm, and the distance between anode and cathode is 110 nm. In general, high-speed emission modulation of the emission current can be achieved in devices with such small anode-cathode gap size. Comsol Multiphysics software was used to simulate the electric field at the tip of the electrodes (maximum 9.07×10^{7} V/m). The anode and cathode materials were both chosen to be copper within an ideal vacuum environment.
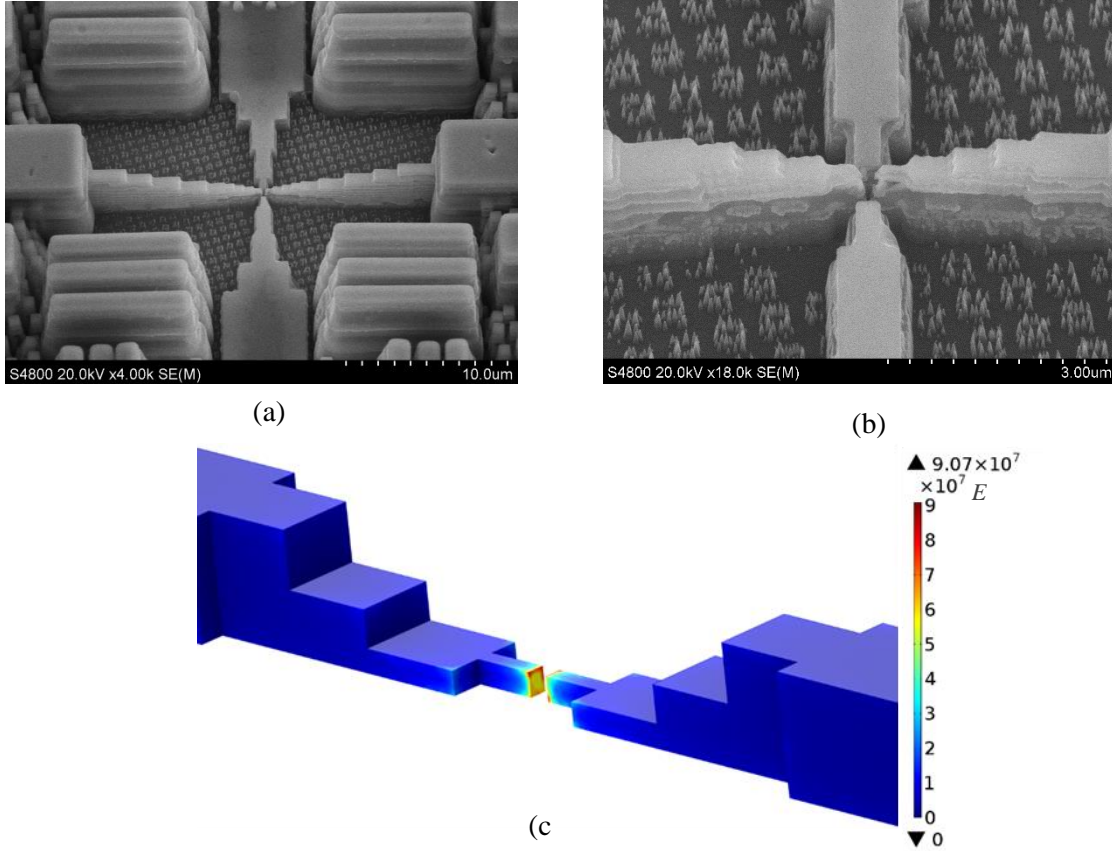
Figure 3.8. (a,b) SEM micrograph of the laterally-oriented nanowire pair (device number 3). (d) CAD simulation for the electric field distribution for an anode-cathode voltage of 6 V.

Figure 3.9 illustrates the experimental results of device number 3. The current-voltage characteristic in Figure 3.9(a) depicts a turn on voltage of 4 V, with a measured emission current of 8 nA from the device with two opposing tips and a maximum standard deviation of 0.98 nA after five repeated measurement. Note that the low operating voltage of the device is due to a small anode cathode distance and rather sharp tips. The current levels remain even in the beginning and then increases substantially beyond the turn on voltage. The $Ln(I/V^2)$ versus $1/V$ plot presented in Figure 3.9(b) leads to an estimated field enhancement factor (β) of ~450. The measured current isnstable over a period of 60 minutes of continuous operation as shown in Figure 3.9(c). The

lifetime measurement shows standard deviation of 3.2 pA from the average, which is ±7.4% of the operation current.

(a)

(b)

(c)
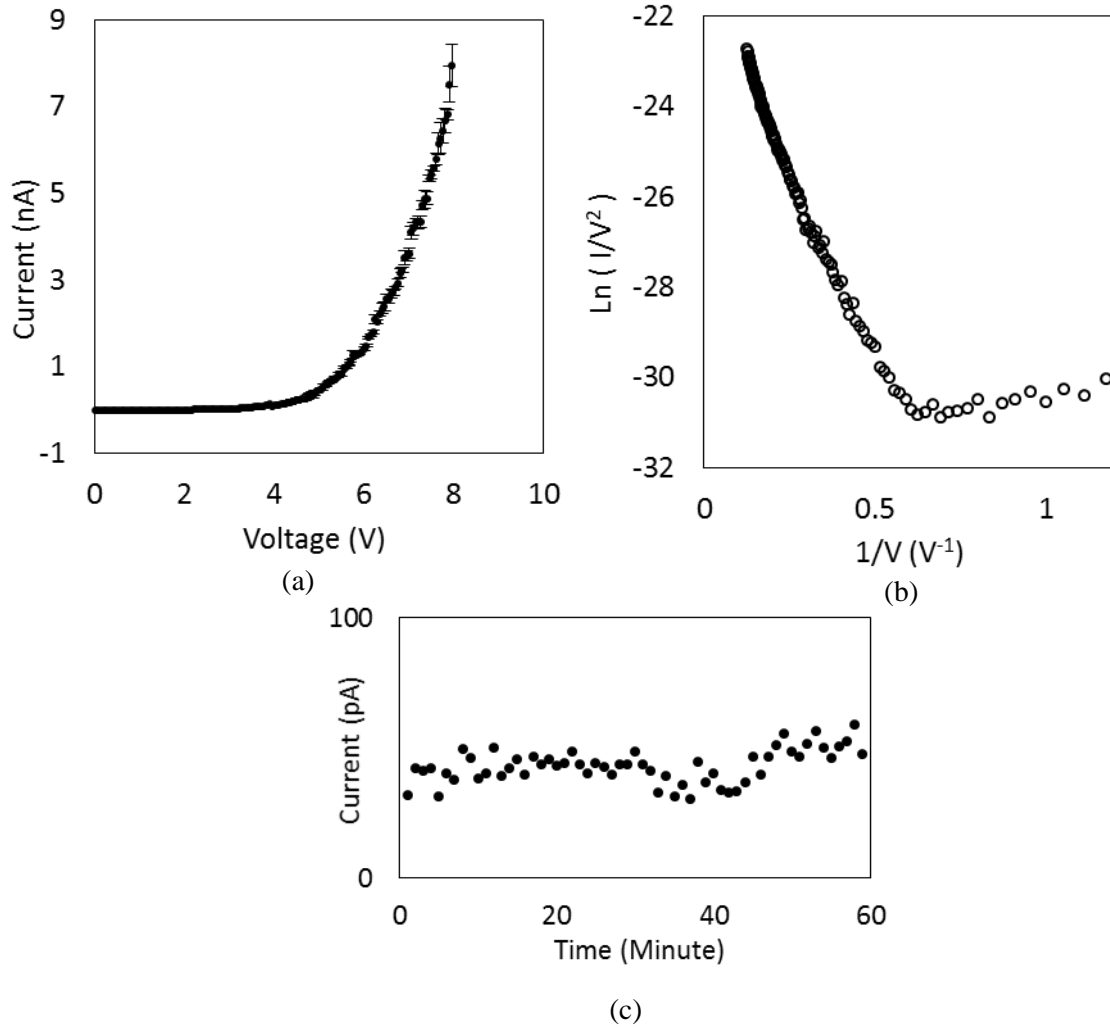
Figure 3.9. Experimental result obtained from device number 3. (a) The emission current as the result of sweeping voltage. (b) The corresponding Fowler-Nordheim plot. (d) A long term current measurement obtained at an anode-cathode voltage of 4.3 V.

In order to confirm that the observed currents are due to the field emission phenomenon, the current characteristics of the targeted devices were compared at three different conditions: (i) $8.3_\times10^{-8}$ Torr; (ii) atmospheric pressure; and (iii) before post-

processing when the anode-cathode gap is filled with SiO_2. No measurable current was observed for the second and third conditions. Lack of measurable current in atmospheric environment is due to gas molecules such as H_2, H_2O, Ar, N_2 and O_2 absorption effect on the emission behavior [90] under atmospheric pressure environment.

3.3　Summary

In summary, different CMOS integrated field emission devices have been fabricated and tested. Field emitters shaped after CMOS post-processing take advantage of a well-developed procedure of standard CMOS process towards fabrication of engineered, extremely uniform, nano-tips, which results in a uniform distribution of electric field among the nano-tips. Both laterally- and vertically-oriented field emitters have been implemented in a CMOS process for the first time, and the experimental results show stable operations of the integrated field emitters, with as small as ±1.8% standard deviation from the average current. Table 3.2 summarizes the characteristics of the three devices proposed in this work.

Table 3.2. Summarizing characteristics of three different devices investigated in this work.

Device number	CMOS technology	Nanowire orientation	Anode/cathode distance	Tip dimension	β	Lifetime current deviation
1	130nm Bulk	Vertical	17 μm	150 nm radius	5984	±4.1 % over 12 hours
2	130 nm Bulk	Lateral	320 nm	150 nm radius	779	±1.8 % over 12 hours
3	45 nm SOI	Lateral	110 nm	60 nm radius	454	±7.4 % over 1 hour

4. ENGINEERED CMOS SUBSTRATES

4.1 Introduction

Integrated circuits (ICs) play a major role in the modern electronically connected world. Basically, ICs are reshaping the interaction between human beings and their surroundings. Containing billions of transistors, ICs enable a wide range of applications such as data storage, transmission and processing. A broader range of capabilities, however, may be envisaged through the development of engineered substrates for ICs. Replacing the silicon substrate with another material or air, while still taking advantage of a single crystalline silicon active device layer enables novel functionalities and improved characteristics of ICs. Single crystalline silicon is the industry standard for transistor fabrication and offers high performance electronics with reliable fabrication techniques.

In order to replace or remove the silicon substrate, the wafer or chip goes through an exfoliation process. Several methodologies have been explored including chemical [91], mechanical [92], stress-controlled [27], [93] and epitaxial [94] exfoliation. One common technique relies on etching a sacrificial layer buried underneath a thin layer of active devices, followed by transferring the exfoliated layer to a different substrate. In this technique, first, photolithography is used to define device regions. Then the wafer is covered with a PECVD passivation layer, such as Si_3N_4, followed by a step of reactive ion etching (RIE) to open chemical access to the buried sacrificial layer. (111) silicon can serve as a sacrificial layer, as KOH or TMAH are suitable chemicals for etching it. The silicon dioxide in an SOI substrate can also be used [95], as it can be selectively etched by hydrofluoric acid. After the exfoliation process, an assembly of the layers is done to build the final structure. For this purpose, layers of two dimensional (2D) structures, such

as nanoribbons and nanomembranes, are generated individually through an exfoliation process on a separate donor substrate. The final device is shaped by the sequential transferring of the exfoliated layers to a host substrate. Although this technique has made key advancements in many applications [96], issues such as unpredictability of the transfer and limited applicability still remain unresolved [27], [31], [97], [98]. On the other hand, a number of research groups have explored novel approaches for transferring a fully processed device in one step [97], [99]. In this method, active components, such as transistors, and their metal interconnections are transferred all at once.

4.2   A Wideband RF Power Amplifier in 45 nm CMOS SOI Technology with Substrate Transferred to AlN

Advanced CMOS technologies have become attractive for implementation of power amplifiers, due to the availability of high-performance transistors and their high integration capability and low manufacturing cost. One of the challenges for integrating power amplifiers (PAs) into CMOS SOI technology is the self-heating phenomenon caused by high power dissipation in active transistors. As a result, the power gain of SOI-based PAs degrades with increasing output power due to the higher operating temperatures. Moreover, the parasitic capacitances of CMOS active and passive components on low resistivity SOI substrates cause a performance limitation in terms of device and circuit bandwidth and loss [100]. In stacked CMOS SOI PAs, parasitic capacitance leads to unwanted variations in voltage amplitude and phase, which imposes limitations on the overall output power and efficiency of PAs [100].

In this work a technique for transferring the device layer of CMOS SOI chips to an AlN substrate to improve PA power performance and efficiency is proposed. AlN offers higher thermal conductivity (285 $W.m^{-1}.K^{-1}$) than silicon (145 $W.m^{-1}.K^{-1}$), leading to better heat dissipation through the substrate. In addition, the semi-insulating characteristics of AlN, in contrast with the conductive characteristics of silicon, reduce the parasitic capacitances and loss of the devices and circuits on CMOS SOI technology. In order to validate this approach, first the heat dissipation though different substrates is studied using CAD simulation. Following these simulations, an RF power amplifier has

been designed and fabricated in the CMOS SOI platform. Next, substrate transfer to AlN has been performed and experimental results obtained from characterization of the PA before and after the substrate transfer are presented and compared. The design and characterization of the PA on both Si and AlN substrates have been done by another student.

4.2.1 CAD Simulation

In order to study the advantages of the substrate replacement, a heat transfer CAD simulation has been performed for power devices with different substrates. For the purpose of simulation, the electronic circuit is assumed to be a heat source with a power density of 0.33 ($\frac{mW}{(\mu m)^3}$). The effect of cooling by the top metallization (heat sink) is ignored because the layout of the proposed power amplifiers is large (contact pads are far from the active components). The chip is surrounded by air at room temperature. A Comsol simulation was conducted for the device under five different conditions: (i) with a bulk Silicon substrate; (ii) with an SOI substrate; (iii) with an AlN substrate in the presence of an intermediate SiO_2 layer (AlN/SiO_2 substrate); (iv) with an AlN/SiO_2 substrate in presence of an adhesive polymer; and (v) with AlN/SiO_2 substrate in presence of an air gap.

Figure 4.1(a) illustrates the temperature profiles as a function of distance across a cut in the middle of the device for these different substrates. As shown in the figure, a trend of large drop of the temperature profile after a peak is observed for all of the curves, except for the bulk silicon substrate (green curve). This peak temperature followed by a sudden drop is due to a ~150 nm buried SiO_2 layer in the CMOS SOI technology, which is characterized by a low thermal conductivity (1.4 $\frac{W}{m.K}$). According to the figure, using AlN as a substitute for Si (red curve) results in a smaller peak device temperature. Notice that the peak temperature is even lower than the bulk Si case, in which there is no buried oxide layer to block the heat transfer (green curve). Figure 4.1(b) depicts the temperature profiles as a function of the distance across a 100 μm cut through the substrates.

Figures 4.1(c,d) compare the color scale surface temperature profile between conditions (i) and (iii). The surface is produced by a cut in the middle of the device, from top to bottom. Although the buried oxide has blocked the heat in the left Figure (device with the AlN substrate), the maximum temperature remains below that of the device on the bulk Si substrate (right Figure). This difference is attributed to the high thermal conductivity of AlN ($285\frac{W}{m.K}$) in comparison with Silicon ($145 \frac{W}{m.K}$).

The fourth and fifth designs were studied as they represent the device under circumstances closer to the real experiment. Figure 4.1(e) depicts the substrate heat dissipation, in the presence of an air gap at the middle of the device, in comparison with the case where the gap does not exist (Figure 4.1(f)). The asymmetric lines in Figure 4.1(f) are the result of the air gap heat blocking at the center. The air gap of 50 μm wide and 100 nm thick is assumed to be at the middle of the device, between the SiO_2 layer and the AlN substrate. Overall, the study shows that SOI with the Si substrate exchanged with an Aluminum Nitride substrate is a good approach to achieve thermal dissipation through the substrate, and thus lower device temperatures.
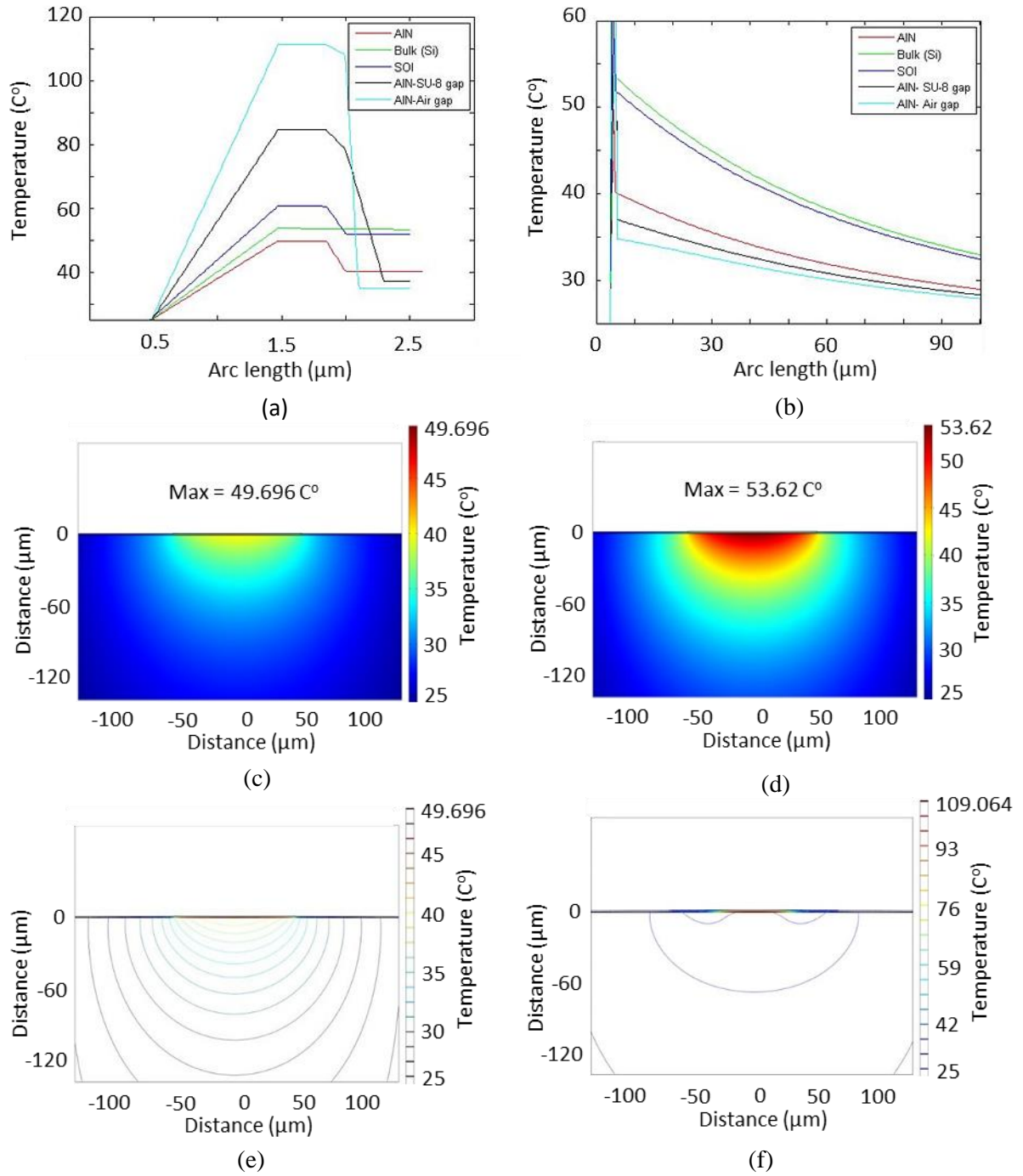
Figure 4.1. CAD simulation for devices with different substrates. (a,b) The temperature profiles as functions of distance across a cut in the middle of the device (a), and substrate (b). (c,d) The cross section color scale temperature profile for AlN substrate (a), and bulk Si substrate (b). (e,f) The substrate heat

distribution in the presence of an air gap (f), in comparison with the case with no air gap (e).

4.2.2   Power Amplifier Design

A wideband radio frequency power amplifier (RF PA) was designed and taped out by another group member, and fabricated in a standard 45 nm CMOS SOI technology. The circuit schematic of the proposed device is shown in Figure 4.2. The circuit consists of a stack of 16 low-breakdown-voltage transistors. Bypass capacitors (C_1 and C_2) are optimized to achieve stable and high gain operation. Resistors (R_1-R_3) are designed to prevent the gate-oxide breakdown of the transistors achieved by forming a feedback network to self-bias the transistors individually.
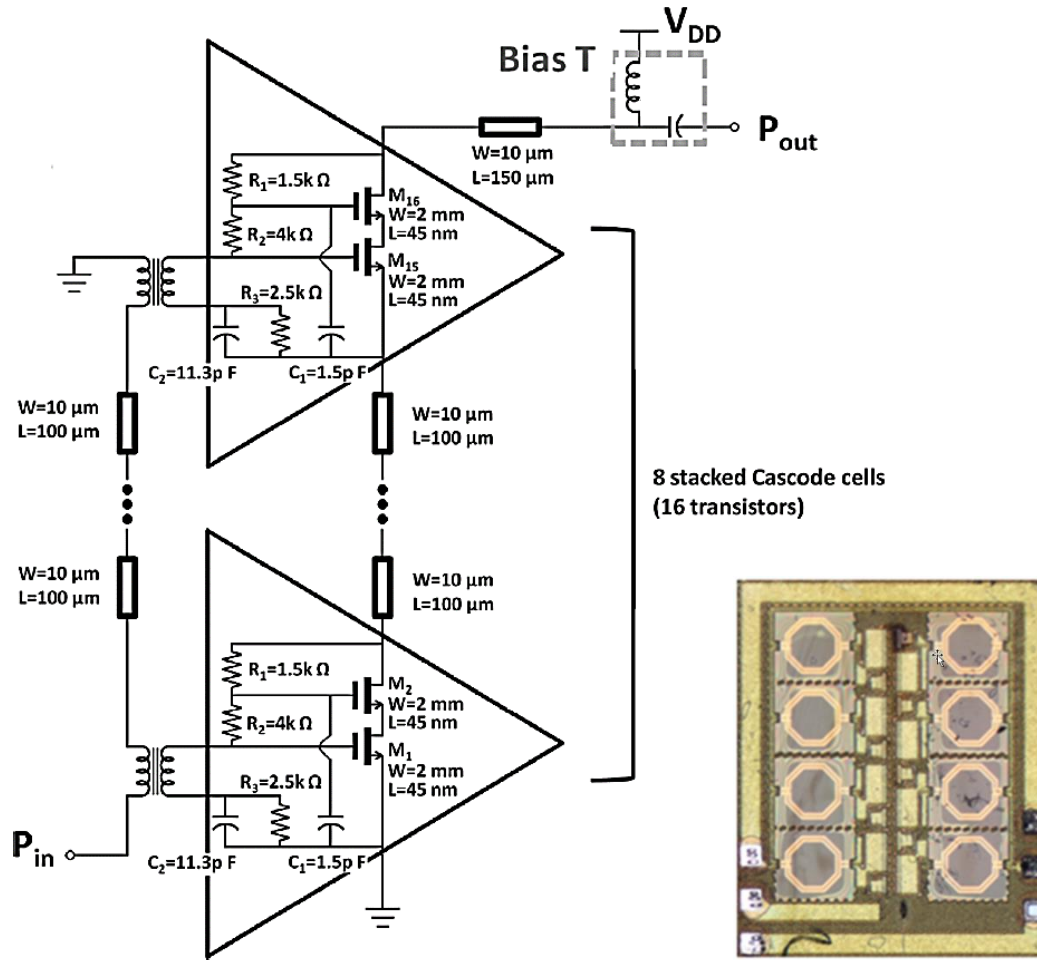
Figure 4.2. Circuit schematic for the proposed PA. The inset is an optical microscope image of the device after fabrication.

4.2.3 Transferring to AlN Substrate

The post-processing technology to transfer the device layers of SOI chips to an AlN substrate is shown in Figure 4.3, where no photolithography step is necessary (US patent [101]). The backside Si substrate is completely etched using a Xenon Difluoride XeF_2 silicon dry etching process with an etch rate of 5 μm/min at room temperature. The process does not generate plasma, which is a possible cause for transistor performance alteration during etching. The process also has high selectivity between the Si and silicon dioxide (1000:1 selectivity); hence, the etching stops at the SOI BOX layer. After the etching, the SOI flake with a thickness of 10 μm is bonded at 80 C^o to an AlN substrate

by applying a thin adhesive layer (100 nm) of polymethylmethacrylate (PMMA). No air gap between the thin SOI flake and the AlN substrate should be created during the bonding process. Figure 4.4 shows SOI flake in different steps of exfoliation, and after bonding to AlN substrate. The PA including its pads occupies a chip area of 1.2 mm^2. Details of the post-processing recipe are presented in Appendix A.3.
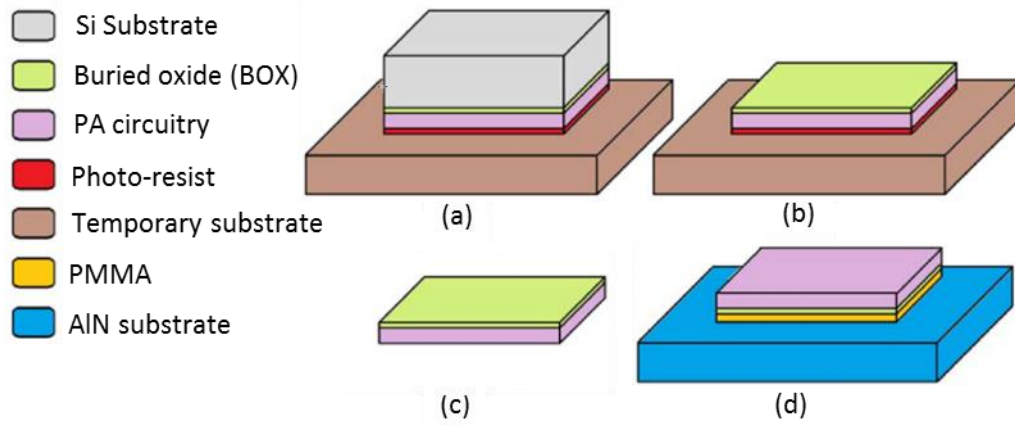
Figure 4.3. The post-processing steps for AlN substrate transfer. (a) Bonding the chip to a temporary substrate using photoresist. (b) Etching the backside silicon substrate using XeF$_2$. (c) Releasing the chip from the temporary substrate using acetone. (d) Bonding the chip to an AlN substrate using a thin adhesive PMMA layer on a heat plate at 80 ^{o}C.

After 30 minutes   After 40 minutes   After 50 minutes   After 60 minutes

(a)

CMOS flake
(10 µm thick)

(b)

(c)

AlN substrate

Exfoliated CMOS chip

S4800 15.0kV x220 SE(M)   200um

(c)
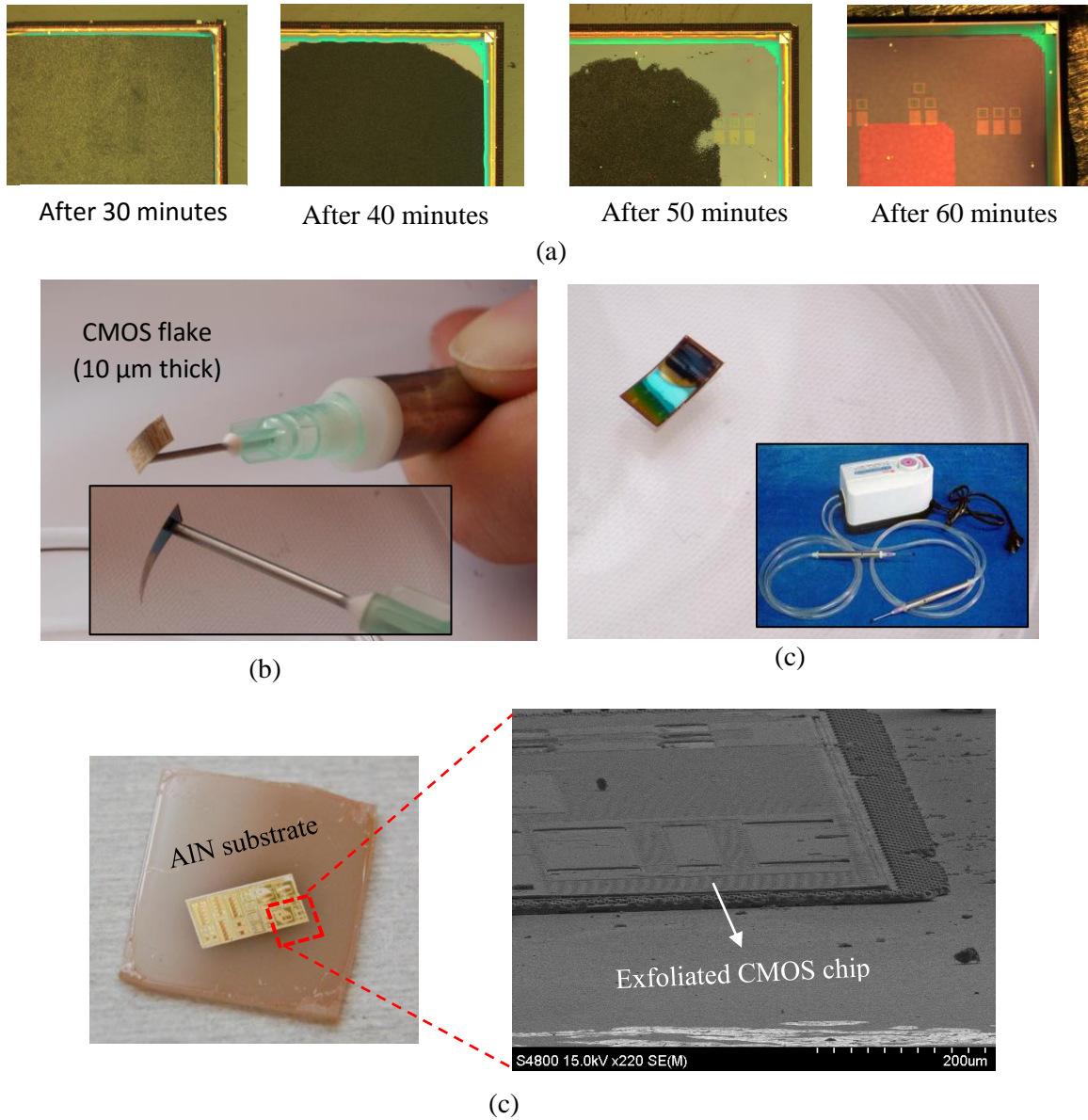
Figure 4.4. CMOS exfoliation and bonding to an AlN substrate. (a) An optical microscope micrograph of the back side of the chip in different steps of XeF_2 etching. The SOI buried oxide layer has been revealed completely in the right Figure. (b) 10 µm thick SOI. The left image shows the flake being handled using a vacuum tweezer. The right figure shows the flake as well as the vacuum tweezer setup. (c) The chip after transferring to AlN substrate.

4.2.4 Experimental Results

In order to validate the functionality of the CMOS circuits after post-processing, a 640 μm NMOS transistor with a finger width of 500 nm has been implemented as a test device. Figure 4.5a illustrates the I_d-V_{ds} characteristics of the test transistor before and after post-processing, which depicts a small change in the performance of the device. RF performance of the same transistor has also been measured, using a small-signal S-parameter measurement, setup which indicated no degradation in the functionality of the device.

Performance of the PA was also tested before and after the substrate transfer procedure (tests performed by another student). An Agilent E8361A network analyzer was used for small-signal S-parameter measurement. The short-open-load-through calibration was performed from 1 to 5 GHz. Figure 4.5(b) illustrates the experimental small-signal power gain of the PA after being transferred to the AlN substrate. Under a biasing voltage of 12 V and at 1.8 GHz, a power gain of 12.2 dB is achieved. Smaller I_d in lower biasing voltage (9 V) results in smaller power gain as illustrated in the figure.
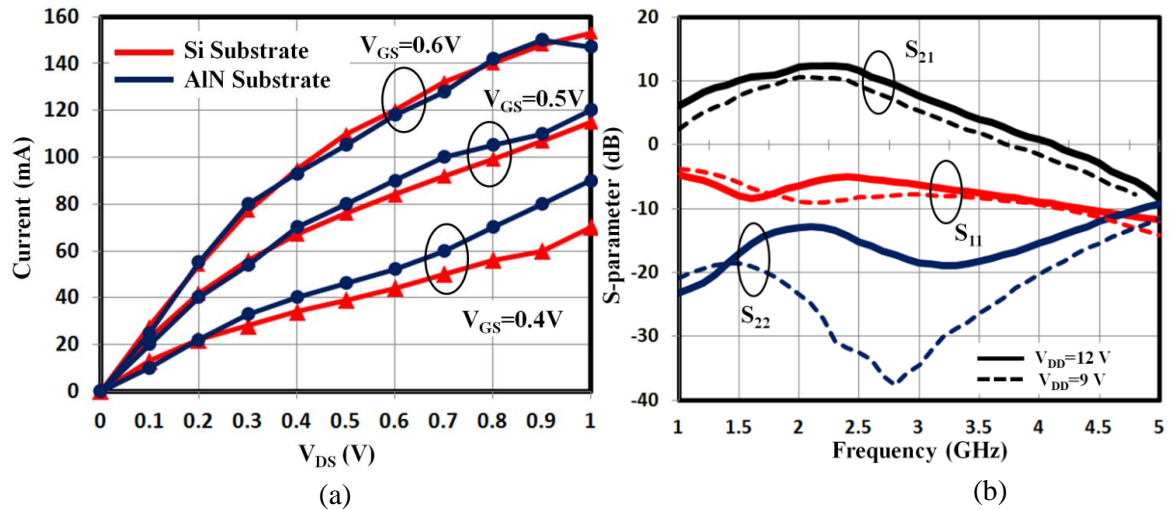
Figure 4.5. (a) The measured I_d versus V_{ds} characteristics of a transistor before and after transferring to AlN substrate. (b) The S-parameters experimental result of the PA, at different voltages of 9 and 12 V.

Large-signal performance of the PA has been evaluated for PAs with silicon and AlN substrates. In the measurement setup, an Agilent 83640L CW signal generator was used to provide the input power and an Agilent E4448A spectrum analyzer was used to measure the signal. The power measurement results (Figure 4.6) depict enhancement in both output power and power-added efficiency (PAE) after transferring to the AlN substrate. PEA can be calculated using equation 4.1 and describes the efficiency of a power amplifier by taking its gain into account.

$$\text{PAE} = 100 \cdot \frac{P_{(out-RF)} - P_{(in-RF)}}{P_{DC}} \tag{4.1}$$

Figure 4.7 compares saturated power P_{SAT}, linear power P_{1dB} and peak PAE as functions of sweeping voltage for PAs with and without transferred substrate (P_{1dB} is the output power when the amplifier is at the 1 dB compression point and P_{SAT} is the output power when the amplifier is saturated.) P_{SAT}, P_{1dB} and peak PAE versus frequency have also been measured from 1.5 to 2.6 GHz (Figure 4.8) for both Si and AlN substrates. The PA on the AlN substrate shows values above 27.9 dBm for P_{SAT}, above 24.8 dBm for P_{1dB} and above 20% for peak PAE. According to Figures 4.6, 4.7 and 4.8 the amplifier with an AlN substrate depicts enhanced performance due to a reduction of parasitic capacitances in the amplifier circuit aided by the substrate transfer technology.

A wideband code-division multiple-access (WCDMA) signal with a chip rate of 3.84 Mcps (Agilent E4433B) was used to measure the power amplifier. Figure 4.9 compares the measured adjacent channel leakage ratio (ACLR) for both PAs with Si and AlN substrates. This figure indicates an improvement in linearity after Si substrate is replaced by AlN substrate.
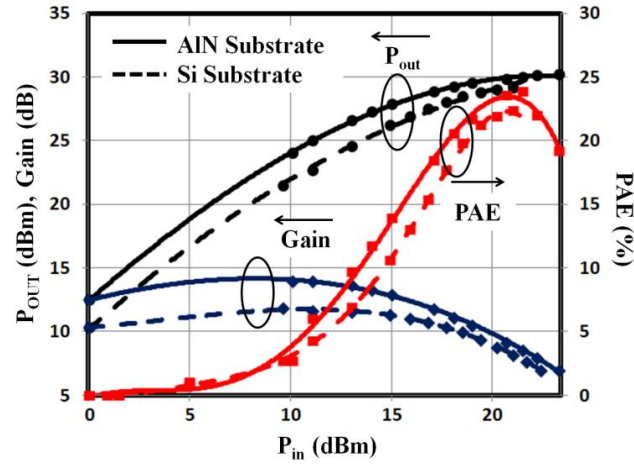
Figure 4.6. Experimental results comparing P_{SAT}, P_{1dB} and the peak PAE at different input power at 1.8 GHz, for the Si and AlN substrates.
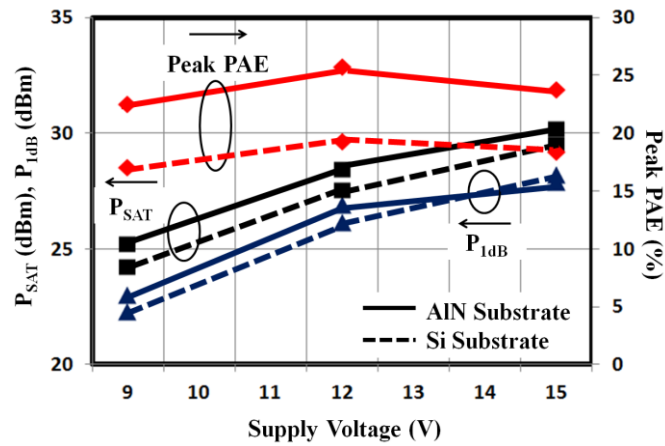
Figure 4.7. Experimental results comparing P_{SAT}, P_{1dB} and the peak PAE of the PAs under different supply voltages at 1.8 GHz, for the Si and AlN substrates.
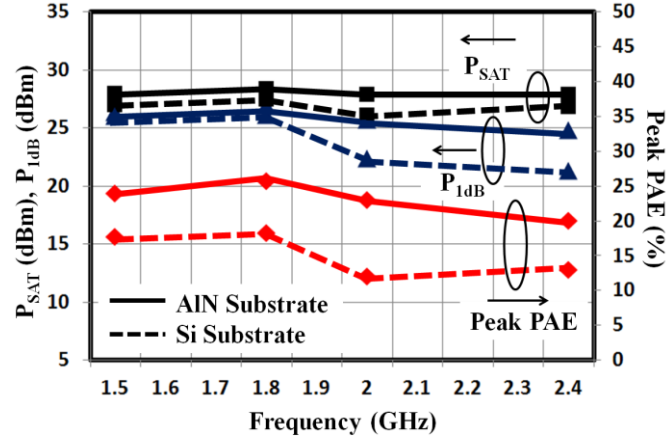
Figure 4.8. Experimental results comparing P_{SAT}, P_{1dB} and the peak PAE at various frequencies, for the Si and AlN substrates.
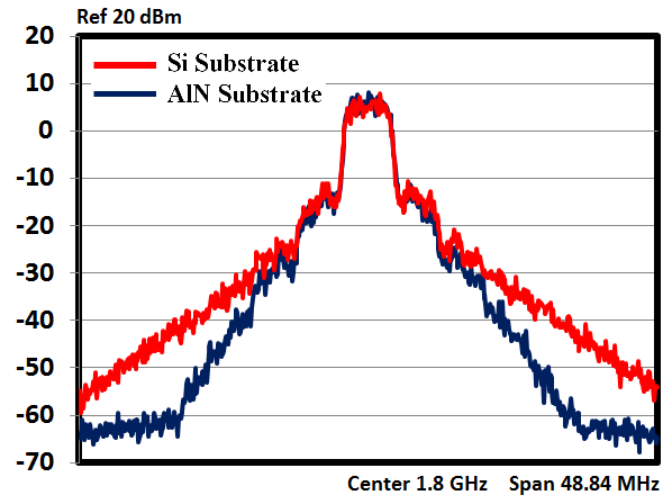
Figure 4.9. Experimental results comparing the WCDMA output spectra at 1.8 GHz, for the Si and AlN substrates.

4.2.5   Summary

In summary, a novel post processing approach is developed to enhance the performance of a CMOS SOI power amplifier. The approach is based on transferring the device layer onto an AlN substrate. CAD analysis is performed to simulate heat transfer through different substrate materials for the PA. The conductive silicon substrate of the CMOS chip, with prefabricated PA circuit on top, is etched and the device layer is

transferred to an AlN substrate to lower the parasitic elements of the circuit and improve thermal dissipation through the substrate. The improvement in the PA performance is validated by comparing small-signal power gain, saturated and linear output power and peak power-added efficiency of the PA before and after substrate transfer to AlN.

4.3   An Integrated Rectenna for Implantable Applications

Self-powered operation of micro/nano sensor systems can be achieved by taking advantage of integrated rectifiers and antennas (rectenna) that provide an electromagnetic energy harvesting platform. One of the most important applications for such integration is in implantable devices, where the integrated rectenna eliminates the necessity of surgeries for replacing the battery. On-chip integration of a rectenna enhances the device performance by eliminating external-to-chip parasitic elements. Moreover, it reduces the device size which is desirable for implantable devices. Integrated rectennas have been reported by several research groups [102]–[105], however, most are not suitable for implantable applications. Body tissues and muscles result in considerable attenuation to the transmitting signal, thus, imposing limitations to the optimal frequency band for device operation [104], [105].

Removing the silicon substrate of a rectenna results in enhanced device performance by increasing the equivalent resistance of the device at resonance. Moreover, the substrate removal enhances the transparency of the antenna on the chip to incoming EM waves from the back of the chip, leading to a rectenna that does not have a front or backside. In addition, higher power conversion efficiency PCE (generated dc power divided by incident EM power at the antenna) can be achieved due to better matching between the rectifier and the antenna. An integrated rectenna on a chip with removed Si substrate is compact and flexible, These characteristics are very desirable for an implantable device.

4.3.1   Rectenna Design

This project presents a novel post processing technique which results in the improved performance of a CMOS integrated rectenna. A standard 45 nm CMOS SOI

technology is used to integrate the device, and CMOS post-processing steps are developed to selectively remove the silicon substrate underneath the rectenna. A miniaturized antenna was first designed by another student [106] with an area of only 700 μm × 620 μm (0.43 mm^2) on the chip. The unloaded antenna is designed to resonate at 1.3 GHz. When connected to a full bridge rectifier circuit with a 20 KΩ load resistance, however, the antenna resonance shifted to a lower frequency of 0.95 GHz, providing about 1 V of dc voltage and 50 μW of dc power. This performance is achieved when the device is placed at 16 cm distance from a source with 36 dBm equivalent isotropically radiated power (EIRP) output. The rectifier design is based on a differential full wave rectifier as presented in [106]. The SOI process is used because of the advantages it offer in the post-processing step, described later in this section.

4.3.2   CAD Simulation

In order to study the effect of removing the silicon substrate on the performance of the antenna, Ansys HFSS simulations have been performed (simulation and optimization done by another student). The simulation was performed for a device with an overall area of 700 μm × 550 μm. Copper was chosen as the antenna metallization (electrical conductivity of 16.78 nΩ.m) and silicon was used as the substrate material (resistivity of 2.3 x 10^3 Ω.m). Figures 4(a, b) show the simulated reflection coefficient of the input impedance of the antenna from 0.5 to 3.5 GHz. The simulations show a resonance at 1.3 GHz. Figures 4.10(a,b) also illustrate the antenna measurement results before substrate removal, and compares it with the simulation results. Simulation shows a resonance frequency of 1.3 GHz with an impedance of 6.6 + j3.6 Ω, while measurement result shows a resonance frequency of 1.26 GHz with an impedance of 3.4 + j3.4 Ω. Small differences are possibly due to a variation in the conductivity of CMOS metal interconnections and loss tangent of the silicon substrate. Figure 4.10(c) illustrates the simulation results, comparing the antenna impedance before and after the substrate removal. The simulations show the resistance at resonance increases after the substrate removal (40.5 + j5.6 Ω), which is desirable for achieving better overall performance of the rectenna.
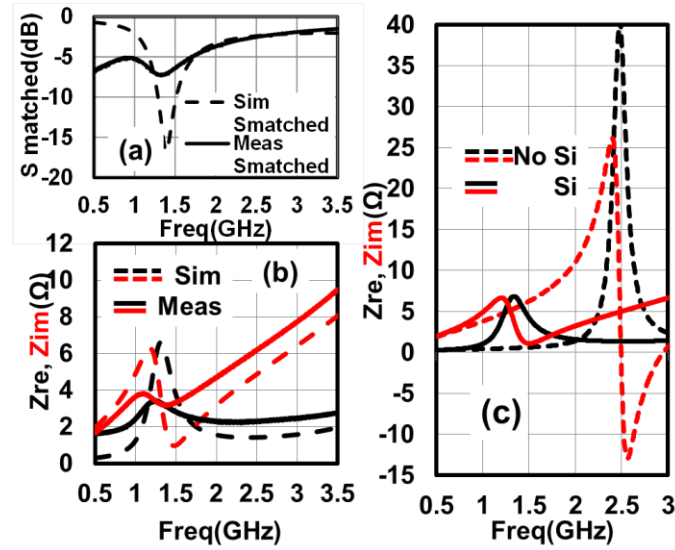
Figure 4.10. The measured and simulated (a) input reflection coefficient and real and imaginary impedance of the antenna at 6.6 Ω impedance environment. (c) The simulated antenna impedance with and without silicon substrate.

4.3.3 Si Substrate Removal

The developed integrated rectenna will become a part of a thinned down single-chiplet wireless implantable device, which does not require any contact pads since information and power flow in and out of the device, wirelessly. The rectenna test structure, on the other hand, requires testing pads. As it is impractical to probe or wirebond to test pads on a thinned CMOS SOI chiplet, one has to develop a technology to selectively remove the Si substrate under the antenna, while keeping the Si substrate elsewhere for mechanical rigidity. Therefore, a special processing technology has been developed to remove the substrate underneath the antenna after the device is wirebonded to a PCB.

Fabrication steps to selectively remove the Si substrate underneath the antenna are shown in Figure 4.11. Prior to the etching, the chip is attached and wirebonded to a punched PCB with a 1 mm hole drilled into it. Then a double-sided tape is applied to the PCB and is punched by a laser to make a through hole aligned with the PCB hole. Next,

the chip is bonded to the PCB, taking advantage of alignment marks generated in the laser-cutting step. The chip is then wirebonded and the module is placed upside down inside a holder setup made of Acrylic, which is an inert material in the etching environment. XeF_2 gas is used to etch the exposed silicon substrate through the punched hole. The SOI buried oxide (BOX) layer serves as the etch stop that protects CMOS circuits from being attacked by XeF_2 gas. Also shown in Figure 4.12 are the front and back views of the chip after the substrate is selectively removed. The SOI process is used to allow selective Si substrate removal to achieve a thin antenna layer with a total thickness of about 10 μm [8]. Details of the post-processing recipe are presented in Appendix A.4.
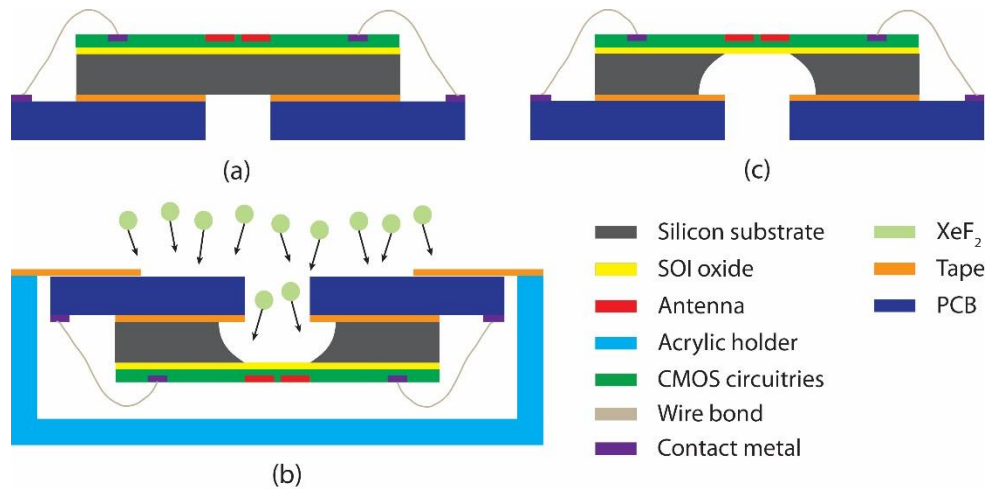
Figure 4.11. Post-processing steps to selectively remove the Si substrate under the rectenna. (a) Aligning and bonding the CMOS chip onto a punched PCB. (b) The chip with sidewall protection being etched in a XeF_2 setup. (c) The chip after selective etching of the substrate, targeting the region underneath the antenna.
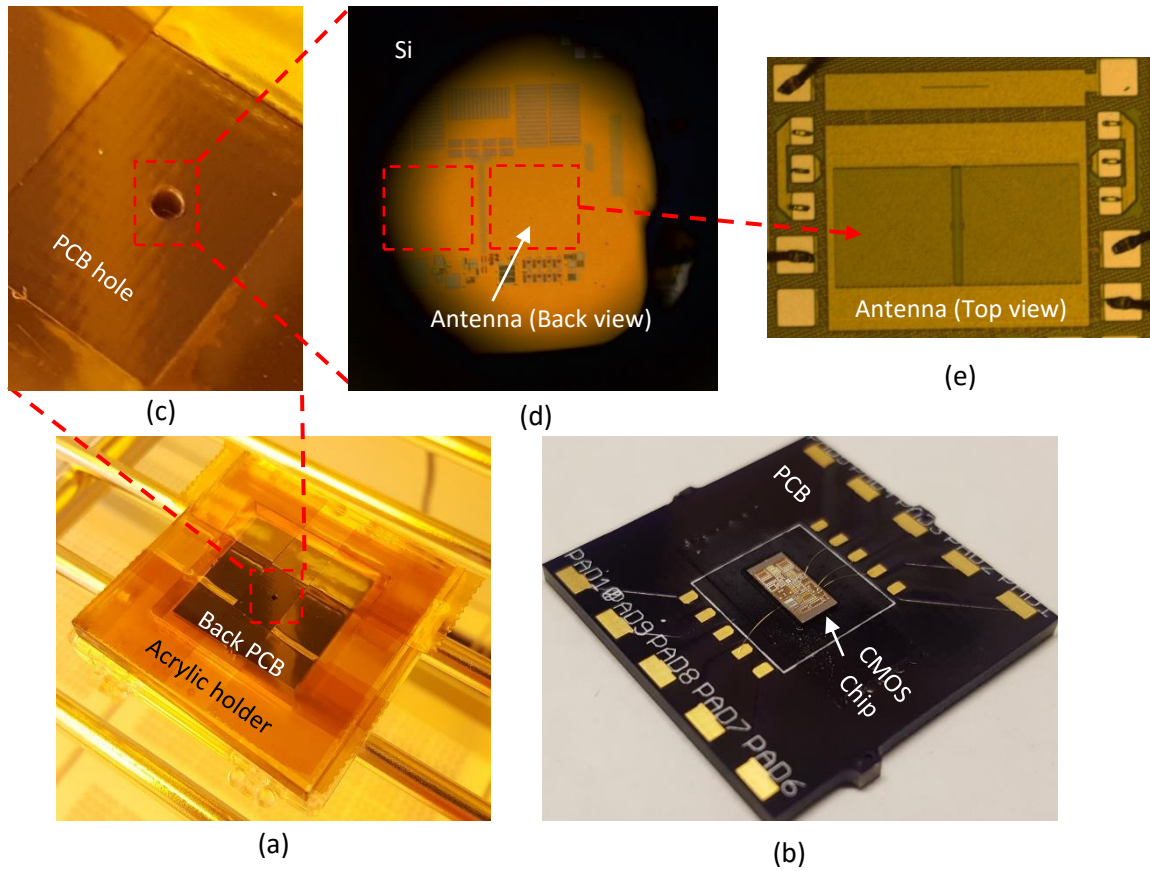
Figure 4.12. An illustration of the experimental chip during and after post-processing. (a) The PCB mounted inside the acrylic holder and secured/sealed by tape. (b) The chip wirebonded on the punched PCB. (c) A drilled hole through PCB. (d,e) An optical microscope image showing back and front views of the Si chip, with the back view showing the etched region under the antenna.

4.3.4 Experimental Results

The measurement of the antenna was performed using a Keysight E8361A PNA by another student. Figure 4.13 compares the performance of the device on low- and high-resistivity silicon substrates, as well as a device without a silicon substrate. In the measurement setup, a transmitting horn antenna is brought into the vicinity of the rectenna and the measurements are conducted with a power amplifier at an output power

of 30 dBm (36 EIRP). The presented rectenna is a part of an RFID circuit, therefore the measurement depicts higher load current compared to a single rectenna design.

According to Figure 4.13, the rectenna on the low-resistivity substrate resonates at 1170 MHz (peak voltage of 0.07 V) while the one with high-resistivity Si substrate resonates at 910 MHz (peak voltage of 0.11 V). The shift in the resonance frequencies compared to the simulation values are probably because of the capacitive load facing the antenna (as a result of utilizing modulator/demodulator circuits in the design). The rectenna with removed substrate depicts the highest rectified output voltage, compared to the other two designs, with a peak voltage of 0.33 V at 1260 MHz. Although it offers a slight shift in the resonance frequency, substrate removal of the rectenna seems to boost the rectified output voltage up to 470% compared to the design with low-resistivity silicon substrate (300% compared to high-resistivity silicon substrate).
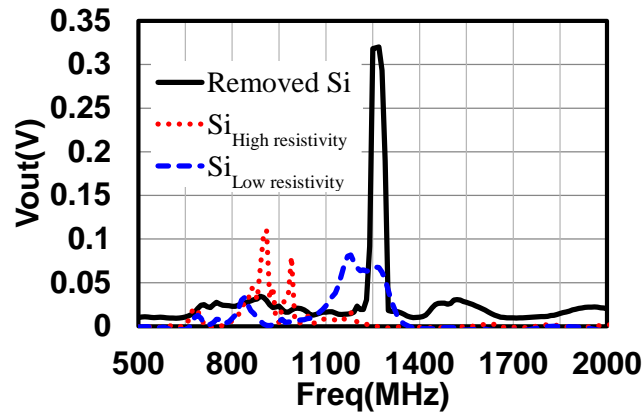
Figure 4.13. The measured rectenna performance on low- and high-resistivity silicon substrates, and no substrate. The output voltage of a rectenna as part of an RFID system is measured from 500 MHz to 2000 MHz with a 36 dBm EIRP source. The rectenna is part of the whole RFID/sensor system design for this measurement.

The proposed rectenna will be part of an implantable device, which requires flexibility to adapt to the curved and pulsating tissues inside the body. The presented work illustrates the effect of removing the silicon substrate in improving the electrical

performance of the rectenna. For the complete integrated sensor/RFID system, the entire silicon substrate will be removed, leading to a single flexible and thin chiplet suitable for implantable electronics as shown in Figure 4.14.
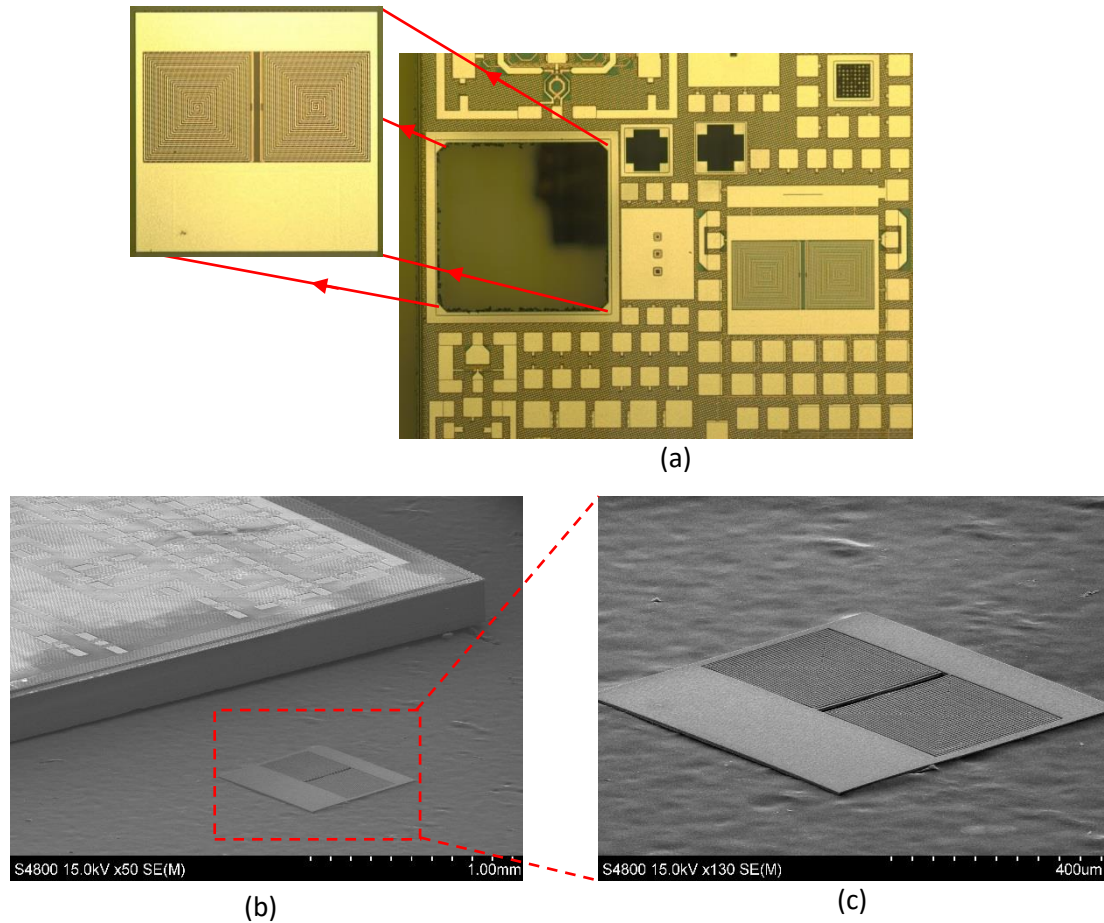
Figure 4.14. (a) Optical microscope image illustrating the original CMOS chip in the absence of the thinned down RFID dielet. (b,c) SEM images illustrating thinned down RFID dielet and the original CMOS chip with 400 μm thick silicon substrate.

4.4   Potential Applications

Proposed exfoliation techniques may provide pathways to future development of next generation flexible and wearable electronics. Figure 4.15 demonstrates an exfoliated CMOS chips for flexible electronic applications. By taking advantage of the proposed

post-processing techniques in this chapter, single crystalline silicon can be adopted for flexible electronics. In contrast with organic based flexible electronics, single crystalline silicon offers high performance reliable devices mainly due to the mature standard CMOS processing technology. Moreover, the proposed technology can potentially find applications in the 3D integration of electronic circuits [93]. In this case, stacks of circuits can be sequentially integrated on top of each other to increase device density [107].
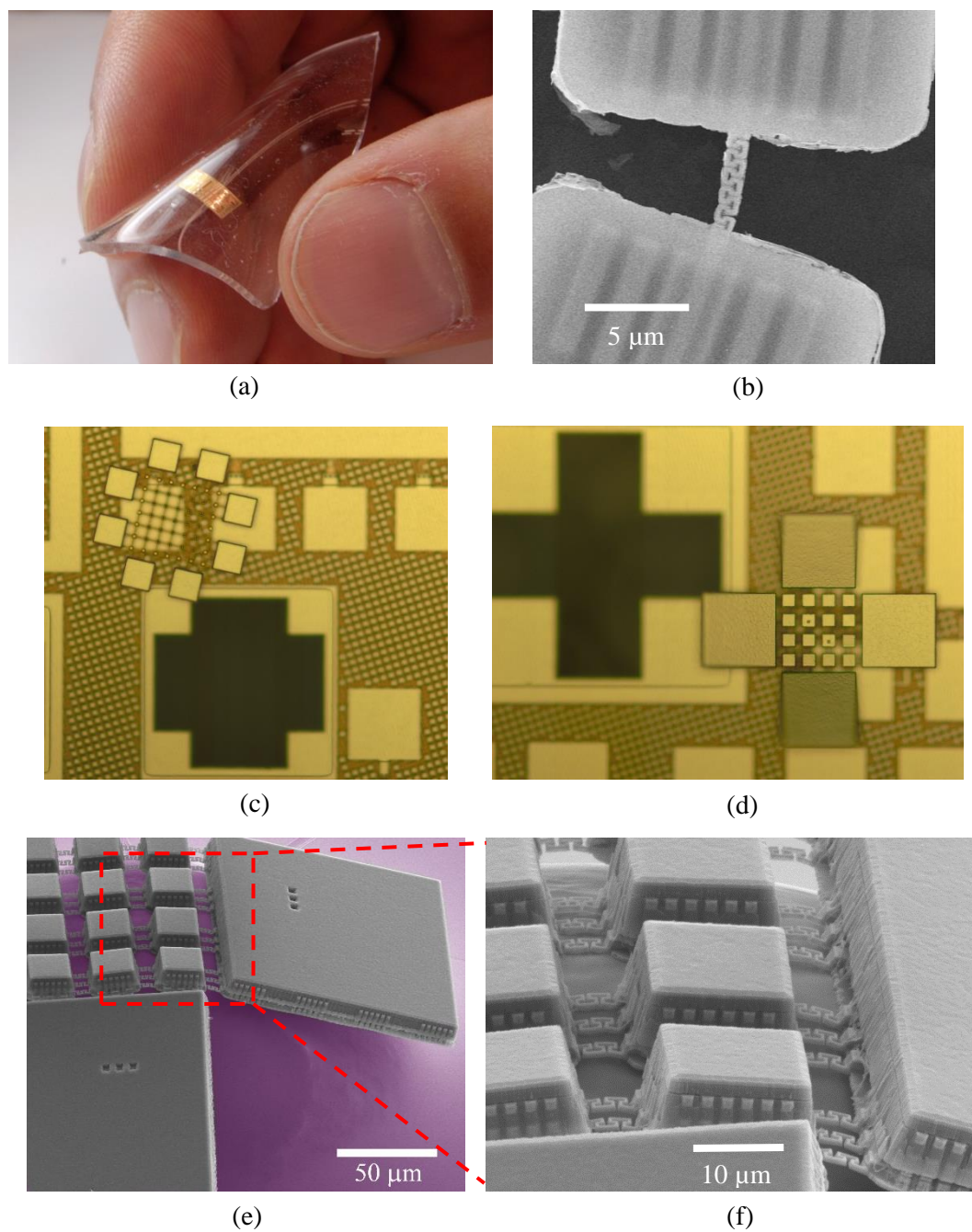
Figure 4.15. CMOS substrate exfoliation for flexible electronic applications. (a) A bended SOI flake after exfoliation. (b,c,d,e,f) Ultra-thin flexible CMOS microelectrode arrays with flexible nano features. (c,d) The MEA df after exfoliation and detachment from the donor CMOS chip. (e,f) The MEA manipulated on a micron scale curvature surface.

4.5   Summary

In summary, this research has demonstrated new approaches to produce high-performance CMOS-based devices by selectively or completely removing the chip substrate. The post-processing did not damage the prefabricated circuits on top of the chip and the device performance improved after replacing/removing the substrate. In the first project, a fully-integrated wideband power amplifier was implemented in a standard 45 nm CMOS SOI technology. Using a post-processing technology, the Si substrate was substituted by an AlN substrate to eliminate the effects of parasitic capacitances and further improve the PA performance, including its output power, efficiency, and linearity. In the second project, a miniaturized integrated rectenna, with an area of 0.43 mm^2, was implemented in a standard 45 nm CMOS SOI platform. Rectenna performances on low and high resistivity substrate and no substrate were compared, where the device with no substrate outperformed its counterparts on Si substrate.

5. DEVELOPED POST-PROCESSING TECHNIQUES

5.1 Post-processing Technologies for Integrated CMOS-Fluid Channels with Applications in Detecting Biomolecules

5.1.1 Introduction

In this section integration technologies that may lead to systems suitable for sensing, detecting, classifying, and analyzing single biomolecules, RNAs, DNAs, single cells and viruses [108], [109] are presented. A variety of techniques have been developed for single-biomolecule detection such as mass spectroscopy [110], surface-enhanced Raman spectroscopy [111], patch clamp [112], optical and fluorescence microscopy [113], atomic force microscopy [114], nanoresonator based detection [115], [116], and chemical and biochemical reaction based detection [109]. Technologies based on the electrical characterization of biomolecules have been a point of attention in recent years. A nano-pore technology, which is based on an ionic current blocking method through a very narrow pore with diameters on the order of a few nm, has been investigated in recent years [117]. In this method, an ionic current in the nano-pore, composed of free ions in the solution, is blocked by a biomolecule such as a DNA as it translocates through the nano-pore. The blockage current duration is proportional to the length of the biomolecule, which enables the bio-molecule classification. Current-blockage measurements, however, do not work across nanochannels as the current is limited by the largest biomolecule inside the nanochannel. Transverse sensing electrodes across the channel walls have been proposed as a method to detect DNAs inside these nanochannels

[118]. High-frequency electrical characterization in fluidic nanochannels provides valuable information about both conductance and dielectric properties of the biomolecule inside the nanochannel.

5.1.2   Motivation

CMOS integration may offer several advantages to the proposed nanochannel technology with transverse electrodes mentioned above. First of all, noise is one of the main problems in these devices with the traditional solution to reduce the noise based on the averaging of several data points, which leads to slow measurements [119]. CMOS integration reduces the noise leading to less averaging required and hence boosting the measurement speed. Secondly, system integration is an inevitable fact in order to enhance the measurement performance including noise and bandwidth of the current biosensors. Third, the fabrication reproducibility achieved by CMOS standard processing leverages a well-established process of the sensors, and leads to a step closer to commercialization and the consumer market. Fourth, the integration of all components of such a complex sensor in one IC leads to a more compact and user-friendly device. Fifth, CMOS integration enables simultaneous and multi-channel measurements on thousands of biomolecules at the same time. There is no need for external optical, mechanical and electronic equipment on the electrical sensing method. As a result, multiple parallel fluidic nanochannels can be measured at the same time, for which the massive data can be handled digitally on the CMOS chip.

Techniques to integrate six different micro- and nanochannel devices have been presented (herein referred to devices number one to six) as shown in Table 5.1. The fabrication of both vertical and horizontal fluidic channels has been investigated. Also, channel openings ranging from nano-scale to micro-scale dimensions have been demonstrated. Three main post-processing methods have been used to fabricate the presented fluid channels: (i) Plasma-based post-processing; (ii) Acid-based post-processing; and (iii) FIB-based post-processing. Details of these post-processing recipes for both vertical and lateral channels have been presented in Appendices A.5 and A.6. In the following section, the fabrication procedures of different sensors are discussed.

5.1.3   Sensors based on Transverse Electrodes across the Channel

In device number 1 (refer to Table 5.1 below), a horizontal microchannel has been fabricated in a standard 45 nm CMOS SOI technology. The length of the micro-fluidic channel in this device is 100 μm, and the height and width are set to 2.1 μm and 3 μm, respectively, due to the pre-determined dimensions and rules in this CMOS technology. Figure 5.1(c) illustrates the SEM image of the device. The post-processing technology is based on the wet etching of metals to open the fluidic channel. Designed CMOS metallization and vias are etched using a combination of heated (60 ^{o}C) water and Nitric acid ($H_2O:HNO_3$) with 1:5 volume ratio, followed by a drying step on an 80 ^{o}C hot plate. For future applications, both conductive and capacitive transverse electrodes may be designed along the channel. The conductive electrodes are the ones that measure conductance and come in contact with the fluid within the channel. They are also connected to the gate of an NMOS transistor, in order to evaluate the functionality of the electrical components after post-processing. Moreover, the transistor can serve as a simple amplifier for the proof-of-concept demonstration. Figure 5.1(a) illustrates the Cadence layout design of the sensor.
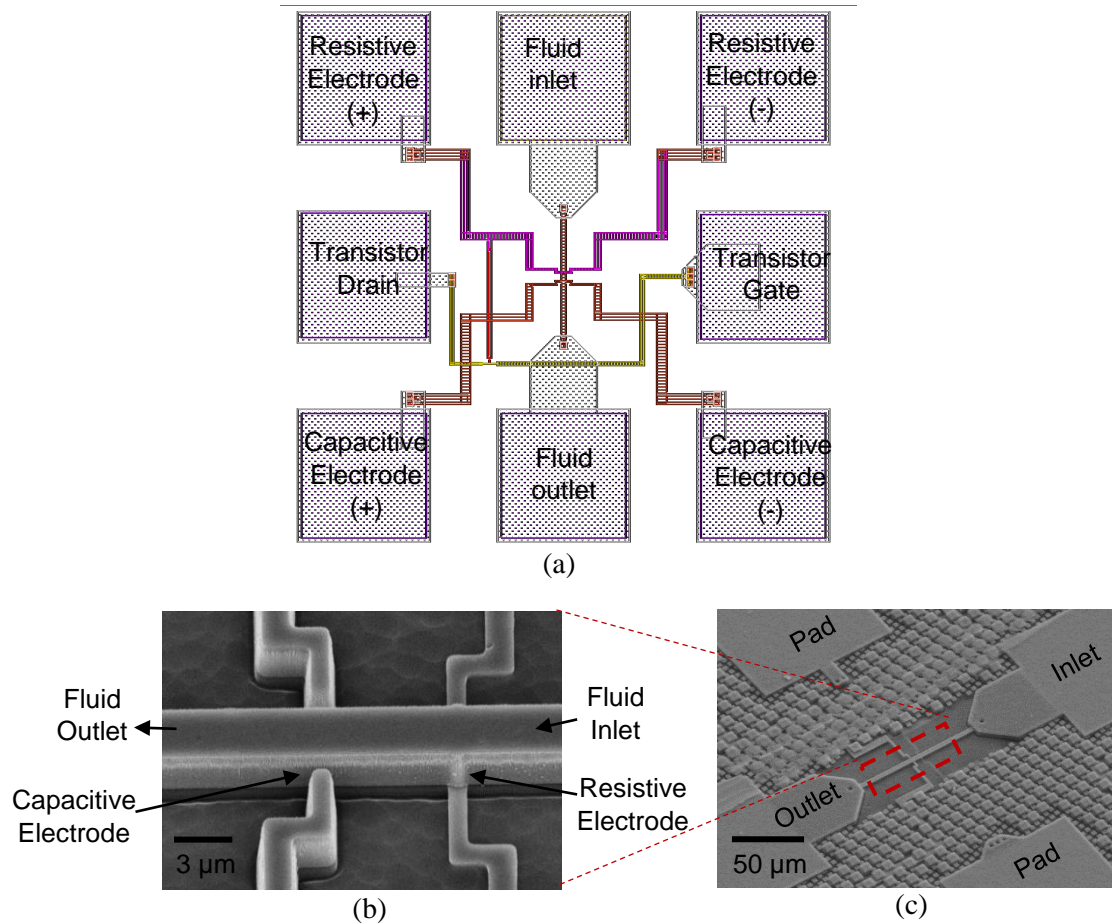
Figure 5.1. Device number 1 (horizontal microchannel): (a) A cadence layout of the horizontal microchannel (b) An optical microscope image of the device after the foundry fabrication and before post-processing. (c) An SEM image of the device after CMOS post-processing, illustrating the channel, transverse electrodes and pads.

In device number 2, a through vertical microchannel has been formed on the CMOS device layer. An opening on the chip substrate was designed to pass the flow vertically through the chip. The channel dimensions are designed according to a typical cell size in mind, with a cross section of 20 μm × 25 μm and a length of 11 μm. Figure 5.2(b) illustrates an SEM image of the channel during the post-processing. Four different transverse micro-electrodes are designed across the channel that will be utilized for measuring the impedance of a single cell that flows through the fluidic channel. As

shown in Fig. 40(b), two electrodes are located on the left and right of the image and two are located at the bottom of the image. Electrodes 3 and 4 are on top of each other. Movement direction and velocity may be controlled by applying control voltages to transverse metal electrodes close to the top of the fluidic channel. To perform post-processing of the CMOS-SOI chips, small openings in the Polyimide and Aluminum layers are designed. A two step post-processing technology that consists of a top processing to define the electrodes and opening in the device layer (Figure 5.2(b)) and a back processing to gain access to the channel from the chip substrate (Figure 5.2(c)) are utilized to make the fluidic channel. The top processing is based on plasma anisotropic etching and the back processing is based on XeF_2 isotropic silicon etching. The SOI buried oxide (box) layer serves as the etch stop in the back processing. The device is equipped with an on-chip amplifier illustrated in Figure 5.2(a).
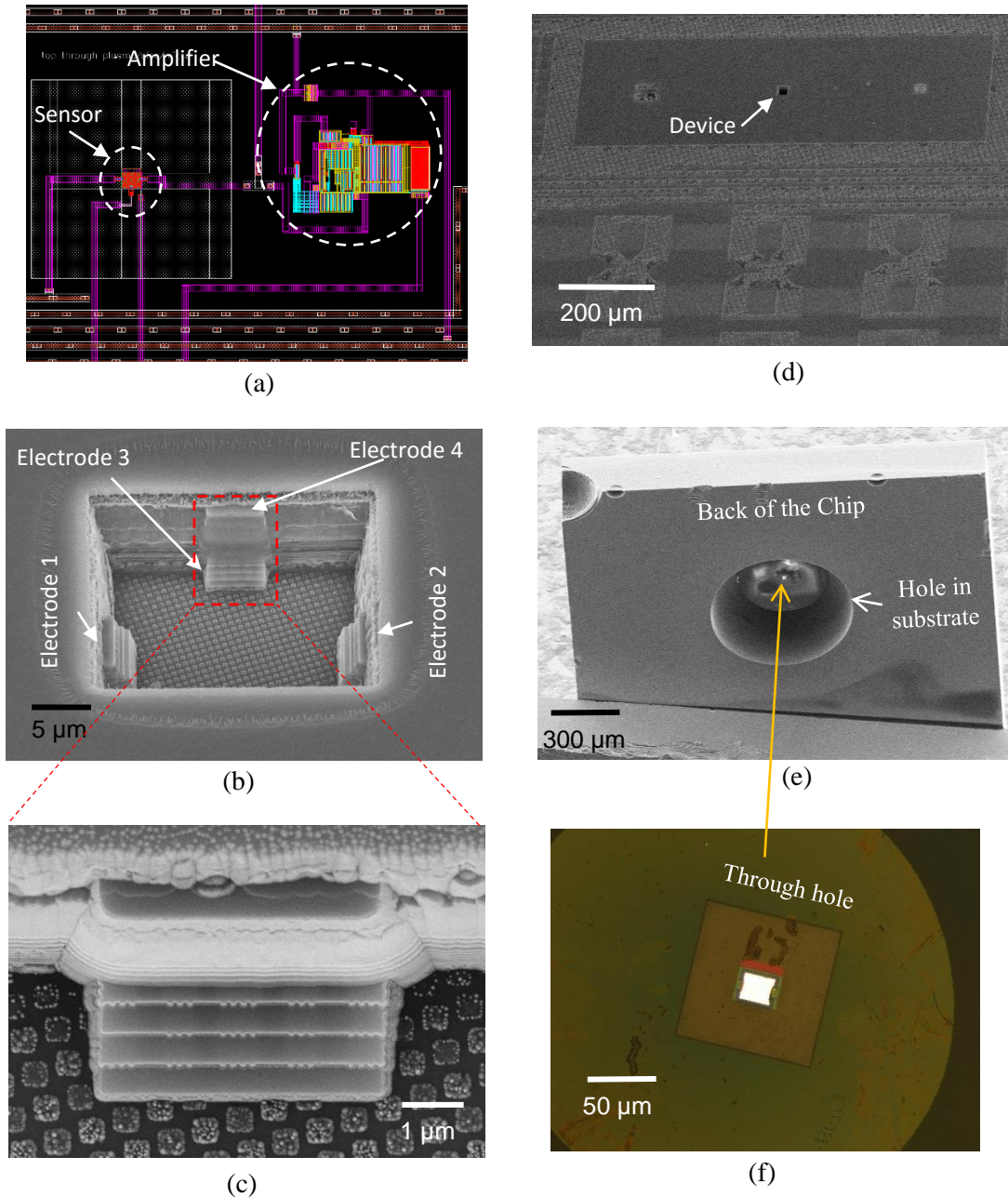
Figure 5.2. Device number 2 (vertical microchannel): (a) A cadence layout of the device illustrating the channel and the integrated amplifier a few microns away from the electrodes. (b,c) SEM image of the channel after the top post-processing and before back-chip post-processing. (d,e,f) Optical & SEM microscope images illustrating the channel through the CMOS chip after all of the post-processing.

One of the difficulties in the fabrication of a fluidic sensor is the need for both electrical and fluid packaging of the device. The fluidic packaging requires inlets and outlets to the micro/nano channels to and from a fluidic environment under test. At the same time, wires and interconnects have to be routed out of the pads on the chip to facilitate the electrical readout of the sensors. As the distance between the channel and the electrical pads are only in the order of several hundred μm, the electrical/fluidic co-packaging becomes extremely challenging. To solve this problem, a 3D printed packaging technique as illustrated in Figure 5.3(a) was proposed. In this packaging, the chip is sandwiched between layers of 3D printed caps, with defined openings for fluid and electrical connections. A thin layer of polymer sheet surrounds the chip to serve as a spacer, and to reduce stress on the chip. Layers are then screwed together using miniature screws. The packaged chip is then bounded to a punched PCB and wirebonded to make the required electrical connections. Figure 5.3(b) illustrates the packaged and wirebonded chip on a punched PCB. Figure 5.3(c) illustrates the setup, which was built for the alignment of the syringe inlet/outlet to the PCB board.
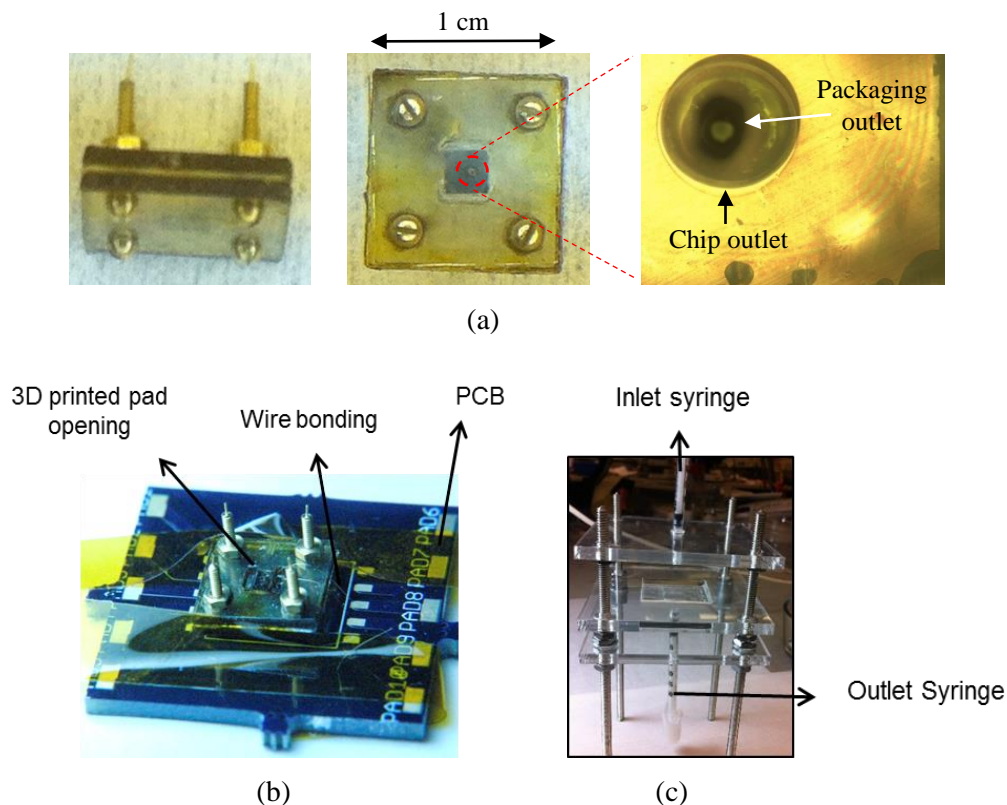
Figure 5.3. Packaging: (a) The 3D printed packaging caps with built-in opening designed for flow and electrical connections. (b) The packed chip wirebonded on PCB. (c) The customized setup for fluid inlet and outlet alignments. This was also used for preventing the device layer to break due to unwanted micrometer movements of inlets and outlets.

In device number 3, a vertical nanochannel has been fabricated using a plasma etching technique. As a demonstration for potential application, Figure 5.4(c) illustrates the schematic of the transverse electrodes designed for this device. The measured current between the two nanoelectrodes that are across from each other depends on both the conductance and the capacitance of the fluidic media in the channel and the biological mediator translocating in the channel. Figures 5.4(a) illustrates the transistor level schematic of the integrated amplifier, located about 50 µm from the electrodes. Note that the amplifier design carried out by another student and is based on a current-mirror wide-swing Operational amplifier and achieves a simulated voltage gain of ~30 dB. The

amplifier operates at up to 500 KHz to capture the high-frequency signals associated with fast transitions of the biomolecules in the nanochannel. The value of the parasitic capacitance from the sensing electrodes to the input of the amplifier in the proposed device is ~ 10 fF, which is considered much lower than competing technologies such as the non-integrated patch-clamp amplifiers with several pF input capacitance. Extremely small (~10 fF) parasitic capacitance leads to low undesired signal couplings and low RC time constants (wide measurement bandwidth).

Figure 5.4. Device number 3 (vertical nanochannel): (a) A transistor level schematic of the built-in amplifier. (b) Post-layout simulation results of the amplifier. (c) A schematic illustrating the multi-channel measurement concept. (d) An SEM image of the fabricated vertical channel on the CMOS chip.

Device number 4 utilizes a Focused Ion Beam (FIB) etching technique for the post-processing of the CMOS chip. The FIB has the capability to scan a focused beam of high energy ions on the surface of the target. Etching is achieved by attacking the substrate surface with high energy heavy ions. The first advantage offered by this technique is the ability to fabricate vertical nanochannels with lengths varying from ~2 μm to ~11 μm after the chips are fabricated by the foundry. Seven different pairs of electrodes are designed in different CMOS metallization levels, with different dimensions and thicknesses. Such a wide range of electrode dimensions facilitates customized post-processing according to the type and dimensions of biomolecules or cells under study. The second advantage of FIB post-processing is the excellent condition of probing pads after post-processing, since the ion beam is focused on the nanochannel during the fabrication and does not affect the pads. The sensor is integrated with an on-chip amplifier. Figure 5.5 illustrates an optical microscope image of the device and also the corresponding Cadence layout.
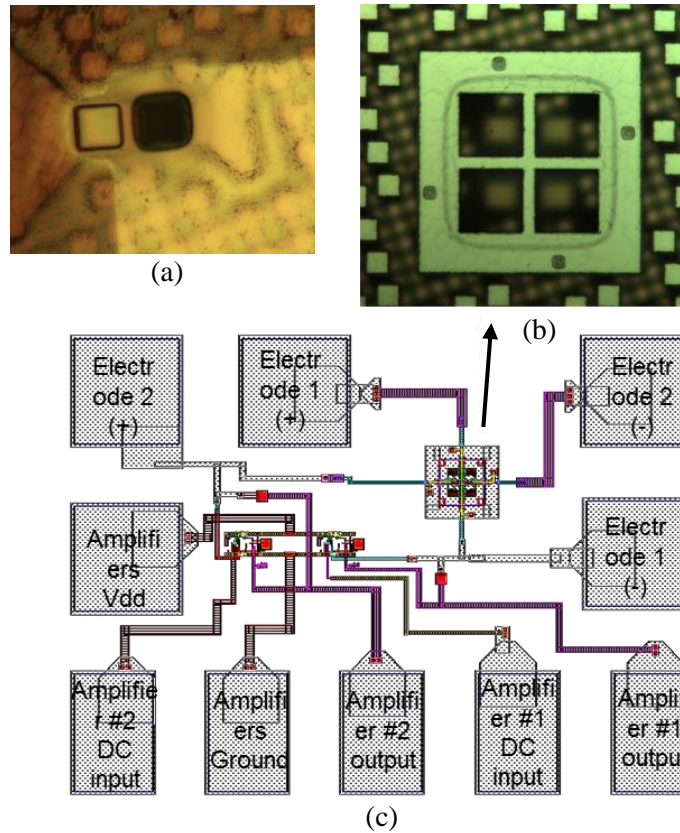
Figure 5.5. Device number 4 (FIB based vertical channel): (a) An optical microscope image of the channel fabricated using a FIB technique. (b) An optical microscope image of the device after the foundry fabrication and before post-processing. (c) The cadence layout of the device illustrating the device and the integrated amplifier 70 μm far from electrodes.

5.1.4   Sensors Based on Modulating a MOS Electrical Current

Device number 5 is a horizontal nanochannel, which has the potential to function based on sensing the electrical charges of a biomolecule passing over the gate of a nano-scale NMOS transistor. The critical dimension of 45 nm in this technology yields fluidic nanochannels with cross sections close to the dimensions of some viruses and virions. For the post-processing technology, first, large openings (100 μm × 100 μm) are fabricated using wet etching (or plasma etching) to serve as the flow inlet and outlet (illustrated in Figure 5.6). Then, the nanochannel (40 nm × 65 nm) is opened using polysilicon wet etching. Figure 5.6(c) illustrates the schematic of the device after fabrication. The

presumed operation of the device is discussed in the following. The etched polysilicon material will serve as the fluid nanochannel, immediately above the MOS transistor channel. Charged ions, inside the fluid, would modulate the current passing through the source and drain, leading to their detection. Furthermore, the device may takes advantage of additional integrated CMOS transistors to amplify the measured signal. Passing the fluid through the nanochannel, and the consequent measurements, have not been demonstrated for the presented device (Figure 5.6). However, the feasibility of passing fluid through a nanochannel has been demonstrated in our group (by another student) [118].
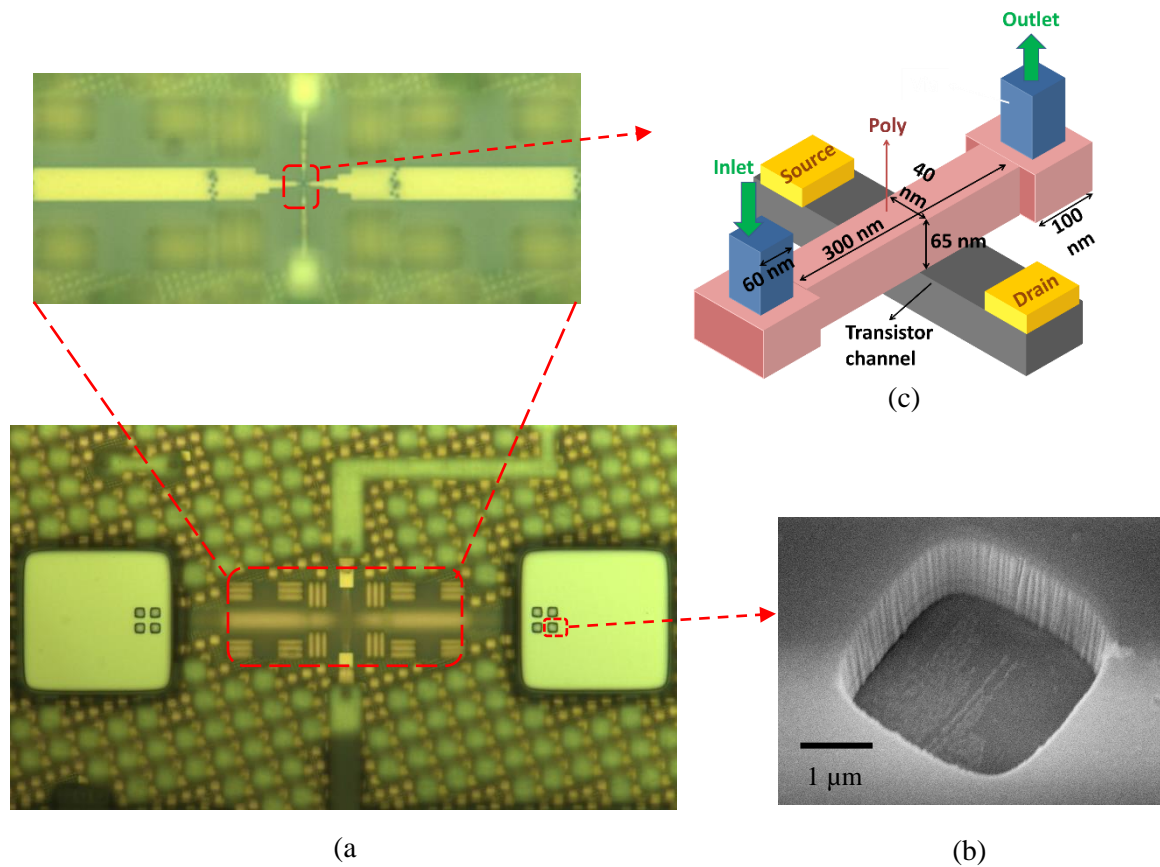
Figure 5.6. Device number 5 (MOS-based horizontal nanochannel) (a,b) Optical microscope and SEM images of the device after partial post-processing. (c) A schematic illustrating the function principal of the sensor.

Device number 6 has been designed based on a novel structure referred to as perforated MOS structure (US patent [120]). Figure 5.7(b) illustrates the SEM image of a 200 nm wide fluidic nanochannel post-processed with no additional lithographic steps. The fabrication of ~50 nm wide fluidic nanochannels are feasible using the same 45 nm technology. In the following, novelties of the design and potential applications of such device are discussed. CMOS technology offers a thin polysilicon layer and several layers of thin Copper metallization suitable for implementing sensing electrodes in the range of DNA biomolecule dimensions. Additionally, a very thin gate oxide layer (oxide between the poly-silicon gate and silicon channel) of about 1 nm is available in the technology. Figure 5.7 illustrates a schematic of the different layers used in this device. It is presumed that the current measured across the poly-silicon gate and the silicon device layer, when the electrical channel of the MOS structure is in an active region may be correlated to the sequence of a small segment of the biomolecule that transverses through this fluidic nanochannel device. CMOS technology enables thousands of such nanochannel devices to be built in an array on the same chip. High yield and very low fabrication cost are among the other advantages that CMOS offers in this technique. Moreover, the sense electrodes are directly connected to the inputs of the CMOS operational amplifiers with large transimpedance gains. Note that as long as the biomolecule is attached to the walls of the fluidic channel as it transverses through it, the biomolecule is "sensed" with no need for the channel opening to be in the range of the biomolecule cross section. Therefore, a standard CMOS process such as the one utilized here may be adopted for making the perforated MOS nanochannel structure.
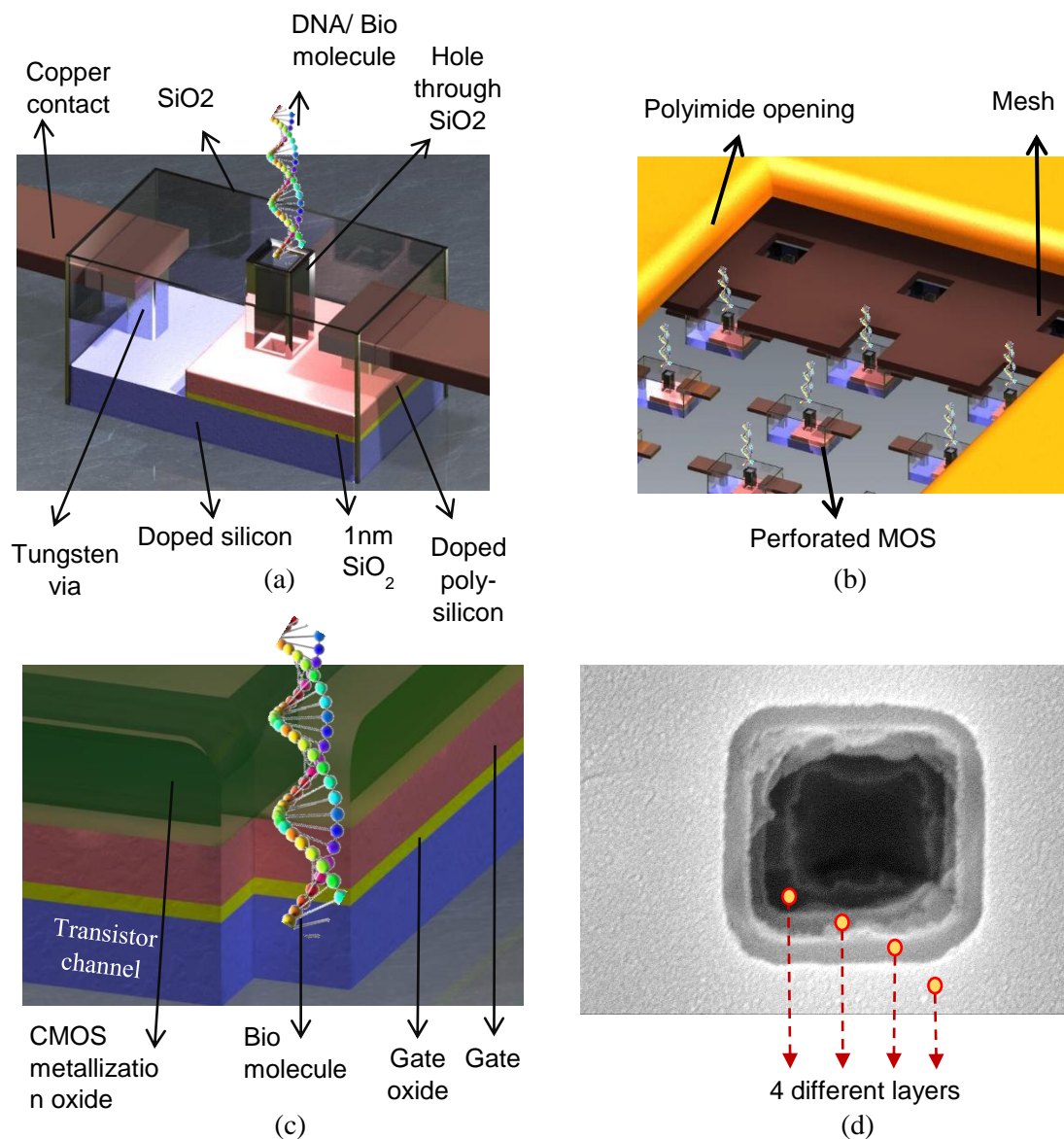
Figure 5.7. Device number 6 (Perforated MOS): (a,b) Array of nanochannel devices to be built with high yield and at a very low cost. (c) A schematic illustrating layers of CMOS used for DNA detection. (d) An SEM image of the CMOS post-processed nanochannel, illustrating four different layers.
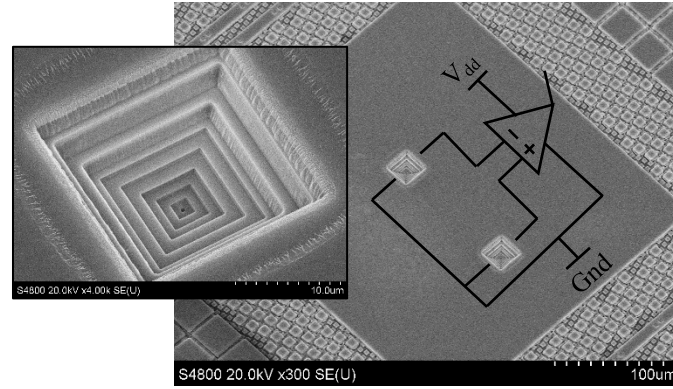
(a)
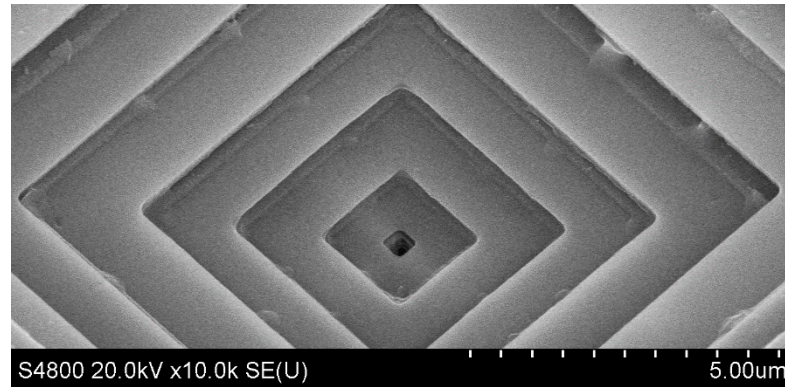
(b)

Figure 5.8. (a) An SEM image of a pair of perforated MOS sensors integrated with a differential amplifier. (b) An SEM image of the MOS sensor. The three-dimensional stepped structure are made utilizing different CMOS metal layers. This topology helps to achieve a fine nanochannel during post-processing.

5.1.5   Summary

In summary, fabrication technologies for integrated micro- and nano-fluidic have been presented. Such devices may potentially be used in sensor systems for the detection and analysis of cells, viruses and single-biomolecules. Six different fluidic channel designs based on different fabrication techniques and sensing methods have been fabricated for a variety of potential applications. The design parameters of the proposed devices are summarized in Table 5.1 The two main potential detection principles utilized in these devices are sensing based on CMOS integrated transverse electrodes and MOS-

based electrical charge detection. The layout design, post-processing and packaging steps are fulfilled successfully.

Table 5.1. Summarizing the six different devices fabricated in this project

Device Number	Dimension	Channel Orientation	Detection Technique	Post-processing Technique	On-chip Amplifier
1	micron scale	horizontal	transverse electrodes	acid based metal etching	transistor
2	micron scale	vertical	transverse electrodes	plasma anisotropic	yes
3	nano scale	vertical	transverse electrodes	plasma anisotropic	yes
4	micron and nano scale	vertical	transverse electrodes	FIB etching	yes
5	nano scale	horizontal	MOS detection	plasma and acid	yes
6	nano scale	vertical	MOS detection	plasma anisotropic	yes

5.2   Post-processing to Fabricate Nanoelectromechanical Resonators

5.2.1   Introduction

Integrating Micro-Electro-Mechanical-Systems (MEMS) devices fabricated on the same chip with CMOS transistors have already enabled various novel systems, such as on-chip driving, on-chip signal processing and closed-loop control systems [8]. Resonators, gyroscopes [8] and RF-MEMS capacitive switches [9] are examples of successful MEMS/CMOS integrated devices that have been commercialized. By further miniaturizing MEMS devices, researchers are targeting devices that are lighter, more compact, show better performance and are less costly [121]. As a result, Nano-Electro-Mechanical-Systems (NEMS) are playing a major role in advancing science and

technology today [121]. Ultra-sensitive mass sensors [122] and nano-scale oscillators [123],[124] are examples of such NEMS devices.

5.2.2 Motivation

Many advancements in nanofabrication technologies have been achieved in recent years. Nevertheless several challenges have to be addressed in order to bring NEMS to the consumer market. Reliable high-yield methods of fabrication can make this technology available to everyone. On the other hand, developing novel high-precision low noise instruments can help to further empower NEM devices by amplifying their weak output signals. NEMS-CMOS integration offers many advantages, which help overcome these challenges. The first advantage of the integration is the low levels of coupled noise, which leads to high signal-to-noise ratios. The second advantage of such integration is increased detection bandwidth (as discussed in Chapter 1). Higher production yield and lower fabrication cost are additional advantages of NEMS-CMOS integration [11]. The schematic shown in Figure 5.9 illustrates the NEMS-CMOS integration concept.
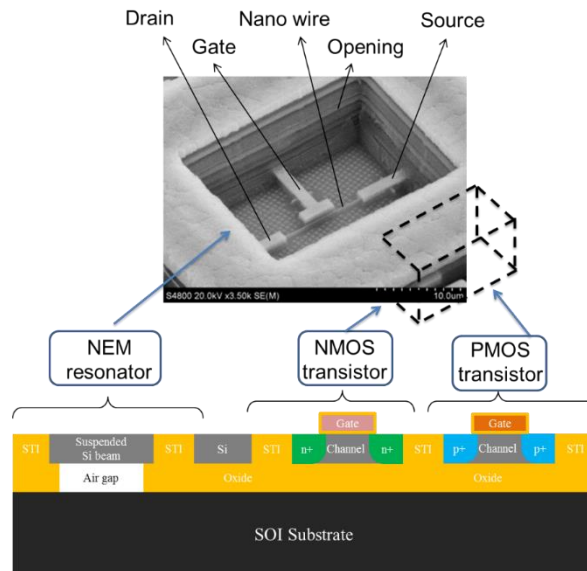
Figure 5.9. Side view schematics and SEM images of a suspended nanoresonator, illustrating the NEMS-CMOS integration concept.

In this work, post-processing of a standard 45 nm CMOS SOI chip has led to nano-scale beams integrated within the CMOS chip. In particular, this work explores different suspension techniques for NEM devices integrated in CMOS technology as summarized in Table 5.2. Most fabricated NEM devices consist of a suspended nanostructure, clamped on one or both ends. Releasing is considered to be one of the most critical steps. The very small dimensions of NEM devices emphasize new properties, such as van der Waals forces, which impose limitations to the suspension process. By choosing a suitable suspension recipe, the technology can be optimized for minimum degradation in both CMOS and NEMS devices. The following two factors plays a major role in developing suspension techniques for NEMS-CMOS integrated devices: First, no extra lithography steps are added to the CMOS process, which ensures the simplicity, reproducibility and high yield of the process. At the same time, the cost of the processing will be significantly lower and it can be done in a batch fabrication manner. Next, 100% dry etching processes should be used which further enhances the fabrication yield. In the following, three different materials, available in CMOS technology, have been investigated as sacrificial layers for the suspension purpose.

The general recipe to fabricate the presented devices consists of two major steps. First, an anisotropic dry etching is used to shape the nanostructure, using CMOS metal layers and a polyimide passivation layer, which serve as masks. Secondly, a time-controlled etching of the sacrificial layers is performed to release the beams. As a result, a suspended beam is formed on the Si device layer and/or metallization layer of a CMOS chip, and selective layers are used as sacrificial layers to release the beam. In the layout design, openings of about 20 μm × 20 μm are designed in the polyimide and top metal layers to expose only small sections of the chip to post-processing while masking the rest. This approach helps to protect the circuits and metallization layers that are designed next to and away from these openings (Figure 5.9). The resonance frequencies of these NEMS beams are set by the beam dimensions and the properties of the Si or metallization layers. Beam thickness and width, beam-substrate gap and beam-gate distance are among the important parameters that influence the device processing and behavior and are affected by the CMOS standard design rules. For example, the minimum width of the first metal

layer M1 (70 nm) dictates the minimum width of the silicon nanoresonator, because M1 serves as a masking layer to etch the Si beam later on in the post-processing step.

5.2.3 Suspension using SiO$_2$ as a Sacrificial Layer

In one approach, SiO$_2$ was used as a sacrificial layer and was etched away with vapor-phase Hydrofluoric Acid (HF) [125]. Several oxide layers, in different levels, are available in the CMOS technology. Different levels of oxide provide different thickness options for the air gap, which is an advantage of using SiO$_2$ as the sacrificial layer. The main advantage of etching using the vapor phase over the liquid phase HF is eliminating the surface tension phenomenon after the suspension and eliminating the risk of adhesion of the beam to the substrate or other nearby structures after suspension. It is important to point out that although the HF is used is in a gas phase, the temperature barely exceeds the room temperature, so this method preserves the thermal budget of the chip. The NEM resonators presented in this section are based on doubly clamped beams with source and drain contacts on each side and a close-by gate electrode. Figure 5.10 illustrates resonators post-processed using SiO$_2$ as sacrificial layer and vapor HF as the etching technique. Post-processing recipe is presented in Appendix A.7.
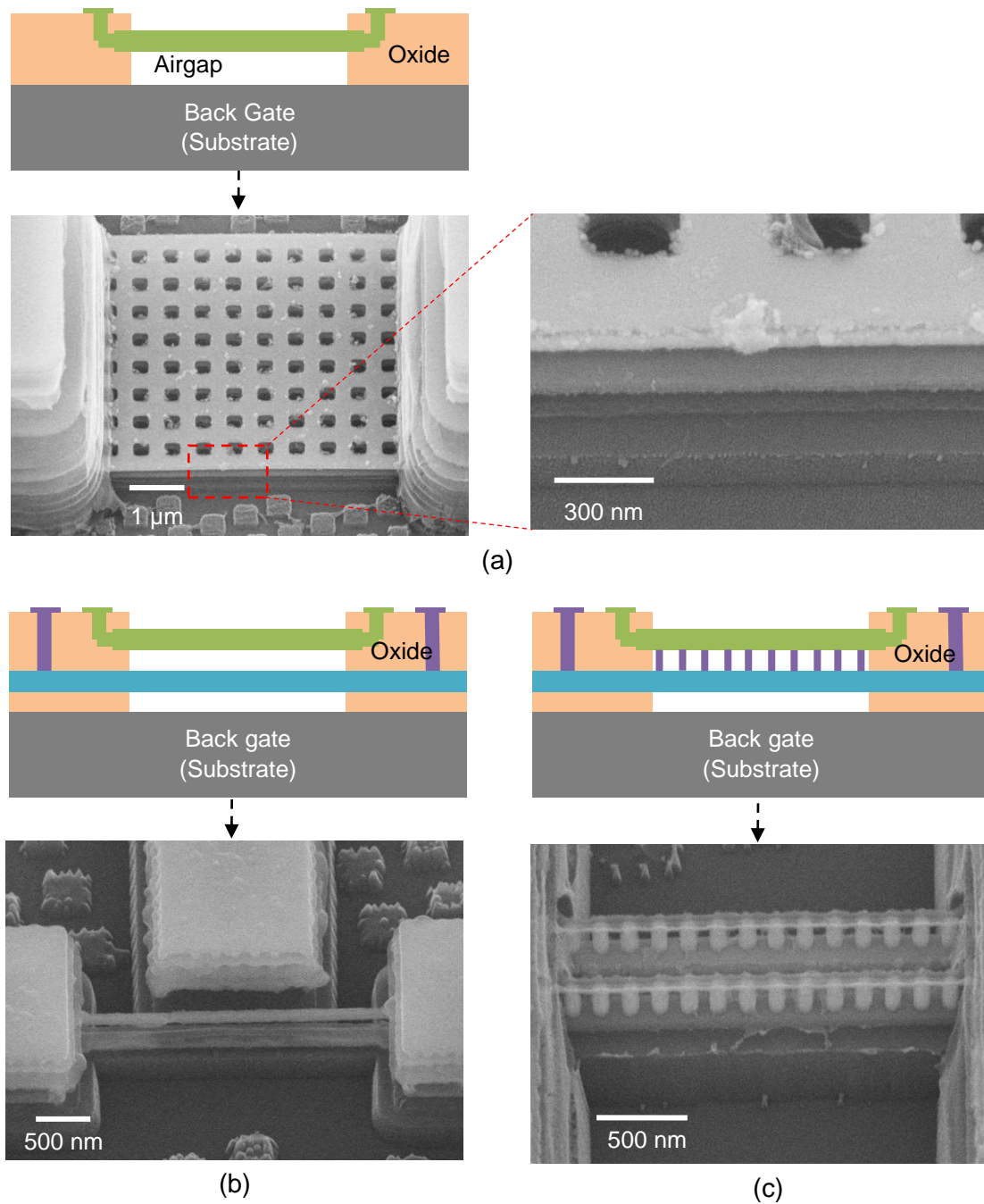
Figure 5.10. Using SiO_2 as sacrificial layer and vapor HF dry etching as the suspension technique. (a) A suspended metal plate, (b) parallel metal and silicon beams, and (c) a conjugated metal and silicon beam tied together using a row of vias.

Three different types of beams are suspended using the vapor HF technique, which are (i) metal beams (Figure 5.10(a)), (ii) parallel metal and silicon beams (Figure 5.10(b)), and (iii) conjugated metal and silicon beam tied together using a row of vias (Figure 5.10(c)). As an alternative approach, isotropic plasma etching was used in the RIE setup (Figure 5.11) to etch oxide as sacrificial layer. Plasma processing is a popular technique in different steps of standard CMOS fabrication, and using such a technique for beam suspension is considered an advantage. On the other hand, isotropic etching in a harsh plasma environment can attack the metal parts of the nanoresonator. One can realize this effect by looking at the thinned down nanoresonators presented in Figures 5.11(d,f). Post-processing recipe based on RIE etching of sacrificial layer of nano-resonators is also presented in Appendix A.7.
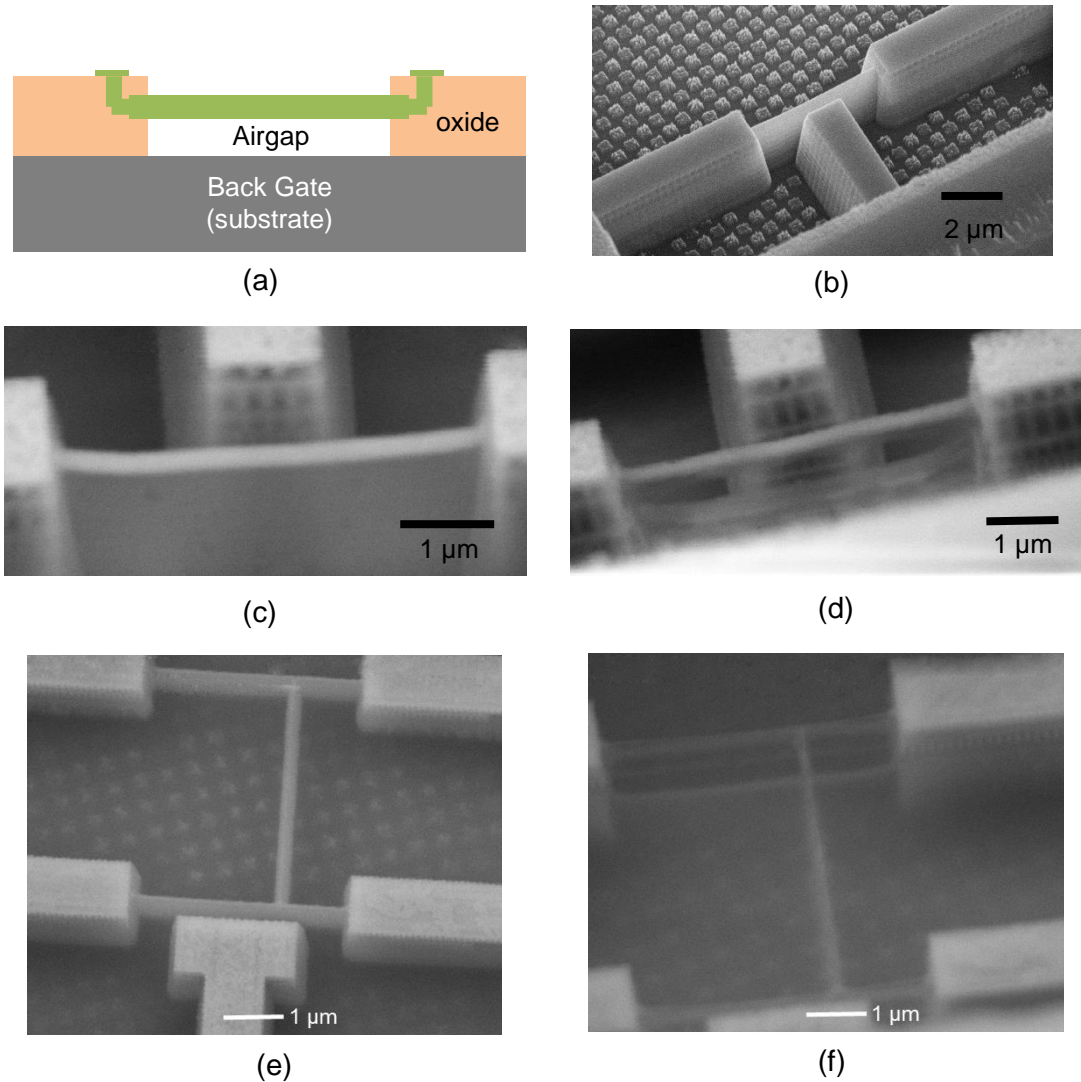
Figure 5.11. Using SiO$_2$ as a sacrificial layer and isotropic plasma etching as a suspension technique. (a) A schematic of the device. (b,c,d) SEM images illustrating nanoresonators during different post-processing stages (b) before, (c) after 30 minutes and (d) after 45 minutes of isotropic plasma etching. (e,f) SEM image of mechanically coupled beam (e) before and (f) after suspension.

5.2.4   Suspension using Si as a Sacrificial Layer

Alternatively, silicon was used as the sacrificial layer for metal-based NEMS beams and XeF$_2$ was used as the etching gas to remove Si. Figure 5.12 illustrates an integrated vertical microresonator, designed and post-processed in the CMOS chip. The suspended

micropillar illustrated at the center of Figure 5.12(b) is surrounded by four clamped actuators. Four meandered metal wires provide electrical connection to the center pillar. Five different pads in this structure enable electrical access to the micropillar as well as four actuators. XeF_2 gas offers excellent etching selectivity between the silicon and any other material used in this standard CMOS SOI chip. This is a significant advantage of this technique because in the suspension step, no additional consideration needs to be taken into account to protect other exposed CMOS components, such as pads (Post-processing recipe is presented in Appendix A.8). The fast silicon etch rate is another advantage of using this method. However, silicon is used as the active device layer in the CMOS chips, leading to the requirement of a large separation between the NEMS device and CMOS circuits (more than the dimension of the suspending structure). Therefore, utilizing Si layer as a sacrificial layer leads to larger chip areas with higher fabrication costs.

(a)

(b)

(c)

(d)
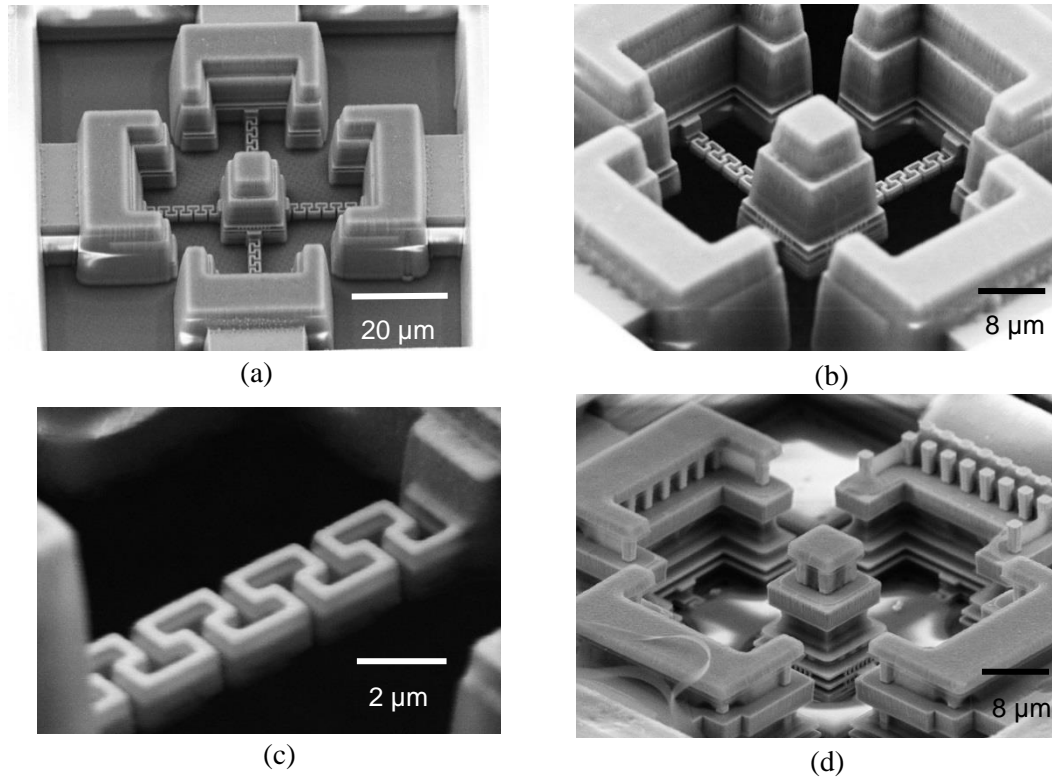
Figure 5.12. Using silicon as a sacrificial layer and XeF_2 etching as a suspension technique. (a) An SEM image of the vertical microresonator after isotropic vertical etching and before suspension. (b) The device after being suspended. (c) The flexible corrugated wires used to enable electrical access to the resonator. (d) An SEM image shows the electrical connections and vias inside the device. In order to be able to take this image, additional wet etching of oxide has been performed.

5.2.5   Suspension using Metal as a Sacrificial Layer

As the third material, metal (copper) was used as the sacrificial layer and acid solutions were used as the etchant for the sacrificial layer. Figure 5.13 illustrates an SEM image of a double-clamped copper beam suspended using this technique, with air gaps as small as 200 nm easily achieved. The post-processing steps are designed based on an initial anisotropic dry etching step (explained before), followed by a metal wet etching to suspend the beams. In the suspension step, the copper beam and contact pads are buried under a layer of oxide in order to prevent them from being etched by the acid solution.

Protective oxide layers are then etched, using an additional plasma etching step. Details of the post-processing steps are presented in Appendix A.9. The fast etch rate of the acid and availability of multiple metal layers with different thicknesses in the CMOS technology are among advantages of this method. However, additional considerations need to be taken into account in order to protect the CMOS circuits from being attacked by the acid. These considerations increase the cost of fabrication as some of the chip area is devoted to such sacrificial metallization layers. Imposing additional processing steps to get rid of the protection layer are among other disadvantages of this approach.
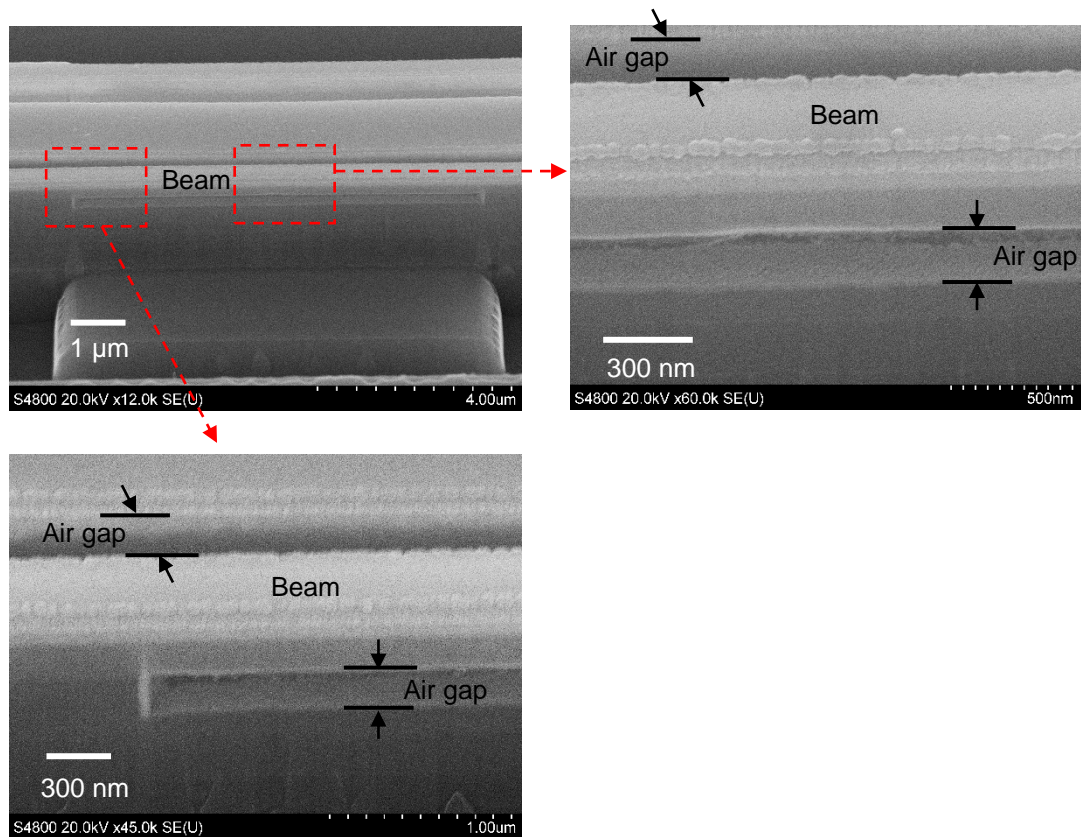
Figure 5.13. Using metal (copper) as a sacrificial layer and wet etching as the suspension technique. Air gaps as small as 200 nm are demonstrated in this figure.

5.2.6   Summary

In summary, novel post-processing technologies to integrate NEM devices with CMOS have been introduced. Three different materials available in CMOS, namely SiO_2 and Si and Cu, have been investigated as sacrificial layers to generate the air gap under the suspended nano-resonator structures. The advantages and disadvantages of each method are discussed and summarized in Table 5.2.

Table 5.2. Summarizing the advantages and disadvantages of utilizing three different materials available in CMOS as sacrificial layer.

Sacrificial layer	Suspension technique	Advantages	Disadvantages
SiO_2	Vapor HF	Vast availability of oxide layers in different levels of the CMOS chip	Random contamination particles appear after suspension
SiO_2	Isotropic plasma	Similar to other steps of standard CMOS processing	Metal beam being thinning due to low etching selectivity
Silicon	XeF_2	High etching selectivity of XeF_2 to other materials utilized in CMOS Fast etch rate	Using the active area of the chip for sacrificial layer Low control over etching
Metal	Acid	Vast availability of metal layers in different levels in CMOS chip. Fast etch rate	The pads need to be protected by additional layers in the suspension step

6. SUMMARY AND FUTURE WORK

6.1 Summary

High tech industries are in need of transformative approaches for sensors and biosensors. The various post-processing technologies to achieve CMOS integration have been pursued in this thesis and may pave the way towards integrated nano-sensor systems. Developing integrated CMOS technology partially overcomes the instrument noise problem through the utilization of an on-chip measurement system. Lower measurement noise and wide measurement bandwidth help enhance the frequency resolution, which leads to improved measurement precision. In this thesis, standard industry-scale 45 nm CMOS SOI technology has been used as a platform for the fabrication of a variety of nanostructures. Main demonstration vehicles have been investigated: (i) Technology for flexible MEAs suitable for characterization of single cells and neurons; (ii) Integration technology for lateral and vertical CMOS Integrated Field Emitters; and (iii) Engineered CMOS substrates for higher performance circuits. In all of these devices, post-processing recipes have been developed that do not require lithography, leading to high-yield and reproducibility of the proposed integrated sensors. In addition, post-processing procedures are developed for implementation of NEM resonators and fluidic nano-sensors that may be suitable for detecting cells and biomolecules.

6.2 Future Work

The next phase is to demonstrate the applications of the integrated sensors and nanostructures presented in Chapters 2, 4 and 5 as autonomous or implantable units, achieved by adding amplifiers, signal processing circuits and wireless communication modules for seamless and real time data analysis and transfer. Integration of a wireless

telemetry module (presented in Chapter 4) offers advantages toall of the categories of sensors presented in this dissertation. For example the following systems may be pursued: (i) An implanted wireless MEA sensor system (presented in Chapter 2) that may be powered and communicated with from a wearable base station for Neural Prosthetic applications; (ii) Fabrication of a low-cost, fully-integrated battery-less NEMS-CMOS integrated circuit chip (presented in Chapter 5) that paves the way for the internet of "tiny" things. Additionally, wireless molecular-scale mass, force and chemical sensor systems may become possible through this integration. In this case the integrated CMOS-sensor chip will replace the entire measurement setup. Such devices have applications in environmental monitoring among others; (iii) The CMOS-Fluid channels presented in Chapter 5 can benefit from the integration with wireless communication and powering system by simplifying the packaging requirements, since only fluidic packaging will be required. Such fully-integrated battery-less systems with integrated antenna are based on a single chip and enable non-expert users to easily operate complex sensors. For example, patients can use bio-sensors for self-diagnosis purposes using a combination of a wireless module and a smartphone.

Figure 6.1 depicts the integration concept for the devices presented in Chapters 2 and 4. The proposed flexible and implantable MEA (Figure 6.1(a)) is equipped with an integrated wireless link and a miniaturized on-chip antenna (Figure 6.1(c)), which facilitate wireless communication and powering. An array of nano-pillars (Figure 6.1(b)) enables sensing from various sites of the surface of living tissues. Each sensing island (Figure 6.1(d)) consists of multiple sensors including action potential and pH sensors for multifunctional applications. High signal-to-noise ratios are achievable by introducing an on-chip amplifier as part of the readout system, and, integrated CMOS-based analog multiplexer circuits facilitate multiple sensor port measurements.
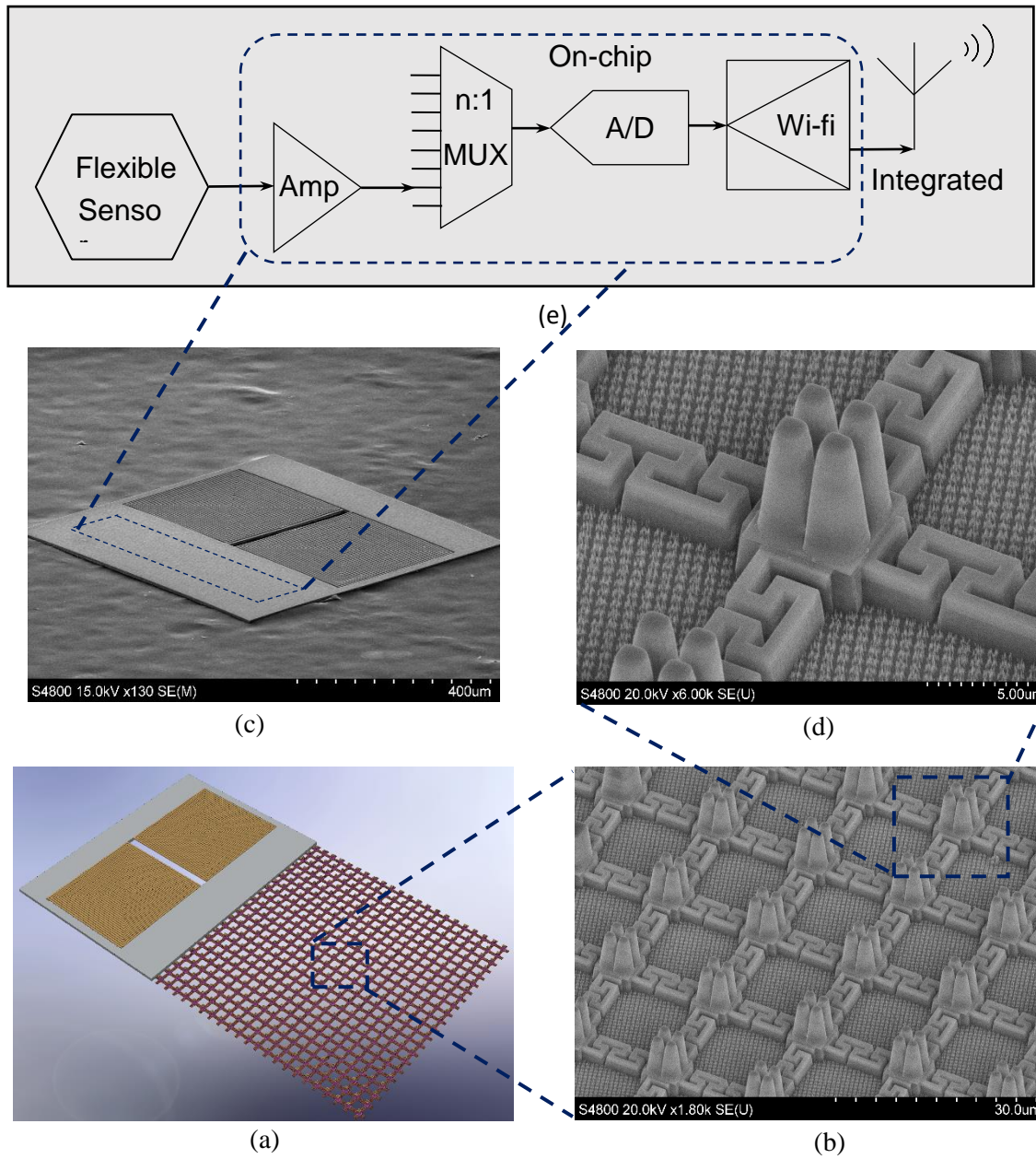
Figure 6.1. (a) A schematic of a flexible implantable wireless-powered single-chip sensor with communication link with an on-chip antenna. (b) An SEM image of an arrays of flexible nano-pillars, presented in Chapter 2. (c) An SEM image of the exfoliated CMOS antenna presented in Chapter 4. (d) An SEM image of each sensing island, illustrating 4 nano-pillars. (e) A block diagram of the ultra-low-power system for the sensor applications.

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APPENDIX

APPENDIX

A. POST-PROCESSING:

A.1. MEA Post-Processing:

- Anisotropic plasma etching using inductively coupled plasma etching setup (Panasonic E620 etcher):
    - Etch time: 32 min.
    - Perform the etching in three different runs and let the system cool down for 10 min between the runs.
    - Pressure: 1 Pa.
    - CF_4 flow rate: 10 sccm.
    - CHF_3 flow rate: 40 sccm.
    - RF power: 700 W.
    - DC power: 250 W.
    - Etch rate: ~ 0.34 nm/min.

- Al_2O_3 depostion using atomic layer deposition (Cambridge Nanotech Fiji ALD):
    - 0.06 second, TMA precursor.
    - 0.06 second, water precursor.
    - 200 cycles.
    - Deposition rate = 0.85 Angstrom/min.

- Anisotropic plasma etching using inductively coupled plasma etching setup (Panasonic E620 etcher):
    - Time: 30 s.

- Pressure: 1 Pa.
- CF_4 flow rate: 10 sccm.
- CHF_3 flow rate: 40 sccm.
- RF power: 500 W.
- DC power: 150 W.

- Isotropic silicon etching using XeF_2 etching setup (Xactix Xetch Xenon Difluoride etcher):
  - Cycle time: 20 s.
  - Pressure: 2.8 T.
  - Number of cycles: 15.

- Making a micro-curvature PDMS stamp:
  - Mix PDMS resin and it's hardener with a ratio of 10:1 (Sylgard 184 silicon elastomer kit).
  - Put the PDMS in a low vacuum chamber for 20 min to make it bubble free.
  - Mold a thick layer of PDMS in Petri dish (Thickness about 1 mm).
  - Cover the Petri dish with Aluminum foil and cure it on hot plate for 4 hours in 70 ^{o}C.
  - Cut a PDMS square (2 cm x 2 cm) using blade.
  - Place a Fluorescent micro-bead on the PDMS sheet.
  - Place the sheet on a glass slide.
  - Mix PDMS resin and it's hardener with a ratio of 10:1.
  - Put the PDMS in a low vacuum chamber for 20 min to make it bubble free.
  - Spin coat the PDMS on the PDMS sheet (with a bead on top) with the speed of 3000 rpm for 40 seconds.
  - Cure it on 70 ^{o}C hot plate for 4 hours.

- Use micromanipulator and optical microscope setup to transfer-print the MEA on top of the curvature.

A.2. Field Emitter Post-Processing:

- Anisotropic plasma etching using inductively-coupled plasma etching setup (Panasonic E620 etcher):
    - Time: 32 min.
    - Perform the etching in three different runs and let the system cool down for 10 min between the runs.
    - Pressure: 1 Pa.
    - CF_4 flow rate: 10 sccm.
    - CHF_3 flow rate: 40 sccm.
    - RF power: 700 W.
    - DC power: 250 W.
    - Etch rate: ~ 0.34 nm/min.

- Wirebonding (Westbond 7440E wirebonder):
    - Attach the chip to PCB using double-sided tape
    - Wirebond the gold first 250 ^{o}C,
    - Second wirebond the Al pad at 180 ^{o}C (Second one leaves smaller footprint)

A.3. Substrate Transferring to AlN:

- Attach to glass slide:
    - Drop AZ 9260 photoresist on glass.
    - Spin at 650 rpm and attach the chip on it.
    - Bake on hot plate at 100 ^{o}C for 10 min.

- Isotropic silicon substrate etching using XeF2 etching setup (Xactix Xetch Xenon Difluoride etcher):

- Cycle time: 15 s.
- Pressure: 2.9 T.
- Number of cycles: 122.

- Transferring to AlN substrate:
    - Put the flake and holder inside PRS solution for 10 min at 110 $^{\circ}$C.
    - After dis attaching, clean the flake in IPA for 2 min.
    - Clean the AlN substrate.
    - Use vacuum tweezer to handle the flake.
    - Use PMMA (Microchem A4) to bond the flake to AlN substrate.
    - Bake the PMMA for 10 min at 100 $^{\circ}$C.
    - Then for 5 min at 160 $^{\circ}$C.
    - Then for 3 min at 180 $^{\circ}$C.
    - Then for 70 min at 75 $^{\circ}$C.

A.4. Removing the Substrate underneath the Antenna:

- Packaging:
    - Drill a 1 mm hole inside PCB.
    - Apply a double sided tape on the hole.
    - Laser cut a hole on the double-sided tape (Universal Laser System). Aligned the hole exactly on top of the PCB hole.
    - Laser cut a water-mark on the double sided tape as your guide to be able to put the chip exactly on the desired location. (Use low power laser for this purpose).
    - Locate the chip on the double sided tape, using laser cut markers as your guide.
    - Wirebond the chip to the punched PCB (Westbond 7440E wirebonder).
    - Place the module upside down inside a holder setup made of Acrylic to protect the side wall.

- Isotropic selective substrate etching using XeF2 etching setup (Xactix Xetch Xenon Difluoride etcher):
    - Locate the Acrylic holder in the XeF2 setup.
    - Cycle time: 20 s.
    - Pressure: 2.9 T.
    - Number of cycles: 140.
    - The SOI buried oxide layer serves as the etch stop.

A.5. Fluidic Vertical Micro and Nanochannel Post-Processing:

- Back chip lithography to make a hole on the chip substrate:
    - Spin photoresist (AZ9260) on glass with the speed of 2500rpm.
    - Bond the chip upside down on to the glass.
    - Bake for 2 min in oven 80 $^{\circ}$C.
    - Spin coat back side of the chip (chip substrate) with HMDS with the speed of 8000 rpm.
    - Spin coat back side of the chip (chip substrate) with photoresist (AZ1815) with the speed of 8000 rpm.
    - Bake for 10 min on a 100 $^{\circ}$C hot plate.
    - Use MJB3 setup for lithography exposure (exposure time 20 s).
    - Develop the photoresist in MF26A for 1 min.
    - Bake 2 min in 80 $^{\circ}$C oven.

- Protecting the chip side wall from the etching gas:
    - Laser cut a 1 mm hole on a UV tape (Universal Laser System). This will be used to protect the chip sidewalls and the hole will let the photoresist hole to be exposed to the etching gas.
    - Align the hole in the UV tape with the hole generated by photolithography on the back side of the chip (do this under an optical microscope with hand).

- Apply another layer of UV tape on the top side of the chip (so the chip will be sandwiched between two layers of UV tape).

- Isotropic selective substrate etching using XeF_2 etching setup (Xactix Xetch Xenon Difluoride etcher):
    - Cycle time: 20 s.
    - Pressure: 2.8 T.
    - Number of cycles: 80.
    - The SOI buried oxide layer serves as the etch stop.

- Preparing the chip for top-chip processing:
    - Gently remove UV tape by exposing the tapes to high density UV light.
    - Soak the chip in room temperature acetone for 1 hour to remove the. photoresist from the back side of the chip. (Alternatively, you can use PRS 2000 overnight at 100 ^{o}C.
    - Wash the chip with water.
    - Dry the chip in 80 ^{o}C oven for 15 min.
    - Ash the photoresist residue (if any) using plasma (Branson Asher).

- Top-chip processing:
    - In the inductively couple plasma system (Panasonic E620 etcher):
    - Etching time: 32 min.
    - Perform the etching in three different runs and let the system cool down for 10 min between the runs.
    - Pressure: 1 Pa.
    - CF_4 flow rate: 10 sccm.
    - CHF_3 flow rate: 40 sccm.
    - RF power: 700 W.
    - DC power: 250 W.

A.6. Fluidic Lateral Micro and Nanochannel Post-Processing:

- Anisotropic plasma etching using inductively coupled plasma etching setup (Panasonic E620 etcher) to form the fluid vertical inlet and outlet channels:
  - Etching time: 11 min.
  - Pressure: 1 Pa.
  - CF_4 flow rate: 10 sccm.
  - CHF_3 flow rate: 40 sccm.
  - RF power: 700 W.
  - DC power: 250 W.
  - Built-in metal layer will serve as etch-stop.

- Wet etching to open up the horizontal fluid channel:
  - Prepare copper etchant ($H_2O:HNO_3$, 1:5).
  - Heat it to 50 ^{o}C.
  - Put the chip inside etchant for 9 min.
  - Wash with water.
  - Dry on hot plate 80 ^{o}C.

- Second anisotropic plasma etching using inductively coupled plasma etching setup (Panasonic E620 etcher) to reveal the buried wirebonding pads:
  - Etching time: 9 min.
  - Pressure: 1 Pa.
  - CF_4 flow rate: 10 sccm.
  - CHF_3 flow rate: 40 sccm.
  - RF power: 700 W.
  - DC power: 250 W.
  - Pad itself will serve as etch-stop.

A.7. Nanoresonator Post-Processing (Suspension using SiO$_2$ as Sacrificial Layer):

- Anisotropic plasma etching using inductively coupled plasma etching setup (Panasonic E620 etcher):
    - Etching time: 30 min.
    - Perform the etching in three different runs and let the system cool down for 10 min between the runs.
    - Pressure: 1 Pa.
    - CF$_4$ flow rate: 10 sccm.
    - CHF$_3$ flow rate: 40 sccm.
    - RF power: 700 W.
    - DC power: 250 W.

- Isotropic plasma etching using inductively coupled plasma etching setup (Panasonic E620 etcher, to thin down the polymer generated on the side wall, as the result of the previous step).
    - Etching time: 18 min.
    - Perform the etching in two different runs and let the system cool down for 10 min between the runs.
    - Pressure: 12 Pa.
    - CF$_4$ flow rate: 40 sccm.
    - CHF$_3$ flow rate: 0 sccm.
    - RF power: 900 W.
    - DC power: 0 W.

- Isotropic SiO$_2$ etching using vapor etching setup (Advanced Micromachining Tools AMMT) to etch the sacrificial layer.
    - Wait 30 min to let the chip to rehydrate.
    - Attach the chip to the vapor HF holder setup. Apply gentle electrostatic force for the attachment purpose.

- Set the temperature to 22 $^{\text{o}}$C above the room temperature. Wait for 10 min the chip temperature adapt with the chuck temperature.
- Run the vapor HF setup (etching time 3 min).

A.8. Nanoresonator Post-Processing (Suspension using Si as Sacrificial Layer):

- Anisotropic plasma etching using inductively coupled plasma etching setup (Panasonic E620 etcher):
  - Etching time: 30 min.
  - Perform the etching in three different runs and let the system cool down for 10 min between the runs.
  - Pressure: 1 Pa.
  - CF_4 flow rate: 10 sccm.
  - CHF_3 flow rate: 40 sccm.
  - RF power: 700 W.
  - DC power: 250 W.

- Isotropic etching using XeF_2 etching setup (Xactix Xetch Xenon Difluoride etcher):
  - Cycle time: 10 s.
  - Pressure: 2.6 T.
  - Number of cycles: Depends on the area to be suspended. Etch rate is about 600 nm per cycle.
  - The SOI buried oxide layer serves as the etch stop.

A.9. Nanoresonator Post-Processing (Suspension using Metal as Sacrificial Layer):

- Anisotropic plasma etching using inductively coupled plasma etching (Panasonic E620 etcher):
  - Etching time: 32 min.
  - Perform the etching in three different runs and let the system cool down for 10 min between the runs.

- Pressure: 1 Pa.

- CF_4 flow rate: 10 sccm.

- CHF_3 flow rate: 40 sccm.

- RF power: 700 W.

- DC power: 250 W.

- Built-in metal layer will serve as etch-stop.

- Wet etching to etch the metal sacrificial layer:

  - Prepare copper etchant ($H_2O:HNO_3$, 1:5).

  - Heat it to 50 ^{o}C.

  - Put the chip inside etchant for 5 min.

  - Wash with water.

  - Dry on hot plate 80 ^{o}C.

- Second anisotropic plasma etching using inductively coupled plasma etching setup (Panasonic E620 etcher) to reveal the buried wirebonding pads:

  - Etching time: 6 min and 40 seconds.

  - Pressure: 1 Pa.

  - CF_4 flow rate: 10 sccm.

  - CHF_3 flow rate: 40 sccm.

  - RF power: 700 W.

  - DC power: 250 W.

  - Pad itself will serve as etch-stop.

VITA

VITA

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