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A self-powered single-chip wireless sensor platform

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A SELF-POWRED SINGLE-CHIP WIRELESS SENSOR PLATFORM

For the degree of Doctor of Philosophy

Is approved by the final examining committee:

Saeed Mohammadi
Chair

Byunghoo Jung

Dan Jiao

Dimitrios Peroulis

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Approved by Major Professor(s): Saeed Mohammadi

Approved by: Venkataramanan Balakrishnan 11/30/2016

Head of the Departmental Graduate Program Date

A SELF-POWERED SINGLE-CHIP WIRELESS SENSOR PLATFORM

A Dissertation

Submitted to the Faculty

of

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In Partial Fulfillment of the

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of

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TABLE OF CONTENTS

Page

Page

ABSTRACT

Jou, Alice. Ph.D., Purdue University, December 2016. A Self-powered Single Chip Wireless Platform. Major Professor: Saeed Mohammadi.

"Internet of things" requires a large array of low-cost sensor nodes, wireless connectivity, low power operation and system intelligence. On the other hand, wireless biomedical implants demand additional specifications including small form factor, a choice of wireless operating frequencies within the window for minimum tissue loss and bio-compatibility. This thesis describes a low power and low-cost internet of things system suitable for implant applications that is implemented in its entirety on a single standard CMOS chip with an area smaller than 0.5 mm^2. The chip includes integrated sensors, ultra-low-power transceivers, and additional interface and digital control electronics while it does not require a battery or complex packaging schemes. It is powered through electromagnetic (EM) radiation using its on-chip miniature antenna that also assists with transmit and receive functions. The chip can operate at a short distance (a few centimeters) from an EM source that also serves as its wireless link. Design methodology, system simulation and optimization and early measurement results are presented.

1. INTRODUCTION

1.1 Introduction

"Internet of things" demands a large array of sensors with wireless connectivity, low power operation, and system intelligence. Today, a wide range of sensors has been realized and being integrated with electronics to reduce cost, improve performance and provide intelligence. Physiological sensors are a sub-category of sensors that are being developed for future medicine and healthy living. Among these sensors are electroencephalography EEG (scalp), electrocorticography EcoG, and active potential AP sensors that allow detection and diagnosis of abnormal neural activities leading to epilepsy seizure, sleeping disorder, coma and encephalopathies and brain death. Furthermore, using these sensors, the possibility of control prosthetic limb or paralyzed limb [67] has been demonstrated. Electrocardiography ECG (heart) sensors, as another example, are utilized to measure heart's electrical conduction system. Electromyography EMG (skeletal muscles) sensors help identifying neuromuscular diseases, assessing lower back pain, kinesiology, disorders of motor control and avoidance of postoperative residual curarization (PORC) as well as finding applications in prosthesis. Glucose sensors have been utilized for detecting diabetes, while DNA/protein sensors help detect Hepatitis B and cardiac Troponin-I proteins. [2][9].

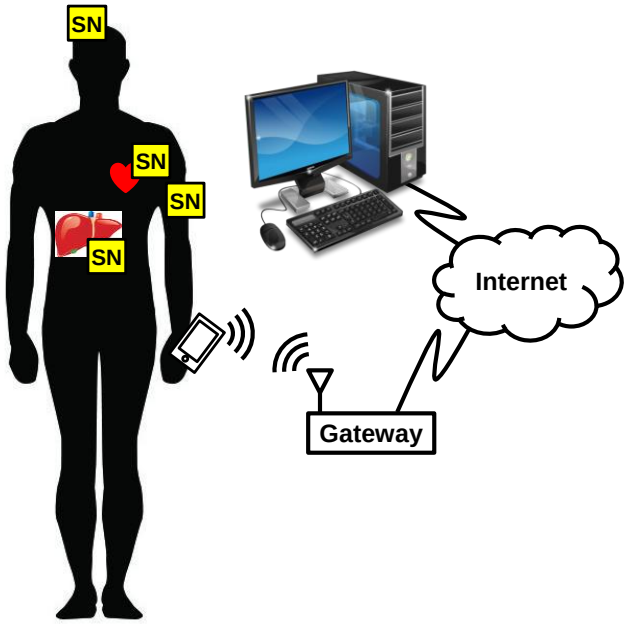


Figure 1.1 Low-cost, Portable Health Monitoring Systems with Hand Held Monitor and Sensor Nodes. [Human icon source: https://a2ua.com/human/human-008.jpg, Liver icon source: http://www.hairlossrevolution.com/wp-content/uploads/2013/10/clean-liver-help-hair-loss.jpg, Computer icon source: http://www.wiu.edu/academics/majors/business_and_technology/computer-science.php]

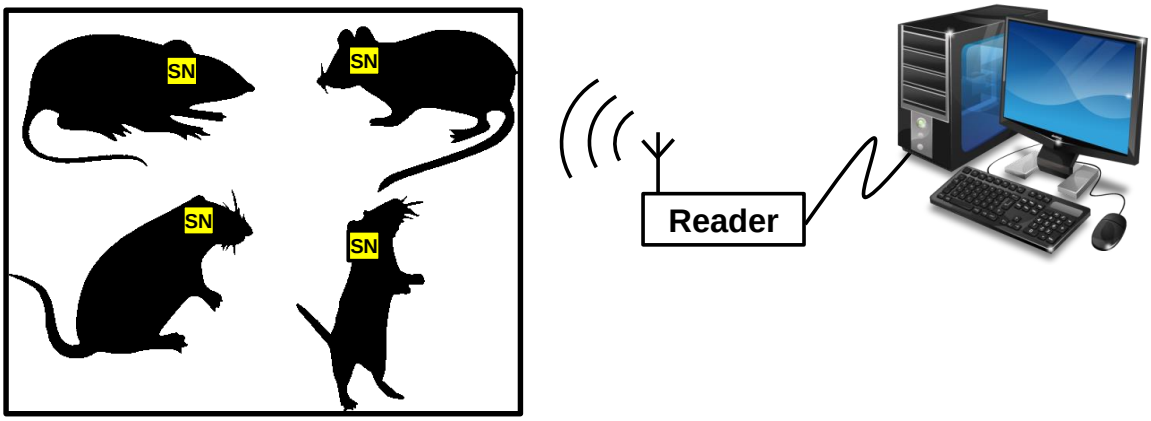


Figure 1.2 Biomedical conditions monitoring on mice without interference. [Mice picture: http://vcctherapy.blogspot.com/p/color-options.html]

Implantable sensors have been widely used for various health monitoring applications with the advantage of constant monitoring through wearable reader devices such as smart phones. Most implantable sensors are powered by batteries, leading to their

limited lifetime. Some of the associated problems with the large size of the battery such as uncomfortable feeling by some patients, isolation requirement, possibility of toxicity and high cost are unresolved. Even in designs with battery-less power harvesting methods, while the problems associated with the battery are eliminated, the requirement for off-chip powering components such as antenna coils or other power scavenging devices increases the packaging cost and the form factor of the device. Furthermore, the performance degradation exists from the packaging between off-chip components and wireless communication IC.

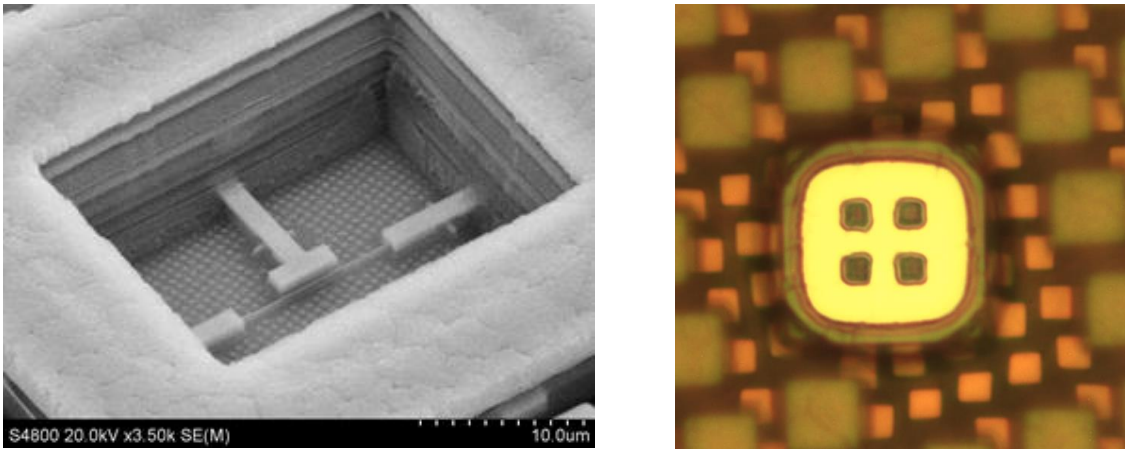
This work aims at implementing a system in its entirety on a single standard CMOS chip with an area smaller than 0.8 mm^2 for both affordability and patients' comfort. The chip includes integrated multi-channels sensors, ultra-low power transceivers, and additional interface and digital control electronics without a battery or specific packaging requirements. It will be powered electromagnetically using an on-chip antenna to perform transmit, receive and sense functions from a short distance (a few centimeters). Design methodology, system simulation and optimization and measurement results are presented.

In the context of healthy living, applying low-cost semiconductor technology working with handheld devices and smart phones with extremely high signal processing capability to biomedical applications provides the possibility of self-diagnosis without utilizing expensive medical equipment. Such smart, low-cost medical platforms will also provide access to diagnosis in poor localities where access to medical facilities is not

available. As an example, a recent invention of a capacitive micro-machined ultrasound transducer (CMUT) device by a start-up company named Butterfly Network is propelling a low-cost hand-held ultrasound imaging system for diagnosis of breast cancer, visualizing a fetus, or even eradicating tumors [30]. Healthcare systems using such smart health monitoring implant devices will be very effective in diagnosing diseases at early stages preventing the need for complicated surgery or other expensive treatments. [65] In addition, miniature low-cost biomedical sensors may help in enhancing research and data collection in health care and biomedical engineering.

CMOS-based nano- and micro-electromechanical (NEMS and MEMS as shown in Fig. 1.3 (a)) resonators and switches recently developed at Purdue using a simple post-processing technology promise fully integrated compact and low cost intelligent sensor nodes. CMOS integrated sensors benefit from on-spot signal amplification, which significantly reduces the sensor load capacitance, leading to limited undesired signal coupling, less noise and enhanced measurement bandwidth. For example, such resonators can enhance the performance of an EEG sensor. EEG activities show oscillations at various frequencies, and a NEMS resonator can be designed to resonate at a particular frequency to couple to abnormal neuro activities such as seizure. The signal detected by the resonator can be amplified on spot and sent out to a hand held device for immediate treatment or precautions. Another example of integrated sensors on CMOS platform is a recently developed nanofluidic device as shown in Fig. 1.3 (b). The fluidic device is post processed on a standard CMOS chip and a simple fluidic packaging is performed to provide inlet and outlet to the sensor system. The availability of wireless

powering and communication allows a simple packaging of the chip inside a fluidic environment without concern about leads and electrical connections. The device can be utilized for detecting cancerous cells using the characteristic of larger deformability of cancer cell comparing to normal cell hence passing through microfluidic channel faster than normal cell [31].



(a) (b)

Figure 1.3 (a) A NEMS resonator post-processed on a CMOS Chip (b) A Nano-/Micro-fluidic sensor post-processed on a CMOS Chip [Picture courtesy of Hossein Pajouhi]

1.2 Miniature Passive Sensor Node Trend

Miniature passive wireless sensor nodes have found many applications including chemical detection and medical health monitoring. These integrated sensors are capable of sensing temperature [4-6], pH, DNA, glucose [9] and neural electro activities such as Electroencephalography EEG (scalp), Electrocorticography EcoG (brain) [37], Electrocardiography ECG (heart), Electromyography EMG (skeletal muscles), Electronystagmography ENG (eye), Active Potential and Field Potential (neural) [2], intraocular pressure [44], and image sensors [45]. For instance, reference [9]

demonstrates the highest integration level with several sensors on a single chip that includes resistance, voltage, current and capacitor sensors. However, a hydrogel packaging for glucose CMOS MEMS sensor and an additional coil or solar cells for wireless power scavenging are required, which increases the device form factor, and makes it unwearable or uncomfortable. In reference [2], off-chip electrode array is utilized for active potential sensing, which leads to signal degradation from electrode to IC leading to worsening of the sensitivity of the active potential measurement. Reference [44] demonstrates the integration of sensor node with intraocular pressure detection as an eye implant. Reference [45] integrates the sensor node with image sensors. References [44] and [45] both need additional packaging among dies modules and thin film batteries for power supply leading to an increase of the cost and form factor.

From medical health monitoring stand point, changing battery would not only increase the danger of infection but is also inconvenient for the patient. Even though thin film batteries are currently under development, the capacity is still too small for applications that will last for days [7]. Among several energy harvesting methods including photo-voltaic, piezoelectric [8], [10] and thermos-electric [13], radio wave wireless charging is the only strategy that would work in an environment that does not require light sources, vibration or thermal gradient. Therefore, wireless powering is a solution that can work with health monitoring applications. In other words, wireless rechargeable systems provide more convenience as well as possibility for smaller form factors accompanied with reduced fabrication cost.

In [1] an on-chip antenna with RF front end and power management circuits that occupies an area of 3 mm ×1.5 mm is presented. The design is compact and achieves sufficient gain at 5.8 GHz. In [2] an in-vivo tested neural sensor with a chip coil occupying an area of 500 μm × 250 μm operating at 1.5GHz in near-field is presented. EE times news [34] reported a fully-integrated temperature sebsor less than 2 mm^2 that operates in a range of 2.5 cm implemented in 65 nm CMOS technology using wireless charging for batteryless energy harvesting. Reference [5] has implemented a 24 GHz on-chip antenna and uses dual antenna topology with design area of 3.6 mm × 1.6 mm in 0.18 μm CMOS process. In reference [36], dual on-chip antenna operating at 24 GHz and 60 GHz with an area of 3.7 mm × 1.2 mm in 65 nm CMOS technology is implemented that works at a distance of 28 cm under an effective isotropically radiated power (EIRP) of 40 dBm. These examples demonstrate the effectiveness of wireless charging with small chip area for biomedical implant applications.

1.3 Challenges with Fully-Integrated Passive Wireless Sensor Nodes in CMOS Process

There are several challenges in developing a fully integrated sensor node platform, that consist of a sensor data acquisition IC, with an on-chip antenna, rectified charge storing capacitors, and sensor units. First, in order to save rectified charges as a power source, a large capacitor is required. However, since there is a trade-off between capacitor area and its stored charge capacity, the tag system would have to operate at very low power consumption in order to achieve miniaturized characteristic. Second, an on-chip antenna integrated with the tag has to be miniaturized or it would lose advantages of

cost effectiveness and small size. However, antenna miniaturization adversely impact antenna efficiency, bandwidth, and impedance matching [27]. Although it has been demonstrated that on-chip antennas operating at higher frequencies may increase the ratio of miniature antenna size over operating wavelength, the energy loss due to propagation at higher frequencies would be higher according to Friis equation $P_{received} = P_{transmitted} \cdot G_R(\theta, \varphi) \cdot G_T(\theta, \varphi) \cdot (\frac{\lambda}{4\pi R})^2$. In [15], an on-chip antenna implemented in a 0.35μm CMOS technology is presented that operates at 35 and 94GHz with gain of 7.4 and 6.5 dBi and an area of 2.9 mm^2. Reference [16] demonstrates an on-chip antenna in a 65nm CMOS process with simulated gain of 2.28 dBi that occupies 0.48 mm^2 area. The path loss, when the operating frequency of the antenna is 10 times higher, would be 100 times higher at the same distance. Therefore a 94 GHz antenna would have approximately 20 dB more path loss comparing to a 900 MHz antenna. On the other hand a 94 GHz antenna can be implemented in a much smaller area compared to a 900 MHz antenna. The optimum length for a dipole antenna is half of wavelength λ/2 and a quarter of wavelength λ/4 for monopole antenna [33]. However, half of wavelength and quarter of wavelength are considered impractical for an on-chip antenna design. In [31], author analyzes the minimum require length of octave antenna to be 0.365 λ, where λ is the free space wavelength, in order to maintain a sufficient quality factor Q of $\sqrt{2}$. The assumptions for such calculation are that the antenna is lossless and uses spherical volume efficiently. However, 0.365 λ is still too large for on-chip application. A trade off among the efficiency of the antenna and its gain, quality factor or bandwidth for has to be

made for a smaller size antenna. This trade-off between antenna gain optimization and propagation attenuation puts a challenge for on-chip antenna design.

An optimized low-power design can meet the requirement of small available power and battery-less operation. In [7] an efficiency tracking loop control of rectifiers has been utilized to maintain optimum efficiency of the rectifiers. However, overall low power consumption is still necessary for a higher sensitivity sensor node.

The proposed system in this thesis utilizes near-field communication at GHz frequencies with sensor node with transmitting horn antenna at centimeter range distance from the power source (antenna). Both capacitive coupling and near-field operation share the same on-chip antenna/metal plate structure. When the sensor node is positioned in the field (for instance implanted into body), a hand held or wearable device that uses GHz frequency radio wave to power up and communicates with the sensor nodes is utilized. The same device is envisioned to constantly monitor the health condition. In addition, owing to the tiny size of the proposed system, it can be utilized for in-vivo experiments on mice or other small animals without interference in their behavior.

1.4 System and Thesis Overview

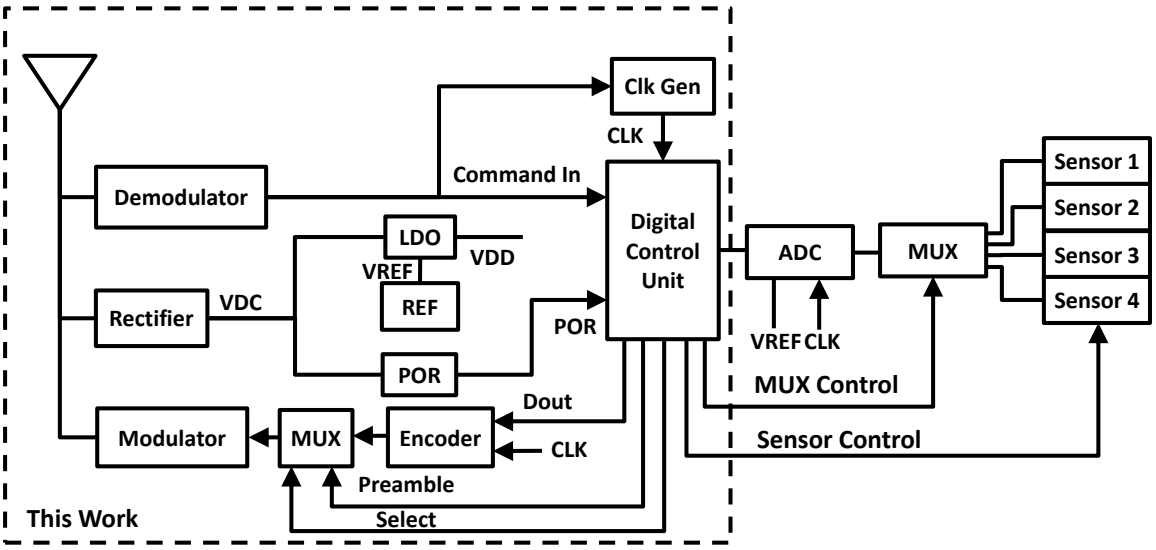


Figure 1.4 Sensor Node System Block Diagram

Fig.1.4 demonstrates the block diagram of the proposed sensor node system. The front-end rectifiers rectify Hz wave into DC voltage for power source. The incoming radio wave also feeds the demodulator that demodulates the encoded command and clock frequency tuning beacon from reader and sends the command to the base-band processor and clock generation circuit. Power on reset enables start up signal to baseband processor to initialize the system. The digital control oscillator generates a 10 MHz clock for an integrated ADC, a Miller sub-carrier encoder and the demodulator. A clock divider divides the 10 MHz clock signal down to a 2.5 MHz clock signal for both encoder and baseband processor and a 1 MHz signal for the Miller sub-carrier encoder. The digital control units control the state machine and stimulate/activate sensors and select sensor multiplexer output among different sensor channels. The modulator backscatters the output data with the radio wave to transmit the signal from the tag to a distant reader/interrogator.

The thesis is divided into 7 chapters. Chapter 2 describes the near-field operation and rectifier design and measurements. Chapter 3 explains the uplink and down link protocol definitions as well as decoder and encoder designs. Chapter 4 provides information on the design and implementation of the RF front-end circuit. Operation of the state machine of the baseband processing circuit and the timing control while collaborating with ADC and sensor control circuit, as well as the digitally controlled oscillator design are presented in Chapter 5. Chapter 6 describes the integration of all blocks while conclusion and future work are described in Chapter 7.

On-chip sensors, sensor multiplexer, and analog to digital converter that are shown outside of the dotted line box in the block diagram of Fig. 1.4 are implemented by other students and will not be discussed in this Thesis.

2. ON-CHIP ANTENNA WITH NEAR FIELD WIRELESS HARVESTING

2.1 Frequency Selection for Wireless Harvesting

According to FCC regulations title 47 Part 18, certain frequency bands are open for industrial, medical and scientific (ISM) applications as listed in Table 2.1. FCC regulations title 47 Part 15.247 specifies digital modulation band allowed in 902-928 MHz, 2400-2483.5 MHz, and 5725-5850 MHz bands. The minimum 6 dB bandwidth shall be at least 500 kHz. For these bands, the maximum peak conducted output power of the intentional radiator shall not exceed 1 Watt. Antenna gain should not exceed 6 dBi with 1 Watt output power to the antenna. With antenna gain over 6dBi, band 2400-2483.5 MHz in fixed point to point operation requires an output power to the antenna to decrease by 1dB by every 3dBi increase in the antenna gain (Table 2.2). For band 5725-5850 MHz in a fixed point to point operation, an antenna gain greater than 6dBi can be used without any reduction in the output power to the antenna. Part 15.249 describes the restriction for band 24.05-24.25 GHz with an antenna gain of at least 33 dBi and that the main lobe should not exceed 3.5 degrees with maximum field strength of 2500mV/meter. According to Part 15.255, the maximum EIRP average power for band 61.25 GHz is 40dBm, and maximum peak power is 43dBm while conducted output power should be less than 500 mW for bandwidths less than 100MHz. There is also medical implantable communication services (MISC) bands ranging from 401 MHz to 406 MHz described in Part 95.627. For

medical implantable devices that do not incorporate frequency monitoring system, the operating frequency bands of 401-402 MHz, 403.5 and 405-406 MHz are allowed. The maximum allowed power when using MICS band is only 25 micro watts and the duty cycle has to be less than 0.1% with less than 100 transmissions per hour [20]. In [25], dielectrics of different body tissues have been characterized. With the assumption of tissue thickness of less than skin depth, reference [12] presents an experiment of wireless power transmission through a beef sirloin to find the maximum power gain at radio frequencies to be around 3 GHz. Simulation shows through air-muscle interface and air-skin-fat-muscle-skull-brain achieve a maximum power gain between 1 to 3 GHz. Therefore, the frequency of implantable wireless systems should be aimed at the frequency bands that follow FCC regulation while taking the transmission loss through the body tissue into consideration.

From implant application aspect, reference [12] states that the optimum frequency for implants in GHz range lays in 1-3 GHz range. Therefore, in this Thesis, a frequency between 1-3 GHz has been selected coinciding with optimal frequency for implantable applications.

Table 2.1 FCC CFR Title 47 Part 18.301 and Part 15 ISM Operation Frequency and Limited Output Power and Field Strength

ISM frequency	**Tolerance**	**Transmitted Power**	**Antenna gain**	**EIRP**	**Field Strength**
6.78 MHz	±15.0 kHz	<57dBm			<25uV/m at 300m
13.56 MHz	±7.0 kHz	<57dBm			<25uV/m at 300m
27.12 MHz	±163.0 kHz	<57dBm			<25uV/m at 300m
40.68 MHz	±20.0 kHz	<57dBm			<25uV/m at 300m
915 MHz	±13.0 MHz	<30dBm	<6dBi	<36dBi	<50V/m
2,450 MHz	±50.0 MHz	<30dBm	Table 2.2	Table 2.2	<50V/m
5,800 MHz	±75.0 MHz	<30dBm			<50V/m
24,125 MHz	±125.0 MHz	<57dBm	>33dBi		<2500mV/m
61.25 GHz	±250.0 MHz	<27dBm		<40dBm	<25uV/m at 300m
122.50 GHz	±500.0 MHz	<57dBm			<25uV/m at 300m
245.00 GHz	±1.0 GHz	<57dBm			<25uV/m at 300m

Table 2.2 FCC CFR Title 47 Part 15.247 Antenna Gain and Power to Antenna with Fixed Point to Point Operation in Band 2400-2483.5 MHz

Transmitted Power(dBm)	**Antenna Gain(dBi)**	**EIRP(dBm)**
30	6	36
29	9	38
28	12	40
27	15	42
26	18	44
25	21	46
24	24	48
23	27	50
22	30	52

2.2 Regulations for Maximum Exposure Limit and Local Heating

FCC 96-326 Appendix B sets the limitation for microwave exposure limit to the human body. Implantable devices fall into categories in Table 2.3(A). According to this table, utilizing 950 MHz frequency, the average power density over 6 minutes has to be smaller than 3.17 mW/cm^2. This limitation in power density can be achieved with either a power density of 3.17 mW/cm^2 with 100% duty cycle over 6 minutes or a power density of 63.4 mW/cm2 with 5% duty cycle, which translates to a 50 ms exposure every 1 second. As a result, operation duty cycle can be estimated according to this regulation.

Table 2.3 ANSI/IEEE C95.1-1992 (IEEE C95.1-1991) Radio Frequency Protection Guides

(A) Maximum Permissible Exposure (MPE): Controlled Environments Electromagnetic Fields

Freq Range (MHz)	Electric Field Strength E (V/m)	Magnetic Field Strength H (A/m)	Power Density (S) (mW/cm^2)	Averaging Time (minutes)
0.3-3	614	163	(100)*	6
3.0-30	1842/f	4.89/f	($900/f^2$)*	6
30-300	61.4	0.163	1	6
300-1500	--	--	f/300	6
1500-100,000	--	--	5	6

f= frequency in MHz, * = Plane-wave equivalent power density

(B) Limits for General Population/Uncontrolled Exposure

Freq Range (MHz)	Electric Field Strength E (V/m)	Magnetic Field Strength H (A/m)	Power Density (S) (mW/cm^2)	Averaging Time (minutes)
0.3-1.34	614	163	(100)*	30
1.34-30	824/f	2.19/f	($180/f^2$)*	30
30-300	27.5	0.073	0.2	30
300-1500	--	--	f/1500	30
1500-100,000	--	--	1.0	30

f= frequency in MHz, * = Plane-wave equivalent power density

Note 1 to Table 2.3: Occupational/controlled limits apply in situations in which persons are exposed as a consequence of their employment provided those persons are fully aware of the potential for exposure and can exercise control over their exposure. Limits for occupational/controlled exposure also apply in situations when an individual is

transient through a location where occupational/controlled limits apply provided he or she is made aware of the potential for exposure.

Note 2 to Table 2.3: General population/uncontrolled exposures apply in situations in which the general public may be exposed, or in which persons that are exposed as a consequence of their employment may not be fully aware of the potential for exposure or cannot exercise control over their exposure.

2.3 Wireless Energy Harvesting Methodology Comparison

2.3.1 Scalability with Distance

According to Biot-Savart and Faraday equation for inductive coupling using two coils, the voltage induced on the second coil decreases with R^3 and the power decreases by R^6. The induced voltage on the second coil can be written as $V = \oint_C E\, dl = -\int \frac{\partial B}{\partial t} \cdot ds$ and $\frac{\partial B}{\partial t} = \frac{\partial}{\partial t}\frac{\mu_0 b}{4R^3}(a_R 2\cos\theta + a_\theta \sin\theta)$[76], where C denotes the loop of the second coil, s is the surface of second coil, b is the radius of the first coil and R is the distance between first and the second coil. a_R and a_θ are the unit vectors pointing along the distance and angel θ from the axis perpendicular to the center of the first coil.

The far-field Friis equation describes the received to transmit power gain as $\frac{P_r}{P_t} = G_t G_r \left(\frac{\lambda}{4\pi R}\right)^2$, where P_r and P_t are received power at receiving antenna and transmitted power at transmitting antenna, respectively, G_t and G_r are transmitting and receiving antenna gain, respectively, λ is the wavelength, and R is the distance between two antennas. As a result, the received power degrades with square of the distance.

According to Fig. 2.1 from reference [49], horn antenna near-field power degradation is much less sensitive to the distance between the two antennas comparing to far-field for both E-plane and H-plane as shown in Fig. 2.1. Therefore, wireless harvesting with near-field is will be less sensitive to distance comparing to coil inductive coupling and can operate with further distance.

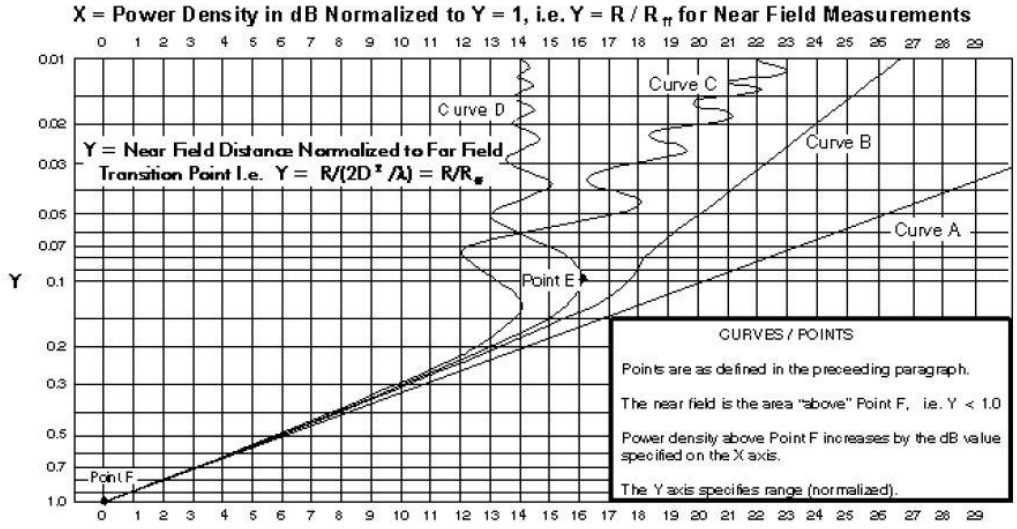


Figure 2.1 Antenna Near-Field On-Axis Power Densities (Normalized) for Various Aperture Illuminations. A: Using far-field equation for reference only. B: Power density variations on axis for an antenna aperture with a cosine amplitude distribution. This is typical of a horn antenna in the H-plane. C: Power density variations on axis for a uniformly illuminated antenna aperture or for a line source. This is typical of a horn antenna in the E-plane. D: power density variations on axis for an antenna aperture with a tapered illumination. Generally the edge illumination is approximately -10 dB from the center illumination and is typical of a parabolic dish antenna. [49]

Compared to inductive coupling with lower frequency range, near-field and far-field communication supports larger distance between reader and tag with smaller antenna design. There are several reports on far-field communication platforms with on-chip antenna demonstration with operating distances ranging from centimeters to meters

[1, 2, 5, 14-19]. A high data rate can be achieved by utilizing a higher carrier frequency at the cost of larger power dissipation.

2.3.2 Scalability with Size

According to reference [28], a miniature antenna with an area of 0.2 λ_0 × 0.2 λ_0 and a gain of -3 dBi is achieved. In this thesis, an antenna is targeted that has a soze of only 0.002 λ_0 ×0.002 λ_0 while the gain is only -56 dBi. On the other hand, the induced voltage on the second coil (receive antenna) for inductive coupling is proportional to the area of the coil according to Faraday law as discussed in the previous section. Therefore, power induced on the secondary coil has linear relationship with the square of the coil area. A reduction in the area from 0.2 λ_0 × 0.2 λ_0 to 0.002 λ_0 ×0.002 λ_0 will lead to a decrease in the area with the factor of 0.01^2. Therefore, a reduction of the induced power by -80 dB is expected. Note that the designed miniature slot antenna has only -53 dBi reduction of power gain, which may hint at the benefits of scaling down as well as the optimal design of the antenna.

2.4 Integrated On-chip Rectenna Fabricated and Tested in GF 45nm SOI

2.4.1 On-chip Antenna Design in GF 45 nm SOI

In reference [1], a dual antenna design with a dipole-loop structure, with resistive and inductive stubs in CMOS 0.18 μm is implemented. The antenna operates at 5.8 GHz for receive and in 3.1-10.6 GHz ultra-wide band (UWB) using impulse-radio for transmit with an area of 4.5 mm^2. The receive antenna scavenges 0.45 μW with 1V DC voltage output at 7.5 cm away from 36 dBm EIRP source. Both transmitting and receiving

antenna are folded-dipoles. A dual on-chip antenna designed at 5.2 GHz for receiving and 2.4 GHz for transmitting implemented in 0.18 μm standard CMOS process with an area of 4.8 mm^2 is demonstrated in [17]. The antenna has a simulated -14.3 dBi receiving gain and a -28.8 dBi transmitting gain and a rectified 1.1 V output voltage with 36 dBm EIRP source at 3 cm distance. Reference [2] uses a 0.125 mm^2 on-chip coil implemented in 65 nm CMOS technology to scavenge 10.5 μW with 1 mm distance from 50 mW transmit power at 1.5 GHz. A printed dipole horn on-chip antenna in 0.18 μm CMOS process operating at 24 GHz is demonstrated in [5]. The antenna has 6.77 dBi simulated gain. The antenna combined with on-chip rectifier can source out 1 μW of output DC power and 1V DC voltage with -2 dBm input power at the antenna. Reference [15] has a dual-band corrugated linaer tapered slot antenna (LTSA) operating in the frequency range of 35 to 94GHz with an area of 2.9mm^2 implemented in CMOS 0.13 μm technology. The measured gain of the antenna is 7.4 and 6.5 dBi. However, this work does not consider or calibrate the receiving power from ground-signal-ground (G-S-G) on wafer probe nor the reflection caused by the probe or environment. The rectifier integrated with antenna circuit (rectenna) rectifies an output power of 1.6 mW at 35 GHz and 0.6 mW at 94 GHz with effective isotropic radiated power (EIRP) of 52 dBi source at a distance of 90 cm. A dual antenna operating at 24 GHz folded-dipole for receiver and 60 GHz dipole for transmitter has been designed in 65 nm CMOS technology with 3.7 mm × 1.2 mm of area. The receiving antenna is designed to have -2.5 dBi gain and transmitting antenna with 0 dBi. In Table 2.5 most on-chip antennas that have been published in the literature so far have been compared.

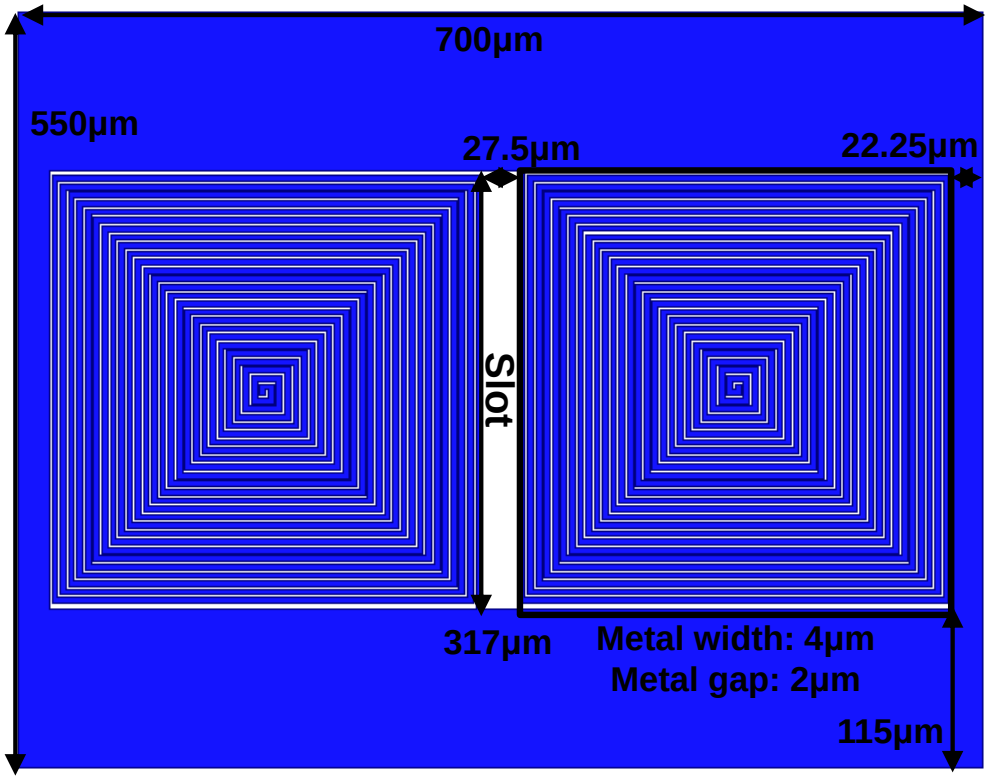
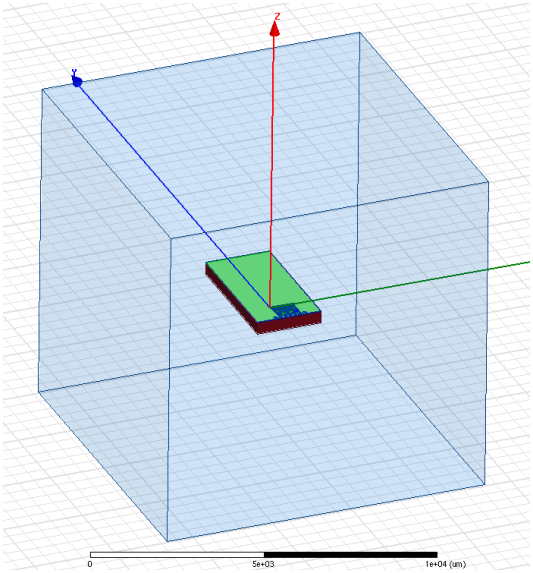


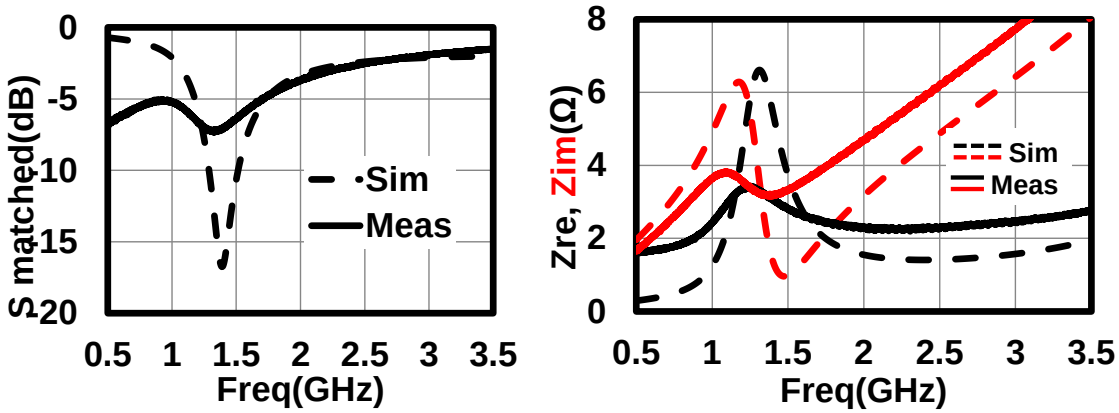
Figure 2.2 On-chip antenna designed in 45nm CMOS SOI dimensions

The on-chip antenna designed here is based on the approach used in reference [27] and [28]. The miniature slot antenna was chosen rather than a miniature dipole antenna because it can intercept more power with larger ground plane. Note that a miniature dipole antenna can only intercept power with its wired portion. Furthermore, miniature slot structure provides already existing large metal ground plane that can be implemented directly on the accompanying system-on-chip (SoC) circuitry without affecting antenna performance. The design structure and dimensions are shown in Fig. 2.2. The miniaturization was achieved from creating voltage discontinuity at two end of the slot with a length much shorter than $\frac{\lambda}{2}$, where λ is the wavelength at the operating frequency. The voltage discontinuity is created by loaded impedance of $X_t = Z_{0s} tan \frac{2\pi}{\lambda} \times \frac{1}{2}\left(\frac{\lambda_s}{2} - l\right)$,

where Z_{0s} is the characteristic impedance, λ_s is the guided wavelength of the slot line and l is the length of slot line [28]. The loaded impedance can be constructed with smaller series slot line with lengths less than $\frac{\lambda}{4}$ for inductive loading. The relation of impedance of the series smaller slot line is $\frac{X_t}{2} = Z'_{0s} tan \frac{2\pi}{\lambda'_s} l'$, where Z'_{0s} is the characteristic impedance, λ'_s is the guided wavelength and l' is the length of terminating slot line. The final antenna size in a 45nm CMOS SOI technology is 700 μm×550 μm for a 1.3 GHz operating frequency. Slot line width of 27.5 μm, length of 316.7 μm and terminating slot line width of 2 μm and total length of 1.8 mm are used. According to [28], the longer the terminating slot line is the higher impedance it has. However, there is a limit set by antenna rules of the semiconductor manufacturing process that requires a minimum distance between metals and minimum width of metals.



(a)



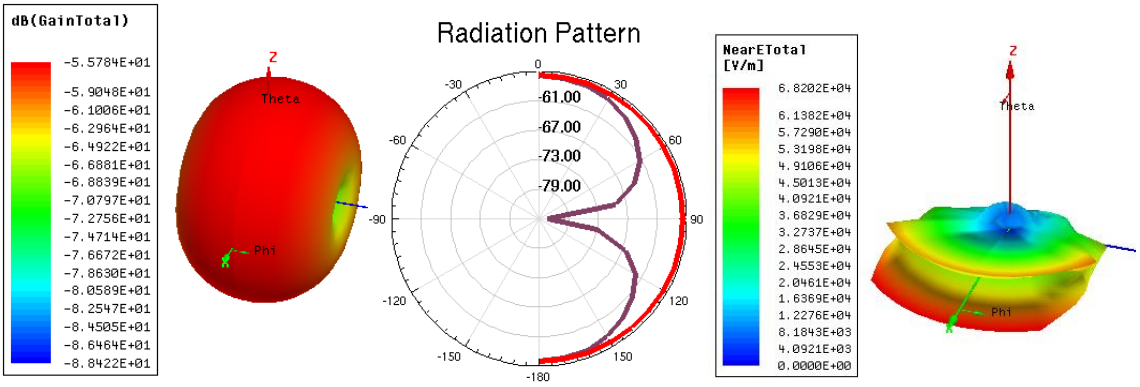
(b) (c)

Figure 2.3 (a) HFSS simulation model, (b) Simulated and measured S parameter, (c) Z parameter of Antenna

Fig. 2.3 (b, c) shows the simulated reflection coefficient (S11) as well as real and imaginary parts of the input impedance of the antenna from 0.5 to 3.5 GHz. The simulations show a resonance at 1.3 GHz, with antenna impedance of 6.6 + j3.6 Ω, which corresponds to the input reflection coefficient of S11 = -16.75 dB for a 6.6 Ω impedance environment, which matches the input impedance of the rectifier when the input power is around -4.2 dBm. The Ansys HFSS simulation model setup is shown in Fig. 2(a). As expected, the conductive nature of the substrate led to reduced radiation resistance and increased bandwidth of the antenna. While the antenna dimensions are very small compared to the wavelength, it is still effective in harvesting the power from its environment.

On-chip antenna and connecting feed lines are measured with a Keysight E8361A PNA vector network analyzer and Cascade probe station using a SOLT calibration. Measurement showed that the first resonance of an unloaded antenna occurs at 1.26 GHz presenting an impedance of 3.4 + j3.4 Ω and reflection coefficient of S11 = -7.34 dB for a

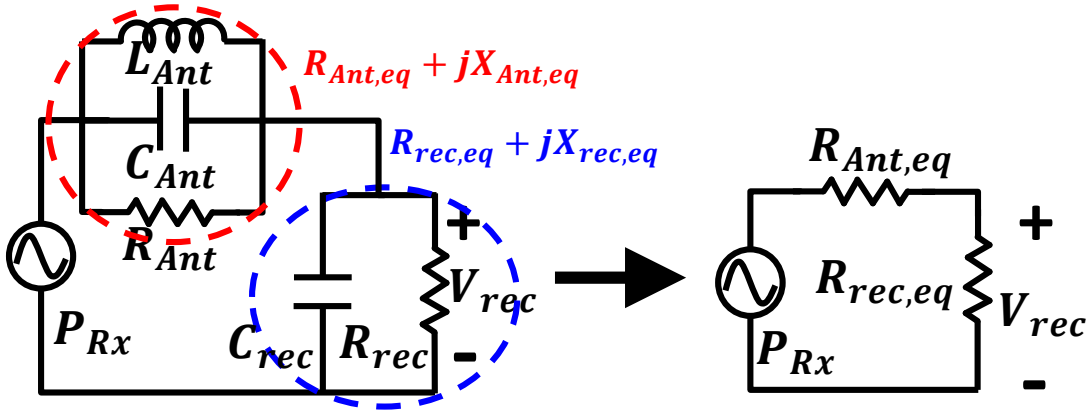
3.4 Ω impedance environment as shown in Fig. 2.3 (b, c). While measured first resonant frequency is very close to the simulated value, there is a slight difference in the measured and simulated impedances of the antenna, which is possibly due to the choice of metal conductivity or substrate resistivity parameters selected in the ANSYS HFSS environment.



(a) (b) (c)

Figure 2.4 (a) Antenna Far Field Radiation Pattern at 1.3GHz in ANSYS HFSS and (b) Radiation Pattern and (c) Near Field E-field Distribution with 20 mW Applied at Antenna Port

2.4.2 On-chip Antenna and Rectifier Integration



(a) (b)

Figure 2.5 (a) Rectenna Circuit Model (b) Rectenna Circuit Model at Resonance

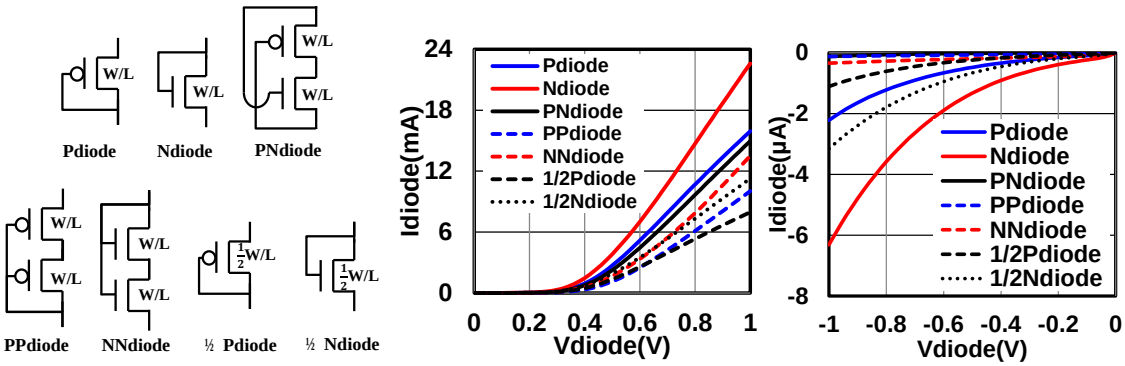
Reference [51] derived the model of RF-DC rectifier equation and led to the conclusion that output voltage has direct relation to the rectifier input voltage as shown by the following equation:

$$V_{out,rec} = V_{rec} - V_{th} - \left(\frac{15\pi}{8}\frac{I_{forward}\sqrt{2V_{rec}}}{\mu_n C_{ox}}\right)^{\frac{2}{5}} \quad (2.1)$$

In addition, according to [19], at resonance reactance of zero, $R_{Ant,eq}$ is the transformed resistance from R_{Ant}, L_{Ant} and C_{Ant}, and $R_{rec,eq}$ is the transformed resistance from R_{rec} and C_{rec}. The rectified voltage is strongly related to the rectifier input voltage $V_{RF} = \sqrt{(1-|\Gamma|^2)P_{Rx} * (R_{rec})}$, where $\Gamma = \frac{R_{rec}-R_A}{R_{rec}+R_A}, 0 \leq |\Gamma| \leq 1$ is the reflection coefficient between antenna and the rectifier interface. Therefore the maxima of V_{RF} occurs when R_{rec} is maximum and $R_A = R_{rec}$ leading to Γ =0. As a result, the best wireless harvesting at RF frequencies for this antenna will be at frequencies around 1.3 GHz because of the maximum real part of the impedance of the antenna. From equations (2.1) and (2.2) we can come to the conclusion that the optimization of the Rectenna integration is a combination of power matching and voltage applied to the rectifier input.

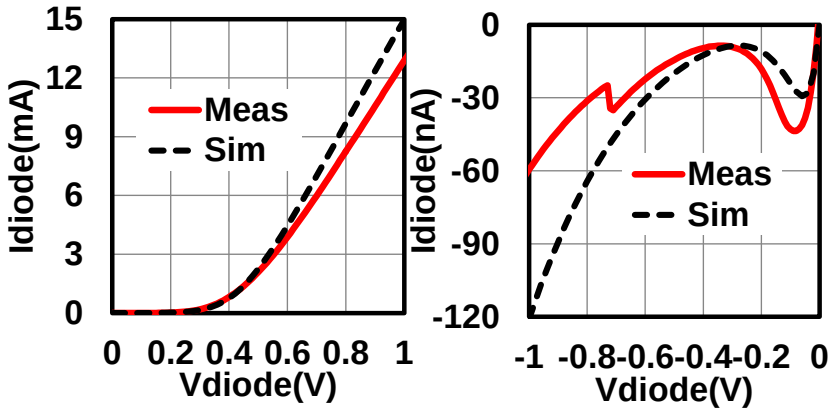
The closer the rectifier resistance to the antenna resistance at resonance, the smaller the reflection power is. On the other hand, on-chip antenna has a small resonance resistance originated from the loss of the silicon substrate while rectifier has large input resistance caused by diode non-linear operation at weak inversion. In order to improve the matching between the antenna and rectifier, one can add an on-chip inductor as part of a matching network. Unfortunately, high losses of the on-chip inductor with low

quality factors (Q~6) and its large area and the possibility of coupling between the inductor and the on-chip antenna make this approach undesirable. Therefore, in order to have a proper matching between the antenna and the rectifier, rectifier transistor width must deviate much from its optimum size for maximum power converted efficiency (PCE.) An alternative approach is to bring the two resistances close to each other by increasing the resistance of the antenna at resonance through utilizing high resistivity Si substrate or by removing the substrate. Same antenna design with high resistivity Si substrate has been implemented and compared with an antenna on a standard low resistivity silicon substrate in section 2.1.2.6.



(a) (b) (c)

Figure 2.6 (a) Diode Topologies, (b) Schematic Simulation of Forward Biased and (c) Reverse Biased Current for Each Diode Topology



(a) (b)

Figure 2.7 Measured Fabricated and Simulated PN Diode (a) Forward Biased Current and Reverse Biased Current

2.4.3 Rectifier Design Optimization for Maximum Efficiency

Small form factor is a crucial requirement when it comes to miniaturized sensor nodes design. As a result, topologies that require large inductors for DC bias are undesirable [54-56] that lead us to differential or single ended drive topology rectifiers.

Rectifier loss comes from diode resistive loss, diode turn on voltage and reverse leakage current [26]. Methods of transistor threshold voltage cancelation have been proposed in [57-60, 75.] The high efficiency obtained from optimum timing of switching on and off of transistors in topologies presented in [57-58] are technology dependent and will lead to premature transistor turn on, which in turn causes large amount of leakage current. References [59-60] delay transistor turn on time in order to reduce reverse leakage current due to premature transistor turning on with additional comparator and delay circuits. Reference [59] was designed for 13.5 MHz rectifiers and reference [60] was designed for 1.5 MHz. This solution is not suitable for UHF frequencies applications

as the accuracy of a fixed delay would be challenging as the period of the signal drastically reduced and can deviate much from process corner.

In terms of optimizing transistor diode size of rectifiers, using larger diode size leads to smaller resistive loss but also higher reverse leakage current. Therefore, with the trade-off between resistive loss and reverse leakage current, there is an optimum diode size with each topology. Power conversion Efficiency *PCE* of the rectifier is defined as $PCE(\%) = {V_{Load}}^2/R_{Load}P_{rec,in}$, where $P_{rec,in}$ is the received rectifier power [51]:

$$P_{rec,in} = I_{LeakP}\left(V_{th} + \frac{6}{7}V_{D,FOVP}\right) + I_{Load}\left(V_{th} + \frac{6}{7}V_{D,FOVP}\right) + P_{Leak} \quad (2.2)$$

where V_{Load} and I_{Load} are the load voltage and current, $V_{Diode,FOVP}$ is is the peak diode overdrive voltage $\left(V_{rec,inP} - V_{Load} - V_{th}\right)$ and $V_{rec,inP}$ is the peak input voltage of the rectifier. In order to maximize *PCE*, one has to maximize the load current of the rectifier I_{Load} at a certain rectifier input power and the peak forward overdrive diode voltage $V_{D,FOVP}$ since it is related to root of forward bias current, and at the same time, minimize the following three components: The peak reverse leakage current of the diode I_{LeakP} and the threshold voltage V_{th} of the diode, which is dominated by the threshold voltage of the transistors used in the diode configuration.

Different topologies of diode-connected CMOS transistors are shown in Fig. 2.6(a). Simulated forward bias currents and reverse leakage currents of these topologies are compared in Figs. 2.6(b) and (c), respectively. With transistor threshold voltage of

~0.3 V these topologies provide similar diode threshold voltage V_{th} as shown in Fig. 2.6(c). The results indicate that PN diode is an optimum choice with one of the lowest leakage current and the highest forward current.

Cadence Spectre simulation for *PCE* of a full bridge rectifier using various diode-connected designs shown in Fig. 2.6(a) was conducted and transistor sizes were optimized to achieve the highest *PCE* at relatively low input powers. The results demonstrated PN and PP diodes achieve high *PCE* (77 %), with PN diode being a better choice due to its smaller input power The rectifier was designed with cross-coupled MOSFET diodes due to their lower reverse leakage currents comparing with other MOSFET diode configurations. Reverse current would cause charge originally stored on output load flow back to the RF input node when the diode is reversed biased. For a 50 μA target load consumption, a reverse current of a micro amp is significant. As shown in Fig. 2.6 (b), single PMOS or NMOS transistors have higher reverse leakage current even if their size is reduced by half. Series connected MOSFET diode has smaller reverse leakage current and cross coupled PMOS and NMOS pair has the smallest, leading to this topology to have the largest size diode at the optimum operation frequency compared to other topologies. Notice that the topology of cross-coupled MOSFET does not increase the turn on voltage and it would be the same as the higher threshold voltage between NMOS and PMOS transistors.

The post-layout simulated rectifier with 20 kΩ and 1 kΩ is shown in Fig. 2.8. The maximum *PCE* of 72% has 5% difference from schematic simulation due to parasitic passives from layout.

Table 2.4 Comparison of Rectifiers at Maximum PCE

Topology	**MaxPCE(%)**	**Prec,in(dBm)**	**Vload(V)**	**VdiodeP(V)**
Pdiode	59.3	-8.35	1.31	0.69
Ndiode	53.2	-11.33	0.886	0.47
PNdiode	**77.1**	**-4.45**	**2.35**	**1.22**
PPdiode	77.5	-2.27	3.03	1.59
NNdiode	73.5	-4.39	2.31	1.2
1/2 Pdiode	61.7	-7.6	1.46	0.77
1/2 Ndiode	56.5	-9.66	1.1	0.58

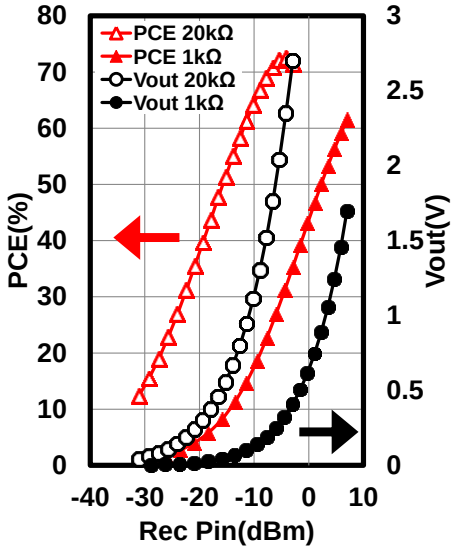


Figure 2.8 Post-layout simulated rectifier PCE and output voltage with 1 kΩ and 20 kΩ load resistance

2.4.4 Rectenna with Regular Low Resistivity Silicon Substrate in GF 45 nm SOI Measurement

Measurement using a 4-port Precision network analyzer (PNA) with differential input is required to achieve balanced S-parameter measurement in order to verify the rectifier design in the same way demonstrated in [23]. On-chip antenna measurement has always been a challenge due to reflection of probe station and comparably high inductance of packaging material such as wire bond. In order to solve the probe station reflection, measurement with customized wood made probe station have been proposed [22]. On-chip antenna measurement while integrated with rectifier and calibrated with rectifier individual measurement is an alternate approach, which has been utilized for antenna and rectifier performance characterizations in this Thesis.

According to [20] and [21], a rule of thumb to estimate whether antenna is working in near-field coupling or far-field charging for an electrically small antenna is $r = \frac{\lambda}{2\pi}$, where r is the distance from the tag antenna, (λ is the wavelength, λ = 230.77 mm in air for 1.3 GHz), leading to a distance r ~ 3.7 cm. On the other hand, the threshold distance to differentiate near-field and far-field operation of a horn antenna would be $r = \frac{2D^2}{\lambda}$, where D is the largest antenna dimension [20]. The largest dimension of the horn antenna used in the measurement setup is 244 mm (A-info 1080 antenna), leading to r ~ 516 mm at 1.3 GHz. Therefore when the tag antenna is placed within 51.6 cm from the horn antenna, it will be operating in near field coupling.

The RF-DC rectifier and antenna circuit (rectenna) has a double folded slot antenna and a differential rectifier as shown in Fig.2.9. A rectifier with cross-coupled P-channel and N-channel mosfets is designed to reduce back flowing leakage current from the load capacitor as shown in Fig. 2.10. A load resistor is soldered off-chip.

The antenna and rectifier are designed with and without on-chip matching network. While the matching network is optimized to enhance the antenna performance during the simulation, the design with on-chip matching components yielded inferior performance as the matching inductor consumes significant portion of accepted power. This is due to the fact that during the simulation, the conductive loss of the matching inductor was calculated from Cu bulk conductivity, but in reality, the conductivity of the thin film Cu was smaller than the bulk value. The micrograph of the antenna implemented in GF 45nm CMOS SOI technology is shown in Fig. 2.9 and its equivalent circuit is shown in Fig. 2.10 for a circuit without matching components.

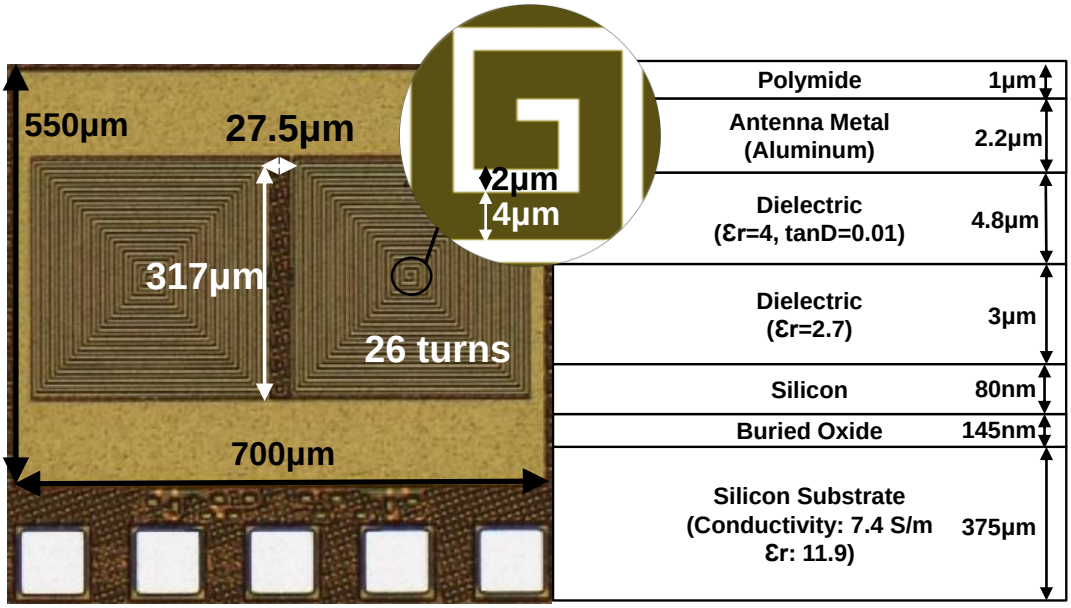


Figure 2.9 On-chip Rectenna Circuit Micrograph Fabricated with GF 45nm SOI Process

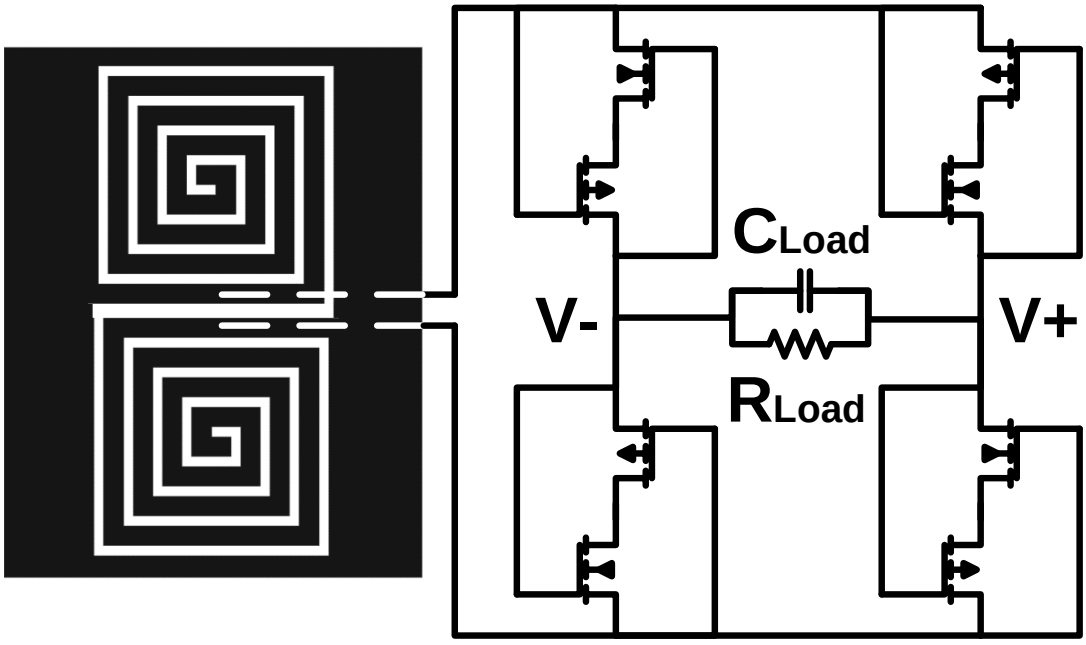


Figure 2.10 Schematic of Rectenna Fabricated with GF 45nm SOI Process

The measurement of the rectenna has been done with convoluted absorber ETS Lindgren CV-05CL absorber, which is rated to have more than -20 dB attenuation starting from 1 GHz. The measurement is performed with signal excitation from a high-

performance 6 GHz Signal Generator (Agilent 8665B) and amplified with HP 8349B 2-20 GHz power amplifier along with Mini Circuits 800 MHz – 2000 MHz ZHL-10W-2G+ to cover the frequency range of the measurement.

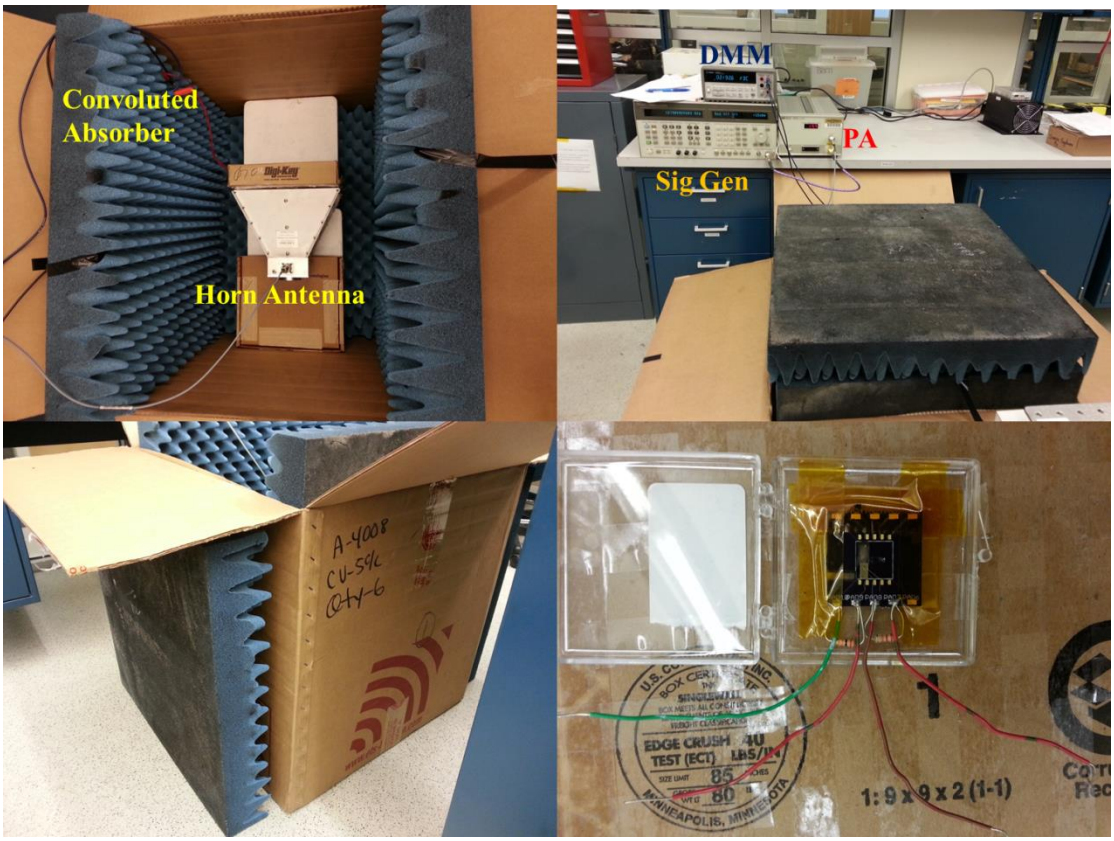


Figure 2.11 GF 45nm SOI Rectenna Near-field Wireless Harvesting Measurement Set Up

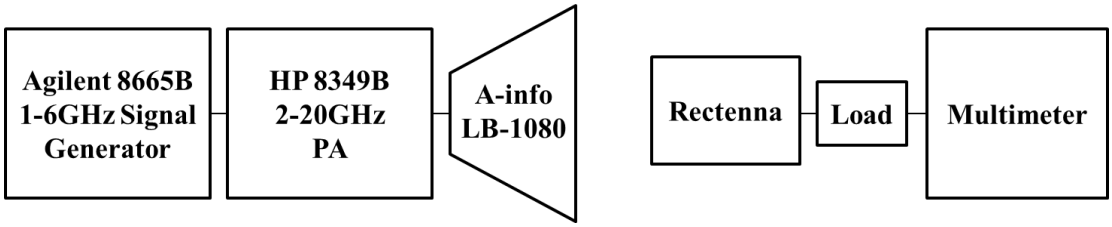


Figure 2.12 On-chip Rectenna Near Field Wireless Harvesting Measurement Set Up Diagram

The measurement set up is shown in Fig. 2.11 and measurement is performed from 0.1 GHz to 6 GHz and with power amplifier output power of 21 dBm EIRP with

load resistance of 20 kΩ for searching resonance frequency of rectenna to be 950 MHz as shown in Fig. 2.13. The 20 kOhm resistive load was connected at the output of the rectanna to emulate the load of the RFID tag chip.

Fig. 2.15 depicts the measurement of the rectenna (antenna together with a rectifier implemented separately) performed with a load resistance ranging from 1 KΩ to 20 KΩ with a power source having an effective isotropic radiated power (EIRP) of ~36 dBm. The measurements are performed at various distances between the source horn antenna (A-info 1080) and the CMOS rectenna. Note that the resonance frequency of the rectenna is shifted to a lower value of 0.95 GHz compared to that of the antenna alone (1.26 GHz) due to the loading effect of large transistors used in the rectifier. The circuit achieves an output voltage higher than 1 V with a delivered DC power of 50 μW at 0.95 GHz for distances below 16 cm. Moreover, with a 1 KΩ load, one can achieve a DC output voltage of 1.2 with a DC power of 1.44 mW for distances below 2 cm. The rectenna shows a wide bandwidth of 0.9 to 1.3 GHz when the input frequency is swept while the output voltage is recorded. The wide bandwidth of the antenna is attributed to its low radiation resistance and the lack of a matching network. Power density at the rectenna is also characterized with an Aaronia PBS1 near field probe set, which measured magnetic and electric fields of 0.23 μT and 398.1 V/m, respectively, at a distance of 16 cm away from the source antenna with 36 dBm EIRP power.

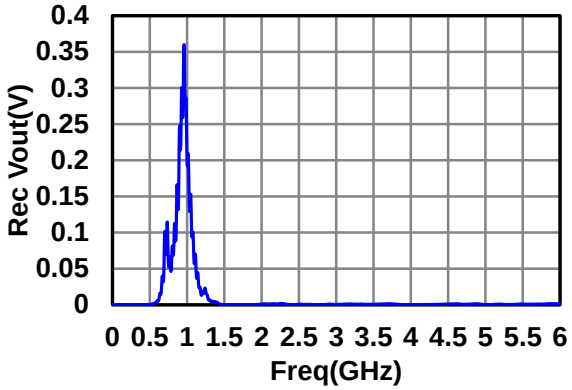
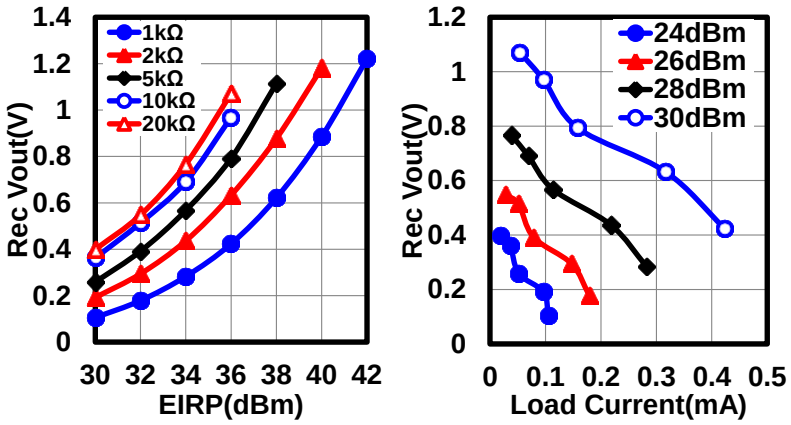


Figure 2.13 Rectified Output Voltage with 21 dBm EIRP Source with Different Frequency



(a) (b)

Figure 2.14 Rectified Output Voltages with Distance of 16 cm from Transmitting Antenna and Different Load and Input Power

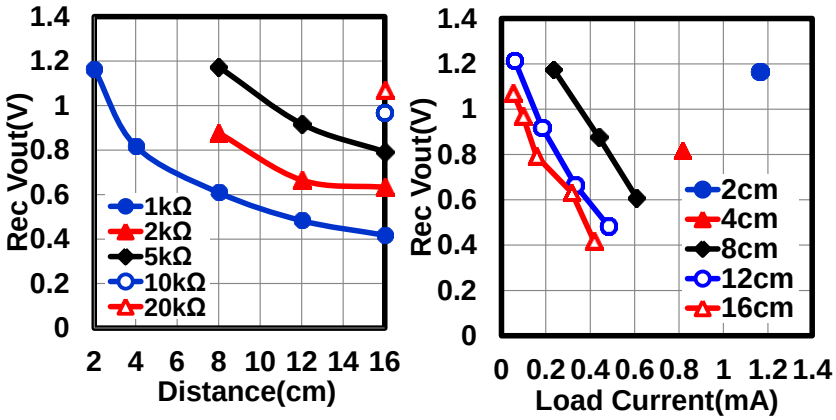


Figure 2.15 Rectified Output Voltages with Source Power of 36 dBm EIRP and Different Load and Distance from Transmitting Antenna

The antenna performance is compared with other on-chip rectennas in Table 2.5. The proposed rectenna circuit occupies smaller area than all the other work except [2]. However, it shows higher rectified output DC power (50μW) with larger distance (2 cm) though characterized with 10.2dB higher EIRP input power (30.8dBm) as Reference [2] achieves a rectified DC power of 10.5μW with 20.6dBm EIRP source placed 5 mm away.

Table 2.5 On-chip CMOS Rectenna Comparison

Ref	**Tech**	**Freq (GHz)**	**Gain (dBi)**	**Pin (dBm)**	**Dis (cm)**	**V_{out} (V)**	**I_{out} (μA)**	**Pout (μW)**	**A (mm^2)**
[1]	0.18um CMOS	5.8	NA	36 EIRP	7.5	1	0.45	0.45	4.5
[2]	65nm CMOS	1.5	NA	17	0.1	0.7	1.5	10.5	0.125
[14]	65nm CMOS	30	-1.68 sim @60 GHz	15	2	1.14	1.14	1.3	NA
[15]	0.13um CMOS	35	7.4	$30\frac{mW}{cm^2}$ at device	20	0.4	4000	1600	2.9 with pad
		94	6.5			0.3	2000	600	
[17]	0.18um CMOS	5.2	-14.3 sim	36 EIRP	3	1.1	NA	NA	4.8
[18]	65nm CMOS	24	NA	40 EIRP	28	0.9	1.7	1.5	<4.44
This work *	**45nm CMOS SOI**	**0.95**	**-50 sim**	**30, 36 EIRP**	**16**	**1**	**50**	**50**	**0.42**

2.4.5 Measurement of GF 45 nm CMOS SOI with Bio Tissue

Measurement of the Rectenna on low resistivity Si substrate has been conducted with a 1 cm thick chicken breast tissue placed between the Rectenna and the transmitting horn

antenna (A-info 1080). The measurement setup uses a Keysight 8665B signal generator and ZHL-10W-2G+ driver amplifier to amplify the input signal to the horn antenna. The measured performance of the Rectenna on low-resistivity Si substrate with and without the bio tissue is shown in Fig. 16. As shown in Fig. 16 (a), with a 1 cm thick chicken breast and at a distance of 4 cm away from the transmitting horn antenna with 36 dBm equivalent isotropically radiated power (EIRP), the output voltage of the Rectenna peaks at 1.02 V with a dc power of 52 μW when a 20 kΩ load is used. The performance comparison of the Rectenna on low-resistivity Si substrate with and without the bio tissue is shown in Fig. 2.16(b). In both cases, the Rectenna is placed at 8 cm distance away from the horn antenna. The Rectenna with the bio tissue on top requires 6 dBm more power compared to the one without the bio tissue to achieve the same amount of output voltage and dc output power. Nevertheless, the measured performance demonstrates the possibility of device operation under relatively thin tissues.

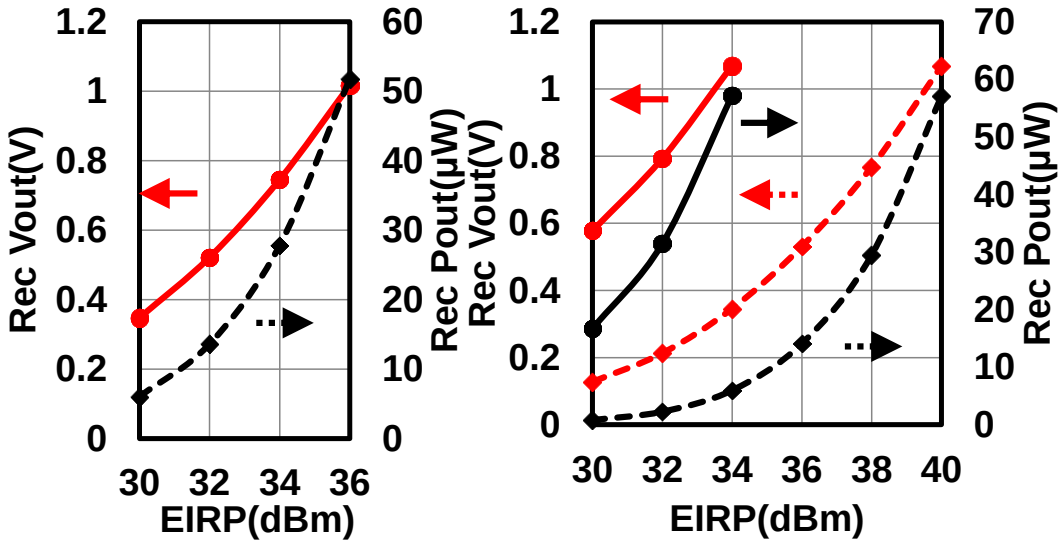


Figure 2.16 (a) Measured Rectenna Rectified Voltage and Power with 1 cm Chicken Breast Covering the Rectenna at 4 cm Distance from the Transmitting Antenna. (b)

Measured rectified Voltage and Power with (dashed line) and without (solid line) 1 cm Chicken Breast Covering the Rectenna at 8 cm Distance from the Transmitting Antenna.

Table 2.6 Comparison of On-Chip Rectennas for Biomedical Implants

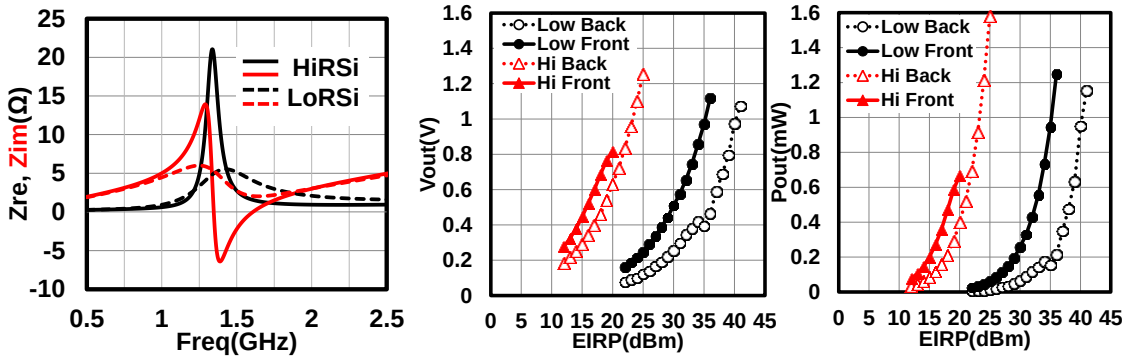
Ref	[17]	[2]	[52]	[53]	**This work***
Tech	0.18μm CMOS	65nm CMOS	4μm Au/ SMMFD101 core	Cu/ SMMFD101 core	**45nm CMOS SOI**
Freq(GHz)	5.2	1.5	0.25	0.3	**0.95**
Pin(W)	5 EIRP	0.05	0.011	NA	**1**
Pout(μW)	513	10.5	76.4	19600	**52**
Vrec(V)	1.15	0.7	NA	NA	**1.02**
Media	5 mm saline water/ 25 mm air	0.6 mm brain tissue	3 mm Air	11 mm liquid/ 5 mm air	**10 mm chicken breast/ 30 mm air**
Topology	NA	Coil	Cylindrical Loop	Loop	**Folded Slot**
Tx Device	Patch Ant	Coil	Loop Ant	Two Turn Ant	**Horn Ant**
Size(mm^3)	1.4	0.125*thickness	1	8	**0.163**

2.4.6 Measured Performance Comparison between High Resistivity Silicon Substrate and Regular Low Resistivity Silicon Substrate

A comparison between simulated impedance of the antenna with the standard low resistivity silicon substrate and a high-resistivity silicon substrate is shown in Fig. 2.17(a). The resonance frequency of the antenna on high resistivity (ρ = 1 kΩ.cm) silicon substrate is 100 MHz lower while the resistance is 15 Ω higher than those of the device on low resistivity (ρ = 13.5 Ω.cm) substrate, leading to higher input voltage at resonance for identical input powers. A comparison between measured Rectenna performance with standard low-resistivity silicon substrate and high-resistivity silicon substrate is shown in

Fig. 2.17(b, c). A 1 kΩ load resistance is utilized as the load. The distance between the Rectenna and transmitting horn antenna is very small for this measurement. To identify how much of the signal goes through the substrate, the Rectenna is placed with either front or back of the chip facing the electromagnetic radiation. This study is important as the implant may be accidentally placed upside down or may turn upside down by moving tissues. The orientation of the implantable device is hard to control once the device form factor goes below 1 mm^2 and good performance with both orientations is crucial.

The Rectenna on high resistivity Si substrate generally needs 13 dB less power to achieve the same output performance as the one on low-resistivity substrate. The Rectenna with high resistivity substrate is able to harvest 1.2 mW and 1.1 V with only 18 dBm from the power amplifier, which translates into an EIRP of 24 dBm. It is interesting to note that the high resistivity substrate not only requires much less power from the horn antenna to generate the same output, it also is more transparent to the incoming electromagnetic radiation. The Rectenna on high resistivity substrate requires only 2 to 3 dB more power if it faces the horn antenna from its backside compared to its front side. On the other hand, the Rectenna on the low resistivity Si substrate requires 5 to 6 dB more power to achieve the same rectified voltage and power while operating from the back compared to the front side of the chip.



(a) (b) (c)

Figure 2.17 (a) Simulated Real and Imaginary Parts of Antenna Impedance with High and Low Resistivity Substrates. Measured (b) Rectified Output Voltage and (c) Output Power of Rectenna on Low Resistivity and High Resistivity Silicon Substrates when Transmitted Power is Radiated from Front and Back of Rectenna.

2.4.7 Simulated Performance Comparison between with Low Resistivity Silicon Substrate and without Silicon Substrate

Impedance of antenna with standard low resistivity silicon substrate and without silicon substrate is simulated and compared in Fig. 18. The resonant resistance of antenna without silicon substrate increased from 6.6 Ω to 40.5 Ω. Increasing resonant resistance is beneficial for matching between antenna and rectifier thus reduces the matching loss. And resonant frequency increased from 1.3 GHz to 2.5 GHz. The resonant frequency 2.5 GHz still lays inside the optimum frequency for biomedical implants. The sensor node was released from silicon substrate using the process described in work [63.] Fig. 2.19(a) shows the design for post-process releasing from silicon die and Fig. 2.19(b) shows the post-processed thinned downed chiplet with thickness around 10 μm compared to the original die thickness of 400 μm.

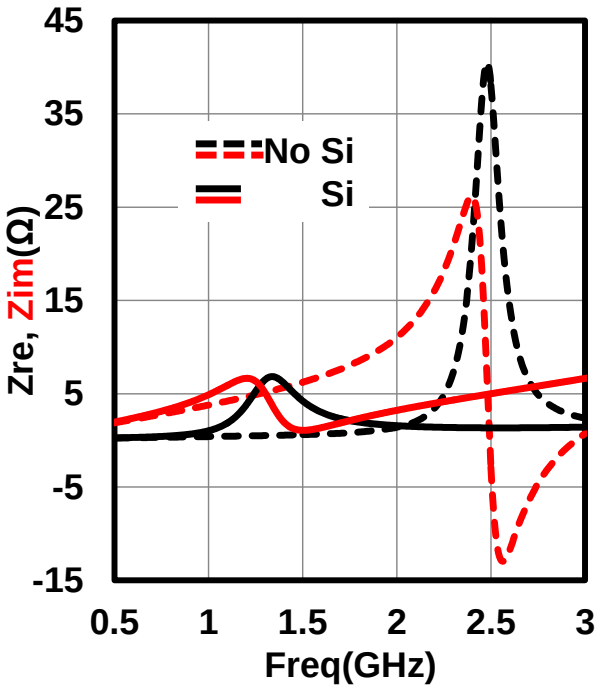
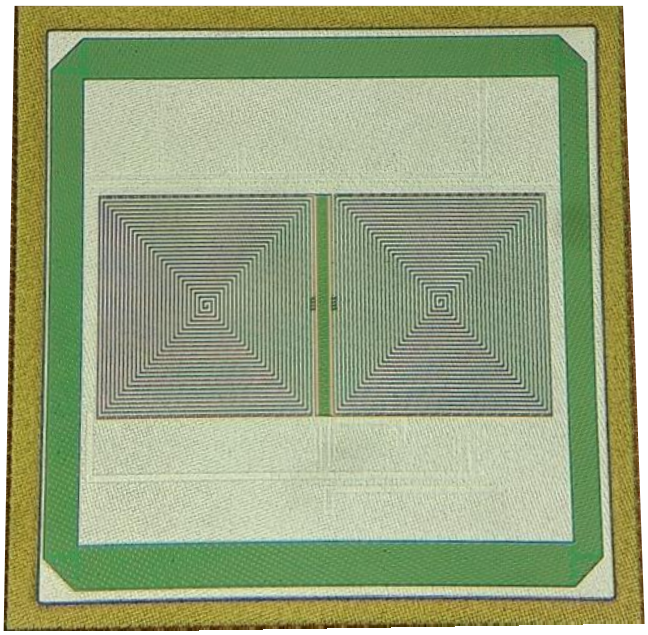
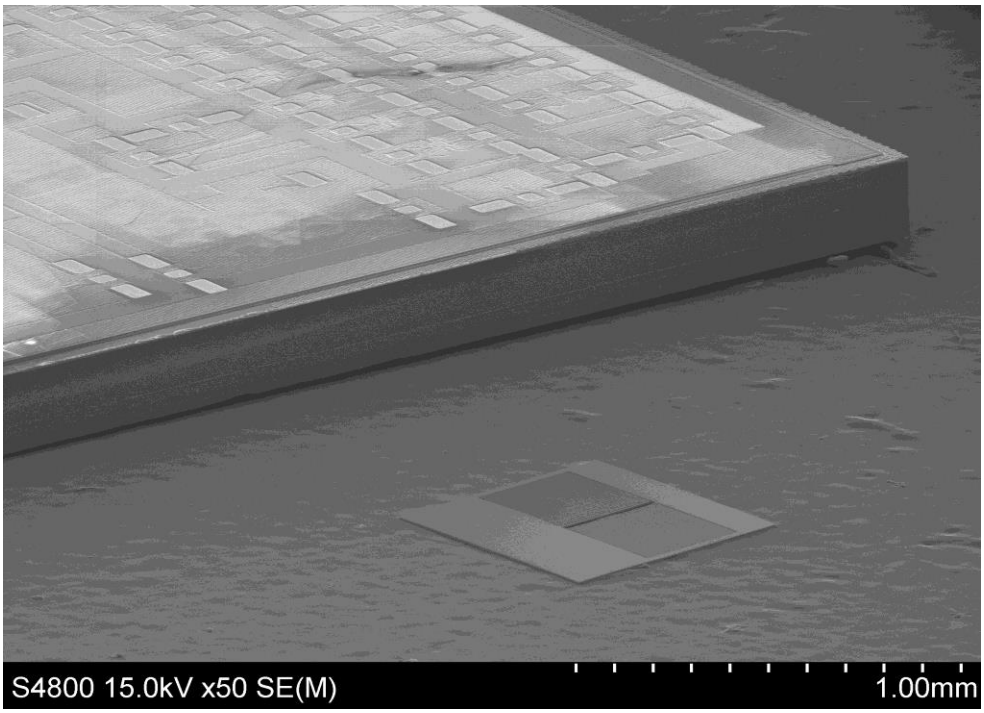


Figure 2.18 Simulated Antenna Impedance with Standard Low Resistivity Silicon Substrate and with Silicon Substrate Removed.



(a)



(b)

Figure 2.19 (a) Micrograph of Integrated Passive Sensor Node in GF 45nm CMOS SOI Technology for Post-processing Releasing from Silicon Substrate (b) Sensor Node after Post-processed Thinned Down to $\approx 10\mu m$ Thick Next to Orginal 400μm Thick Silicon Die. [Picture courtesy of Hossein Pajouhi]

3. FRONT END DESIGN: MODULATION SCHEME, DEMODULATOR AND MODULATOR DESIGN

The following sections describe the uplink and downlink modulation scheme choice as well as demodulator and modulator designs implemented in GF 45 nm CMOS technology. Reader front-end design will be discussed in this chapter as well.

3.1 Downlink and Uplink Modulation Scheme

The downlink utilized in this work is based on On-Off Keying (OOK) digital modulation scheme due to its simplicity and low power consumption of the demodulator design. OOK is well suited for ultra-low power circuit downlink that require data rate ranging from several hundreds of kilo-bit-per-second (kbps) to mega-bit-per-second (Mbps) as widely demonstrated in the literatures [2, 5, 6, 10, 36, 38, 39, 40, 41, 43, 47, 48]. Previous work has presented uplink modulation using three major methods: back-scattering [2, 4, 5, 6, 37, 40, 43,] ultra-wide band (UWB) transmitter and pulsed, OOK, FSK or BPSK transmitter with a different frequency than the RF input [7, 9, 10, 18, 35, 36, 39, 41, 42, 44 – 48, 50]. Previous designs that utilize transmitters operating at a frequency other than the input RF frequency typically need a separate transmitting antenna, which increases the design area, since energy harvesting path cannot be turned off at any time during the operation [7, 18, 35, 36, 39, 41, and 42]. An alternative solution is to have a different energy harvesting strategy [9, 10, and 13]. Therefore, these designs

would need additional environmental condition for operation as discussed in Chapter 2. References [44- 48] use power supplies based on thin-film battery, which may be undesired for implantable and low cost applications. Reference [50] used a 2.4 GHz transmitting frequency and a 3.65 GHz wireless powering frequency. However, the antenna is designed to resonate at 2.4 GHz thus has an inferior performance at 3.65 GHz which affects the efficiency of the wireless powering. Furthermore, it requires an off-chip frequency diplexer to separate the transmitting and wireless powering link leading to an increase in the packaging cost and a large form factor. This work utilizes backscattering method to modulate radio cross section (RCS) of antenna with shunt transistors across to minimize power consumption of the rectified voltage supply necessary by low power requirement of the battery-less design implemented in this work.

The OOK downlink modulation and back-scattering uplink modulation concerns regarding to power management will be further discussed in Chapter 5.

3.2 Demodulator Design

Conventional demodulator designs for OOK modulation scheme include rectifier output and peak detector at RF input port. While using rectifier output would affect the efficiency of the rectifier circuit, the power consumed by the peak detector connected to the RF input port can be minimized and does not affect the rectifier output efficiency. This approach seems to be a better design option than implementing the peak detector at the RF input port. The demodulator design utilizes a low power leaky detector presented in [6] along with a dynamic comparator and an SR latch as shown in Fig. 3.1 (a). The

envelope detector generates a reference voltage through diode voltage divider. The diode size has been tuned for low current consumption but fast enough response in order to demodulate signal correctly. A dynamic comparator is utilized to lower the power consumption comparing to an operational amplifier (OPAmp) based continuous comparator. The design eliminates the need for accurate bias voltage and current for the OPAmp circuit. The entire demodulator circuit consumes only 1.72 μA from RF port and 0.9 μA from the rectified DC power supply.

Demodulator operating with OOK modulation on RF input is shown in Fig. 3.2. RF differential port in modulated with 0.15 modulation index, meaning OOK off period voltage swing is only 0.85 of OOK on period voltage peak to peak as shown in Fig. 3.2(a). In Fig. 3.2(b) signal V_{env} tracks the envelope of RF port input and demodulator circuit generated V_{ref} for comparison with V_{env}. During OOK on period, V_{env} is higher than V_{ref}, therefore the system demodulates an output high signal. During OOK off period, V_{env} is lower than V_{ref} thus it demodulates an output low signal. V_{ref} is generated from the voltage divided from the envelope of RF input. Therefore, the demodulator can work with wider input RF power range compared to a circuit designed with a fixed reference voltage.

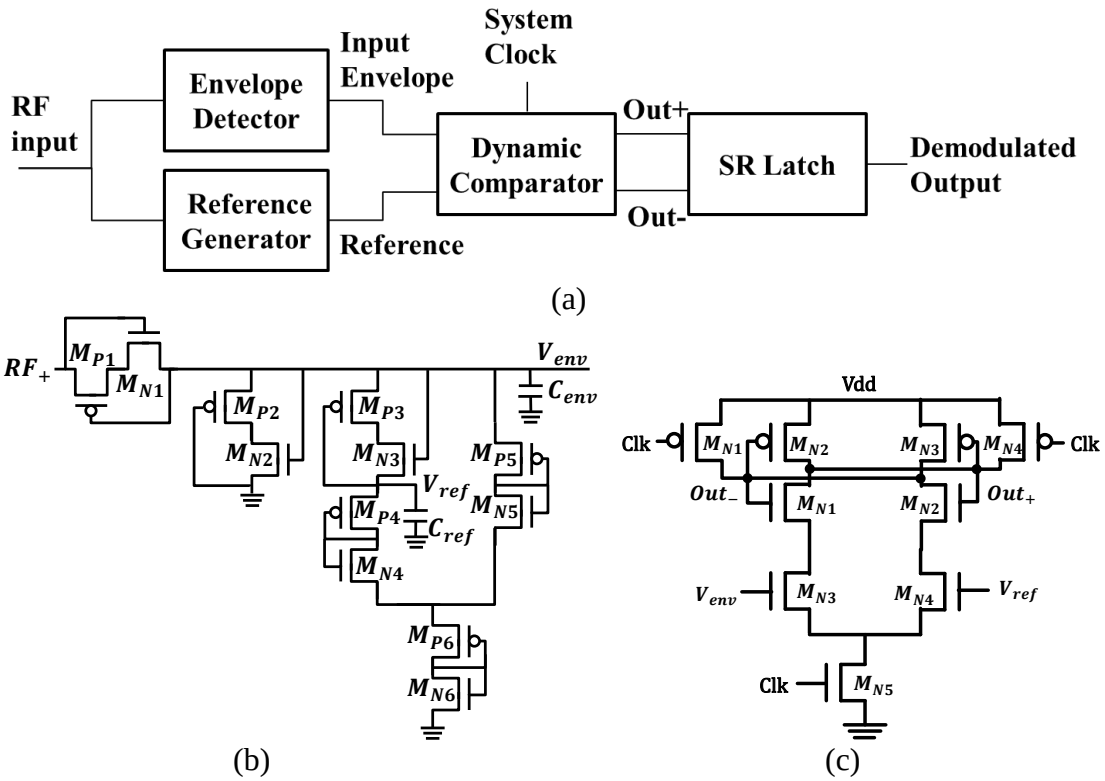


Figure 3.1 (a) Demodulator Block Diagram, (b) Envelope and Reference Generator, (c) Dynamic Comparator

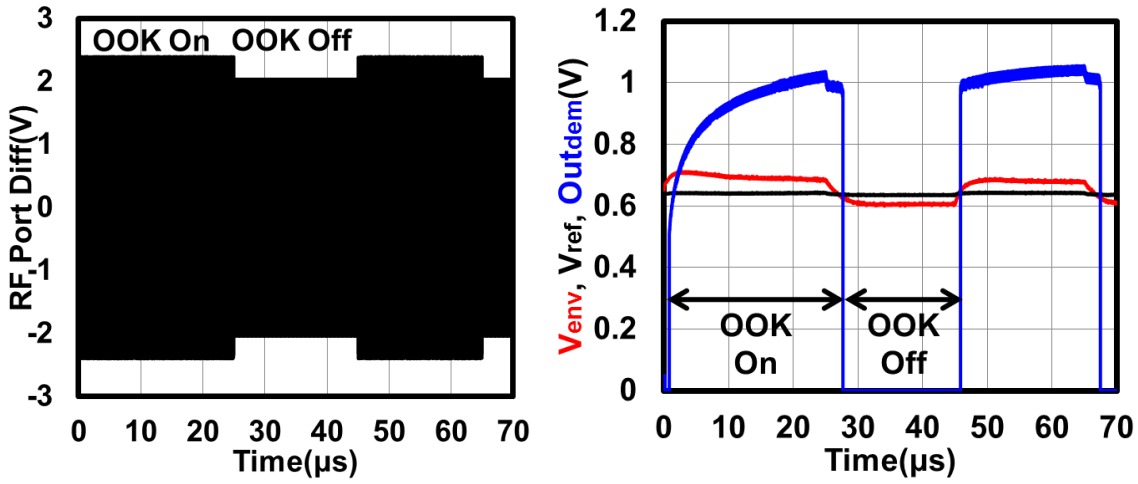


Figure 3.2 Demodulator Post-layout Simulation (a) RF Input, (b) Input Envelope (red) and Reference Voltage (black), Demodulated Output (blue).

Minimum symbol length with different modulation index is determined with simulated results shown in Fig. 3.3. The minimal symbol length is calculated as sum of delay from high to low RF voltage peak transition and low to high RF input voltage peak transition. The longest minimum symbol length is 31 μs with modulation index of 0.25 and unmodulated RF input voltage peak of 2.9 V.

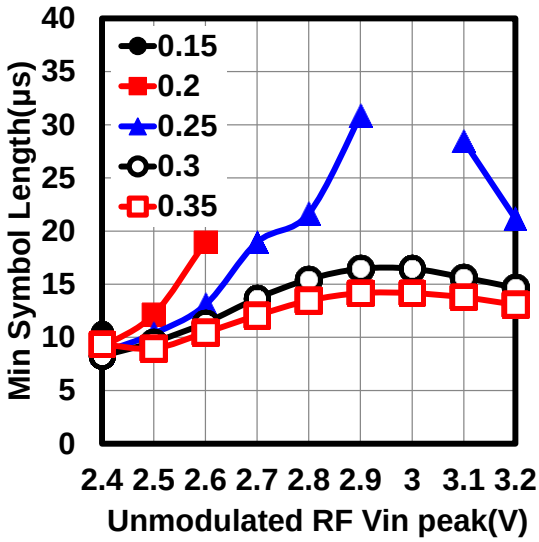


Figure 3.3 Minimal Symbol Length Determined by Sum of Demodulator High to Low Input RF Voltage Peak and Low to High Input RF Voltage Peak Transition Delay with Different Modulation Index

The demodulator along with the rectifier and low drop-out regulator (LDO) output were measured with the set up shown in Fig. 3.4. The measurement result with 8 dB power modulation index is shown in Fig. 3.5. The demodulator only works with large modulation index leading to large variation of LDO output and requires improvement of design integration.

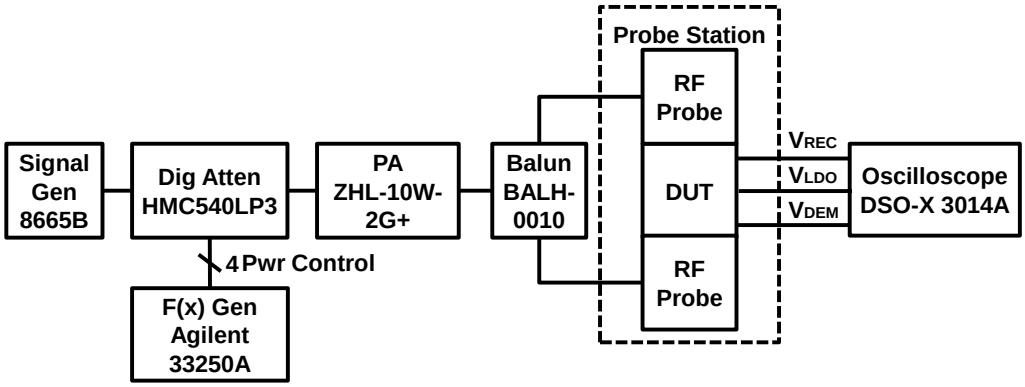


Figure 3.4 Demodulator, Rectifier, and LDO Integrated Measurement Setup

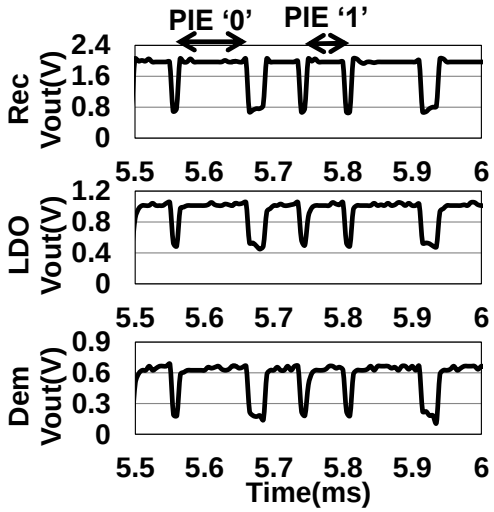


Figure 3.5 Demodulator, Rectifier, and LDO Integrated Measured Output with 8 dB Power Modulation

3.3 Modulator Design

Modulator uses shunt transistor across the differential antenna terminal in order to modify the back-scattered power at the sub-carrier frequency. The shunt transistor is controlled by a 10 MHz subcarrier for ease of back-scatter detection. As shown in Fig. 3.5, back-scatter detecting circulator only has limited isolation. As a result, much larger power comparing to back-scattered power would leak from transmitting power amplifier to the low-noise amplifier (LNA) if power leakage cancellation technique is not used.

Such design leads to a very stringent requirement on the LNA dynamic range. While enormous dynamic range LNA is very rare and expensive, using notch filtering of the RF leakage presents an easy to implement solution. To alleviate the requirement of high quality factor of the notch filter design, the back-scattered frequency is chosen to be 10 MHz with consideration along with the power consumption of the clock generation module.

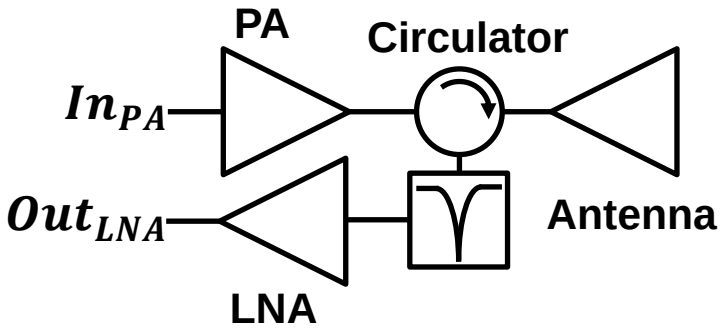


Figure 3.6 Reader Circuit Front-end

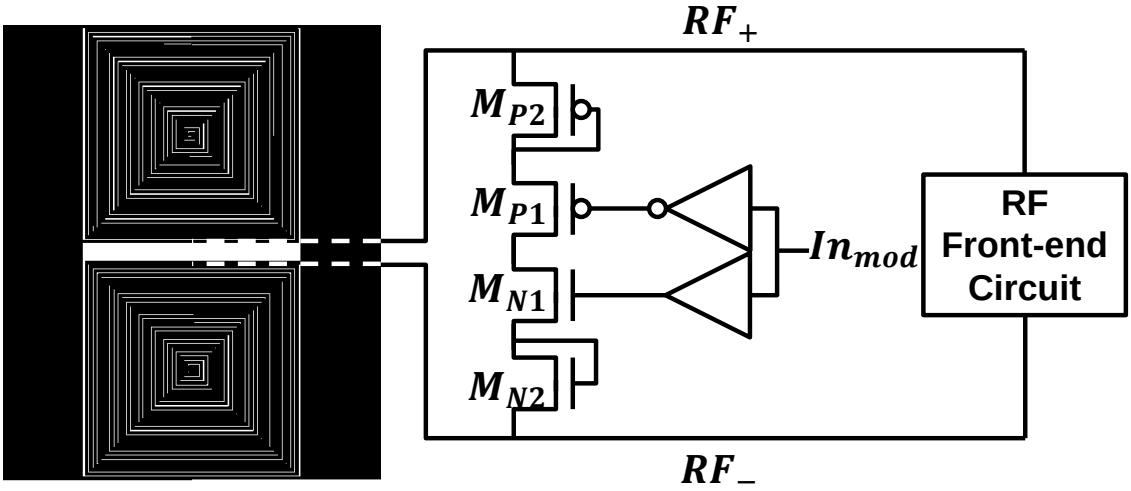


Figure 3.7 Modulator Circuit Diagram

Measurement was conducted using an external MOSFET with measurement setup shown in Fig. 3.8. The experiment is crucial in finding the transistor size for backscatter switch for detectable backscattered power received from the sensor node. Multiple shunt transistors are tested with backscattering measurement. In these experiments, the backscattered power increases as the shunt transistor conductance increases as show in Table 3.1. Therefore 2 mm width of on-chip back scattering transistors was determined to have similar conductance with the one achieved by the external MOSFET. The shunt transistor was designed with thick oxide along with diode connected transistors stacked on top and bottom of pmos-nmos shunt transistors pair for reliability concern.

Figs. 3.9(b) shows a comparison of Discrete Fourier transform (DFT) of power presented at the RF input port when modulator is either activated or not activated. The power consumed at 10 MHz away from carrier frequency has a 37.6 dB difference between the two cases when modulator is activated (-16.2 dBm) and not activated (-53.8 dBm). Therefore, the backscattered power at sub-carrier frequency differs when modulator is activated due to fact that radar cross section (RCS) changes by an addition power consumption by the modulator at that frequency. The modulator driving buffers consume 1.2 μA at 1V power supply when modulator is off and 72 μA when it is on.

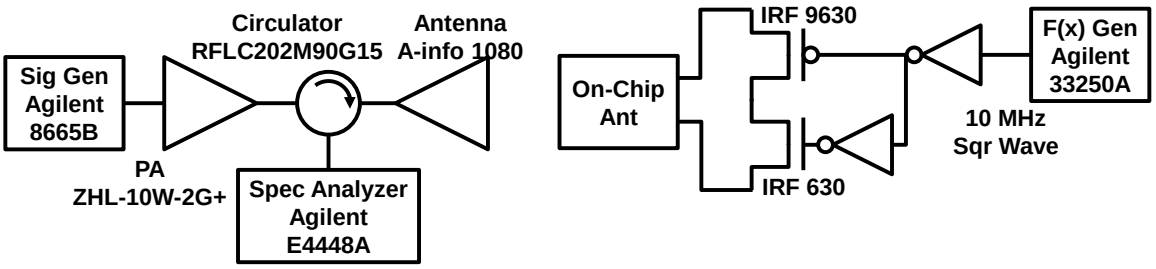
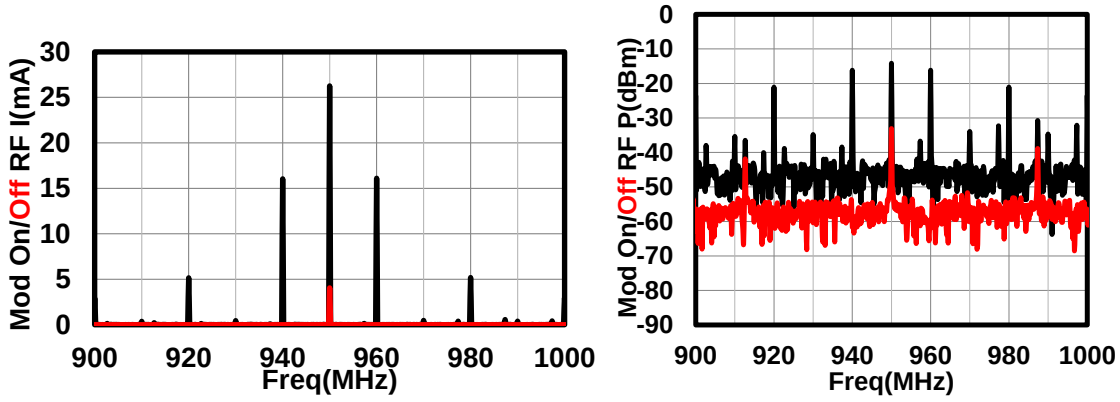


Figure 3.8 Backscattering Measurement Setup of On-chip Antenna with External Off-chip MOSFET

Table 3.1 Backscattered Power from On-chip Antenna and External Shunt Transistor with Different Control Signal Voltage Level and Conductance with 16 dBm EIRP Horn Antenna Transmitted Output Power

MOSFET Control Voltage(V)	**Backscattered Power (dBm)**	**Conducted I with 2 V/1.5 V/1 V Across Shunt Transistors(mA)**		
		2 V	**1.5 V**	**1 V**
1.5	-76.11	243	50.9	2.33
2	-73.25	250	51.35	2.36
2.5	-71.09	256.6	52	2.39
3	-68.04	267	52.4	2.43



(a) (b)

Figure 3.9 (a) Current and (b) Power Presented on RF Input across Frequency Spectrum when Modulator is inactive and Modulator is Active

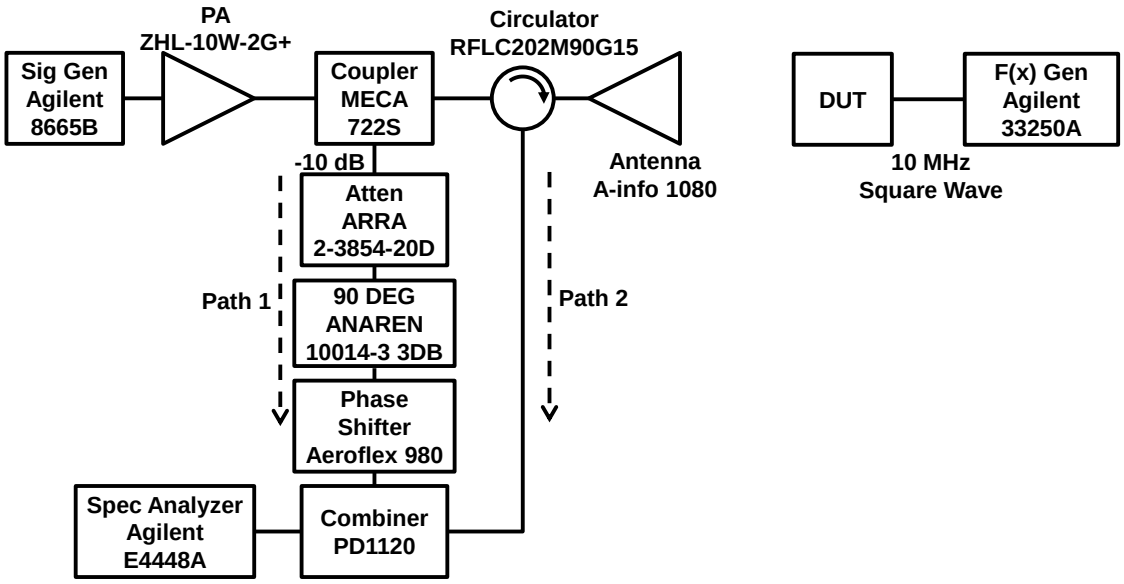


Figure 3.10 Backscattering Measurement Setup with On-chip Antenna and Shunt Transistors

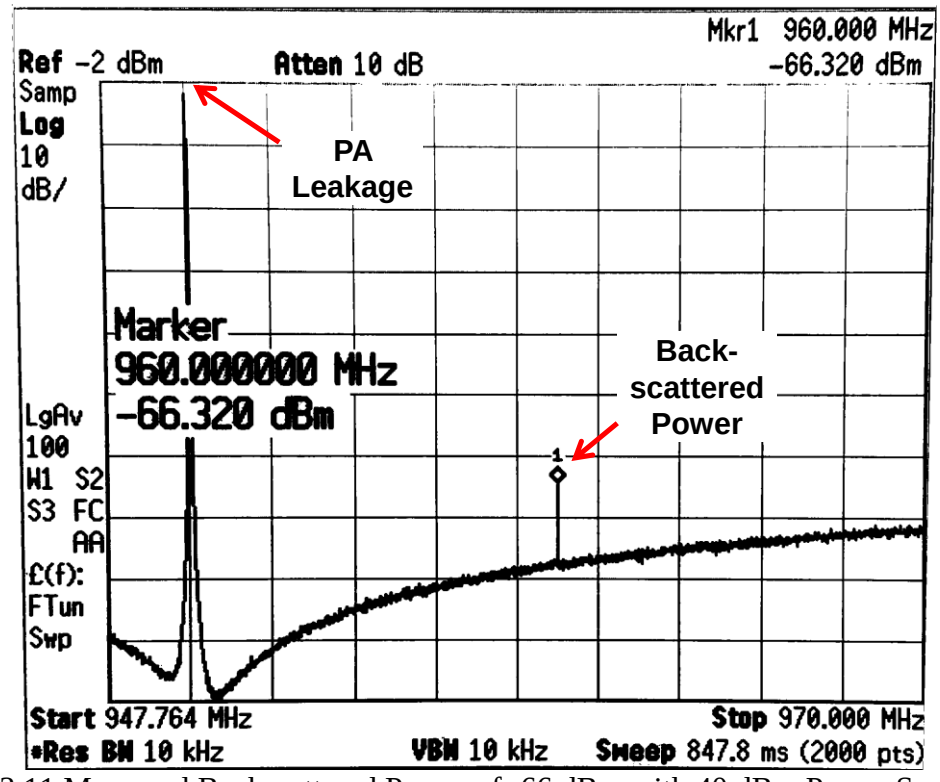


Figure 3.11 Measured Backscattered Power of -66 dBm with 40 dBm Power Source at 0 cm Away

Modulator was measured along with the sensor node on-chip antenna with the measurement setup shown in Fig. 3.10. The coupled power amplifier (PA) path 1 was tuned to the exact same amplitude but 180 degree phase shift with a circulator leakage from the PA on path 2 to cancel the PA leakage power at the power combiner. The circulator isolation rating was 17 dB. As shown in Fig. 3.11, the circulator leakage power from the power amplifier has been reduced from +13 dBm to -3.877 dBm with a power amplifier output of 40 dBm. A function generator was connected to the modulator control with 10 MHz square wave. The backscattered power from the sensor node was detected to be -66 dBm at 10 MHz away from the carrier frequency of 950 MHz coming from the horn antenna A-info 1080 at 0 cm distance between sensor node and the transmitting horn antenna.

3.4 Reader Front-end Design

A reader receiver front-end was designed as shown in Fig. 3.10, which utilizes the same topology as references [71, 72, and 74]. This topology has been demonstrated to achieve 70 dB of transmit to receive isolation [74]. Power leakage cancelation is characterized which provides an excellent cancellation of the leakage power from +13 dBm to -3.887 dBm (~ -17 dB) as shown in Fig. 3.11. The limitation on the maximum cancellation of -20 dB is the result of finite resolution of the phase shifter and the attenuator used in this experiment. Furthermore, the suppression of PA leakage decreases over time and with different measurement setup as the antenna mismatch loss changes with a time variant environment [73]. Therefore, the system also needs an automated control phase shifter and an attenuator to maintain the maximum PA leakage suppression.

According to the design shown in Fig. 3.11, the leakage power will saturate the three stage LNA (P1dB= 17.8 dBm) if the input power of the LNA is larger than its input P1dB, which would be 17.8 dBm (output P1dB) – 52 dB (Gain) = -34.2 dBm. Therefore further suppression of the PA leakage power is required to achieve design improvement.

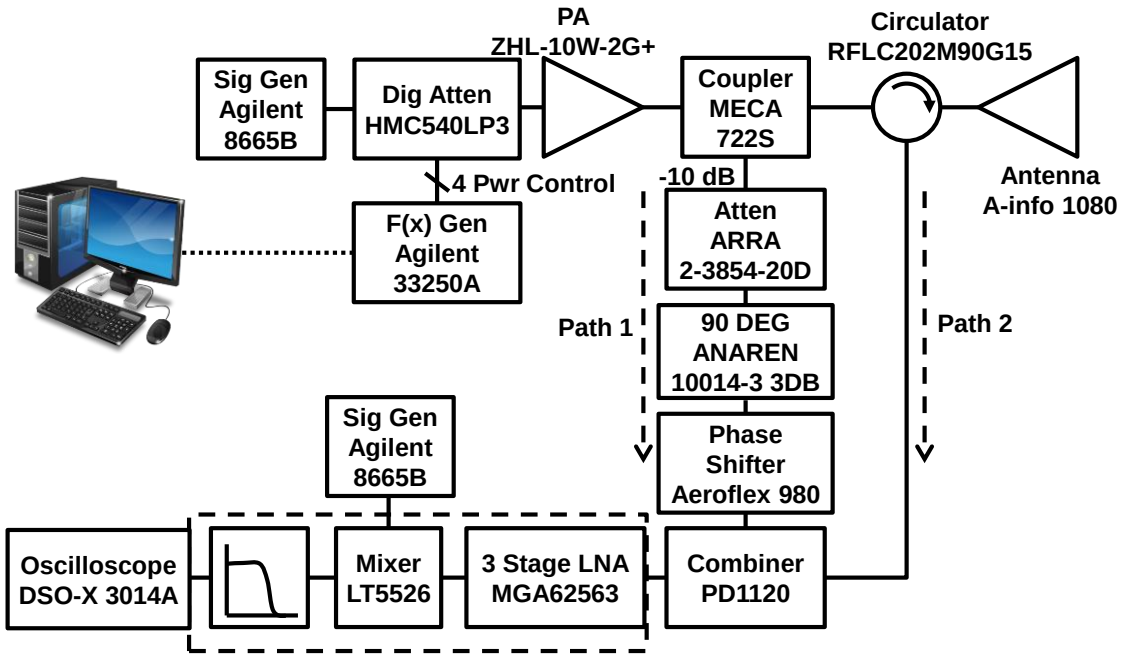
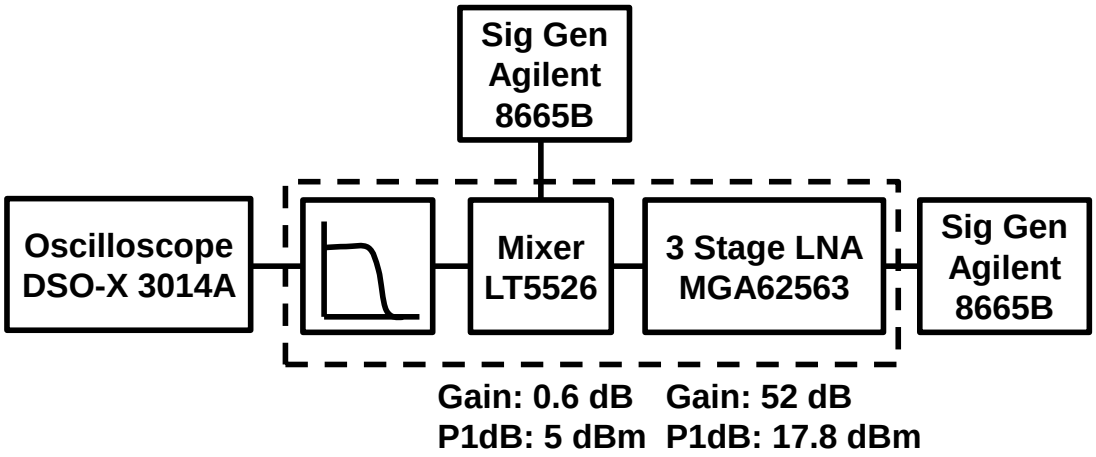
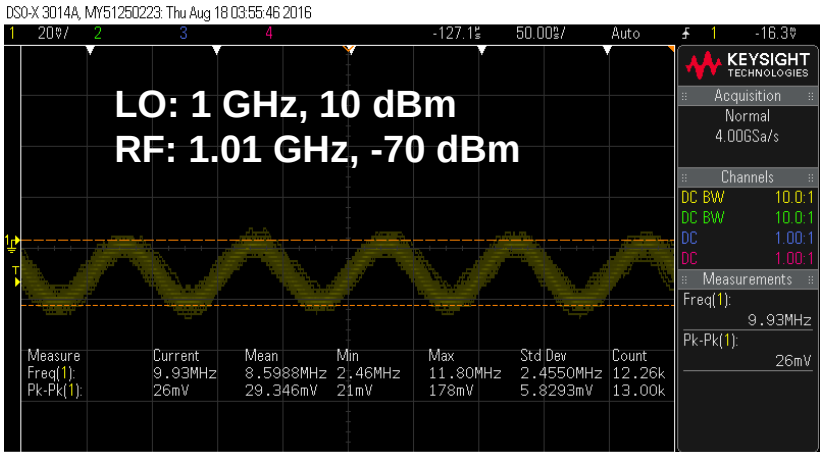


Figure 3.12 Reader Front End Design

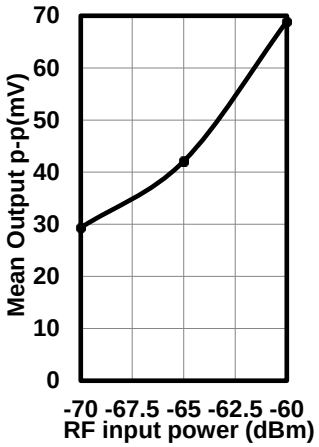
Receiving path shown in Fig. 3.12 dashed box is characterized and oscilloscope plot of the low-passed output signal with an RF input power of -70 dBm, -65 dBm and -60 dBm is shown in Fig. 3.13(b.) For this experiment the measurement setup of Fig. 3.13(a) is used.



(a)



(b)



(c)

Figure 3.13 Three Stage LNA, Mixer and Low-pass filter Path Measurement (a) Setup (b) Oscilloscope Plot with -70 dBm RF input (c) Mean Output Voltage Peak-Peak with -70, -65 and -60 dBm RF Input Power.

4. UPLINK AND DOWNLINK ENCODER SCHEME AND ENCODER DESIGN

4.1 Downlink Encoding Scheme and Command Packet Format (Reader to Sensor Node)

The main concern for the choice of downlink protocols is the discharging time duration. If the discharging activity is too long or too often, the charge stored in the storage capacitor might not be enough for tag operation. The work presented in this Thesis adopts pulse interval modulation (PIE) protocol discussed in [29]. The encoded '1' and '0' are differentiated by the length of the high voltage level duration. As shown in Fig. 4.1, a high level duration above 80 μs is recognized as symbol '0' and below it recognized as '1'. With system clock of 10 MHz, the low voltage level duration is carefully controlled within 1 μs accuracy at the output of the demodulator. Therefore, the tag can sample the low voltage level input at least twice. (Fig. 3.1) The length difference and input off timing is widely depended on demodulator design trade off with RF power consumption as discussed in Chapter 3.

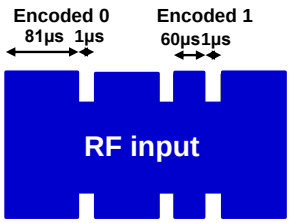
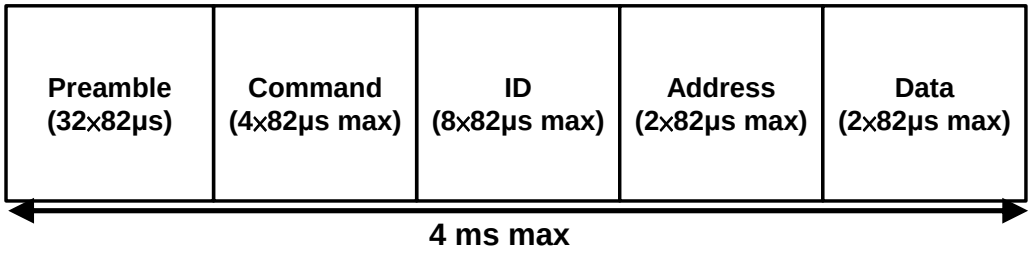


Figure 4.1 Downlink PIE Encoded symbol '0' and '1' Example

Decoder of this encoding downlink scheme counts input logic high cycle numbers with a certain threshold value and resets the counter whenever the input is logic low. In this design the system clock frequency is 10 MHz, therefore the threshold can be set as 80 μs to distinguish encoded logic 1 with 60 μs high level duration and encoded logic 0 with 81μs (or any length longer than 80 μs) high level duration for encoding timing shown in Fig. 3.1.



(a)

Figure 4.2 Downlink Command Format for Standalone Test Sensor Platform

The commands for the operation are: Write data and Read data. The write data command writes the data specified within command set into the tag specific internal register specified by an address. The read command reads the data previously stored in the tag registers. ID field are not used at this point but implemented for future work included non-volatile memory stored ID applications.

4.2 Uplink Encode Scheme and Data Packet Format (Sensor Node to Reader)

Typical uplink encoding schemes are FM0 and Miller sub-carrier encoding according to Gen 2 EPC ISO 18000-6C. The uplink data encoding scheme utilizes a sub-carrier Miller encoding scheme for its major benefits of the back-scatter frequency is

presented farther from carrier frequency for reader design. Other advantages are good symbol error rate performance in the presence of noise [64] and easy detection from a higher number of transitions between two antenna loads per bit [61]. Miller encoding has a transition in the middle of symbol for encoded bit 1 and a transition on the edge of the symbol for encoded bit 0. Miller sub-carrier encoding follows a similar idea but with phase change instead of voltage level transition as shown in Fig. 4.3 (a). For simplicity, Fig. 4.3 (a) shows a miller subcarrier encoded ‘0’ and ‘1’ with subcarrier frequency of 10 MHz and data rate of 312.5 kbps. At the reader side, due to different subcarrier frequencies, the data on each thread can be demodulated and decoded after filters separate and process each subcarrier frequency individually.

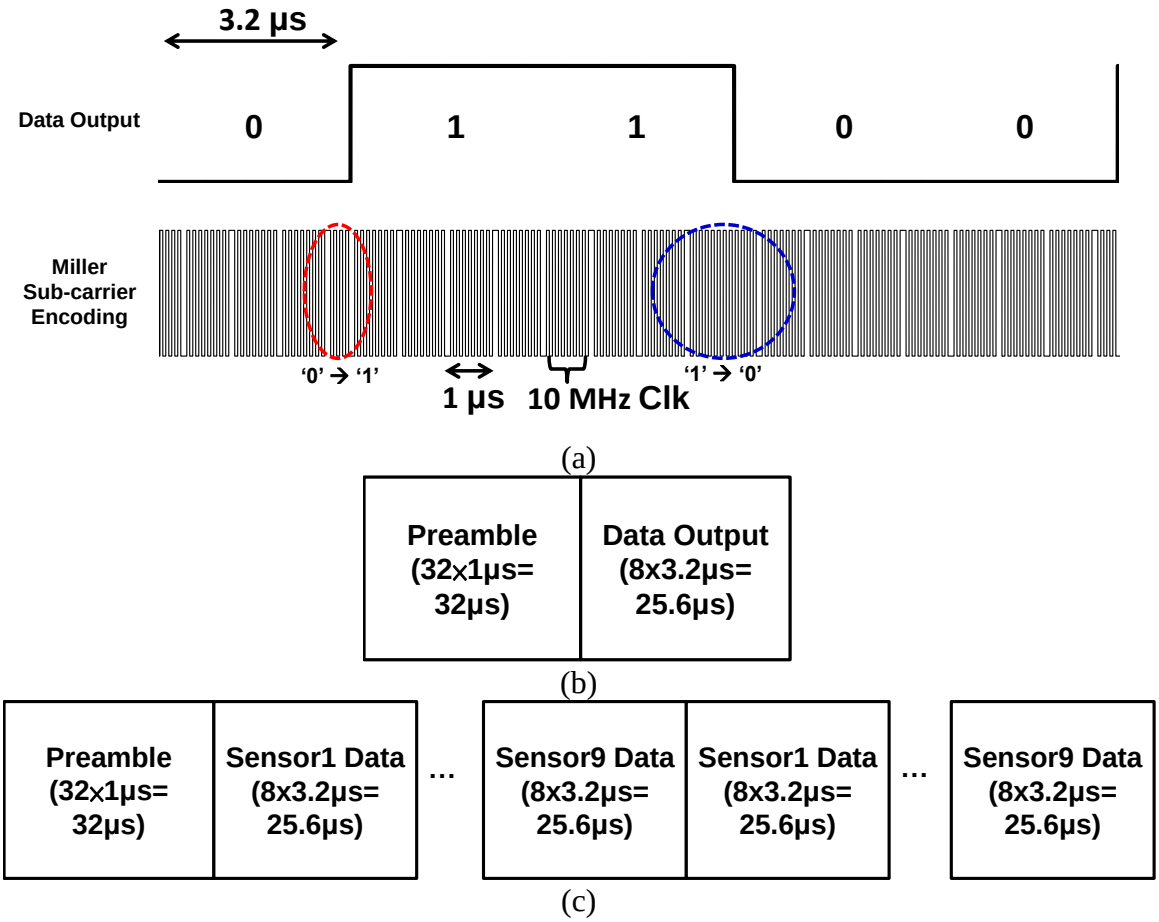


Figure 4.3 (a) Miller Sub-carrier Encoding with 3.2µs Symbol Length and 10 MHz Sub-carrier. Operation Mode Uplink Data Format for Standalone Test Sensor Platform (c) for Design Integrated with ADC and Sensors

Uplink data transmission for standalone sensor platform is composed of 32 bit preamble and 8 bit data. For a design integrated with an analog to digital converter (ADC) and sensors first send out 32 bit preamble bit, than send 9 channels of different sensor data twice and repeat the cycle starting from 32 bit preamble bit.

The Miller sub-carrier encoder is designed with transmission gates multiplexer and CMOS logic gates for low power consumption. The design is shown in Fig. 4.3 (a) and post-layout simulation plot is shown in Fig. 3.4.The miller sub-carrier uses 10 MHz

signal in this simulation plot and the uplink data rate is 312.5 kbps. Transition of ‘0’ to ‘1’ and ‘1’ to 0 can be identified in red and blue dashed circles in the plot. The encoder post-layout simulation shows a dc current dissipation of 36.95 µA.

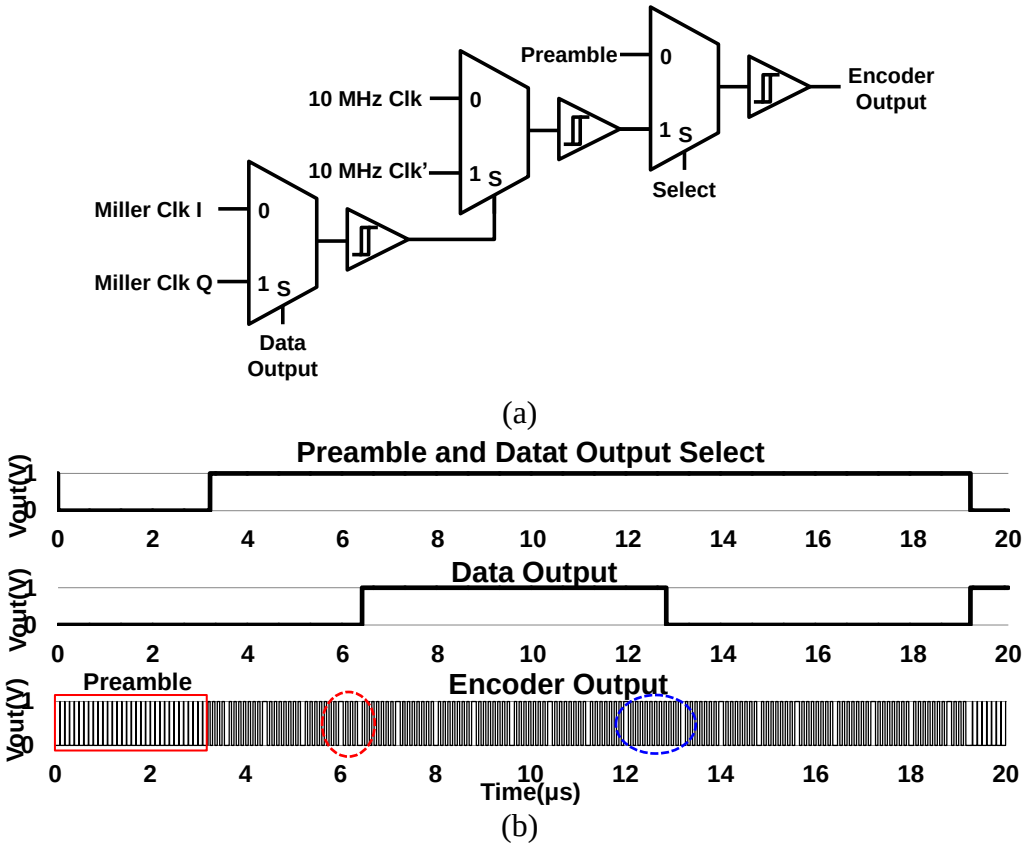


Figure 4.4 (a) Miller Sub-carrier Encoder Schematic and (b) Post-Layout Encoder Simulation Plot Showing Miller Sub-carrier Encoding Symbol ‘0’ to ‘1’ Transition (Red Dashed Circle) and ‘1’ to ‘0’ Transition (Blue Dashed Circle.)

5. POWER MANAGEMENT UNITS: POR AND LDO

Power management circuit includes low drop-out regulator (LDO) and power on reset (POR) units. LDO maintains the voltage stability against changes of RF input power. Especially when RF input power is modulated externally or by on-chip backscattering modulator, the function of LDO in establishing a constant voltage supply become critical. POR resets the digital process unit when output voltage of the LDO reaches to certain level, signaling the availability of the EM signal for communication.

Measurement of integration between LDO, POR, on-chip clock generation and digital process unit will be demonstrated and discussed in Chapter 6.

5.1 Power on Reset

Power on reset uses a traditional structure using the idea implemented in [5] as shown in Fig. 5.1.

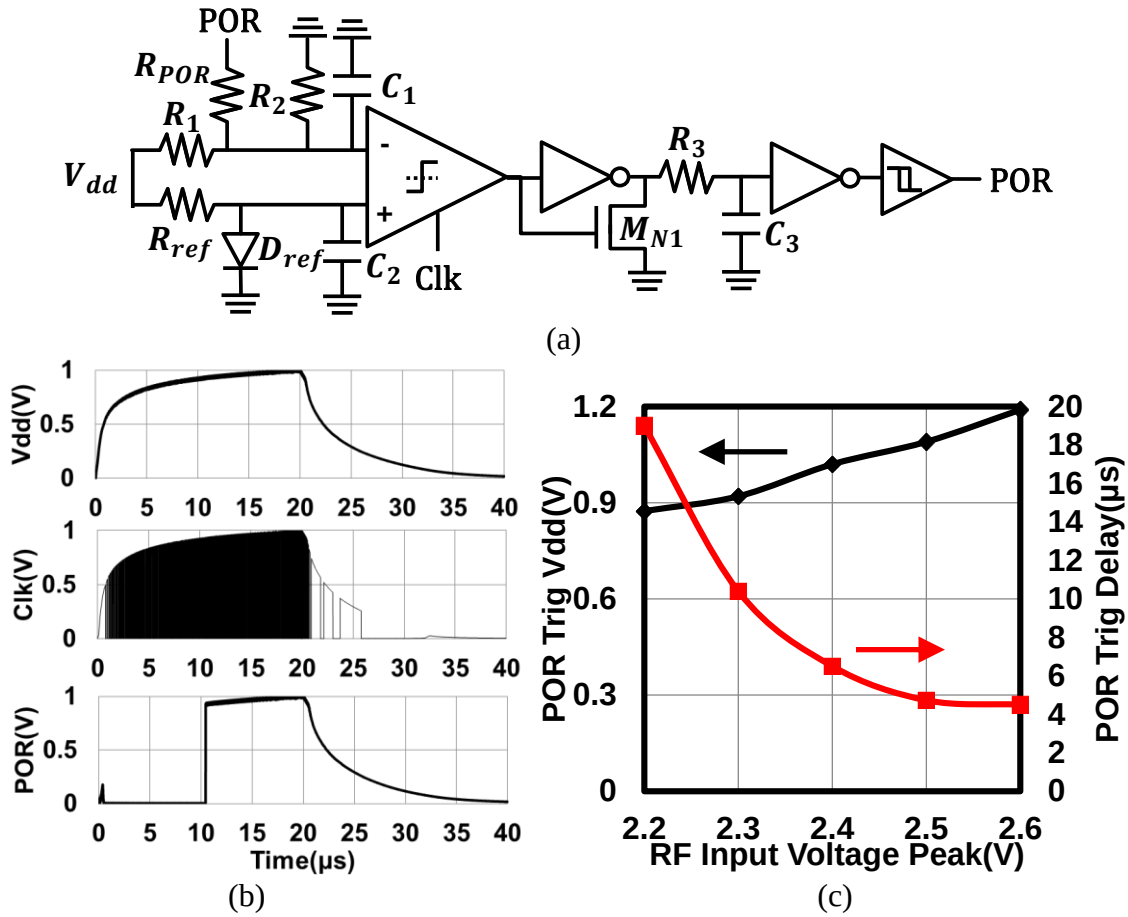


Figure 5.1 (a) POR Circuit, (b) System Simulation with LDO, Clk Gen and POR Output (c) POR Trigger Voltage and Delay with Different RF Input Peak Voltage.

In this design, power on reset (POR) is triggered when low drop-out regulator (LDO) output reaches 0.88 V. The divided supply voltage at the node connecting R_1, R_2 and R_{POR} reaches the threshold voltage of the diode available in this technology for reference voltage generation. Transistor M_{N1} is for minimizing the time latency of POR triggering on. R_3 and C_3 generate a time constant delay to avoid POR triggering off when a short falling pulse appears across Vdd. R_{POR} is utilized for hysteresis function where it requires higher Vdd for POR to trigger high and lower Vdd to trigger low. The operation of POR with the whole system is shown in Fig. 5.1 (b). Fig. 5.1(c) shows the trigger

voltage and delay condition for different RF input peak voltage. The POR is triggered only when supply voltage reaches 0.88V to ensure that regulated voltage supply of 1V is stable. The POR circuitry consumes 8.6 μA in steady state.

5.2 Low Drop-out Regulator

The low drop-out regulator (LDO) uses a digital control signal to achieve low power consumption and more less sensitivity to process variations. Following the generic idea presented in reference [62], the low drop-out regulator topology adopted here is shown in Fig. 5.2. The comparators compares voltage divided power supply with threshold voltage generated by a reference diode. The back to back nmos-pmos diode pair is introduced to this topology to achieve long RC time constants in order to reduce the regulator output voltage ripple. Fig. 5.3(a) shows LDO output voltage variation due to input OOK modulation with RF input voltage peak of 2.4 V and voltage modulation index of 0.15. Figs. 5.3(b, c) show the simulation results of the voltage across LDO and rectifier during input modulation for different RF voltage peaks and modulation indexes. Rectifier output voltage is affected much more than LDO output with input modulation. Fig 5.4(a) shows how LDO output is affected when output shun transistors modulator turned on and Fig. 5.4(b) shows the simulation of voltage regulator during output modulation with different RF input voltage peak values. For both input and output RF port modulation, LDO output has less average voltage drop comparing to rectifier output. Fig. 5.5(a) demonstrates measurement results of the LDO with different input voltages when it is supplying the power of the whole sensor node chip. When LDO input is less than 1.5 V, V_{div} is constantly lower than voltage across reference diode when transistor M_{N2} is on and the

LDO output is 0.2 V lower than the input. When LDO input is greater than 1.5 V, V_{div} can reach higher than voltage across the reference diode and the LDO starts the operation. The LDO has a voltage ripple of about 0.15 V with a 10 MHz frequency component. This output ripple is too large for the integrated ADC and sensor output amplifier and requires further improvement. Furthermore, the measurement result shows that this design consumes 113 μA with an LDO output of 1.01 V and 75.2 μA with an LDO output of 0.9V. Fig. 5.5(b) shows the performance of the Rectenna with the LDO when transmitting antenna is 0 cm away from the sensor node circuit and transmitting 40 dBm of output power. The rectifier output reaches 1.12 V and the LDO output reaches 0.6 V. Both rectifier and LDO voltages stabilized 2 ms after the RF source is switched on, while simulation shows a stabilizing time of 0.1 ms. The stabilizing time of the measurement shown in Fig. 5.5(b) also included the RF power switch on time.

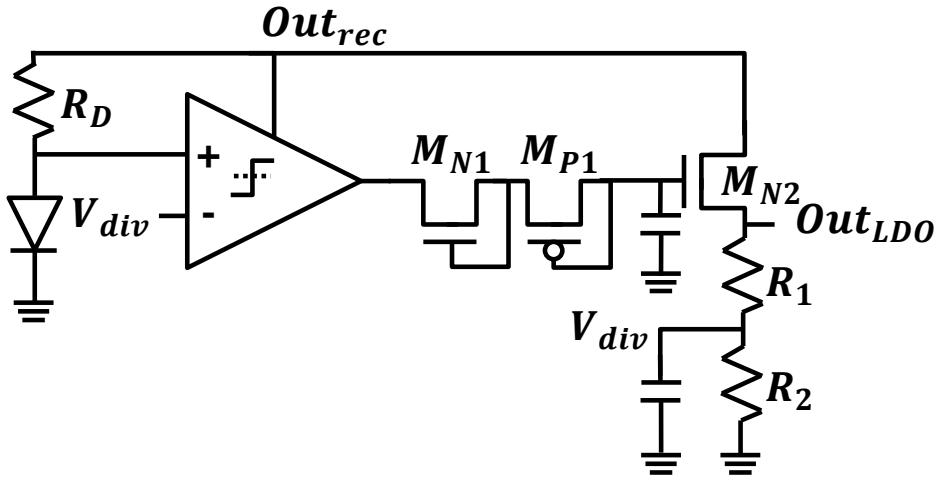
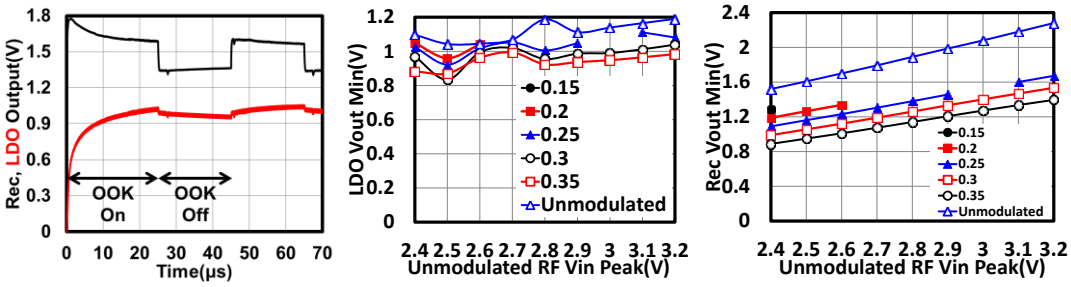
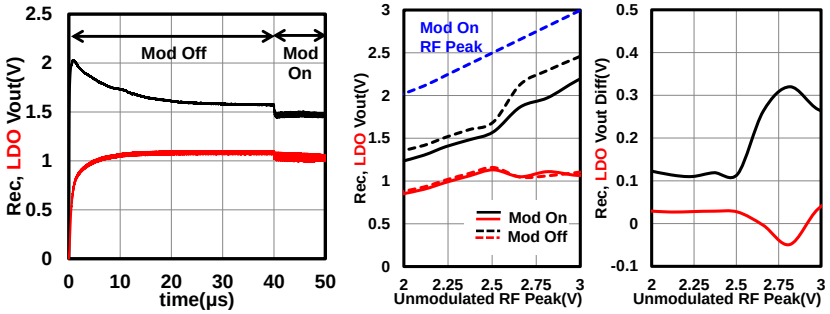


Figure 5.2 LDO Schematic



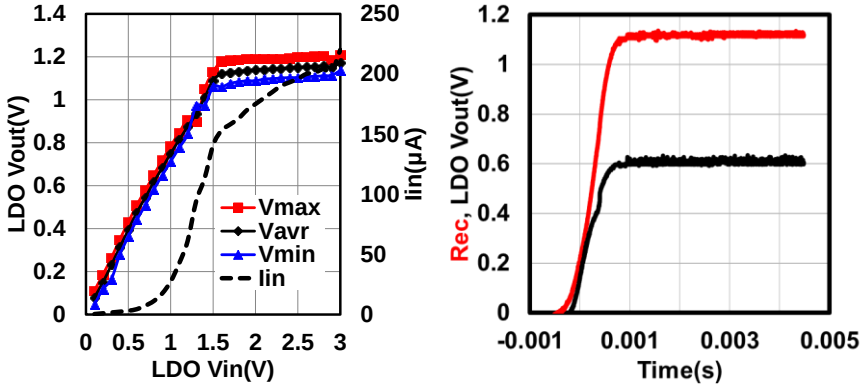
(a) (b) (c)

Figure 5.3 Simulation of LDO Output Voltage when RF Input is Modulated (a) Transient with RF Vin Peak of 2.4 V and Modulation Index of 0.15. (b) LDO Output Voltage with Different RF Vin Peak and Modulation Index. (c) Rectifier Output Voltage with Different RF Vin Peak and Modulation Index.



(a) (b) (c)

Figure 5.4 Simulation of LDO Output Voltage when Output Modulator is On (a) Transient with RF Vin Peak of 2.3 V. (b) Rectifier and LDO Output Voltage with Different RF Vin Peak. (c) Rectifier and LDO Output Voltage Difference with Modulator turned On and Off



(a) (b)

Figure 5.5 (a) LDO Measurement and Input Current Consumption with the Load of Sensor Node Circuit. (b) Rectenna and LDO Measured Voltage Output with 40 dBm Transmitting Source and 0 cm between Source Antenna and Sensor Node.

6. DIGITAL BASBAND OPERATION AND CLOCK GENERATION

Digital baseband operation includes synchronization of clock frequency for proper decoding of input commands, decoding of the command and other input signals such as POR in order to generate control signals to various part of the system, writing data specified from a command into a particular register and transmitting out previously stored data in a register memory or a stream of data generated on spot from on-board sensors. This Chapter starts with clock generation and frequency locking circuits and continues with description on the state machine used for digital operation, and is followed by the state machine design and operation measurements.

6.1 Digital Controlled Relaxation Oscillator

The main two considerations during the design of on-chip clock generation for the sensor node system are: 1) power consumption, as the whole circuitry needs to operate within limited rectified power and 2) clock frequency accuracy. For protocols that have more stringent clock frequency accuracy such as EPC Gen-2 (with clock jitter tolerance smaller than ±4% for link frequency from 40 kHz to 107 kHz), designs usually adopt frequency divider from the input RF frequency [4]. Frequency division from high frequency in GHz frequency range down to baseband clock frequency such as 10 MHz, however, consumes tremendous amount of power given the available rectified DC power

may be only a few hundred microwatts. On the other hand, with less stringent protocols, designers tend to use free running oscillator [2, 4, and 6]. Nevertheless, free running oscillators are susceptible to process variations and temperature change. For the proposed system application that encompasses an integrated ADC, the clock needs to be as close to 10 MHz as possible to achieve good ADC accuracy and resolution (effective number of bits). The proposed design utilize an oscillator with a frequency lock loop similar to what has been presented in [2] to maintain a nearly fixed clock frequency upon powering up the sensor node. The design in [2] uses a digital controlled oscillator with digital integrator for lower power design and the structure is presented in Fig. 6.1 (a). The first stage counter counts the number of clock pulses and resets with input beacon from the reader during clock frequency locking state. The beacon also activates the evaluate function to compare the clock cycles within certain time duration with a fixed number. This work uses a beacon every 20 μs to reset the clock. By comparing 500 cycles in order of the clock with the 20μs beacon the frequency of the oscillator (clock) is adjusted to 10 MHz. A second stage accumulator further increments or decrements the binary control output based on the comparator results. The system utilizes 20 beacons for frequency lock loop. Therefore a total of 16 control bits is able to adjust to any frequency range in the full scale frequency range of the DCO circuit if necessary.

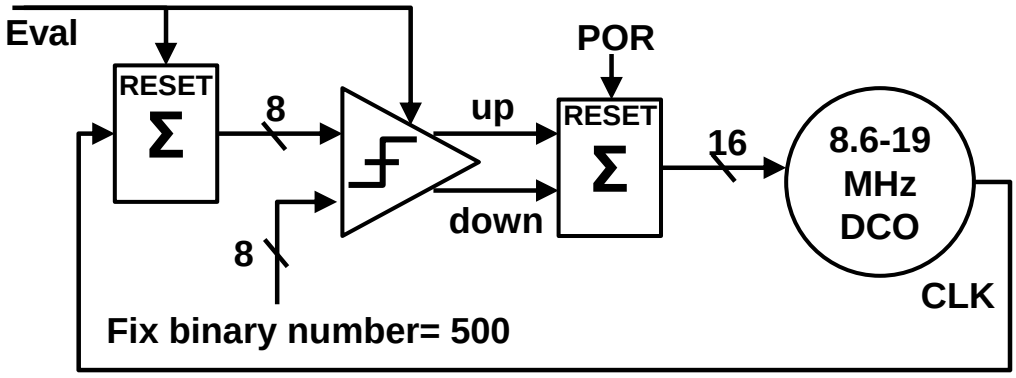
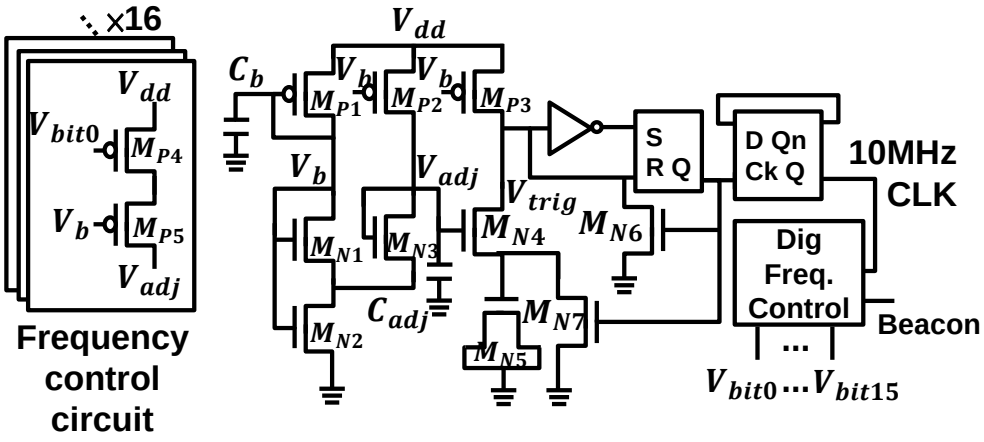


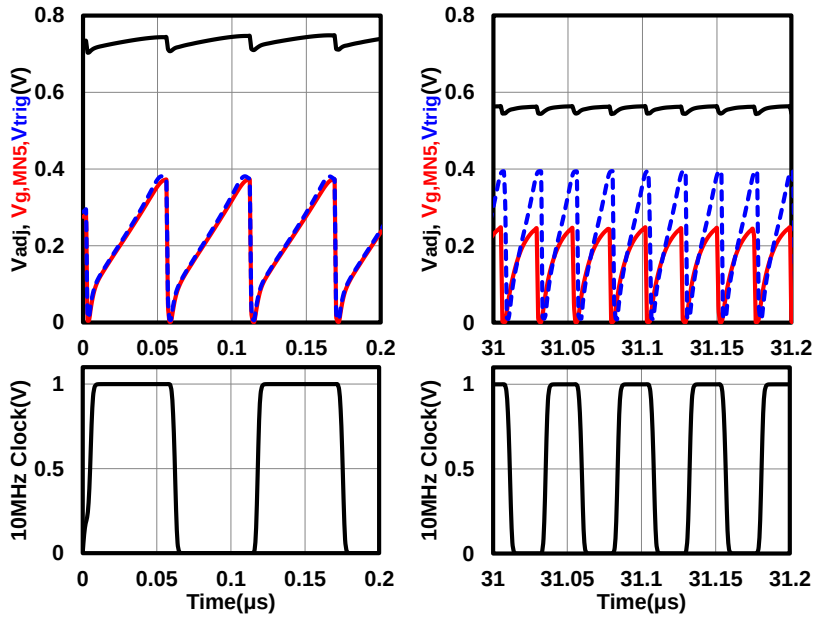
Figure 6.1 Digital Controlled Oscillator Design with Frequency Control Unit System

The free running oscillator utilizes a relaxation oscillator rather than LC or chain invertor oscillators as it consumes less power. The relaxation oscillator designed in this work is comparator-based as shown in Fig. 6.2(a) [30]. The operation of the circuit is described in the following. The comparator is constructed with transistor M_{N4}. The current I_{MN4} through transistor M_{N4} charges the gate voltage of transistor M_{N5}. The voltage is built up across a capacitance formed by M_{N5} when the SR latch following transistor M_{N4} has an output low. When the gate voltage of transistor M_{N5} is charged up to higher values, the drain voltage of M_{N4}, marked as V_{trig} also increases. When V_{trig} reaches above the threshold voltage of the invertor, it will invert the set control on SR latch and triggers reset action through a buffer and turns on the shunt transistor M_{N7} to short the gate voltage of transistor M_{N5} to ground and repeat the charging cycle. The post-layout simulated voltage of V_{adj}, $V_{g,MN5}$, V_{trig}, and reset control of SR latch and CLK output are shown in Fig. 6.2(b, c). Each clock period is determined by the time it takes for the current I_{MN4} to charge the capacitor formed by transistor M_{N5} until $V_{trig} > V_{th,INV}$. Incrementing the voltage V_{adj} lowers the resistance of the transistor M_{N4}, which leads to V_{trig} to become closer to $V_{g,MN5}$. Thus the capacitor formed by M_{N5} has to be charged for

a longer period in order to trigger the SR latch, leading to a slower frequency as shown in Fig. 6.2(b.) The relaxation oscillator post layout simulation shows that it consumes 27.2 μA with a digital frequency control unit that consumes only 4.3 μA when switching at 10 MHz. The 10 MHz clock generated by DCO is further sent to frequency dividers, which generate 2 MHz and 125 kHz clocks for digital baseband and data output applications. The frequency divider designed using the standard ARM cell consumes a simulated dc power of 2.8 μW at 10 MHz switching frequency.



(a)



(b) (c)

Figure 6.2 (a) Comparator Based Relaxation Oscillator and Frequency Control Unit and (b) Simulation of Relaxation Oscillator with High V_{adj} and Low Frequency (c) Simulation of Relaxation Oscillator with Low V_{adj} and High Frequency.

In order to simulate the full scale tunable frequency range of the DCO, the control signal is started as all low and a short 2 µs beacons was sent to DCO to purposely increase the frequency with each beacon as the clock count within 2µs is much smaller than 500. Each control bit turned from low to high when the clock count during each beacon high period is less than 500 as shown in Fig. 6.3(b.) The DCO is designed with 16 different frequency range from 8.6 MHz to 18.9 MHz with 250 kHz to 2 MHz resolution depending on control bits in typical-typical (TT) simulation environment at 27 degree Celsius in the post-layout simulation as shown in Fig. 6.3(a).

The DCO was optimized to operate with most of the process corners including typical-typical (TT), slow-slow (SS), fast-slow (FS) and slow-fast (SF) corner with

tunable frequency ranges that covers the 10 MHz operating frequency as shown in Table 6.1. Only fast-fast (FF) corner does not cover the 10 MHz oscillation. Further optimization to lower frequency tunability range of FF corner is required, while other process corners still maintain their 10 MHz operations.

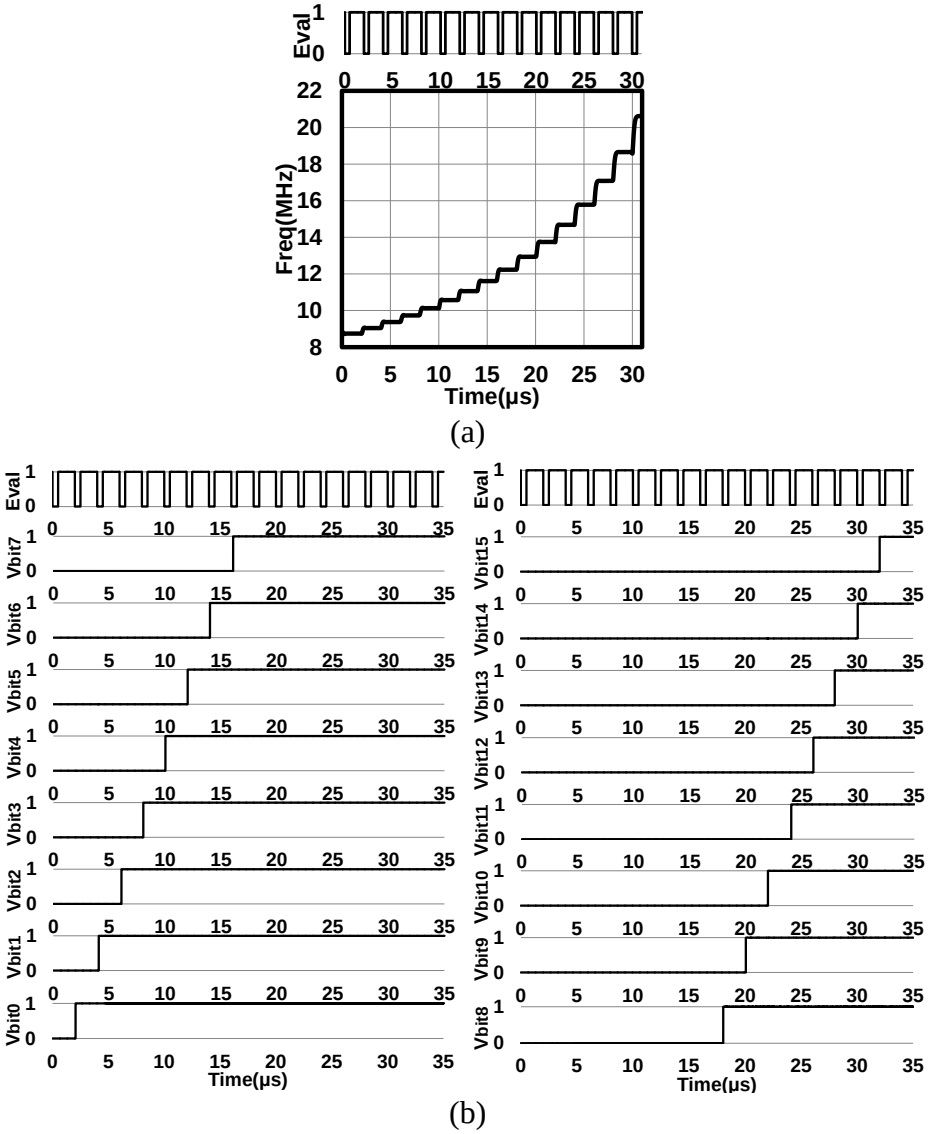


Figure 6.3 Relaxation Oscillator Frequency Locking Operation Full Scale Simulation with (a) Short 2 µs Beacon and Clock Frequency (b) 2 µs Beacon Digital Control Signal.

Table 6.1 Frequency with All Process Corners (MHz)

Control	TT	FF	SS	FS	SF
All LOW	8.66	12.72	5.81	7.93	7.95
All HIGH	18.9	16.12	15.83	15.83	21.24

The free running oscillator is measured with Vdd from 0.78 V to 1.01 V and the average frequency varies from 5.67 MHz to 19.34 MHz as shown in Fig. 6.4(a). The simulated free running clock frequency appears to be higher than the measured value and is possibly due to a possible difference in loading and parasitic capacitances. Also shown in the figure is the simulated frequency in typical-typical (TT) process corner. Clock frequencies during frequency locking operation with Vdd of 0.9 V and 1 V are shown in Fig. 6.4(b.) As shown the measured frequency is very close to the ideal frequency calculated from the beacon length of 500 clock cycles. The maximum frequency can be achieved with a Vdd of 1 V is higher than when that with Vdd of 0.9 V.

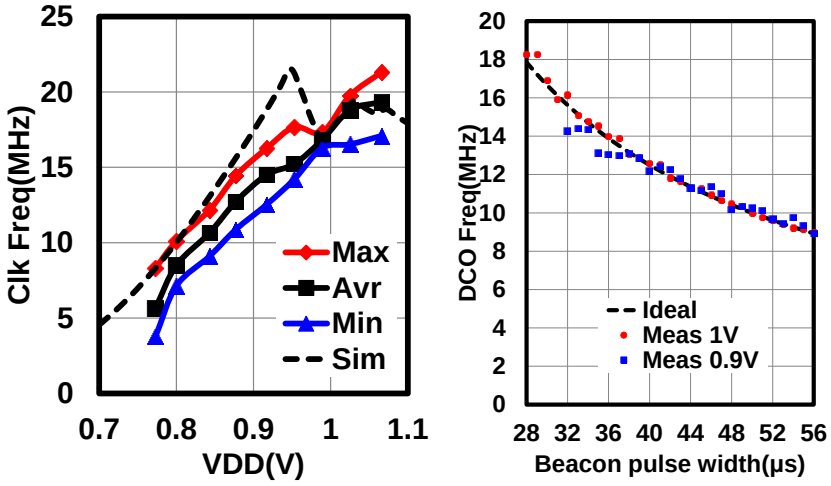


Figure 6.4 Relaxation Oscillator Frequency Measured (a) Free Running Frequency with Different Vdd (b) Locking Operation Frequency Comparing to Ideal Frequency with Vdd 1V and 0.9V.

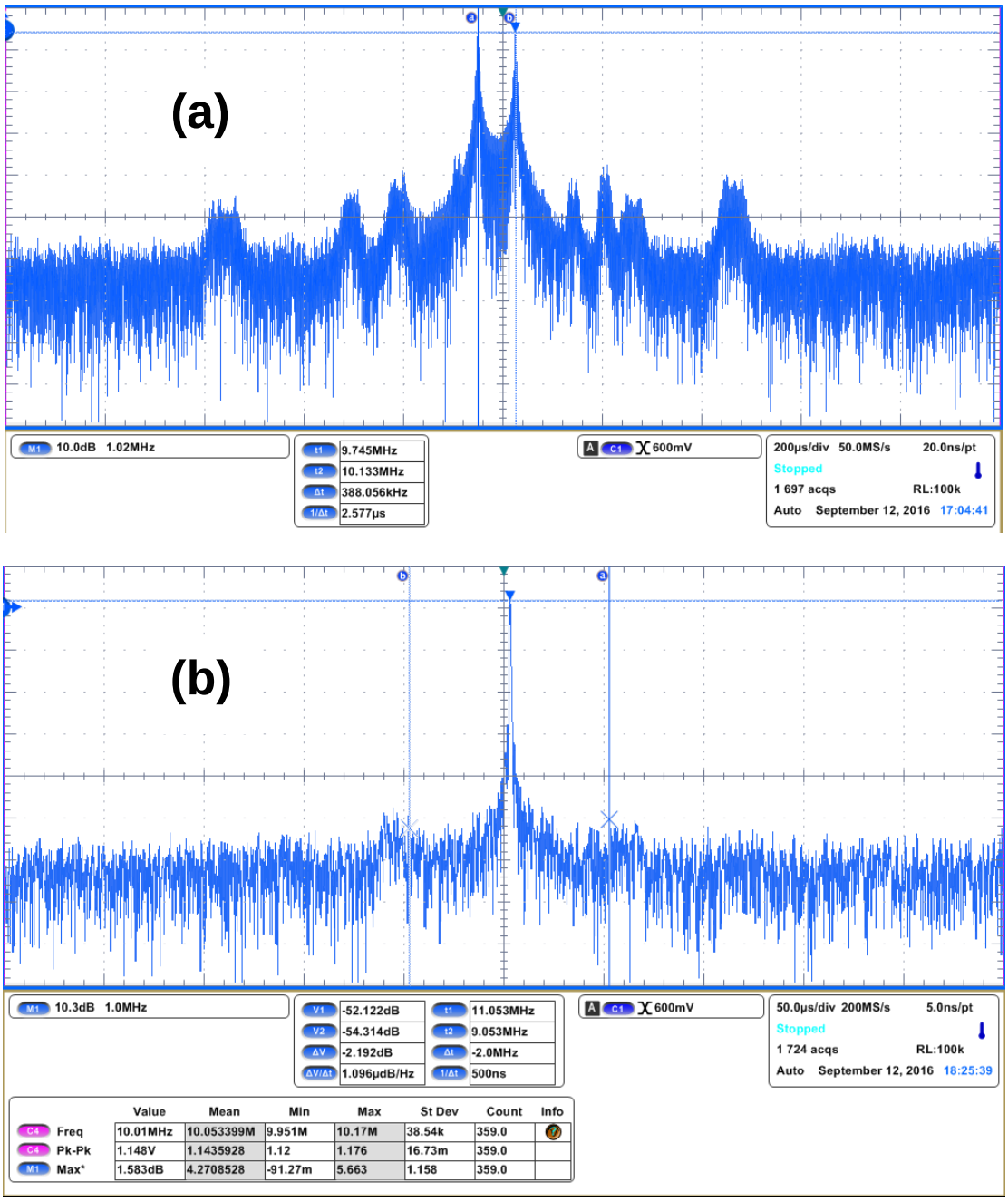


Figure 6.5 (a) Fourier Transform of Clock Frequency during Locking State (b) Fourier Transform of Clock Frequency after Locking State.

Locking operation was also measured and Fourier Transform of clock signals during locking operation and after locking operation are shown in Figs. 6.5(a) and (b),

respectively. For these measurements, a 50 μs beacon length was used. During the locking operation, two distinctive frequencies with larger power are observed due to control bit constantly switching when the clock count during beacon length is higher or lower than the fixed number of 500. After the locking operation, only one frequency with higher power is remained. The results are obtained after frequency lock loop operation with 20 beacons each with a length of 50 μs.

6.2 Digital Baseband State Machine

The state machine for the digital baseband operation of a stand-alone wireless transceiver that can be tested on its own is shown in Fig. 6.6(a). The initial start state is at Power Off state. The power on reset (POR) changes it into the Delay state when it turns into logic high. The Delay state pauses for a certain time delay in order for clock generation signal to become stable and LDO to start the operation. After the Delay state, state machine enters the Read state. In order to respond to the interrogator with a confirmation of being powered on properly, the sensor node circuit sends a fixed output in this read state. After sending the data is completed, state machine enters the Standby state and waits upon input commands. If input commands are a write command, it writes data specified by the command into a certain register assigned by the address in the command during the Write state. After write operation is done, the state machine goes back the to Read state and sends the registered data from the previous write command back to the reader unit to ensure that the write command was successful. After sending the data is complete, the state machine returns to the Standby state and waits upon the

next command. The system is designed to have the capability to be tested standalone without the presence of sensors, interface circuits and the analog to digital converter.

Fig. 6.6(b) shows the state machine designed for a wireless transceiver, integrated with ADC, interface circuits including sensor multiplexers and sensors. The sensors in this implementation are an array of microelectrodes that will be recording and stimulating neural signals. Similar to the machine of Fig. 6.6(a), the operation starts of from Power Off state until POR signal triggers high when Vdd reaches a certain value. The operation is followed by the Delay state. During the Delay state, a neuron stimulation control signal is triggered for 1 ms. Next the state machine enters the Send Sensor state to respond to reader indicating a successful wireless power condition has been reached. After transmitting a cycle of all sensors data one by one, the system enters the Clk Synch state. In this state, the system waits for clock beacon of 20 μs to achieve a fixed 10 MHz clock signal. After 20 beacons have been detected, state machine enters sending sensors data sequence again. Before sending out the first sensor data, the sensor node sends 32 bits of preamble indicating starting of the sensor sending sequence. After sending all the sensors data, the state machine returns back to the Send Preamble state and repeating sending each sensor data until the power of the system is turned off.

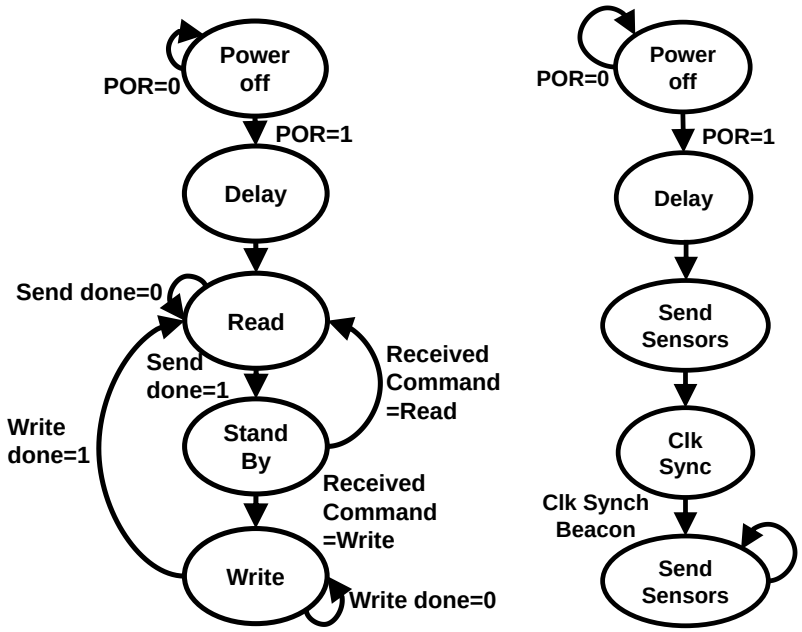
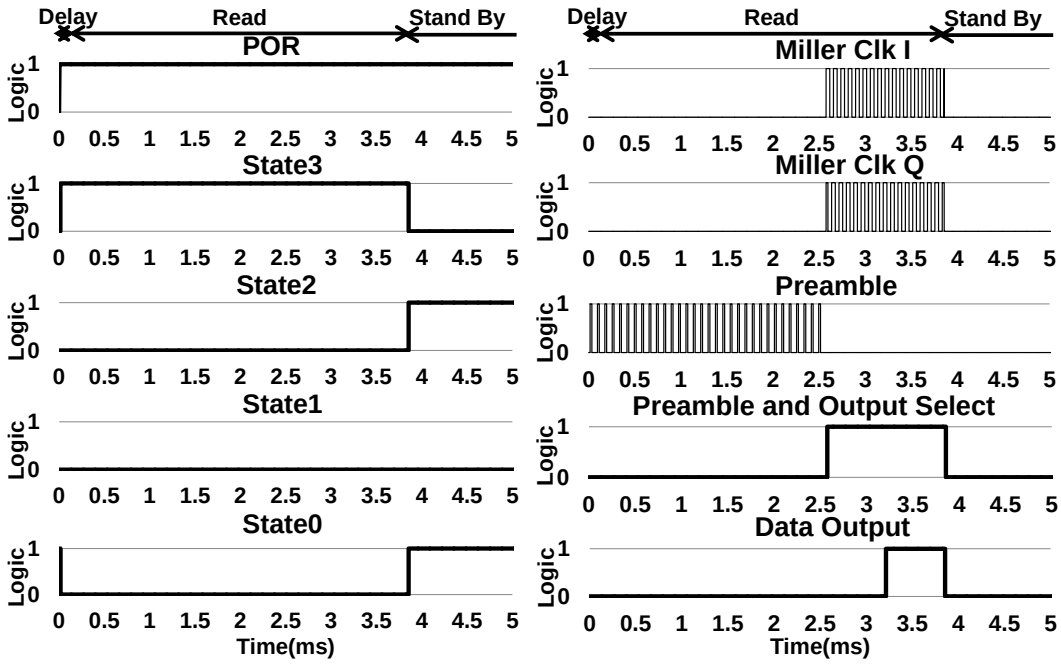
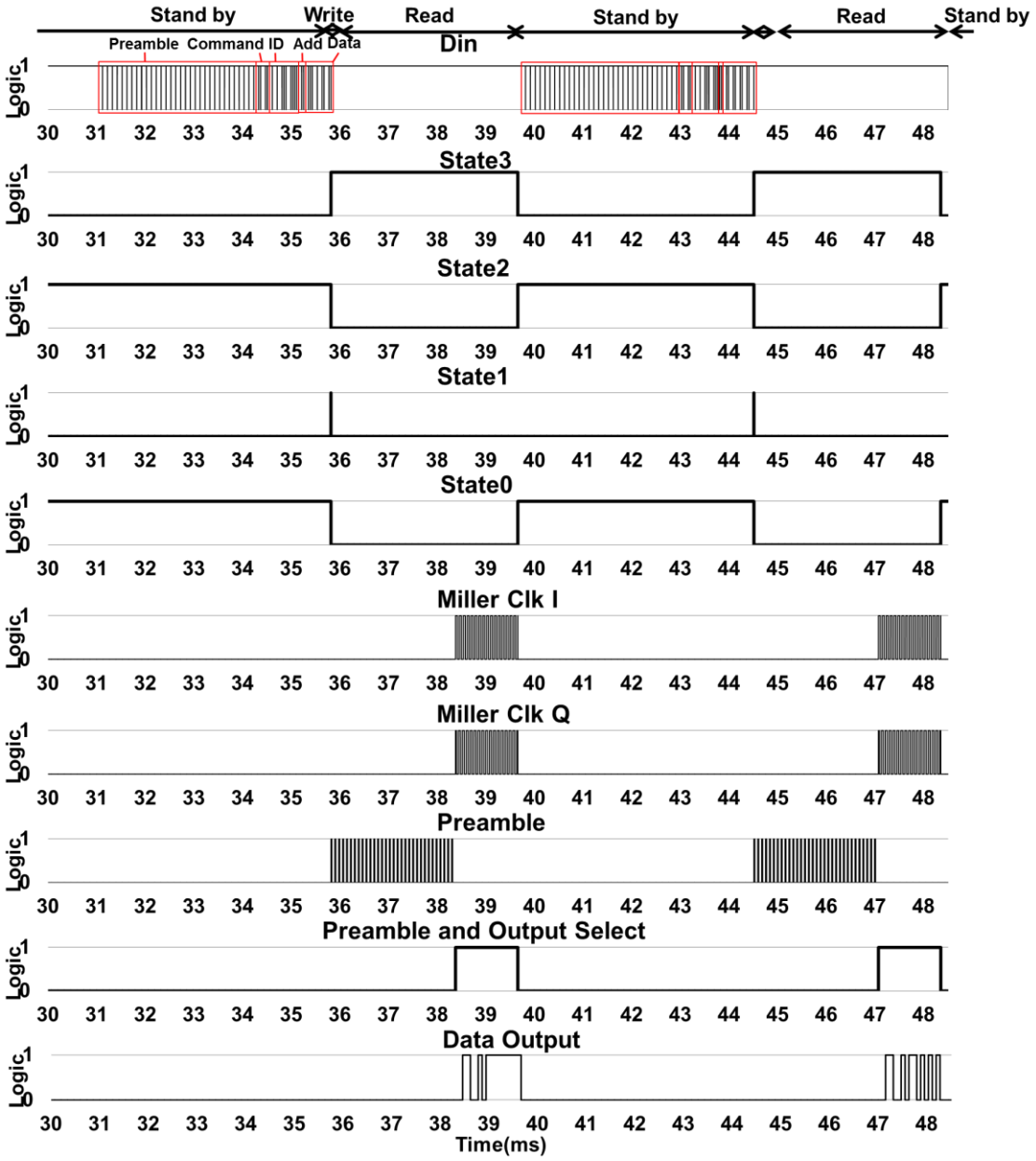


Figure 6.6 (a) Digital Baseband State Machine for Sensor Platform Stand Alone Testing (b) Digital Baseband State Machine Integrated with ADC and Sensor Multiplexer

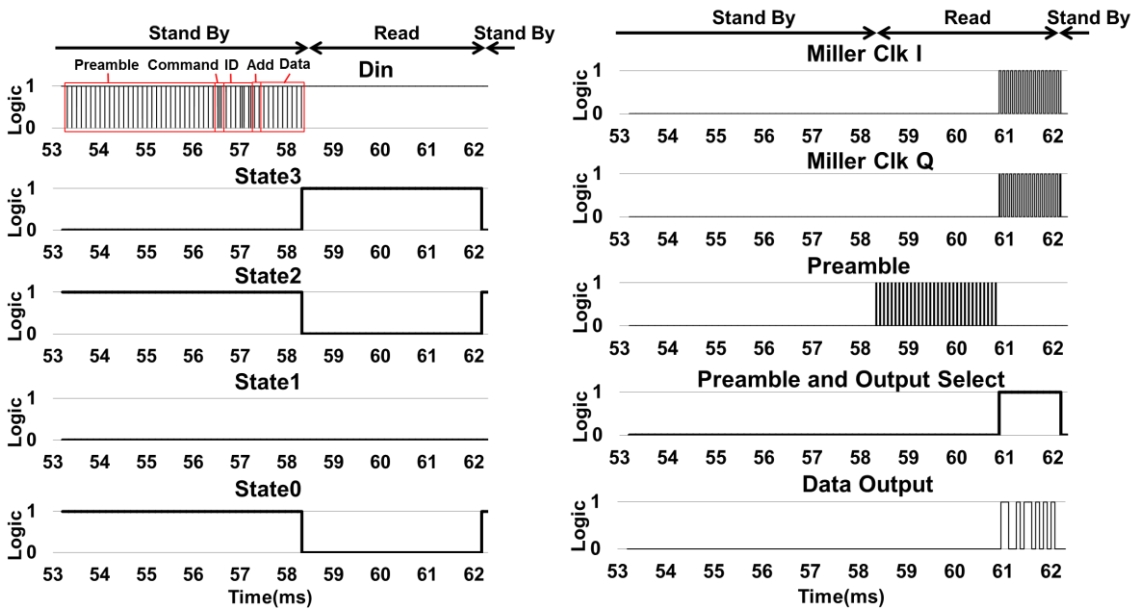
Synopsis Design Compiler was used for synthesizing the wireless node system that is composed of the integrated decoder, digital baseband block based on the state machine shown in Fig. 6.6(a). The entire system was simulated altogether using Mentor Graphic Modelsim as shown in Fig 6.7 with test bench generated POR and signal emulated demodulator outputs. Fig. 6.8 shows the simulation of the system synthesized by Synopsis Design Compiler with decoder and state machine shown in Fig. 6.6(b). The simulation in Figs. 6.7 and 6.8 shows correct transition between states during power up sequence and also upon input commands. In Fig. 6.7, data output after the Write command shows the same data that has been written into it, which indicates the correct functionality of this unit. Furthermore, Fig. 6.8 shows a successful integration with the digital unit of the analog to digital converter (ADC), which provides access to the data from the ADC using its clock.


Delay
Read
Stand By
POR
State3
State2
State1
State0
Miller Clk I
Miller Clk Q
Preamble
Preamble and Output Select
Data Output
Logic
1
0
0 0.5 1 1.5 2 2.5 3 3.5 4 4.5 5
Time(ms)

(a)

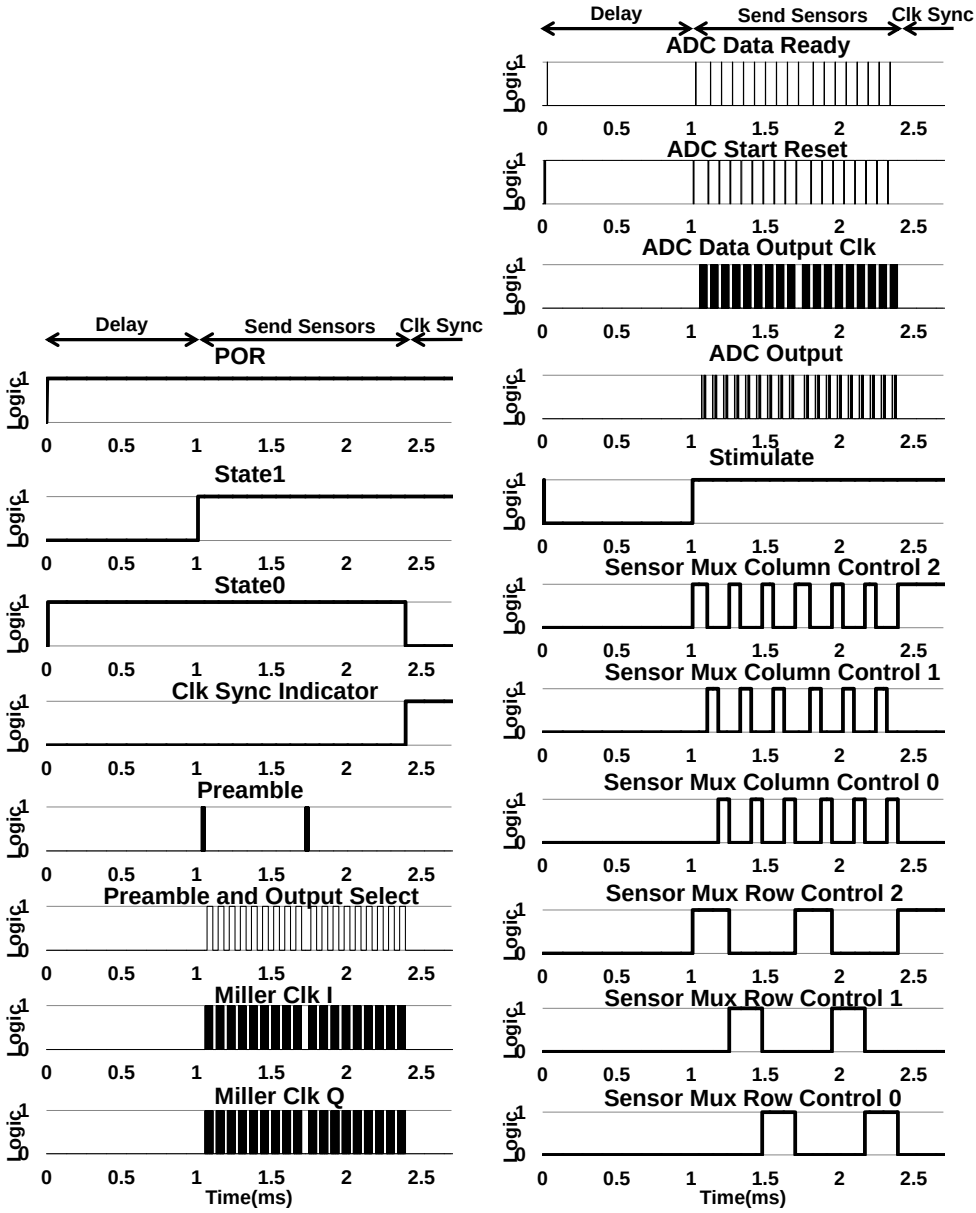

Stand by
Write
Read
Stand by
Read
Stand by
Preamble
Command
ID
Add
Data
Din
State3
State2
State1
State0
Miller Clk I
Miller Clk Q
Preamble
Preamble and Output Select
Data Output
Logic
1
0
30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48
Time(ms)

(b)

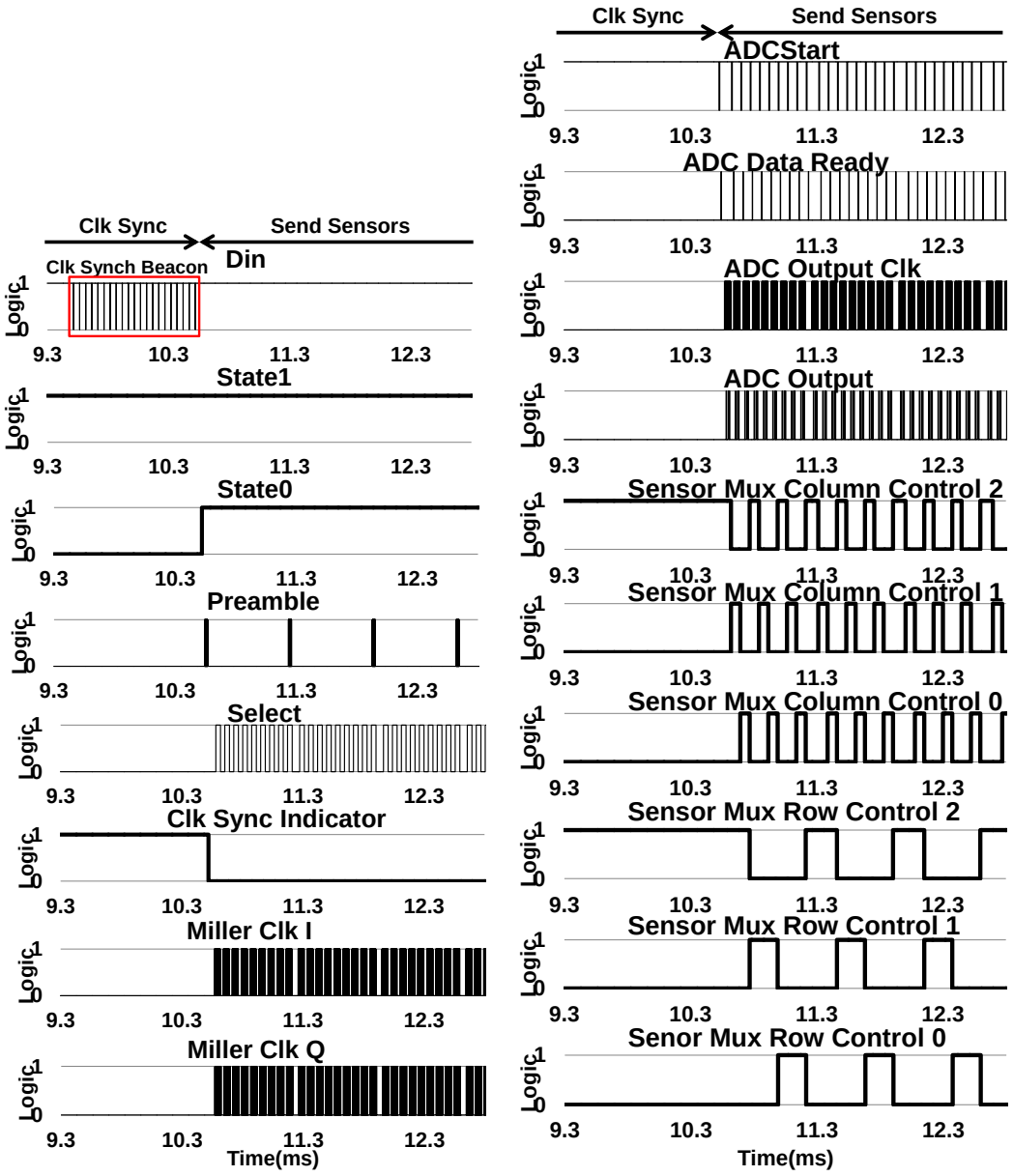


(c)

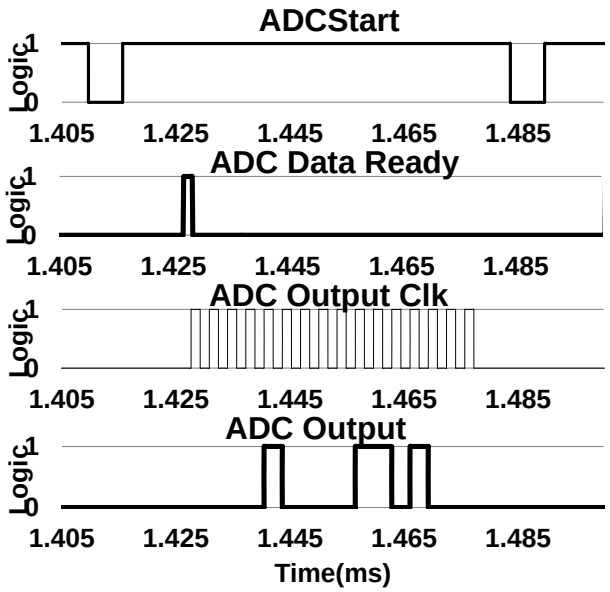
Figure 6.7 For Sensor Platform Stand Alone Test (a) Synthesized Decoder and Digital Baseband Operation from Power Off Sate to Delay State, Read and Standby state with POR Triggered. (b) Synthesized Demodulated Input, Preamble, Miller Encoder Controls, Output Data and States with Input Write Command with Writing Different Data into Two Different Registers. (c) Synthesized Demodulated Input, Preamble, Miller Encoder Controls, Output Data and States with Input Read Command.


Delay
Send Sensors
Clk Sync
POR
State1
State0
Clk Sync Indicator
Preamble
Preamble and Output Select
Miller Clk I
Miller Clk Q
ADC Data Ready
ADC Start Reset
ADC Data Output Clk
ADC Output
Stimulate
Sensor Mux Column Control 2
Sensor Mux Column Control 1
Sensor Mux Column Control 0
Sensor Mux Row Control 2
Sensor Mux Row Control 1
Sensor Mux Row Control 0
Logic 1
Logic 0
0 0.5 1 1.5 2 2.5
Time(ms)

(a)


Clk Sync
Send Sensors
Clk Synch Beacon
Din
State1
State0
Preamble
Select
Clk Sync Indicator
Miller Clk I
Miller Clk Q
ADCStart
ADC Data Ready
ADC Output Clk
ADC Output
Sensor Mux Column Control 2
Sensor Mux Column Control 1
Sensor Mux Column Control 0
Sensor Mux Row Control 2
Sensor Mux Row Control 1
Senor Mux Row Control 0
Logic 1
Logic 0
9.3
10.3
11.3
12.3
Time(ms)

(b)



(c)

Figure 6.8 Design for Integration with ADC and Sensor Multiplexers for Neuron Active Potential Sensors (a) Synthesized Decoder and Digital Baseband Operation from Power Off Sate to Delay State with POR Triggered, (b) Synthesized Demodulated Input, Preamble and Output Data (c) Zoomed-in View of ADC Control Signals

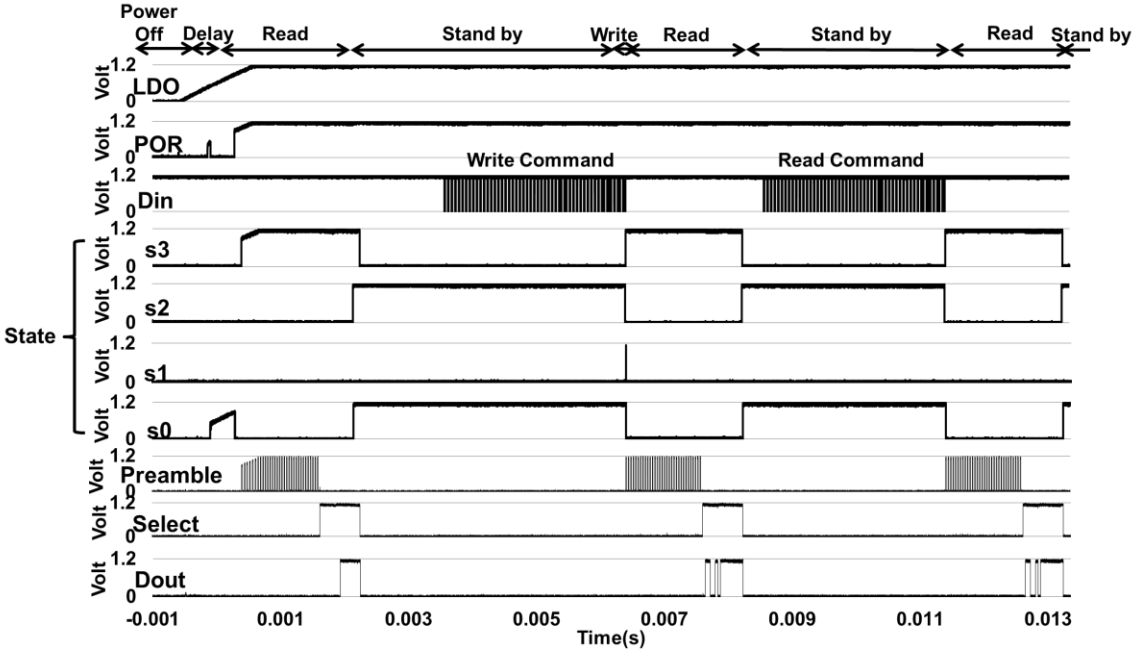


Figure 6.9 Digital Baseband Unit for Sensor Stand Alone Test Measurement with LDO, POR and Clock Generation Integrated

Synopsis design compiler indicates the digital baseband combined design for sensor node with the state machine shown in Fig. 6.6(a) has a static power consumption of 13.5 μW and a dynamic power of 0.3 μW based on 10 MHz toggle rate. The system based on the state machine shown in Fig. 6.69b) (with integrated sensors interface circuits and ADC), on the other hand, consumes 10.7 μW of overall power with 0.4 μW of dynamic power consumption. Note that a part of the baseband operation is less than 2 MHz clock frequency, which leads to even smaller dynamic power consumption. The majority of the power consumption, however, lays in the static power dissipation caused by transistor leakage currents. Therefore the overall power consumption will not deviate much from the simulated values.

7. CIRCUIT INTEGRATION

7.1 Layout Integration Placement of Each Circuit Module

The whole chip layout for wireless transceiver only in GF 45nm CMOS SOI technology is shown in Fig 7.1. The layout occupies 970 μm × 940 μm area (0.9 mm^2) including pads and 660 μm × 700 μm area (0.46 mm^2) when no test pads are utilized. Layout of the design with interface circuit and ADC and sensors has similar area with the previous design and the chip micrograph is shown in Fig. 7.2. Design can be further minimized with a tradeoff between the amounts of energy stored and the size of the storage capacitors, leading to a total chip area of less than 0.4 mm^2.

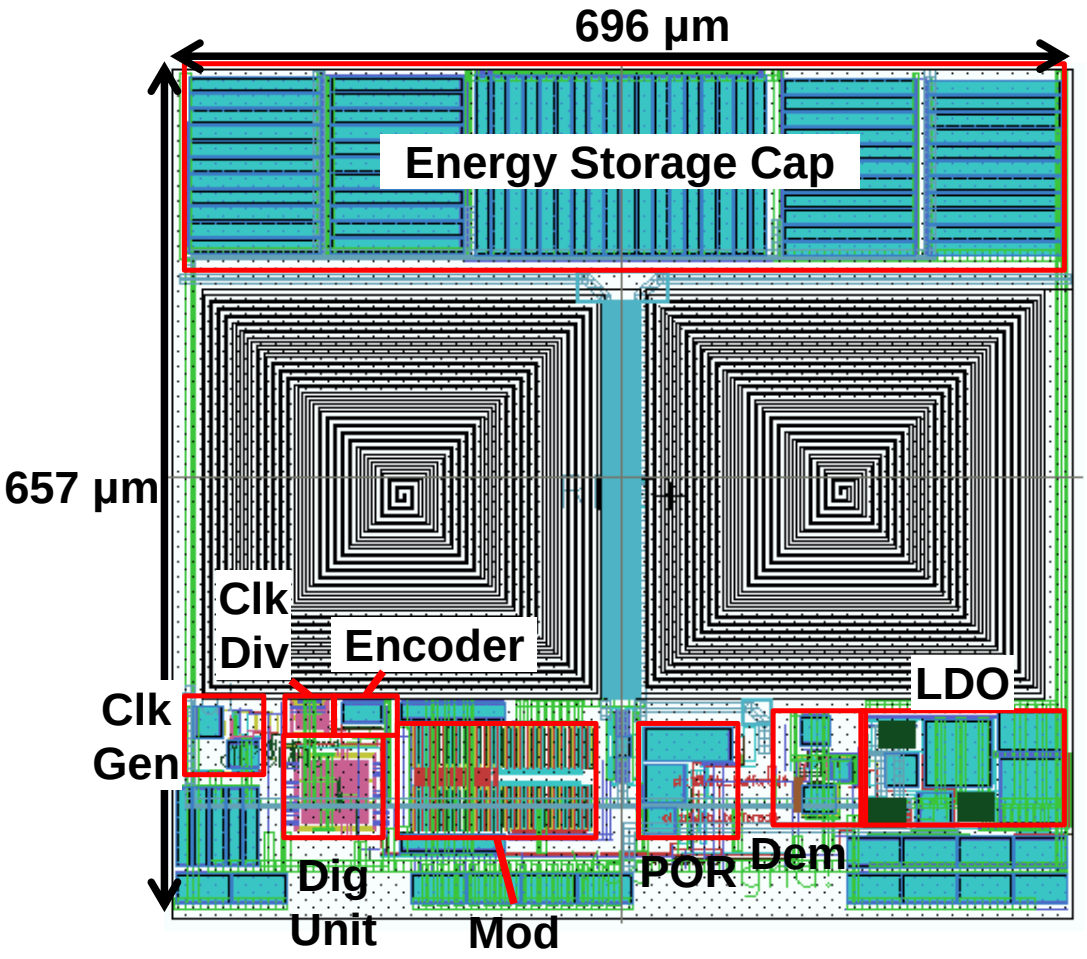


Figure 7.1 Integrated Passive Sensor Node Layout Design in GF 45nm CMOS SOI Technology

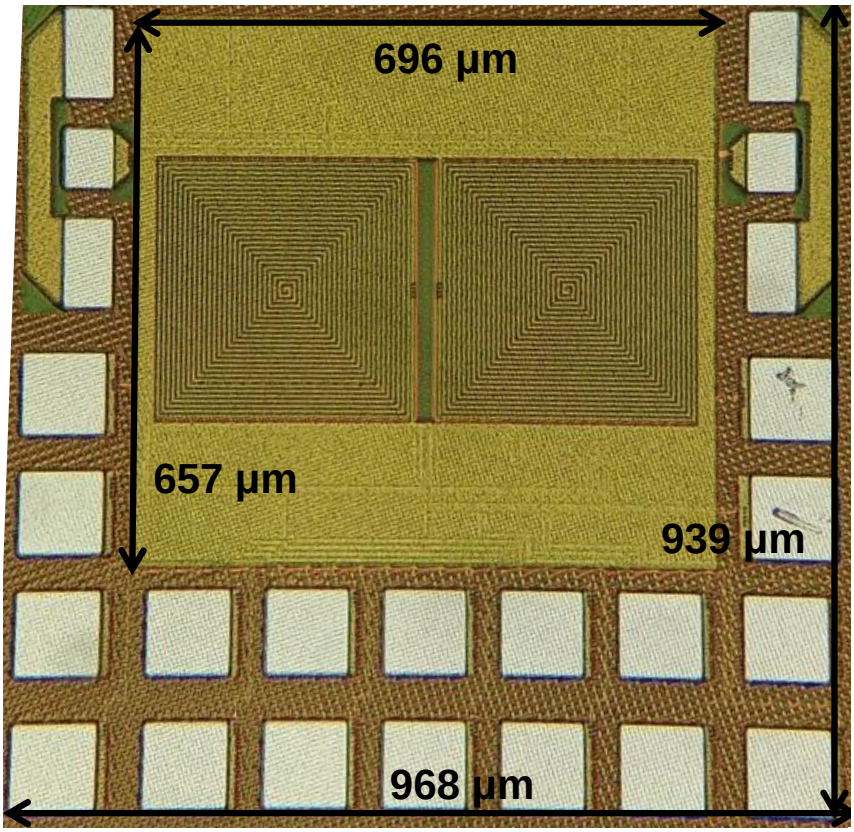


Figure 7.2 Micrograph of Integrated Passive Sensor Node in GF 45nm CMOS SOI Technology

7.2 Power Consumption with Integration

Initial tests have been performed on one of the designs. Power consumption of those circuit powered by the LDO is 67.7 µW when a Vdd of 0.9 V is used and increases to 114 µW when Vdd increases to 1 V. The simulated power consumption of each block is listed in Table 7.1. The major power consumption lies in the clock generator and encoder. The large power consumption of the encoder unit is mainly due to the charging of a large waveform smoothing capacitor and can be further optimized to reduce the overall power consumption.

Table 7.1 Steady State System Power Analysis

Module Connect to RF input	**RF Input Power (μW)**
Rectifier	835.1 (Vout = 1.76 V)
Demodulator	1.72
Modulator	830.8
LDO input power	355.8
LDO output power	190.3 (Vout = 0.99 V)
Modules Connected to Regulated Vdd	**DC Input Power (μW)**
Demodulator	0.9
POR	8.6
Clock Generator	27.2
Encoder	36.95
Backscatter Transistor Buffer	1.2 (72 when Mod On)
Digital Control Unit	16.35
Clock Tree Buffers	11.82

7.3 Time Duration of Operation

7.3.1 Standalone Sensor Platform Design

One way to resolve local heating and meet the FCC maximum exposure limit mentioned in Chapter 2 is to turn on and off the RF source power with a certain duty cycle thus the average power emitted over 6 minutes is less than the value regulated by the FCC. For the wireless transceiver design, the minimum of the RF source is powered on is the time sensor node requires to perform a single operation. This time is set by the sum of the time required for the power supply to become stable, the time for downlink command, and the time for the uplink response. These processes take 6.1 ms minimum for a single command operation as shown in Fig. 7.3. In this figure, the time required for

the power supply to become stable is 2 ms but can be reduced to about 100 μs if the rise time of the envelop signal of the RF power source is minimized.

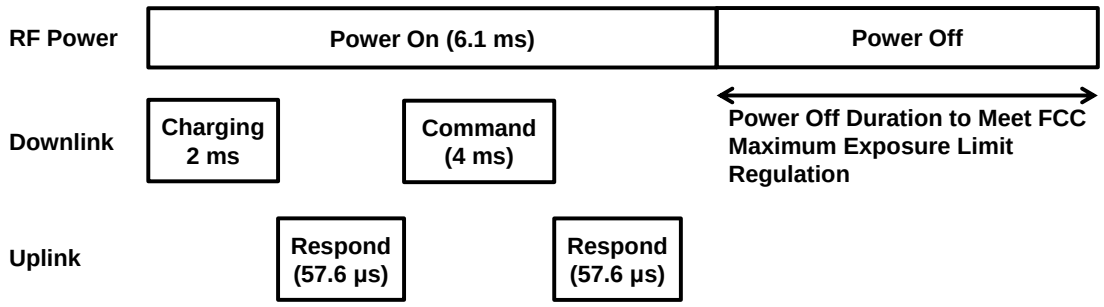


Figure 7.3 Standalone Sensor Platform Design Operation Downlink and Uplink Timing Diagram and Minimum Power on Duration

7.3.2 Design Integrated with ADC and Sensors

Comparing to wireless alone test purpose design, design with the integrated ADC, and sensors does not have downlink command but requires clock frequency synchronization beacon. Before measuring the biosensor response (e.g. active potential and field potential,) live cells and neurons may require stimulation from the sensor interface circuit. In the design with integrated ADC and sensors, there are 9 different sensor channels. The timing diagram of the stimulation recording and transmission of data is shown in Fig. 7.4. Note that it takes 0.5 ms to transmit the data from all these channels twice.

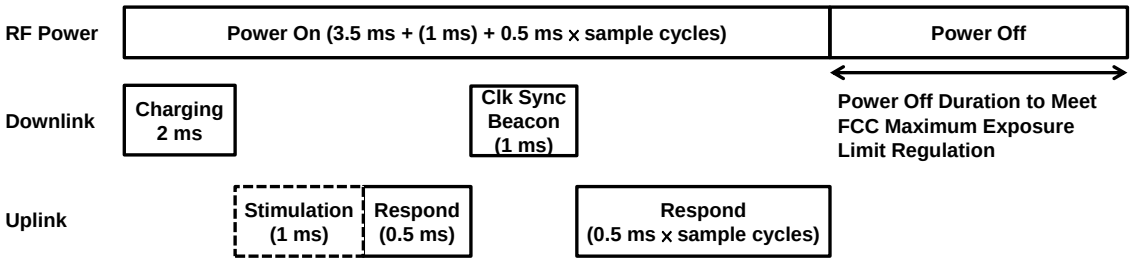


Figure 7.4 Sensor Platform Design with ADC and Sensors Operation Downlink and Uplink Timing Diagram and Minimum Power-on Duration

7.4 Comparison of Wireless Harvesting Single-Chip Radio

Table 7.2 shows previous work on single-chip RF powered radios that have been demonstrated to date. Only references [2] and [35] are designed with implantable application in mind. However, reference [35] is not designed with the optimum frequency for implant applications as discussed in Chapter 2 and large absorption of the EM signal in the tissue is expected. Furthermore, the distance for harvested rectified voltage of larger than 1V is only 3 cm. Furthermore, the wireless harvest performance is not reported for single chip operation. Although reference [2] is designed within optimized frequency range for bio implant application, inductive coupling utilized in this work does not scale well with distance and will be limited to mm range of operation as reported. Reference [36] is designed for non-implantable purpose, and as a result, is able to achieve higher antenna gain with smaller area at a much higher frequency than optimum frequency for biomedical implants. In this thesis, the distance and RF input power is estimated off the Rectenna with a load without backscatter transistor integrated. When the LDO is included, the power consumption is 123 μW at rectifier output with Vdd of 0.9 V and the sensor node is expected to be powered more than 10 cm away from the reader with a 36 dBm EIRP (see the measured performance of Rectenna in Chapter 2).

The free space path loss (FSPL) of backscattered signal can be estimated from equation $FSPL = 20log_{10}(d) + 20log_{10}(f) + 20log_{10}\left(\frac{4\pi}{c}\right)$, and leads to 12 dB path loss at 10 cm. From measurements presented in Chapter 3, backscattered power from 10 cm away will be about -78dBm and is still detectable with a reader topology of reference [73.] When the LDO is not included in the design, the power consumption is 67.7 μW at rectifier output voltage Vdd of 0.9 V is achieved and the sensor node is expected to operate from a distance of up to 16 cm away from the reader with a 36 dBm EIRP as presented in Chapter 2. And backscattered power is estimated to be -82 dBm when the sensor node is 16 cm away from the reader which is just about the limit of being detectable with the reader performance presented in reference [73.]

Table 7.2 Comparison of RF Powered Single-chip Radio

Reference	[2]	[5]	[35]	[36]		**This Thesis***	
Tech	CMOS 65nm	CMOS 0.18μm	CMOS 0.18μm	CMOS 65nm		**CMOS SOI 45nm**	
Freq s(GHz)	1.5	24	Rx: 5.2	Rx: 24		**0.95**	
			Tx: 2.4	Tx: 60			
Wireless Harvesting	Inductive Coupling	Far Field	Near Field	Far Field		**Near Field**	
Uplink Data Rate (bps)	800k	<4k	NA	>12M		**333k**	
Implant	Yes	No	Yes	No		**Yes**	
P_{RFin} (ERIP)	50 mW	NA	36	40	45	**36 (1000mW)**	
Dis (mm)	1	NA	30 (5mm Saline)	280	500	**160**	**100**
P_{DC} (μW)	10.5	13.2	513	1.5		**67.7**	**123**
Vdd (V)	0.5	1.8	1	0.9		**0.9**	
Area (mm^2)	0.125	6.9	4.8	4.4		**0.046**	

8. FUTURE WORK

Improving the design in terms of consumed power, performance and measurement set up for both wireless performance measurement and recorded data collection are some if the key aspects of the future work.

8.1 Measurement Improvement for GF 45nm CMOS SOI Sensor Tag

8.1.1 Reader Front-end Improvement

Reader front-end circuit needs larger suppression from the PA leakage power in order to further amplify and demodulate the back-scattered signal from the sensor node without saturating the LNA stage as mentioned in Chapter 3. Further suppression of the PA signal may be achieved by an automatic phase and attenuation control with sufficient resolution in amplitude and phase tuning that tracks and adjusts the cancellation signal [71, 72, 73, and 74].

8.1.2 Specific Absorption Rate (SAR) Local Heating Characterization

Characterizations of local heating with different power on duration, power and distance at 950 MHz to determine duty cycle needed to meet FCC requirements and SAR effects on human along with the sample rate and duration needed per sample when integrating with biomedical sensors. As discussed in Chapter 2, Rectenna with high

resistivity silicon substrate requires 13 dB less power compared to the one on low resistivity substrate and might not encounter the tissue local heating limitations. Furthermore, according to the simulation results, real resonant impedance of Rectenna with silicon substrate removed is even higher than the one on the high resistivity silicon substrate leading to the same rectifier output voltage at much less RF powers. The reduction of the required RF power further alleviates the local heating of the live tissue.

8.1.3 Wireless System Performance Measurement

Wireless system characterizations through bit-error-rate measurements at different distance, transmitting powers, and various angles between the reader antenna and wireless sensor chip and measurement within live tissues are required to understand the range and optimal performance of the device.

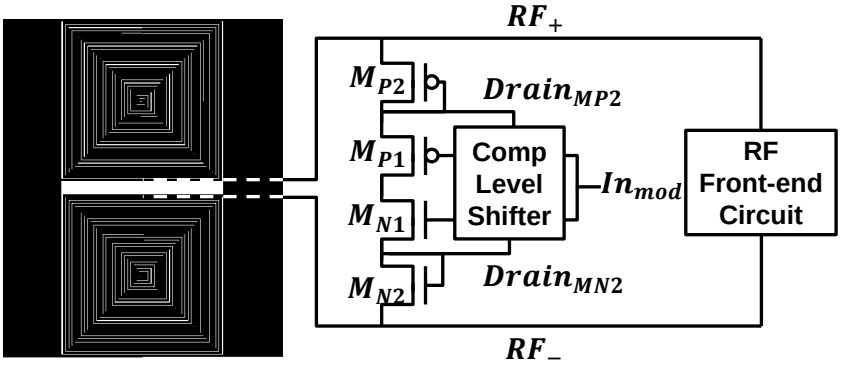
8.2 Circuit Improvements

8.2.1 Front-End Power Deliver Efficiency

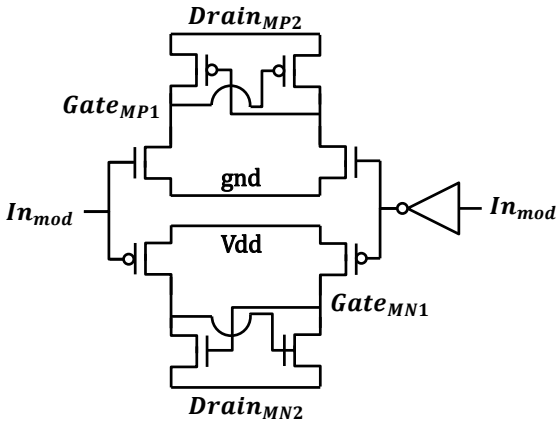
8.2.1.1 Modulator Leakage Power during Modulator Off Period Improvement

With current design, half of the RF power is dissipated in the modulator due to partial turn on of the modulator during the operation cycle as shown in Table 7.1. A new design is proposed in Fig. 8.1. According to the simulation the power dissipation will be reduced by 68% of its original, leading to a reduction from 50% of the total input RF power to 24%, reducing the total RF input power required by 34%. Backscattering

modulator on current is only reduced by only 9% of the original value leading to more or less similar backscattered power measured at the reader.



(a)



(b)

Figure 8.1 (a) New Proposed Modulator Design with Standby Power Consumption Improvement (b) Complementary Level Shifter Used in New Proposed Modulator

8.2.1.2 Rectenna Matching Optimization

Rectifier transistor size can be further optimized with front-end circuit to reduce matching loss.

8.2.2 Demodulator

An improve demodulator circuit to reduce the modulation index is needed. This improved design helps minimizing RF input power change which leads to less variations of the rectifier and LDO output have voltage with the modulation.

8.2.3 Power Management

Further lowering of the power consumption especially by encoder and clock generator circuit is required. The drop-out voltage of the LDO design needs to be optimized to achieve maximum efficiency. Also, to reduce the ripple voltage of the LDO, a more sophisticated voltage comparator unit with different voltage dividing ratios is required that can provide both coarse and fine tuning as described in reference [62].

8.2.4 System Integration with ADC and Sensor Multiplexer

Verification of the whole system with post-layout simulation needs to be done to ensure the driving capability of clock lines and digital signal outputs when integrated with ADC and sensor interface circuits.

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