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K. P. Drummond

D. Back

M. D. Sinanis

D. B. Janes

D. Peroulis

See next page for additional authors

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Authors
K. P. Drummond, D. Back, M. D. Sinanis, D. B. Janes, D. Peroulis, J. A. Weibel, and S V. Garimella

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Characterization of Hierarchical Manifold Microchannel Heat Sink Arrays Under Simultaneous Background and Hotspot Heating Conditions [1]

Kevin P. Drummond [(a,c)], Doosan Back [(b,c)], Michael D. Sinanis [(b,c)], David B. Janes [(b,c)], and Dimitrios Peroulis [(b,c)], Justin A. Weibel [(a,c)], Suresh V. Garimella [(a,c)2]

[(a)] Cooling Technologies Research Center, an NSF I/UCRC and School of Mechanical Engineering

[(b)] School of Electrical and Computer Engineering

[(c)] Birck Nanotechnology Center

Purdue University, West Lafayette, Indiana 47907 USA

Abstract: A hierarchical manifold microchannel heat sink array is fabricated and experimentally characterized for uniform heat flux dissipation over a footprint area of 5 mm × 5 mm. A 3 × 3 array of heat sinks is fabricated into the silicon substrate containing the heaters for direct intrachip cooling, eliminating the thermal resistances typically associated with the attachment of a separate heat sink. The heat sinks are fed in parallel using a hierarchical manifold distributor that delivers

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[2] Corresponding author: sureshg@purdue.edu

flow to each of the heat sinks. Each heat sink contains a bank of high-aspect-ratio microchannels; five different channel geometries with nominal widths of 15 μm and 33 μm and nominal depths between 150 μm and 470 μm are tested. The thermal and hydraulic performance of each heat sink array geometry is evaluated using HFE-7100 as the working fluid, for mass fluxes ranging from 600 kg/m^{2}s to 2100 kg/m^{2}s at a constant inlet temperature of 59 °C. To simulate heat generation from electronics devices, a uniform background heat flux is generated with thin-film serpentine heaters fabricated on the silicon substrate opposite the channels; temperature sensors placed across the substrate provide spatially resolved surface temperature measurements. Experiments are also conducted with simultaneous background and hotspot heat generation; the hotspot heat flux is produced by a discrete 200 μm × 200 μm hotspot heater.

Heat fluxes up to 1020 W/cm^2 are dissipated under uniform heating conditions at chip temperatures less than 69 °C above the fluid inlet and at pressure drops less than 120 kPa. Heat sinks with wider channels yield higher wetted-area heat transfer coefficients, but not necessarily the lowest thermal resistance; for a fixed channel depth, samples with narrower channels have increased total wetted areas owing to the smaller fin pitches. During simultaneous background and hotspot heating conditions, background heat fluxes up to 900 W/cm^2 and hotspot fluxes up to 2,700 W/cm^2 are dissipated. The hotspot temperature increases linearly with hotspot heat flux; at hotspot heat fluxes of 2,700 W/cm^2, the hotspot experiences a temperature rise of 16 °C above the average chip temperature.

Keywords: boiling; two-phase flow; manifold; microchannel; hotspot; HFE-7100

Nomenclature

A	area
d	depth
D_H	hydraulic diameter
c_p	specific heat
G	mass flux, $G = \dot{m}/(2N_{sink}N_cA_c)$
h_{wet}	heat transfer coefficient
h_{LV}	latent heat of vaporization
I	electrical current
k	thermal conductivity
L	length
$\dot{m}$	mass flow rate
N_c	number of channels per heat sink
N_{sink}	number of heat sinks
P_{el}	electrical power
P_c	channel perimeter
Q_{loss}	heat loss
Q_{net}	net heat input
q''	heat flux
$R_{HS,heater}$	hotspot heater electrical resistance
$R_{HS,tot}$	combined electrical resistance of hotspot heater and traces
R''_{th}	overall thermal resistance
R''_{cond}	conduction thermal resistance
R''_{fluid}	caloric thermal resistance
T	temperature
$T_{fl,ref}$	fluid reference temperature
V	voltage
$\dot{V}$	volumetric flow rate
w	width
x_{out}	outlet thermodynamic quality
z	location along channel

Greek symbols

ρ	mass density
η_f	fin efficiency
η_0	overall surface efficiency

Subscripts

avg	average
base	base of channels
BG	background

c	channel	*sat*	saturation
chip	chip surface	*sens*	sensible
el	electrical	*Si*	silicon
f	fin	*sink*	heat sink
fl	fluid	SiO_2	silicon dioxide
HS	hotspot	*tot*	total
i	individual zone	*w*	wafer
in	inlet	*wet*	wetted area
out	outlet		

1. Introduction

Chip-level heat fluxes exceeding 1,000 W/cm² must be dissipated while maintaining chip temperatures at levels safe for reliable operation of next-generation radar, power electronics, and high-performance computing systems [1,2]. Indirect cooling utilizes a heat sink that is separated from the silicon die with a heat spreader inserted between. Large temperature rises across this stack occur due to the parasitic thermal interface and spreading resistances between the device and attached heat sink. Additionally, non-uniform heating — specifically localized hotspot heating — can cause extreme temperature variations across chip surfaces. These application trends necessitate the development of transformative evaporative cooling strategies, with coolant channels deployed directly in the semiconductor device, to enable improved functionality of electronic systems. While direct, intrachip cooling allows for reduced conduction resistances and eliminates contact resistances, there is little material thickness between the heat-generating device and heat sink

available for heat spreading; this exposes the heat sink directly to the high heat fluxes generated from the device and necessitates higher heat transfer coefficients to maintain the desired low thermal resistance across the heat sink. Local hotspots also can lead to high local chip temperatures and large temperature gradients across the device.

Heat sinks containing deep, high-aspect-ratio microchannels provide high heat transfer coefficients and large area enhancement, which make them a candidate for high-heat-flux applications. Single-phase microchannel heat sinks have been widely studied for electronics cooling applications [3,4]. In general, increasing channel depth, decreasing channel width, and increasing fluid flow rate all allow for larger heat dissipation over a given chip area at a given chip temperature. However, there are practical limits to how deep and narrow channels can be made. Additionally, pressure drop along the length of the channels leads to large pumping power requirements at small channel diameters and high flow rates. Two-phase operation can enable reductions in size, weight, and overall power consumption when compared to single-phase systems, which can lead to lower overall system costs. Two-phase evaporative cooling in traditional microchannel heat sinks has been widely explored and found to improve surface temperature uniformity and heat dissipation efficiency relative to single-phase cooling [5–8]. Even with the advances in performance achieved via evaporative cooling in current designs, the maximum heat dissipation remains limited by impractically large pressure drops as the channel dimensions decrease and vapor fractions increase.

Manifold microchannel heat sinks decouple the dimensions of the device being cooled from the flow length by introducing the working fluid at multiple locations along the length of the channels, resulting in multiple flow paths of decreased effective flow length. Figure 1(a) shows a

traditional microchannel heat sink which contains a single inlet, a bank of microchannels spanning the entire device length, and a single outlet; Figure 1(b) shows a manifold microchannel heat sink design where the heated area is discretized into an array of multiple heat sinks, each with separate inlets and outlets fed in parallel. The pressure drop is significantly reduced at a given mass flux in this configuration due to the decrease in channel flow length. In most manifold microchannel heat sink designs, the manifold layer is overlaid on the heat sink channels; the manifold consists of an inlet header on one side of the chip with an outlet header on the opposite side, as described in Ref. [9]. The inlet and outlet headers each have many parallel flow passages in the manifold that span the width of the chip. The distance between adjacent inlet and outlet manifold flow passages dictates the flow length in the heat sinks channels.

A number of numerical studies have identified optimized geometries for both the fluid distribution manifold and the microchannel heat sink in single-phase operation [10–20]. The optimal geometric and operational parameters depend on the desired heat flux removal and allowable pumping power, but these studies have shown that manifold microchannel heat sinks can increase heat dissipation without significantly increasing pressure drop compared to conventional microchannel heat sinks. For example, Ryu *et al.* [12] found that manifold microchannel heat sinks can remove over 50% more heat from a given area than a conventional microchannel heat sink at the same allowable pressure drop. Experimental studies have also shown that manifold microchannel heat sinks can dissipate high heat fluxes at moderate pressure drops [20,21,9]. However, due to the increased number of parallel flow paths in manifold microchannel heat sinks, flow maldistribution between channels, caused by uneven pressure drops in the manifold, can cause significant performance reduction. The shape of the flow passages in the

manifold is critical to the flow distribution into the heat sink channels. Manifolds with constant cross-sectional area passages result in heat sink channels at the end of the manifold receiving a disproportionately large portion of the total flow [13,18]. For the geometry and flow rates studied, Tang *et al.* [18] showed that the four heat sink channels (out of 10 total) farthest from the header received 85% of the total flow, with the last channel receiving over 35 %. Similarly, Escher *et al.* [13] showed that there is a 70% difference in mass flow rate between the channel at the beginning of the manifold and the last channel. This amount of flow maldistribution can lead to significant chip temperature gradients and hotspots across the chip surface. Both studies found that flow maldistribution can be drastically reduced, but not eliminated, during single-phase operation by using tapered flow passages in the manifold.

Two-phase operation of manifold microchannel heat sink systems has not been widely investigated. In one study, Baummer *et al.* [21] demonstrated dissipation of a heat flux of 300 W/cm² over a 1 cm² area using a manifold microchannel heat sink having 42 μm wide and 483 μm deep channels. In our previous study [22], hierarchical manifold microchannel heat sinks were experimentally tested during two-phase operation using HFE-7100 as the working fluid; the array of heat sinks was fabricated directly into the silicon wafer containing the heaters and matched the heated area of 5 mm × 5 mm. Each heat sink contained a bank of 50 high-aspect-ratio microchannels with nominal channel widths of 15 μm and channel depths between 35 μm and 300 μm. Because channel width was constant for all samples, the effect of channel width could not be studied. For a fixed heat flux and channel mass flux, chip temperature decreased with increasing channel depth due to the increase in wetted area. Increasing mass flux also decreased chip temperatures for a fixed heat flux, with diminishing returns at high mass fluxes. Heat fluxes over

900 W/cm² were dissipated at chip temperatures less than 50 °C above the fluid inlet temperature and pressure drops less than 165 kPa.

In many practical electronics cooling applications, non-uniform heat flux generation is common, and must be accommodated by the heat sink design to limit temperature gradients in the chip. For example, Sharma *et al.* [15,23] tested a manifold microchannel heat sink designed to dissipate non-uniform heat fluxes more effectively by utilizing varying channel geometries depending on spatial location on the chip. Background heat fluxes of 20 W/cm² with periodic 300 W/cm² hotspots evenly distributed across the chip surface were considered; chip temperature uniformity was maintained within a 15 °C spread using single-phase water as the working fluid. Lorenzini *et al.* [24] modelled and experimentally tested pin fin heat sinks with variable pin sizes and pitches to dissipate a hotspot heat flux superimposed on a background heat flux. Hotspot heat fluxes up to 750 W/cm² were dissipated with a 250 W/cm² background heat flux, with the local substrate temperature at the hotspot remaining below the maximum substrate temperature, which occurred near the fluid outlet. Abdoli *et al.* [25] modelled a pin-fin heat sink with a hotspot heat flux of 2,000 W/cm² superposed on a background heat flux of 1,000 W/cm². Using single-phase water as the working fluid, they predicted that an array of pin fins would yield spatial temperature uniformity with a maximum variation of less than 10 °C. Recent heat sink designs have targeted simultaneous dissipation of a high, uniform die-level heat flux (>1,000 W/cm²) with significantly higher heat flux hotspots representative of RF electronic devices. Technologies that have been evaluated include a GaN-on-diamond manifold microchannel heat sink [26], an embedded pin-fin heat sink with a manifold fluid distributor [27], a manifold microchannel heat sink with non-uniform channel height and shape [28], and a heat sink employing fluid impingement onto

diamond-lined, silicon-carbide microchannels [29]. Additional complexities arise in evaporative heat sink systems during non-uniform heating. For example, Ritchey *et al.* [13-14] found that non-uniform heating can lead to flow instabilities and flow maldistribution that induce premature critical heat flux during two-phase operation of microchannel heat sinks.

The present work focuses on further characterizing intrachip heat sink systems that utilize hierarchical manifolds to distribute flow to microchannel arrays during two-phase operation. This work aims to build upon our previous work on characterization of a hierarchical manifold microchannel heat sink array [22] by investigating a broader set of channel geometries that includes channel width variations, as well as subjecting the heat sink to hotspot heat fluxes. The effects of channel dimensions and mass flux are studied for heat sinks with banks of small-width, high-aspect-ratio microchannels. Results are presented for the cooling of a uniform background heat flux and with simultaneous hotspot heating.

2 Approach

A manifold microchannel heat sink distributes coolant through multiple inlets and outlets along the length of the heated area such that the flow length through the microchannels is significantly reduced. In the current work, a multi-level, hierarchical manifold is used to feed an array of intrachip microchannel heat sinks featuring high-aspect-ratio channels. Direct liquid cooling minimizes conduction resistances and eliminates contact resistances that result from approaches relying on externally attached heat sinks. Figure 2 shows the fluid flow paths in a manifold microchannel heat sink; fluid from the manifold (not shown) arrives normal to the microchannels through a plenum plate, which defines the inlets and outlets to the channels. The

flow impinges on the channel base, splits and travels along the channel in both directions, and exits the channels through the plenum plate.

A thermal test vehicle is fabricated to demonstrate the thermal and hydraulic performance of the hierarchical manifold microchannel heat sink array; Figure 3(a) shows the thermal test vehicle with a half-symmetry section removed and Figure 3(b) shows a zoomed-in view of the test chip with a quarter-symmetry removed to show the channel features and internal fluid flow paths. The system consists of a manifold base, manifold distributor, plenum interface plate, microchannel plate, and printed circuit board (PCB). The manifold base is used to interface with the flow loop and contains ports for inlet and outlet temperature and pressure measurements. The manifold distributor (Figure 3(c-f)) splits the single fluid inlet into nine parallel flow streams that enter the 3 × 3 array of microchannel heat sinks covering the 5 mm × 5 mm chip area; each heat sink covers a footprint area of 1667 μm × 1667 μm with channels covering 1500 μm × 1500 μm; after traveling through the channels, the manifold combines the 18 flow streams into a single fluid outlet. The plenum plate matches the finest-level manifold features and provides smooth surfaces for sealing between the manifold distributor and the microchannels. The microchannel plate contains the 3 × 3 array of heat sinks, each with a bank of parallel, high-aspect-ratio microchannels; the opposite side of the microchannel plate is instrumented with heaters and sensors to evaluate the thermal performance. The PCB provides a convenient electrical interface to the heaters and sensors (Figure 3).

3 Test vehicle fabrication and assembly

3.1 Test chip fabrication

All fabrication steps were performed in the Birck Nanotechnology Center at Purdue University. This section provides an abbreviated overview of the fabrication steps detailed in Ref. [22]. While the heater layout and channel dimensions are different in the current work, all fabrication steps are the same.

Starting with a thermally oxidized 4-inch silicon wafer, high-aspect-ratio microchannels were deep reactive-ion etched on one side of a silicon wafer using the Bosch process. On the opposite side of the wafer, heater and sensor features were patterned using a lift-off process. The heaters and resistance temperature detectors (RTDs) consist of a 20-nm layer of Pt deposited on top of a 5-nm adhesion layer of Ti. The heater and RTD lead-wire traces are a 400-nm thick layer of Au on top of a 10-nm layer of Ti. The silicon dioxide layer was then removed from the channel side of the wafer using a buffered oxide etch. Figure 4(a) shows a schematic diagram of the microchannel plate cross-section (features are not to scale). This fabrication process was repeated (while adjusting the channel pattern and etching parameters) to achieve multiple channel geometries; the critical channel dimensions, measured from scanning electron microscopy (SEM) images (Figure 5), are summarized in Table 1. The listed number of channels, N_c, is for a single heat sink; the total number of channels is calculated by multiplying the number of channels per heat sink by the number of heat sinks, N_{sink}, which is held constant at nine for the current work. The channel cross-sectional area is based on the actual perimeter along the channel boundary, accounting for any tapering in the channel sidewalls and curvature at the bottom of the channels. Channel wetted area includes the sidewall surfaces, base surface, and surfaces at the ends of the

channels ($A_{wet} = P_cL_c + 2w_ch_c$); the wetted area of the manifold is not included because the manifold temperature is expected to be significantly lower than the channels due to contact resistance at the interface. It is noted that the 15×150 and 15×300 samples were previously characterized in Ref. [22].

Plenum plates, which contain through-features that define the fluid inlet and outlet regions to the microchannels, were fabricated using separate 4-inch silicon wafers. These features were patterned and deep reactive-ion etched through the wafer; the silicon dioxide layer was then removed using a buffered oxide etch and the wafer was cleaned. A schematic diagram of the final cross-section is shown in Figure 4(b).

The 4-inch microchannel wafers were diced into 20 mm × 20 mm dies with the heaters, RTDs, and microchannels occupying the center 5 mm × 5 mm area of the channel wafer. Similarly, the plenum wafers were diced into 20 mm × 20 mm dies with the fluid -routing features covering the center 5 mm × 5 mm area.

Figure 6(a) shows the layout of the heaters and temperature sensors on the thermal test chip. The background heaters are patterned over nine zones that match the locations of the 3 × 3 grid of microchannel heat sinks on the opposite side. Figure 6(b,d) show an example trace layout for a single zone that does not contain the hotspot heater. In each such zone, the heater is composed of nine linear resistors powered in parallel. Lead wires deliver power to each end of the resistors and terminate at two pads located along the periphery of the test chip; these pads are wire-bonded to a printed circuit board (PCB) in the subsequent assembly steps. Two RTDs are patterned in each zone, providing 18 total temperature measurements over the 5 mm × 5 mm chip area. Each four-wire RTD contains two lead wires to supply electrical current and two wires to measure voltage.

Figure 6(c,e) show the heater layout for the central zone that contains the hotspot. In this zone, the background heater is divided into two parallel arrays of four resistors each, with the hotspot heater positioned tightly in between the background heaters.

3.2 Test chip assembly

A custom printed circuit board (PCB) was designed for connection of the wire-bonded pads to the data acquisition system and to the heater power supplies. The outer edge of the channel plate was fixed to the underside of the PCB using epoxy. All the electrical traces for each of the background heaters, hotspot heater, and 18 four-wire RTDs are wire-bonded to corresponding gold contact pads on the PCB. Figure 7 shows photographs of the assembled test chip.

3.3 Manifold fabrication

A multi-layer, hierarchical manifold distributor is used to deliver fluid to the array of microchannel heat sinks. The hierarchical manifold architecture allows for scaling to larger footprint dimensions and smaller inlet and outlet features [32]. The manifold consists of four layers of laser-cut (PLS65MW, Universal Laser Systems) acrylic sheets and an acrylic base, as shown in Figure 3(c-f). The laser-cut layers contain the hierarchical network of channels that distribute flow from a single inlet to the array of heat sinks; these layers are assembled with 100 μm-thick double-sided adhesive sheets (9150, Nitto Denko) that are laser-cut to match the fluid-routing features. The acrylic base routes fluid from the flow loop to the bonded sheets and contains ports for inlet and outlet pressure and temperature measurements. A silicone gasket is laser-cut and is used to seal between the acrylic base and manifold layers. One side of the plenum plate is bonded to the manifold using a 10 μm-thick double-sided adhesive (9105, Nitto Denko) that is laser-cut to match

the dimensions of the plenum plate; the opposite side of the plenum plate is bonded to the microchannel plate using the same adhesive. The adhesive is aligned on the manifold using guide pins before attaching the test chip.

3.3 Test vehicle assembly

Stainless steel fittings are inserted into the manifold base for fluid connections to the flow loop and placement of thermocouples and pressure transducers. A PEEK insulation block is used to limit heat lost from the chip to the environment. The heaters that are used to provide the background heat flux are all wired in parallel to a programmable DC power supply (XG100-8.5, Sorensen). A variable resistor is added in series with each heater; during testing, this variable resistor can be adjusted to ensure that a uniform background heat flux is generated. The voltage drop across each background heater is measured using a divider circuit to step down the voltage, and the corresponding electrical current is measured using a shunt resistor (Y14880R10000B9R, Vishay). The overall electrical current supplied to the background heaters is measured using a shunt resistor (HA-5-100, Empro). The hotspot heater is wired to a separate power supply (1550, B&K Precision); hotspot voltage drop and current were measured in the same manner as the background heater zones. The RTDs are wired to a constant-current power supply and the data acquisition system using a ribbon cable.

4 Experimental methods

4.1 Flow loop

A two-phase test loop is used to evaluate the chip temperature rise and pressure drop across the heat sink for a specified fluid mass flux, fluid temperature at the test section inlet, and pressure

at the test section outlet. A detailed description of the flow loop can be found in Ref. [22]; the key components and sensors are briefly summarized here.

An adjustable reservoir maintains system pressure during testing, while a magnetically-coupled gear pump (GB-P23, Micropump) circulates fluid through the test section. The fluid mass flow rate is measured using a Coriolis mass flow meter (CMF010M, Micromotion). The test section inlet and outlet absolute pressures are measured with pressure transducers (S-10, WIKA) and the pressure drop across the test section is measured with a differential pressure transducer (PX2300, Omega). Inlet and outlet temperatures are measured using calibrated T-type thermocouples. The test section inlet temperature is controlled using an inline heater. All data are monitored and collected through a LabVIEW interface using a NI cDAQ-9178 chassis with appropriate input modules.

4.2 Test chip calibration

The RTDs patterned directly on the back side of the microchannels were calibrated in a laboratory oven at temperatures spanning the operational temperature range. A Pt100 RTD (PR-10-3-100, Omega) was placed in the oven with the test chip and was used as the reference temperature for the calibration. A linear regression was used to interpolate the temperature dependence of electrical resistance and develop a unique calibration for each of the 18 sensors.

Heat loss from the test vehicle assembly, Q_{loss}, was estimated by draining the test section of fluid and then applying a uniform background heat input. Once the system reached a steady-state condition, the temperature of each RTD on the chip surface was recorded. The temperatures were then averaged spatially and temporally to determine the average chip temperature, $T_{chip,avg}$. This procedure was repeated for heat inputs that resulted in a range of chip temperatures

experienced during the experiments. A best-fit line to the temperature-dependent heat loss gave the equation: $Q_{loss} = 0.02768 * (T_{chip,avg} - 22.52)$.

4.3 Test procedure

Dissolved air is removed from the working fluid, HFE-7100, via vigorous boiling of fluid in the reservoir and subsequent recollection of condensate. The flow loop is then sealed from the environment and degassed fluid is circulated at the desired flow rate; the mass fluxes, flow rates and Reynolds numbers for each sample are shown in Table 2. The fluid inlet temperature is maintained at 59 °C and the outlet pressure is maintained at 121 kPa (corresponding to a saturation temperature of 65 °C). Power to the background heaters is stepped up in small increments from zero to a power at which a maximum RTD temperature reading of 130 °C is recorded; testing is ceased at this point to prevent damage to the heaters and wire bonds. Once steady-state conditions are reached for a fixed power level, data are collected at a rate of 6,000 Hz for 2 min. These data are time-averaged to yield a single steady-state data point.

To investigate the effect of a hotspot on chip temperatures, a fixed uniform background heat flux is applied to the entire 5 mm × 5 mm chip area while the power to the 200 μm × 200 μm hotspot heater is increased in ~550 W/cm² increments up to a heat flux of ~2,700 W/cm². The process is repeated at multiple background heat fluxes. The hotspot heat flux is limited below 3,000 W/cm² to avoid potential electromigration at high current densities.

4.3 Data reduction

The fluid mass flux through each channel is calculated using $G = \dot{m}/(2N_{sink} N_c A_c)$. Electrical power supplied to each of the heaters is calculated as $P_{el,i} = V_i I_i$. The total power supplied to the background heaters, $P_{el,BG}$, is then calculated by summing the power to each of the zones. The net heat input is calculated by subtracting the heat loss from the supplied electrical power, $Q_{net} = P_{el,BG} - Q_{loss}$. The base heat flux, q''_{base}, is calculated by dividing the net heat input by the base footprint area, A_b; similarly, the wall heat flux, q''_{wet}, is calculated by dividing the net heat input by the total channel wetted area $(A_{wet,tot} = N_c N_{sink} A_{wet})$.

The fluid thermodynamic quality at the channel outlet is calculated by:

$$x_{out} = \frac{Q_{net} - \dot{m} c_p \left(T_{sat,out} - T_{fl,in}\right)}{\dot{m} h_{LV}} \quad (1)$$

where the latent heat of vaporization is evaluated at the saturation temperature based on the outlet pressure. The effective overall thermal resistance, which represents an effective resistance that includes the caloric resistance of the fluid, conduction resistance through the microchannel base, and resistance due to convection at the channel walls, is calculated based on the base area and the average chip temperature rise above the fluid inlet temperature:

$$R''_{th} = \frac{\left(T_{chip,avg} - T_{fl,in}\right)}{q''_{base}}. \quad (2)$$

The contribution of conduction and caloric resistances to the total resistance is calculated using:

$$R''_{cond} + R''_{fluid} = \left(\frac{d_w - d_c}{k_{Si}} + \frac{d_{SiO_2}}{k_{SiO_2}}\right) + \frac{A_{base}}{2\dot{m} c_p} \quad (3)$$

The heat transfer coefficient, which is a measure of the convective heat transfer at the channel walls, is estimated using the channel wetted area and the difference between the average temperature at the channel base and average fluid temperature:

$$h_{wet} = \frac{q''_{wet}}{\eta_o \left(T_{base,avg} - T_{fl,ref} \right)}, \tag{4}$$

For heat fluxes at which $x_{out} \le 0$, $T_{fl,ref}$ is the average fluid temperature in the heat sink. For $x_{out} > 0$, the location where the saturation temperature is reached, z_{sat}, is estimated using an energy balance; the fluid temperature is assumed to increase linearly up to the local saturation temperature at z_{sat} and decrease as the local pressure decreases along the remaining length of the channel. For this calculation, the pressure drop in the channel is assumed to be linear throughout and the heat flux is uniform along the length of the channel. The reference temperature is calculated by taking a length-weighted average of these temperatures:

$$T_{ref} = \begin{cases} \dfrac{T_{fl,in} + T_{fl,out}}{2} & , if \ x_{out} \le 0 \\ \left(\dfrac{T_{fl,in} + T_{sat,x_{sat}}}{2} \right) \dfrac{z_{sat}}{L_c} + \left(\dfrac{T_{sat,x_{sat}} + T_{sat,out}}{2} \right) \dfrac{\left(L_c - z_{sat} \right)}{L_c} & , if \ x_{out} > 0 \end{cases} \tag{5}$$

The temperature at the base of the channels is calculated assuming 1D conduction across the silicon base and silicon dioxide insulation layer:

$$T_{base,avg} = T_{chip,avg} - q''_{base} \left(\frac{\left(d_w - d_c \right)}{k_{Si}} + \frac{d_{SiO_2}}{k_{SiO_2}} \right) \tag{6}$$

The overall surface efficiency is defined as:

$$\eta_0 = 1 - \frac{NA_f}{A_{wet}} \left(1 - \eta_f \right), \tag{7}$$

where the fin efficiency is defined as:

$$\eta_f = \frac{\tanh(md_c)}{md_c}, \text{ where } m = \sqrt{\frac{2h_{wall}}{k_{Si}w_f}}. \tag{8}$$

The heat transfer coefficient is first solved assuming a fin efficiency of unity; fin efficiency is then iterated until the calculated heat transfer coefficient value converged.

The total power supplied to the hotspot is calculated using $P_{el,HS} = V_{HS}I_{HS}$. Due to the relatively long lead wires and the low resistance of the hotspot heater, a significant portion of the supplied power is dissipated in the lead wires. Prior to testing, the electrical resistance of the hotspot heater, excluding the lead wires, is measured using a probe station (4200-SCS, Keithley); the combined resistance of the hotspot heater, lead wires, wire bonds, and PCB traces is then measured using the same method. The net heat input into the hotspot heater is calculated using $Q_{HS} = \left(R_{HS,heater}/R_{HS,tot}\right)P_{el,HS}$.

The temperature of the hotspot heater is determined *a posteriori* by calibrating the hotspot heater resistance as a function of temperature using the RTDs adjacent to the heater as a reference under uniform heating conditions under which it can be assumed that all of these resistors are at the same temperature. The hotspot heater resistance is estimated at each background heating level for which hotspot heating tests are performed (because electrical resistance of the hotspot heater cannot be determined while the hotspot heater is not powered, its resistance is estimated by extrapolating the measured resistances to a hotspot heat flux of zero). A linear regression is fitted to these resistances as a function of chip temperature and is used to determine the hotspot temperature.

4.5 Uncertainty

The measurement uncertainties of each instrument in the experimental test facility are obtained from the manufacturers' specifications sheets and are listed in Ref. [22]. In the case of the custom RTDs, the uncertainty for the chip temperatures (±1 °C) are conservatively estimated using the accuracy of the reference RTD used for the calibration, the linearity of the sensor calibration, and the repeatability of the sensors over time. The uncertainties of calculated values are determined using the method outlined in Ref. [33]. The uncertainty in the stated heat flux is calculated to be ±2%, while uncertainty in effective thermal resistance and heat transfer coefficient are ±4 to 12% and ±8 to 17%, respectively. The maximum uncertainties in both thermal resistance and heat transfer coefficient occur at low heat fluxes where uncertainties in chip temperature rise are largest.

5. Results and discussion

5.1 Uniform background heat flux

5.1.1 Effect of channel mass flux

Figure 8 shows the steady-state base heat flux as a function of average chip temperature for Sample 33×470 (channel width × channel depth: 33 μm × 470 μm, Table 1) at three mass fluxes. Single-phase fluid is delivered to the channels at 59 °C (~6 °C subcooling based on the outlet pressure). At low heat fluxes (up to 275 W/cm² for a mass flux of 2100 kg/m²s), the heat input is insufficient for the fluid to reach the saturation temperature, so the fluid remains as single-phase liquid throughout the channels. In this low-heat-flux region (shown with open symbols in Figure 8), chip temperatures increase linearly with heat flux for all mass fluxes, as is characteristic

of single-phase flow. For a fixed heat flux in the single-phase region, the chip temperature decreases with increasing mass flux. The heat input required to transition from single-phase to two-phase operation increases with mass flux due to the increased sensible heat necessary to reach the saturation temperature; this increase in required heat input for transition is characteristic of two-phase systems [34]. At sufficiently large heat inputs, boiling is initiated, which results in a slight increase in the slope of the curve. While no optical access was available to visually observe the flow in the channels, the outlet fluid in the manifold is visually monitored for the presence of vapor; for all three mass fluxes, vapor is observed at the heat flux where the increase in slope of the curve is also seen. The onset of boiling is often accompanied by a sharp drop in the wall temperature in systems containing straight, parallel microchannels [35]; this behavior is not seen in Figure 8 due to the large number of parallel channels, each of which exhibits boiling at a slightly different heat flux. This trend is explained further in Ref. [22] where the spatial temperature distribution is discussed in detail for the same heat sink system. As heat fluxes are increased further within the two-phase regime, the chip temperature rises in a relatively linear manner, with higher mass fluxes resulting in higher slopes. Up to a heat flux of ~500 W/cm^2, the chip temperatures do not show a noticeable dependence on mass flux; at heat fluxes beyond this value, the curves for the different mass fluxes deviate. It is observed that the chip temperature for the lowest mass flux (600 kg/m^{2}s) increases more rapidly with heat flux than at higher mass fluxes. The maximum heat flux dissipated also increases with mass flux, with a maximum of 1020 W/cm^2 dissipated at a mass flux of 2100 kg/m^{2}s and an average chip temperature of 127 °C. It is worth noting that this particular experiment was allowed to operate at a higher chip temperature than the cutoff to demonstrate the ability to dissipate high heat fluxes.

Figure 9(a) shows heat transfer coefficient as a function of exit thermodynamic quality for Sample 33×470. In the single-phase region, the heat transfer coefficient is relatively constant for a given mass flux and increases with increasing mass flux. This increase indicates the importance of developing flow and jet impingement effects in manifold microchannels; these effects have been shown in numerical models [12] and in experimental testing of manifold microchannels with smaller channel widths [22]. For all three mass fluxes, boiling is initiated at heat fluxes where the exit thermodynamic quality is less than zero, signifying subcooled boiling; while the bulk mean fluid temperature at the channel outlet is lower than the saturation temperature, local fluid temperatures near the wall can reach a superheat that causes bubble nucleation. As with the heat transfer coefficients in the single-phase region, the two-phase heat transfer coefficients also increase with mass flux for a given exit quality. For flow boiling in traditional microchannels, the nucleate boiling contribution to heat transfer has been shown to be largely unaffected by mass flux, whereas the convective transport is strongly affected by mass flux [35]. In the current work, the heat transfer coefficient is a function of mass flux for a given exit quality, which indicates that both nucleate boiling and convection transport mechanisms are significant [36]. Figure 9(a) shows that heat transfer coefficients begin to decrease at lower exit qualities for higher mass fluxes. Critical heat flux correlations that were developed for flow boiling in straight, parallel microchannels predict that the thermodynamic quality at critical heat flux decreases with increasing mass flux [37]. The decrease in heat transfer coefficient at high heat fluxes occurs due to intermittent dryout at the channel walls and has been shown to correspond to the suppression of bubble nucleation at the channel wall in microchannel systems [7,35,38].

The effective thermal resistance as a function of base heat flux is shown in Figure 9(b) for Sample 35×470; the plotted points show the total thermal resistance (Equation (2)), while the horizontal, dashed lines represent the sum of conduction and caloric thermal resistances (Equation(3)) at the three different mass fluxes considered. The horizontal lines define the minimum possible thermal resistance, in the absence of any convective thermal resistance, given the base thickness, base material, fluid, and fluid mass flux. The single-phase thermal resistance (open data points) decreases with increasing mass flux, which correlates to the corresponding increase in heat transfer coefficient in Figure 9(b). For a fixed mass flux, thermal resistance decreases significantly from single-phase to two-phase operation (closed data points), especially at low mass fluxes for which the single-phase thermal resistance is relatively large. At these low thermal resistances in the two-phase regime, the conduction and caloric resistances contribute significantly to the overall thermal resistance; for example, at a mass flux of 2100 kg/m²s, the conduction and caloric resistances together contribute 34% of the total thermal resistance at the minimum thermal resistance (2.20×10^{-6} m²K/W of 6.46×10^{-6} m²K/W). Because the thermal resistance includes significant contributions from resistances other than convection resistance, the decrease in thermal resistance is muted even for relatively large increases in heat transfer coefficient. For example, increasing the mass flux from 600 kg/m²s to 2100 kg/m²s increases the maximum heat transfer coefficient by 32% (32.4×10^{6} m²K/W to 42.8×10^{6} m²K/W), while the minimum thermal resistance only decreases by 15% (7.62×10^{-3} m²K/W to 6.46×10^{-3} m²K/W).

5.1.2 Effect of channel geometry

Figure 10(a) shows the base heat flux dissipated as a function of the average chip base temperature increase above the fluid inlet temperature for a mass flux of 2100 kg/m²s, for all the

channel geometries listed in Table 1. For a fixed channel width, the maximum base heat flux dissipated increases with channel depth; both heat transfer area and fluid flow rate increase with increasing channel depth, which allow for the dissipation of higher base heat fluxes. For a fixed aspect ratio (*viz*, Samples 15×150 and 33×300, $AR \approx 10$), the sample with the smaller hydraulic diameter (Sample 15×150) is able to dissipate a higher maximum base heat flux (618 W/cm² compared to 494 W/cm²). These samples have similar wetted areas and Sample 33×300 has over twice the flow rate as Samples 15×150. For traditional microchannel heat sinks, this increase in flow rate would result in a higher base heat flux , where critical heat flux is largely dependent on fluid quality [37]. The effect of channel diameter on critical heat flux is not agreed upon for conventional microchannels [39], but the critical heat flux increases with increasing hydraulic diameter for the manifold microchannels tested in this study. For a fixed channel depth (Samples 15×300 and 33×300, $d_c \approx 300$), the sample with thinner channels dissipates a 77% higher maximum heat flux (874 W/cm²) than the sample with wider channels (494 W/cm²). This can largely be attributed to the 86% increase in wetted area due to the decrease in fin pitch for the thinner channels.

Figure 10(b) shows the wall heat flux, which is calculated based on the wetted area, dissipated as a function of the average chip temperature increase above the fluid reference temperature. For a fixed wall heat flux and channel width, chip temperature rise increases with increasing channel depth; the samples with the highest aspect ratio at each channel width exhibit significantly higher temperature rises for a given wall heat flux. For a fixed channel depth, Samples 15×300 and 33×300 ($d_c \approx 300$) achieve similar maximum wall heat fluxes, with Sample 15×300 having a higher temperature rise at any given wall heat flux. This behavior is in contrast to the

observation in the literature for larger channel widths (100-1000 μm) in traditional microchannels that decreasing the channel width decreases chip temperature rise for a fixed channel depth [40]. Experimental data are not available for small-diameter, high-aspect-ratio channels similar to those used in this work; however, all available trends in the literature indicate lower temperature rises for thinner channels, contrary to the observation in the current work. The increase in temperature rise with decreasing width seen here can be attributed to the decrease in impingement effects and decrease in flow rate in the lower portion of the deep channels, which are caused by the increased flow resistance in the direction normal to the channel [22]. In traditional, low-aspect-ratio microchannels with larger hydraulic diameters (400-1000 μm), wall superheat has been shown to be largely independent of hydraulic diameter [40]; smaller hydraulic diameter channels (<400 μm) were shown to have lower wall superheats at low wall fluxes, but reached critical heat flux at lower wall heat fluxes. These trends are not seen in the high-aspect-ratio, manifold microchannels tested in this work. For a fixed aspect ratio, Samples 15×150 and 33×300 (AR ≈ 10) show similar temperature rises to each other until wall heat fluxes of ~50 W/cm^2, above which Sample 33×300 experiences large temperature rises.

Heat transfer coefficient as a function of wall heat flux is plotted in Figure 11(a). In the single-phase region, the heat transfer coefficient is relatively flat for each channel geometry. Upon boiling incipience, the heat transfer coefficient increases significantly and continues to rise as boiling is progressively initiated in more of the channels. While the boiling curves (Figure 10(b)) were similar for Samples 33×150 and 33×300 (AR ≈10) up to wall fluxes of 50 W/cm^2, the heat transfer coefficients are much larger for Sample 33×300; this occurs due to the relatively low fin efficiency in the wide, deep channels (49-63% for Sample 33×300 compared to 86-92% for Sample

33×150). In traditional microchannel systems, two-phase heat transfer coefficient is slightly dependent on channel dimensions and strongly dependent on fluid quality: the heat transfer coefficient increases with increasing quality and decreasing channel hydraulic diameter (at low qualities) [40]. This trend is not seen in the current data where heat transfer coefficient is significantly larger for wider channels; this could be caused by the reduced flow resistance in wider channels allowing for better fluid replenishment in the lower (near the base) portions of the channel. For each sample, the heat transfer coefficient reduces sharply with heat flux after a maximum is reached, which may be caused by local/intermittent dryout at the wall [41] or flow instabilities that decrease flow to individual channels [42].

Thermal resistance as a function of base heat flux is shown in Figure 11(b). Single-phase thermal resistance shows little variation for a given channel geometry, reflecting the corresponding single-phase heat transfer coefficient trends. Thermal resistance decreases as the flow enter two-phase operation, again matching the trend in heat transfer coefficient. For a given base heat flux, Sample 15×150 has the highest thermal resistance due to its relatively small wetted area and low fluid flow rate. For all base heat fluxes, the thermal resistance of Sample 33×300 is significantly less than that of Sample 15×150, which has the same nominal wetted area and aspect ratio; this could be due to the increase in fluid flow rate for the deeper channels. For a fixed channel depth of ~300 μm (Samples 15×300 and 33×300), the sample with thinner channels has a minimum thermal resistance that is 15% lower than the sample with wider channels despite having a significantly lower heat transfer coefficient; in this situation, the increase in wetted area (Sample 15×300 has ~86% more wetted area than Sample 33×300) outweighs the decrease in the heat transfer coefficient.

5.1.3 Pressure drop

Figure 12(a) shows the pressure drop as a function of base heat flux for Sample 33×470 at three mass fluxes. The inlet and outlet pressure taps are located upstream and downstream of the manifold distributor, respectively (Figure 3(a)); therefore, this pressure drop includes contraction into and expansion out of the microchannels as well as flow splitting and contraction/expansion resistances in the manifold. During single-phase operation, the pressure drop decreases slightly with increasing heat flux due to the decrease in viscosity at elevated temperatures. In the two-phase region, pressure drop increases with heat flux since the length of the channel experiencing two-phase flow increases, as does the mixture velocity due to increase in vapor void fraction. Pressure drop during single-phase and two-phase operation increases with increasing mass flux for all base heat fluxes.

Pressure drop as a function of base heat flux for each of the samples is shown in Figure 12(b) at a mass flux of 2100 kg/m^{2}s. Generally, single-phase pressure drop increases with increasing channel depth due to increased velocities in the manifold (to maintain a constant mass flux through the channels). For example, Sample 33×300 has a larger hydraulic diameter than Sample 15×150, which would lead to a lower pressure drop in straight, parallel channels because pressure drop is inversely proportional to hydraulic diameter for a fixed flow length [43]; however, Sample 33×300 has a single-phase pressure drop ~66% larger than Sample 15×150 (49 kPa compared to 30 kPa). This different behavior for the manifold microchannel heat sink is attributed to the increased fluid flow rate for a given mass flux for deeper channels leading to increased manifold pressure drops. Because the manifold dimensions remain fixed for all channel geometries, the manifold velocities increase with increasing channel depth for a given mass flux.

For a fixed channel depth of ~300 μm, where both samples are expected to have similar manifold pressure drops, the sample with wider channels has slightly lower single-phase pressure drop due to the increase in hydraulic diameter. The slope of the pressure drop curve is slightly steeper for samples with thinner channels because the two-phase pressure gradient depends on the inverse of hydraulic diameter, which is smaller for the thinner channels. Pressure drops do not exceed 120 kPa in any of the experiments.

5.2 Simultaneous background and hotspot heat flux dissipation

Experiments were conducted with a hotspot heat flux applied over the central 200 μm × 200 μm area while simultaneously applying a uniform background heat flux over the entire 5 mm × 5 mm chip area. As mentioned in Section 4.3, the supplied power to the hotspot heater was scaled to account for electrical resistances external to the 200 μm × 200 μm heater. For the sample tested in this work, the hotspot heater resistance was measured to be 19.0 Ω and the combined resistance of the hotspot heater, lead wires, wire bonds, and PCB traces was 39.9 Ω; therefore, ~48% of the power supplied to the hotspot was dissipated external to the hotspot. All hotspot heat fluxes discussed here are based on the heat generated solely by the hotspot heater. Hotspot heat fluxes were increased from 0 to ~2,700 W/cm² at background heat fluxes of 100, 300, 500, 700, and 900 W/cm² for mass fluxes of 600, 1300, and 2100 kg/m²s using Sample 33×470 (Table 1); the corresponding heat inputs for these hotspot heat fluxes were 0 to 1.1 W. Note that all background heat fluxes are not possible for each mass flux due to chip temperature cut-off limits and that for all combinations of background and hotspot heat fluxes, the total power supplied to the hotpot heater is negligible compared to the total power of the background heating (0.4 – 5%). The minimum power to the background heaters is ~25 W (for a heat flux of 100 W/cm² over a 5 mm ×

5 mm area) and the maximum power for the hotspot heater is ~1.1 W (2,700 W/cm² over a 200 µm × 200 µm area).

Figure 13(a) shows the steady-state hotspot temperature as a function of hotspot heat flux for a fluid mass flux of 2100 kg/m²s and various background heat fluxes. The temperatures at q''_{HS} = 0 W/cm² correspond to the hotspot temperature under background heating conditions and the subsequent points show the hotspot temperature as hotspot heat flux is increased. The hotspot temperature rise increases linearly with hotspot heat flux to a constant value of 16±1 °C at the maximum hotspot heat flux (q''_{HS} = 2,700 W/cm²) for all background heat fluxes. The hotspot temperature rise for the other two mass fluxes (not shown) exhibits the same trends, with a linear temperature rise and a slope that is unaffected by background heat flux. For the background heat fluxes tested, the heat transfer coefficients are between 17×10^3 W/m²K and 43×10^3 W/m²K (Figure 11(a)), a 150% difference; this large range in heat removal rate at the backside has little effect on the measured hotspot temperature (*i.e.* the hotspot temperature rise due to hotspot heat flux generation is independent of background heat transfer coefficient and is instead dictated by the heat spreading and conduction resistances in the base).

Figure 13(b) shows the background heat flux as a function of the hotspot temperature rise above the fluid reference temperature with the hotspot heating cases overlaid on the boiling curves. Black data points represent the measured hotspot temperatures with only the background heat flux applied; blue data points represent hotspot temperatures during simultaneous hotspot and background heating conditions. The blue data points in Figure 13(b) are the same data as in Figure 13(a), now showing the relationship between hotspot temperature rise and background heat flux; since the background heat flux does not change for each case, the hotspot temperatures appear as

a horizontal line on the plot. The hotspot temperature rise resulting from the high local heat flux is significant compared to the temperature rise from uniform, background heating. The RTDs just adjacent to the hotspot heater (~200 μm from the edge of the hotspot) measure temperature rises of only 3±1 °C above the background temperature at the maximum hotspot heat flux; the RTDs across the chip surface do not increase by more than 1 °C during hotspot testing for any background heat flux and mass flux. This indicates that the temperature rise at the hotspot is extremely localized and the rest of the chip surface is largely unaffected by the high hotspot heat flux. Also, given the relatively thick base substrate (185 μm), the temperature at the channel base is expected to be relatively uniform. This allows the heat sink to operate without any significant flow maldistribution (indicated by the chip temperatures remaining relatively constant throughout hotspot testing) despite the highly localized heating of the channels directly under the hotspot.

6 Conclusions

Single-phase and two-phase thermal and hydraulic performance characteristics for a variety of hierarchical manifold microchannel heat sink arrays, each with a unique channel geometry, are presented. The test vehicle uses a hierarchical manifold to feed an array of intrachip microchannel heat sinks with high-aspect-ratio channels. A heated chip area of 5 mm × 5 mm is cooled by a 3 × 3 array of microchannel heat sinks fabricated directly into the heated die, which also covers 5 mm × 5 mm. The test vehicles have channel widths of 15 μm and 33 μm and depths between 150 μm and 470 μm; the effective flow length in any microchannel flow passage is 750 μm.

It was shown in our previous study [22] that the maximum heat flux dissipation increases with increasing channel depth and mass flux; heat transfer coefficient is largely independent of channel depth, but strongly depends on exit thermodynamic quality. In this study, the effect of channel width and aspect ratio are investigated. Heat sinks with wider channels yield higher heat transfer coefficients, but not necessarily the lowest thermal resistance. For a fixed channel depth of ~300 μm, the sample with 15-μm wide channels has a wetted area ~86% larger than the sample with 33-μm wide channels; while the heat transfer coefficient is lower for the sample with narrower channels, the increased wetted area outweighs the decrease in heat transfer rate. To investigate the effect of hydraulic diameter on thermal performance, samples with a fixed aspect ratio of ~10 and equal wetted areas were tested; the sample with a larger hydraulic diameter (Sample 33×300) provided a higher heat transfer coefficient and lower thermal resistance compared to the sample with a smaller hydraulic diameter (Sample 15×150), which is attributed to the increase in fluid flow rate to maintain a constant mass flux. In traditional two-phase microchannel heat sinks, heat transfer coefficient has been shown to be largely unaffected by channel dimensions for a given mass flux; maximum heat flux dissipation, therefore, increases with increasing wetted area (decreased fin pitch and deeper channels). The current work shows that, unlike traditional heat sinks, maximum heat flux dissipation does not necessarily increase with increasing wetted area for two-phase manifold microchannel heat sinks.

Heat fluxes up to 1020 W/cm² are dissipated at pressure drops of less than 120 kPa and measured chip-to-fluid-inlet temperature rises less than 58 °C using HFE-7100 as the working fluid and a heat sink with 33 μm × 470 μm channels. The cooling approach provides a minimum thermal resistance of 5.5×10^{-6} m²K/W at a mass flux of 2100 kg/m²s.

Hotspot heat fluxes of ~2,700 W/cm² (200 μm × 200 μm) were dissipated simultaneous with background heat fluxes up to 900 W/cm² (5 mm × 5 mm). The hotspot temperature rise was linear with hotspot heat flux for all mass fluxes and background heat fluxes; at ~2,700 W/cm², the hot spot temperature rise was 16±1 °C above the chip surface temperature.

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Figure 10. (a) Base heat flux as a function of chip temperature rise above the fluid inlet temperature and (b) wall heat flux as a function of chip temperature rise above the fluid reference temperature (Equation (5)), at a mass flux of 2100 kg/m²s.

Figure 11. (a) Heat transfer coefficient as a function of wall heat flux and (b) thermal resistance as a function of base heat flux, at a mass flux of 2100 kg/m²s.

Figure 12. (a) Pressure drop as a function of base heat flux and mass flux for Sample 33×470 and (b) pressure drop as a function of base heat flux and channel geometry at a mass flux of 2100 kg/m²s.

Figure 13. (a) Hotspot temperatures as a function of hotspot heat flux for a variety of fluid mass fluxes and background heat fluxes. (b) Hotspot temperature rise above fluid reference temperature (Equation (5)); boiling curves with black data points show hotspot temperature at zero hotspot heat flux and colored data points show hotspot temperature during hotspot testing.

Tables

Table 1. Summary of microchannel dimensions.

Sample	N_c	w_c (μm) (actual value)	d_c (μm) (actual value)	AR (-)	D_H (μm)	$A_{wet,tot}$ (mm²)	$A_{c,tot}$ (mm²)	d_{wafer} (μm)
15×150	50	15 (14.7)	150 (153)	10.4	28.8	217	2.05	300
15×300	50	15 (16.2)	300 (310)	19.1	31.7	434	4.50	385
33×300	25	33 (33.7)	300 (317)	9.4	64.6	233	4.82	390
33×400	25	33 (33.5)	400 (397)	11.9	65.5	290	6.08	500
33×470	25	33 (33.0)	470 (465)	14.0	63.0	331	6.66	650

Table 2. Summary of experimental operating conditions.

Sample	G (kg/m²s)	$\dot{V}$ (mL/min)	Re (-)
15×150	1300, 2100, 2800	160, 255, 340	96, 155, 207
15×300	1300, 2100, 2800	350, 565, 750	105, 171, 229
33×300	600, 1300, 2100	170, 375, 435	99, 216, 349
33×400	600, 1300, 2100	215, 470, 550	100, 219, 354
33×470	600, 1300, 2100	240, 515, 605	97, 211, 341

Figures

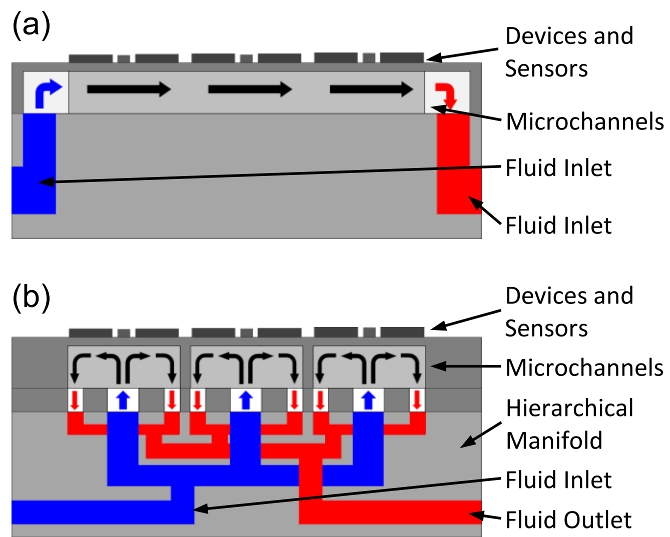

Figure 1. Cross-sectional schematic diagrams of direct cooling using (a) a traditional microchannel heat sink and (b) an intrachip hierarchical manifold microchannel heat sink design.

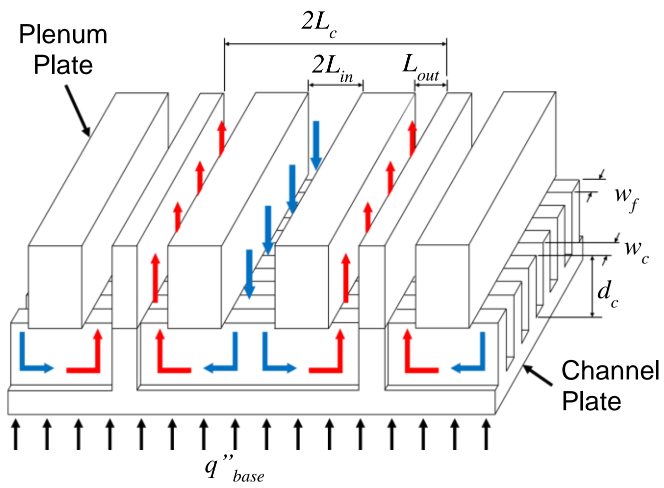

Figure 2. Schematic diagram showing the fluid flow paths and relevant dimensions in a region of the heat sink array.

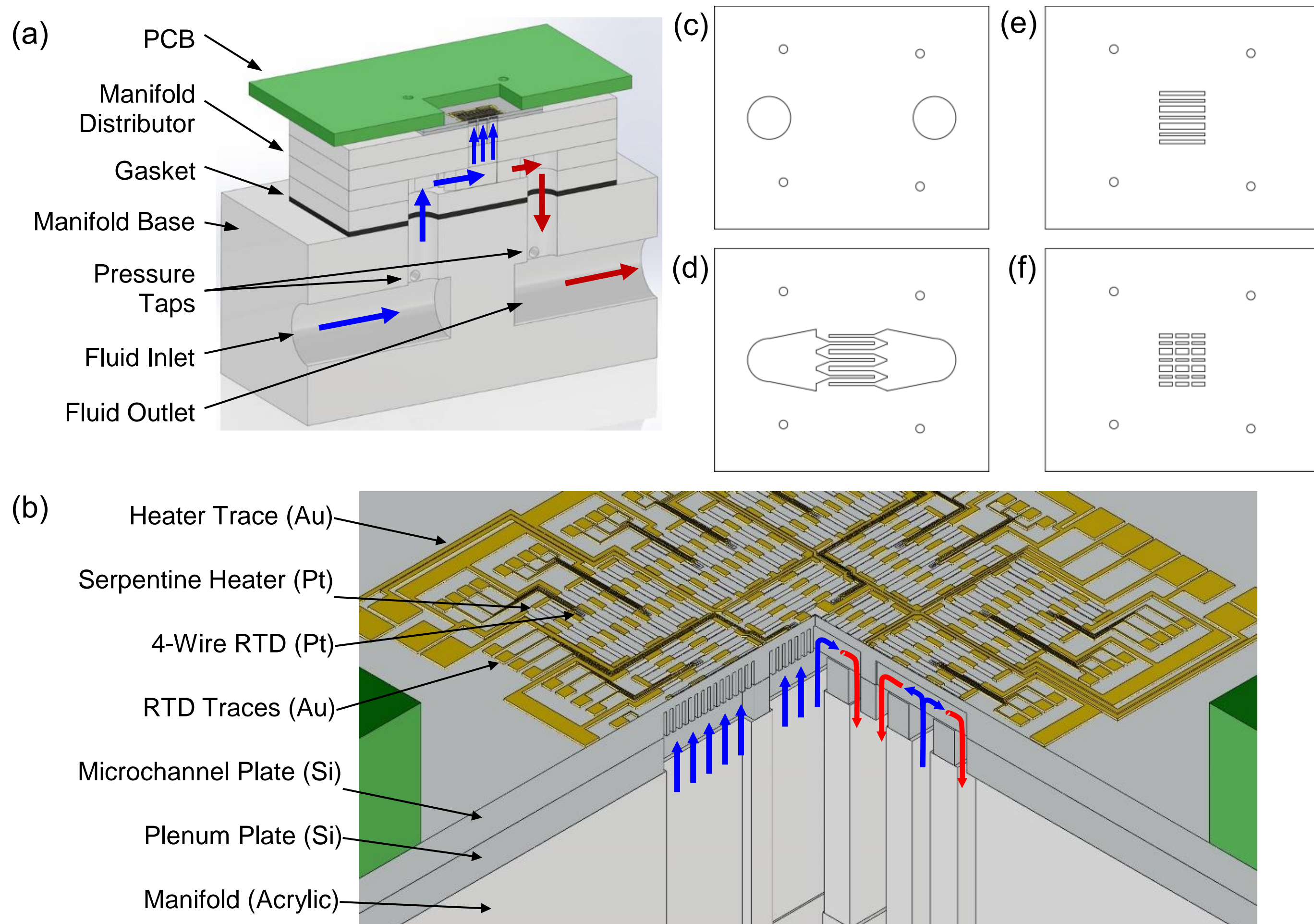

Figure 3. (a) CAD image of the test vehicle with a half-symmetry section removed and fluid inlets (blue) and outlets (red) shown; (b) zoomed-in view of the test vehicle with a quarter-symmetry section removed showing the fluid flow paths in the test chip; and (c-f) each plate level of the manifold distributor used to deliver fluid to individual heat sinks.

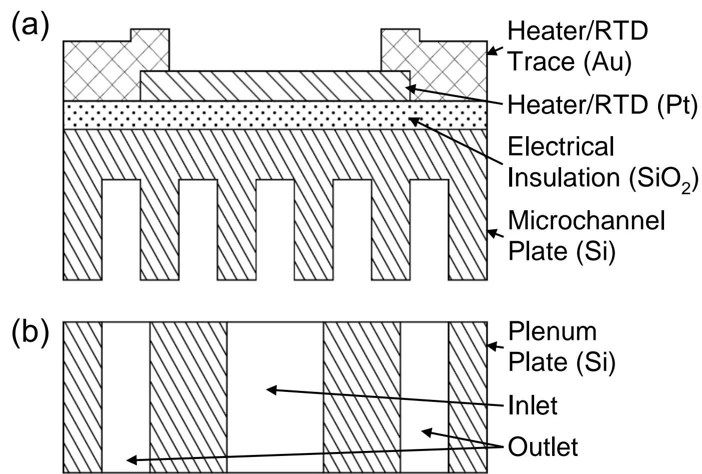

Figure 4. Cross-sectional schematic diagram of (a) the microchannel plate and (b) the plenum plate. Representative features are not drawn to scale.

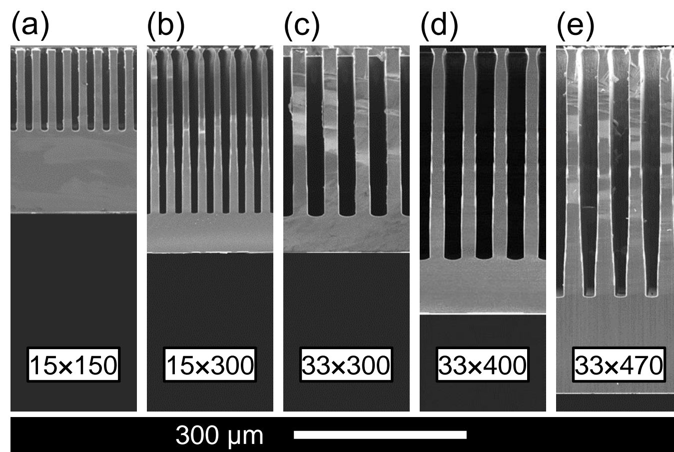

Figure 5. SEM images of the five microchannel cross-sections tested: (a) 15×150, (b) 15×300, (c) 33×300, (d) 33×400, (e) 33×470.

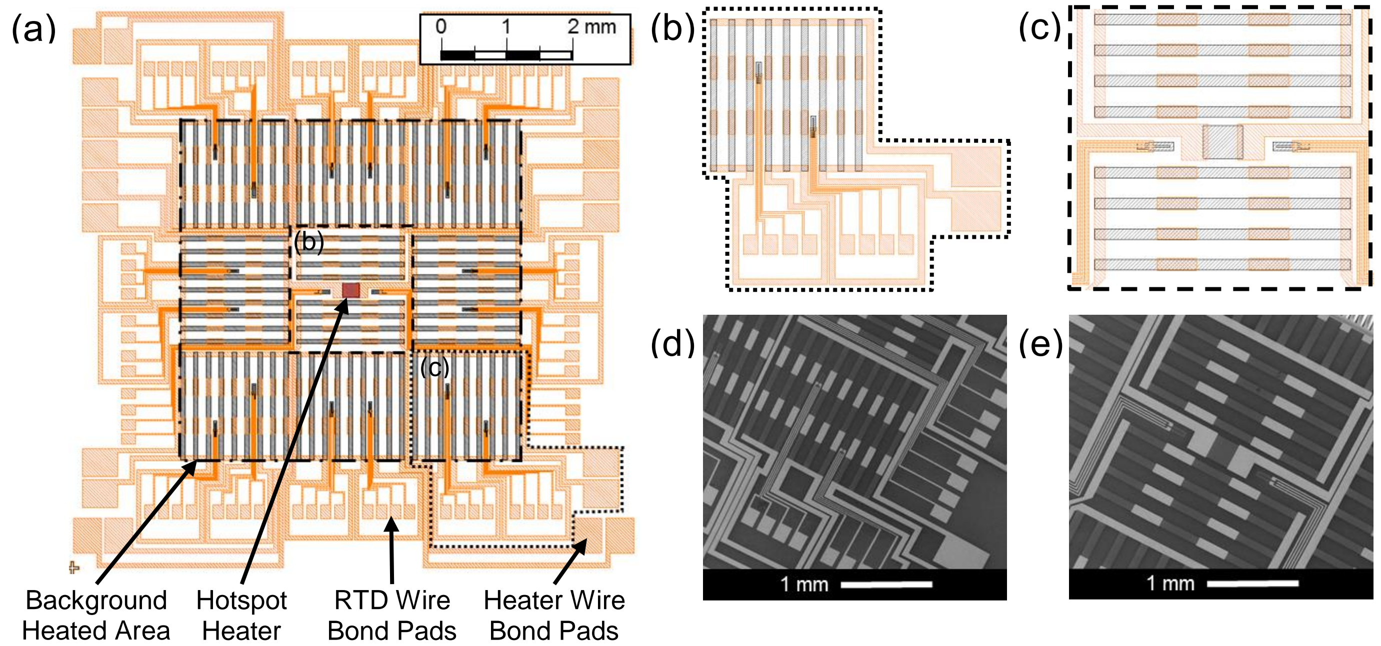

Figure 6. CAD drawing of (a) entire heater and RTD layout, (b) a background-only heater zone, and (c) the center zone with background and hotspot heaters. SEM images are shown for these same two heater zones consisting of (d) only background heaters and (e) background and hotspot heaters.

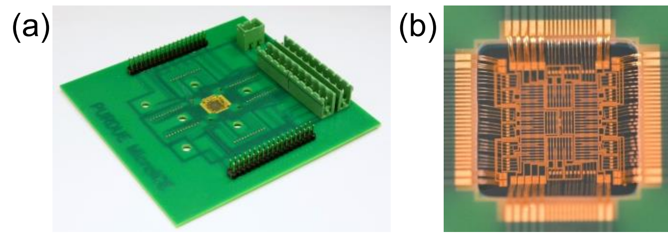

Figure 7. (a) Photograph of the test chip mounted to the PCB with heaters and sensors face up, and (b) zoomed-in view of the heaters and sensors wire-bonded to PCB contact pads.

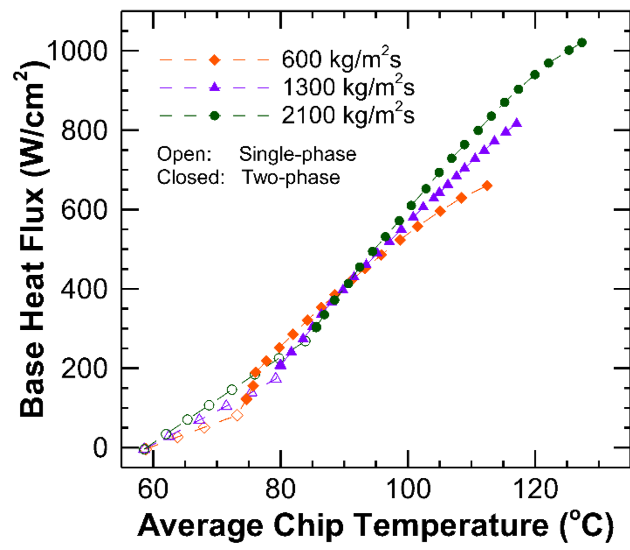

Figure 8. Base heat flux as a function of average chip temperature for Sample 33×470 at three different mass fluxes.

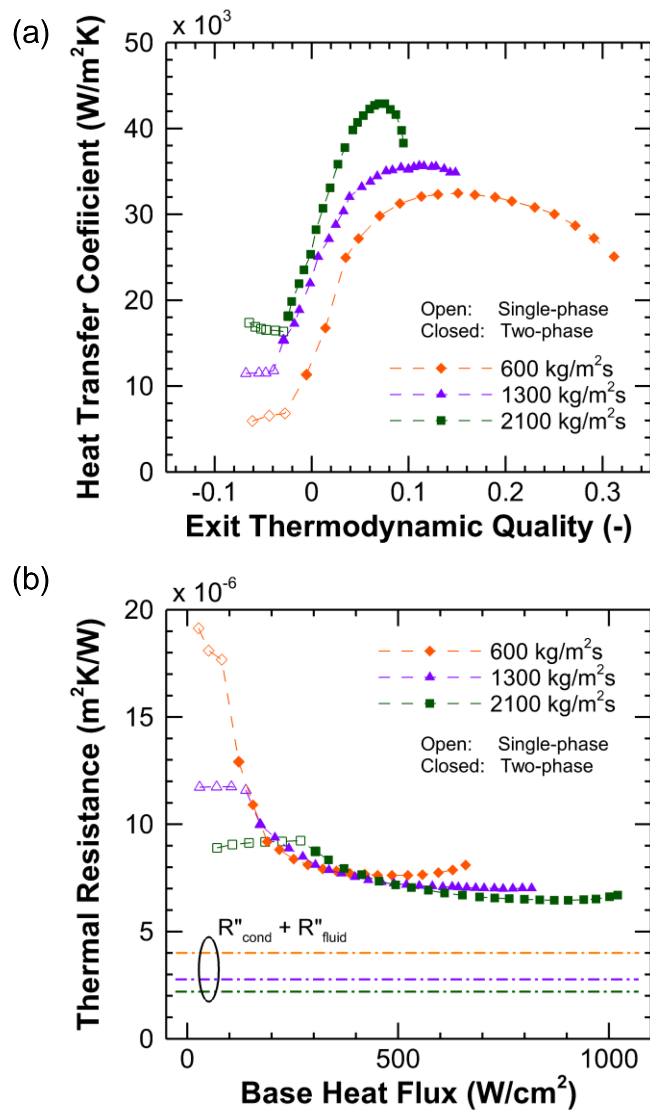

Figure 9. (a) Heat transfer coefficient as a function of exit thermodynamic quality, and (b) effective thermal resistance as a function of base heat flux for Sample 33×470 with data points showing total resistance and dashed lines showing sum of conduction and caloric resistances at the three different mass fluxes considered.

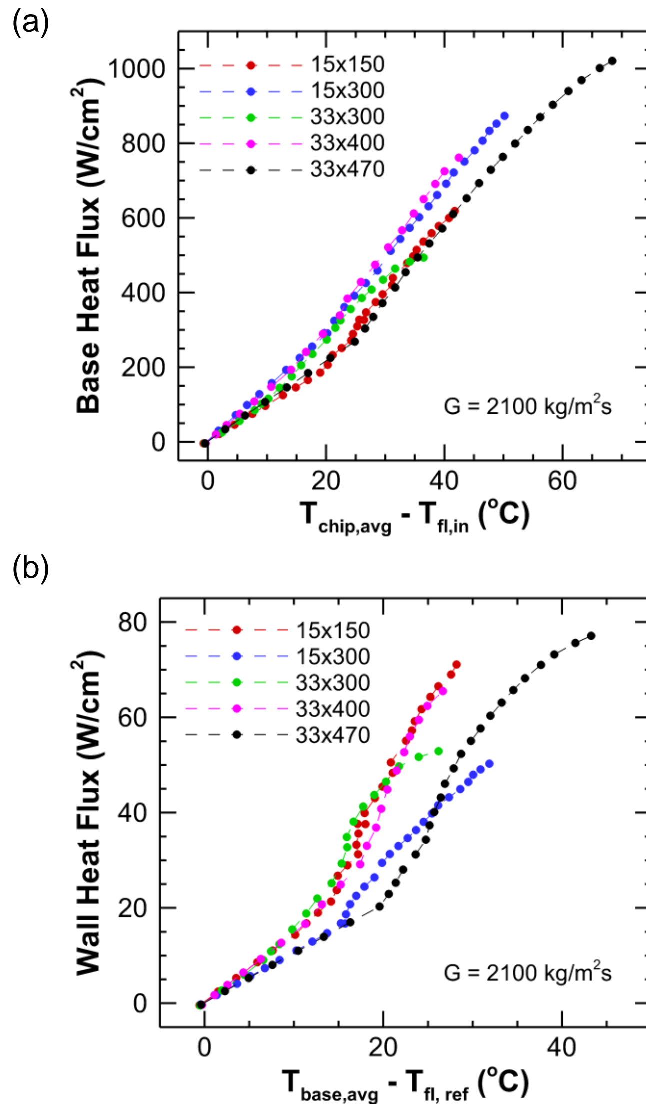

Figure 10. (a) Base heat flux as a function of chip temperature rise above the fluid inlet temperature and (b) wall heat flux as a function of chip temperature rise above the fluid reference temperature (Equation (5)), at a mass flux of 2100 kg/m²s.

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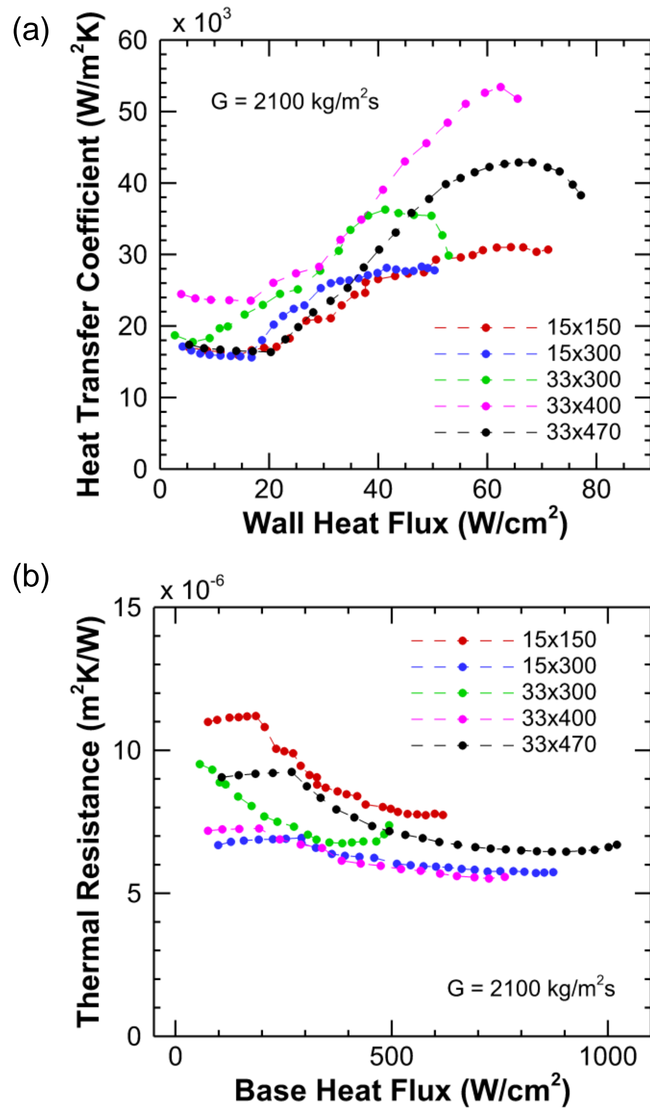

Figure 11. (a) Heat transfer coefficient as a function of wall heat flux and (b) thermal resistance as a function of base heat flux, at a mass flux of 2100 kg/m²s.

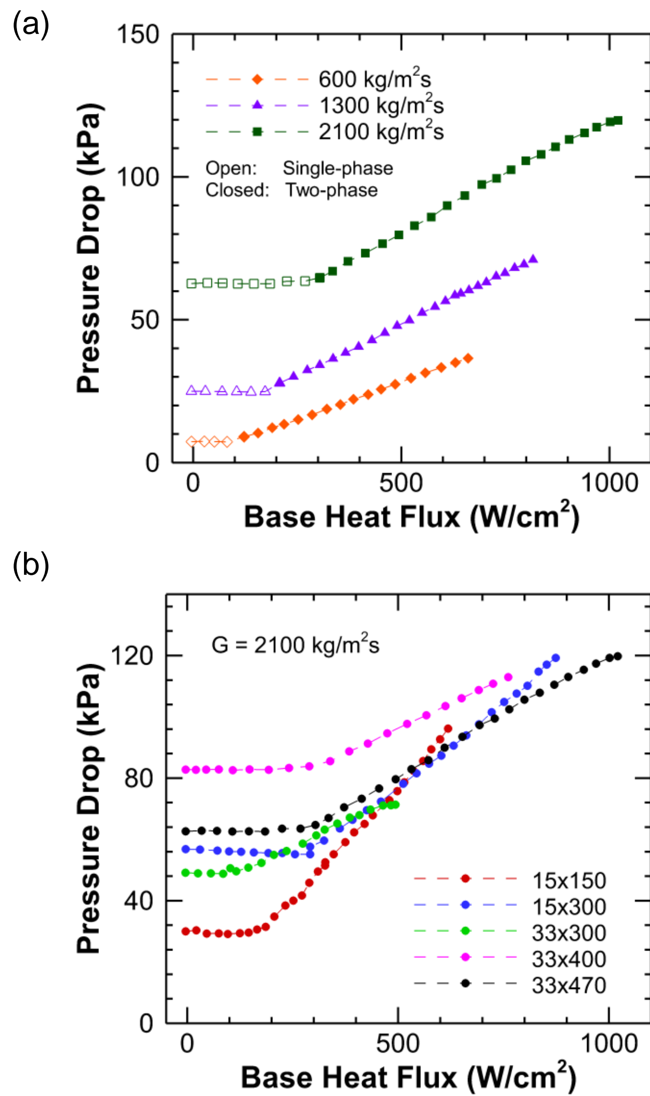

Figure 12. (a) Pressure drop as a function of base heat flux and mass flux for Sample 33×470 and (b) pressure drop as a function of base heat flux and channel geometry at a mass flux of 2100 kg/m²s.

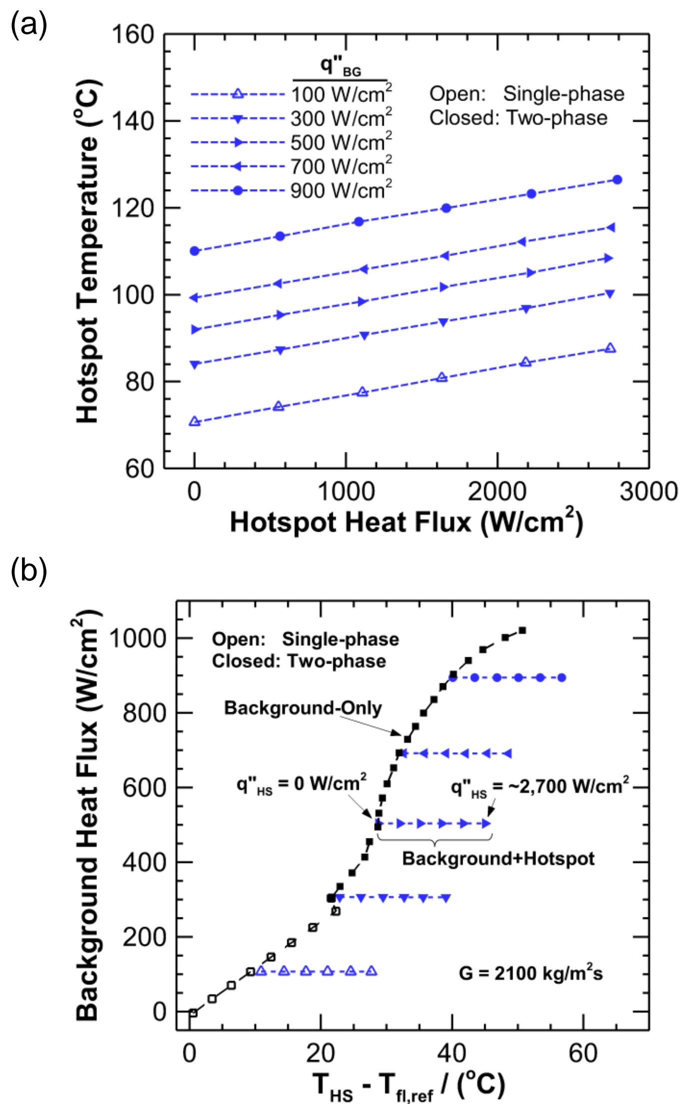

Figure 13. (a) Hotspot temperatures as a function of hotspot heat flux for a variety of fluid mass fluxes and background heat fluxes. (b) Hotspot temperature rise above fluid reference temperature (Equation (5)); boiling curves with black data points show hotspot temperature at zero hotspot heat flux and colored data points show hotspot temperature during hotspot testing.