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Integration and Testing of the Nanosatellite Optical Downlink Experiment

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ABSTRACT

Free space optical (FSO) communications have the potential to outperform traditional radio frequency data rates by orders of magnitude using comparable mass, volume, and power. The Nanosatellite Optical Downlink Experiment (NODE) is a 1.2U, 1 kg, 15 W, 1550 nm CubeSat downlink transmitter that uses a master-oscillator power amplifier configuration with a modest 1.3 mrad half-power beamwidth (HPBW) enabled by a microelectromechanical system (MEMS) Fast Steering Mirror (FSM) [1],[4]. NODE is designed to be compatible with the Portable Telescope for Lasercom (PorTeL) ground station [3],[6],[19], which has successfully demonstrated tracking of low Earth orbit objects to better than 5 arcseconds RMS.

The flight-like opto-mechanical NODE engineering model has successfully passed vibration testing at qualification levels specified by NASA GEVS [9]. The engineering model has also passed thermal testing in vacuum under worst-case expected environmental loads, and component operational temperatures remained within limits. Tests of the opto-mechanical alignment and control algorithms meet +/- 0.05 mrad (3-sigma) for the space and ground terminals. We present results from the NODE engineering unit and flight unit development, integration, and testing, as well as interface test results with PorTeL.

INTRODUCTION

Motivation

CubeSat sensor performance continues to improve, and new sensor constellations and swarms demand power-efficient, high-rate data downlinks using compact and cost-effective space and ground terminals [11]. Nanosatellite size, weight and power (SWaP) constraints can limit their ability to accommodate high-gain antennas or higher power radio systems that need to operate alongside high duty cycle payloads [1]. Larger constellations of nanosatellites and small satellites in upcoming scientific, defense, and commercial missions make it increasingly challenging to solely place the high-gain burden on the ground stations to enable downlinks of over 10 Mbps [1]. The cost to acquire, maintain, and continuously operate facilities with high-gain dish diameters from 5 to 20 meters can quickly exceed the cost of the space segment for nanosatellites. It is also becoming difficult or infeasible to obtain radio frequency licenses for CubeSats requiring significant bandwidth or for large numbers of CubeSats [4].

On April 12th of 2018, the Federal Communications Commission (FCC) has released a Notice of Proposed Rulemaking (NPRM) requesting comment on a new set of regulations regarding radio frequency licensing for small satellites. The stated purpose of these changes is to make it easier to license CubeSat and other smallsat radios through the FCC Part 25 Commercial process. However, many missions are currently licensed through the FFC's Experimental and Amateur rules. The FCC points out in the NPRM that many smallsat missions are increasingly commercial endeavors and thus should not be licensed under those rules indicating that the FCC may seek to require some or all CubeSat missions to be licensed under Commercial rules in the future. Even with the streamlined process proposed in the NPRM, Commercial licensing will be more difficult in terms of cost, approval time, and required documentation than the Experimental and Amateur paths [15]. For free space optical communications, the infrared (IR) and visible bands is not currently subject to regulation except for safety purposes, although coordination with the Laser Clearinghouse is recommended.

The Nanosatellite Optical Downlink Experiment (NODE) and the Portable Telescope for Lasercom (PorTeL) are a university effort from the Space, Telecommunications, Astronomy and Radiation (STAR) Laboratory at the Massachusetts Institute of Technology. The objective of NODE and PorTeL is to demonstrate a complete, CubeSat-scale optical communication solution using easily accessible, commercial-off-the-shelf (COTS) components and amateur telescope hardware.

In this work, we give a brief overview of the NODE payload and its PorTEL ground station in the Introduction; we present updates on current status of and results from vibration and thermal testing [9] in the Payload Testing and Results section.

The Nanosatellite Optical Downlink Experiment

The goal for the initial NODE demonstration is to present a competitive solution with greater than 10 Mbps downlink data rate, using a system approach designed to be scalable to Gbps at costs compatible with developing large nanosatellite constellations and swarms for high-bandwidth distributed sensors [1]. The transmitter payload will also demonstrate use of built-in self-testing and data from fast steering mirror (FSM) feedback to characterize payload performance [1]. NODE will demonstrate a direct-detect architecture, using a FSM to improve coarse bus pointing. NODE uses acquisition of an uplink beacon to supplement bus pointing knowledge for pointing, acquisition, and tracking (PAT) of the ground station [1]. The NODE payload (Fig. 1a) is designed to be compatible with a modest cost and performance, standard 3U CubeSat (10 cm x 10 cm x 30 cm) operating in LEO. The low-SWaP downlink terminal has a 1550-nm optical beam that is modulated with M-ary Pulse Position Modulation (PPM), to support rate-scalable data transmission [1], [14], (e.g. rates greater than 40 Mbps to a 1 m terminal or 10 Mbps to a 30-cm terminal), and is designed to accommodate bus pointing error less than +/- 3° [10], [18].

The NODE payload supports bus pointing error within +/- 3° open-loop and is limited by the beacon field-of-view [11]. For the host bus to track the ground station, slew rates of up to 1.1°/s must be supported for LEO satellites at 400 km. Required slew rates are lower for higher altitudes (e.g., 0.72°/s for a 600 km orbit). Disturbance models, incorporating feedback signal delay and lag between the beacon and feedback signal samples, estimate the body pointing error to be 0.0225°/sec (3-sigma) [18].

The first-generation NODE pointing and tracking system is designed to use a 976 nm uplink beacon from the ground station. Other experiments at MIT have demonstrated that it may be possible to replace the laser uplink beacon with a visible or infrared LED beacon in future generations [5], [16]. MIT has built and tested the visible LED uplink beacon with an orbiting CubeSat, and has built and characterized an infrared LED beacon [5]. Key NODE terminal specifications and other architectural development notes are captured in Table 1.

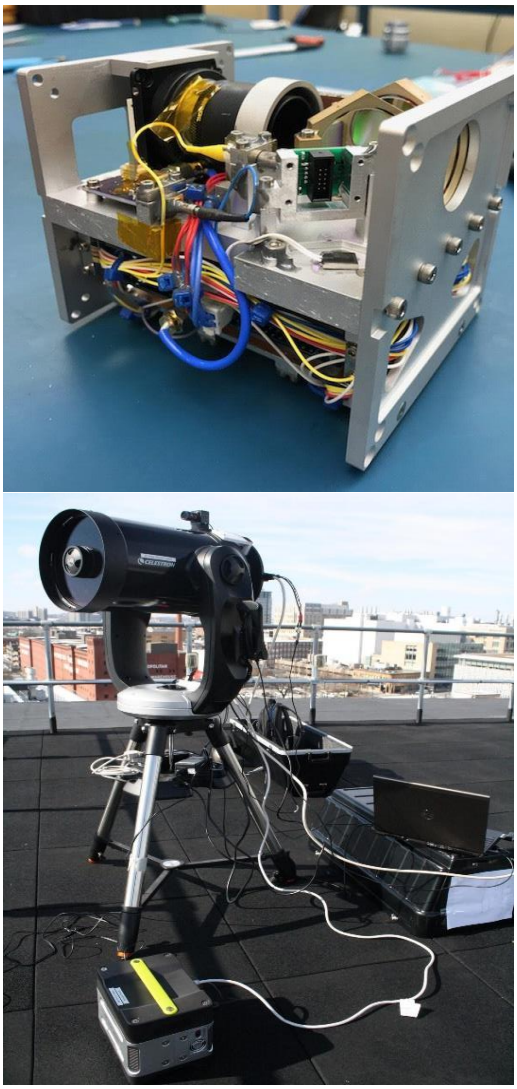
Table 1: NODE terminal specifications, version 2018-06-12.

Application	Low-cost, compact lasercom transmitter suitable for constellations and swarms.
Approach	Direct detection master oscillator power amplifier (MOPA) with downlink at 1550 nm and uplink beacon at 976 nm.
Size	Mass < 1.0 kg, Volume < 1.2 U (96 mm x 96 mm x 119 mm)
Power Interface	0.2 W (average transmit power), < 15 W (consumed power). Requires 5V (3A, 25 mVpp ripple) and 3.3V (3A, 25 mVpp ripple) from bus.
Mechanical Interface	Alignment of beacon camera boresight to within ~0.05° of reference datum.
Data Interface	USB 1.1 from Bus to NODE CPU (compatible also with USB 2.0 full speed, 12 Mbps). NODE uses own Spartan 6 FPGA. NODE has 4 GB EEPROM and 1GB RAM (of which 2GB EEPROM and 512MB RAM are available). Bus turns on/off. Bus sends file with command script. Bus receives log file with telemetry data. CPU also has possible master mode with USB 2.0 high speed, 480 Mbps.
Attitude Control	Desired bus coarse pointing: accuracy: +/- 0.15° (3-sigma), stability +/- 0.0225 °/s (3-sigma). With desired pointing performance (open loop) Allotted worst case bus pointing (fine stage throw): +/- 3° (beacon FOV). Near worst case pointing, NODE may need to generate commands for the bus attitude control system in closed loop using the beacon signal. Validation of pointing accuracy: 20 urad bias tracking error with +/- 31.5 urad (3-sigma) precision.
Beacon Camera	FOV: +/- 5.4° (10.8° full angle) Detector: mvBlueFOX-MLC205wG, Aptina MT9P, 2592 x 1944 pixels, 1/2.5" sensor size, 2.2 um x 2.2 um pixel size, 5.8 frame rate, CMOS
Beamwidth	NODE: 1.3 mrad half power (first generation, initial demo).
Downlink Data Rates	10 Mbps, initial demo to COTS 30 cm diameter amateur telescope, MIT PorTeL 100 Mbps (to a 1-m diameter aperture)
Signal	PPM4 to PPM128, RS(255,239), 8 bits per symbol
Commercializ-ation	Generation 2: 0.2 mrad beamwidth, 0.5 W transmitter, 400 Mbps to 1-m diameter telescope Generation 3: < 0.2 mrad beamwidth, 3 W transmitter, 1 m diameter telescope, possible OOK at 1064 nm with different amplifier, > 1 Gbps

Portable Optical Ground Station

Optical ground stations available for laser communications space experiments and operational use are currently limited [6]. New ground station networks are being developed; however, it is unclear whether they will be suitable for CubeSat research projects or large-scale CubeSat constellations [6], [19], [21]. A large number of low-cost, rapidly deployable laser communication ground stations can help overcome unavailability due to weather. Current optical communications ground stations typically require significant infrastructure. The objective of the Portable Telescope for Lasercom (PorTeL) is to provide a low-cost, optical ground station that is easily deployable and capable of enabling widespread access to lasercom. PorTeL uses a 28 cm amateur astronomy telescope and is able to track LEO objects to better than 5 arcsec RMS using COTS components [3].

The PorTeL telescope utilizes a novel calibration algorithm that accomplishes rapid, auto-alignment through use of a star tracker [6]. The calibration approach is quaternion-based and is unique in that it is agnostic to initial instrument orientation, capable of autonomous rapid star identification, and can maintain the accuracy of professional software [3]. PorTeL has demonstrated blind pointing accuracy of 60 arcseconds RMS, with ability to actively track LEO objects to better than 5 arcseconds RMS using only two-line element sets [6]. It is also designed to support a direct detection receiver at NODE's 1550 nm transmission wavelength [3], [6]. The PorTeL system design, algorithms, and performance metrics have been validated in Riesing, 2018 [6], [20].



Figures 1a (top) and 1b (bottom). NODE Engineering Model and the Portable Telescope for Lasercom, respectively. Image Credit: Derek Barnes and Cadence Payne

Downlink Budget

Table 2 displays a representative link budget for a downlink between the NODE space terminal and the PorTeL ground terminal. These are conservative estimates and follow the deterministic analysis and measurements done by Kingsbury [14], and secondary analysis done by Clements [1]. Nominal operations use PPM-16, PPM-32, PPM-64, and PPM-128 with a fixed slot width of 5 ns to enable variable data rates [1]. The parameters listed in Table 2 reflect the COTS components chosen for each architecture (see Notes column in Table 2 for justification).

Table 2 NODE Optical Link Analysis. Link analysis results from Clements 2018 [19].

Key Input Parameters	Value	Units	Notes
Channel Data Rate	11	Mbps	Variable
Slot width	5	ns	Fixed
PPM Order	128	-	Variable
Laser Transmitter			
Average Optical Output Power	0.20	W	Average-power limited EDFA
Laser Wavelength	1550	nm	
Extinction Ratio	42	dB	Kingsbury measurement [14]
Full-Width Half-Max	2.26	mrad	Collimator
Transmit Optical Losses	-1.5	dB	0.3 dB per planned splice
Channel			
Atmospheric Loss	-1.0	dB	
Pointing Loss	-3.0	dB	Worst case, half angle of beam
Receive Telescope & Optics			
Focal Length	2.8	m	Telescope specification [23]
Receiver Aperture Diameter	30	cm	Telescope specification [23]
Receive Optics Losses	-2.0	dB	Beam splitter
Background Noise			
Sky Spectral Radiance	6.0E-04	W/ cm^2*SR*μm	Based on Hemmati [13]
Optical Filter Bandwidth	1	nm	
Receiver Electronics			
APD Gain	20	-	
Responsivity	1.0	A/W	Kingsbury measurement [14]
Excess Noise Factor	4.3	-	Kingsbury measurement [14]
Noise Equivalent Power	2.8E-09	W	Kingsbury APD specification [14]
Noise Equivalent Bandwidth	3.0E+08	Hz	Greater than signal bandwidth [14]
Link Budget Summary			
Laser Avg. Optical Power	-7.0	dBW	
Transmit Optical Losses	-1.5	dB	
Transmit Antenna Gain	64.96	dBi	
Pointing Loss	-3.0	dB	
Path Loss at 1000 km	-258.2	dB	
Atmospheric Loss	-1.0	dB	
Receive Antenna Gain	115.7	dB	
Receive Optical Losses	-2.0	dB	
Receive Implementation Loss	-3.0	dB	
Signal Power at Detector	-89.03	dBW	
Signal Power Req'd, 1E-4 BER	-92.79	dBW	
Receiver Sensitivity	339	Photons per Bit	
Margin at 1000 km	**3.78**	**dB**	Nominal Operations

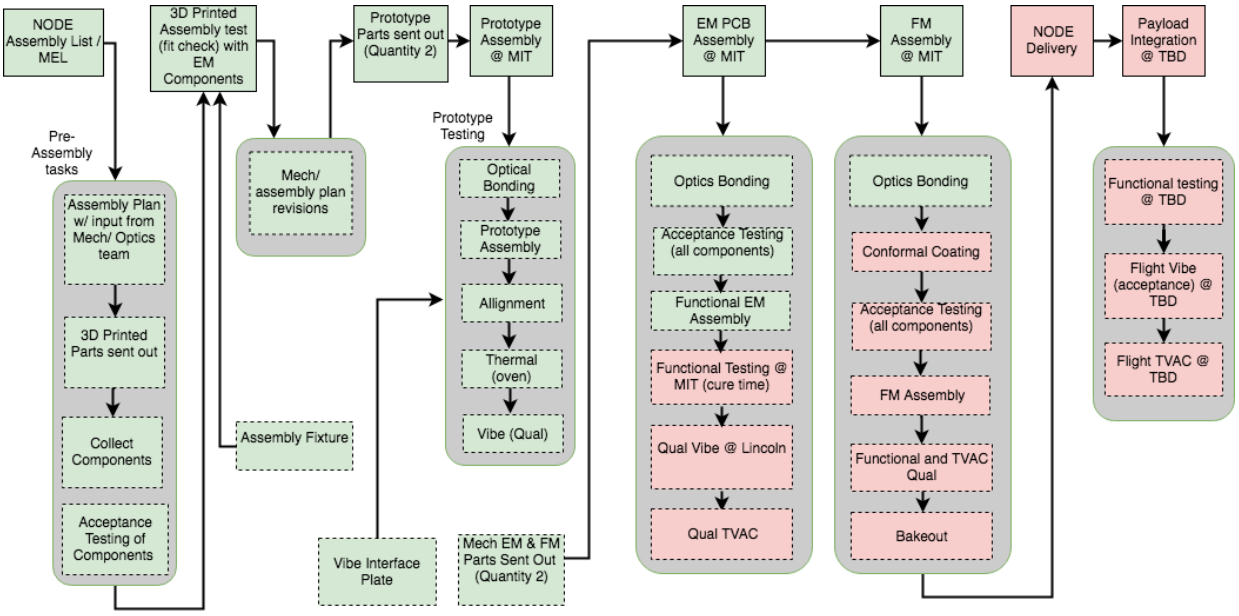


Figure 2. Overview of the NODE Integration and Testing procedure

NODE PAYLOAD TESTING METHODOLOGY AND RESULTS

Vibration Testing

The NODE payload structural design goals include surviving expected loads induced by the payload's surrounding environment, ability to integrate with the host spacecraft, and ability to establish and maintain optical alignment within ~0.05 deg of reference datum. These design requirements were achieved through kinematic design, interface control/definition, and material selection [10].

To validate the structural integrity of the payload design and determine the first resonant frequency, the NODE prototype was subjected to vibration testing at a Lincoln Laboratory facility in November 2017.

Finite Element Analysis (FEA) was performed on the payload prototype model to determine NODE's first resonant frequency. This analysis identifies locations in the model with low fundamental frequencies and is used to help determine the placement of accelerometers during vibration testing.

Table 3. Generalized random vibration test levels for components weighing 22.7 kg or less specified by NASA GEVS [9]. The NODE prototype was tested to qualification levels.

Frequency (Hz)	ASD Level (g^2/Hz)	
	Qualification	Acceptance
20	0.026	0.013
20-50	+6 dB/oct	+ 6 dB/oct
50-800	0.16	0.08
800-2000	-6 dB/oct	-6 dB/oct
2000	0.026	0.013
Overall	14.1 G_{rms}	10.0 G_{rms}

Figure 3 shows a Solidworks model of the NODE structural Finite Element Mesh used for FEA. Aluminum components are pictured in gray and PCBs in purple. Optics and other components, such as PCB-mounted components, are excluded from the mesh model due to their small mass contributing negligible effects to model results [10]. The green arrows show boundary conditions,

which are assumed to be the location of mounting interfaces with the host spacecraft [10]. FEA was performed with the assumption of a "direct mounting" configuration [10].

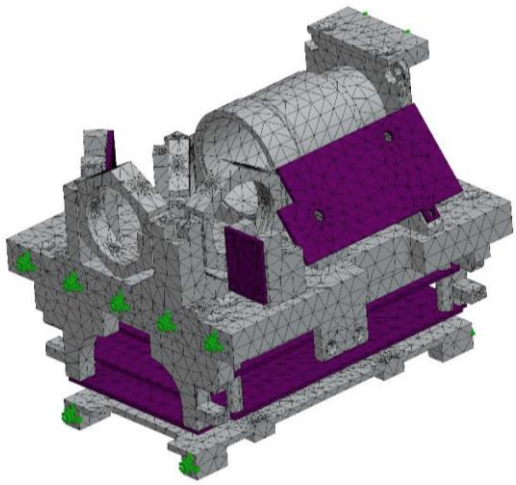


Figure 3. Solidworks model of NODE Structural Finite Element Mesh used for analysis. Figure from Barnes, 2018 [10].

FEA predicts the location of the first resonant frequency to be 500 Hz at the Modulator board, mounted underneath the model shown in Fig. 3 [10]. Table 4 shows the predicted and measured resonant frequencies of NODE's components, the location of each within the payload design, and harmonic direction. Order of resonance describes the nodular order of the resonant frequency (e.g., whether the frequency is a 1 or 2 node frequency), and harmonic direction indicates the presence of structural deformation or structural response to acceleration in that direction. Ten accelerometers were placed on the NODE structure including locations at the FPGA board, daughter board, and Raspberry Pi. These locations were identified by FEA to be places with low resonant frequencies. White Noise, Random Vibe and Sine Burst were tested across all three axes.

Launch vehicle selection is a driving factor for determining the minimum resonant frequency of a spacecraft or payload [15]. Although no minimum payload resonant frequency is specified in the Ariane V rocket user guide, it states that high energy sinusoidal excitations are induced under 100 Hz [22]. Incorporating a safety factor of 2, the NODE payload is designed to have a fundamental frequency greater than 200 Hz [10]. Vibration data in Table 4 shows that payload design meets this goal and identifies the first resonant frequency at 500 Hz located on the CPU board [10].

Analysis of the white noise data showed some small frequency shifts in the fundamental frequency. Shifts in the transfer function during vibration testing indicate mechanical changes in the system. While small shifts often occur, and are attributed to shifts in fixture fastener interfaces, large shifts in the first frequency greater than 5% are indicative of fastener pre-load loss or mechanical failure in the structure [8]. The fundamental frequency was shifted 2% during testing (see Fig. 4), which is less than the 5% failure limit in first frequency shift recommended for satellites of this size [8], [10]. The size of the shift observed is indicative of the settling of the mechanical system rather than structural failure [10]. No mechanical failures were identified after testing was complete [10].

Table 4. FEA Predicted and actual measured resonant frequencies of the NODE structure. Results reported in Barnes, 2018 [10]. Resonance order is listed from lowest to highest.

Predicted Order of Resonance	Predicted Location	Predicted Frequency [Hz]	Harmonic (Direction)	Actual Order of Resonance	Actual Location	Actual Frequency [Hz]
1	Modulator Board	500	1	1	CPU Board	500
2	Daughter Board	500	1	2	Modulator Board	700
3	CPU Board	700	1	3	Daughter Board	900
4	Modulator Board	900	2	-	Coupler Tray	1000
5	Daughter Board	900	2	-	Coupler Tray	1500
-	Coupler Tray	1000	1	-	Main Plate	1600
-	Coupler Tray	1700	2 (x)	-	Coupler Tray	2100
-	Main Plate	2100	1	-	EDFA	2900
-	Coupler Tray	2100	2 (z)	-	-	
-	EDFA	2900	1	-	-	

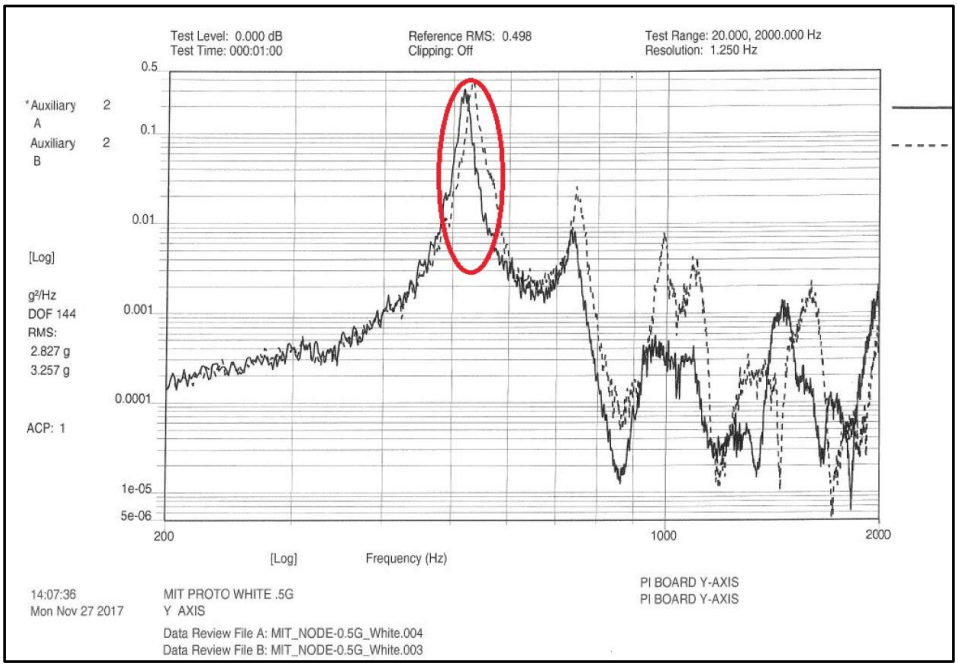


Figure 4. Overlay of White Noise comparison data resulting from random vibe in the Y axis. A small shift of 2% is observed in the first frequency estimated to be 500 Hz. Failure limit for shift in first frequency limit is at 5% for satellites of this size [8], [10].

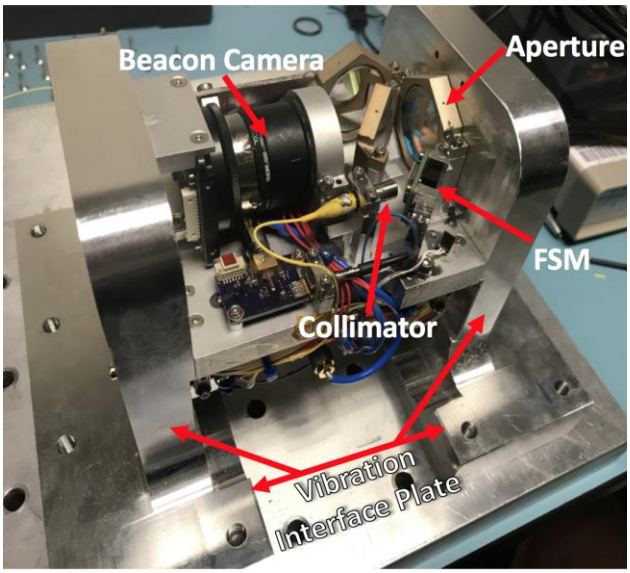


Figure 5. NODE Payload integrated into vibration fixture, secured in expected mounting location of spacecraft bus. Image credit: Derek Barnes [10].

Thermal Testing

Thermal testing was performed at subsystem and component levels. NODE's EDFA was tested in a Thermal Vacuum (TVAC) chamber to determine its ability to maintain functionality in the space and launch environments. The EDFA is a non space-rated, COTS component, necessitating TVAC testing to determine its behavior and characterize performance as a function of operating temperature [10]. TVAC testing took place in the MIT Space Systems Laboratory (SSL) abbess chamber in February 2017. The chamber is 2 ft. x 2 ft. x 2 ft. in size and is pulled down to an approximately ~ 1E-4 mTorr vacuum level.

The device was mounted in the vacuum chamber and operated at flight-like power levels (23 dBm and 24 dBm) [10]. The tests were run in a hot operational case, which simulates the payload experiencing full sunlight while all components dissipate their maximum expected output power [10]. This case demonstrates one of the most rigorous operational modes the thermal control system will experience on-orbit. Testing was performed using continuous wave operation with 15 minute operational periods over three cycle iterations [10]. These 15 minute periods include marginal operating time as the NODE payload is only expected to operate for approximately 10 minute periods, the time when the satellite is visible in the sky from a defined point on Earth [10]. Results indicate the EDFA reached a maximum temperature of 55°C in the hot operational case, below its operational temperature limit rated at 65°C [10].

A measurement of the output power (see TVAC Trials 1-3 in Fig. 6) indicate that the EDFA experienced average power degradation of 0.4 dBm when cycled

through a thermally worst-case scenario [10]. A comparison of the EDFA's pre/post TVAC output power (Fig. 6) demonstrates an average power loss of 0.2 dBm when operated in air [10]. Despite the 0.4 dBm loss in the hot operational case, the EDFA remained functional during testing. The NODE link budget (Table 2) can manage this loss while maintaining 3.78 dB of margin for a 10 Mbps data-rate at 1000 km [19].

NODE's FSM is also a non space-rated component, yet it plays a critical role in the transmit beam pointing to the ground station as it compensates for spacecraft pointing error. To quantify the pointing error experienced over expected temperature ranges (-20°C to 60°C), the FSM was tested in the same thermal chamber [10], [11]. A 10o FOV CMOS detector measured the FSM's pointing accuracy during testing by comparing differences in the calibration and beacon signals (procedure further discussed in the "Over-the-air" section) [10]. To maintain fine pointing accuracy, the FSM is required to hold pointing accuracy to within ± 216 arcseconds of its commanded location [11].

Two ramp/soak profiles were used for FSM thermal cycling. Each comprised nine "soak" intervals stepping from -20°C to 60°C. The first profile ramped up with 20°C increments and the second in 10°C increments [11]. Full tests were completed over 350 minute and 300 minute periods respectively [11]. Test results prove that the FSM satisfies the ± 216 arcsecond pointing requirement as it maintains 12 arcsecond (3-σ) pointing accuracy throughout both tests. This accuracy is based on measurement of the FSM's pointing repeatability, as some drift was induced by coefficients of thermal expansion from the mounting mechanism. We therefore refer to these results as a measurement of the relative pointing error for the FSM rather than a measurement of absolute pointing accuracy of the system.

Future Environmental Testing

Once electronic functional testing is complete, MIT's SSL thermal vacuum chamber will be used to verify absolute pointing accuracy of the fully-assembled, fully-functional payload EM. Testing will occur over 5 cycles, recommended for protoflight qualification levels by NASA GEVS [9]. Mechanisms for measuring system pointing accuracy through the chamber window are under consideration. The test plan involves mounting an IR camera and IR power meter external to the chamber to measure fluctuations in transmit output power and induced drift in the transmitter's pointing accuracy as a function of temperature.

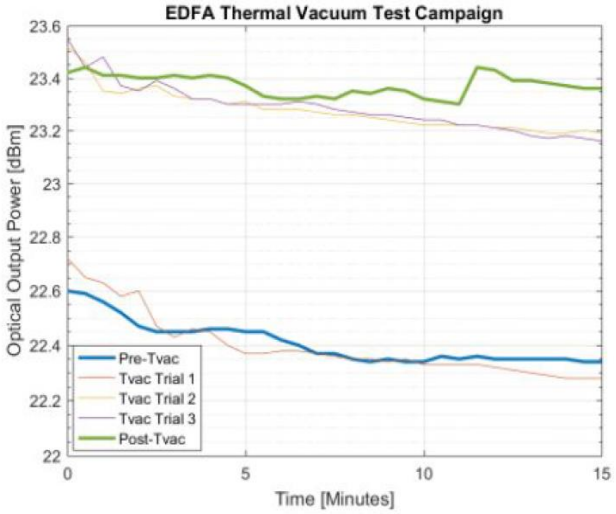


Figure 6. Comparison of pre/post EDFA TVAC testing results performed in MIT's SSL chamber for a hot operational case. Pre/post testing of the EDFA (blue/green lines respectively) were performed in air. This test was designed to determine expected power loss for a worst-case, flight-like scenario used to characterize performance of this COTS component. Results demonstrate an average power loss of 0.4 dBm over TVAC trails 1-3, compared to a loss of 0.2 dBm in the pre/post test phases [10].

NODE Electronics Integration and Testing

Table 5 provides a summary of the NODE electronics boards and their respective functions. There are five custom PCBs that use COTS electrical components and opto-electronics to achieve NODE's target data rate of 10 Mbps. The CPU board interfaces with the spacecraft bus, camera, and Modulator board, and monitors and controls payload electronics. The Modulator board interfaces with the CPU board, Daughter board, and TOSA board, and implements physical layer communication protocols to enable interfacing with opto-electronics and peripheral boards. The Daughter Board acts as a breakout board, routing signals from the Modulator Board to respective components. The Photodiode Board interfaces with the Modulator Board and creates closed-loop feedback with the transmitted optical signal to finely tune the transmitter wavelength. The TOSA Board also interfaces with the Modulator Board and converts the electrical signal containing modulated data into an optical signal. This work focuses on the integration and testing of the CPU board, the Modulator board, the Daughter board, camera, and heaters. NODE electronics integration and testing has four steps: acceptance testing, functional testing, integration into the payload module, and system functional testing. Figure 7 shows the status of each board.

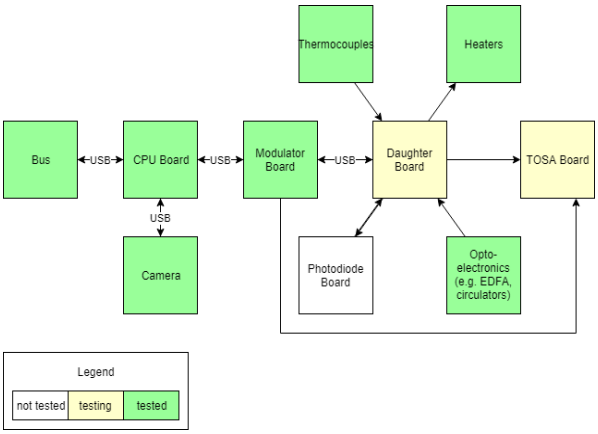


Figure 7. NODE electronics boards integration and test flow and status as of June 2018

Table 5: Summary of NODE Electronics Boards and Functions as of June 2018

Board Name	Function	Iteration	Interfaces With
CPU	Configures Modulator board, controls payload components, processes frames from camera	Flight Model	Host spacecraft, modulator board, camera
Modulator	Implement Pulse Position Modulation (PPM), route modulated data to TOSA board, implement memory map (described below), implement physical layer communication protocol	Flight Model	CPU board, Daughter board, TOSA
Daughter	Routes signals from Modulator board to respective component or opto-electronics	Engineering Model	Modulator board, thermocouples, heaters, TOSA, EDFA, photodiode board, feedback layer board, FSM driver board
Photodiode	Verify frequency and optical power output, provide closed-loop feedback to the TOSA	Engineering Model	Daughter board
TOSA	Converts the electrical signal from the Modulator to the optical signal	Engineering Model	Daughter board, Modulator board

CPU Board Development and Acceptance Testing

A challenge with developing a custom CPU board is satisfying the requirement that the Raspberry Pi operates in slave mode to receive commands from and send telemetry data to the bus. During software updates and upgrades, the CPU must be reprogrammed through the USB 2.0 port in slave mode. Due to these constraints, a USB hub is added to the CPU board to accommodate peripheral connections, RF switches added to control the USB 2.0 I/O depending on the CPU mode configuration (i.e. slave or master), and a SPI-to-USB peripheral is added to act as the USB slave for the bus during normal operations. Fig. 8 illustrates the final design form that emerged from functional requirements.

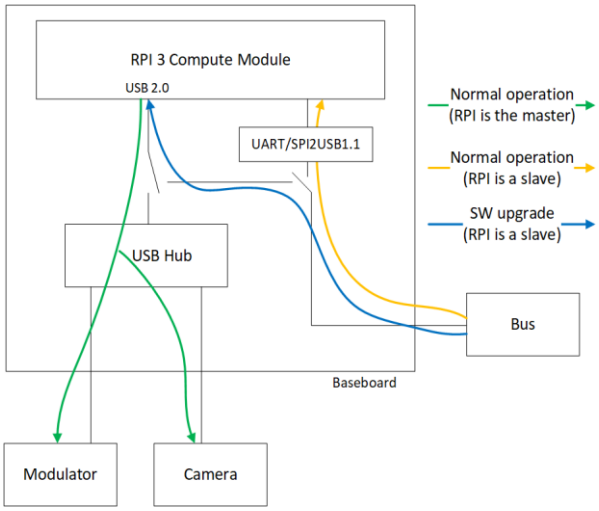


Figure 8. CPU Board Operational Modes

To test the CPU board, an external PC is used as a bus emulator and connected via USB. Successful power on and boot up indicated that CPU was operating as expected. The USB 2.0 connection was tested by reprogramming the CPU board on startup, simulating on-orbit operation. This demonstrates successful communication with the CPU board during software upgrade operations and gives confidence that in the event of a corrupted operating system (OS), the CPU board can be successfully reprogrammed and continue nominal operations.

The CPU board was also tested in master mode by integrating the beacon camera, which is used for pointing, acquisition and tracking of the ground terminal. The CPU board is responsible for configuring the internal registers of the camera, collecting frames, and processing images. The CPU board successfully received and processed an image of the camera, meeting functional requirements and confirming that the USB hub operates as intended.

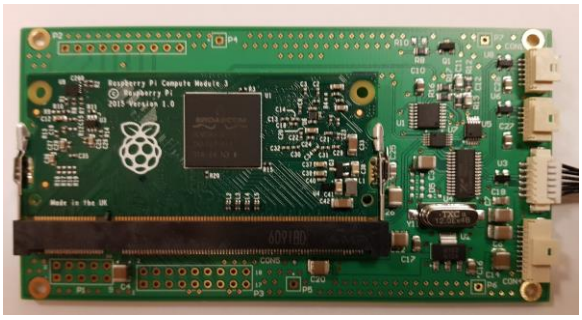


Figure 9: CPU Board (105mm x 55mm)

Modulator Board Development and Acceptance Testing

Following the camera integration is the Modulator board. The physical setup is identical to the CPU board, but the role of the PC changes to emulate the flight CPU board (see Fig. 7 or Table 5). There are four designs implemented in the Spartan 6 Field-Programmable Gate Array (FPGA) on the Modulator board, one for each of its main functions: 1) USB interface with the CPU board, 2) control and protocol interfaces, *e.g.* power monitoring, SPI, serial, parallel, UART, etc., 3) PPM modulator, and 4) Built-In-Self-Test (BIST). A memory map is developed to streamline functional testing and operation during flight. Figure A.1 shows the memory map implemented in the FPGA. The addresses are categorized into 11 groups with a name, read/write permission, and a bit-by-bit description. The highlighted addresses are those repetitively used during testing. The memory map implements a level of abstraction that is advantageous to future development and integration; successful use of the memory map implies future programmers only need to know the memory map to communicate with peripheral components.

Detailed functional testing of the Modulator board using the memory map involves: first, the address containing the FPGA Core version (VER, see Fig A.1) is read to verify the correct configuration of the device. Second, the address containing a free-running counter (FRC) is read twice to confirm that its value is changing and the design is correctly driven by the clock. Third, different addresses in the memory map are written and consecutively read to verify the correct write access operations. Additionally, the counter containing the number of accepted commands (ACC) is read to verify that commands are correctly received. Fourth, invalid addresses and invalid values for valid addresses are used to verify that the rejected command counter (RCC) is increasing and commands are correctly rejected. Finally, different addresses mapped to physical interfaces are probed using an oscilloscope to verify pins in the FPGA are driven correctly. Completion of the memory map test verifies the operation of the USB interface and control and protocol interfaces. Testing the BIST core and the Modulator core requires integration of the Photodiode board and the TOSA board, which is

scheduled to take place after the completion of the photodiode board acceptance testing.

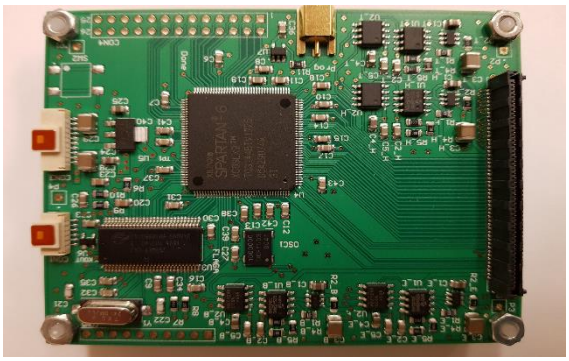


Figure 10: Modulator board (90mm x 70mm)

CPU Board and Modulator Board Development and Testing

After functionality of the Modulator and CPU boards are checked, the transition is to system-level integration and testing. The CPU board is connected to the PC (acting as a bus emulator) via USB 1.1, and then connected to the Modulator board via USB 2.0. The tests initially conducted with the PC acting as the flight CPU board are repeated with the EM CPU board. The CPU configures the Modulator board, and implements tests using the memory map. This shows that successful communication between the boards is established, and integration can move to the next step(s).

Daughter Board Integration and Testing

Proceeding with system-level integration and testing, the Daughter board is then integrated with the Modulator board (which still connected to the CPU board). The interface between the two boards is a custom, 50-pin connector, creating a mezzanine structure.

The functional test of the Daughter board is a two-step process. The current consumption for each subsystem connected to the Daughter board is monitored with a circuit on the Modulator board. In an overcurrent event, the Modulator board opens the corresponding power rail.

External potentiometers are connected to the Daughter board to simulate different system loading conditions, and the response of the Modulator board is observed. After exceeding the current threshold, the Modulator board opens the corresponding switch, meeting functional requirements of the power management subassembly and demonstrating successful corresponding power connections between the Daughter board and peripheral loads. The thresholds are circuit-dependent parameters in the application SW running in the CPU. The CPU reads the current consumption values from the memory map implemented in the FPGA (CC1 to CC4, see Figure A.1) and, in case of overcurrent, switches off the corresponding payload by writing in the memory map (PO1 to PO4). The same power on/off registers are used by the CPU to implement the different operational modes.

Continuing with system integration, the thermal control system is evaluated by connecting the heaters and thermocouples to the Daughter Board. Presently, the thermal control system has been integrated, and testing will be completed by changing the thermal conditions of the system.

Figure 11: Daughter board, 90mm x 70mm (left), TOSA board (top right), and PD board (bottom right)

Future Work in Electronics Testing

Future work includes acceptance testing and integration of the EM Photodiode board and integration of the TOSA board with the Daughter board. The EM Photodiode board has been designed, fabricated, and assembled, and the TOSA board has been acceptance tested. Integration and testing of both boards will begin once the thermal control system testing concludes. The PPM modulator core in the FPGA will interface with the TOSA board, and the BIST core with the photodiode board. NODE achieves a high transmitter extinction ratio by shifting the laser diode (mounted on the TOSA board) wavelength in and out of the passband of the Filter Bragg Grating (FBG) through closed-loop feedback, bias current and temperature control [1], [14]. The Modulator core implements M-ary PPM and sends it to the TOSA, whose output is fed into the laser diode. The optical output of the laser will be measured in a setup similar to [2]. The photodiode board receives a fraction of the modulated optical signal, which is input into the BIST core to calculate the differences between the transmitter signal (provided by the Modulator core) and the received signal. This value is known as the Slot Error Rate (SER), and is sent to the CPU to implement its tuning algorithm of the bias current and temperature of the TOSA [12]. Fig. 12 shows the control flow diagram of this process.

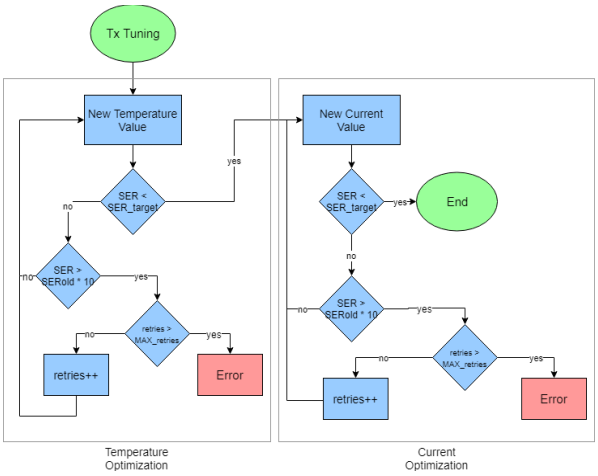


Figure 12: Diagram of transmitter tuning process to achieve a high extinction ratio

Over-the-air Testing

Fig. 13 shows the setup of the initial over-the-air (OTA) test conducted in the MIT STAR lab environment in Spring 2017 (see Fig. 13). This demonstration shows the back end optomechanical instrumentation fully assembled, as well as the PorTeL ground station successfully tracking the injected signal [5].

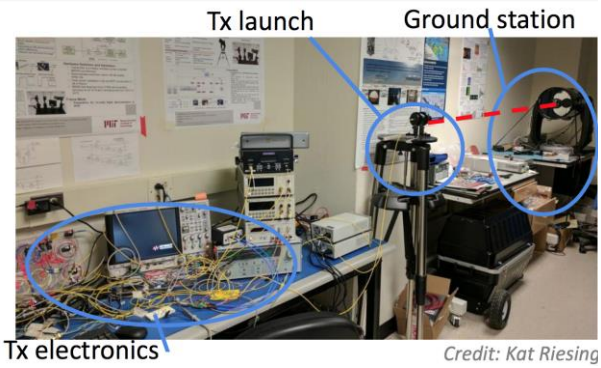


Figure 13. Over-the-air test setup in the STAR Lab environment [2]

The primary objective of this test was to verify the functionality and maintained precision of the fine pointing system developed for the space and ground terminals to within our desired bus coarse pointing accuracy of +/- 0.15° (3σ). The test also sampled over the air data to verify signal modulation and demodulation, stepping through all desired PPM orders. Fig. 14 shows one example of successful transmission and reception of symbols using PPM-16 with 12 samples per slot and 8 bits per sample [2].

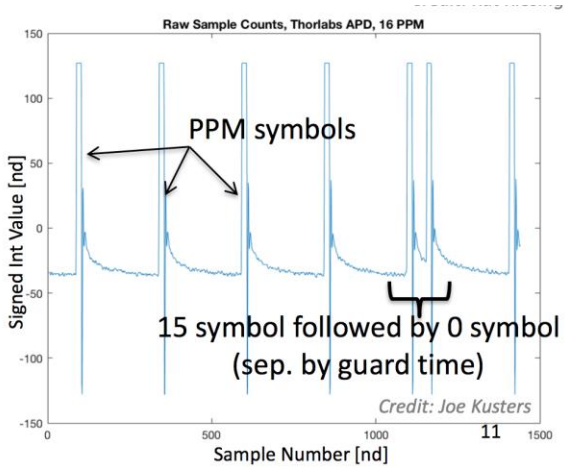


Figure 14. Raw sample counts received on ThorLabs APD (APD110C) during initial OTA test. Test was configured with 16 Pulse Position Modulation, 12 samples per slot and 8 bits per sample. No coding was applied [2].

The pointing, acquisition, and tracking (PAT) system consists of a coarse pointing stage followed by a fine pointing stage (MEMS FSM) to accommodate residual coarse pointing error, environmental disturbances, and spacecraft jitter. The coarse pointing stage directly uses the host spacecraft's attitude determination and control system (ADCS) to inertially point and slew towards the ground station. The fine pointing system consists of a MEMS fast steering mirror (FSM) for actuating the transmit and calibration beams as demonstrated in Fig. 15. The calibration signal is received on a 10° FOV CMOS camera, which also receives the beacon signal. Because of the reflection of the calibration laser, shown in Fig. 15, the transmit and beacon signals are co-aligned when the calibration spot is symmetrically aligned opposite of the beacon spot. The position error of the calibration laser relative to this reference is determined via a custom image processing algorithm. An integral control law is used to command the FSM to actuate the transmit and calibration beams to compensate for bus pointing error and other disturbance sources. The system has been validated against a simulated bus coarse pointing error of ± 0.15 deg (3σ) with a stability of ± 0.0225 deg/s (3σ) and maximum pointing bias of ± 1 deg [11], [20]. A Thorlabs APD110C was used by the receiver for test purposes, which is limited to a 50 MHz bandwidth. Therefore, a data rate check was not performed and the slot times were increased to accommodate the APD.

Once full functional testing of the EM is complete, EM OTA testing will proceed similar to the process presented in Fig. 13. The EM will be placed at a known distance from the ground station, a command will be issued to transmit a signal with the desired data rate and PPM order, and PorTeL's ability to receive the transmitted signal will be

determined. There is an ongoing investigation of appropriate mechanisms for performing OTA between the NODE payload and PorTeL during thermal vacuum testing.

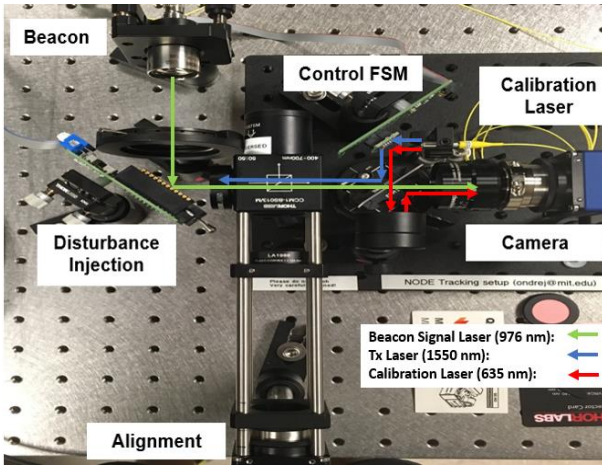


Figure 15. Test Setup for Demonstration of Fine Pointing Control Algorithm

CONCLUSION

This paper provides an updated status on NODE integration and test progress. The NODE payload met vibration requirements with a small shift of 2% in the first resonant frequency transfer function, below the 5% failure limit. NODE has also successfully interfaced with the PorTeL ground station implementing PPM-16 via OTA testing. Acceptance testing, integration, and test of the CPU board, Modulator board, and Daughter board have been successful to date, with all boards meeting functional requirements. Moving forward, the NODE team will complete functional and integration and testing of the Photodiode board and the TOSA board.

Once tests are complete, all boards will be integrated into the NODE optomechanical structure in preparation for full functional and environmental testing. Tests will be performed to protoflight levels as specified by NASA GEVS. The flight unit will be ready for integration with a host in Summer 2018.

ACKNOWLEDGEMENTS

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REFERENCES

1. Clements, E., et al., "Nanosatellite optical downlink experiment: design, simulation, and prototyping," Opt. Eng. 55(11) 111610 (13 September 2016).

2. Clements, E., et al., "Integration and Testing of the Nanosatellite Optical Downlink Experiment," AIAA/USU Conference on Small Satellites 2017.

3. Riesing, K., Yoon, H., Cahoy, K. "A Portable Optical Ground Station for Low-Earth Orbit Satellite Communications," IEEE ICSOS 2017.

4. Henry, C., "FCC issues warning in wake of swarm's unauthorized launch." http://spacenews.com/fcc-issues-warning-in-wake-of-swarms-unauthorized-launch/2018.

5. Figura, J., Cahoy, K., "Design, Construction and Testing of LED Beacon to Enable Location of a Lasercom Ground Station," May 2017.

6. Riesing, K., "Portable Optical Ground Stations for Satellite Communication," PhD Thesis, Massachusetts Institute of Technology (2018).

7. Interagency Operations Advisory Group, "Optical Link Study Group Final Report," 2012.

8. Sarafin, T., et al. Vibration testing of small satellites - part 3. Retrieved from http://www.instarengineering.com.

9. Baumann, R., "General Environmental Verification Specifications for STS and ELV Payloads, Subsystems, and Components," NASA Goddard Space Flight Center, Greenbelt, Maryland 20771, rev. a edition, June 1996.

10. Barnes, D., "Optomechanical Design, Analysis, and Testing of the Nanosatellite Optical Downlink Experiment," Master's Thesis, Massachusetts Institute of Technology (2018).

11. Riesing, K., "Development of a pointing, acquisition, and tracking system for a nanosatellite laser communications module," Master's Thesis, Massachusetts Institute of Technology (2015).

12. Lee, M. "Optomechanical and Wavelength Alignments of CubeSat Laser Communication Systems," Master's Thesis, Massachusetts Institute of Technology (2017).

13. Hemmati, H. Near-Earth Laser Communications, CRC Press (2009).

14. Kingsbury, R., "Optical communications for small satellites," PhD Thesis, Massachusetts Institute of Technology (2015).

15. Federal Communications Commission. (2018, April 17). *In the Matter of Streamlining Licensing Procedures for Small Satellites [NOTICE OF PROPOSED RULEMAKING]*. Retrieved from https://transition.fcc.gov/Daily_Releases/Daily_Business/2018/db0417/FCC-18-44A1.pdf

16. Haughwout, C., "Non-coherent LED Arrays as Ground Beacons for Small Satellite Optical Communications Systems," AIAA/USU Conference on Small Satellites 2018.

17. Long, M. "Pointing Acquisition and Tracking Design and Analysis for CubeSat Laser Communication Crosslinks," Master's Thesis, Massachusetts Institute of Technology (2018).

18. Cierny, O., "Precision Closed-Loop Laser Pointing System for the Nanosatellite Optical Downlink Experiment", M.S. Thesis, Julius Maximilians University of Würzburg, 2017.

19. Clements, E., "Probabilistic Methods for Systems Engineering with Application to Nanosatellite Laser Communications," PhD Thesis, Massachusetts Institute of Technology (2018).

20. Riesing, K., "Rapid telescope pointing calibration: A quaternion-based solution using low-cost hardware," Journal of Astronomical Telescopes, Instruments, and Systems, March 2018.

21. "Global ground station network." http://www.bridgesatinc.com/products/ #ground

22. Lagier, R. Ariane 5 User's Manual. Arianespace, Greenbelt, Maryland 20771, issue 5 revision 2 edition, October 2016.

23. Celestron, "CPC 1100 GPS (XLT) computerized telescope," May 2016. Retrieved from http://www.celestron.com/browse-shop/astronomy/telescopes/cpc-1100-gps-(xlt)-computerized-telescope

APPENDIX

Group	Address (hex)	Name	Description	R/W	B7	B6	B5	B4	B3	B2	B1	B0
Control & Status	00	CTR	Control	RW						SPI2 en	PID en	Tx en
	3F	FLG	Status	RO	Mod error	UART Tx Ready	UART Rx New		SEM uncorrectable	SEM stopped	SEM initialized	DCM locked
	31	ACC	Accepted commands	RO	D7	D6	D5	D4	D3	D2	D1	D0
	32	RCC	Rejected commands	RO	D7	D6	D5	D4	D3	D2	D1	D0
	33	LAC	Last acepted command	RO	D7	D6	D5	D4	D3	D2	D1	D0
	34	LRC	Last rejected command	RO	D7	D6	D5	D4	D3	D2	D1	D0
	35	FRC	Free running counter	RO	D7	D6	D5	D4	D3	D2	D1	D0
	36	VER	Core version	RO	0	0	0	0	0	0	0	1
	37	WRS	Write accesses	RO	D7	D6	D5	D4	D3	D2	D1	D0
	38	WRA	Last write Address	RO	D7	D6	D5	D4	D3	D2	D1	D0
Cal. Laser	20	CAL	Calibration diode	RW	ON/OFF code (ON = 0x55, OFF = 0x0F)							
Power management	21	PO1	Power on/off 1	RW	ON/OFF code (ON = 0x55, OFF = 0x0F)							
	22	PO2	Power on/off 2	RW	ON/OFF code (ON = 0x55, OFF = 0x0F)							
	23	PO3	Power on/off 3	RW	ON/OFF code (ON = 0x55, OFF = 0x0F)							
	24	PO4	LD TEC Power on/off	RW	ON/OFF code (ON = 0x55, OFF = 0x0F)							
	60	CC1a	Current consumption 1 (MSB)	RO					D11	D10	D9	D8
	61	CC1b	Current consumption 1 (LSB)	RO	D7	D6	D5	D4	D3	D2	D1	D0
	62	CC2a	Current consumption 2 (MSB)	RO					D11	D10	D9	D8
	63	CC2b	Current consumption 2 (LSB)	RO	D7	D6	D5	D4	D3	D2	D1	D0
	64	CC3a	Current consumption 3 (MSB)	RO					D11	D10	D9	D8
	65	CC3b	Current consumption 3 (LSB)	RO	D7	D6	D5	D4	D3	D2	D1	D0
	66	CC4a	Current consumption 4 (MSB)	RO					D11	D10	D9	D8
	67	CC4b	Current consumption 4 (LSB)	RO	D7	D6	D5	D4	D3	D2	D1	D0
Thermal management	68	TE1a	Temperature 1 (MSB)	RO					D11	D10	D9	D8
	69	TE1b	Temperature 1 (LSB)	RO	D7	D6	D5	D4	D3	D2	D1	D0
	6A	TE2a	Temperature 2 (MSB)	RO					D11	D10	D9	D8
	6B	TE2b	Temperature 2 (LSB)	RO	D7	D6	D5	D4	D3	D2	D1	D0
	6C	TE3a	Temperature 3 (MSB)	RO					D11	D10	D9	D8
	6D	TE3b	Temperature 3 (LSB)	RO	D7	D6	D5	D4	D3	D2	D1	D0
	6E	TE4a	Temperature 4 (MSB)	RO					D11	D10	D9	D8
	6F	TE4b	Temperature 4 (LSB)	RO	D7	D6	D5	D4	D3	D2	D1	D0
	70	TE5a	Temperature 5 (MSB)	RO					D11	D10	D9	D8
	71	TE5b	Temperature 5 (LSB)	RO	D7	D6	D5	D4	D3	D2	D1	D0
	72	TE6a	Temperature 6 (MSB)	RO					D11	D10	D9	D8
	73	TE6b	Temperature 6 (LSB)	RO	D7	D6	D5	D4	D3	D2	D1	D0
	25	HE1	Heater 1 on/off	RW	ON/OFF code (ON = 0x55, OFF = 0x0F)							
	26	HE2	Heater 2 on/off	RW	ON/OFF code (ON = 0x55, OFF = 0x0F)							
LD temp controller	01	LTSa	Temp Set Point(MSB)	RW					D11	D10	D9	D8
	02	LTSb	Temp Set Poin (LSB)	RW	D7	D6	D5	D4	D3	D2	D1	D0
	74	LTMa	Measured temp (MSB)	RO					D11	D10	D9	D8
	75	LTMb	Measured temp (LSB)	RO	D7	D6	D5	D4	D3	D2	D1	D0
LD Bias Current	03	LBCa	Bias Current (MSB)	RW	A3 (0)	A2 (0)	A1 (0)	A0 (0)	D11	D10	D9	D8
	04	LBCb	Bias Current (LSB)	RW	D7	D6	D5	D4	D3	D2	D1	D0
Tx power level	05	THRa	Threshold configuration	RW			C2	C1	C0	A2	A1	A0
	06	THRb		RW	D15	D14	D13	D12	D11	D10	D9	D8
	07	THRc		RW	D7	D6	D5	D4	D3	D2	D1	D0
	40	PDI	Power level	RO							PD2	PD1
FSM	08	FSMa	FSM configuration	RW			C2	C1	C0	A2	A1	A0
	09	FSMb		RW	D15	D14	D13	D12	D11	D10	D9	D8
	0A	FSMc		RW	D7	D6	D5	D4	D3	D2	D1	D0
EDFA	0B	ETX	UART Tx	RW	D7	D6	D5	D4	D3	D2	D1	D0
	41	ERX	UART Rx	RO	D7	D6	D5	D4	D3	D2	D1	D0
SEM controller	0C	SEP	Error Period	RW	D7	D6	D5	D4	D3	D2	D1	D0
	42	SCE	Corrected Errors	RO	D7	D6	D5	D4	D3	D2	D1	D0
	43	SIE	Inserted Errors	RO	D7	D6	D5	D4	D3	D2	D1	D0
	44	SST	SEM Status	RO	uncorrectable					observation	initialization	heartbeat
Modulator	0D	DAT	PPM order / Data	RW	D7	D6	D5	D4	D3	D2	D1	D0
	0E	DEL	Delay	RW	D7	D6	D5	D4	D3	D2	D1	D0
	39	FFF	FIFOs Flags	RO	ONES FIFO PTR9, PTR8		ERRORS FIFO PTR10, PTR9, PTR8			DATA FIFO PTR10, PTR9, PTR8		
	3A	ERR	Errors	RO	D7	D6	D5	D4	D3	D2	D1	D0
	3B	ONE	Ones	RO	D7	D6	D5	D4	D3	D2	D1	D0
	3C	DFP	Data FIFO Pointer	RO	D7	D6	D5	D4	D3	D2	D1	D0
	3D	EFP	Errors FIFO Pointer	RO	D7	D6	D5	D4	D3	D2	D1	D0
	3E	OFP	Ones FIFO Pointer	RO	D7	D6	D5	D4	D3	D2	D1	D0

Figure A.1. Memory map implemented in the FPGA