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Radiation-Tolerant, GaN-based Point of Load Converters for Small Spacecraft Missions

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ABSTRACT

As computational loads for spacecraft continue to grow, the requirements levied on power-conversion electronics have become increasingly demanding. Designing for compute-intensive processing capabilities in the CubeSat form-factor further encourages the use of lightweight, compact, and efficient power-conversion electronics. However, the radiation-tolerant and radiation-hardened point-of-load converters available from existing vendors are large, expensive, and inefficient relative to their commercial counterparts. To alleviate this disparity, this paper presents the design, development, and testing of three radiation-tolerant, point-of-load (PoL) converters using Gallium Nitride (GaN) High-Electron Mobility Transistors (HEMT) and commercial controllers to enable the success of future small-satellite missions.

INTRODUCTION

Converters with Gallium Nitride (GaN) high-electron mobility transistors (HEMTs) have shown considerable promise for low-earth orbit (LEO) spacecraft applications. They provide higher efficiencies with lower volumes, mass, and cost when compared to conventional Silicon MOSFETs. This research takes advantage of the performance gains provided by commercial and flight-quality GaN HEMTs, and coupled with commercial fault-tolerant controllers to develop and test a set of converters for next-generation spacecraft electronics. The experimental point-of-load (PoL) converters are designed to operate at 2.0 MHz with an input voltage of 12 V and a load current of 1.0 A. The PoL converter design is capable of operating with an input voltage up to 38 V and load currents as high as 20 A. When compared to radiation-hardened converters, the proposed GaN PoL converters require 84% less mass, 79% less volume, and reduce component cost by 83%. All of which are achieved while maintaining a full-load efficiency of 96%.

Rad-hard controllers are typically very large and use older technologies that do not take full advantage of the high frequency GaN HEMTs capabilities. Converter design with COTs controllers allow for smaller and more efficient power converters. For the proposed converters, an average efficiency of 87% to 91% is expected with comparable rad-hard converters reporting between 65% and 80% efficiency [1]. The increased efficiency represents a significant decrease in lost power and heat dissipation for space flight systems. Performing radiation testing on the COTs controllers and obtaining flight heritage should provide sufficient evidence for the viability of these converters for LEO CubeSat applications.

In-situ evaluation of the GaN PoL converters will be performed as a part of the Department of Defense Space Test Program- Houston 6 (STP-H6) mission. As a sub-experiment of the experiment called Spacecraft Supercomputing for Image and Video Processing (SSIVP), three different GaN PoL buck converters will be evaluated throughout a multi-year mission on the exterior of the International Space Station (ISS). Dedicated circuitry will measure the voltage and current to track each GaN PoL converters' performance and degradation, enabling a multi-year characterization of efficiency and stability.

GAN HEMT TECHNOLOGY

GaN for power electronic applications has several advantages over silicon, primarily a significantly wider band-gap (3.4eV compared to 1.12eV) [2]. The larger energy gap permits GaN devices to operate at a higher temperature, despite slightly poorer material thermal conductivity, and shrinks the physical depletion region of the transistor while maintaining a high blocking and

breakdown voltage. The smaller depletion region width also reduces on resistance which improves efficiency of switching converters [3][4]. GaN power devices are typically HEMTs, a type of heterojunction field effect transistor (HFET) that allows electrons to move more freely throughout the material and provide faster gate turn-on [5]. As a result, GaN HEMTs can switch higher voltages at a higher frequency in a smaller area than an equivalent silicon transistors [6]. Additionally, these properties reduce switching losses and allow for the selection of smaller inductors while retaining the same power output as silicon-based converters.

The construction and material properties of GaN HEMT provide several innate advantages over silicon when operating in harsh radiation environments. There are four main types of semiconductor radiation effects that can impact the performance of a transistor: total ionizing dose (TID), single event effects (SEEs), dose-rate radiation, and radiation displacement damage [7]. Throughout a mission duration, TID develops from photons or high-energy particles passing through the oxide that leads to an accumulation of charges building at both the gate and field oxide. The Schottky metal gate on many GaN HEMTs eliminates most of the TID effects observed in standard silicon FETs. When energetic ions pass through the semiconductor, electron hole pairs are created from deposited energy that induce SEEs. The band-gap of GaN HEMTs require a much higher energy photon or ion to achieve ionization in the semiconductor, reducing the susceptibility to SEEs [7]. With smaller depletion region volumes of GaN HEMTs compared to silicon FETs, dose rate radiation has less impact. Radiation displacement damage, caused by neutrons and protons, displace the semiconductor atoms from the crystalline lattice and create traps-recombination sites in the device. GaN HEMTs are very resilient to this type of radiation and very rarely experience failure [7]. Previous testing at NASA JPL has shown that GaN HEMTs are extremely resistant to both radiation-induced TID and SEEs [7][8].

Historically, manufacturing difficulties of GaN FETs led to higher costs, by a factor of three when compared to silicon devices, but recent advancements in manufacturing technology have driven costs down [9]. As a result of their innate radiation tolerance, special packaging is not needed to improve radiation fault tolerance, enabling more efficient operation at MHz switching frequencies that would be prohibitively inefficient to achieve with traditional silicon rad-hard components [8]. Most rad-hard converters using silicon operate in the 100 - 500 kHz range [1][10]. By operating in the MHz range, inductors and capacitors can be scaled down by an order of magnitude further reducing converters size and weight.

HIGH FREQUENCY CONVERTER DESIGN

This section provides an overview of the design, simulation, layout, and characterization of the proposed high-frequency GaN HEMT converters that will run as a sub-experiment on STP-H6 SSIVP.

Converter Design and PCB Development

The PoL synchronous buck converters were selected based on prior performance in radiation environments. The Linear Technology LTC3833 has been tested as a PoL converter in the Large Hadron Collider (LHC) at CERN, and has shown promise in resisting the effects of SEE, TID, and strong magnetic fields [11]. The silicon process technology of the Texas Instruments LM25141 is expected to survive the radiation environment in LEO. The selected GaN HEMTs were chosen to provide high efficiency over the full converter range in both high-density commercial and flight-proven hermetic packages. Parameters for the selected controllers and GaN HEMT devices are given in Table 1 and Table 2, respectively.

Table 1. Buck Controller Parameters

Parameter	LTC3833	LM25141-Q1
Input Voltage Range	4.5 – 38 V	3.8 – 42 V
Output Voltage Range	0.6 – 5.5 V	1.5 – 15 V
Switching Frequency	2 MHz	2.2 MHz
Gate Drive Voltage	5.3 V	5 V

Table 2. GaN FET Parameters

Parameter	EPC2014C	TDG100E15BSDX
Drain-Source Voltage	4.5 – 38 V	3.8 – 42 V
Threshold Gate-Source Voltage	1.4 V	1.3 V
Maximum Gate-Source Voltage	6 V	7 V
On Resistance	16 mΩ	21 mΩ
Gate Charge	2.5 nC	6.2 nC
Package Type	Passivated BGA Die	SMD-0.6

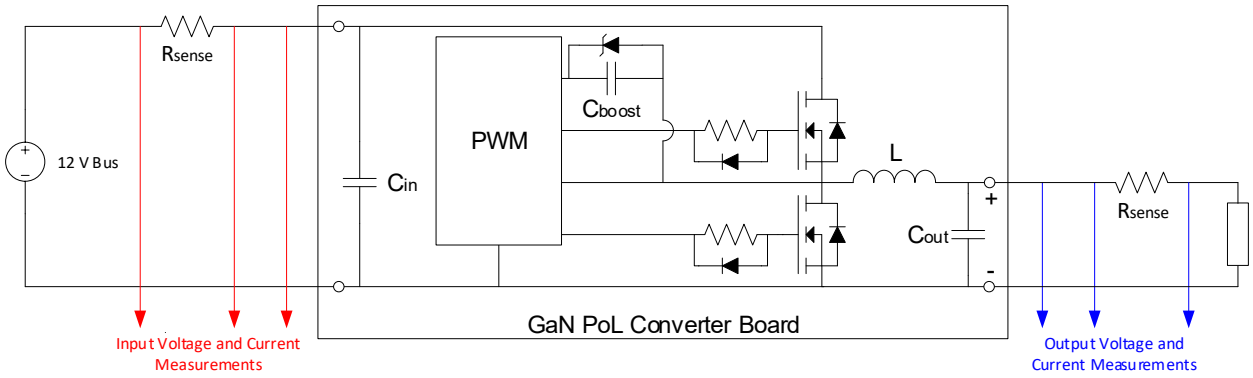

Figure 1. Converter Configuration for SSIVP GaN Experiment

A key challenge of driving GaN HEMTs is controlling gate-source voltage overshoot during device turn-on. To prevent this overshoot, several steps were taken, as illustrated in Fig. 1. First, an optimally selected gate resistor was used to slow the rise-time and reduce the magnitude of the gate overshoot while maximizing converter efficiency. To ensure that high-side drive voltage does not drift during system transients, a 5.1 V clamping Zener diode was added across the boost capacitor. Additionally, Schottky diodes were placed between the controllers and the gate on each GaN HEMT to provide a rapid discharge path during device turn-off, reducing switching losses and minimizing Miller turn-on effects. Both controllers have fixed dead-time logic to ensure the top and bottom gates are not driven on simultaneously, eliminating shoot-through that further reduces efficiency and can damage the FETs.

The converters were designed for a 30% ripple current at 2.5 A. The inductor for the LTC3833 controller was the Taiyo Yuden 2.2 µH with a rated current of 2.5 A and a DC resistance of 80 mΩ. The inductor for the LM25141 controller was the Würth Elektronik 3.3 µH with a rated current of 3.23 A and a DC resistance of 33 mΩ. The inductors were selected based on manufacturer recommendations from the datasheets. However, depending on the application, the inductor can be sized appropriately to further optimize efficiency based on the desired load current, ripple current, and package dimensions. With a maximum input voltage of 38 V, the bypass capacitors were selected with a 50 V rating to allow future testing at 28 V, a common de-rating practice. High quality ceramic capacitors were selected based on trade-offs between size, performance, parasitics, and serviceability.

The test PCB converters, shown in Fig. 2, were designed using a 4-layer stackup and manufacturing tolerances that include a 10 mil minimum via diameter with a 4 mil annular ring. The stackup of the test converter PCBs were designed to provide optimal performance at minimal cost: (Top) signal/power, (Layer 1) ground, (Layer 2) signal/power, (Bottom) ground. Castellated vias were placed at the input and output terminals to allow the converter PCB to act as a drop in power supply module that can be easily modified to meet the needs of individual missions.

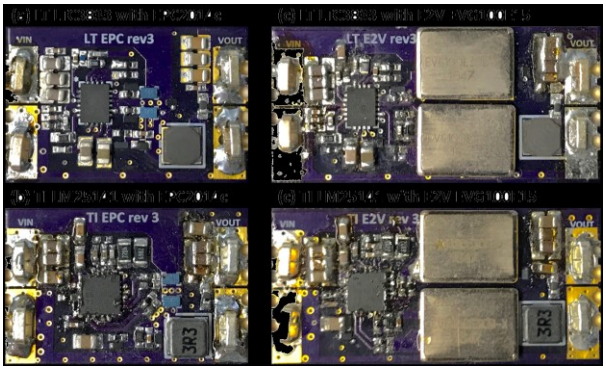

Figure 2: Assembled Test Converter PCBs

During the PCB layout process, focus was placed on minimizing the footprint area for each GaN HEMT for two primary reasons: reduced harmonic content of high switching frequency, and address area constraints for CubeSat applications. Gate drive traces are as short and wide as feasibly possible to minimize inductance that can induce ringing on the gate. Since the switching node between the source and drain of the GaN HEMTs is also switching at high frequency, vias were designed to reduce inductance to the internal plane that provides a low impedance connection with high-current handling capability. Additionally, isolation of sensitive traces required for converter control becomes difficult as the dimensions of the PCB are reduced. The PCB stackup was designed to provide a solid ground return path directly under the high frequency and high current traces that prevent coupling. Sensitive signals were carefully routed on the internal layer to increase the noise immunity of sensing signals.

Power density and specific power considerations are particularly important for power converters in CubeSat applications. The proposed converter layouts represent a significant reduction in the average area (54%), volume (79%), and weight (84%) when compared to other representative PoL radiation-tolerant converters. Mechanical parameters are provided in Table 3.

Table 3: Mechanical dimensions of GaN converters

Configuration	GaN HEMT	Area [in^2]	Volume [in^3]	Weight [g]
Test Converter	EPC	0.62	0.09	2.32
	E2V	0.85	0.11	4.74
Flight Converter	EPC	0.41	0.05	1.31
	E2V	0.64	0.09	3.76
Representative Rad-Tolerant PoL Converter	-	1.16	0.31	16.00

Converter Simulations Results

The proposed converter topologies with SPICE models were obtained from and simulated in LTspice prior to manufacturing, ensuring the proposed topologies would operate within the design specifications. Each simulation was configured with the previously discussed design parameters, however only SPICE models for the EPC GaN HEMTs were commercially available. Individual simulations were used to evaluate a wide range of common converter parameters including: gate switching waveforms, inductor current ripple, and output voltage ripple. The waveforms for the LTC3833 controller and the EPC2014c converter topology are presented in Fig. 3 – Fig. 8 for 5 V and 3.3 V output voltages.

Simulations results for the LTC3833 with EPC2014c HEMTs are shown in Fig. 3 – Fig 5, for an input voltage of 12 V, output voltage of 5V, and a load resistance of 4.7 Ω.. An average steady state inductor current of 1.05 A was observed with a current ripple of 771 mA which corresponds to 31% ripple. The simulation produced an output voltage of 4.95 V with a ripple voltage of 6 mV or approximately 0.1. The gate voltage waveforms switched at 1.9 MHz with the top gate turning on slightly slower than the bottom gate, resulting from the 5 Ω resistor placed in between the controller and the gate of the EPC2014c. No overshoot is observed since the simulation model does not account for trace and package inductance which are the primary factors impacting overshoot in high frequency converters.

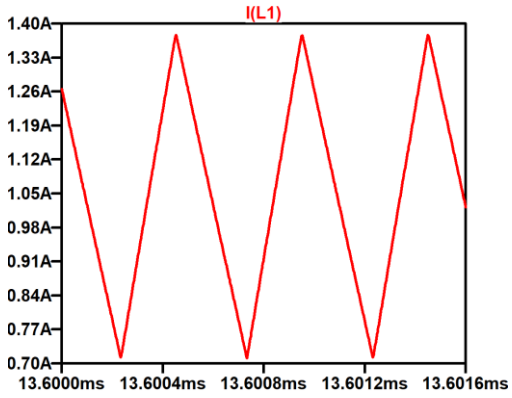

Figure 3: Inductor current ripple of LTC3833 with EPC2014c configured to regulate 12 V to 5 V

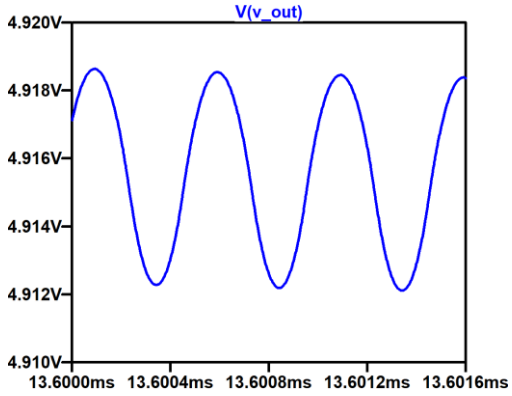

Figure 4: Output voltage ripple of LTC3833 with EPC2014c configured to regulate 12 V to 5 V

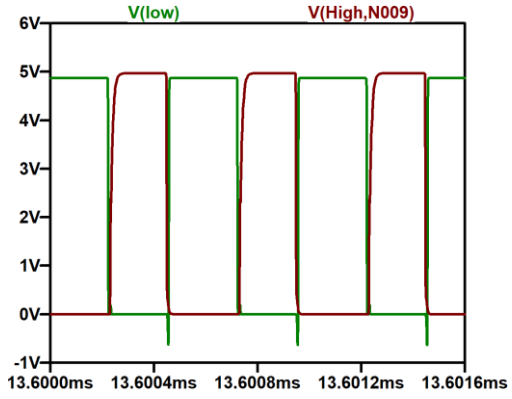

Figure 5: Top gate (red) and bottom gate (green) waveforms of LTC3833 with EPC2014c configured to regulate 12 V to 5 V

The results for the LTC3833 converter, configured to output 3.3 V under similar operating conditions as the 5 V converter, are shown in Fig. 6 – Fig. 8. The output voltage ripple (0.1%) and inductor ripple current

(28.1%) matched closely with the values predicted by the proposed design with a percent error of 5.2%.

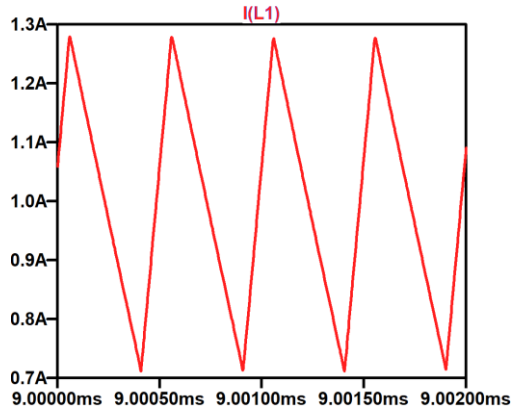

Figure 6: Inductor current ripple of LTC3833 with EPC2014c configured to regulate 12 V to 3.3 V

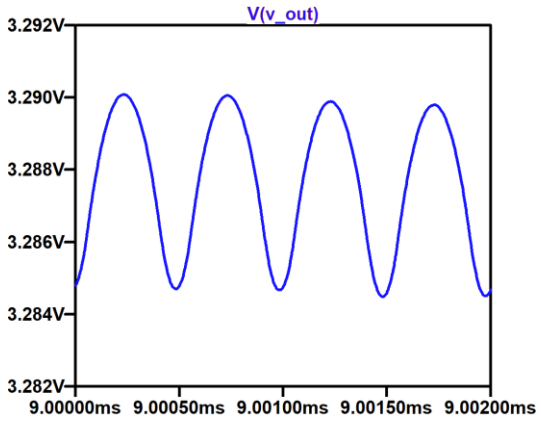

Figure 7: Output voltage ripple of LTC3833 with EPC2014c configured to regulate 12 V to 3.3 V

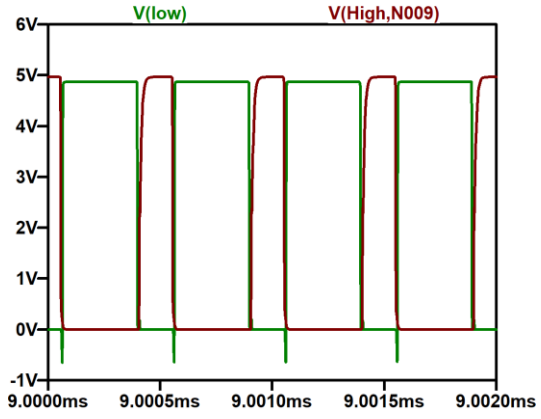

Figure 8: Top gate (red) and bottom gate (green) drive voltage of LTC3833 with EPC2014c configured to regulate 12 V to 3.3 V

Similar results were observed with other controller and GaN HEMT configurations, with the proposed design and simulation data being consistent to within 3% for both LTC3833 and LM25141 controllers.

Converter Hardware Results

The characterization of the proposed test converter PCBs was performed using the test setup shown in Fig. 9. A B&K Precision 9183B DC power supply was configured to output a constant 12 V supply to the converters. An AMETEK SLH series electronic load was programmed to incrementally step converter load current for efficiency measurements. Load currents were verified with a Fluke 115 multimeter that was placed in series with the converters. Oscilloscope measurements on the test converter PCBs were taken with 10x probes on a Tektronix DPO7254 2.5 GHz to ensure minimal distortion of the high-frequency switching signals.

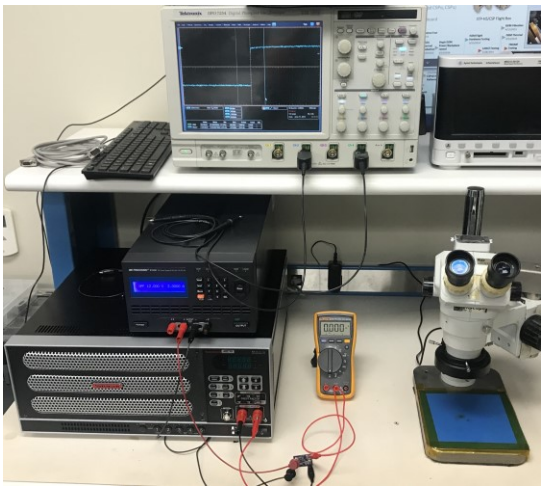

Figure 9: Test setup with AMETEK Electronic Load

Measurements were taken on the LTC3833 converter using EPC2014c GaN HEMTs that was configured to output 3.3 V, and the electronic load was programmed to sink 1 A. The data taken on this converter directly relates to Fig. 10 – Fig. 13 but other converter configurations were found to have comparable waveforms and therefore their plots are omitted. Inductor current measurements were performed differentially across a 0.015 Ω current sense resistor, and an 8 mV voltage drop was measured, corresponding to a 26.7% ripple as seen in Fig. 10. The measured ripple matches within 1.5% of the simulated converter. The output voltage ripple measurements of 13.2 mV were consistent with predicted and simulated results, representing less than 0.5% ripple as seen in Fig. 11. Measurements on the LM25141 controller provided an output voltage ripple less than 1%. If the degree of voltage ripple can be maintained for a 28 V input voltage with only minor component changes, the proposed converters are suitable for use as direct PoL converters for other computational devices, such as processors or FPGAs [12], at lowered efficiency.

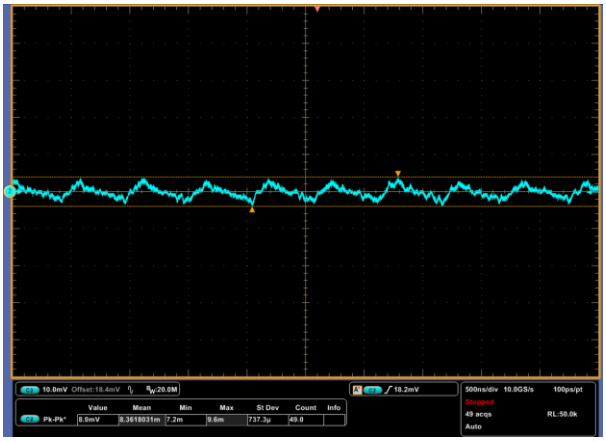

Figure 10: Inductor current oscilloscope waveforms for the LTC3833 with the EPC2014c converter

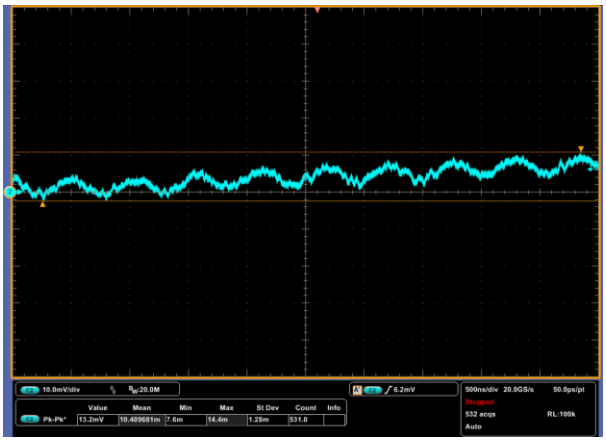

Figure 11: Output voltage oscilloscope waveforms for the LTC3833 with the EPC2014c converter

As discussed previously, the gate of the GaN HEMT is expected to experience some ringing during turn-on and turn-off states, resulting from trace inductance and package parasitics. The gate voltage oscilloscope waveforms in Fig. 12 and Fig. 13 show significant overshoot and undershoot on both the top gate and bottom gate. The 5Ω resistor on the top gate is successful in reducing overshoot, which is of primary concern for the top gate since the source node of the GaN HEMT is connected to the to the controller switching node. The bottom gate is inherently more tolerant to as the source of the GaN HEMT is connecter to ground. A 0 Ω resistor was placed between the controller and the bottom gate to switch the transistor faster. As such, significant ringing was observed on the bottom gate during turn-off. The However, all measured gate voltages are within the tolerances provided by EPC and E2V.

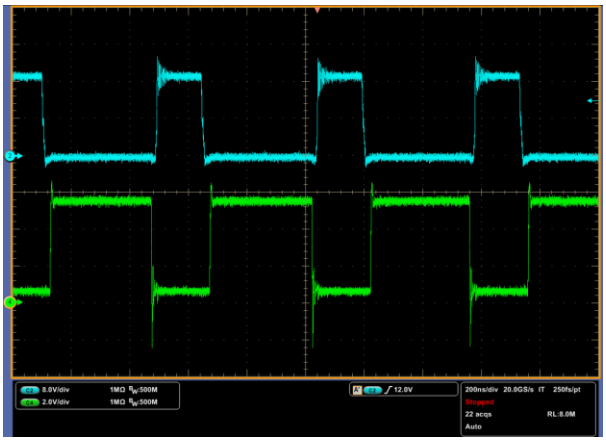

Figure 12: Gate drive oscilloscope waveforms for the LTC3833 with the EPC2014c converter

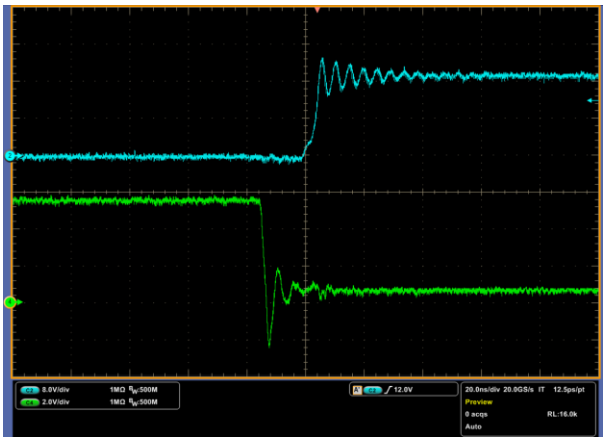

Figure 13: Gate drive oscilloscope waveforms for the LTC3833 with the EPC2014c converter

The 5 V test converters produced consistently high efficiencies ranging from 89% to 96% across the measured load currents seen in Fig. 14 and Fig. 15. As expected, the measured efficiency of the 3.3 V converter was less than the 5 V converter, but measured efficiency values ranged from 72% to 85%. Both 5 V and 3.3 V high frequency GaN HEMT converter topologies performed nearly 20% better than commercially available rad-tolerant converter designed to regulate the same input and output voltages. In both 5 V and 3.3 V converter configurations, the EPC2014c performed consistently better with higher efficiencies when compared to the EVG100E15 and was expected as a result of the hermetically sealed package.

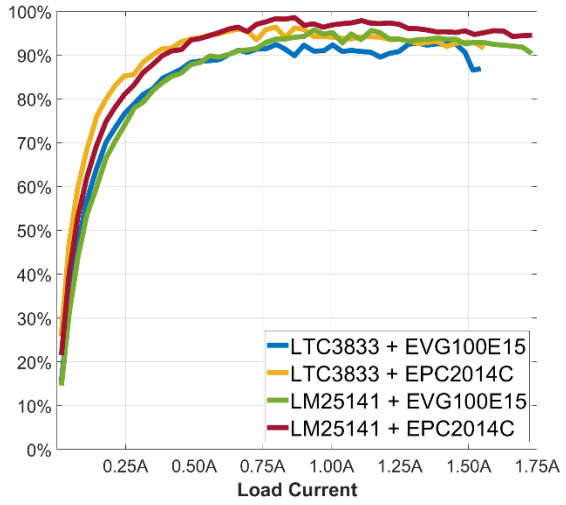

Figure 14: 5 V Test Converter Efficiencies

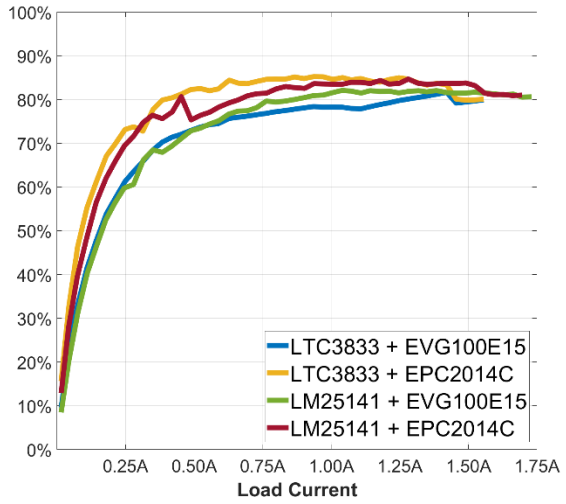

Figure 15: 3.3 V Test Converter Efficiencies

Thermal Performance

High-frequency GaN converters show promise for CubeSat missions in part because of the smaller package dimensions. However, the size reduction can increase thermal stresses placed on components that may negatively impact the rated lifetime, even in the presence of higher efficiencies. Analysis of the converter's steady state thermal performance can provide insight into the expected lifetime of the components. Two of the test converter PCBs with the LM25141 controller were configured to output 3.3 V, and a current was selected on the electronic load. The test converter PCB was allowed to reach a steady state temperature in a controlled lab environment, at which point the peak temperature was measured with a FLIR thermal camera. Analysis of Fig. 16 shows the EVG100E15 test converter performed slightly better than the EPC2014c. This is the result of the larger PCB reuired to accommodate the EVG100E15's ceramic package and the improved thermal transfer of the SMD-0.5 package. The FLIR thermal images show that the GaN HEMTs are dissipating minimal heat in comparison to the LM25141 controller and the inductor.

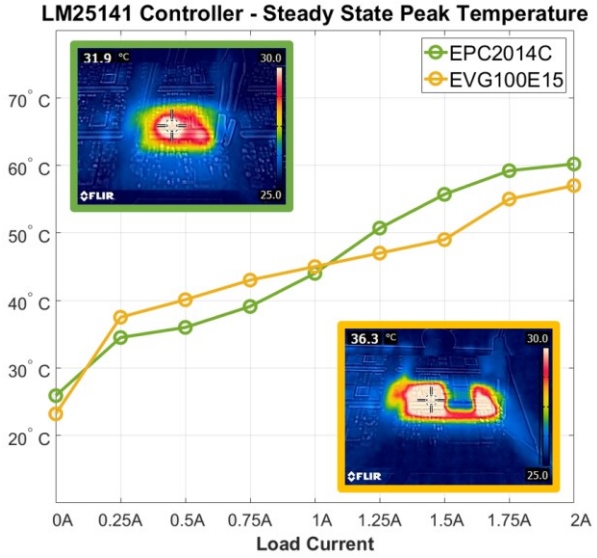

Figure 16: Peak Temperature at Steady State for Texas Instruments LM25141 Converter

STP-H6/SSIVP GAN SUBEXPERIMENT

This section provides a cursory overview of the SSIVP experiment on STP-H6 mission. Additionally, a discussion is presented of the measurement electronics, testbed, and GaN HEMT converters selected for the GaN sub-experiment on STP-H6 SSIVP.

STP-H6/SSIVP Testbed

CSP is a concept for multifaceted hybrid space computing developed by researchers at the NSF Center for Space, High-Performance, and Resilient Computing (SHREC) at the University of Pittsburgh. CSP features a hybrid System-on-Chip (SoC), combining fixed-logic CPU with reconfigurable-logic FPGA. The CSP system combines a hybrid mix of COTS and rad-hard technology, supplemented with fault-tolerant computing. CSPv1 is the first iteration the CSP concept featuring the Xilinx Zynq SoC, which includes dual-core ARM Cortex-A9 processor with 7-Series Artix FPGA [13]. With the success of the STP-H5/CSP mission, the Technology Readiness Level (TRL) of the CSPv1 card was increased to a flight-proven technology (TRL-9) [14]. Building on the technology advancement and lessons learned during the STP-H5 mission, SSIVP provides a supercomputing platform for CubeSat and SmallSat missions , and will launch to the ISS as part of STP-H6 in early 2019 [15]. Designed around the 3U

CubeSat shown in Fig. 17, the SSIVP computing system features five flight-qualified CSPv1 compute nodes that interface with two cameras, one µCSP on Smart Module with the GaN converter experiment, one power card, and a backplane to distribute power and provide an interconnect topology between the computing nodes.

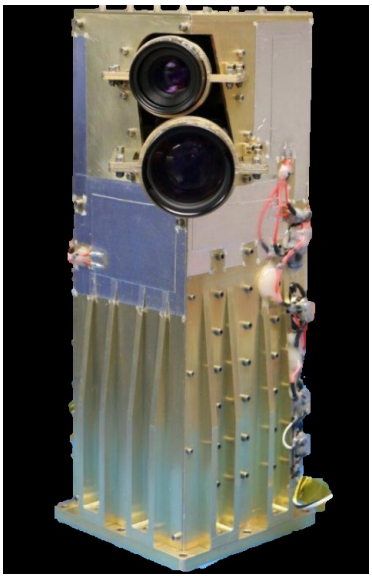

Figure 17: SSIVP assembly for STP-H6

The Smart Modules concept is a framework for rapid development and integration of sensor experiments with networking capability in a reusable form factor. The µCSP is the second realization of the CSP concept designed for a System-on-Module (SoM) development platform with the commercial Microsemi SmartFusion2 hybrid SoC that includes a fixed-logic ARM Cortex-M3 microcontroller with reconfigurable-logic, flash-based FPGA [16]. The µCSP serves as the controller for the smart module providing a data collection interface, sensor processing platform, and a networking interface that reduces experiment integration complexity, all of which is contained in a 1U form-factor. The three GaN converters and corresponding measurement circuitry were integrated onto a Smart Module, as seen in Fig. 18.

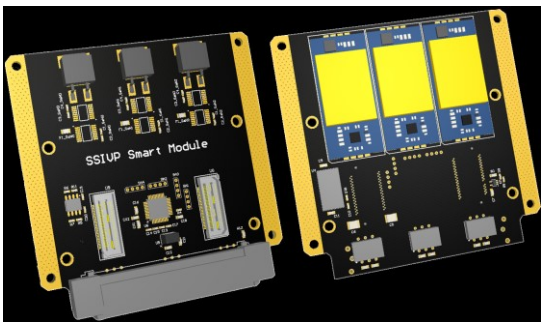

Figure 18: Front (left) and Back (right) of Smart Module with GaN Converters and Load Resistors

The power card is composed of an EMI filter and an isolated rad-hard DC/DC converter to reduce the supplied STP-H6 pallet voltage (28 V) down to the required voltages (12 V, 5 V, and 3.3 V) for the cameras and computing nodes. The reported converter efficiency is approximately 76% when operating over the proposed SSIVP power levels. Due to power and thermal limitations of SSIVP, the GaN experiment and cameras will be multiplexed with solid state relays to enable testing over the course of the multi-year mission. Data collection via the Smart Module will continue throughout the duration of the STP-H6 mission, or until the converters fail from radiation. The SSIVP experiment will be evaluated on the ISS with an altitude ranging from 401.1 km to 408.0 km, and an inclination of 51.64 degrees. The ISS orbital path includes the South Atlantic Anomaly, which will be used to test the converters in a high upset-rate environment and provide valuable data on their reliability in LEO.

GAN Sub-Experiment and Testbed

On the STP-H6/SSIVP mission, three of the PoL synchronous buck converters were selected to fly on a smart module, including two Linear Technologies LTC3833 controllers and one LM25141. The Teledyne e2v EVG100E15 GaN HEMTs were selected to provide a comparison between the known flight-grade components and the ultra-small package. The synchronous buck controllers were designed to regulate 12 V down to 5 V. The flight converters were designed to drive a 4.7 Ω load or 5.25 W.

Table 4: SSIVP GaN Converter Configurations

SSIVP Slot	Controller	GaN HEMT	Switching Frequency
PoL-1	LTC3833	EVG100E15	1.887 MHz
PoL-2	LM25141	EVG100E15	2.212 MHz
PoL-3	LTC3833	EPC2014c	1.887 MHz

The converter configurations in Table 4 were selected to allow for the remote deduction of component failure if it occurs throughout the course of the mission. The hermitically sealed ceramic EVG100E15 GaN HEMT has flight heritage, and extremely stable over a wide temperature range that enables controller testing. With a low probability of failure on the EVG100E15, any in-flight converter failure on PoL-1 or PoL-2 is likely a result of the controller, and not the GaN HEMT. The primary purpose of PoL-3 is to provide flight heritage to the EPC2014c with a secondary task of testing the feasibility and survivability of the ultra-small package.

Each flight converter has isolated measurement circuitry to calculate the DC current and voltage at the input and output for in-flight calculation of efficiency. Individual converters are fused allowing the failure of any converter without impacting the success of the sub-experiment.

FUTURE WORK

STP-H6 is set to launch in early 2019, at which point converter data collection in LEO can begin. There are plans to test both the LTC3833 and LM25141 synchronous buck controllers for SEE and TID to provide a metric of operation in a hash radiation environment. Future testing of the converter is planned with input voltages at 28 V and output voltages from 2.5 V to 1 V, providing coverage across voltages commonly required by FPGA and SoC systems processing systems.

CONCLUSIONS

The benefits and advantages of the proposed controllers with GaN HEMTs are clear when compared to traditional rad-hard converters. The radiation tolerant nature of GaN provide significant cost reduction when compared to traditional rad-tolerant converters. High switching frequency require lower component values with smaller component packages that introduce less loss to the converter. Both combine to produce efficiencies as high as 96% with package areas as small as 0.41 in^2. The in-flight success of the LTC3833 and the LM25141 controllers will provide a low-cost solution for CubeSat missions that costs orders of magnitude less than current offerings.

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References

[1] VPT, “SVRTR2800 Series Space Qualified Hybrid DC-DC Converters,” *Data sheet*, no. 425, pp. 1–15.

[2] G. Longobardi, "*GaN for power devices: Benefits, applications, and normally-off technologies*," 2017 International Semiconductor Conference (CAS), Sinaia, 2017, pp. 11-18.

[3] C. De Santi, M. Meneghini, G. Meneghesso and E. Zanoni, "Review of dynamic effects and reliability of depletion and enhancement GaN HEMTs for power switching applications," *IET Power Electronics,* vol. 11, no. 4, pp. 668-674, 4 10 2018.

[4] He Li, Chengcheng Yao, Lixing Fu, Xuan Zhang and Jin Wang, "Evaluations and applications of GaN HEMTs for power electronics," *2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, Hefei, 2016, pp. 563-569.

[5] F. Schwierz, "The frequency limits of field-effect transistors: MOSFET vs. HEMT," *2008 9th International Conference on Solid-State and Integrated-Circuit Technology*, Beijing, 2008, pp. 1433-1436..

[6] W. J. de Paula et al., "A review on gallium nitride switching power devices and applications," *2017 Brazilian Power Electronics Conference (COBEP)*, Juiz de Fora, 2017, pp. 1-7.

[7] J. Y. Tsao *et al.*, “Ultrawide-Bandgap Semiconductors: Research Opportunities and Challenges,” *Adv. Electron. Mater.*, vol. 4, no. 1, pp. 1–49, 2017.

[8] L. Scheick, “Single-Event Effect Report for EPC Series EPC1012 Single-Event Effect Report for EPC Series NASA Electronic Parts and Packaging (NEPP) Program,” *Natl. Aeronaut. Sp. Adm.*, 2013.

[9] A. Lidow and J. Strydom, “Gallium Nitride (GaN) Technology Overview,” *White Paper WP001*, pp. 1–6, 2012.

[10] D. G. Morrison, “Rad-Hard Power Converters Ride Intermediate Bus Into Space,” *How 2 Power Today*, no. August 2011, pp. 1–8, 2012.

[11] C. Abbate *et al.*, “Developments on DC/DC converters for the LHC experiment upgrades,” *Topical Workshop on Electronics for Particle Physics.*, Perugia, Italy, Sep. 27, 2013.

[12] Hudgins Dennis, “Power Supply Design Considerations,” *Power Des.*, no. 121, pp. 45–65, 2012.

[13] D. Rudolph *et al.*, “SSC14-III-3 CSP: A Multifaceted Hybrid Architecture for Space Computing,” *28th Annu. AIAA/USU Conf. Small Satell.*, Aug. 7, 2014.

[14] C. Wilson *et al.*, “SSC15-III-10 CSP Hybrid Space Computing for STP-H5 / ISEM on ISS,” *29th Annu. AIAA/USU Conf. Small Satell.*, Aug. 13, 2015.

[15] S. Sabogal *et al.*, “SSC17-XIII-02 SSIVP : Spacecraft Supercomputing Experiment for STP-H6,” *30th Annu. AIAA/USU Conf. Small Satell.*, Aug. 11, 2016.

[16] C. Wilson *et al.*, “A Diminutive , Hybrid , Space Processor for Smart Modules and CubeSats,” *30th Annu. AIAA/USU Conf. Small Satell.*, Aug. 11, 2016.