A 10b SAR ADC with an Ultra-Low Power Supply

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***Abstract*—A 0.2V 10-bit 5 kS/s Successive Approximation Register ADC design is presented. This design achieves a very low power consumption due to the ultra-low power supply voltage used. Different aspects in the ADC design are optimized for 0.2V and modified to meet the speed requirements for the ADC. Preliminary Cadence simulations show a 4nW total power consumption with a peak SNDR of 57 dB and a FOM of 1.3 fJ/conversion-step.**

I. Introduction

A. Wireless Sensor Networks in Space-Based Applications

There is an ever-increasing need for wireless sensor networks in different environments. Wireless sensor networks are spatially distributed autonomous sensors that monitor different physical and environmental conditions, such as temperature, sound, and air quality. [1] They cooperatively gather data and then pass the data through a network to a main location to be processed and analyzed. These sensor networks have been successfully used in health care, [2] environmental sensing [3], and military applications including surveillance and reconnaissance. [4] They provide a flexible, cost-efficient alternative to traditional remote monitoring. Instead of manufacturing one large sensor, engineers have been able to create many small, cost-efficient sensors called "nodes" to work together and perform the same function. Wireless sensor networks are composed of these individual sensing nodes that are each made up of one or more microcontrollers, an energy source, a radio transceiver, and electronic circuits interfacing with the sensors and microcontrollers. They are actively being studied for many applications, including use in space exploration.

Wireless sensor networks provide an attractive option for use in space exploration because of their flexibility and low cost of operation. In space, wireless sensor networks could be used for a variety of functions such as: weather monitoring missions in low earth orbit (Figure 1) and missions where the networks are deployed on a planet to monitor the surface conditions. Several space-based applications are currently being researched. Wireless sensor networks could be deployed around a spacecraft on a planet to aid in ground measurements [5]. They could be used on the outside of a spacecraft to check and report hull integrity. [6] Furthermore, they could be distributed in a planetary atmosphere to collect data about the atmospheric conditions. [7]

In order to function effectively in space-based applications, wireless sensor networks need to be able to operate while consuming very low power. [8] Traditional wireless sensor network nodes will need to be modified in order to meet the power requirements of operating in space. One of the most important requirements for the individual sensing nodes is that each consumes as little power as possible. It is critical to the success of wireless sensor network space applications that the networks operate for as long as possible with a given amount of battery power.

Figure 1. An artist's rendition of a wireless sensor network in space monitoring Earth's atmosphere. [7]

B. ADCs in Wireless Sensor Networks

In order to properly digitize signals from the sensor node's environment, each node must contain an Analog-to-Digital Converter (ADC). The ADC takes in an analog input and outputs a digital code that best represents the analog input. This digital data can then be transmitted to a network center, where it can be analyzed and manipulated. Obviously, the stringent power requirements placed on the sensing nodes extend to the ADC. The ADC must consume extremely low power (<10nW) and have a sample rate of 1-5kHz to properly function. We propose a 10-bit ADC that can operate according to these requirements due to an unprecedented lowering in power supply voltage. This 10-bit ADC can operate at 5kHz, which is fast enough for wireless sensing node applications.

II. ADC Design

For our ADC design, we chose to build a Successive Approximation Register (SAR) ADC. The SAR architecture was chosen due to its simplicity and inherent low power consumption. Its basic operation is described in the subsequent section

A. General SAR ADC Architecture

The SAR ADC realizes a binary search algorithm to obtain the digital code that best matches an analog input. An example for a 3-bit SAR ADC is shown in Figure 2, where an analog input voltage (Vin) is converted to an output code. In the first step, the unknown Vin is compared to a reference (Vref) that is initially set to the middle of the ADC range, which is 0 V in this example. As shown in the figure, Vin < Vref, so the first bit is a 0, and the reference is now changed to the middle of the remaining search range. Since we know that Vin is between -1 and 0 V, the new reference is thus set to -0.5 V. In the next cycle, Vin > Vref, so the second bit becomes 1; and, therefore, the reference voltage is now updated to -0.25 V, which again is the middle value of the remaining search range. The third comparison resolves the third and final bit, which is 0, causing the final digital code to be 010.

The circuitry to implement this algorithm requires three main parts. The first is a digital-to-analog converter (DAC) is necessary to produce the reference voltage Vref that is updated depending on the previous bit decisions. Second, a comparator is required to compare Vin to Vref. Finally, logic is needed to time the various operations and to store the attained digital code. Additionally, a sample and hold switch is also required to sample the analog input voltage before holding the value and performing the binary search method. Figure 3 shows a block diagram of a SAR ADC. In this case, rather than comparing Vin against Vref, Vref is subtracted from Vin first, and the comparator simply determines the sign of Vin – Vref, which is identical to comparing Vin against Vref. Typically, the sample and hold is nothing more than a set of switches, and the DAC is composed of a switched-capacitor network, which leads to a straightforward hardware implementation.

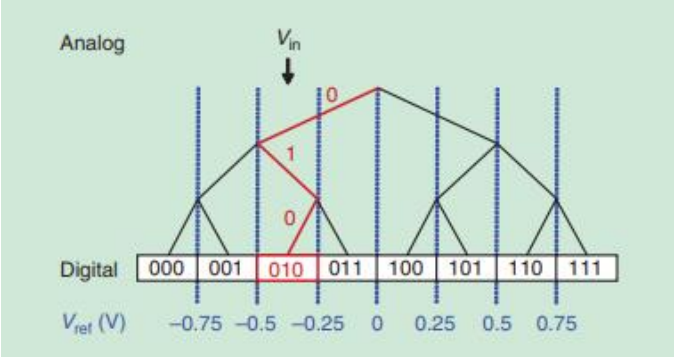

Figure 2. A binary search tree of a 3-bit SAR ADC. [9]

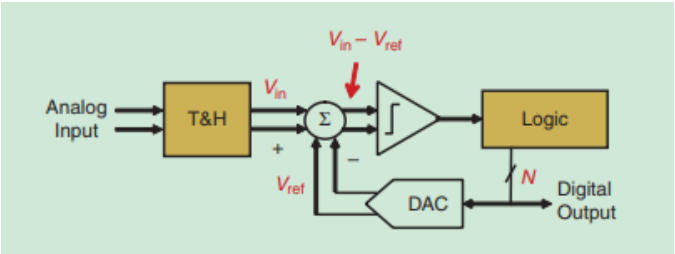

Figure 3. A block diagram of a differential SAR ADC. [9]

B. Proposed SAR ADC Architecture

We chose to design a 10-bit ADC, which provides high accuracy. When the ADC resolution goes beyond 10 bits, the switched-capacitive DAC tends to be limited by capacitor mismatch and has to be sized larger, thus degrading power efficiency. The ADC design is differential, to combat power supply noise. It consists of double bootstrapped sample and hold switches, a switch-capacitor DAC, a dynamic, two-stage comparator, and digital logic. Our SAR

ADC is asynchronous, meaning that it internally generates all required clock signals to operate and only needs a sampling clock input.

C. Lowering the Power Supply Voltage

Many previous designs have taken advantage of the simplicity of the SAR ADC and have successfully used a reduced power supply voltage in an effort to conserve more power. [9-13] The lowest supply voltage these designs have used is 0.3V. In order to reduce power consumption even further, our design uses a power supply of 0.2V, which is unprecedented, especially considering that the nominal supply voltage for the process we use is 1.8V.

D. ADC Design Issues with a 0.2V Power Supply Voltage

Reducing the power supply voltage in the aforementioned manner presents non-trivial problems. With such a low supply, the transistors in the design conduct more than a thousand times less current than with a nominal supply. This results in the comparator and digital logic becoming excruciatingly slow. Additionally the sampling switches do not conduct well enough to track the analog input voltages. To show how poorly conducting transistors can affect a circuit, we consider a digital inverter operating at 1.8V, and the same inverter operating at 0.2V. Table 1 summarizes the performance comparison of the two inverters. It can be easily observed that the speed of an inverter decreases by a factor greater than 30,000. Merely modifying an existing design by changing the voltage supply from 1.8V to 0.2V will not be enough to reduce power and have a circuit that operates fast enough.

VDD (V)	Inverter Delay (ns)
1.8	0.052
0.2	1600

Table 1. Inverter delays with different supply voltages.

An additional requirement that must be considered is noise. The LSB voltage of an ADC can be calculated by EQUATION, which for our design is 0.39mV. Careful steps must be taken to ensure that the noise of the system is not greater than the LSB voltage, or else the accuracy of the design would greatly suffer. In our design, we implement several techniques to mitigate the aforementioned problems and still achieve a sampling rate of 5kS/s. While 5kS/s is still significantly less than what is attainable with a 1.8V supply, it is adequate for the intended space-based applications. The specific techniques are detailed in the following section.

III. Circuit Design

A. Bulk Biasing the Digital Logic

In order to address the aforementioned issue of the slow digital logic, a technique called “bulk biasing” is used. A MOSFET transistor has four terminals—gate, drain, source, and bulk. Typically, circuit designers connect the bulk connection of a PMOS transistor to the supply voltage and the bulk connection of an NMOS transistor to ground. However, changing the typical bulk connection voltages can affect the threshold voltage of the transistor. This is according to the threshold voltage equation for a transistor given by:

$$V_{th} = V_{th0} + \gamma\left(\sqrt{2\Phi_F + V_{SB}} - \sqrt{2\Phi_F}\right) \quad (1)$$

According to (1), if the source-to-bulk voltage of an NMOS transistor is negative (or positive in the case of a PMOS transistor), the threshold voltage of that transistor will decrease. This allows the transistor to draw more current given a fixed gate voltage, which makes for higher digital logic speeds. We can exploit this by biasing the gate voltages of all PMOS transistors at ground and all NMOS transistors at the supply (Figure 4), thus giving lower threshold voltages for all MOSFETs in the digital logic. By means of circuit simulation software (Cadence), it was found that when the MOSFETs are biased in this manner, PMOS transistors draw 3.2 times more current than an NMOS transistor of the same width. Therefore, for equal rise and fall times in the digital logic, the PMOS transistors must be sized 3.2 times greater than the NMOS transistors. In all digital logic blocks, this bulk biasing and new transistor sizing was implemented. The tradeoff for this design is an increase in leakage current, dominated mostly by the PMOS transistors. The transistors were carefully sized so as not to be too large so the leakage current

could be minimized. Table 2 shows the performance comparison of an inverter at 0.2V supply without bulk biasing, and an inverter with bulk biasing and the different transistor sizing.

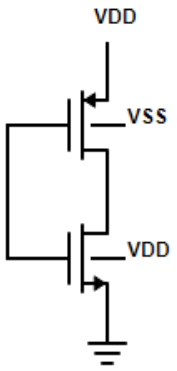

Figure 4. A bulk-biased inverter.

Inverter Type	Delay (us)	Power (pW)
No Bulk Bias	1.6	19.7
Bulk Biased	0.31	21

Table 2. Delay and power consumption comparison of a bulk-biased inverter vs. no bulk biasing

B. Double Bootstrapped Switch

In most modern ADCs, the problem of poorly conduction sampling switches is resolved by bootstrapping the switches. A bootstrapped switch (Figure 5) is a circuit that minimizes the on resistance of a transistor despite large input and output voltage swings. During the sampling phase, switches are turned on so the gate voltage remains a constant VDD. During hold phase, the capacitor is recharged to VDD. Typically, this approach provides enough linearity in the sampling switch so the output tracks the input well. However, at our intended supply of 0.2V, just a single bootstrap is not enough to provide the needed linearity. We need to 'double bootstrap' the switch which adds an additional capacitor. During the hold phase, both capacitors are charged to Vdd. During the sampling phase, the two capacitors are connected in series, thus providing a gate voltage of 2*Vdd. Figure 6 shows the design used to provide the double bootstrapping. This design was simulated in Cadence and the SFDR was measured. The simulated design was able to achieve a SFDR of 94.01dB (Figure 7) thus ensuring that the sampling switches will provide enough sampling linearity for our 10-bit design.

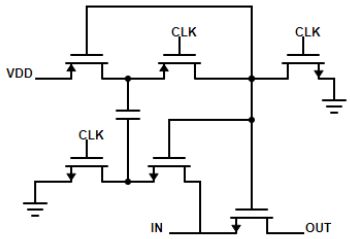

Figure 5. A bootstrapped switch.

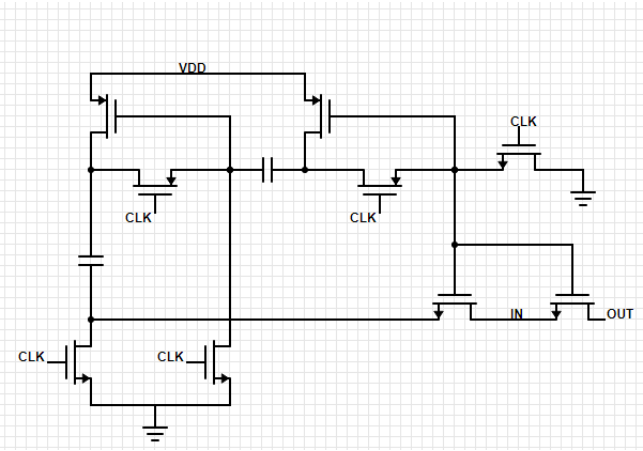

Figure 6. A double bootstrapped switch

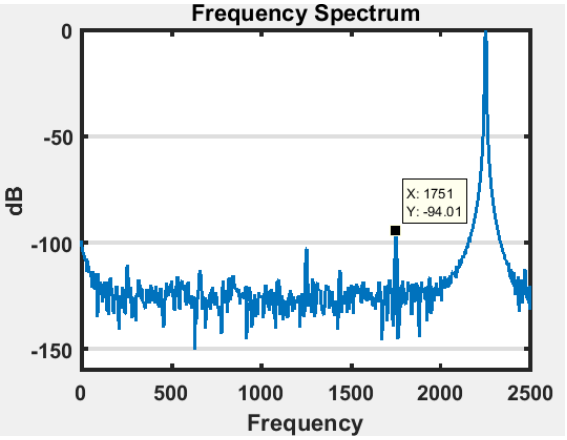

Figure 7. Output spectrum plot of double bootstrapped switch.

C. Dynamic Two-Stage Comparator

A dynamic two-stage comparator is implemented, shown in Figure 8. The first stage is a voltage amplification stage with VIN and VIP as differential inputs and AN and AP as differential outputs. The second stage consists of both a voltage amplifier and a positive feedback regeneration latch to obtain a rail-to-rail digital outputs (OUTN and OUTP). Before comparison, the first stage output nodes are pre-charged to a high voltage while the second stage output nodes are pre-charged low.

When there is a rising clock edge, the pre-charging ceases and Nodes AP and AN discharge towards ground. As they discharge, the PMOS second stage inputs slowly turn on and activate the latch. The difference in inputs is amplified by the two stages and then the latch takes over and provides a rail-to-rail output. At a 0.2V supply, this comparator's delay is too slow for our targeted frequency. Bulk biasing was implemented on the first and second comparator stages to increase comparison time to 7us.

In the comparator design, noise must also be considered because the comparator is one of the main noise sources in the whole ADC. The comparator noise level must be kept below the LSB voltage level for proper operation, and should be further lowered to obtain good signal to noise ratio. The overall noise of the comparator is mostly dependent on the noise of the first stage, which is inversely proportional to the Gm of the input transistors. A full analysis of this type of comparator's noise is explained in [14]. In order to reduce comparator noise in our design, the bulk connections of the input transistors of the second stage are connected to the comparator inputs. This technique increases the overall Gm of the circuit, which decreases the noise level of the comparator.

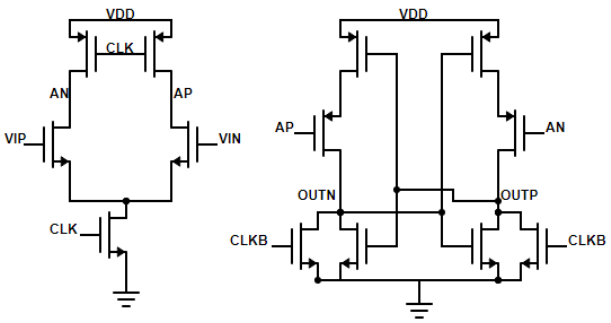

Figure 8. A dynamic, two-stage comparator.

IV. Simulation Results

The proposed 10 bit differential SAR ADC is designed using a 0.18 um CMOS process. The design is currently being simulated and verified in Cadence. Simulations have been run to extract the SNDR and SFDR with and without transient noise. Without noise, the SNDR is 61.5dB (Figure 9). With noise, the SNDR drops to 57dB. The ADC consumes 4.2nW of power while operating at 5kS/s. Calculating Walden's figure of merit for our circuit yields a power efficiency of 1.3fJ/conversion-step

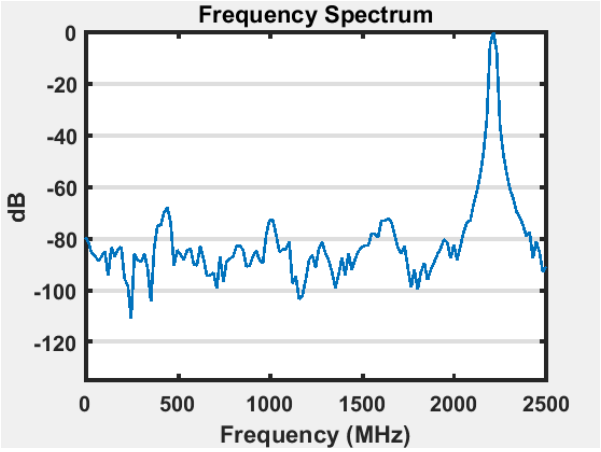

Figure 9. Output Spectrum of ADC

V. Conclusion and Future Work

This paper has discussed a 10 bit 0.18um CMOS SAR ADC for use in a distributed wireless sensor network in space. By using a 0.2V supply voltage, asynchronous dynamic logic, and low-complexity design, an energy efficiency of 1.3 fJ/conversion-step could be achieved at 5kS/s in preliminary Cadence simulations. The future research that needs to be done is design work and simulations with the intent of further increasing noise immunity. The static properties of the ADC (INL and DNL) need to be characterized. Additionally, redundancy [something] should be added to the DAC to decrease sensitivity to parasitic capacitance. The design will be laid out and fabricated so we can test it on a chip. We expect to have our design fully fabricated and tested by Spring 2019.

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