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A Discrete-Time Technique for Linearity Enhancement of Wideband Receivers

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A DISCRETE-TIME TECHNIQUE FOR LINEARITY ENHANCEMENT OF WIDEBAND RECEIVERS

A Dissertation Presented

by

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DEDICATION

To my parents, Fatemeh and Ahmad, who dedicated their lives to their children's success, my two inspirational sisters, Fereshteh and Saeedeh , and my wife, my friend, and my colleague, Shirin.

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ABSTRACT

A DISCRETE-TIME TECHNIQUE FOR LINEARITY ENHANCEMENT OF WIDEBAND RECEIVERS

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A new signal processing technique is introduced to enhance the linearity performance of wideband radio frequency (RF) receivers. The proposed technique combines the advancements in mixer first architectures with a library of binary sequences as local oscillator signals to enable wide instantaneous bandwidth and high linearity for the RF receiver. To do so, N-bit pseudo-random-binary-sequences (PRBS) are used as local oscillator signals. The RF input signal is multiplied with the PRBS at the mixer and then averaged over the full sequence. This in effect reduces the amplitude of the signal and improves the overall linearity of the system. In order to enable full reconstruction of the input signal N channels are used with each employing a shifted version of a PRBS.

The effect of the proposed technique on different aspects of the system performance such as noise and linearity is discussed. In addition, the effect of nonidealities

stemming from hardware implementation on the overall performance are studied. A prototype integrated circuit (IC) is implemented in 130 nm CMOS technology to demonstrate the feasibility of the proposed technique. The design procedure of each circuit block is described and simulation results are used to evaluate the performance. The device is fabricated and characterized using a custom data acquisition system. Measurement results show good agreement with the expected values from simulation and analytical analysis.

Calibration techniques are introduced to minimize the effect of DC offsets, gain mismatches, and timing skews. Modifications to the implemented CMOS circuit are proposed to enable such calibrations and further enhance the overall performance of the system. The requirements for the precision of calibration techniques are derived and used to find the specifications of circuit block that are designed to enable these techniques. Calibration of DC offsets along with gain mismatches is carried out for the fabricated IC and results are shown. A digitally assisted technique is proposed to enable the calibration of timing skews. In addition, a review of additional implementation shortcomings that can affect the system performance are reviewed. Finally, a conclusion of the dissertation is presented along with potential future work for further enhancement of the system performance.

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CHAPTER 1

INTRODUCTION

This dissertation is focused on the development of a novel discrete-time technique to enhance the linearity of wideband radio frequency (RF) receivers. The effect of the proposed technique on different RF receiver performance metrics is studied and discussed. The dissertation is organized as follows:

1. **Motivation and current state-of-the-art wideband receivers**(Chapter 1)– The recent growing demand for wideband receivers is discussed and some of the challenges associated with these systems are described. Some examples of available techniques to mitigate these challenges are reviewed and their advantages and shortcoming are discussed.

2. **Theory** (Chapters 2, 3)– The discrete-time RF signal-processing technique is introduced and a matrix representation of the overall system is described to further demonstrate the operating principles of the proposed technique. Using both analytical and numerical solutions, the effect of the proposed technique on different aspects of the receiver performance is studied. In addition, the effect of nonidealities that would arise with system implementation on silicon integrated circuit (IC) is studied.

3. **Implementation** (Chapter 4)– The implementation of a prototype CMOS IC to evaluate the performance of the proposed technique is presented. Different design considerations for the implementation are discussed. Computer aided simulations are used to evaluate the performance of the design.

4. **Measurement Results and Discussion** (Chapter 5)– The measurement results of the fabricated IC in 130nm CMOS technology are reported. The measurement setup and the reconstruction procedure are described in detail and limitations on performance due to the setup are discussed. The basic operation of the system is evaluated with time domain measurements. Then several measurement results are used to evaluate linearity and noise performance of the system. It will be shown that nonidealities in the system limit the spurious free dynamic range (SFDR) of the system and appropriate techniques are required to reduce their effect.

5. **Calibration Techniques to Enhance System Performance** (Chapter 6)– Several techniques that can be used to reduce the effect of mismatches are proposed. The circuit implementation of these techniques is also presented. Some of these techniques are implemented on the CMOS IC of Chapter 4 and measurement results are shown to discuss the effect of calibration.

1.1 High Data Rate Communication Systems

As technology becomes more integrated with every aspect of daily life, more and more electronic devices are used that require wireless connection. New applications such as internet-of-things (IoT), smart cars and wearable electronics are expected to increase the number of wireless connected devices to more than 1000 times the current number by the year 2020 [1]. This large increase in the number of users along with already limited frequency spectrum has become a big challenge in development of the next generation of communication devices such as fifth generation mobile networks (5G).

In addition to larger number of users, higher data rates required for many of new applications, such as high resolution video streaming, has created significant demand for communication systems with wider instantaneous bandwidth. One early example

Table 1.1. Examples of frequency bands used for 2G,3G and 4G applications. Reproduced from [2] ©IEEE 2013. The narrowband nature of all bands should be noted.

Band	Uplink (MHz)	Downlink (MHz)	Signal Bandwidth (MHz)
700MHz	746–763	776–793	1.25–10
AWS	1710–1755	2110–2155	2.5–15
IMT Extension	2500–2570	2620–2690	2.5–20
GSM 900	880–915	925–960	1.25–5
UMTS Core	1920–1980	2110–2170	5–10
GSM 1800	1710–1785	1805–1880	1.25–5
PCS 1900	1850–1910	1930–1990	1.25–5
Cellular 850	824–849	869–894	1.25–5
Digital Dividend	470–854	470–854	1.25–20

that can highlight the importance of wideband signal operation in recent years is the allocation of frequency band between 3.1-10.6 GHz by FCC for the unlicensed use of ultra-wideband (UWB) in 2002 [3]. Ultra-wideband is defined as signals with bandwidth larger than 500 MHz. This at the time was the largest allocation of spectrum by FCC in history which illustrates the preceived importance of growing wideband applications in the past decade [4]. Since then, wideband orthogonal frequency division multiplexing (OFDM) systems that operate in the allocated band have provided data rates of 53.3-480 Mbps [5]. These data rates along with predicted data rates of 100Mbps predicted for 5G [6] applications when compared to those of traditional cellular standard (shown in Table 1.1), show significant shift towards higher bandwidth systems.

As a result, future generanios of wireless devices face two major challenges: the increased number of users in the already dense spectrum spaces and the higher data transfer rates. The capacity of a communication channel (C) with a fixed bandwidth (B) and signal to noise ratio (SNR) performance can be found using the Shannon-Hartley theorem as

$$C = B \log_2(1 + SNR). \tag{1.1}$$

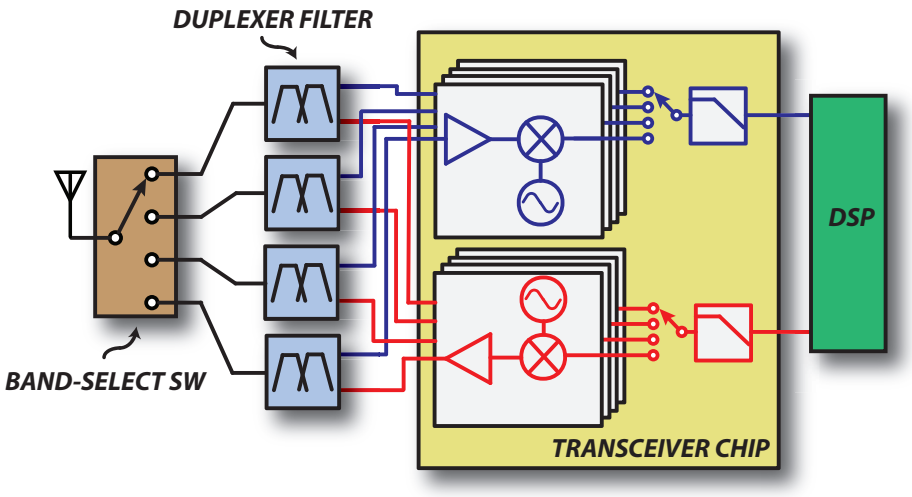

Figure 1.1. Conceptual schematic diagram of a traditional multi-carrier multi-mode cellular modem.

Thus the signal capacity an be significantly enhanced for wider channel bandwidths. Several proposals have been introduced to address this issue such as the use of higher unallocated frequency bands, such as mm-Wave frequency range, and more efficient communication channels. The former has gained a lot of attention specially for the prospect of 5G where multiple mm-wave bands have been considered as potential candidates [6]. The latter is focused on addressing the issue of low utilization of already allocated frequency spectrum. One way of increasing utilization is to employ cognitive radios that scan the spectrum and exploit any unused frequency band [7]. Another technique is to employ carrier aggregation (CA) which uses two or more adjacent (intra-band) or none-adjacent (inter-band) channels for the transmission of wideband data [8–10].

Traditional wireless communication systems are designed to transmit and receive in specific frequency bands that are limited in bandwidth. An example of such systems is current cellphone devices. These devices use multiple off-chip duplexers that are each tuned to a specific carrier frequency to eliminate unwanted signals out of the band of interest. A conceptual example of such system is illustrated in Fig. 1.1.

However, development of advanced communication systems, such as cognitive radios, requires the ability to communicate over a wide frequency range. The large number of duplexers and switches to enable such operation using traditional systems increases the loss and form factor of these devices beyond what is acceptable for current devices [11]. An alternative approach is to use advanced wireless devices such as software-defined-radios (SDR) that, unlike the traditional receivers, are capable of receiving multiple channels and multiple standards by adapting themselves [12–14]. Such systems require receivers that operate with large bandwidths and a processing block that controls the receiver. There are several challenges that are associated with such wideband devices that will be discussed next.

1.2 Challenges Associated with Wideband Receivers

At each instance of time many different signals that differ in frequency, bandwidth and power occupy different portions of the frequency spectrum received by a given device. In addition, the spectral content significantly changes from location to location. Thus the desired message signal for a specific communication device may be accompanied by large blocker signals with small frequency offsets. Hence, a wideband receiver that does not incorporate off-chip high quality factor (Q) filtering would be susceptible to large blocker signals. These large blocker signals can be from other users or even from the transmitter path of the same device. This puts stringent requirements on the receiver dynamic range. Prior to further discussion of challenges associated with these requirements, some fundamental concepts of radio frequency (RF) receivers will be reviewed.

1.2.1 Sensitivity and dynamic range of RF receivers

Two of the main performance metrics of a RF receiver are the noise performance and linearity. There are several metrics set by each communication standard that

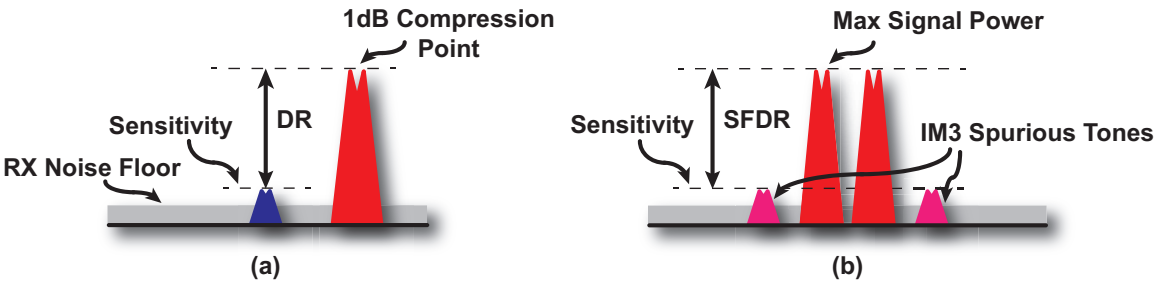

Figure 1.2. Illustration of (a) dynamic range definition and (b) spurious free dynamic range (SFDR) definition [15].

define the required performance of a receiver. These metric specifications are derived based on several factors such as neighboring channels, self interference and modulation scheme. Two of the general specifications that are used to quantify the desired receiver performance are dynamic range and sensitivity.

Sensitivity can be defined as the lowest signal power that can be received with the desired signal-to-noise-ratio [15]. For a system operating at room temperature (300 K) and connected to a 50 Ω antenna, the sensitivity (S_{n}) in dBm can be written as

$$S_{\mathrm{n}}(dBm) = -174(\mathrm{dBm/Hz}) + NF(dB) + SNR(dB) + 10\log_{10}(BW)(dBHz), \quad (1.2)$$

where -174 dBm/Hz is the noise floor due to the receiver thermal noise, NF is the noise figure of the receiver in dB, SNR is the desired signal to noise ratio in dB desired for a particular modulation and coding scheme, and BW is the bandwidth of the receiver in Hz.

Simply put, the dynamic range is defined as the difference between the power of the largest input signal that can be received with tolerable distortion and the sensitivity level. There are two definitions of dynamic range that are typically used in RF designs. The first one is simply called the dynamic range (DR) which is the difference between the 1 dB compression point and the sensitivity level (as illustrated

in Fig. 1.2(a)). The second one is called the spurious-free-dynamic-range (SFDR) and is defined as the difference between sensitivity level and the power of the largest input signal that can be received before any spurious tones due to non-linearity raise above the sensitivity level (as illustrated in Fig. 1.2(b)). Throughout this document the latter definition is used for SFDR.

Depending on the communication standard used, specifications for these metrics may become challenging to meet for wideband receivers with no upfront filtering. For instance the GSM standard requires the receiver to withstand a 0 dBm blocker at 20 MHz offset while maintaining -99 dBm sensitivity level at 200 kHz bandwidth [16]. This requires the receiver to achieve a dynamic range of close to 100 dB. Traditional devices, such as the one showed in Fig. 1.1, employed the rejection provided by off-chip filters (duplexers) to relax this requirement. For every dB of blocker rejection provided by the filter, the dynamic range requirement on the receiver chain is relaxed by 1 dB. However, for a wideband receiver system that does not incorporate any off-chip filtering the full dynamic range requirement should be met. This has been the topic of significant research in recent years and many different approaches have been developed and demonstrated to address this issue. Next, some of these approaches are introduced and reviewed.

1.2.2 Methods for Implementing High Dynamic Range Wideband Receivers

Efforts to address the issue of large required dynamic range of receivers can be generally divided into two categories. The first is to focus on mimicking the filter response of off-chip components with on-chip filtering techniques. Second is to develop new techniques to enhance the dynamic range of wideband receivers to meet the stringent requirements.

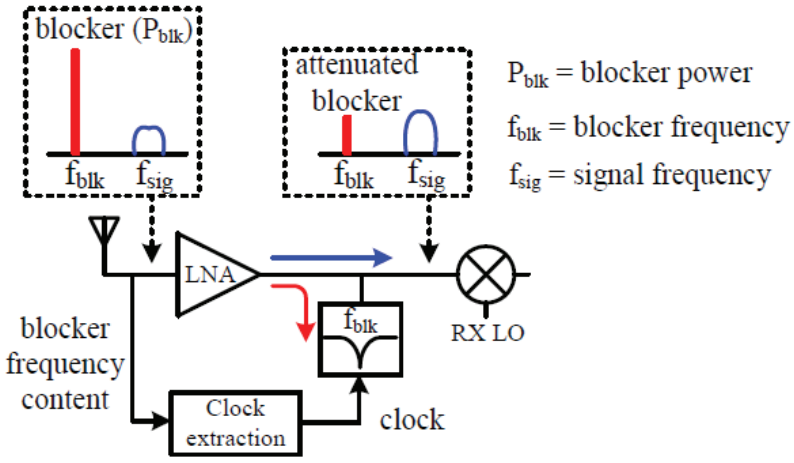

Figure 1.3. An example of a blocker filtering scheme that incorporates the power of a large blocker to tune a notch filter for providing rejection. Reproduced from [17] ©IEEE 2016.

The first approach mainly focuses on developing programmable filtering in order to relax the required dynamic range due to out-of-band blockers by creating narro-band responses [11, 16–25]. An example of such systems is shown in Fig. 1.3. These approaches have been proved highly effective in achieving similar levels of out-of-band rejection to those of traditional receivers. However, they are only effective for signals with small fractional instantaneous bandwidth with all having fractional bandwidths less 15% and mostly less than 1%. This is due to the inherent narrowband response created by the filtering implemented in these receivers. Although these techniques address some of the new applications such as carrier aggregation where narrowband signals are used with programmable center frequencies, they fail to address the need for high data rate communications where signal bandwidths of greater that 100 MHz are required.

The second approach has focused on enhancing the in-band dynamic range of receivers through different techniques to avoid narrow-band responses and accomodate wide-instantaneous bandwidths [5, 26, 27]. The block diagram of an example of such receivers is shown in Fig. 1.4. One of the challenges that these approaches face, other

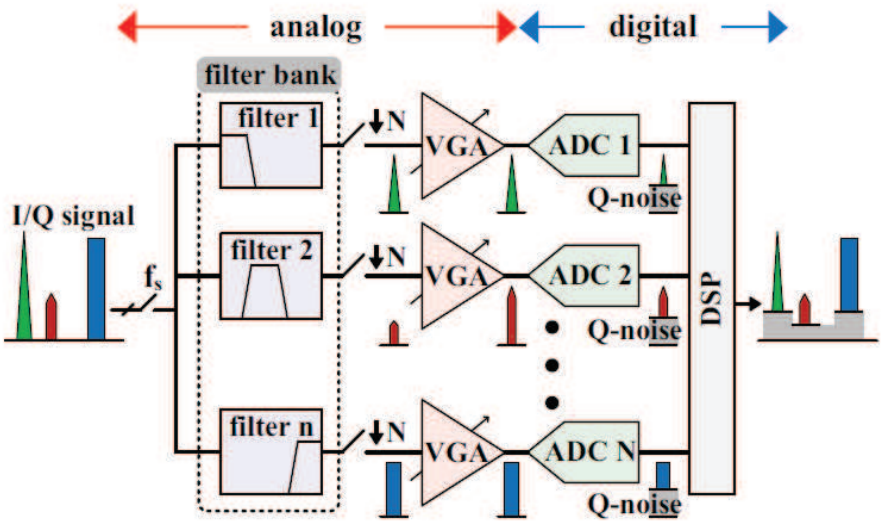

Figure 1.4. An example of a wideband receiver where polyphase filtering is used for channelizing RF band. Reproduced from [26] ©IEEE 2017.

than large dynamic range, is the high speed analog-to-digital converter required for sampling at such high rates. In the system shown in Fig.1.4, the requirement on ADC performance is realxed by downsampling the signal at each channel. While a simple high-speed ADC could be potentially used for direct sampling of the RF signal, it has been proven difficult to achieve the required DR at reasonable power consumption [26]. Next, some examples of techniques implemented for both approaches are discussed.

1.3 State-Of-The-Art High Dynamic Range Wideband Receivers

In this section a review of current state-of-the-art high dynamic range receivers is presented. Several techniques have been demonstrated to enhance the linearity of individual blocks in the receiver chain such as LNA and mixer but the focus of this section is on the system level approaches proposed to enhance the overall dynamic range. Some of these techniques include passive mixer first [28], N-path filters [11, 16,

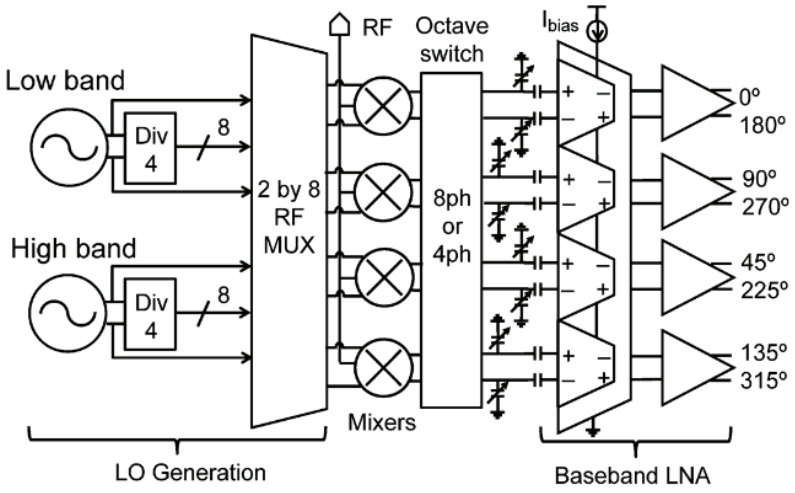

Figure 1.5. Schematic diagram of the multiphase passive mixer phase receiver for low power and high linearity applications. Reproduced from [28] ©IEEE 2013.

21,25], $\Delta-\Sigma$ techniques [18], blocker detection [5,17,24,29,30], RF channelization [26] and RF sampling ADCs [31]. Some of these techniques will be discussed here.

- **Mixer first receivers**– Traditionally, low noise amplifiers (LNA) have been used as the first block of the receiver chain to provide sufficient gain and low noise performance. However, recent advancements in CMOS technology have enabled the use of passive mixers connected directly to the antenna. One advantage of this approach is the high linearity and wideband operation of these devices [28]. An example of a passive mixer first receiver is the work reported in [28], where a multiphase local oscillator (LO) is used to achieve low noise and sufficient out-of-band linearity. The block diagram of the receiver is shown in Fig. 1.5. The multiphase LO is mainly used to implement harmonic rejection mixing (HRM) which allows for rejection of LO harmonics by correctly weighting different LO phases. This is crucial since any blocker signal at harmonics of the LO would be downconverted to the same baseband frequency [28,32,33].

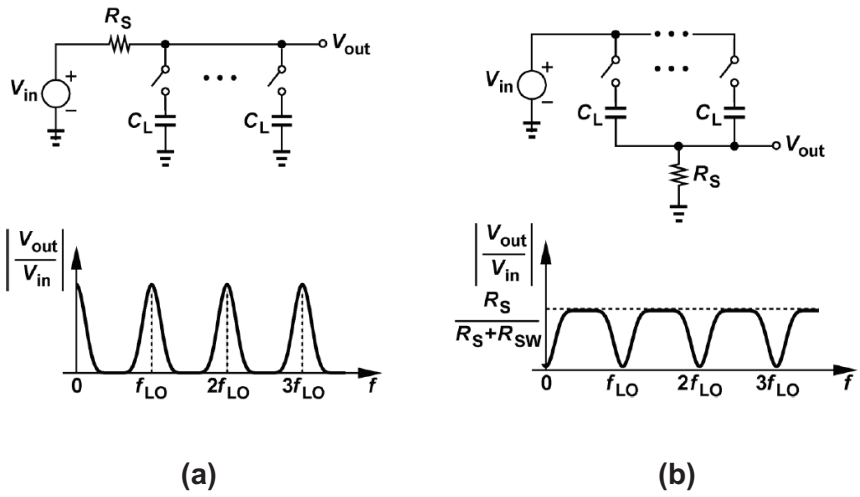

Figure 1.6. Example of N-path filters used to implement (a) bandpass response and (b) notch response. Reproduced from [16] ©IEEE 2014.

- **N-path filters**– One of the most promising approaches to mimic the filtering response of off-chip filters is the use of N-path filters [34]. These filters usually employ multiple parallel branches of switched-capacitor combinations that are controlled with non-overlapping clocks. The passband shape is set by the number of phases and the center frequency of the filter can be tuned effectively without degrading the Q [35]. Fig. 1.3 shows simple N-path filters used to create bandpass and notch filters. As reported in [35] these filters can achieve out-of-band rejections of up to 60 dB. As a result there has been significant research devoted to the use of these filters for eliminating the need of off-chip filters. However these architectures fail to address the need for wide instantaneous bandwidth and the challenge of high in-band linearity.

- **Blocker detection and rejection**– Another approach that has been proven effective, is to employ the knowledge of a blocker to effectively reject it. In [5,17] the blocker signal is detected through an auxiliary path and then used to tune an N-path notch filter and reject the blocker at the output of the LNA. An

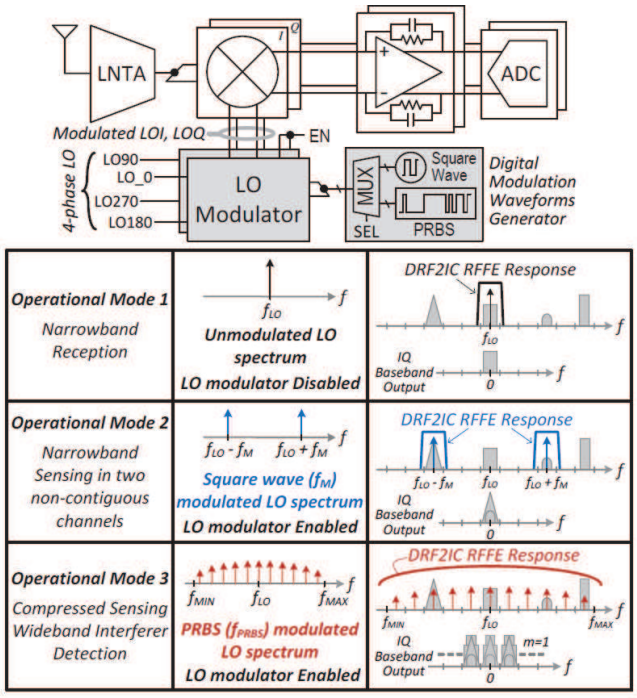

Figure 1.7. System diagram of a wideband compressive sensing based receiver with blocker rejection. Reproduced from [29] ©IEEE 2017.

innovative approach is presented in [30], where an auxiliary path parallel to the main RX path is implented with lower gain to enable detection of any possible nonlinearity. If any nonlinearity is detected, this information is used in digital domain to linearize the signal received from the main path. In [24, 29] compressive sensing techniques are used for detection of any large blockers across the band and then digital techniques such as sequence design and LO modulation are used to reject the band where blocker exists(as demonstrated in Fig. 1.7). These methods have been able to achieve large instantaneous bandwidths of up to 1 GHz. However, they are limited in the number of blockers and their bandwidth.

- **RF channelization**– An approach presented in [26] employs polyphase FFT filtering to create bandpass filter responses and hence channelize the entire frequency band. The operation principle of the PFFT is demonstrated in Fig. 1.8.

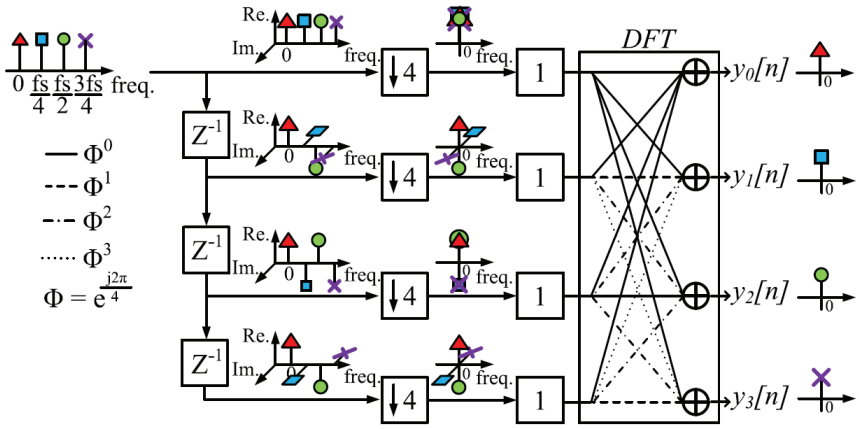

Figure 1.8. Operating principle of the polyphase-FFT. Reproduced from [26] ©IEEE 2017.

In this work a four channel implementation is used which divides the entire spectrum into four effective bands. While this implementation achieves large in-band linearity for each band, the noise performance of the system is high which is due to the complete passive implementation of the system. In addition, any in-band blockers pass through the system and can compress the corresponding channel.

- **RF Sampling ADCs**– As discussed previously, direct sampling of RF signals with an ADC and achieving the required DR has proved to be power inefficient. However, techniques such as time-interleaving have helped achieving higher effective data rates while employing ADCs with lower sampling frequencies [36]. While these ADCs can achieve data rates of higher than 12 GS/s [37], their low effective number of bits (ENOB) limits their use as a direct RF sampling receiver. As an instance the work reported in [37] achieves a 5-bit resolution which corresponds to an effective noise figure of approximately 46 dB. This is much higher than the requirement for most wireless standard which usually require the receiver noise figure to be less than 10 dB. An alternative approach is to use a broadband LNA prior to the ADC to enhance the sensitivity of the overall

Table 1.2. Example of wideband receivers with no off-chip filtering

Reference	Technique	Wide/Narrow Inst. BW	In/Out-of-Band Linearity	Maximum No. of Blockers rejected
[28]	Mixer first	NB	OB	unlimited
[32]	Mixer first	NB	OB	unlimited
[35]	Active N-path filter	NB	OB	unlimited
[25]	Passive N-path filter	NB	OB	unlimited
[16]	Passive N-path filter	NB	OB	unlimited
[11]	Active N-path filter	NB	OB	unlimited
[17]	Blocker detect+N-path	WB	OB	limited
[5]	Blocker detect+N-path	WB	OB	limited
[30]	Blocker detect+dig. proc.	NB	IB	unlimited
[29]	Blocker detect+ CS.	WB	IB	limited
[24]	Blocker detect+CS	WB	IB	limited
[26]	RF Channelization	WB	OB	unlimited
[31]	WB LNA+ RF ADC	WB	IB	unlimited

receiver as presented in [31]. In this work a BiCMOS wideband LNA is used in front of a CMOS 2.7 GS/s ADC. While achieving good SFDR performance the use of two separate integrated circuits implemented in different technologies makes this approach unsuitable for highly integrated devices.

Table 1.2 presents example of state-of-the-art wideband receivers with no off-chip filtering along with the main technique used, the effective instantaneous bandwidth, high in-band or out-of-band linearity, and the fundamental number of blockers that can be rejected. It can be seen that very few efforts have addressed the need for high in-band linearity for wide instantaneous bandwidth receivers with presence of multiple blockers.

Based on the discussion presented here the need for new receiver architectures that enable wider instantaneous bandwidths and better in-band blocker tolerance is evident. In this dissertation a new analog technique will be introduced which focuses on achieving wide instantaneous bandwidth along with high in-band linearity.

1.4 Contributions of this Work

The work reported in this dissertation provides several contributions to the field of radio frequency integrated circuits. These contributions include:

- Introduction of a new technique that combines the benefits of mixer first receivers with library of pseudo random binary sequences to enhance linearity of wideband RF receivers. A detailed analysis on the effect of the proposed technique on system noise and linearity performance is presented to highlight the effectiveness of the proposed method. In addition, the effect of systematic errors due to non-ideal implementation on system performance are discussed and evaluated.

- To evaluate the effectiveness of the proposed technique a CMOS integrated circuit implementation of the system is presented. The design procedure for passive mixers, switched-capacitor block, and baseband amplifiers required for system implementation are each discussed in detail. A custom built data collection system is use for measurements of the fabricated IC. In addition, calibration techniques are introduced to enhance the overall performance of the implemented systems. Circuit implementation of the proposed calibration schemes are presented. Some of the techniques are implemented on-chip and evaluated through measurement results.

The work reported in this dissertation has resulted in a filed US patent for the original idea and a peer reviewed journal paper that presents the main idea along with measurement results of the implemented IC [38].

List of publications during the PhD studies:

- S. Pi, M. Ghadiri-Sadrabadi, J.C. Bardin, and Q. Xia, Nanoscale memristive radiofrequency switches. Nature Communications 6, 7519 (2015).

- S. Pi, M. Ghadiri-Sadrabadi, J. C. Bardin, and Q. Xia, "Memristors as radiofrequency switches," 2016 IEEE International Symposium on Circuits and Systems (ISCAS), Montreal, QC, 2016, pp. 377-380.

- M. Ghadiri-Sadrabadi and J. C. Bardin, "A Discrete-Time RF Signal-Processing Technique for Blocker-Tolerant Receivers With Wide Instantaneous Bandwidth," in IEEE Transactions on Circuits and Systems I: Regular Papers. doi: 10.1109/TCSI.2018.2842

CHAPTER 2

THE PROPOSED DISCRETE-TIME TECHNIQUE

In this chapter, a novel RF discrete-time signal-processing technique for linearity enhancement of wideband RF receivers is introduced. A multi-channel receiver architecture is presented to implement the proposed technique. Fundamentals of system operation are discussed in both time and frequency domain. In this technique, linearity advantages of mixer first architectures are combined with properties of pseudo-random binary sequences as local oscillator signals to achieve high linearity. A matrix representation is introduced to simplify the understanding of the system operation. In addition, analytical and numerical approaches are used for the analysis of linearity and noise performance of the overall system.

2.1 Discrete-Time Signal-Processing Technique

A top level block diagram of the proposed architecture is shown in Fig. 2.1(a). A multi-channel system is used where each channel multiplies the RF input signal ($x(t)$) with a shifted version of a pseudo-random-bit-sequence (PRBS) (P_{i}). A review of PRBS properties is presented in Appendix A. The resulting signal is then averaged over a full period of the PRBS and then sampled, generating $y_i[m]$. These samples are updated after each period of the PRBS which results in y_i signals to be N times slower than the rate of PRBS signals. This, effectively decimates the input signal rate to a lower frequency of $f_{\mathrm{BB}} = f_{\mathrm{s}/N}$. Fig. 2.1(b)-(d) shows the time domain signals at different stages of the system for an example input signal. The lower speed of

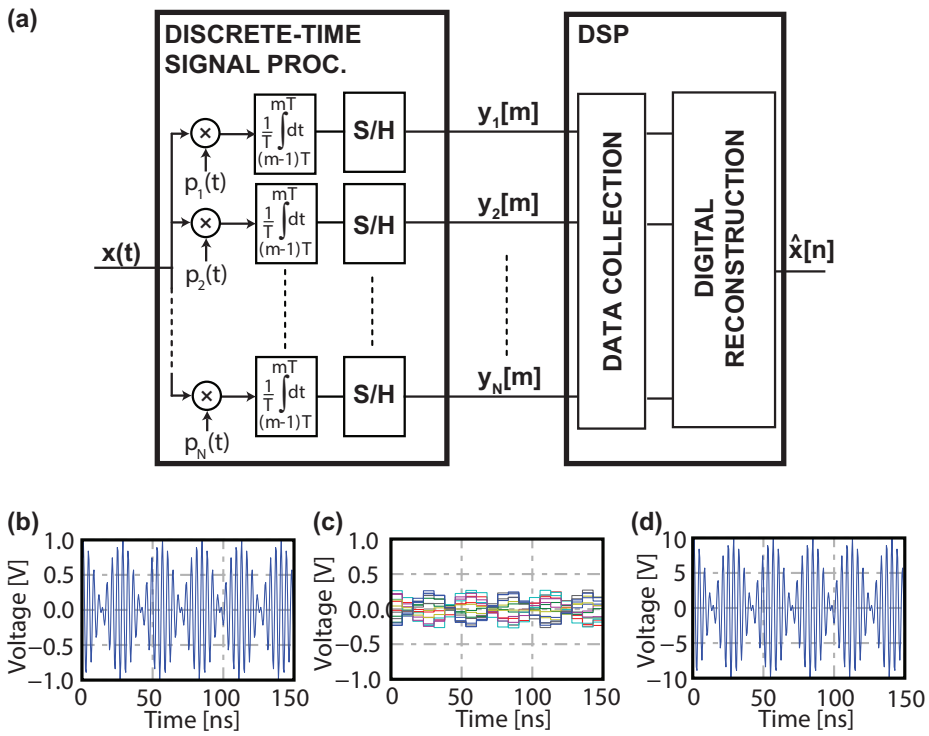

Figure 2.1. (a) Schematic diagram of the proposed discrete-time signal-processing technique along with the digital signal processing block required for collection of samples and reconstruction of the sampled input signal. Example of a signal at (b) input, (c) baseband channels output, and (d) reconstructed output.Reproduced from [38]©IEEE 2018

the baseband signals (y_i) compared to that of the input signal ($x(t)$) can be seen in Fig. 2.1(c).

The reduction of bandwidth at each channel causes the full RF spectrum to fold back to only a fraction of the bandwidth. This would violate the Nyquist criteria and can result in corruption and loss of data as demonstrated in Fig. 2.2. This is due to the fact that each N set of RF samples result in only one baseband sample at each channel. As a result, for the full reconstruction of the input signal, N separate channels are required that each provide a unique data sample at baseband. This can be achieved by employing sufficiently uncorrelated signals multiplied with RF input signal at each channel. Such signals can form a vector basis for the projection of the input signal [39].

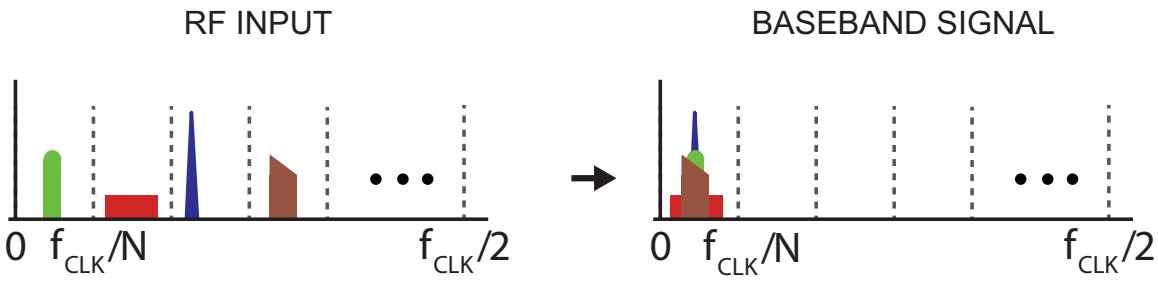

Figure 2.2. Spectrum folding due to sub-sampling of the input signal and reduced bandwidth at each baseband output

As discussed in the Appendix A, shifted versions of the same PRBS are approximately orthogonal to each other. This implies that the multiplication of the input signal with each shifted version of the PRBS provides unique baseband samples at each channel. This property along with the simplicity of PRBS implementation on an integrated circuit is the main motivation for employing these signals in the proposed architecture of Fig. 2.1(a).

The minimal correlation between the generated baseband samples enables close to full reconstruction of the input signal from those. As such, a means of signal processing is required after baseband to enable such reconstruction by the use of these samples. This is performed in digital domain as shown in Fig. 2.1(a) and will be discussed in detail in the next section.

The multiplication of the input signal with a PRBS results in a set of noise-like samples over one period of the sequence. During the integration process, these noise-like samples add in power domain. Hence, the averaging process reduces the average voltage at baseband by a factor of $\approx 1/\sqrt{N}$. If p_{i} signals were true random signals, these samples would be fully uncorrelated and the average amplitude reduction would be exactly $1/\sqrt{N}$. However, since the PRBS basis used in the proposed system is not fully orthogonal, on average, the reduction in baseband amplitudes is expected to be slightly less than $1/sqrtN$.

The proposed architecture in Fig.2.1 provides several advantages in the implementation of the receiver system. First, the RF section of the receiver can be implemented using all passive circuits which generally provide better linearity performance and consume less power compared to their active counterparts. In addition, the active part of the circuit can be moved to the baseband where higher linearity can be achieved with less power consumption. Second, the reduction of signal amplitude at baseband relaxes the linearity requirement of each baseband circuit by $\approx 10\log_{10}(N)$. Both of these advantages suggest that significant linearity enhancement can be achieved through the proposed architecture.

In the next section, a matrix representation of the architecture proposed in Fig. 2.1 will be introduced. This will simplify the understanding of the operational principle of the system.

2.1.1 Matrix Representation

Over a single frame of operation[1], the full system can be modeled as

$$\mathbf{y} = \mathbf{P}\mathbf{x}, \tag{2.1}$$

where $\mathbf{P}$ is a normalized $N \times N$ PRBS matrix as defined in Appendix A, $\mathbf{x}$ is the vector of N RF samples and $\mathbf{y}$ is the vector of corresponding baseband samples at channel outputs. Each row of the matrix corresponds to the $\mathbf{p}_\mathrm{i}$ at each channel in Fig. 2.1. Therefore, each row of the $\mathbf{P}$ is a shifted version of a normalized PRBS and the matrix possesses all properties of the PRBS matrix as discussed in the Appendix A. An example of such a matrix for a seven channel system employing seven-bit PRBSs can be given as

[1]Each frame is the set of N RF samples that result in one baseband sample at each channel at each output

$$P = \begin{bmatrix} -0.14 & -0.14 & -0.14 & 0.14 & 0.14 & -0.14 & 0.14 \\ 0.14 & -0.14 & -0.14 & -0.14 & 0.14 & 1 & -1 \\ -0.14 & 0.14 & -0.14 & -0.14 & -0.14 & 0.14 & 0.14 \\ 0.14 & -0.14 & 0.14 & -0.14 & -0.14 & -0.14 & 0.14 \\ 0.14 & 0.14 & -0.14 & 0.14 & -0.14 & -0.14 & -0.14 \\ -0.14 & 0.14 & 0.14 & -0.14 & 0.14 & -0.14 & -0.14 \\ -0.14 & -0.14 & 0.14 & 0.14 & -0.14 & 0.14 & -0.14 \end{bmatrix}. \tag{2.2}$$

Properties of such matrices have been studied in depth in [40].

2.1.2 Signal Reconstruction

From (2.1) it is clear that the reconstruction of the sampled input signal ($\mathbf{x}$) can be carried out by

$$\hat{\mathbf{x}} = \mathbf{P}^{-1}\mathbf{y}. \tag{2.3}$$

This highlights the fact that each frame of the input signal is reconstructed through a simple superposition of samples from each channel. The values in the inverse of the $\mathbf{P}$ matrix are either zero or $-2N/(N+1)$. Therefore, it can be shown that a hardware implementation of the reconstruction algorithm can be realized with just N adders, each with $(N+1)/2$ inputs each operating at f_{CLK}/N. This is a significant advantage of the proposed architecture compared to systems with more complicated reconstruction schemes such as compressive sensing [29], as it allows for possible real time operation of the system with a reasonable computational power.

Since the inverse of matrix $\mathbf{P}$ ($\hat{\mathbf{P}}$) is used for the reconstruction of the input signal, its condition number can be used to evaluate the quality of the reconstructed signal. The condition number of a matrix provides information on how error prone the inverse operation is, and it is defined as the ratio of the maximum and minimum eigenvalues ($\lambda_{max}/\lambda_{min}$) of a matrix [41]. Assuming a matrix operation of

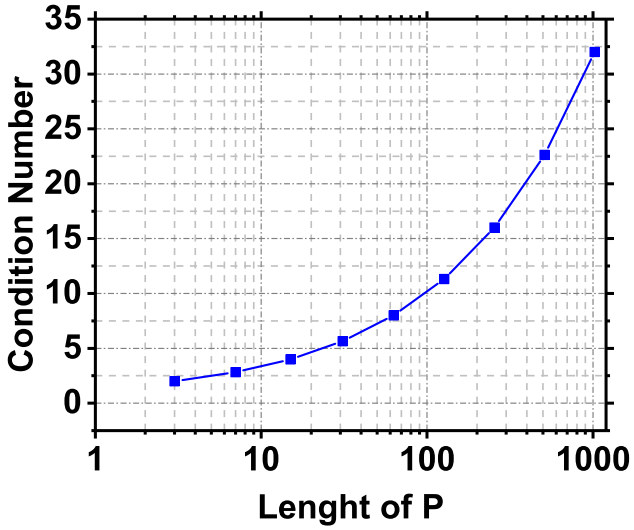

Figure 2.3. Condition number of P for different lengths.

$$\mathbf{b} = \mathbf{A}\mathbf{x} \tag{2.4}$$

where $\mathbf{b}$ and $\mathbf{x}$ are vectors and $\mathbf{A}$ is a square matrix, the relative error in $\mathbf{x}$ ($\hat{\delta_{\mathrm{x}}}$) with respect to the relative error in $\mathbf{b}$ ($\hat{\delta_{\mathrm{b}}}$) is bound by

$$|\hat{\delta_{\mathrm{x}}}| \leq |\hat{\delta_{\mathrm{b}}}||\frac{\lambda_{max}}{\lambda_{min}}|. \tag{2.5}$$

This indicates that the condition number provides a measure on how error prone the inversion process in (2.4) can be.

An ideal inversion can be achieved for a matrix that has a condition number of 1, while a non-invertible matrix has a condition number of infinity. Fig. 2.3 shows the condition number of the $\mathbf{P}$ matrix for different PRBS lengths (N) where all matrices are normalized. It can be seen that for higher values of N, the condition number becomes larger which implies higher degradation of system SNR. However, as will be discussed in the next section, this degradation of SNR is only limited to the frequency range of DC to f_{s}/N. As a result, the increase in the condition number does not result

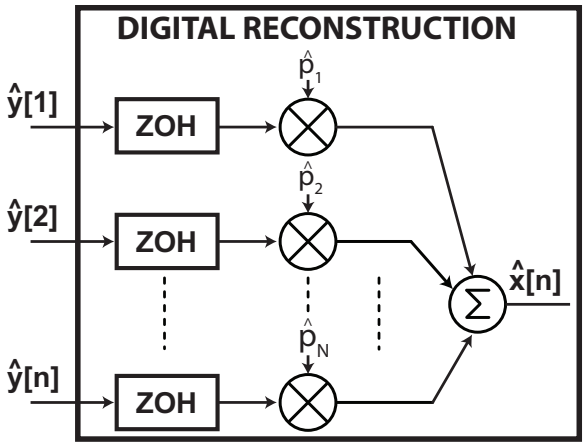

Figure 2.4. Conceptual block diagram demonstrating reconstruction procedure.

in significant degradation of system noise performance when the frequency range of f_s/N to $f_s/2$ is to be used.

In the analysis of linearity and noise, it will prove helpful to reconsider the reconstruction procedure in (2.3) as

$$\hat{\mathbf{x}} = y_1\hat{\mathbf{p}}_1 + y_2\hat{\mathbf{p}}_2 + ... + y_N\hat{\mathbf{p}}_N, \tag{2.6}$$

where $\hat{\mathbf{p}}_k$ is the kth column of the inverse matrix and y_i is the baseband sample from the ith channel. Using a zero order hold (ZOH) function with length N, each baseband sample (y_i) can be replaced with a vector ($\hat{\mathbf{y}}_i$). Therefore, (2.6) can be rewritten as

$$\hat{\mathbf{x}} = \hat{\mathbf{y}}_1\hat{\mathbf{p}}_1 + \hat{\mathbf{y}}_2\hat{\mathbf{p}}_2 + ... + \hat{\mathbf{y}}_N\hat{\mathbf{p}}_N. \tag{2.7}$$

This implies that the signal reconstruction can be considered as the sum of the products of vectors of baseband samples and each columns of the inverse matrix (see Fig. 2.4). As shown in the Appendix A, the ith column of $\hat{\mathbf{P}}$ can be written as

$$\hat{\mathbf{p}}_i = \frac{1}{N+1}\mathbf{p}_i^{\mathbf{T}} - \frac{1}{N+1}\bar{\mathbf{1}}, \tag{2.8}$$

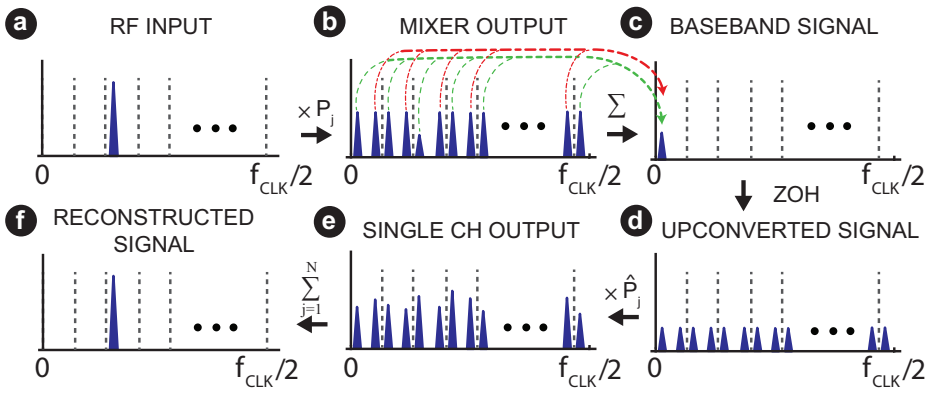

Figure 2.5. Single-sided frequency spectrum at different steps. Steps (b)-(e) represent only one of the channels.

where $\mathbf{p}_i$ is the ith column of the $\mathbf{P}$ matrix, N is the number of channels and $\bar{\mathbf{1}}$ is a column vector of length N with all elements equal to 1. Using (2.8) each column of the inverse matrix can be calculated and used in (2.7) to study the effect of signal reconstruction on system performance. Fig. 2.5 shows an example frequency spectrum at different sections of the system for a given input. Multiplication of the input signal with the PRBS spreads the signal over the spectrum (Fig. 2.5(b)) and the averaging operation folds all of these copies back to the baseband frequency (Fig. 2.5(c)). The ZOH upconverts these baseband samples to the RF rate (Fig. 2.5(d)). Multiplication with the corresponding column of the inverse matrix creates phase shifts at each channel (Fig. 2.5(e)). As a result, after summation of different channel outputs, all different tones except the signal at the correct frequency cancel out (Fig. 2.5(f)). Next, the effect of signal reconstruction on the system linearity and noise performance will be discussed.

2.1.3 Baseband Signal

Without loss of generality, system operation can be studied using a single sinusoidal RF input in the form of

$$x_{\text{in}}[n] = A_0 \cos(2\pi n f_0 / f_{\text{CLK}}). \tag{2.9}$$

The baseband signal ($y_i[m]$) can be found using the Fourier series of the PRBS from (A.12) and summation over one full period. This gives

$$y_{\mathrm{i}}[m] = \frac{A_0}{N^2}\sum_{n=0}^{N-1}\Bigg[-\cos(2\pi\frac{f_0}{f_{\mathrm{CLK}}}n + 2\pi mN\frac{f_0}{f_{\mathrm{CLK}}}) + \sqrt{N+1}\sum_{k=1}^{(N-1)/2}\cos(2\pi(\frac{k}{N}+\frac{f_0}{f_{\mathrm{CLK}}})n + 2\pi mN\frac{f_0}{f_{\mathrm{CLK}}} + \phi_{\mathrm{k}} - 2\pi\frac{ik}{N}) + \sqrt{N+1}\sum_{k=1}^{(N-1)/2}\cos(2\pi(\frac{k}{N}-\frac{f_0}{f_{\mathrm{CLK}}})n - 2\pi mN\frac{f_0}{f_{\mathrm{CLK}}} + \phi_{\mathrm{k}} - 2\pi\frac{ik}{N})\Bigg], \quad (2.10)$$

where ϕ_{k}, as defined in (A.12), is the phase of the kth tone of a reference PRBS and n is an integer time index corresponding to each of the N sampling instances. By employing [42]

$$\sum_{k=0}^{N-1}\cos(ak+b) = \cos(\frac{N-1}{2}a+b)\frac{\sin(\frac{Na}{2})}{\sin(\frac{a}{2})}, \quad (2.11)$$

2.10 can be reduced to

$$y_i[m] = -\frac{A_0}{N^2}c_0(f_0)\cos(d_0(f_0)+\psi_0(m,f_0)) + \frac{A_0}{4}\frac{N+1}{N^2}\sum_{k=1}^{(N-1)/2}\Big[c_k(f_0)\cos(d_k(f_0)+\psi_k(m,f_0)-\Theta_k(i)) + c_k(-f_0)\cos(d_k(-f_0)+\psi_k(m,f_0)-\Theta_k(i))\Big], \quad (2.12)$$

where

$$c_{\mathrm{k}}(f_{\mathrm{a}}) = \frac{\sin\left(N\pi\left(f_{\mathrm{a}}/f_{\mathrm{CLK}}+k/N\right)\right)}{\sin\left(\pi\left(f_{\mathrm{a}}/f_{\mathrm{CLK}}+k/N\right)\right)} \quad (2.13)$$

$$d_{\mathrm{k}}(f_a) = \pi(N-1)\left(\frac{f_{\mathrm{a}}}{f_{\mathrm{CLK}}}+\frac{k}{N}\right), \quad (2.14)$$

$$\psi_{\mathrm{k}}(f_{\mathrm{a}},m) = \pi mN\frac{f_{\mathrm{a}}}{f_{\mathrm{CLK}}}+\phi_{\mathrm{k}}, \quad (2.15)$$

and

$$\Theta_{\mathrm{k}}(i) = i\frac{2\pi k}{N}. \quad (2.16)$$

From (2.12) it is apparent that the only term dependent on the row number is Θ_k. This creates a phase slope among the down converted signals at different channels. The reconstruction procedure should inverse this phase slope such that all extra tones cancel out and only the main tone is fully reconstructed.

2.2 Overall System Linearity and Noise Performance

As discussed in previous sections, the proposed architecture in Fig. 2.1 allows for the implementation of the RF section using passive circuits. In addition, the baseband block can be implemented using active circuits in order to provide sufficient gain. With this in mind, the overall system performance due to noise and nonlinearity can be evaluated. These studies provide intuition on the importance of each system block and should be considered for the optimum implementation of the system.

2.2.1 Linearity

The proposed technique is aimed to employ passive mixer first architecture, which exhibits high in-band linearity [33]. However, to reduce the overall noise figure of the system the baseband circuitry should be implemented using active circuits with sufficient power gain to reduce the noise contribution of following stages. As a result, the main source of nonlinearity is assumed to be the active baseband circuitry. Gain compression and third order intermodulation are metrics that are used in RF circuit design. Gain compression is quantified as the level of the input power that results in 1 dB reduction of small signal gain as depicted in Fig. 2.6(a). The third order intercept point (IIP3) is defined as the input power for which the third order intermodulation tones (IM3) have equal power to that of the main tone. The 1 dB compression point is mainly used to characterize the large signal performance of RF systems as it does not manifest itself at low signal powers. However, the third order

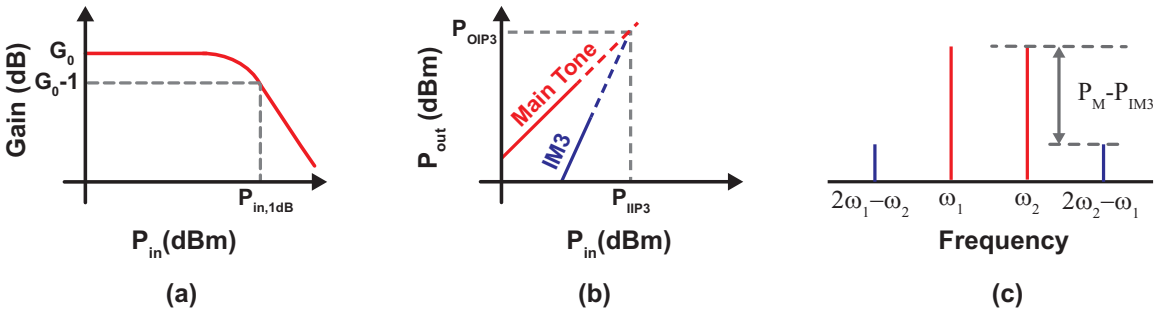

Figure 2.6. (a) Compression of gain due to increase in input signal power. The input power that causes 1dB reduction is called 1dB compression point (P1dB). (b) The input power at which the extrapolated IM3 tone and main tone signal would have equal output power.(c) IIP3 calculation test from close in intermodulation tones.

intermodulation products can interfere with small signals and result in distortion of the desired message.

As discussed in Section 2.1, multiplication of the input signal with the PRBS and averaging over the full sequence reduces the average signal swing at baseband by a factor of $\approx 1/\sqrt{N}$. This results in the overall IIP3 and P1dB of the system to be $\approx 10\log_{10}(N)$ dB higher than that of each individual baseband circuitry. While this provides an estimation of the system linearity performance, a more detailed analysis is required for full characterization of the system.

For a memory free system with weak nonlinearity, the output can be written in terms of the input signal using the power series representation [43]

$$y = c_0 + c_1 x + c_2 x^2 + c_3 x^3 + \dots \,, \tag{2.17}$$

where x is the input to the system, y is the output, and c_is are constant coefficients which depend on the system properties. The importance of the third order nonlinearity term is in the fact that the unwanted tones due to these terms rise above the noise floor of the receiver before higher order terms. Thus they limit the overall system performance at much lower power levels. In addition the effect of even order nonlin-

earities can be significantly reduced by employing fully differential architectures. In addition, higher order odd terms (e.g. fifth, seventh, ...) usually have much smaller coefficients. Thus these terms are excited at higher input power levels. Therefore, the third order terms are usually the first terms rising above the noise floor when the input signal power is increased and limit the performance.

The third order intermodulation tones are generated when two tones at ω_1 and ω_2 are put through a third order nonlinearity. This results in the generation of extra tones at $2\omega_1 \pm \omega_2$ and $2\omega_2 \pm \omega_1$. The importance of these terms is in the fact that they can lay close to the desired message signal (see Fig. 2.6(c)). A common way to measure IIP3 is to put two equally powered tones through the system and then evaluating the resulting intermodulation products. The IIP3 can be found by

$$IIP3 = \frac{P_{\mathrm{M}} - P_{\mathrm{IM3}}}{2} + \mathrm{P}_{in}, \tag{2.18}$$

where P_M is the power of the main tone at ω_1 and ω_2, P_{IM3} is the power of intermodulation tones, and P_{in} is the power of the input signals.

The effect of system operation on linearity performance for a differential implementation (to mitigate the even order effects) can be studied by considering the third-order non-linearity in the form of

$$y = \alpha_1 x + \alpha_3 x^3, \tag{2.19}$$

for each individual channel of the proposed architecture. Assuming that all channels exhibit the same nonlinear behavior, the system can be modeled as shown in Fig. 2.7. The analytical solution to the overall IIP3 of the system requires the employment of results in (2.12) to find the baseband signals due to a two tone excitation. Then, the third order nonlinearity in the form of (2.19) should be applied to the results for each individual channel. Finally, the reconstruction procedure in (2.7) should be used for

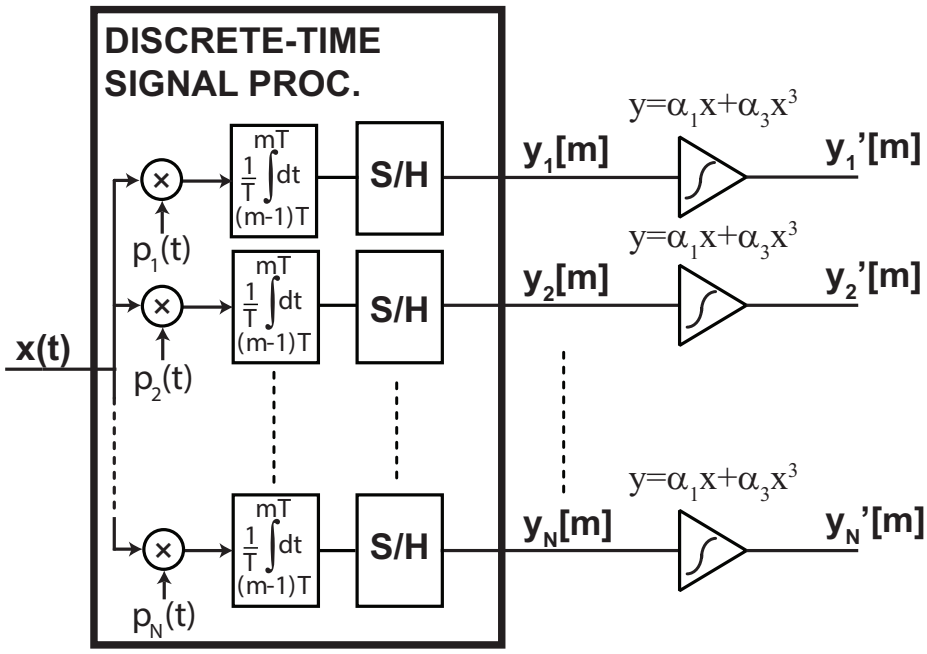

Figure 2.7. Inclusion of the third order nonlinearity in the top level system. All amplifiers are assumed to exhibit the same nonlinearity properties.

these results to find the power of the intermodulation products. Unfortunately, it does not seem that the result of these extensive mathematical calculations can be reduced to a simple intuitive closed form equation. As a result, numerical simulations using Matlab were carried out to evaluate the system performance over different scenarios.

For the system of Fig. 2.7, the linear terms go through the system with a gain of α_1 and are reconstructed as described previously. However, the third order products in the baseband signal of (2.12) experience phase distortion. This distortion results in residual terms after reconstruction procedure which do not cancel out and create multiple spurious tones at the output. An example spectrum of a reconstructed signal for a two tone excitation and third-order nonlinearity in the form of (2.19) is shown in Fig. 2.8. Through numerical simulations, it was verified that except the spurious tones below f_{CLK}/N all other spurious tones were below the IM3 tones. It will later be discussed that the noise floor of the system rises significantly for frequencies below $f_{\mathrm{CLK}/N}$. Therefore, the system should be operated in the frequency range of f_{CLK}/N

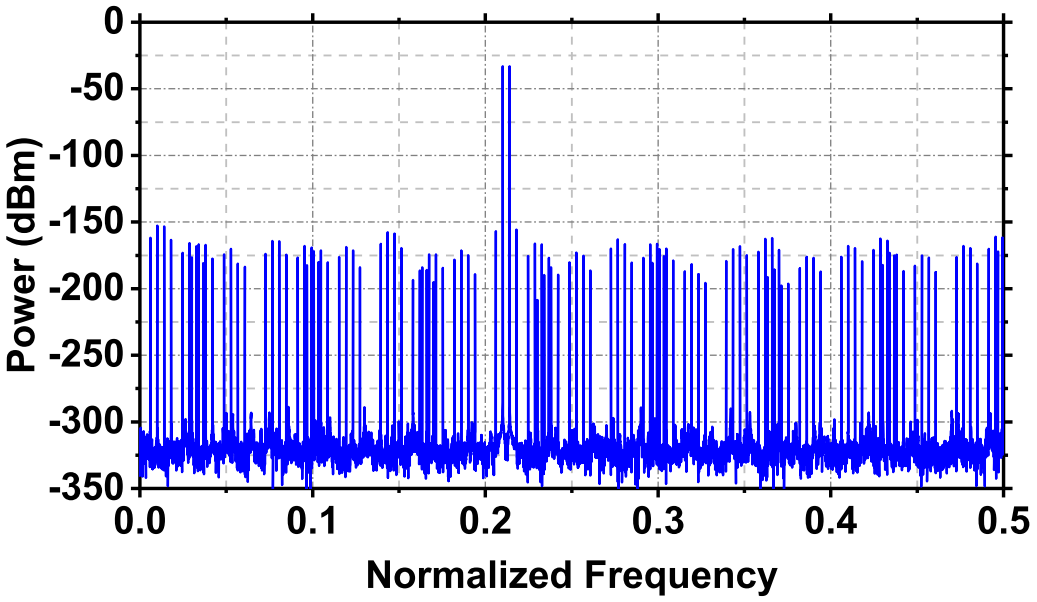

Figure 2.8. An example spectrum of a reconstructed two tone signal with third-order nonlinearity at baseband. For these simulation $\alpha_1 = 1$ and α_3=0.1. These numbers correspond to a gain of 0 dB and IIP3 of approximately 40 dBm into a 1 Ω termination.

to $f_{\mathrm{CLK}}/2$ for optimum performance and as such, spurious tones outside this range are not critical.

The phase slope for the intermodulation products is distorted and can result in frequency dependent nonlinearity performance. Fig. 2.9 shows the simulation results for IIP3 improvement over frequency for two different PRBS lengths of seven and fifteen. Since the DC tone in the PRBS has lower power, the amplitude of the signal at the lowest part of the band is further reduced after multiplication with the PRBS and down conversion to baseband. As a result, higher IIP3 values are achieved for the low end of the RF spectrum. It can be seen from Fig. 2.9 that for N=15 the IIP3 improvement over the band (not including the lower frequencies) varies from 9 dB to 12 dB while the ideal value predicted by the previous analysis is $10\log_{10}(15) = 11.8$. However, for N=7 the IIP3 improvement is less than 8 dB over the frequency range with the ideal value expected to be ≈8.5 dB. As expected, for higher values of N, the

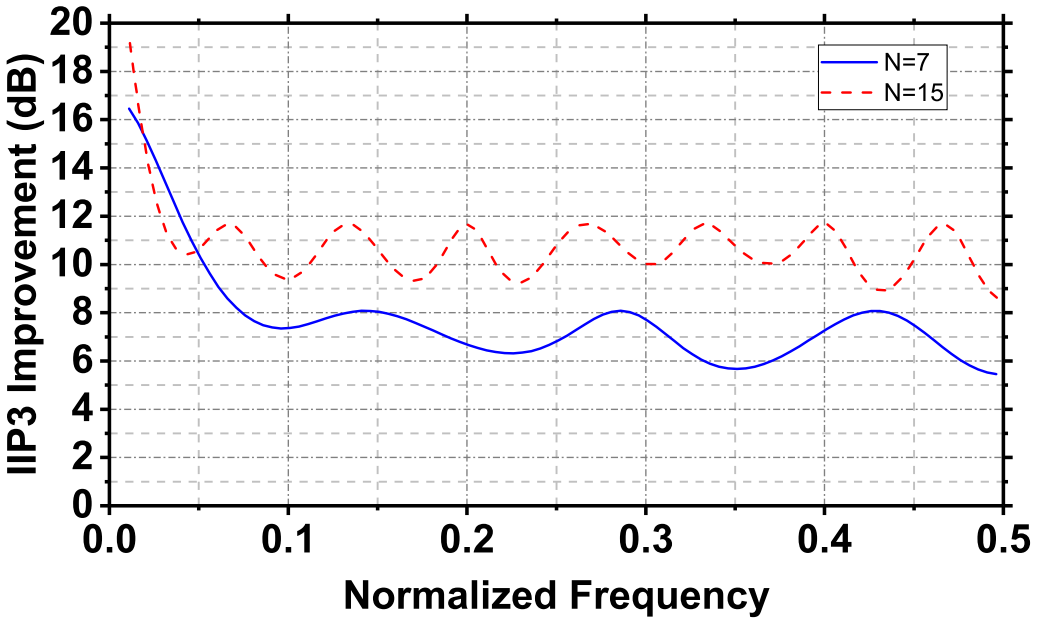

Figure 2.9. Simulation results of system IIP3 improvement over that of each channel for PRBS lengths of N=7 and N=15.

improvement is closer to the ideal value of $10\log_{10}(N)$ since the PRBS provides a closer approximation to a truly random sequence.

As discussed earlier, frequencies lower than f_{CLK}/N exhibit a significant improvement in linearity performance, however the next section will discuss that this improvement comes at the cost of noise degradation.

2.2.2 Noise

The analysis of linearity improvement in the system without the knowledge of noise performance does not provide a complete picture for the effectiveness of the proposed technique. Employment of a single attenuator could potentially achieve the same linearity enhancement, however, this would significantly degrade the noise figure of the receiver. For a passive attenuator, the noise figure in dB is equal to the attenuation in dB. Thus, the signal to noise and distortion ratio (SNDR) of the system does not improve in this case. While the proposed technique provides the means of frequency downconversion such that lower speed ADCs are used, any

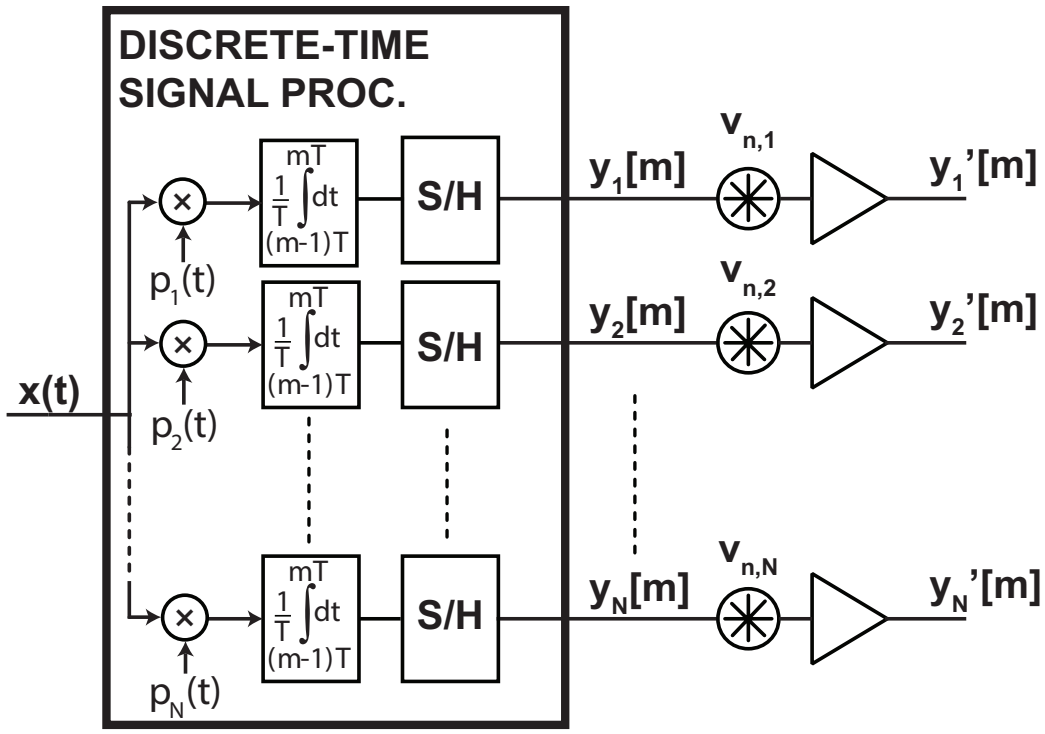

Figure 2.10. Top level diagram of the receiver system including noise sources referred to the input of the baseband amplifier for each channel.

degradation of noise performance due to the signal processing can have significant importance in the effectiveness of the discrete-time technique.

By referring all major sources of noise to the input of the baseband amplifier (as shown in Fig. 2.10), the effect of signal reconstruction on the overall noise performance can be studied. For an amplifier with unity gain, the input and reconstructed signal will be the same. Therefore, the total input referred noise of the system can be also analyzed by finding the noise after the reconstruction procedure. To do so, the reconstruction procedure in Fig. 2.4 can be utilized.

A significant portion of the noise at each channel can be assumed to have a Nyquist-limited white noise spectrum with an RMS noise voltage of σ_{N} stemmed from thermal noise sources. However, noise due to clock jitter does not have a flat frequency spectrum and will be discussed later. To the first order, the noise sources from different channels are uncorrelated with each other. The result of (2.7) shows

that this noise is upsampled by going through the ZOH block and then multiplied with the inverse PRBS and summed over all channels. The discrete time Fourier transform (DFT) of the impulse response of a ZOH with a length N is

$$|H_{\mathrm{ZOH}}|^2 = \frac{\sin^2(\pi f N T_{\mathrm{CLK}})}{N^2 \sin^2(\pi f T_{\mathrm{CLK}})}. \tag{2.20}$$

Thus, the power spectral density of the noise at the output of the ZOH block can be written as

$$S_{\mathrm{n,ZOH}} = \frac{\sigma_{\mathrm{N}}^2}{f_{BB}} \frac{\sin^2(\pi f N T_{\mathrm{CLK}})}{N^2 \sin^2(\pi f T_{\mathrm{CLK}})}. \tag{2.21}$$

The PSD of each individual channel at the output can be found by convolving this result with the PSD of the inverse PRBS ($\hat{p}_{\mathrm{i}}$), which is derived in Appendix A and can be written as

$$P_{\hat{\mathbf{p}}}(f) = 1\delta(f) + \frac{1}{N+1} \sum_{k=1}^{N} \delta(f \pm k f_s). \tag{2.22}$$

As a result, the noise PSD of each individual channel can be found by

$$S_{\mathrm{N,i}} = \frac{1}{N+1} \frac{\sigma^2}{f_{\mathrm{BB}}} \left[(N+1) \frac{\sin^2(\pi f N T_{\mathrm{CLK}})}{N^2 \sin^2(\pi f T_{\mathrm{CLK}})} + \sum_{k=1}^{(N-1)/2} \frac{\sin^2(\pi (f \pm k f_{\mathrm{BB}}) N T_{\mathrm{CLK}})}{N^2 \sin^2(\pi (f \pm k f_{\mathrm{BB}}) T_{\mathrm{CLK}})} \right]. \tag{2.23}$$

since [42]

$$\frac{\sin^2(\pi f N T_{\mathrm{CLK}})}{N^2 \sin^2(\pi f T_{\mathrm{CLK}})} + \sum_{k=1}^{(N-1)/2} \frac{\sin^2(\pi (f \pm k f_{\mathrm{BB}}) N T_{\mathrm{CLK}})}{N^2 \sin^2(\pi (f \pm k f_{\mathrm{BB}}) T_{\mathrm{CLK}})} = 1, \tag{2.24}$$

then (2.23) can be reduced to

$$S_{\mathrm{N,i}} = \frac{1}{N+1} \frac{\sigma^2}{f_{\mathrm{BB}}} [1 + \frac{\sin^2(\pi f N T_{\mathrm{CLK}})}{N \sin^2(\pi f T_{\mathrm{CLK}})}]. \tag{2.25}$$

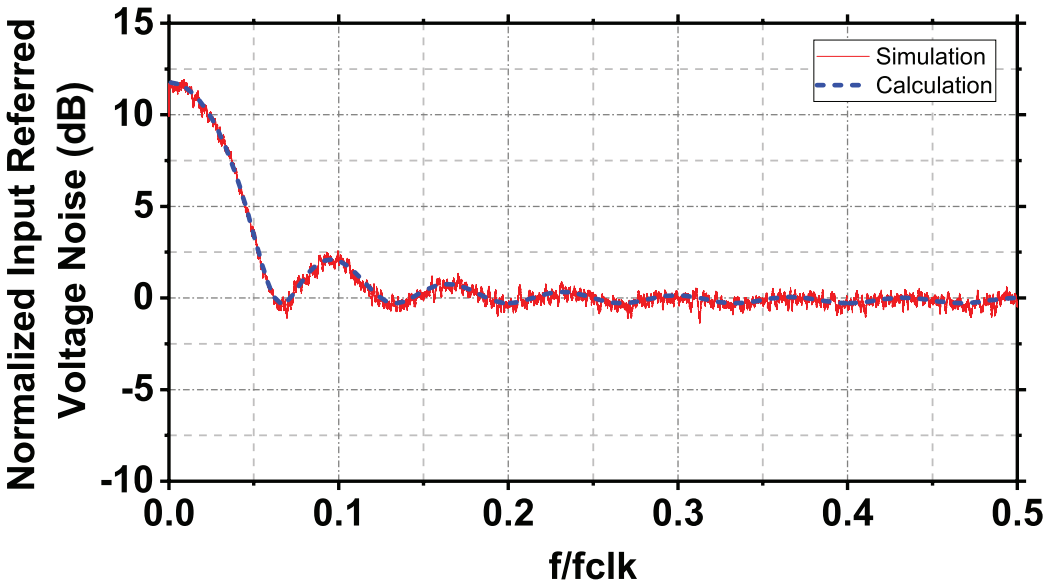

Figure 2.11. Comparison of simulated noise from Matlab Simulink model for N=15 and results of (2.27). Reproduced from [38] ©IEEE 2018

Since the noise of each channel is assumed to be uncorrelated with the others, the total output noise is given by

$$S_N = \sum_{i=1}^{N} S_{i,N} = N S_{i,N}, \tag{2.26}$$

Therefore,

$$S_{\mathrm{N}} = \frac{N}{N+1}\frac{\sigma^2}{f_{\mathrm{S}}}[1 + \frac{\sin^2(\pi f N T_{\mathrm{CLK}})}{N \sin^2(\pi f T_{\mathrm{CLK}})}]. \tag{2.27}$$

Using Matlab Simulink software, a behavioral model was built for N=15 to verify (2.27). The block diagram of the system is shown in Appendix C. The comparison of the simulation results for the total normalized noise and the predicted value by (2.27), where both values are normalized to σ_N^2/f_{BB} which is the noise spectral density of each baseband source, is showed in Fig. 2.11.

The results presented in Fig. 2.11 show that for frequencies below f_{CLK}/N, the reconstruction procedure degrades the system noise performance by up to 11.8 dB which is equal to $10\log_{10}15$. However, there is only a small degradation in noise

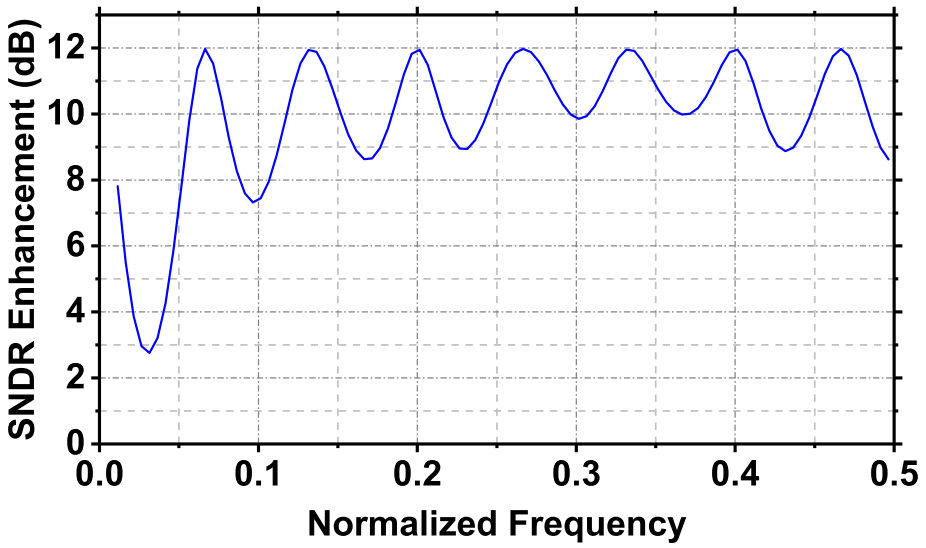

Figure 2.12. Overall SNDR enhancement of the system over frequency for N=15.

at higher frequencies. This is a significant result since for these frequencies, the linearity enhancement can be achieved with a very small penalty in noise. This results in the enhancement of the SNDR for the overall system over that of each individual channel. Fig.2.12 shows the overall SNDR enhancement of the system over frequency. Due to the noise degradation at lower frequencies and lower overall SNDR enhancement, the proposed architecture can be mainly used for the frequency band from $f_{\mathrm{CLK}}/N - f_{\mathrm{CLK}}/2$.

Using the results of (2.27), the noise factor of the system with respect to a 50 Ω source termination can be written in terms of S_N as

$$F \approx 1 + \frac{1-\alpha}{\alpha}\frac{T_a}{T_0} + \frac{2S_N}{\alpha k T_0 R_{\mathrm{s}}}, \tag{2.28}$$

where α is a constant between 0 to 1 that models the loss in the sampling circuit(α=1 corresponds to no loss), T_{a} is the physical temperature, $T_0 = 290K$ is the reference temperature, and $k = 1.38 \times 10^{-23} J/K$ is Boltzmann's constant.

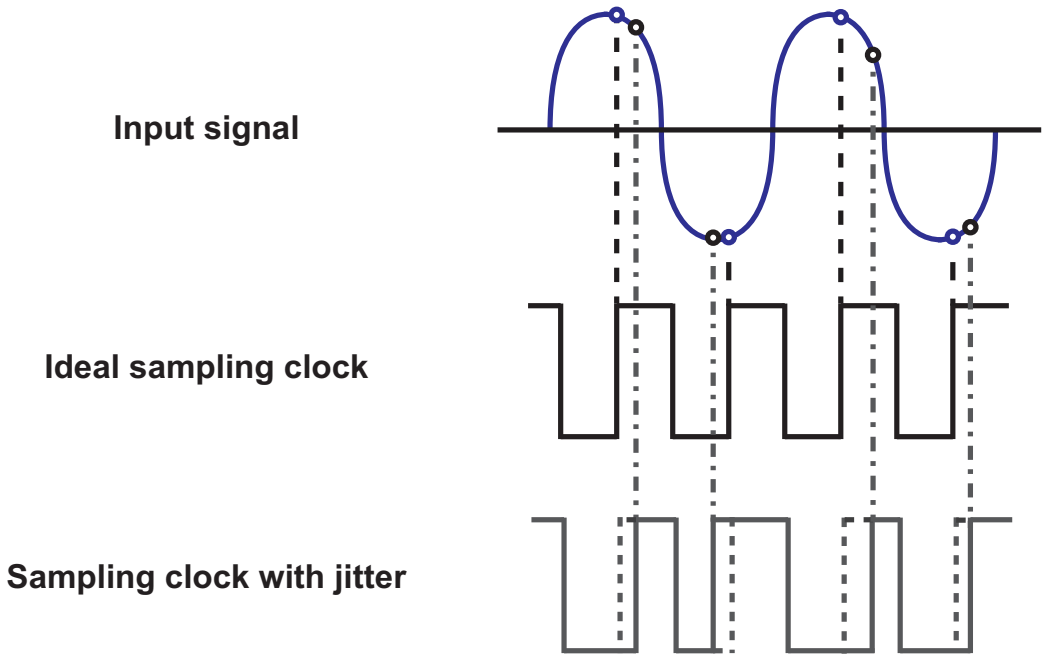

Figure 2.13. Effect of clock jitter on sampling signals.

2.2.2.1 Sampling Jitter

Sampling jitter corresponds to the error in the sampling time of a discrete-time signal due to imperfections in the clock. This error can be due to the noise of the blocks on the clock path and the phase noise of the oscillator generating the original clock signal. Fig. 2.13 demonstrates the effect of clock jitter on incorrect sampling of an input signal. The magnitude of the sampling error due to the clock timing jitter is also dependent on the derivative of the input signal. A higher derivative results in larger errors due to small changes in the sampling timing. As such, input signals at higher frequencies experience more severe effects due to this phenomena.

Jitter can present significant error in discrete-time systems that require sampling, such as analog-to-digital converters (ADCs), and has been the topic of significant research for such applications [44–46]. Jitter in these applications is dominated by the reference oscillator, the phase noise of which adds a skirt-like frequency response to the frequency spectrum of the clock as shown in Fig. 2.14(a). Since this error is a

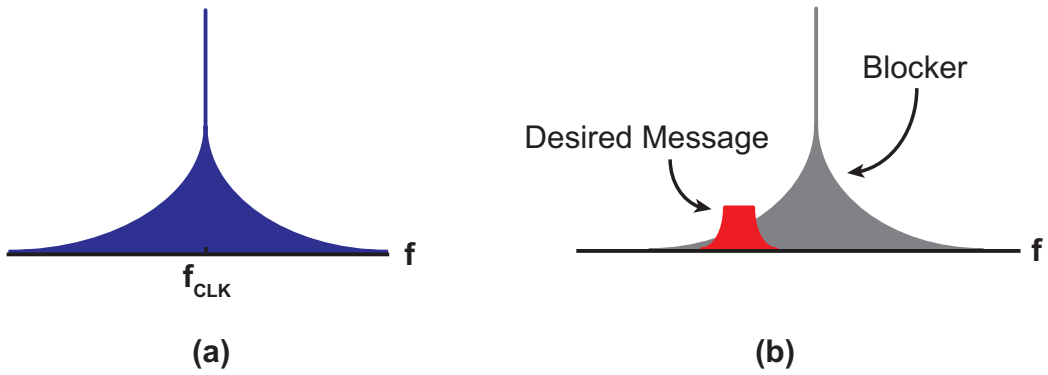

Figure 2.14. (a) Phase noise of the oscillator adds a skirt to the frequency spectrum of the clock signal, (b) The noise skirt of a blocker signal corrupting the spectrum of a message signal.

multiplicative effect, it scales with the amplitude of the signal. The main challenge rises when a small signal is accompanied by a large blocker in its near vicinity. As is graphically explained in Fig. 2.14(b), the noise skirt of a large blocker can corrupt the spectrum of the desired message at a close frequency range.

In the proposed system, the primary source of jitter at each channel is the reference clock signal which affects all channels in a fully correlated way. As such, this system is affected by jitter in the same way as a time-interleaved ADC (TIADC). Thus, the same analysis applied to such systems can be used to estimate the phase noise requirement on the reference clock signal for the proposed architecture.

When discrete-time systems are used for direct sampling of RF signals, the worst case scenario for phase noise is for a blocker signal at the highest possible input frequency and the maximum swing along with a message signal at the sensitivity level. For this case, the estimate of oscillator phase noise requirement results in more stringent requirements for discrete-time receivers compared to the conventional downconversion receivers [45]. However, as discussed in [45], if the emission masks of the communication standards which limit the blocker signal power are considered, the above worst case scenario results in a pesimistic value for the phase noise requirement. In fact, as shown in [45], by considering these standards the phase noise

requirements can be relaxed to the same level as downconversion receivers. As the proposed technique is expected to exhibit similar jitter performance as other commonly used discrete-time systems, the overall jitter performance is expected to be similar to those and it is not further discussed in this dissertation.

2.3 Summary

In this chapter, a discrete-time signal-processing technique to enhance linearity of wideband receiver systems is introduced. The proposed technique enables the use of mixer first approaches that have been shown to achieve higher linearity. It also employs a set of PRBSs as LO signals to enable the full reconstruction of the input signal in digital domain. A matrix representation was also introduced to further demonstrate the operating principles of the system. The reconstruction procedure was also described which includes simple linear operations on baseband samples to reconstruct the sampled RF input signal. The effect of the proposed architecture on system linearity and noise was studied. It was discussed that due to the noise degradation for frequencies below f_{CLK}/N, the proposed system is best suited for operation at frequencies from f_{CLK}/N to $f_{\mathrm{CLK}}/2$. Moreover, it was discussed that the effect of clock jitter in the system is similar to that of TIADCs for which the recent studies have shown similar requirements compared to traditional down-conversion receiver systems. In the next chapter the effect of systematic errors on overall performance is discussed.

CHAPTER 3

EFFECT OF SYSTEMATIC ERRORS ON OVERALL PERFORMANCE

In the previous chapter all properties of different channels were assumed to be ideal. However, the implementation of the system as an integrated circuit will result in mismatches between elements in different channels. These mismatches mostly stem from process variations across the silicon wafer. Process variation is due to several effects such as random dopant fluctuations, line-edge roughness, variation associated with polish and strain, and so on [47]. As the technology scales down these effects become more severe and require more careful consideration [48,49]. This effect becomes more severe for technologies with smaller feature size as the supply voltages scale down. As a result, the effect of these errors on the overall system performance should be studied to enable the development of techniques for reducing their effects. The source of mismatch effects and their severity is implementation dependent, however their effect on the overall system performance can be studied through mathematical analysis.

In this chapter the effect of systematic errors due to DC offsets, gain mismatches, and timing skew among different channels on system performance is analyzed. It will be discussed that these effects result in spurious tones after reconstruction of the signal and limit the overall SFDR performance of the system. Analytical solutions for SFDR values due to these spurious tones are found as a function of the number of channels and severity of mismatches. Matlab numerical simulations are also used to verify the validity of these derivations. For the sake of analysis throughout this chapter the gain of the amplifiers is assumed to be equal to one (0 dB).

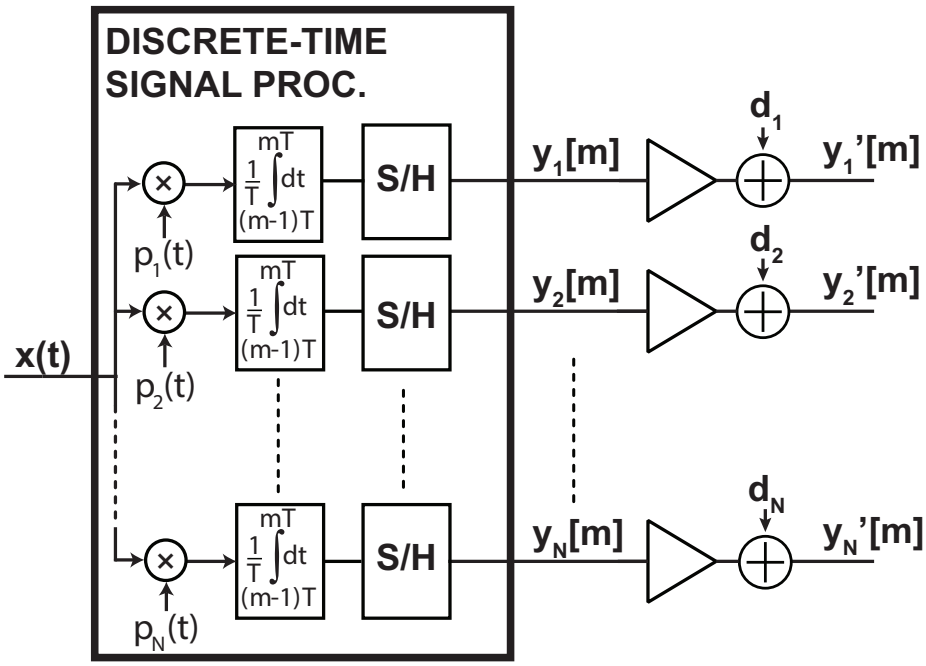

Figure 3.1. Top level diagram of the system including the dc offsets modeled as additive errors to the signal at the output of amplifiers.

3.1 DC Offset Errors

DC offsets in RF systems can stem from several sources, such as clock feedthrough[1], device mismatch, and charge injection. These DC offsets can vary among different channels and since most sources of these errors stem from random variations, the offsets between channels can be modeled as random independent errors. As a result, for the proposed architecture the effect of DC offsets can be studied by modeling them as additive errors at the output of baseband amplifiers as demonstrated in Fig. 3.1.

Using the matrix representation of the system in (2.1), the effect of DC offsets can be modeled as

$$\mathbf{y} = \mathbf{P}\mathbf{x} + \mathbf{d}, \tag{3.1}$$

[1]Clock feedthrough related DC offsets are generated after these signals pass through a second order nonlinearity in the system.

where $\mathbf{d}$ is a column vector of dc offsets at different channels. As a result, the effect of reconstruction on the DC offsets can be simply studied by multiplying the inverse of the $\mathbf{P}$ matrix with the $\mathbf{d}$ vector. Using the reconstruction model presented in Fig. 2.4 the effect of DC offsets at the output can be found independent of the input signal. The DC offset errors at each channel can be modeled as independent and identically distributed (iid) zero-mean Gaussian random variables with standard deviation of σ_{DC}. Using the power spectral density of the inverse PRBS from (A.11), the resulting spectrum after multiplication with the $\hat{\mathbf{p}}_{\mathrm{i}}$ can then be written as

$$P_{\mathrm{DC,i}} = x_{0,i}^2\delta(f) + \sum_{k=1}^{(N-1)/2} x_{1,i}^2\delta(f \pm kf_s), \tag{3.2}$$

where $x_{0,i}$ and $x_{1,i}$ are zero-mean Gaussian random variables with variances σ_{DC}^2 and $\sigma_{\mathrm{DC}}^2/(N+1)$ respectively. Since the errors from different channels are uncorrelated, the total spurious signal power is N times that of one individual channel and can be written as

$$P_{\mathrm{Spur,DC}} = u_0^2\delta(f) + \sum_{k=1}^{(N-1)/2} u_1^2\delta(f \pm kf_s), \tag{3.3}$$

where u_0 and u_1 are random variables with variances $\sigma_{\mathrm{DC}}^2 N$ and $\sigma_{\mathrm{DC}}^2 N/(N+1)$ respectively. Hence, the spurious tones due to the DC offsets have (N+1) times higher power at DC compared to other frequencies. This effect is similar to that of system noise performance. Inspection of (3.3) reveals that spurious signals due to the DC offsets are independent of the input signal ($x(t)$) which is due to the additive nature of these errors. Thus the average power of the spurious tones due to DC offsets at frequency band between $f_{\mathrm{s}/N}$ to $f_{\mathrm{s}}/2$ can be found from

$$P_{avg,DC} = \frac{N\sigma_{\mathrm{DC}}^2}{N+1}. \tag{3.4}$$

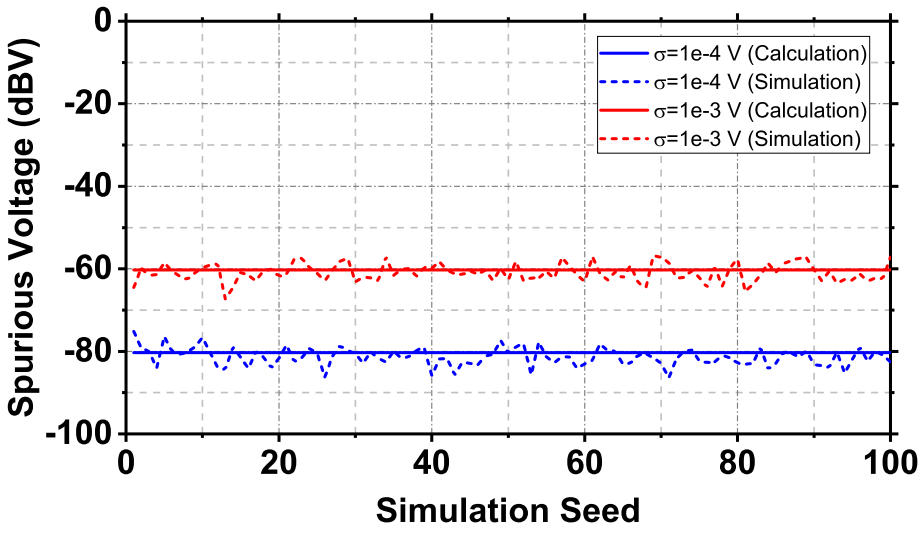

Figure 3.2. Monte Carlo simulation results of DC offset induced spurious content along the average value predicted by (3.4)

To verify (3.3), numerical Monte Carlo simulations were run in Matlab. In these simulations, 100 different random seeds are run. For each of these runs a random number with a constant standard deviation value was used as the DC offset for each channel . While the DC tone is expected to be stronger, since it is rarely of interest in communication systems, the spurious tones at other frequencies were compared with the values found by (3.3) and results are shown in Fig. 3.2. These results show that DC offset voltages with standard deviation of 1 mV can create spurious tones with the power of -47 dBm in a 50Ω system. This can severely limit the system performance since these spurious tones do not scale with the input signal and can land in the middle of the message band. However, as these values are referred to the input of the system, the DC offsets at the output of the channels is divided by its gain and significantly reduced. But nevertheless, this highlights the importance of employing techniques to reduce DC offsets in the system. Moreover, calibration procedures can be employed to further address this issue if necessary which will be discussed in Chapter 6.

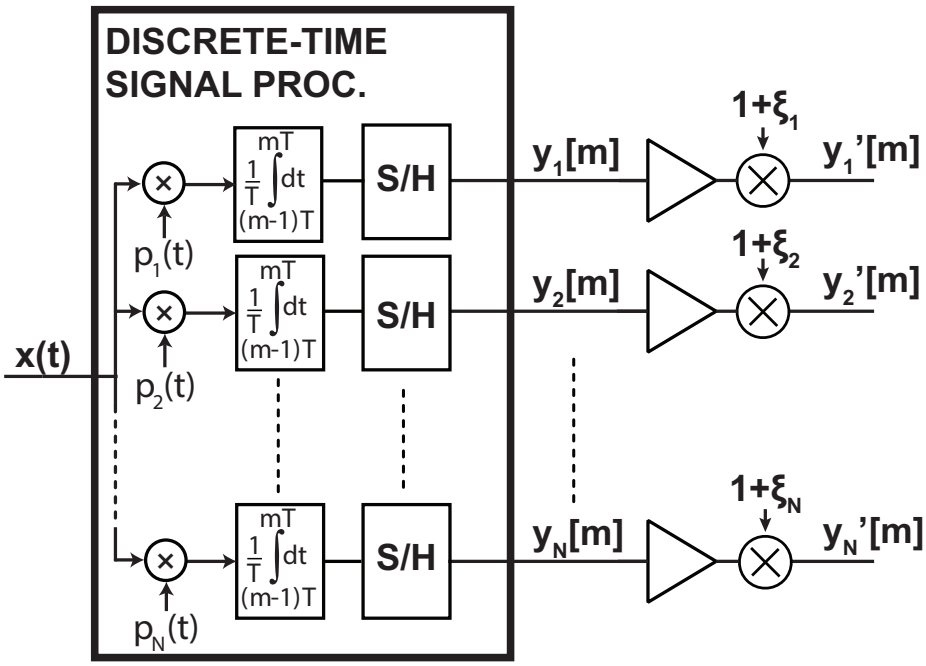

Figure 3.3. Top level diagram of the system including the effect of gain mismatch errors.

3.2 Gain Mismatch

Gain mismatch between different channels can be due to different gains in both the RF section and baseband amplifiers. These effects can be modeled by random scaling of baseband samples as demonstrated in Fig. 3.3. Thus, the resulting baseband samples can be written as

$$\hat{y}_{\mathrm{i}} = (1 + \xi_{\mathrm{i}})y_{\mathrm{i}}, \tag{3.5}$$

where ξ_{i} models the gain mismatch of the ith channel. Without loss of generality, the effect of these mismatches can be studied on the overall signal reconstruction for a single tone input with a unit amplitude and frequency of f_{RF}. By assuming the gain mismatches are iid zero-mean Gaussian random variables with standard deviation of σ_{G} and using the reconstruction model presented in Fig. 2.4 their effect on system performance can be studied. Based on the analysis discussed in Chapter 2 the average baseband signal (y_{i}) can be written as

$$y_{\mathrm{i}} = \frac{1}{\sqrt{N}} \sin(2\pi f_{\mathrm{BB}} t + \phi_{\mathrm{i}}), \tag{3.6}$$

where f_{BB} =mod(f_{RF},f_{s}) is the aliased frequency of input signal to baseband and ϕ_{i} is the phase shift corresponding to each channel as defined in (A.12). By using the spectrum of the baseband signal , considering the ZOH block response and multiplication withe the PSD of inverse PRBS from (A.11), the spectrum at the output of each individual channel can be written as

$$\begin{aligned} P_{\mathrm{G,i}} &= \frac{y_0^2}{2N}\delta\left(f \pm f_{\mathrm{BB}}\right) \\ &+ \frac{1}{2N\left(N+1\right)} \sum_{n=1}^{(N-1)/2} \Big[y_{1,\mathrm{n}}.^2 \delta\left(f \pm (nf_{\mathrm{S}} + f_{\mathrm{BB}})\right) + y_{\text{-}1,\mathrm{n}}.^2 \delta\left(f \pm (nf_{\mathrm{S}} - f_{\mathrm{BB}})\right) \Big], \end{aligned} \tag{3.7}$$

where y_0, $y_{1,\mathrm{n}}$, and $y_{\text{-}1,\mathrm{n}}$ are zero-mean iid Gaussian random variables with variance σ_{G}^2. The overall spectrum after reconstruction is the sum of all channels in power domain which is N times that of (3.7),

$$P_{\mathrm{G}} = \frac{y_0^2}{2}\delta\left(f \pm f_{\mathrm{BB}}\right) + \frac{1}{2\left(N+1\right)} \sum_{n=1}^{(N-1)/2} \Big[y_{1,\mathrm{n}}.^2 \delta\left(f \pm (nf_{\mathrm{S}} + f_{\mathrm{BB}})\right) + y_{\text{-}1,\mathrm{n}}.^2 \delta\left(f \pm (nf_{\mathrm{S}} - f_{\mathrm{BB}})\right) \Big]. \tag{3.8}$$

From (3.8) it is apparent that the spurious signals due to the gain mismatches are stronger at the lowest frequency portion similar to that of DC offsets and noise. Assuming the system is operated at the frequency range between f_{CLK}/N–$f_{\mathrm{CLK}}/2$ the SFDR can be estimated by considering the expected value of the maximum spurious tone. For a normal distribution the expected value of the maximum of N samples is given by [50]

$$\mathbb{E}_{\max} = \Phi^{-1}\{0.52641^{(1/2N)}\}\sigma_{\mathrm{G}} \tag{3.9}$$

where Φ^{-1} is the inverse of the Gaussian CDF. Hence, the SFDR can be estimated as

$$\mathbb{E}\left\{\mathrm{SFDR_G}\right\} \approx \frac{N+1}{(\Phi^{-1}\{0.52641^{(1/2N)}\})^2 \sigma_{\mathrm{G}}^2}. \tag{3.10}$$

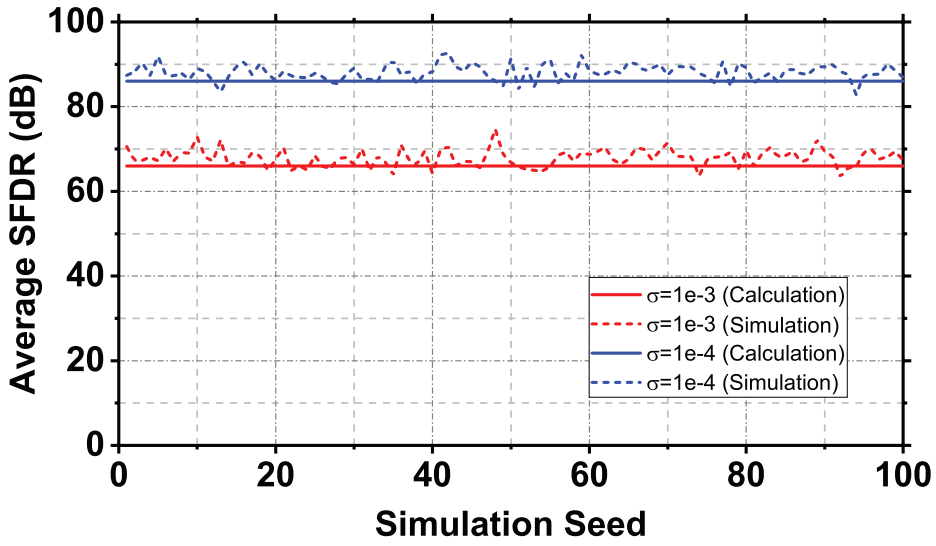

Figure 3.4. Monte Carlo simulation results of SFDR values due to gain mismatch induced spurious tones versus predicted results by (3.10).Reproduced from [38]©IEEE 2018.

Monte Carlo simulations were carried out in Matlab to validate the analytical results from (3.10). The results are shown in Fig. 3.4 and show that 0.1% mismatch in gain between different channels would limit the SFDR performance to about 60 dB which is lower than the requirement for most applications. Achieving this level of mismatch solely through layout techniques can be very challenging for sub micron technologies over the full chip area. Hence, calibration techniques may be required to enhance the achievable SFDR.

3.3 Timing Skew

Timing skews between channels stem from mismatches in the propagation delay of RF and clock signals to each channel. For the purpose of this analysis the delays within each channel of the implemented system are assumed relatively small. The timing skew across different channels can be modeled as a delay at the RF signal getting to each channel. This is demonstrated in Fig. 3.5.

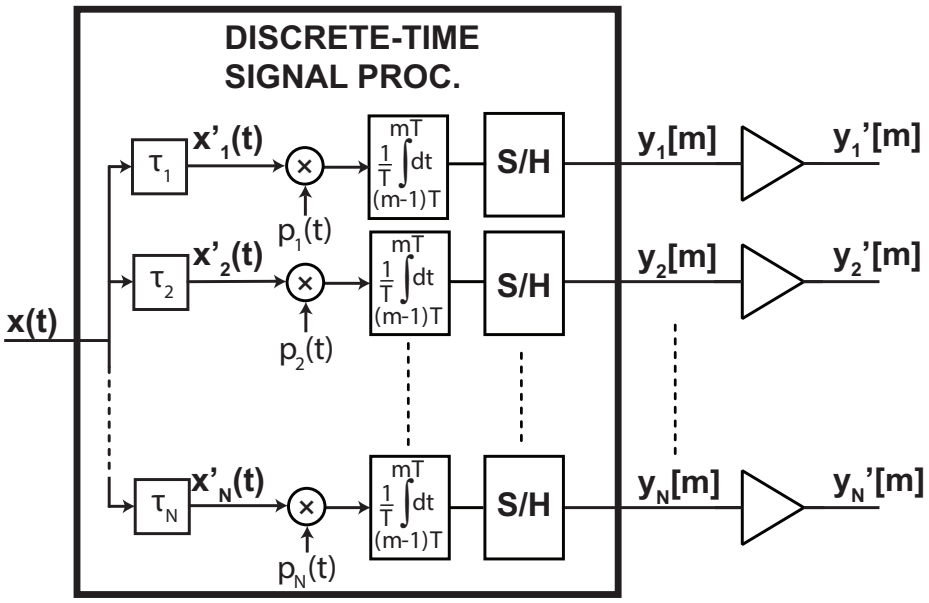

Figure 3.5. Top level diagram demonstrating the effect of timing skew between channels which can be modeled as a different delay for the input signal to each individual channel.Reproduced from [38]©IEEE 2017

Without loss of generality the effect of timing skew can be studied for a single tone sine wave input in the form of

$$x(t) = A\sin(2\pi f_{\text{in}}t + \phi_0). \tag{3.11}$$

The delayed input signal to each channel can then be written as

$$x'_j = A\sin(2\pi f_{\text{in}}(t + \tau_{\text{j}}) + \phi_0), \tag{3.12}$$

where τ_{j} is a zero mean normally distributed random variable which models the delay at each channel. This can be rewritten as

$$x'_j = A[\sin(2\pi f_{\text{in}}t + \phi_0)\cos(2\pi f_{\text{in}}\tau_{\text{j}}) + \cos(2\pi f_{\text{in}}t + \phi_0)\sin(2\pi f_{\text{in}}\tau_{\text{j}})]. \tag{3.13}$$

Assuming that τ_{j} are small relative to the period of the input signal, the above equation can be reduced to

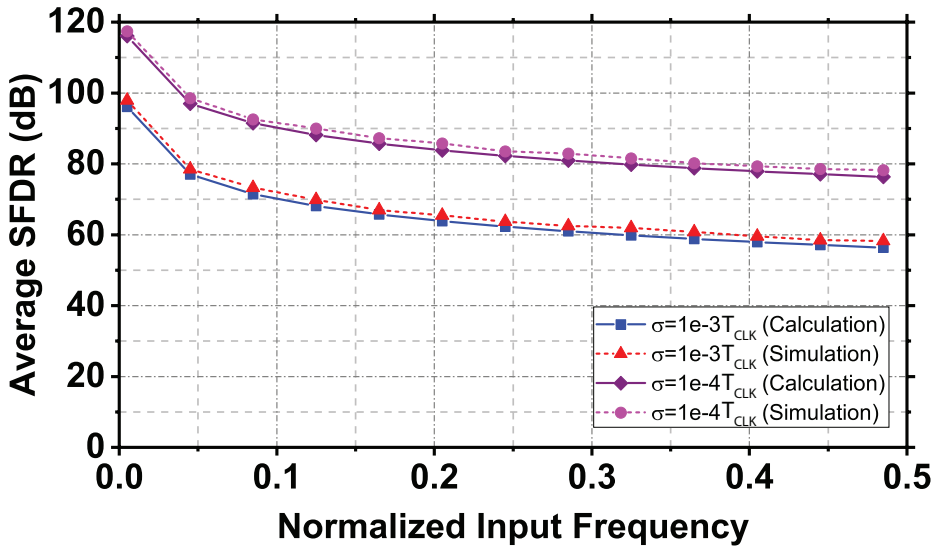

Figure 3.6. Simulation results of the effect of timing skew on expected value of the overall system SFDR versus input frequency.Reproduced from [38]©IEEE 2018

$$x'_j = A\big[\sin(2\pi f_{\text{in}} t + \phi_0) + (2\pi f_{\text{in}}\tau_{\text{j}})\cos(2\pi f_{\text{in}} t + \phi_0)\big]. \tag{3.14}$$

Here the first term is the ideal input signal and the second term is an scaled version of the input signal with a phase shift. Therefore, the effect of timing skew can be studied similar to that of gain mismatch between each channel as described in the previous section. The gain offset term at each channel is then equal to $2\pi f_{\text{in}}\tau_{\text{j}}$. Using the result of (3.10) the expected value of the SFDR due to such timing skew can be found as

$$\mathbb{E}\left\{\text{SFDR}_{\text{SKEW}}\right\} \approx \frac{N+1}{4\pi^2(\Phi^{-1}\{0.52641^{(1/2N)}\})^2 f_{\text{in}}^2\sigma_\tau^2}. \tag{3.15}$$

This shows that the SFDR due to timing skew spurious tones is inversely proportional to the input signal frequency. This is due to the fact that the same delay term would cause larger error for signals with smaller periods. A Matlab model was employed to verify the analytical solution in (3.15). For each input frequency 100 seeds of Monte Carlo simulations are run and the average SFDR is used as the SFDR value. The results are shown in Fig. 3.6 for different standard deviation values.

The results in Fig. 3.6 show that even for a delay error of one thousandth of T_{CLK} the SFDR is limited to 60 dB. For a clock frequency of 1 GHz this means that all signals should be matched better than 1 ps, thus calibration techniques may be required for enhancing the system performance.

3.4 Similarities of Mismatch Errors to Those of Time-Interleaved ADCs

Many of the mismatch effects discussed in this chapter are similar to those present in time-interleaved ADCs. These ADCs employ multiple channels that each sample the input signal at one instance of the time [36]. This enables the use of lower speed ADCs at each channel while achieving higher effective sampling rate for the overall system. As these systems employ multiple channels, systematic errors such as gain mismatch and timing skew among the channels, can have severe impact on the overall system performance [51]. For instance, as discussed in [51], the DC offsets among channels result in spurious tones located at f_{CLK}/N, while gain errors result in tones at $f_{CLK}/N \pm f_{in}$. These are similar to the effect of these mismatches in the proposed technique as descried in this chapter. These similarities between TIADCs and the proposed architecture suggest that some of the calibration techniques proposed for such applications may be employed to address mismatch effects in the proposed system.

The calibration of mismatch effects for TIADCs have been investigated and reported in literature [37, 52–56]. Most of these techniques include background calibration during the regular operation of the ADC which aims to cancel out the effect of mismatches on the collected data. This will be further discussed in Chapter 6, where calibration procedures for each of the aforementioned mismatch effects are described.

3.5 Summary

In this chapter a detailed discussion of different nonidealities that can limit the overall system performance was presented. It was highlighted that process variation results in different mismatch mechanisms which limit the SFDR performance through DC offsets, gain mismatches, and timing skews. Analytical solutions were presented for spurious tone powers due to DC offset terms at each channel and the results were compared with Monte Carlo simulation results from Matlab. In addition, the SFDR limitation due to gain and timing skew errors were also studied analytically and closed form solutions for the average SFDR was presented. The results were verified through Matlab simulations and provide a intuition in the severity of these errors. It was discussed that for SFDR values better than 60 dB both mechanisms put challenging requirements on matching between all elements. As a result, it was concluded that calibration procedures may be required in addition to layout techniques, to achieve such specifications.

CHAPTER 4

CMOS IMPLEMENTATION OF THE PROPOSED ARCHITECTURE

To evaluate the effectiveness of the architecture proposed in Chapter 2, a prototype CMOS integrated circuit was designed and implemented. The design process of this IC provides insight to challenges as well as benefits of the proposed architecture. This prototype IC was designed to take advantage of the linearity benefits of the architecture proposed in Chapter 2, along with circuit techniques to achieve high in-band linearity.

Prior to discussing the prototype implementation, some of the important features of the architecture in Fig. 2.1 that affect the design choices should be highlighted. These include

- The RF section of the receiver (operating at f_{CLK}) can potentially be implemented using all passive circuit blocks to maximize the receiver linearity. Due to the high linearity of passive circuits [57,58], this will put the linearity limitation of the receiver at baseband.

- The amplitude of the signal is reduced at baseband by a factor of approximately $\sqrt{N}$. This means that the IIP3 requirement of the baseband circuitry in dB is approximately $10\log_{10}(N)$ dB lower than the overall system specification.

- Significant effort should be made to employ techniques for maximizing the matching between elements in different channels in order to reduce the non-ideality effects discussed in Chapter 3.

The prototype IC was implemented using fifteen channels. Different design choices for each circuit block are discussed in this chapter. The use of fifteen channels was chosen as a trade-off between complexity of the system implementation, required sampling frequency of the ADCs, and the overall linearity requirement of the system. The circuit was designed to operate for a clock frequency of 1 GHz. Portions of the text in this chapter are from [38].

4.1 System Implementation

The top level diagram of the proposed fifteen channel CMOS IC is shown in Fig. 4.1. For this proof-of-concept demonstration, off-chip analog-to-digital converters were employed to reduce the complexity of the integrated subsystems. However, as will be discussed later, the integration of the ADCs on the same chip can significantly reduce power consumption of the overall system. This can be done in future generations of the system to further enhance the system performance.

Each channel of the system shown in Fig. 4.1 includes a mixer which multiplies the PRBS with the input signal. This is followed by a discrete-time circuit block that collects fifteen samples and performs the averaging. The resulting signal is amplified by the baseband amplifiers and then sampled by the off-chip ADC. To ensure correct timing of the ADC sampling, a reference clock is provided to the ADCs by the CMOS IC. There are several aspects of the system that should be considered for the design of each block such as input matching, noise, linearity, gain, DC power consumption, and signal swings. Next, the design of each individual block is discussed in details.

4.1.1 Discrete-Time Signal Processing Block

The discrete-time signal-processing block consists of the mixer, the sample and hold circuit and the required control signal generation blocks. A simplified schematic diagram of the circuit is shown in Fig. 4.2(a). The signal path consists of a double-

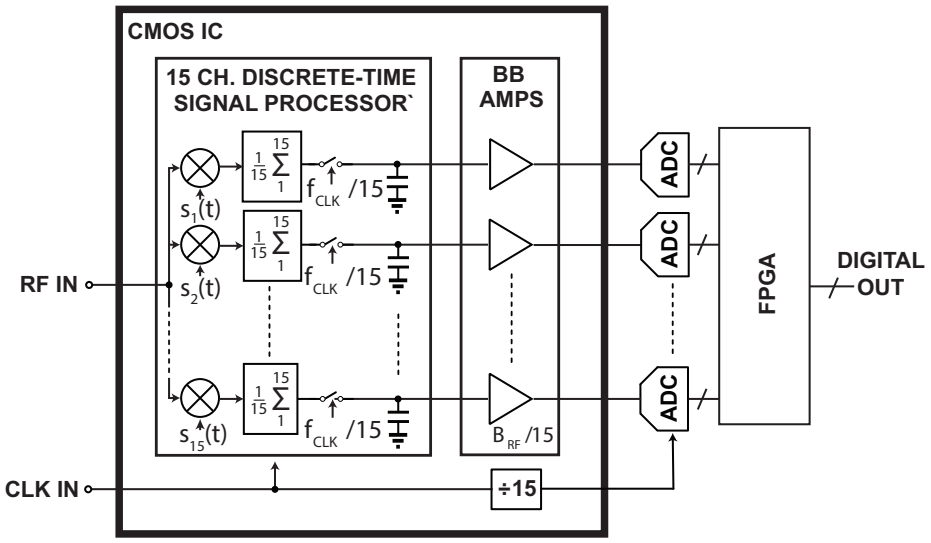

Figure 4.1. Top level schematic diagram of the 15 channel prototype CMOS IC.

balanced passive mixer followed by a switched-capacitor integrator circuit. The double balanced architecture was chosen to minimize the effect of LO to IF feedthrough and even order nonlinearities.

The operation of the circuit can be understood by studying the timing diagram shown in Fig. 4.2(b). Prior to the start of an integration cycle, all capacitors are discharged. This is important to ensure memory-free operation and so that the charge stored on capacitors does not produce re-radiation that propagates out the RF input. During the integration phase ($\phi_1 - \phi_{15}$), charge is stored sequentially on each of the fifteen capacitors. To prevent cross-talk between adjacent samplers, non-overlapping sampling clocks are employed. Moreover, to ensure that the charge remaining on the parasitic capacitance at the output of the mixer (IF node) between sampling operations does not impact the performance, a pair of mixers has been employed. This approach allows for the parasitic capacitance of one mixer to be discharged while the other mixer is processing the RF signal. After the fifteenth sampling operation has completed, the capacitors are connected in parallel (ϕ_{A}), yielding the average voltage stored in the array. This average voltage is then amplified by the baseband

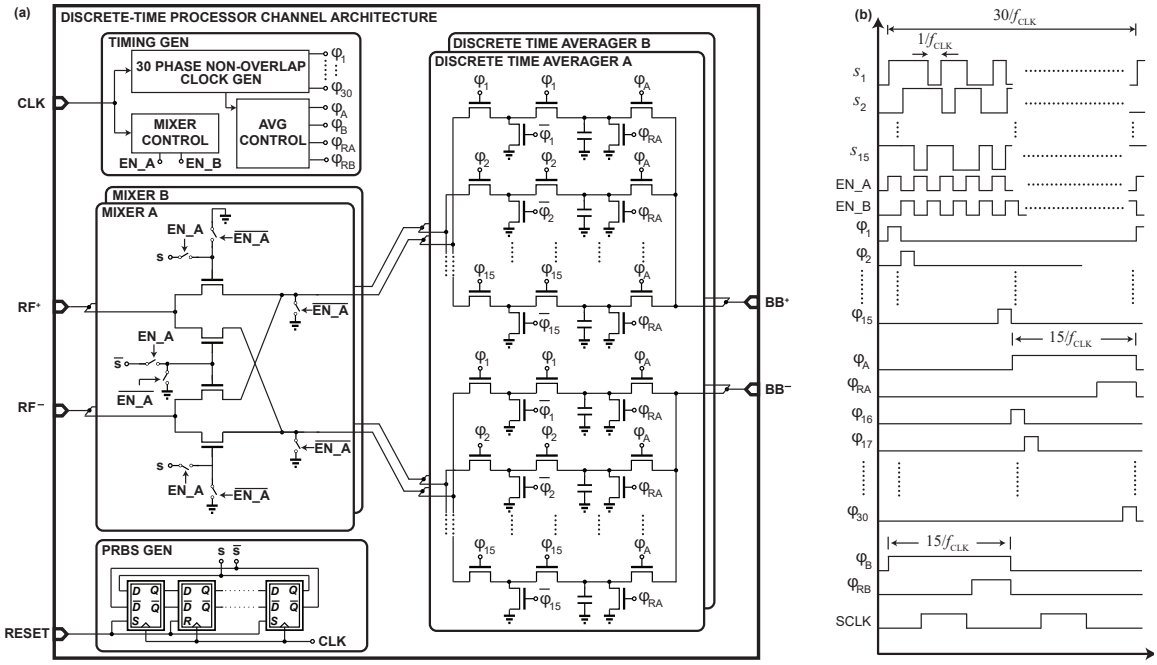

Figure 4.2. (a) Simplified schematic diagram of a single channel of the front-end discrete-time signal processor. (b) Timing diagram. The signal SCLK shown in the timing diagram is generated globally and used to drive off-chip ADCs. Reproduced from [38]©IEEE 2018

amplifier (see Fig.4.1). Finally, the charge is removed from the capacitors to prepare for another sampling sequence (ϕ_{RA}). To avoid dead time while the average charge in a capacitor bank is read out, a pair of differential integrators is employed in a ping-pong style, with one always sampling while the other is being read out. A sampling clock (SCLK) to drive the off-chip ADCs is generated at the top level by dividing the reference clock by a factor of fifteen.

Several aspects of the design are critical to ensuring proper operation. Referring to Fig. 4.2(a), during each sampling instance a series of three switches connects from each RF input terminal to a sampling capacitor. To prevent significant loss due to the on-resistance of each switch, the aggregate series resistance of the mixer and sampling

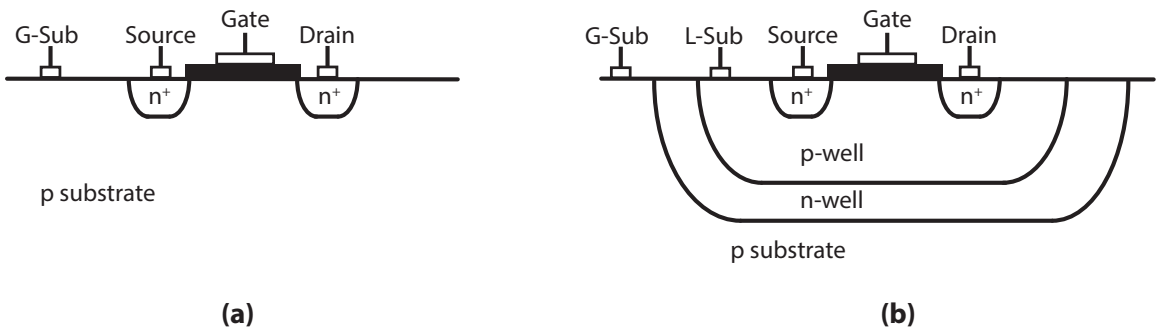

Figure 4.3. Schematic diagram of the cross section of (a) a regular n-FET device and (b) a triple-well n-FET device.

switches should be small with respect to 750 Ω[1]. The transistors within the mixer were sized to be 12 μm×0.13 μm whereas the dimension of each of the two switches employed on the input-side of the sampling circuit were each chosen to be 5 μm×0.13 μm, corresponding to on-resistances of 40 and 96 Ω, respectively. These dimensions were chosen as a trade-off between on-resistance and off-capacitance.

The decision to choose two series switches is to increase the isolation between the sampling capacitor and the IF node at the output of the mixers. Cadence simulations showed significant reduction of charge variation on the capacitors when these switches are used. In addition, to isolate the RF signals from noise in the substrate due to digital signals, all transistors in the signal path are implemented as triple-well devices[2]. Fig. 4.3 shows the schematic diagram of a triple-well device along with that of a regular n-FET device. In the case of the regular n-FET the p substrate is shared among all devices on the same chip and is connected to the lowest voltage. Due to fast transitioning signals digital blocks couple significant noise to the substrate which can be coupled to the RF signal path. However, for a triple-well device, the local substrate (L-sub in Fig. 4.3) is isolated from the global p substrate through an n-

[1]Since fifteen channels are connected in parallel to a 50Ω source impedance each individual channel sees an effective 750Ω resistance to ground.

[2]Also called deep-nwell devices in some cases

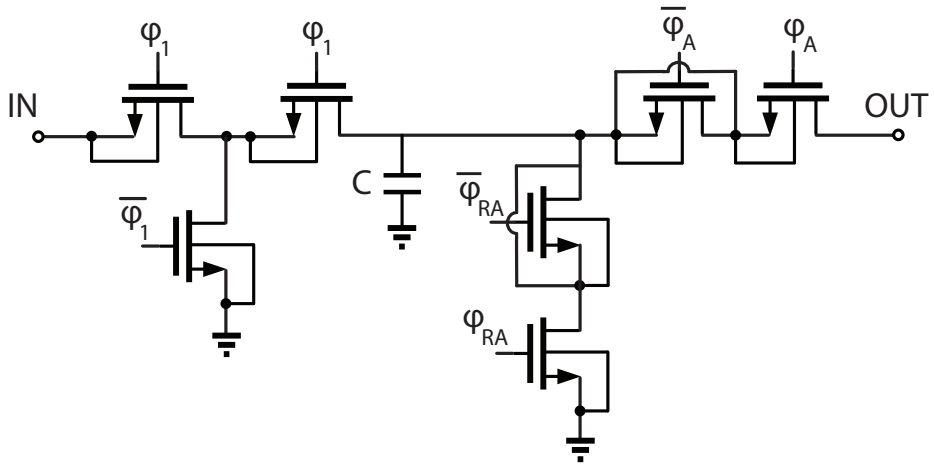

Figure 4.4. Detailed schematic diagram of the switched-capacitor circuit including the dummy transistors to reduce charge injection effects.

well. In addition to providing isolation from the substrate noise, the triple-well device allows for the L-sub to be shorted to the source of the device [59]. This significantly reduces the leakage current through the source-substrate diode (see Fig. 4.4). This proves critical, especially for switches directly connected to the sampling capacitors. In addition, dummy switches for which the drain and source are shorted were used to reduce the effect of charge injection. These devices are sized to half of the size of the sampling switch for which the charge injection is to be canceled [60]. Although this technique does not completely eliminate charge injection, but as discussed in [61] it significantly minimizes its effect. This was also verified through simulations in cadence. Fig. 4.5 shows the time domain simulation of a single channel of the switched-capacitor circuit. This demonstrates the sampling of the input signal on each capacitor and the effect of averaging on reducing the signal swings at the output of the channels prior to the amplifier.

It is important that the sampling capacitors be sized appropriately such that impedance matching is achieved. In [21], the impedance looking into a sampling circuit similar to that employed here was studied. It was shown that the value of the sampling capacitor (C) required to achieve impedance match at low frequencies

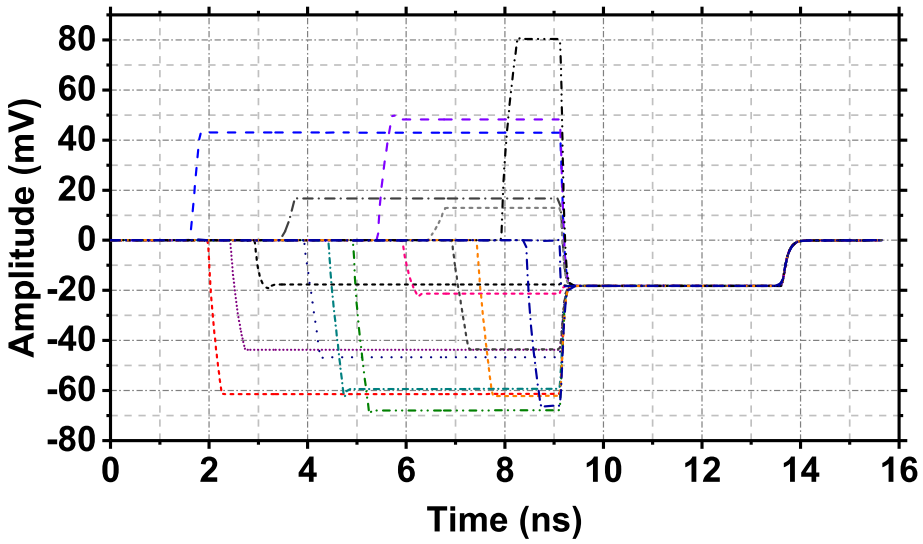

Figure 4.5. Cadence transient simulation of the switched-capacitor circuit demonstrating the sampling and averaging operation of the discrete time signal processing block. Dashed lines show the voltage on each individual sampling capacitor and the solid line shows the voltage at the input node of the baseband amplifier.

is approximately $0.63/f_{\mathrm{CLK}}R_{\mathrm{CLK}}$. For a clock frequency of 1 GHz, an aggregate capacitance of 12.6 pF is required to achieve a single-ended input impedance of 50 Ω (100 Ω differential), corresponding to a value for each sampling capacitor of 840 fF. After taking parasitic capacitances into account, a value of 670 fF was utilized. At the upper end of the RF frequency range, an additional reactive component must be tuned-out to maintain impedance matching. The input reflection coefficient of the circuit without any additional matching network is shown in Fig. 4.6. The low frequency match is quite good for clocking frequencies greater than 600 MHz. Results in Fig. 4.6 for input frequencies above 600 MHz also indicate an effective shunt capacitance. If better input matching is required at higher frequencies this effect can be canceled out by a simple off-chip matching network.

Several design choices were also made in an effort to minimize the systematic errors related to timing skew that were described in Chapter 3. First, the pseudo-random bit sequence required to drive each mixer is generated locally using a fifteen

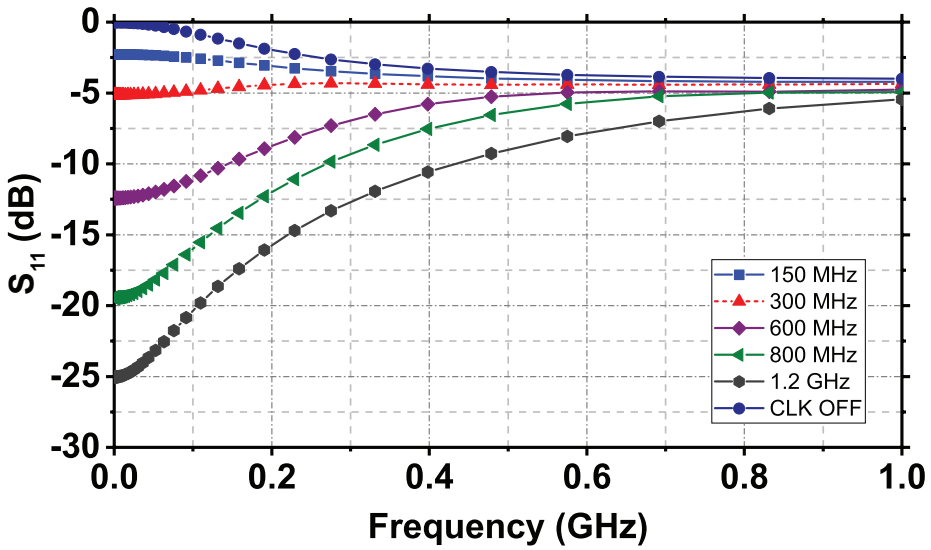

Figure 4.6. Simulated input reflection coefficient for a variety of clock frequencies.Reproduced from [38]©IEEE 2018.

bit circular shift register, which can be initialized with the appropriate PRBS phase. In fact, the sole difference among the fifteen channels is the unique phase of the PRBS sequence that is hard-coded to be loaded into the local shift register during the initialization procedure. In addition, all other non-overlapping signals, such as ϕ_{A} and ϕ_{RA}, are generated locally to each switched-capacitor cell. Doing so reduces the required wiring and interconnects significantly which will be discussed in more detail in the following sections.

4.1.2 Digital Control Signal Generation

The chip was designed to use off-chip low-voltage-differential-signaling (LVDS) clock. The LVDS signal is converted to low-voltage CMOS (LVCMOS) through an on-chip converter. This circuit employs PMOS inputs with a cross coupled load that provides enough gain to cause railing of the output to supply and ground for a small input signal. The schematic of this block is shown in Fig. 4.7 [62]. The circuit is designed for an ac coupled sine wave signal with a minimum amplitude of 300 mV peak-to-peak. The resistors at the input provide the common voltage for biasing of

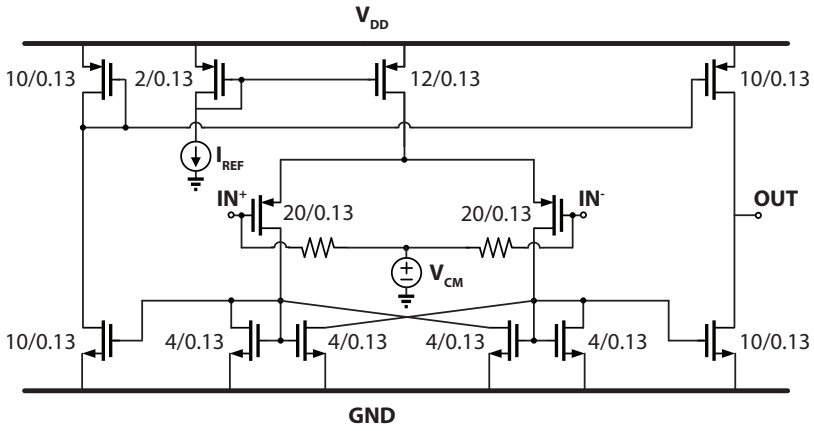

Figure 4.7. Schematic diagram of the LVDS to LVCMOS converter. Off-chip series ac coupling capacitors are required to isolate the bias circuit. For this design $V_{\mathrm{CM}} = 0.6\mathrm{V}$, $V_{\mathrm{DD}} = 1.2\mathrm{V}$, and $I_{\mathrm{REF}} = 250$ uA

the input transistors. The circuit was verified through simulation to operate for clock frequencies up to 4 GHz. Fig. 4.8 shows the simulation result of the circuit for a clock frequency of 2 GHz.

The reference clock generated by the circuit of Fig. 4.7 is gated by a reset signal that is provided from off-chip, and then buffered to be distributed across the chip. The reset signal is used to initiate the sequences at each channel when the chip is powered up. Master-slave D flip-flop blocks are used as storage elements for all shift registers (see Fig. 4.9(a)). The required non-overlapping signals are generated locally in each channel using a shift register based approach in conjunction with the appropriate gating (see Fig. 4.9(b)).

To generate the required ϕ_{A}, ϕ_{RA}, ϕ_{B}, and ϕ_{RB} signals in Fig. 4.2, a simple digital logic circuit was employed as shown in Fig. 4.10(a). In addition, the required SCLK for driving the off-chip ADCs is generated from a separate block at top level which is showed in Fig. 4.10(b). Due to the limited slew rate, to allow time for the discharge of the sampling capacitors the ϕ_{RA} and ϕ_{RB} are extended for 5 clock cycles.

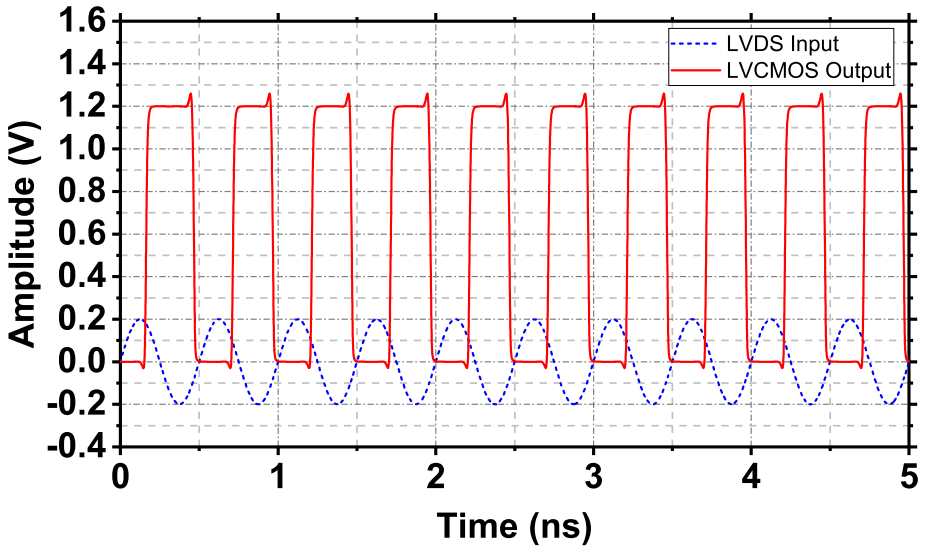

Figure 4.8. Simulation results of the LVDS to CMOS converter for clock frequency of 2 GHz.

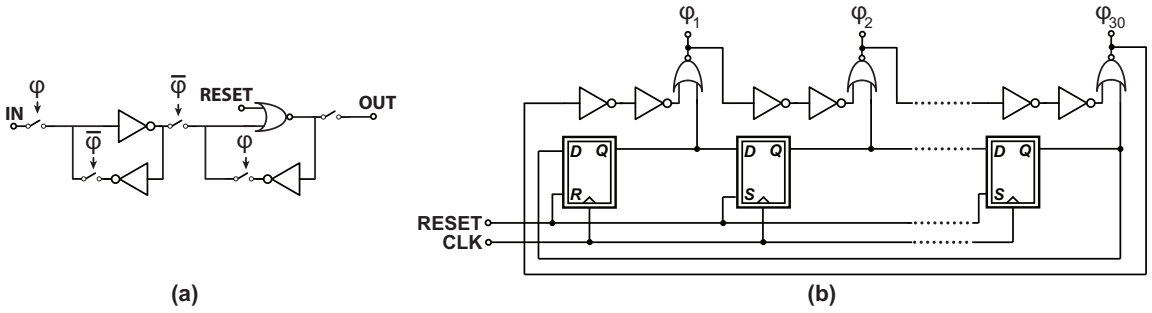

Figure 4.9. Simplified schematic diagram of the (a) D flip-flop circuit and (b) non-overlapping phase generator.

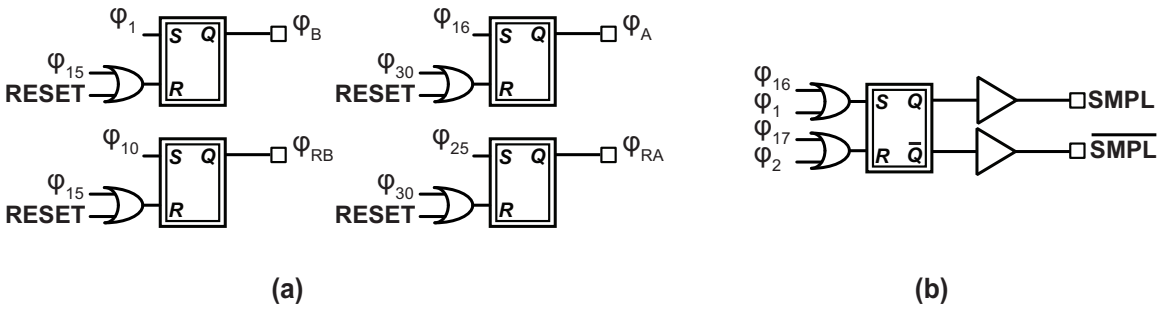

Figure 4.10. Schematic diagram of (a) the control signals generator and (b) the ADC reference clock generator

4.1.3 Baseband Amplifier Design

The performance of the baseband amplifier is critical as it determines the limit on the overall system linearity and noise performance. Since the ADCs were left off-chip, the baseband amplifiers need to be able to drive a resistive load at the full swing of the ADC. To employ the full ADC effective-number-of-bits (ENOB) the amplifier output 1 dB compression point should be beyond the full scale of a commercial ADC. In addition, as the amplifier is the sole active element in the system, its power consumption dominates that of the overall chip and should be optimized.

Considering the aforementioned criteria, a fully-differential two-stage amplifier was designed. To accommodate the outputs from the discrete-time signal processor, the amplifiers were designed to have an input common-mode voltage of 0V. This allows for direct connection of the receiver to the antenna with no complicated biasing scheme required. This was accomplished through the use of a negative supply rail of $V_{\rm SS}$ = -0.65 V. Triple-well devices were employed for all NMOS devices used in the amplifier to prevent the need for biasing the substrate at a negative voltage. The positive supply rail was set to $V_{\rm DD}$ = 1.75V. To prevent these supply levels from exceeding the breakdown voltage of the devices, thick oxide devices with a gate length of (L=0.2μm) were employed. The breakdown voltage of these devices is 2.5 V.

Large area devices (100 μm$\times$0.2μm) were employed for the input transistors to minimize $1/f$ noise and a tail current of 3mA ($g_{\rm m1} = g_{\rm m1} \approx$ 22.5 mS) was selected as a trade off between gain and noise performance. The overall small signal voltage gain of the amplifier can be estimated as

$$A_{\rm v} \approx g_{m,in} R_L \frac{(W/L)_{7,8}}{(W/L)_{3,4}}, \tag{4.1}$$

where $g_{m,in} = g_{m,1} = g_{m,2}$ is the transconductance of the first stage and R_L is the load resistance. The DC current of the second stage is coupled to that of the first stage by the ratio of the PMOS current mirror transistors. Reducing this ratio would directly

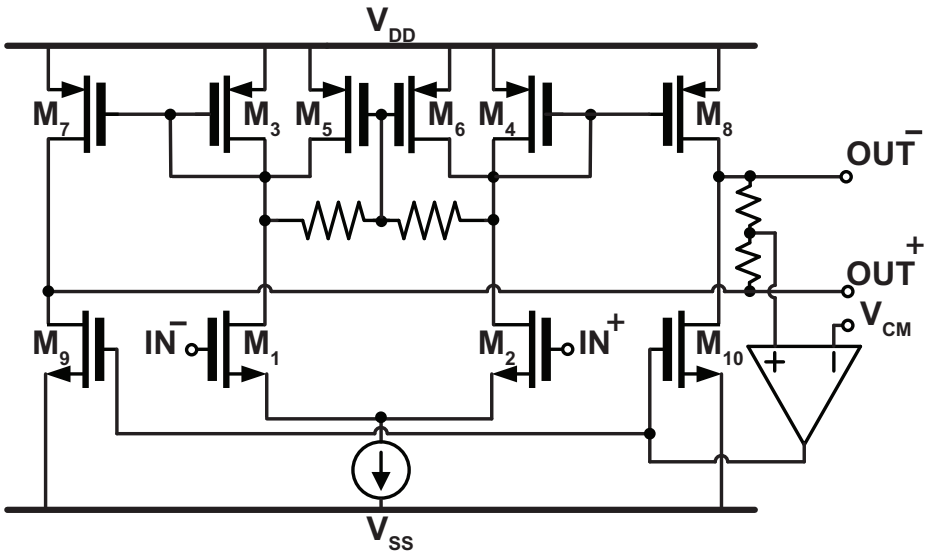

Figure 4.11. Simplified schematic diagram of the baseband amplifier including the common-mode feedback loop to set the output DC voltage.

impact the small signal gain. The required output stage current is set by R_{L} and the voltage swing required to drive the ADC. Having large ratios of $(W/L)_{7,8}/(W/L)_{3,4}$ to maximize the gain, would result in excessively small DC currents in the first stage which reduces $g_{m,in}$ and degrades the noise performance of the amplifier. To decouple the small signal gain and the DC current ratios of the mirror devices, additional transistors (M_5 and M_6) were added which steer some of the DC current but have little effect on small signal gain.

The output stage was designed to linearly drive $2V_{pk-pk}$ into an ADC when terminated differentially in 300Ω. This relatively large load impedance was selected to reduce the power consumption required to drive off-chip components. Transistors M7 and M8 were sized such that they each draw a drain current of 4 mA. The common-mode voltage at the output was set by a common-mode feedback loop, referenced to a voltage (VCM), which was supplied from off-chip.

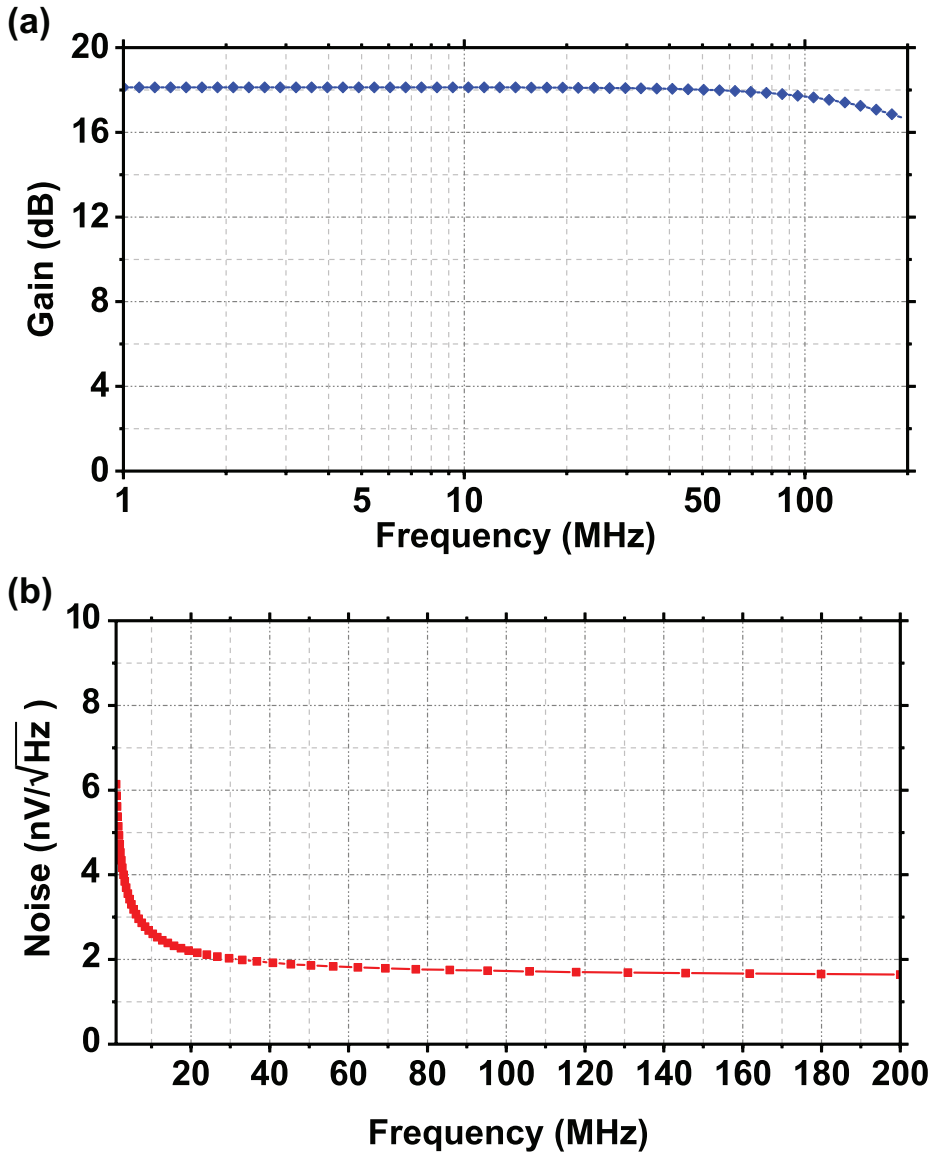

Figure 4.12. Simulation results of (a) baseband amplifier small signal gain and (b) noise.

Simulation results of the baseband amplifier small signal gain are shown in Fig. 4.12(a) for a load of 300Ω in parallel with a 1.5 pF capacitor[3]. The amplifier has a gain of 18 dB at DC with a 3 dB bandwidth of ≈ 300 MHz. Simulation results of the amplifier noise are shown in Fig. 4.12. Employing (2.28), for the system operating at f_{CLK}/N to $f_{\mathrm{CLK}}/2$, the simulated noise of approximately 3 $\mathrm{nV}/\sqrt{Hz}$ at 10 MHz would result in a system noise figure of approximately 13.5 dB. For a clock frequency of $f_{\mathrm{CLK}} = 2\,\mathrm{GHz}$ the baseband sampling frequency (f_{s}) would be about 133 MHz. The extra bandwidth of the amplifier can result in excess integrated noise. Hence, off-chip filtering can be used to reduce such effects.

The linearity of the amplifier sets the overall linearity of the receiver system. Simulation results for the 1 dB compression point and IIP3 of the amplifier are shown in Fig. 4.13. The input 1 dB compression point for $V_{\mathrm{cm}} = 900\,\mathrm{mV}$ is $150\,\mathrm{mV_{peak}}$ and for $V_{\mathrm{cm}} = 800\,\mathrm{mV}$ is $140\,\mathrm{mV_{peak}}$. The IIP3 of the amplifier for the $V_{\mathrm{cm}} = 900\,\mathrm{mV}$ is equal to -4.8 dBm. Based on the analysis presented in Chapter 2 this value correspond to an average IIP3 of 6.7 dBm for the overall system.

The overall noise figure of 13.5 dB calculated based on the noise of the amplifier may be larger than what is acceptable for some wireless communication systems. Hence, for future generations of the system further efforts should be made to improve the noise performance of the baseband amplifier as the main source in the system. In addition, techniques such as the use of feedback should be employed to further enhance linearity of the baseband amplifier.

To ensure that variations due to fabrication do not have severe effect on amplifier performance, Monte Carlo simulations were run using Cadence ADE-XL tool. Simulation results of the amplifier frequency response over 100 runs are shown in Fig. 4.14. These simulations include both process and mismatch variations. In all cases the

[3]This capacitance value was picked as an example based on the input circuitry of Linear LTM9011 ADC.

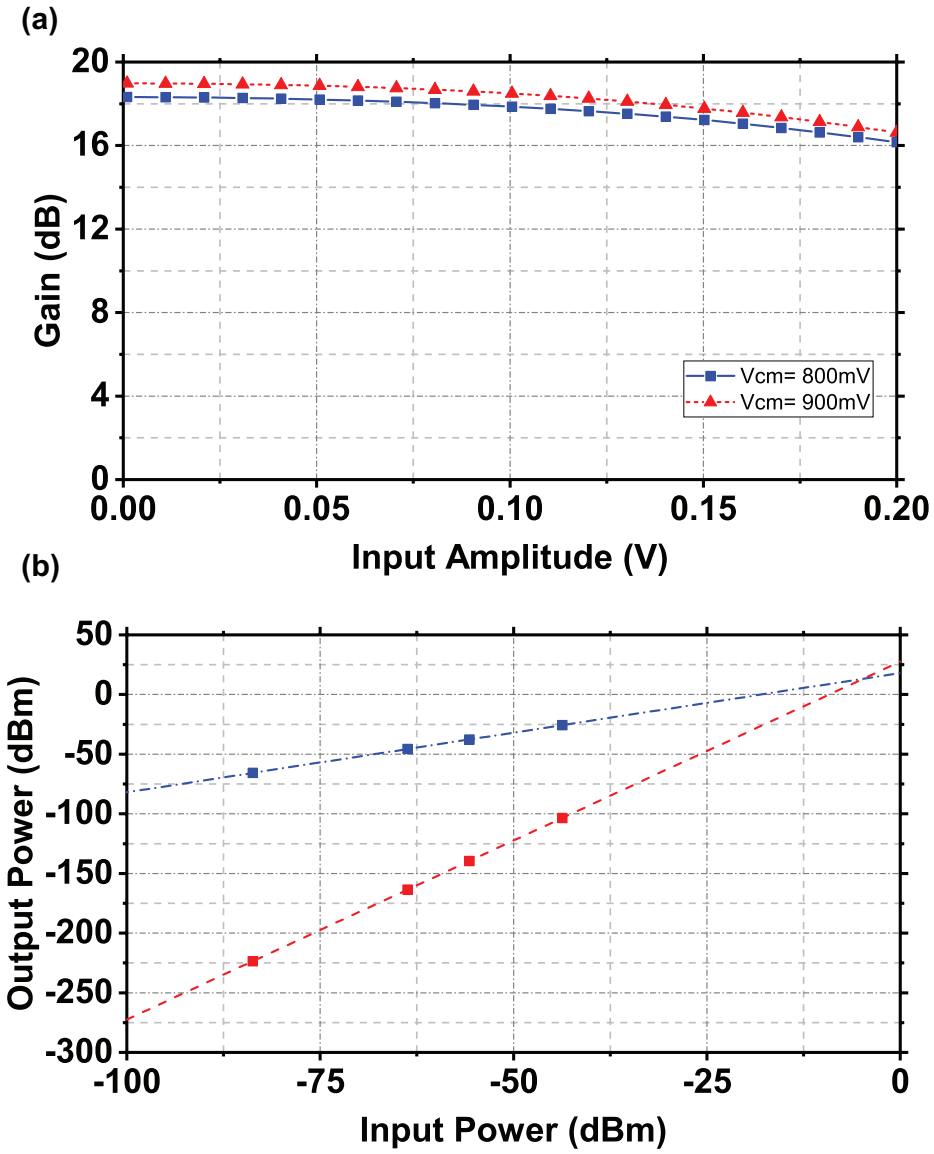

Figure 4.13. Simulation results of (a) the baseband amplifier gain compression for two output common mode voltages of 800 mV and 900 m and (b) the baseband amplifier IIP3 for V_{cm} of 900mV.

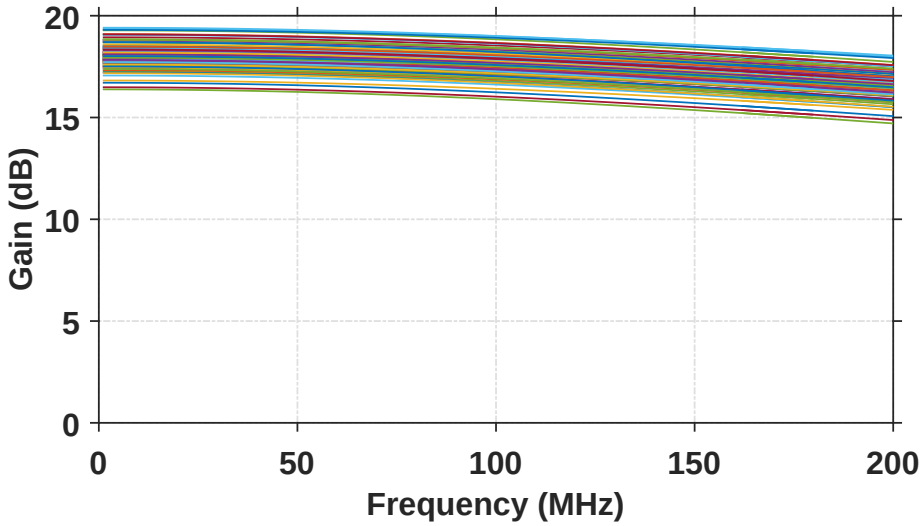

Figure 4.14. Monte Carlo simulation results of the baseband amplifier frequency response over 100 runs. Results include both process and mismatch variations.

gain of the amplifier is within ± 1.5 dB of the nominal point which is tolerable for this design.

Using Cadence Calibre PEX tool the layout parasitics of the baseband amplifiers were extracted to ensure they do not severely impact the performance. The resulting circuit was simulated and compared to the ideal schematic simulations and results are shown in Fig. 4.15. The effect of parasitic elements are negligible and only reduce the gain by about 0.3 dB. Hence no major modification to layout of the cell was necessary.

4.2 Summary

In this chapter, a prototype CMOS implementation of the proposed technique was implemented and several factors impacting design choices were discussed. In this design, the required ADCs were left off-chip to reduce the complexity of the design. A double balanced passive mixer along with a thirty-phase passive switched-capacitor block form the RF portion which provide the multiplication with the PRBS and averaging. It was discussed that sampling capacitor sizes set the input reflection coefficient of the overall system and should be sized according to clock sampling

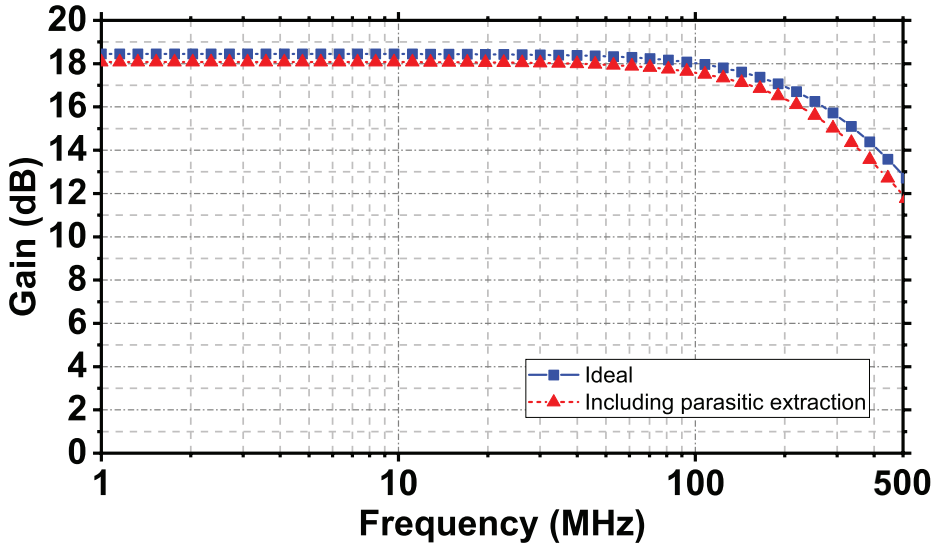

Figure 4.15. Comparison of the simulation results for ideal schematic versus the layout parasitic extracted circuit.

frequency. It was highlighted that the implementation of the RF portion using all passive circuits puts the linearity limitation of the system at baseband.

Cadence simulation results were shown to highlight the expected performance of different parts of the system. The design of the baseband amplifier optimized for driving off-chip DC-coupled ADCs at a full swing of 2 $V_{p\text{-}p}$ was described. The amplifier noise performance was evaluated which results in an expected system noise figure of 13.5 dB. The IIP3 of each individual amplifier was simulated to be approximately -4.8 dBm which corresponds to an average IIP3 of 6.9 dBm for the overall system.

CHAPTER 5

MEASUREMENT RESULTS OF THE PROTOTYPE IC

In this chapter, the design of the required PCB and data acquisition system along with measurement results of the fabricated integrated circuit are presented. Different performance metrics of the system are characterized and compared to the expected values from Chapter 4. The performance is also compared with the available state-of-the-art wideband receiver systems. Portions of the text in this chapter are from [38].

The CMOS integrated circuit was fabricated using Global Foundries BiCMOS8HP technology. This technology includes CMOS devices with minimum gate length of 120 nm. The die photo of the fabricated chip is shown in Fig. 5.1. The chip requires 78 bond pads for all signal, supply and ground connections. As a results the dimensions of the chip is pad limited and to save area a two row approach was used for the pads on the top and bottom rows.To ensure minimum skew between channels, clock and RF signals were distributed among the channels using an H-tree distribution approach.

The chip was mounted on a custom printed circuit board (PCB) for testing. In addition, a custom made data collection board was required to collect the outputs of the fifteen channels synchronously which would allow for reconstruction of the signal and further processing in the digital domain.

5.1 PCB Design

A three layer PCB was designed for testing of the fabricated IC. The PCB consists of two dielectric layers. The bottom layer is a 50 mil thick FR4 and the top layer is a 10 mil thick Rogers RO4350b. The latter was chosen due to its lower dielectric

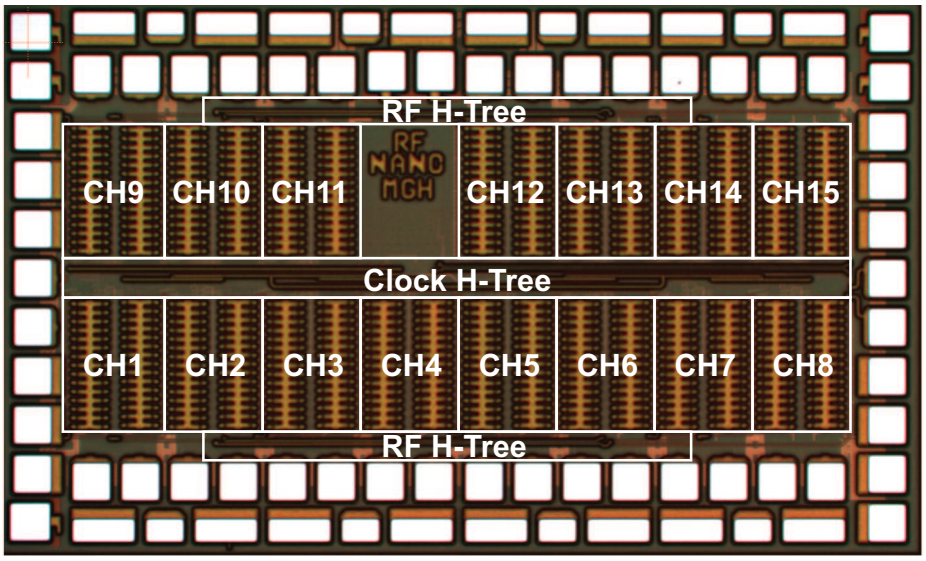

Figure 5.1. Die photo of the fabricated IC in Global Foundries BiCMOS8HP technology.Reproduced from [38]©IEEE 2018.

constant (≈ 3.3) for better RF performance. A 0.5 oz copper layer was used as the conductor for each layer. Gold plating was used on top of the copper traces to enable direct wire bonding of the chip to the PCB. Fig. 5.2 shows a simplified block diagram of the PCB.

The chip requires three separate supply domains incldluing $V_{DD,RF}$= 1.2 V, $V_{DD,AMP}$= 1.75 V, and $V_{SS,AMP}$= -0.65 V. To provide a clean supply to the chip, commercial low noise voltage regulators were used(Linear LT3021-1.8, LT3021-1.2, and LT3090). To monitor the current through each supply voltage a small series resistance was used on each supply lane. High speed digital transceivers (Nexperia 74AVC1T45) were used to buffer the ADC reference clock provided by the chip.

To ensure matched timing, the electrical length of PCB traces for each channel were matched through the use of interactive length matching capability of Altium software (see Fig. 5.3). All differential lines on the PCB are matched within 0.1% of the maximum length. Multiple ground vias were placed between adjacent lines which

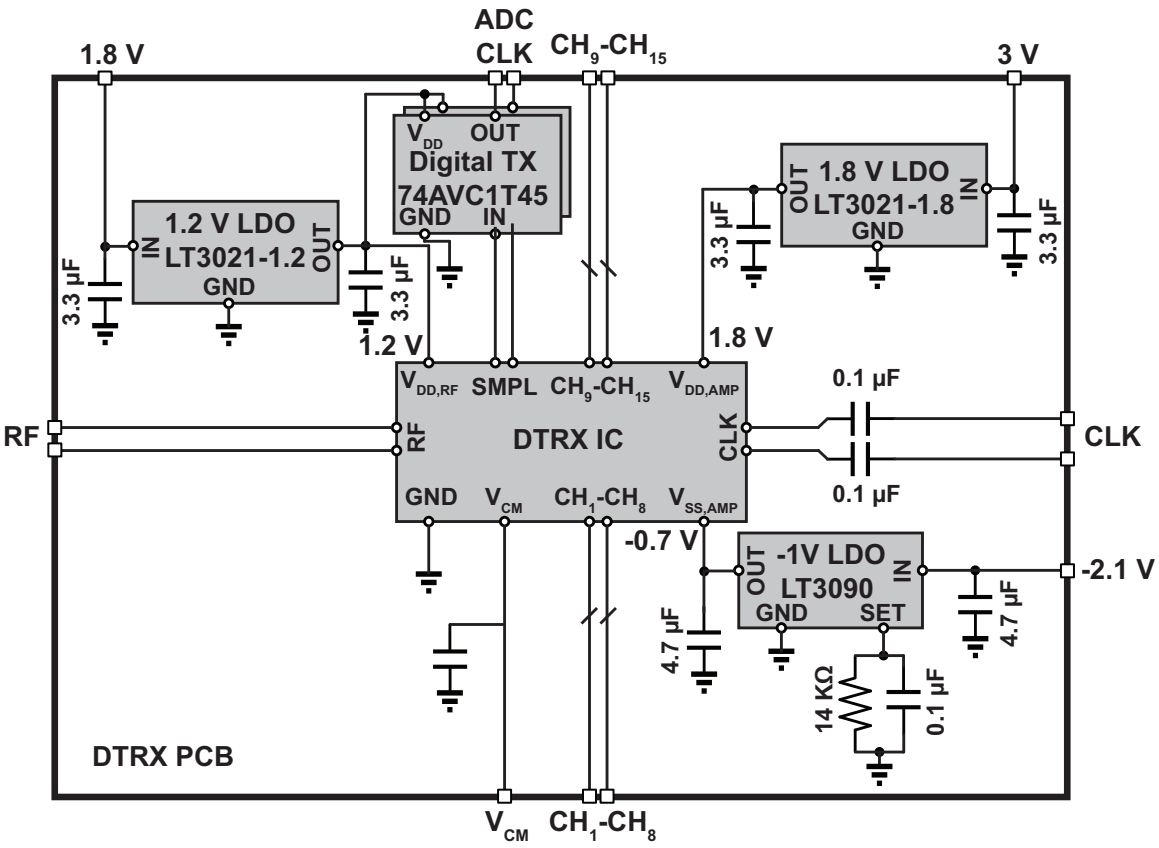

Figure 5.2. Block diagram of the PCB designed for testing of the prototype IC.

confine the electric field in each transmission line and minimize the coupling between them.

The RF and clock traces were routed differentially from the input SMA connectors to the chip with vias placed closely in order to form a coplanar wave guide (CPW) transmission line with a characteristic impedance of approximately 50 Ω. To model the effect of the RF traces on the input match of the system, a schematic model was developed in Microwave Office software by importing the s-parameter simulation results of the IC from Cadence. A block diagram of the setup is shown in Fig. 5.4(a). The CPW lines were added to model the traces on the PCB. In addition, a shunt capacitance of 100fF and a series inductance of 0.5 nH were added to each line to model effect of the pad capacitance and wire bond inductance respectively. Fig. 5.4(b)

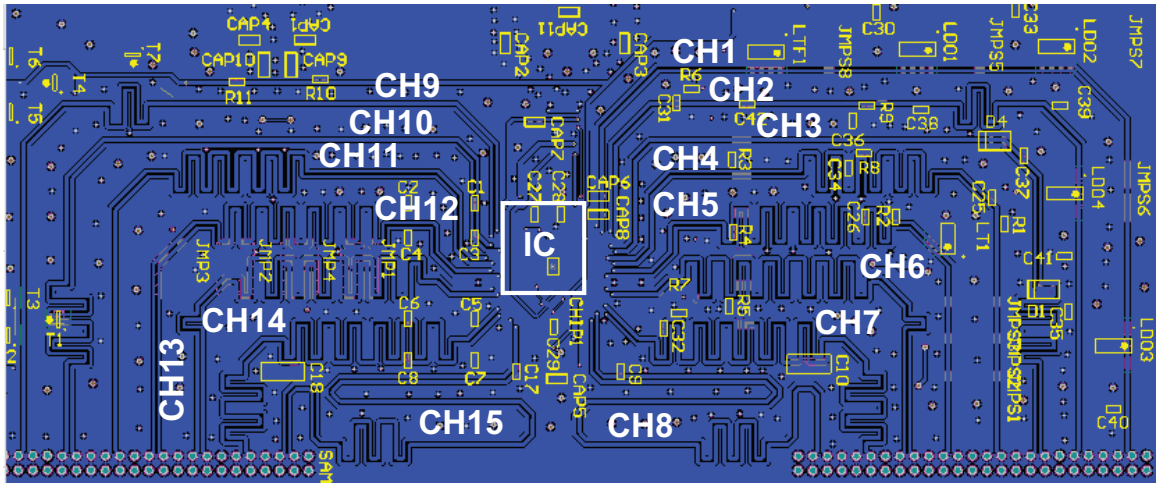

Figure 5.3. Bottom side of the PCB. The lines for all channels are matched to less than 0.1% to ensure matched phasing.

shows the S_{11} simulation results of the overall system. The reactive elements added due to the RF traces on the PCB improve the input match at higher frequencies compared to the reference simulations of the IC shown in Fig. 4.6.

5.2 Custom Data Collection Board Design

Fifteen ADCs are required to collect the output signals of all channels. Three important factors were considered for choosing the ADCs including

- ADC resolution- To ensure that the ADC is not the limiting factor for the overall system noise performance, its quantization error should be below the noise floor of the receiver at the baseband amplifier output. Based on the noise analysis presented in Section 4.1.3 and the gain of the baseband amplifier, the noise power per unit Hz of the receiver at the output of each channel can be written as

$$N_{\text{out}} = k \times T_0 \times F \times G_{\text{V}}^2 \times \frac{R_{\text{S}}}{R_{\text{L}}} \tag{5.1}$$

where k is the boltzman constant, T_0 is the ambient temperature, F is the noise figure, G_{V} is the voltage gain, R_{S} is the source impedance, and R_{L} is the load

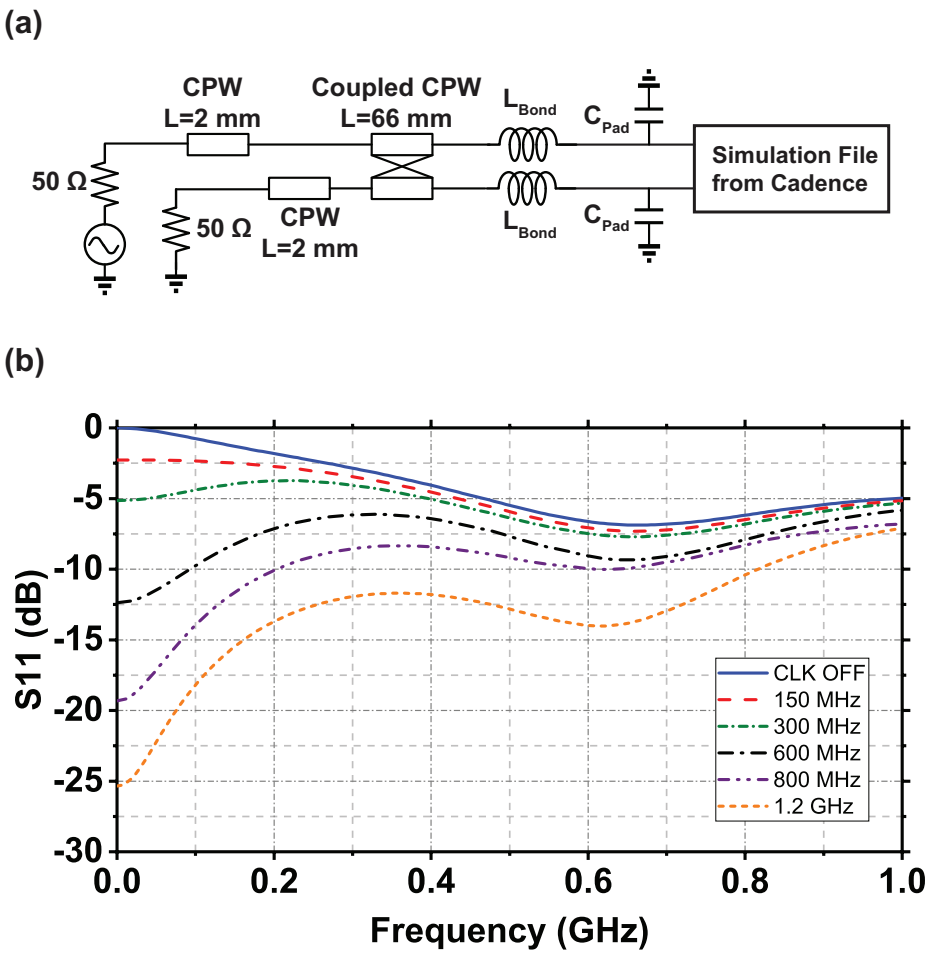

Figure 5.4. (a) Block diagram of the simulation setup in Microwave Office using the extracted S-parameter files from Cadence. For this simulation a bond wire inductance of 0.5 nH and a pad capacitance of 0.1 pF was assumed.(b) S_{11} simulation results of the system for different clock frequencies including effect of PCB traces on RF lines.

impedance. To ensure that the noise floor of the ADC does not limit the overall performance of the system, its input referred noise spectral density was chosen to be less than 5% of the output noise of each channel. Thus the ADC spectral noise density can be written as

$$N_{\mathrm{ADC}} = \frac{1}{20} N_{\mathrm{RX,out}}, \tag{5.2}$$

thus

$$N_{\mathrm{ADC}} = \frac{1}{20} k \times T_0 \times F \times G_{\mathrm{V}}^2 \times \frac{R_{\mathrm{S}}}{R_{\mathrm{L}}}. \tag{5.3}$$

The total integrated noise power of the ADC with the RF input bandwidth of BW_{ADC} can then be found as

$$N_{\mathrm{ADC}} = \frac{1}{20} k \times T_0 \times F \times G_{\mathrm{V}}^2 \times \frac{R_{\mathrm{S}}}{R_{\mathrm{L}}} \times BW_{\mathrm{ADC}}. \tag{5.4}$$

As the noise performance of ADCs is commonly specified in terms of the effective-number-of-bits (ENOB), it is helpful to find the required ENOB in terms of the desired noise floor. The ENOB of an ADC can be approximatly written in terms of the signal-to-noise ratio in dB as [63]

$$ENOB = \frac{SNR_{\mathrm{ADC}}(dB) - 1.76}{6.02}. \tag{5.5}$$

As a result, to find the required ENOB of the ADC the total SNR should calculated. For an ADC with a peak voltage of V_{p} and an input termination of R_{L}, the SNR can be written as

$$SNR_{\mathrm{ADC}} = \frac{{V_{\mathrm{p}}}^2}{2R_{\mathrm{L}}} \times \frac{1}{N_{\mathrm{ADC}}}. \tag{5.6}$$

From (5.4), (5.5), and (5.6) the desired ENOB of the ADC to ensure a small noise contribution to the overall system performance can be found.

For the system proposed in Chapter 4 the noise power in dBm can be written as

$$N_{\mathrm{out}} = -174\mathrm{dBm/Hz} + 13\mathrm{dB} + 13.3\mathrm{dB} = -147.7\mathrm{dBm/Hz}, \tag{5.7}$$

where 13.3 dB is the power gain from the 100 Ω input to the 300 Ω load at the amplifier output. To ensure that the noise contribution of the ADC is below 5% of the system noise, a maximum noise floor of -160 dBm for the ADC is

required. Therefore, for an ADC with sampling rate of 100 MSps with effective anti-aliasing filtering, the total integrated noise power is found as

$$N_{\text{ADC}} = -160\ dBm/Hz + 10\log_{10}(50 \times 10^6) = -83\ \text{dBm}. \tag{5.8}$$

For an ADC with a maximum input swing of $2\,V_{\text{p-p}}$ which is terminated in 300 Ω, the maximum input signal power is $\approx 2.2\,\text{dBm}$. Hence, the SNR of the ADC should be above 85 dB. Then using (5.5), the desired ADC should have an ENOB of 13.8 bits.

- ADC sampling speed and number of channels- The sampling frequency of the ADC is set by the RF sampling clock of the IC. For a correct operation of the system, fifteen synchronized ADCs are required to collect the data at baseband.

- ADC analog input network- Since the chip was designed to drive a 300 Ω DC coupled differential ADC, the data collection board should be compatible with this setup.

Considering the above requirements, initially two LTM9011-14 eight channel ADC boards from Linear Technology were chosen. These boards include eight 14 bit 125 MSps ADCs and the required clock driving circuitry. The input of the ADC boards are DC coupled and were modified by replacing the 100Ω terminations with 300 Ω resistors differentially. The boards provide a 0.9 V reference voltage which can be used as the common mode DC signal for the output amplifier driving the ADC.

To complete the data collection system, the two ADC boards must be synchronized and triggered at the same time. This functionality is not provided by the manufacturer, thus a means of synchronized data collection from ADC outputs was required. To do so, a Xilinx KCU105 evaluation board was employed. A block diagram of the setup is showed in Fig. 5.5. Multiple designs were implemented using the

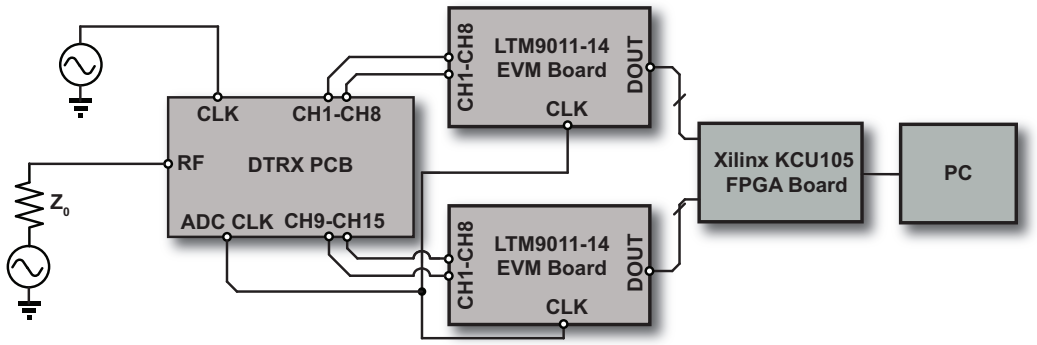

Figure 5.5. Block diagram of the measurement setup employing two LTM9011-14 ADC EVM boards and a Xilinx KCU105 FPGA board.

FPGA board to enable simultaneous data collection from the two boards, however, due to the large number of memory elements required, all of the implemented designs limited the ADC maximum frequency of operation to 30 MHz[1]. It should be noted that the ADC provides two lanes of 8 bit words for each input sample which results in serial data rates of greater than 400 MHz for ADC data rate of 50 MSps. Hence, the FPGA should be able to accommodate thirty of these high speed lanes along with additional reference clock lanes and the required memory elements to store the data. As will be discussed in the Chapter 6, this setup was used for performing calibration of the IC at low RF clock frequencies of 150 MHz, however, the data rate was too low for the normal system operation.

A second option was considered for the data collection which employed ADC boards with maximum sampling rates of 80 MSps which enabled basic evaluation of the system performance for maximum RF sampling frequency of 1.2 GHz. Two ADS5294 evaluation module (EVM) boards from Texas Instrument with 8 channel 14 bit 80 MSps ADCs were chosen. These boards accompanied with TSW1400 FPGA boards from Texas Instruments enable synchronous data collection of the 15 channels

[1]corresponding to a RF sampling frequency of 450 MHz

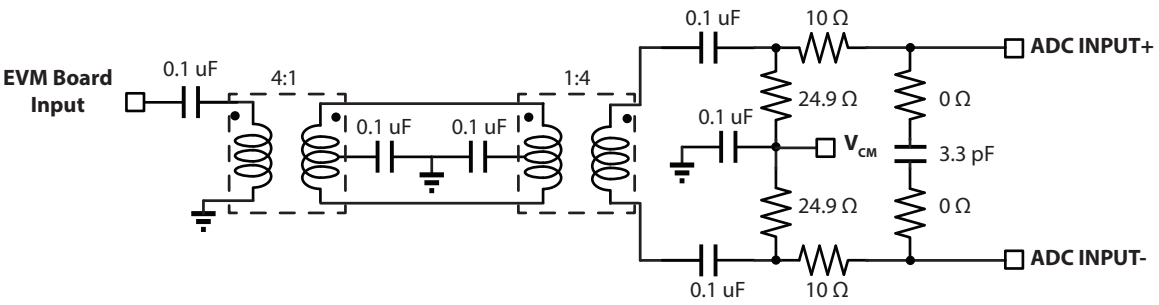

Figure 5.6. The schematic diagram of the ADS5249 EVM board input circuitry.

from the chip. The input circuitry of the EVM board is showed in Fig. 5.6. The board has a single ended ac-coupled input for each channel.

Since the chip and the PCB were designed to drive a differential DC couple ADC board, an adapter board was required. The adapter board provides the common mode voltage for the baseband amplifiers, performs the transformation of the impedance, and converts the differential signal to a single-ended output. To provide additional gain in the system an amplifier based approach was chosen for impedance transformation as shown in Fig. 5.7. Due to the virtual ground at the input of the amplifier, the differential input impedance of the circuit is 300 Ω. This circuit was designed to provide additional voltage gain of 2 V/V. This gain has been de-embedded from all measurement results reported in this chapter. An AD8139 rail-to-rail amplifier from Analog Devices with 3 dB bandwidth of 410 MHz was used in each channel. The amplifier can drive the full input swing of the ADC with minimal harmonic distortion. The noise of the amplifier is only $2.25\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$, which is an order of magnitude less than the noise produced at the output of the baseband amplifier. This results in minimal degradation to the overall noise figure of the system due to the adapter board. Similar to the main PCB, all signals were routed with the same electrical length to ensure matched delays between channels.

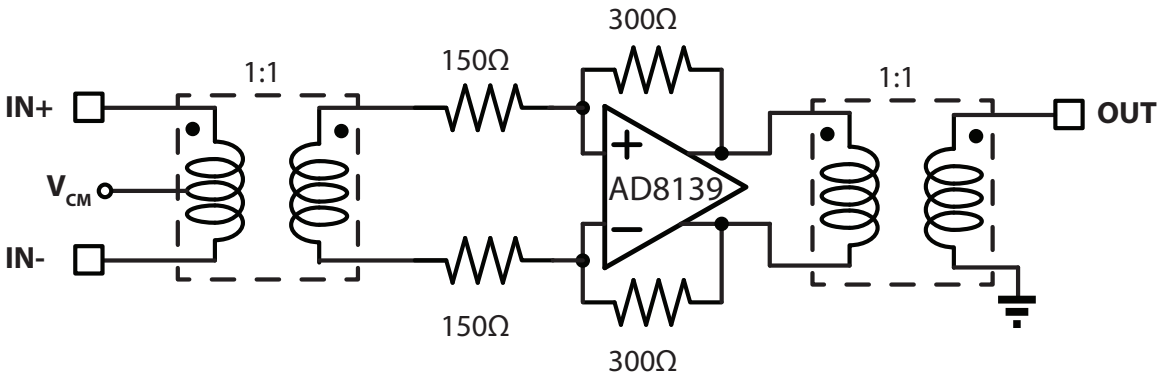

Figure 5.7. Schematic diagram of the single channel of the adapter board.

5.3 Complete Measurement Setup

The die was mounted on the PCB and characterized using the measurement setup shown in Fig. 5.8. A block diagram of the overall setup is shown in Fig. 5.9. The RF input was generated using a Keysight M8190A arbitrary waveform generator (AWG) and the clock signal was sourced from a Keysight E8257D signal generator. The two sources were synchronized using the 10MHz reference of the CW generator. The AWG signal level was set using a step attenuator, with the power calibrated at the reference plane of the PCB input.

To provide a clean clock signal to the ADC, a driving board buffers the ADC reference clock signal provided by the chip. One important aspect of the measurement setup is to ensure that ADC sampling is correctly timed with respect to the data from the channels. Since the channel outputs go through the adapter board and different length paths compared to the ADC reference clock provided by the chip, a variable delay board was designed to ensure correct timing (see Fig. 5.9). The board employs a MC100EP196 programmable delay generator which operates using emitter coupled logic (ECL) input and outputs. The IC can produce delay values ranging from 0 to 10.24 ns with 10 ps steps. Since the ADC reference clock signal provided by the chip is a 1.2 V low-voltage CMOS (LVCMOS) signal, a NB6L16 IC was used to convert

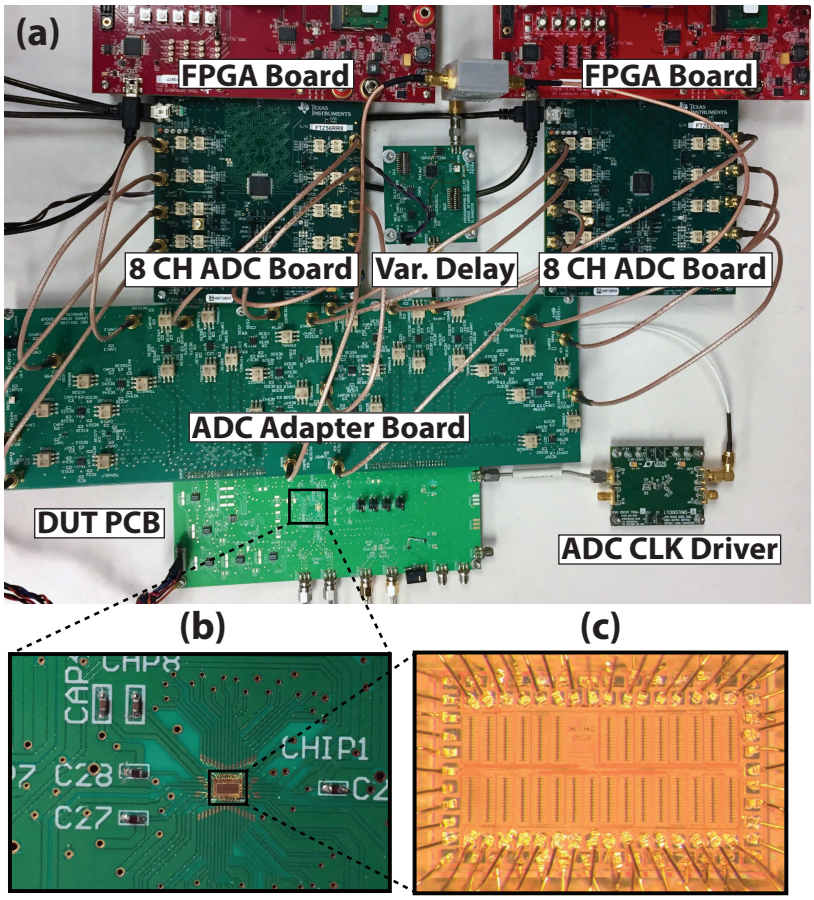

Figure 5.8. Photograph of (a) Measurement setup,(b) assembled PCB, and (c) the wire-bonded chip.

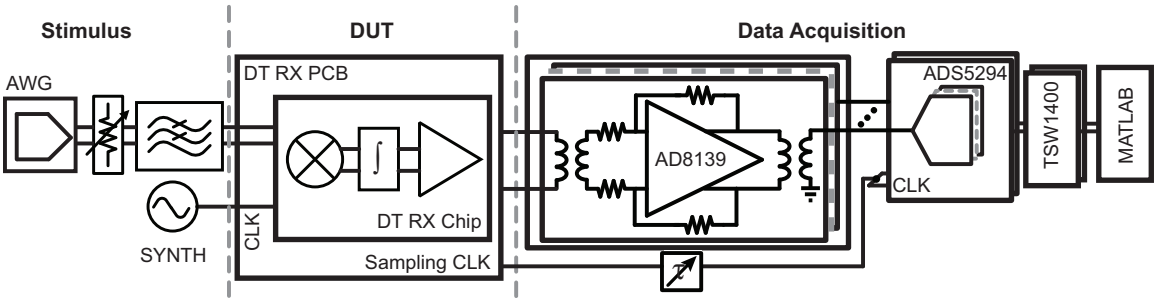

Figure 5.9. Schematic diagram of the complete measurement setup.

this signal to the required ECL signal. The reverse conversion is performed at the output of the delay generator to the ADC clock inputs using a 83021I IC.

The output signals of the ADC boards are collected through two TSW1400 ADC data collection FPGA boards that are synchronized with each other. The FPGA board receives a reference clock from the ADC board to ensure correct data sampling. The data is imported to a PC through the use of Texas Instruments High Speed Data Converter Pro software and then imported to Matlab for reconstruction and further processing. Matlab codes to process the data are available in Appendix B.

5.4 Time Domain Measurements

First, the chip was tested with a sinusoidal excitation to verify the feasibility of the reconstruction procedure from the baseband samples. Reconstruction was possible for clock frequencies as high as 1.2 GHz (f_{RF} =DC-600 MHz). However, at clock frequencies above 800 MHz, the gain was found to roll-off with increasing clock frequency. This is believed to be related to insufficient bandwidth in the clock path. With the exception of the input return-loss, all measurements reported in this chapter are limited to clock frequencies of 600MHz to ensure that any roll-off in the sampling circuit did not artificially increase the linearity performance of the system. The high clock frequency test was carried out by the initial test setup explained in Section 5.2 employing the LTM9011 devices and the custom FPGA programming as described in the previous section. Due to timing issues with the FPGA this setup did not provide reliable measurements and multiple iterations had to be done for a correct data collection. Since the measurements were limited to clock frequency of 600 MHz the data collection setup shown in Fig. 5.9 was used for all other measurements reported in this chapter.

The reconstructed waveform and channel outputs (measured with an oscilloscope) appear in Fig. 5.10(a) for a sine wave RF input and clock frequencies of 58 and 600

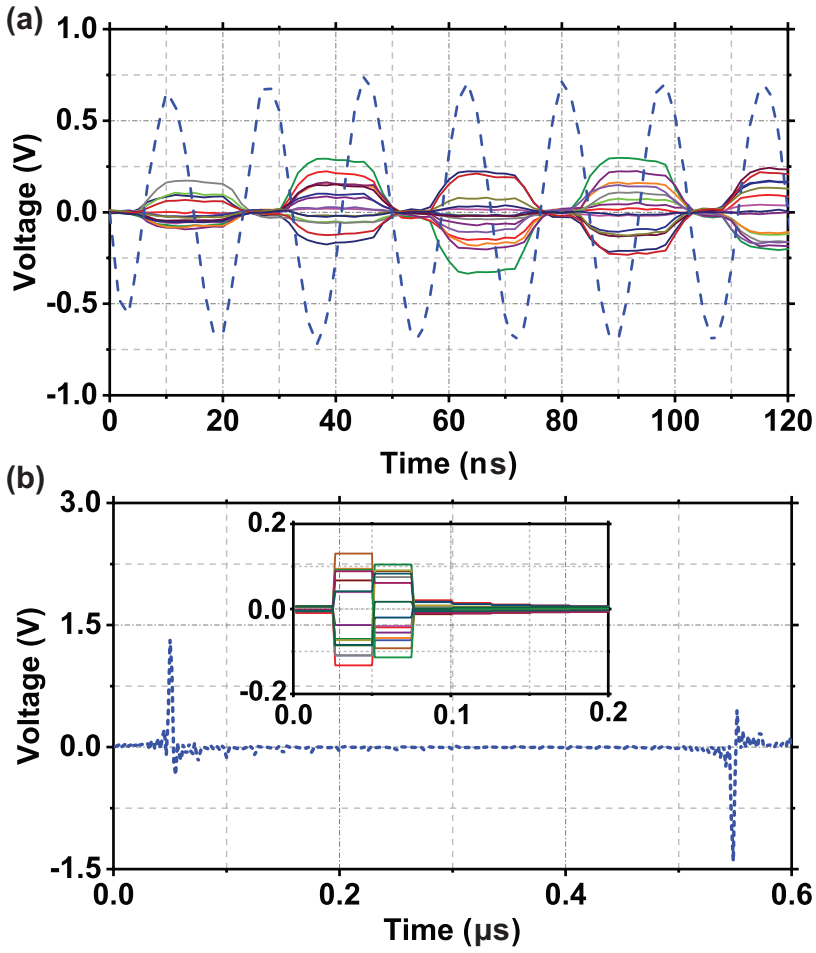

Figure 5.10. (a) Reconstructed waveform for a 58 MHz sinusoidal input (dashed blue line) along with oscilloscope measurements of the 15 ADC inputs. (b) Reconstructed waveform for the case in which the input is excited using a pulse waveform. The inset contains the fifteen digitized baseband outputs over the time period where the pulse was active.Reproduced from [38]©IEEE 2018.

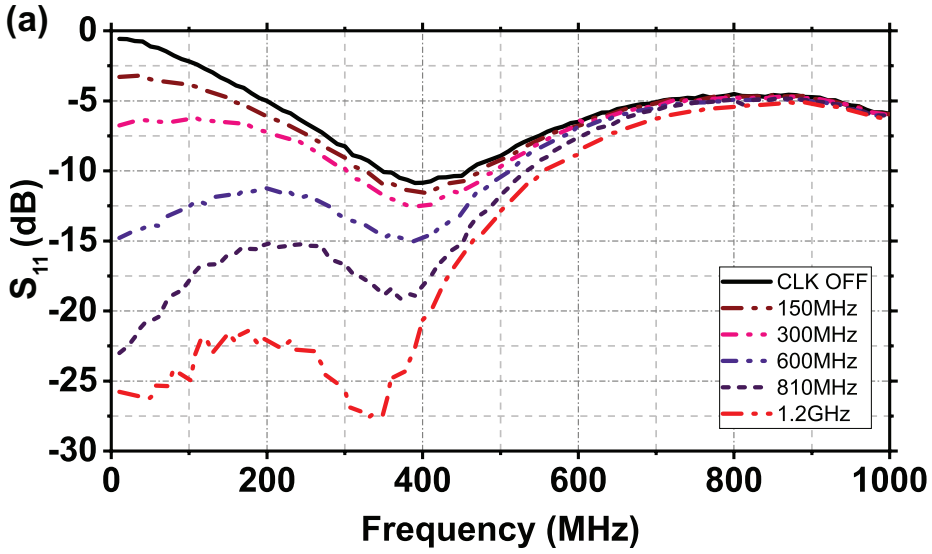

Figure 5.11. Differential mode input reflection coefficient. The measurement reference plane is at the PCB input. Reproduced from [38]©IEEE 2018.

MHz, respectively. As expected, the mean value of the peak-peak amplitude of the baseband samples was approximately 10 dB smaller than that of the reconstructed output. The circuit was also tested with an impulse excitation with a 300 $mV_{p\text{-}p}$ amplitude and 10 ns pulse width. The reconstructed waveform is plotted along with the digital domain baseband samples in Fig. 5.10(b). The peak-peak swings of the reconstructed signal at the reference plane of the chip output were approximately 2.8V, whereas those of the baseband samples were all well below 0.4V. In this case, the suppression was greater than $1/\sqrt{15}$ since the pulse occupied only a fraction of the sequence period (TS = 25 ns).

Next, the differential input reflection coefficient of the chip was characterized using a vector network analyzer (VNA). The results are shown in Fig. 5.11. The measurement reference plane is at the PCB input and as predicted by the simulation results in Fig. 5.4(b), the parasitic effects of the PCB result in more broadband input match. Additional series inductance and shunt capacitance elements can be used to tune the high frequency response if better input match at these frequencies is required.

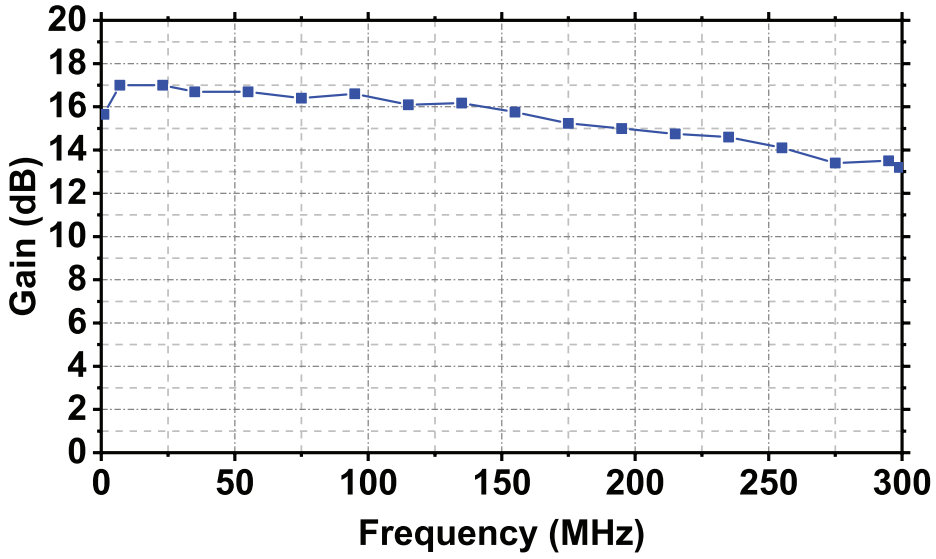

Figure 5.12. Conversion gain of the receiver over frequency. Reproduced from [38]©IEEE 2018.

Measurement results of the receiver gain versus frequency are shown in Fig. 5.12. The overall gain of the receiver system is approximately 17 dB, which is about 1 dB lower than the value predicted by simulations of the baseband amplifiers presented in Chapter 4. This discrepancy may be due to the lower gain of individual amplifiers or losses in the sampling circuit. To evaluate the noise performance of the receiver, the input was terminated in 100 Ω and the noise floor after signal reconstruction was evaluated (see Fig. 5.13). The average noise floor of the reconstructed signal referred to the input of the system is approximately at -154 dBm/$\sqrt{\text{Hz}}$. This value corresponds to a noise figure of ≈20 dB. As predicted by (2.27), there is rise in the noise floor of the receiver for low frequencies.

The ADC cards employed in this work do not include anti-aliasing filters appropriate for digitizing at 40 MS/s. The bandwidth of the baseband amplification chain was significantly greater than the requisite 20 MHz. As such, a degradation factor of 5.2 dB was obtained by taking the ratio, as measured using a spectrum analyzer, of the total integrated noise power at the output of each baseband channel to that in

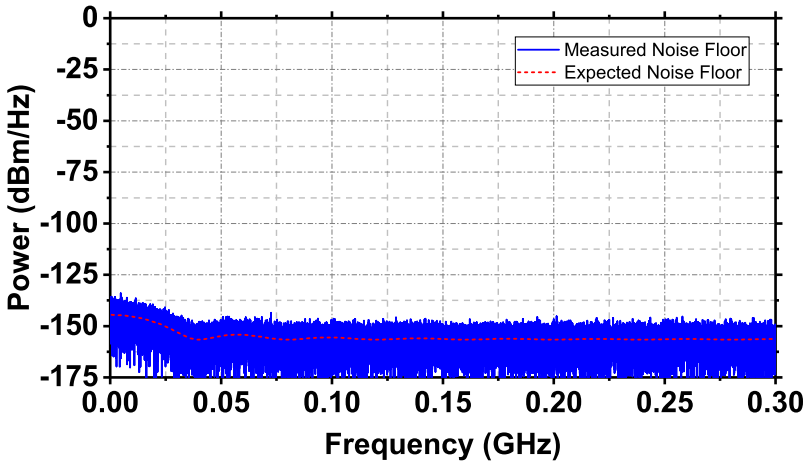

Figure 5.13. Input referred noise floor of the receiver versus the expected noise floor based on simulation results and aliasing factor at the ADC input.

a 20MHz bandwidth. Moreover, the effect was verified by placing a 50 MHz coaxial lowpass filter before one of the digitizer channels and observing that the integrated noise floor dropped by approximately 2 dB in comparison to the case in which no filter was used. By considering the aliasing effect and using the simulation results, the predicted noise figure of the receiver is about 18.7 dB. Since the amplifier is the dominant source of noise, the overall noise performance could be improved through optimization of this block. In addition, migrating the design to a shorter gate-length process, would enable the reduction of input signal loss and can further improve the noise performance.

The linearity of the receiver was characterized using a two-tone excitation with a tone spacing of 1 MHz and a center frequency which was swept from 11 to 300 MHz. The results appear in Fig. 5.14(a). The system IIP3 was found to be better than 5.7 dBm over this entire frequency range. The average IIP3 value of 7 dBm is slightly higher than the 5.7 dBm predicted by simulation. This discrepancy is believed to be related to the measured gain being 1 dB lower than that predicted by simulation.

To further validate the effectiveness of the proposed technique, the measured output third order intercept point (OIP3) of baseband amplifiers was compared to that

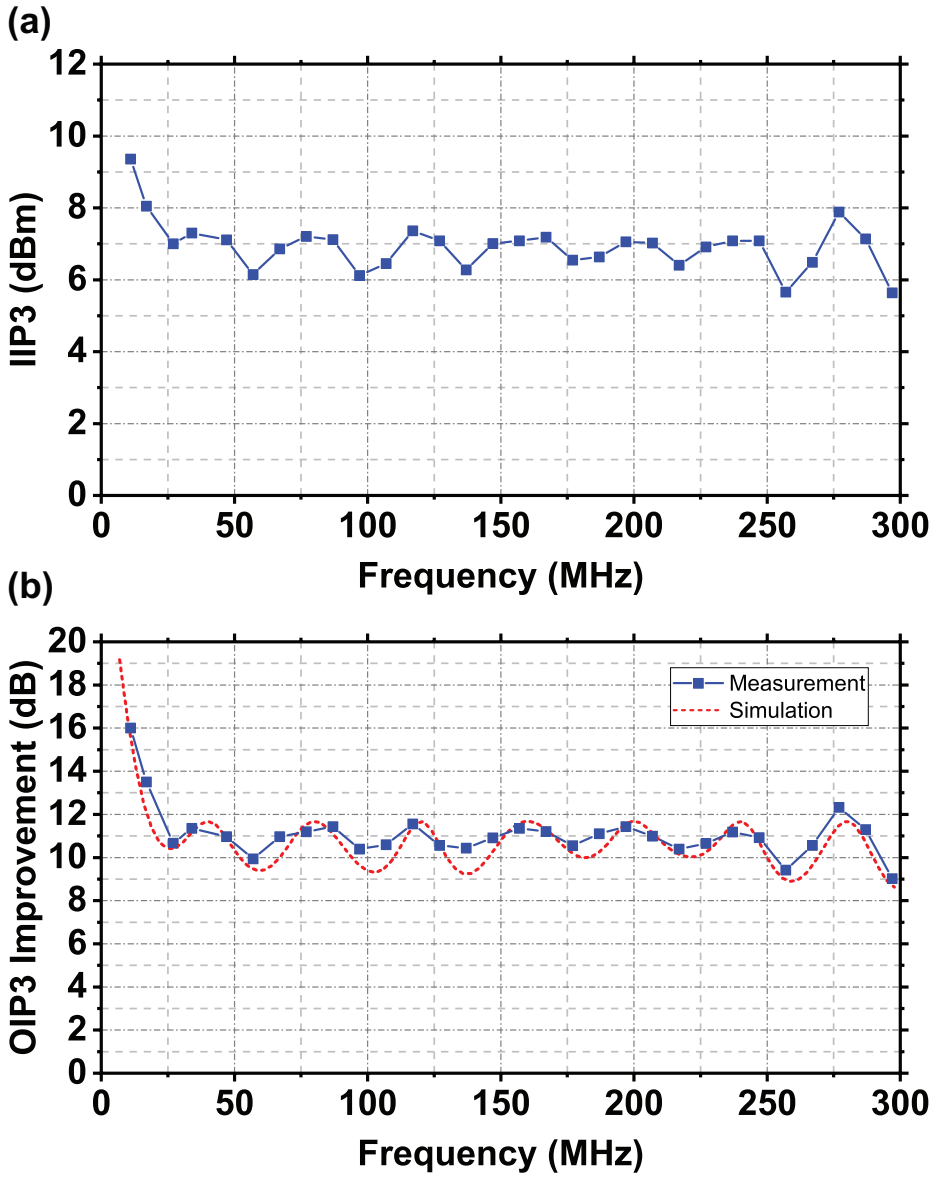

Figure 5.14. Measurement results of the intermodulation performance. (a) Measured system IIP3 as a function of RF frequency. (b) Measured OIP3 improvement of the reconstructed signal to that of the average measured OIP3 at the output of each channel along with the value predicted by simulation. A 1 MHz tone spacing was employed for these measurements.Reproduced from [38]©IEEE 2018.

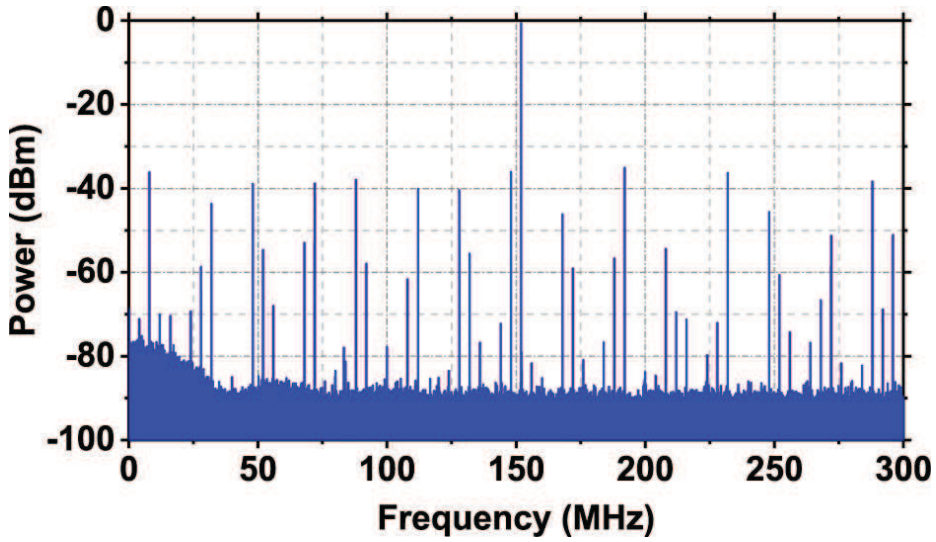

Figure 5.15. Spectrum of the reconstructed waveform for a 152 MHz CW tone. All spurious tones above -70 dBm were verified to be at frequencies predicted by analysis in Chapter 3.

of the complete system and, as expected, the OIP3 of each channel was consistently greater than 9 dB or more lower than that of the full system. Moreover, referring to Fig. 5.14(b), the measured frequency dependence of the OIP3 improvement closely mirrors that predicted by the numerical simulations described in Chapter 2 over the entire frequency range. The second-order distortion performance of the system was also characterized and it was found that the IIP2 was approximately 35.4 dBm. It is believed that this value is limited by the common-mode rejection of the adapter board.

The SFDR of the system was evaluated under CW excitation across the full range of RF frequencies. Fig. 5.15 shows an example for the spectrum of the reconstructed signal for a 152 MHz CW tone. It was found that, without any calibration, the system was able to provide an SFDR of better than 32 dB for all frequencies tested. Moreover, all significant spurious tones were at frequencies consistent with the generation mechanisms described in Chapter 3. As such, calibration techniques explained in the Chapter 6 can be employed to further enhance the SFDR performance.

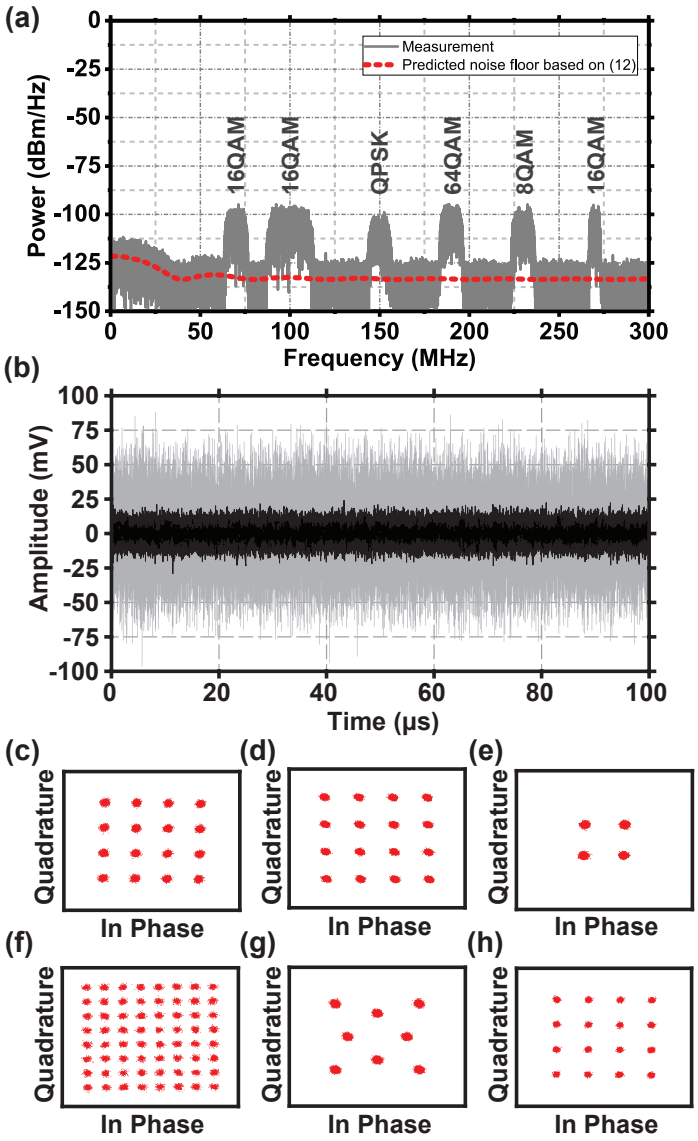

Figure 5.16. Example of wideband operation of the system. (a) Reconstructed spectrum showing the six message signals. (b) Time domain waveforms at the output of each channel (black traces) as well as after reconstruction (grey trace). Constellation diagrams for each of the demodulated data signals: (c) 10 Ms/s 16-QAM signal centered at 70 MHz (EVM ≈6%), (d) 20 MS/s 16-QAM signal centered at 100 MHz (EVM≈ 5%), (e) 10 MS/s QPSK signal centered at 150 MHz (EVM≈ 8%), (f) 10 MS/s 64-QAM signal centered at 190MHz (EVM≈ 6%), (g) 10 MS/s 8-QAM signal centered at 230 MHz (EVM≈ 6%), and (h) 5 MS/s 16-QAM signal centered at 270 MHz (EVM≈ 5%). Each EVM value was calculated with normalization to average symbol power (as opposed to peak symbol power).Reproduced from [38]©IEEE 2018.

The wideband operation of the system was next characterized. The chip was excited with a spectrum containing six different message signals. The reconstructed output spectrum appears in Fig. 5.16(a). Each of the six message signals are clearly visible in the reconstructed spectrum. The time domain response to the broadband excitation appears in Fig. 5.16(b), with the system output shown in grey and each of the fifteen baseband outputs plotted in black. On average, the RMS amplitude of each baseband signal was found to be a factor of 11.7 dB smaller than that of the reconstructed output signal, which is consistent with expectation. The peak to average power ratio (PAPR) for the reconstructed signal and each of the baseband outputs was also computed. In each case, it was found that the PAPR of the baseband signals was smaller than that of the reconstructed waveform, with an average difference of 1.3 dB. Finally, each of the six message signals were demodulated and the constellations appear in Fig. 5.16(c)-(h). The error-vector magnitudes (EVMs), normalized to the average symbol power, were computed and found to range from 5-8 %. These values are in the range expected based upon the power levels and the system noise figure.

The blocker tolerance of the circuit was also characterized. In a first experiment, the input was driven with a -50 dBm 10 MSPS 16-QAM signal centered at 130 MHz and a CW blocker was introduced at 139.5 MHz. The EVM of the reconstructed signal as a function of blocker power appears in Fig. 5.17(a). A representative spectrum is also shown in the inset of Fig. 5.17. The constellation diagram for demodulated message signals over different blocker powers are shown in Fig. 5.17(b). Remarkably, the EVM was found to be insensitive to the blocker signal for blocker powers as high as -10 dBm. It was not until the input blocker level exceeded -5 dBm that a significant degradation to EVM was observed due to saturation of the ADCs. This significant as this high power level is similar to out-of-band blocker tolerance requirements for some communication standards such as GSM which requires 0 dBm blocker tolerance at 20 MHz offset [16].

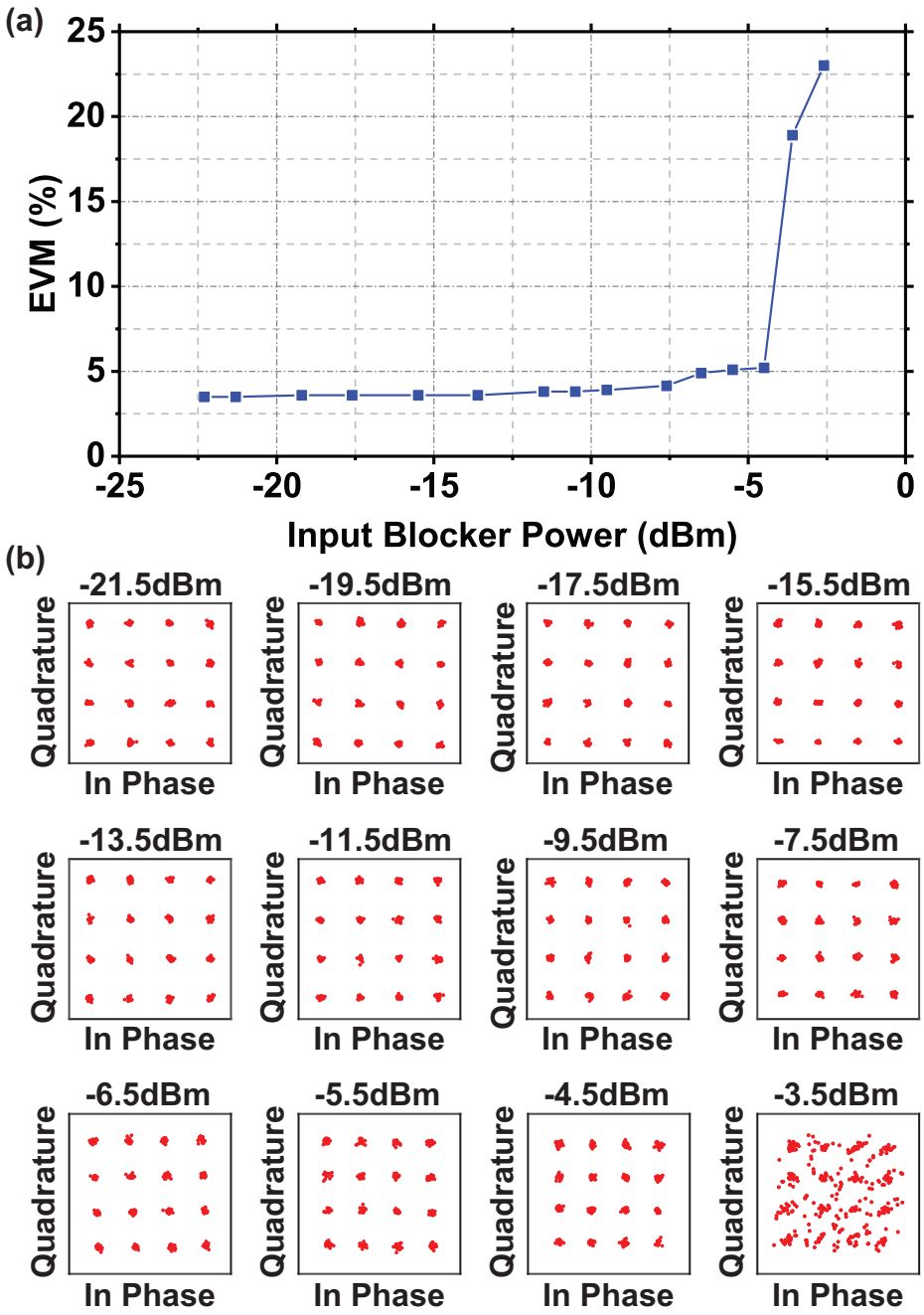

Figure 5.17. (a) In-band blocker tolerance test for a single broadband message signal. EVM, normalized to average symbol power for a -50 dBm 10 MS/s 16-QAM signal with f_c at 130 MHz as a function of the power of a blocker at $f_b = 139$ MHz . The inset figure shows the signal scenario and (b) constellation diagrams for different blocker power levels. Reproduced from [38]©IEEE 2018.

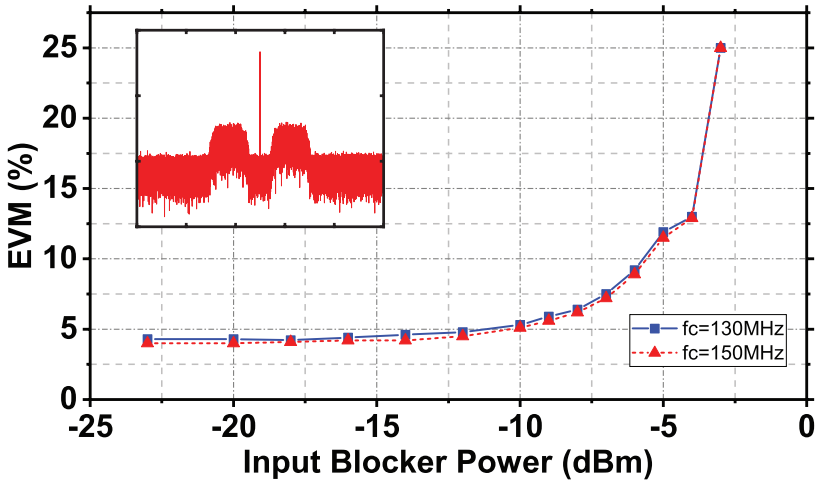

Figure 5.18. In-band blocker tolerance test for two broadband message signals. EVM, normalized to average symbol power for two 10 MS/s 16-QAM signals at f_{c1} = 130MHz and f_{c2} = 150MHz as a function of the power of a blocker at f_b = 139 MHz. The power of each of the 16-QAM signals was -51 dBm. The inset figure shows the signal scenario. Reproduced from [38]©IEEE 2018.

In a second experiment, a blocker signal was placed between a pair of -50 dBm 10 MSPS 16-QAM signals having carrier frequencies of 130 and 150 MHz, respectively (see Fig. 5.18). Each measured EVM appears as a function of the blocker power in Fig. 5.18. In this case, a gradual degradation of EVM was observed for blocker powers greater than approximately -12 dBm before a sharp degradation was observed as the ADCs saturated. The initial degradation is believed to be attributed to interference between the two message signals due to third-order mixing between the message signals and the CW blocker.

In a third experiment, the tolerance of the circuit to wideband blockers was evaluated by exciting the circuit with a -50 dBm 2.5 MS/s 16-QAM message signal centered at 210 MHz and a 2.5 MS/s 16-QAM blocker signal centered at 226 MHz. The corresponding baseband frequencies for the message and blocker signals are 8.75 to 11.25 MHz and 12.75 to 15.25 MHz, respectively. As such, IM3 products due to the blocker signal which are generated in the baseband amplifiers will end up falling into

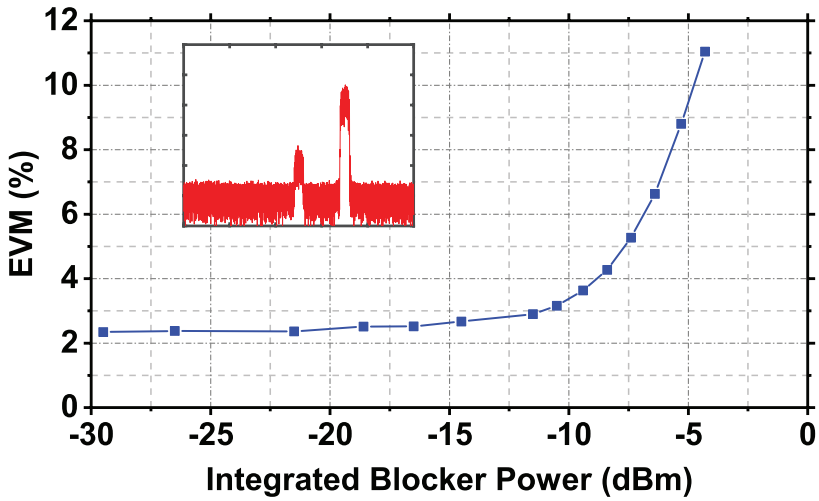

Figure 5.19. Broadband blocker tolerance test. The EVM, normalized to average symbol power, is plotted for a 2.5 MS/s 16-QAM signal with f_c = 210MHz as a function of the integrated power of a 2.5 MS/s 16-QAM blocker with center frequency, f_b at 226 MHz. The frequencies were chosen such that the baseband IM3 products of the blocker land in the message band. The integrated power of the message signal is -50 dBm. The inset figure shows the signal scenario. Reproduced from [38]©IEEE 2018.

the message band. The results are plotted in Fig. 5.19. The EVM was found to be better than 10% for integrated blocker powers as high as -5 dBm.

The total power consumption of the integrated circuit was found to be 454 mW. Of this, 60 mW (13%) was dissipated in the clocking portion of the passive discrete-time signal processing block and the remaining 87% was dissipated in the baseband amplifiers. From simulation, it is believed that 63% of the total power dissipation (288 mW) was in the output drivers, which were designed to drive off-chip ADCs at full-scale without introducing non-linearity. The remaining 24% of the aggregate power consumption (106 mW) is believed to be associated with the low-noise stage of the baseband amplifiers. In a future design, the overall power consumption could be greatly reduced, for instance, by integrating low-power digitizers [64–66] on the chip instead of the off-chip ADCs. As an example, the ADC reported in [64] has an input capacitance of 630 fF. Thus by integrating such ADC on-chip the power

Table 5.1. Comparison table

Reference	This Work	[69]	[24]	[14]	[70]
Technology Node (nm)	130	65	65	65	65
Input Frequency (GHz)	0.04–0.3	0.1–1	0–0.9	0.5–3	0.4–0.9
RF Bandwidth (MHz)	260	2.5–40	5	10.5-63.5	12
In-Band IIP3 (dBm)	5.8	1	14.3	-12	3.5
NF (dB)	20	6.5	31	6.8-13.2	4(DSB)
Gain (dB)	16	18.9	NR	35	34.4
P_{DC} Power (mW)	470	67–74	176	250-600	60
$P_{\mathrm{DC}}/B_{\mathrm{RF}}$ (mW/MHz)	1.75	1.84	35.2	3.8–9.5	5
Die Area (mm^2)	2	4	3.84	5.9	1

required in the output stage of the amplifier to drive the ADC at 80MHz would reduce to only 73.7 μW which is 64 times smaller than the power required to drive the 300 Ω load. This can potentially reduce the total power consumption of the chip significantly. In addition, the power consumption of ADCs tend to increase significantly with frequency scaling. As an example, in [67] a 14-bit 1 GS/s ADC is reported with a power consumption of 1.2 W. However, in [68] a 14-bit 60 MSps ADC is introduced which consumes only 67 mW. Hence, if fifteen of the ADCs reported in [68] are used in the proposed system to achieve a similar Nyquist bandwidth to that of [67] the total power consumption would be approximately 1 W. This shows that the proposed architecture can lead to lower total power consumption for ADCs compared to using a single wideband ADC.

The performance of the prototype circuit is compared to several state-of-the-art wideband receivers in Table 5.1. While the RF input frequency range is more limited, the proposed approach achieves the lowest ratio of dc power dissipation to instantaneous bandwidth. Since a small portion of the power is dissipated in the RF section, this value can be further enhanced by overcoming the frequency of operation limitation. The noise performance of the system is one aspect that needs to be improved in the future generations of the system.

5.5 Summary

In this chapter the measurement results of the fabricated prototype integrated circuit along with the design and implementation of the required test setup were presented. It was discussed that a custom data collection system was required to enable signal reconstruction in digital domain. The time domain performance of the IC was evaluated first to ensure correct reconstruction of the RF signal at digital domain. Next, input reflection coefficient of the overall IC was verified to be better than 10 dB across the desired frequency band of DC to $f_{\mathrm{CLK}}/2$ and close to the expected value by simulation. Several tests were designed to evaluate linearity and blocker tolerance of the receiver. It was shown that the OIP3 enhancement of the overall system compared to that of each individual channel closely mirrored the expected value from Matlab simulations. This demonstrated the effectiveness of the proposed architecture. The noise performance of the system was characterized and the noise figure was calculated to be close to 20 dB. This higher than expected noise figure was attributed to the high bandwidth of the ADC analog input which results in significant noise folding. Nevertheless, future generations of the system should develop techniques to further improve the noise performance.

The power consumption of the chip was reported along with attribution from different parts of the system. It was discussed that relatively high power consumption is mainly due to the driving stage of the baseband amplifiers requiring to drive off-chip ADCs. Hence, integration of ADCs on the chip was proposed to significantly reduce power consumption. The overall performance of the system was compared to other state-of-the-art wideband receiver systems. It was highlighted that despite higher total power consumption, this work presents the lowest ratio of power consumption to instantaneous bandwidth.

CHAPTER 6

CALIBRATION OF MISMATCH EFFECTS

Systematic errors due to hardware implementation result in imperfect reconstruction of the input signal. This limits the system SFDR performance. As the measurement results in the previous chapter showed, despite all the efforts to implement a symmetric layout, the measured SFDR of the fabricated prototype IC is still limited. This demonstrates the need for calibration techniques that address these non-idealities if better performance is desired.

In Chapter 3, different sources of error which contribute to imperfect signal reconstruction were discussed. These errors include DC offsets, gain mismatches, and timing delay mismatches. The effect of these errors were discussed and the sensitivity of system SFDR performance to each of them was quantified. Calibration techniques employed for addressing these errors can be divided into two categories, first, techniques that are implemented on-chip and aim to tweak specific properties of the system to compensate for any systematic error. These approaches require additional circuit blocks to be integrated within the system to enable calibration. The second approach includes techniques that are integrated with the reconstruction procedure in digital domain, and aim to compensate for different sources of error by operating on receiver outputs. These approaches may also require additional blocks to generate the required test signals that are used as the basis for calibration.

In this chapter, calibration techniques are introduced to address each of the three systematic errors. It will be discussed that DC offset and gain mismatches can be

compensated during the reconstruction procedure, while calibration of timing mismatches requires additional circuit blocks that are implemented within the receiver.

6.1 Calibration of DC Offset and Gain Mismatch Error

The effect of DC offset and gain mismatches can be added to the matrix operation introduced in Chapter 2 as

$$\mathbf{y} = \mathbf{P}_{\mathrm{m}}\mathbf{x} + \mathbf{d}, \tag{6.1}$$

where $\mathbf{P}_{\mathrm{m}}$ is the model for the implemented matrix including the mismatch effects and $\mathbf{d}$ is the vector of DC offsets at the output of different channels. The correct knowledge of $\mathbf{P}_{\mathrm{m}}$ and $\mathbf{d}$ enables the reconstruction procedure to compensate for their effects and enhance the overall performance.

6.1.1 Calibration of DC Offset Mismatches

The majority of DC offset errors are expected to stem from mismatches in DC operating point of active circuits in the system. However, other effects such as clock feed through can also lead to small DC offsets which can degrade the performance [71]. All of these effects can be modeled as a constant vector $\mathbf{d}$ in (6.1). From (6.1), it is evident that for a zero input the measured $\mathbf{y}$ values capture the DC offsets. Thus these offsets can be compensated by extracting the effective $\mathbf{d}$ in (6.1). The implementation of such calibration technique will be further discussed in Section 6.2.

If dynamic calibration of DC offset errors are required to further enhance the system performance, other DC offset calibration techniques such as the one proposed in [72] can be implemented. In this work, a digitally assisted closed loop system is employed to actively compensate for DC offsets at the mixer output. DC offset is detected at the output of a current driven passive mixer. Then a compensation current is injected by a digital-to-analog (DAC) converter to cancel this offset. The injected

current is adjusted through a successive approximation register (SAR) approach to balance the DC value at the output of the mixer.

To prevent the spurious tones generated due to the DC offsets from limiting the overall performance, the power level of these tones should be below the noise floor of the system. The noise floor of a receiver at the output of the baseband amplifier can be found as

$$S_{\mathrm{N,out}}(\mathrm{dBm/Hz}) = -174(\mathrm{dBm/Hz}) + NF(\mathrm{dB}) + G(\mathrm{dB}), \tag{6.2}$$

Where G and NF are the gain and noise figure of the receiver respectively. Hence, the DC offset values should be below this noise level. Employing the results of (3.3), the average power of the spurious tones due to DC offsets in the frequency range of $f_{\mathrm{CLK}}/N - f_{\mathrm{CLK}}/2$ can be found from

$$P_{spur,DC} = \frac{N}{N+1}\sigma_{\mathrm{DC}}^2. \tag{6.3}$$

where σ_{DC} is the standard deviation of the DC offset error in each channel. Employing the result of (6.2) and (6.3), the standard deviation of the DC offset errors should be

$$\sigma_{\mathrm{DC}}^2 < \frac{N+1}{N} 10^{(S_{\mathrm{N,out}}-30)/10}. \tag{6.4}$$

As an example, in the system described in Chapter 4, for the spurious tones to be below the receiver noise figure the standard deviation of the DC offset errors should be less than 0.7 μV.

6.1.2 Calibration of Gain Mismatches

Gain mismatches result in spurious tones that are input dependent and can limit the SFDR performance. To reduce these effects, device mismatches should be included

in the matrix model ($\mathbf{P}_{\mathrm{m}}$). This matrix model should be extracted for each fabricated IC and then its inverse should be used for signal reconstruction. Using (6.1) and employing a set of known input vectors $\mathbf{x}$, the $\mathbf{P}_{\mathrm{m}}$ can be found from

$$\mathbf{P}_{\mathrm{m}} = (\mathbf{Y}_{\mathrm{c}} - \mathbf{d})\mathbf{X}_{\mathrm{c}}^{-1}, \tag{6.5}$$

where $\mathbf{X}_{\mathrm{c}}$ is a matrix of a set of known input vectors and $\mathbf{Y}_{\mathrm{c}}$ is the matrix of corresponding measured samples. For the $\mathbf{X}_{\mathrm{c}}$ to be invertable it should be full rank. Therefore, N different sets of known inputs are required to fully characterize $\mathbf{P}_{\mathrm{m}}$.

To minimize the error in the extraction of $\mathbf{P}_{\mathrm{m}}$, the exact knowledge of input vector is essential. Hence, on-chip test signal generators should be employed to ensure proper timing of the input signals. It should be noted that this technique would also calibrate the effect of any weighting mismatches within the individual channels by weighting each element of the matrix separately.

The precision of the extracted matrix from (6.5) depends on the invertability of the $\mathbf{X}_{\mathrm{c}}$. As a result, the set of input vectors used to characterize the matrix should be chosen such that the condition number of the resulting matrix ($\mathbf{X}_{\mathrm{c}}$) is as low as possible. This can be achieved by ensuring that input vectors are as close to orthogonal as possible. Signals such as a set of sine waves that are orthogonal to one another can satisfy such a requirement. However, these types of signals are very sensitive to phase errors and require complicated phase locking circuits for each test signal. On the other hand, binary test sequences can be generated using the same reference clock as the receiver and are not as sensitive to phase errors. Since the PRBS achieves the maximum orthogonality for a periodic binary sequence, it is a good candidate to be used as the test sequence. By applying N shifted versions of a PRBS at the input and employing the resulting output samples the $\mathbf{P}_{\mathrm{m}}$ matrix can be extracted.

The inner product of a PRBS with itself results in N samples with equal values of 1. Hence, the use of the PRBS as the RF input would result in the channel with the same sequence to produce a value of 1 after averaging. However, since LO sequences in other channels are shifted versions of the input PRBS, the resulting output from those channels will be equal to -1/N. By rotating the phase of the input signal the single channel with the high amplitude will also change.

Using the results of the discussion in Chapter 3, the required matching between channels for a given SFDR specification can be found. As shown in Section 3.2, the expected value of the SFDR due to gain mismatches can be written as

$$\mathbb{E}\left\{\mathrm{SFDR_G}\right\} \approx \frac{N+1}{(\Phi^{-1}\{0.52641^{(1/2N)}\})^2\sigma_{\mathrm{G}}^2}. \tag{6.6}$$

For example, for a fifteen-channel system to achieve a SFDR value better than 60 dB the required matching between different channels can be found by

$$\sigma_{\mathrm{G}}.^2 = \frac{16}{(\Phi^{-1}\{0.52641^{(1/30)}\})^2 \times 10^3} = 4 \times 10^{-6}. \tag{6.7}$$

This is a tough specification for the system. Monte Carlo simulation results on the baseband amplifier implemented in Chapter 4 show that a standard deviation of 2% can stem from mismatches in the implemented device. Which would limit the SFDR performance of the system to approximately 52 dB. Thus calibration procedures may be required to achieve SFDR values higher than this value.

6.1.3 Calibration of Timing Mismatches

Timing delay mismatches between different channels can significantly limit the SFDR performance. Since these delays corrupt the phase relationship between the baseband samples they can not be compensated during the reconstruction procedure. As such, on-chip delay compensation blocks are required to cancel out such mismatches.

Based on the analysis presented in Chapter 3, these errors result in a frequency dependent SFDR limitation, with the effect worsening at higher frequencies. Therefore, to ensure these spurious tones are within the specification of the system, the highest input frequency should be considered as the worst case scenario. As explained in Section 3.3, the expected value of the SFDR due to timing skews can be found by

$$\mathbb{E}\left\{\mathrm{SFDR}_{\mathrm{SKEW}}\right\} \approx \frac{N+1}{4\pi^2(\Phi^{-1}\{0.52641^{(1/2N)}\})^2 f_{\mathrm{in}}^2 \sigma_\tau^2}. \tag{6.8}$$

As an example, for a fifteen-channel receiver system to achieve a SFDR value better than 60 dB the timing skew standard deviation normalized to the clock period should be less than 7×10^{-3}. Thus, for a system with a sampling frequency of 1 GHz, the standard deviation of delays among the channels should be less than 0.7 ps. On possible calibration procedure to address these issues is the implementation of programmable delay elements with resolutions close to the required maximum timing offset in clock path for each channel. By optimizing these delay elements the timing skew among the channels can be reduced to the desired value.

6.2 DC offset and Matrix Calibration for the CMOS Implementation

To enable matrix calibration for the CMOS implementation proposed in Chapter 4, additional test circuitry was added at the RF input of the system (see Fig. Fig. 6.1). This circuit block produces fifteen different phases of the PRBS based on four control inputs provided from off-chip. This block is connected to the RF input for the calibration phase and disconnected with high isolation during the normal operation of the system.

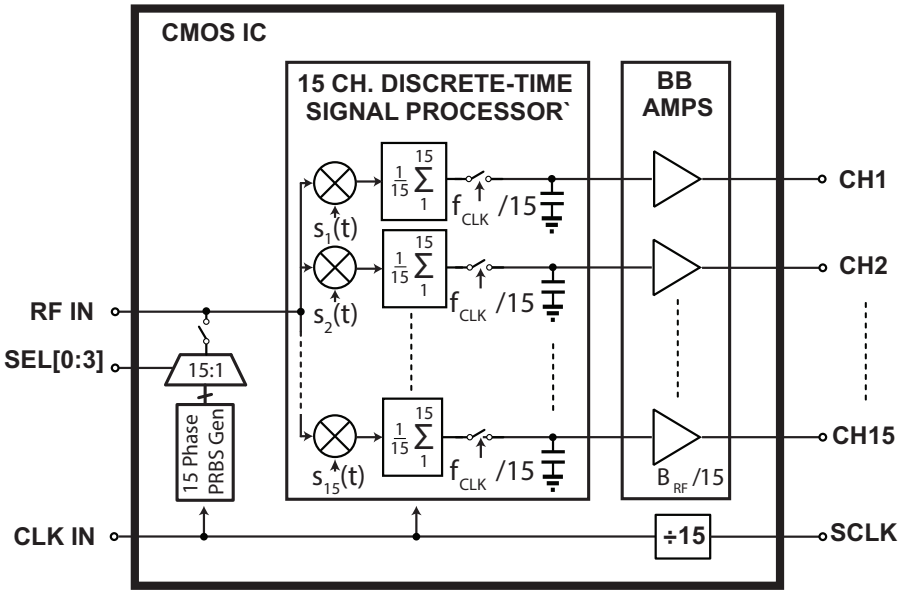

Figure 6.1. Schematic diagram of the CMOS IC including the additional PRBS generator block at the RF input for matrix calibration.

6.2.1 Circuit Implementation of the Test Sequence Generator

As shown in Fig. 6.2(a), a circular fifteen-bit shift register, similar to those used in each channel, was utilized to generate the PRBS. The output of each shift register is tapped to produce one phase of the PRBS. A 15 to 1 multiplexer was used to select between different taps to generate the desired test sequence (see Fig. 6.2(b)). This was implemented using a simple switch approach where the fifteen enable signals are generated from the four digital control bits (SEL). To minimize the loading on the shift register, two buffers were employed to drive the output load.

The PRBS input signals are digital signals and have large amplitudes. As a result, to avoid saturation of the receiver system, their signal levels were reduced by a resistive voltage divider, as shown in Fig. 6.2. By terminating the RF inputs to the chip in 100Ω, a series resistance of 1.75 kΩ attenuates the signal by a factor of 70. This value was chosen so that the maximum peak-peak amplitude of the signal at the input of the baseband amplifier is ≈34 mV. This value is approximately nine times less than the 1 dB compression point of the amplifier and results in about 0.15% gain

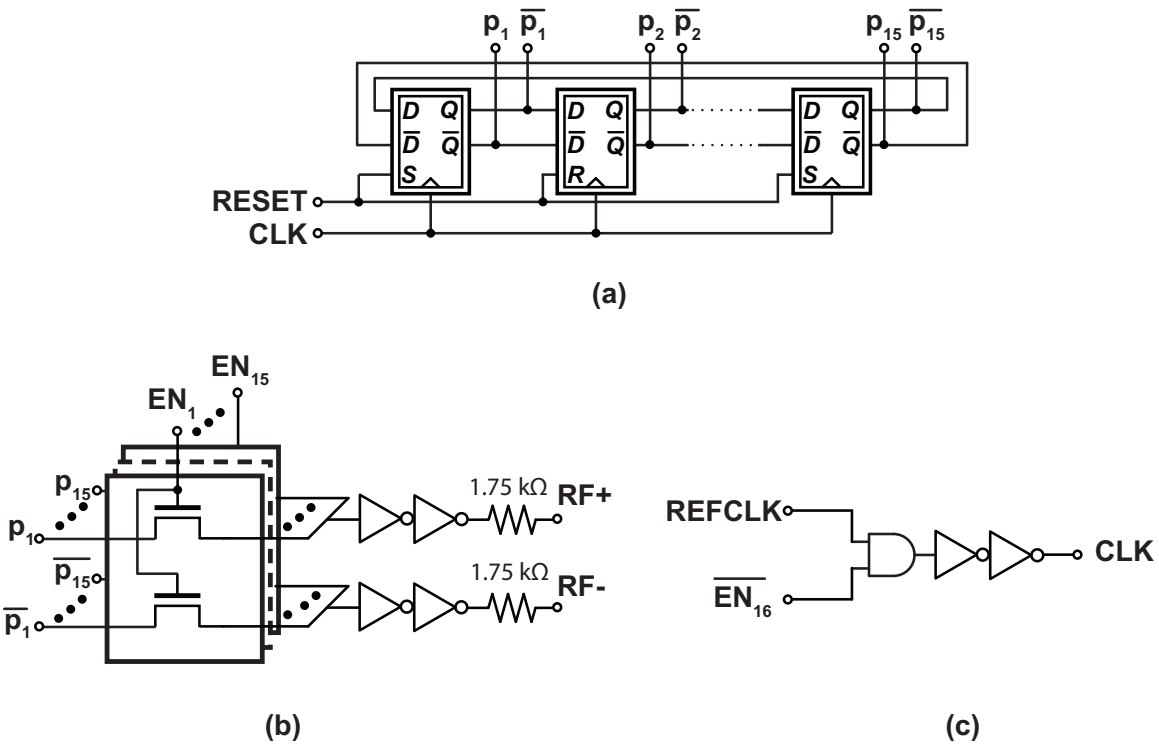

Figure 6.2. Schematic diagram of (a) 15 phase PRBS generator , (b) the 15 to 1 multiplexer, and (c) clock gating for disabling the PRBS generator during normal operation of the system.

reduction due to the compression. This will ensure that any mismatch effects due to the compression would be reduced to below 50 dB.

To minimize the effect of the test circuitry during the normal operation of the system, the clock to the shift register is gated using an enable bit as shown in Fig. 6.2(c). This enable is also generated by the four control bits provided from off-chip. This bit is high when all four control bits are equal to zero. The gating of the clock ensures that no unwanted digital signal due to the PRBS test generator can couple to the RF input during normal operation.

Fig. 6.3 shows the Cadence transient simulation results of channel outputs for a PRBS test sequence selected as an input. In this scenario the input PRBS phase is selected such that it is in-phase with channel 1 while out of phase with all other

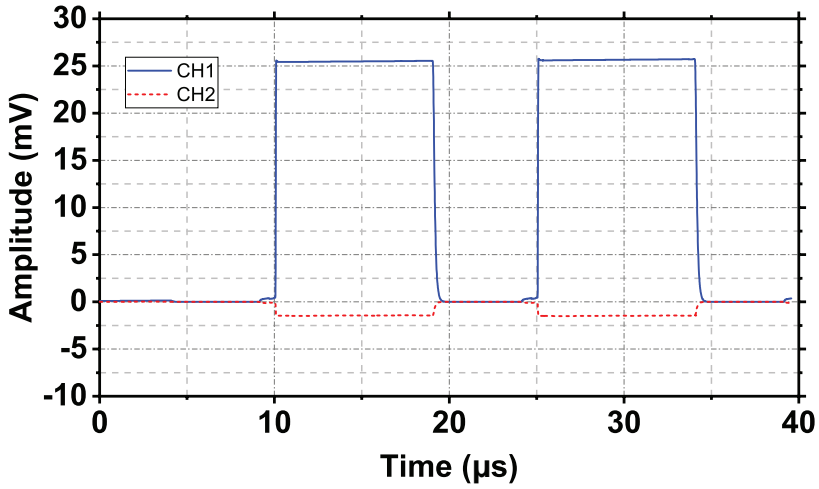

Figure 6.3. Cadence transient simulation results of the signal at the baseband amplifier input for two sample channels with a PRBS sequence connected to the RF input. The input PRBS test signal phase is chosen to be in-phase with channel 1.

channels. As expected, the output of channel 1 is approximately -15 times that of channel 2.

The test sequence generator was implemented at the top level of the CMOS chip described in Chapter 4. The reference clock to this block was provided through the same H-tree structure used to deliver the clock to different channels as explained in Chapter 5. This is done to synchronize the sequence generated by this block and the ones used as LO signals in individual channels. In addition, the output of the block is connected to the RF input of the chip at the input pads to ensure matched propagation delay to different channels. To improve the symmetry of the layout and reduce the area, each flip-flop in the test sequence generator was implemented along with the required multiplexer enables.

6.3 Calibration Measurements

Prior to the description of the calibration procedure, it is worth noting that the implemented chip contains two independent banks of capacitors that are each used to perform the sampling and averaging operations. As these banks have independent

errors, a model reflecting this is required. Taking this into account, we can write the operation over two frames (30 RF samples) as

$$[y]_{30\times1} = \begin{bmatrix} [\mathbf{P}_{\mathrm{m},1}]_{15\times15} & [0]_{15\times15} \\ [0]_{15\times15} & [\mathbf{P}_{\mathrm{m},2}]_{15\times15} \end{bmatrix}_{30\times30} [\mathbf{x}]_{30\times1} + \begin{bmatrix} [\mathbf{d}_1]_{15\times1} \\ [\mathbf{d}_2]_{15\times1} \end{bmatrix}_{30\times1} . \tag{6.9}$$

where $\mathbf{P}_{\mathrm{m},1}$ and $\mathbf{P}_{\mathrm{m},2}$ are the corresponding matrices for the two capacitor banks.

The calibration procedure was carried out on two different ICs using the on-chip test sequence generator and terminating the RF input of the chip differentially in 100Ω. First, it was observed that the PRBS test sequence generator can only produce accurate sequences at low clock rates bellow 150 MHz. This is believed to be mainly due to the slew rate limitation of the circuit. Hence, the calibration procedure was carried out at a clock frequency of 75 MHz. Despite the lowered frequency of operation, the calibration should to the first order provide a closer approximation to the implemented matrix compared to the ideal case. This low frequency of operation allowed for the employment of the measurement setup with two LM9011-14 DC coupled ADC boards as explained in Chapter 5. This setup enables DC offset measurements and therefore, it is more suited for this calibration procedure. Fig. 6.4 shows a photograph of the measurement setup.

To perform the calibration, first, DC offset vectors were extracted by terminating the RF inputs, and then taking the average of every other sample. Next, all different phases of the PRBS were enabled and for each case a long set of data was collected and the DC offset values were subtracted from each corresponding sample. The value for each baseband output was found by taking the average over a long set of data. Fig. 6.5 shows an example output of different channels for a single PRBS phase input. As expected, the average output of the channel which employs the in-phase PRBS with the input test sequence is -15 times that of all other channels. Fig. 6.6(a) and

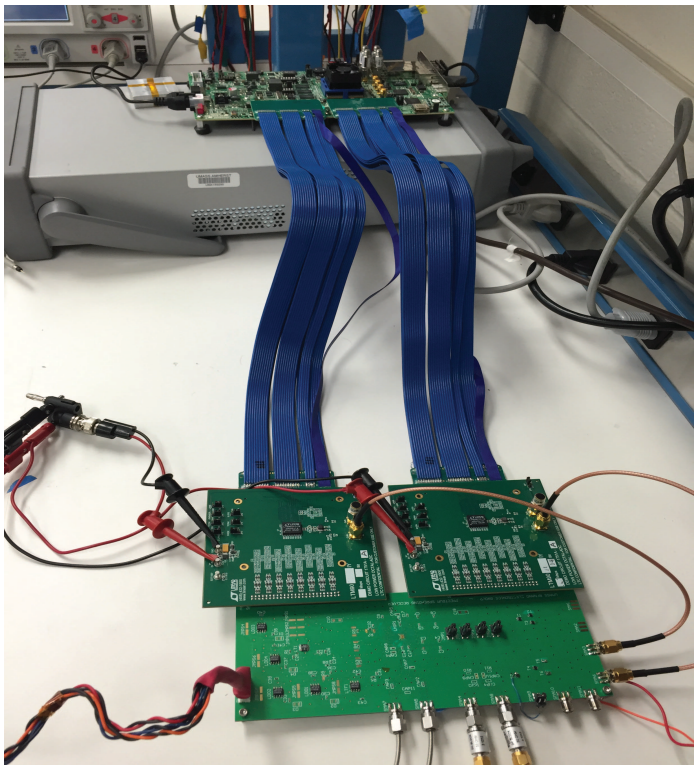

Figure 6.4. Measurement setup used for calibration measurements.

Fig. 6.6(b) show the average output of all channels for different phases of PRBS at the input, for capacitor banks 1 and 2 respectively.

These measurement results were employed to extract $\mathbf{P}_{m,1}$ and $\mathbf{P}_{m,2}$ matrices for the two ICs under test. Fig. 6.7 shows the histogram of the difference in matrix elements between the ideal matrix ($\mathbf{P}$) and the two extracted matrices ($\mathbf{P}_{m,1}$ and $\mathbf{P}_{m,2}$) for each IC. For IC # 1, the individual elements of the extracted matrices differ from those of the ideal matrix by as much as 20%, which highlights the importance of calibration for this integrated circuit. The two matrices for capacitor banks also differ from one another by as much as 20%, further highlighting the importance of differentiating between the two banks. The extracted results for the IC # 2 suggests better matching is achieved between the elements of this IC compared to that of the IC # 1.

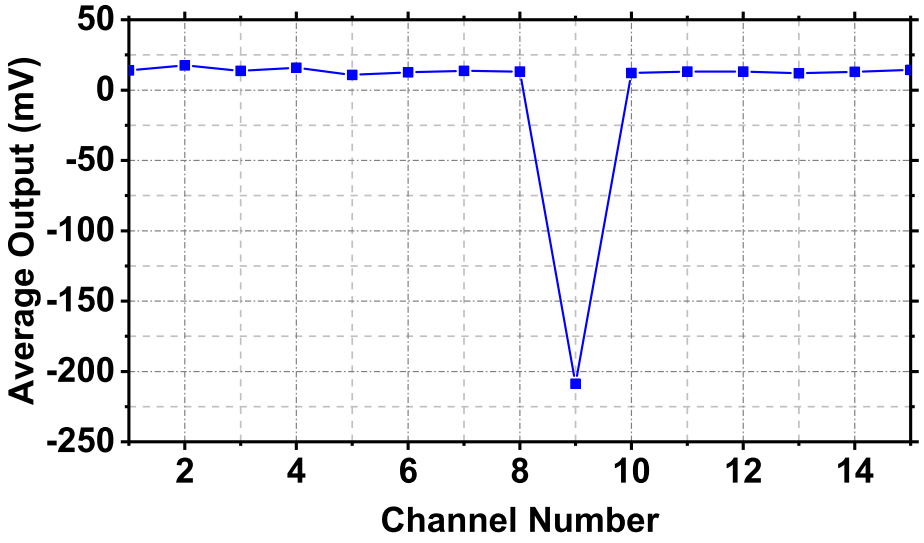

Figure 6.5. Measurement results of the average output value at different channels for a single phase of the PRBS test generator.

The resulting matrices were used to reconstruct some RF signals to evaluate the effectiveness of the calibration procedure. These test were done for both ICs at a clock rate of 600 MHz. Fig. 6.8(a) and (b) show the comparison between the spectrum of the reconstructed signal for a 117 MHz sine wave input signal, using the ideal matrix and the extracted matrices for IC # 1 respectively. As it can be seen, the SFDR is improved by more than 11 dB when the calibrated matrix is employed. Fig. 6.8(c) and (d) show the spectrum of the reconstructed signal for a 152 MHZ sine wave signal for chip # 2, using the ideal matrix and extracted matrices. The reconstruction results using the calibrated matrices in Fig. 6.8(d) show less than 1 dB improvement in the SFDR. These results show that the reconstruction using the ideal matrix achieved better than 34 dB SFDR for IC # 2 which is significantly better than the result achieved with the ideal matrix for the IC # 1. This is believed to be due to the better matching between circuit elements on this IC. In fact, it was observed that for three other assembled ICs that were tested, all SFDR values were better than 31 dB when the ideal matrix was employed. Hence, the IC # 1 was considered as

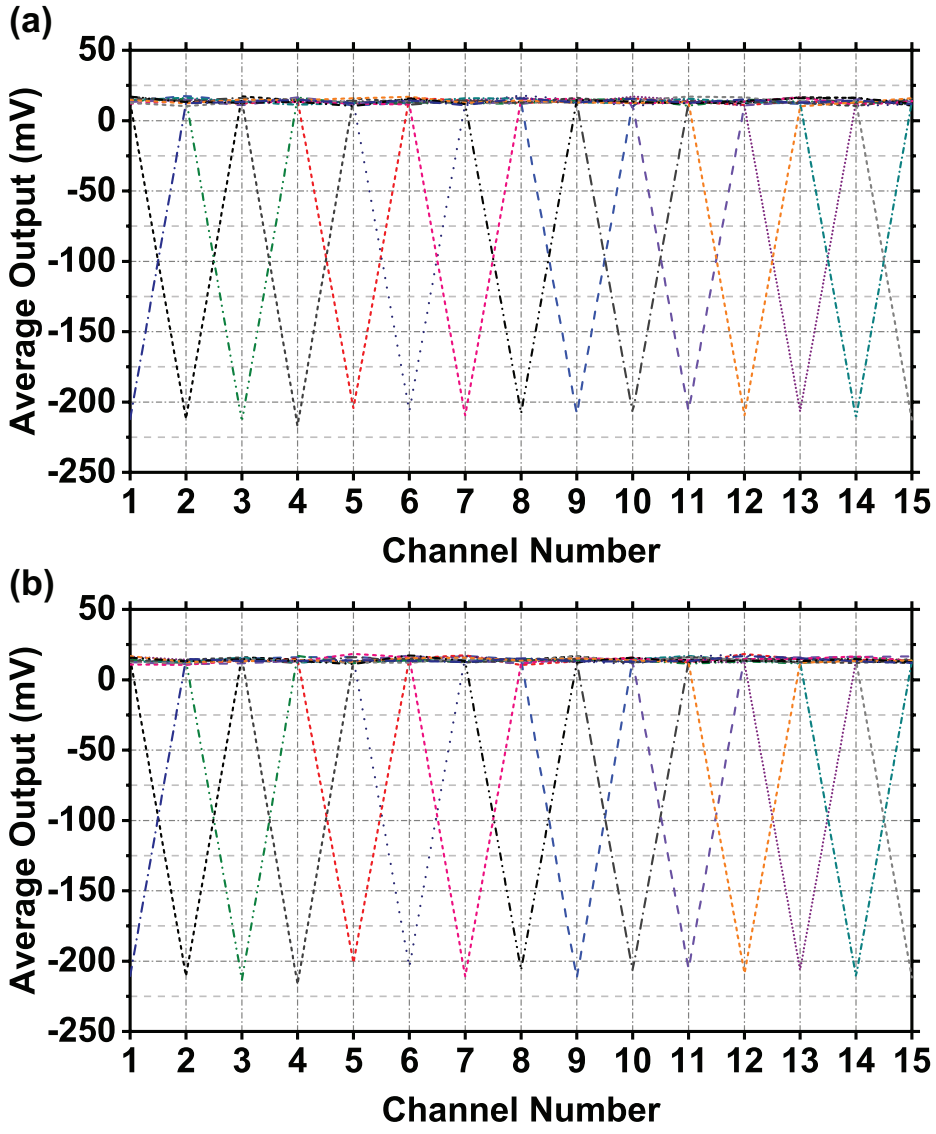

Figure 6.6. Measurement results of the average channel output for all 15 different phases of the PRBS corresponding to (a) capacitor bank 1 and (b) capacitor bank 2.

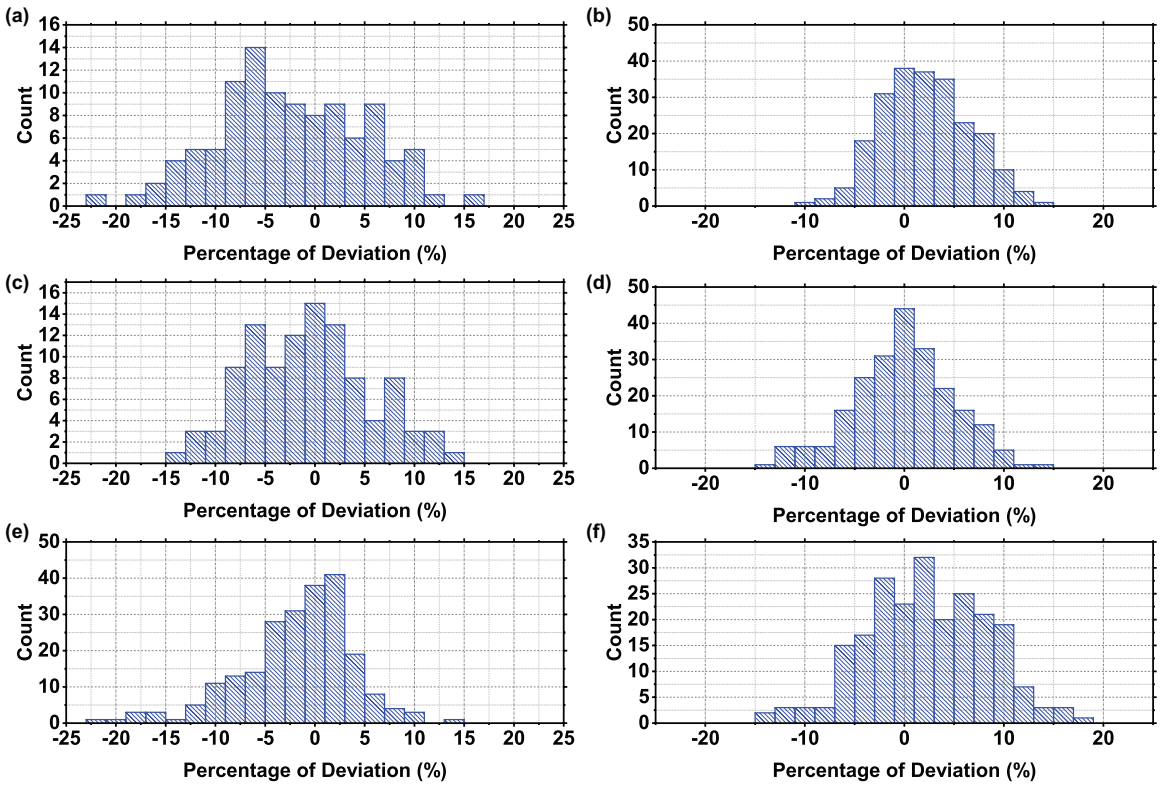

Figure 6.7. Histogram of difference of individual elements of chip # 1 between (a) $\mathbf{P}$ and $\mathbf{P}_{\mathrm{m},1}$, (c) $\mathbf{P}$ and $\mathbf{P}_{\mathrm{m},2}$, and (e) $\mathbf{P}_{\mathrm{m},1}$ and $\mathbf{P}_{\mathrm{m},2}$, and the histogram of the difference of individual elements of chip # 2 between (b) $\mathbf{P}$ and $\mathbf{P}_{\mathrm{m},1}$, (b) $\mathbf{P}$ and $\mathbf{P}_{\mathrm{m},2}$, and (f) $\mathbf{P}_{\mathrm{m},1}$ and $\mathbf{P}_{\mathrm{m},2}$.

an anomaly which could be used to demonstrate the effectiveness of the calibration procedure for devices with large mismatches.

While the extracted matrices improved the SFDR of the IC # 1 significantly, the overall performance of the two chips after calibration was still limited to values between 33 dB to 37 dB over the frequency range. Since the calibration was performed at lower clock rates, frequency dependent effects could potentially limit the best achievable SFDR. To study this, single tone sine waves were put through the system at the much lower clock frequency of 270 MHz. It was observed that the SFDR performance of the chip was only slightly improved compared to that of higher clock frequencies. This showed that the lower frequency of calibration did not limit the SFDR performance to the first order. Next, the SFDR performance of the system

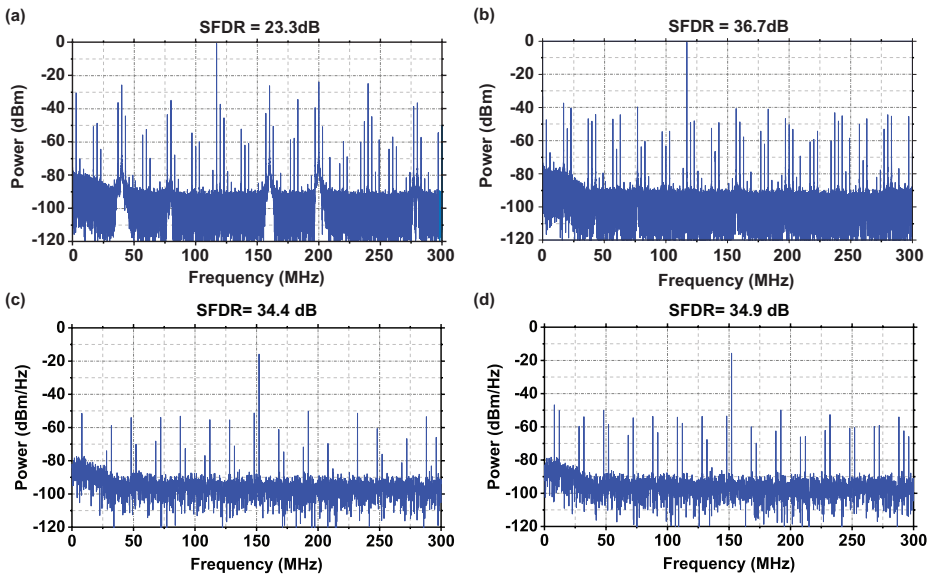

Figure 6.8. Spectrum of the reconstructed signal for a 117 MHz sine wave signal for chip # 1 using (a) the ideal matrix and (b) calibrated matrices, and the Spectrum of the reconstructed signal for a 152 MHz sine wave signal for chip # 2 using (c) the ideal matrix and (d) the calibrated matrices.

was studied as a function of the input RF signal at the clock frequency of 600 MHz for IC #2. Fig. 6.9 shows the measurement results. The dependence of the SFDR performance on input frequency implies that timing skew effects can be a limiting factor in the overall SFDR performance. Thus, the addition of timing calibration procedures may be helpful in further improvement of the SFDR performance.

The improvement of SFDR performance for the IC #1 demonstrated the effectiveness of the proposed matrix and DC offset calibrations. However, the limited achievable SFDR for both ICs signifies the need for further improvement of the calibration procedure. Thus, some modifications to the system implementation are required. The circuitry for the PRBS test sequence generator should be modified to increase its operating frequency so that matrix calibration can be performed at the nominal clock frequency. This can be done by employing larger buffers at the output of the block to ensure sufficient slew rate. Another possible issue that can limit the effectiveness of matrix calibration through the proposed method, is the difference in delays between

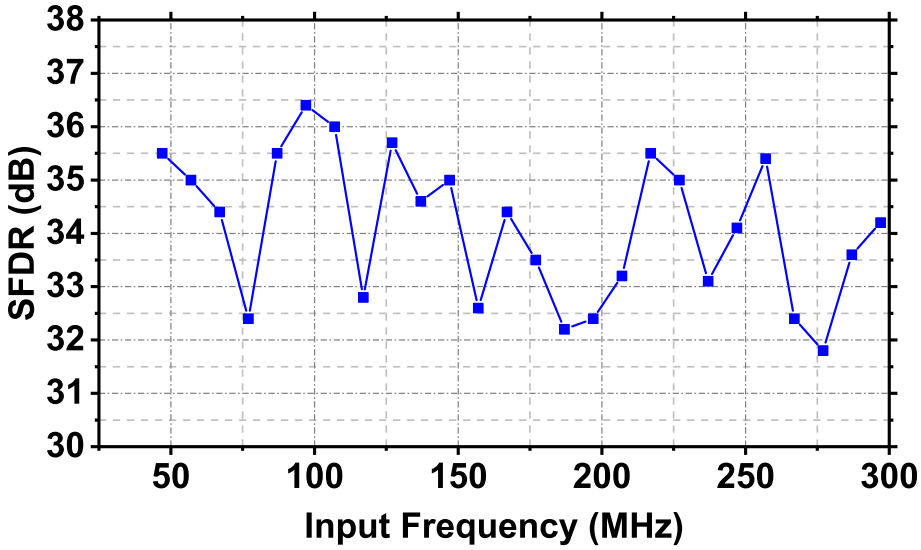

Figure 6.9. SFDR performance of the IC #2 over RF input frequency.

the PRBS signals generated by the test circuit and those generated locally in each channel. This results in uncertainty in the test signals applied to the system. Employment of programmable delay elements on the test signal path and calibration of the delay on this path to the input of each channel can address this issue. In addition, as discussed, a means of calibration for addressing timing skews among channels is required to ensure better performance. Next, the design of a system to address some of the aforementioned issues will be presented.

6.4 Proposed Circuit Modifications for System Performance Enhancement

In order to address the limitations of the implemented system that were highlighted in the previous section, some modifications can be done to the circuit. First, to further enhance the operating frequency of the system, the use of a CMOS technology with shorter gate length can be evaluated. Moreover, additional circuit blocks are required to allow for timing calibrations and the test sequence generator should be modified to enable calibration at higher frequencies.

In this section, modifications to the system architecture introduced in Chapter 4 are proposed to enable calibration of timing skews. The design of additional circuit blocks required to implement these architectural changes is discussed. These circuits were designed and simulated using the TSMC 65nm CMOS technology since future implementations of the system can benefit from this technology to achieve higher operational speed.

A limitation of the system implementation was the lack of timing skew calibrations. To ensure that timing mismatches can be of the order to contribute to this level of SFDR, the variation of the propagation delay through a minimum sized inverter was studied. This was done through Monte Carlo simulations in Cadence. The simulation results over 200 runs of the inverter output for a pulse input are shown in Fig. 6.10. These simulations showed a maximum propagation skew of 6 ps with a standard deviation of 1.1 ps when the circuit is driving a minimum sized inverter as a load. This is a significant delay and can result in limited SFDR performance. A cascade of inverters that are used to buffer the clock signal through channels can add to the variation in delays. Monte Carlo simulation results for a clock frequency of 1 GHz, showed that the cascade of inverters used in each channel to buffer the clock for the system in Chapter 4, can result in propagation delay values with the standard deviation of 1.1 ps and maximum value of 5 ps. As many other elements add to the overall timing mismatches these can lead to significant SFDR limitations. Thus, the goal of the proposed design in this section is to enable the calibration of the timing skews to ensure that these timing skews can be addressed.

Fig. 6.11 shows the top level diagram of the proposed architecture to address timing skews. The receiver employs a fifteen-channel discrete-time signal-processing block with the same architecture as that of Fig. 4.2 along with the additional test sequence generation circuitry. Variable timing delays are introduced to enable compensation of timing skew among the channels.

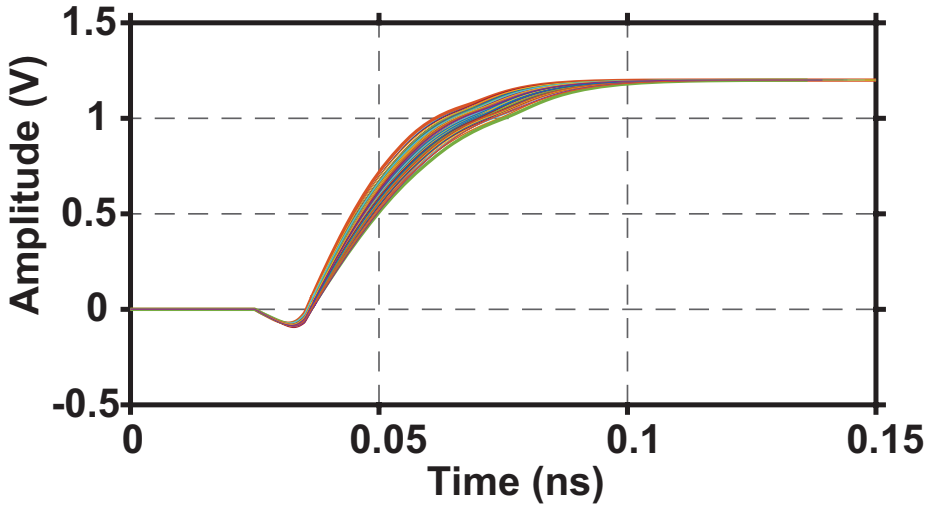

Figure 6.10. Monte Carlo simulation results of a minimum sized inverter output for a pulse input. 200 simulation seeds are run and a maximum delay mismatch of 6 ps is observed. The inverter is loaded with the same inverter.

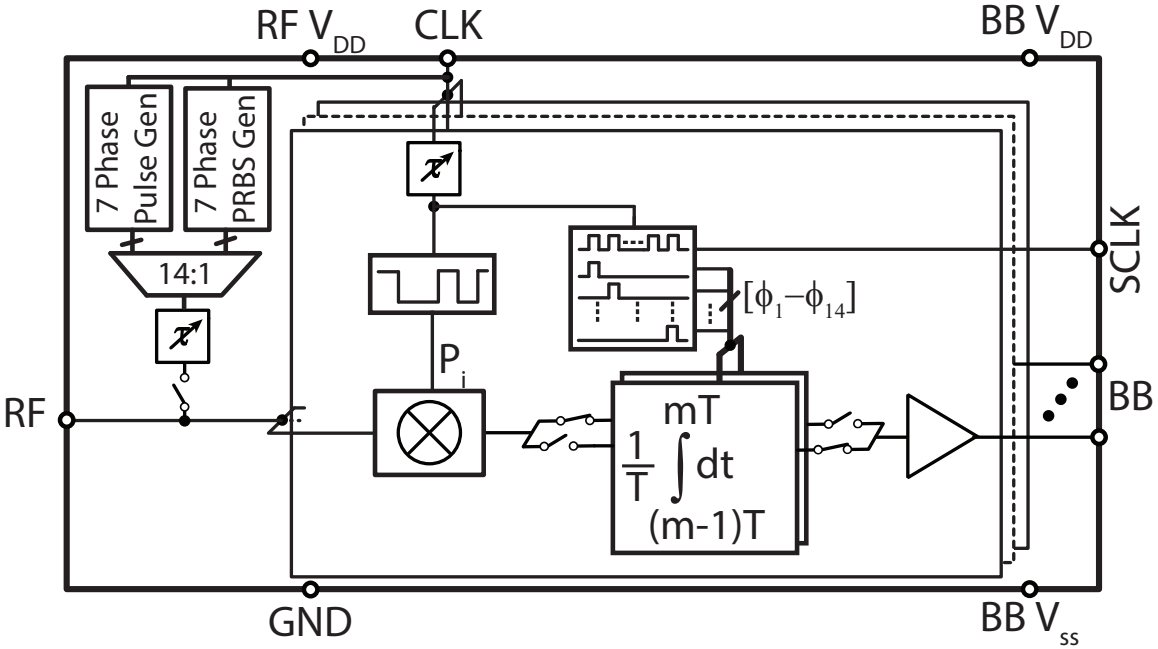

Figure 6.11. Top level schematic diagram of the implemented CMOS circuit in 65nm Technology.

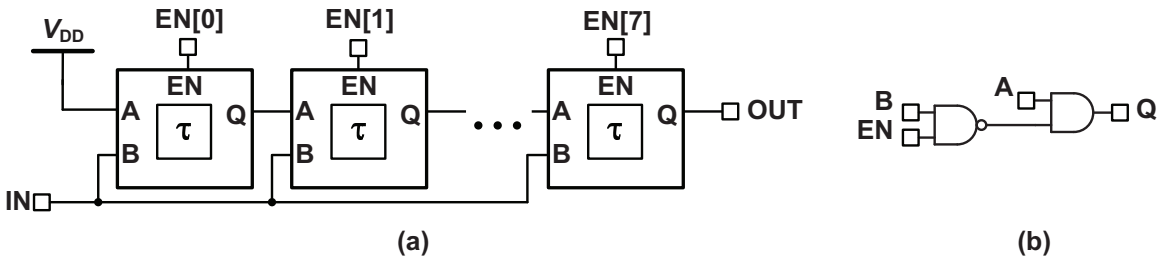

Figure 6.12. Schematic diagram of (a) the full 8 element delay generator and (b) the individual delay cell [73].

6.4.1 Timing Delay Generator Block

As shown in Fig. 6.11, a programmable delay block can be added to the LO generation path for each channel. Based on the analysis presented in Section 6.1.3, to achieve SFDR values greater than 40 dB for a clock frequency of 1 GHz the standard deviation of the timing skew among the channels should be less than 7 ps. Therefore, the programmable delay block was designed to achieve delay resolutions of 14 ps which should ensure the standard deviation of the skew between the channels is within the required range. If a SFDR value in the order of 60 dB is required this resolution should be reduced to below 1 ps. Each block can generate eight different delay values that are controlled by digital enables. The schematic diagram of this block is shown in Fig. 6.12. The propagation delay through the block is controlled by enabling only one of the control signals at each time. The delay is the highest when EN[0] is activated.

Fig. 6.13 shows cadence transient simulation results of the delay generator for a pulse input over different delay settings. The eight element block can create delay values ranging from 14 ps to 112 ps with 14 ps steps. Each delay element dissipates a total power of $\approx$36 μW at a clock frequency of 1 GHz. This delay range covers only a fraction of the clock cycle for a 1 GHz clock signal. A cascade of such delay blocks may be required to ensure all delay values within the system can be compensated for. In addition, if finer resolution delays are required, the delay generator circuit shown in Fig.6.14 may be employed to implement delay values as small as 0.25 ps [37].

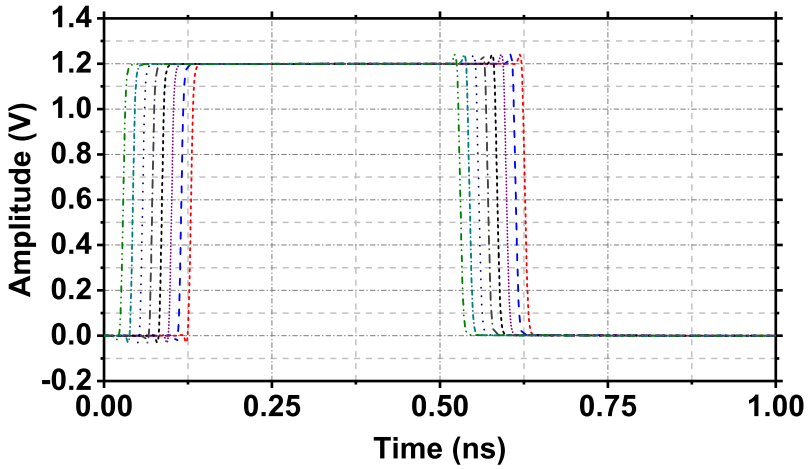

Figure 6.13. Transient simulation results of the delay generator block for a impulse input signal over different delay settings.

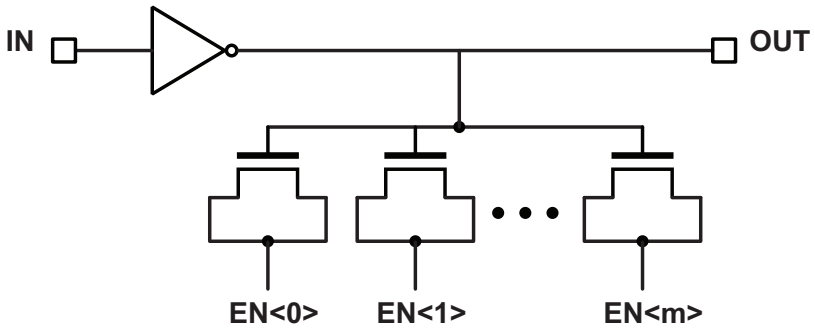

Figure 6.14. Alternative programmable delay generator for finer resolution delays [37].

6.5 Test Sequence Generation Circuitry

A test sequence generation block similar to that shown in Fig. 6.2 can be employed to enable matrix calibration of the system,. In addition to the multi-phase PRBS generation, a pulse generator with a period of $15\times T_{\mathrm{CLK}}$ and a pulse width of T_{CLK} can be implemented. For this sequence, at each sampling period only one of the capacitors collects a non-zero voltage. This can be used to find the relative weighting of each individual capacitor. The pulse generator can be implemented through a circular shift register similar to that used for PRBS generation (see Fig. 6.2(a)). Different phases of the pulse can be selected by tapping from different flip-flop outputs in the shift

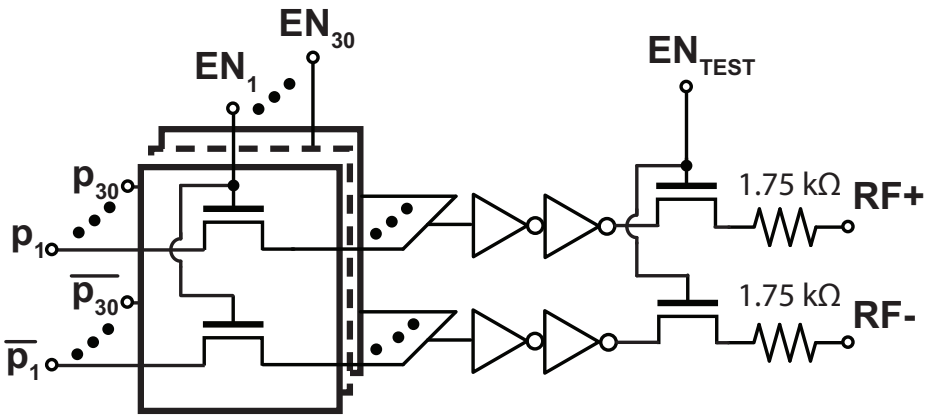

Figure 6.15. Schematic diagram of the 30-1 multiplexer employed at the output of the test sequence generator block.

register. This will enable the generation of clock pulses with delays of 0 to $14T_{\mathrm{CLK}}$. This will allow for testing of all different capacitors. A 30 to 1 multiplexer can be used to select between the fifteen different phases of the PRBS and fifteen phases of the pulse generator. Fig. 6.15 shows the schematic diagram of the multiplexer. To ensure that different outputs of the test sequence generator are phase matched, a symmetric layout with matched lines on RF and clock signals should be employed. Since test sequences are each generated through a single circular shift register, the physical layout of this block occupies a relatively small area which results in smaller variations among elements.

To ensure correct timing between the test circuitry and the LO signals at each channel, the programmable delay blocks of Fig. 6.12(a) can be used in series with the output of the test signal circuitry (see Fig. 6.11). In addition, large driving buffers should be added to ensure sufficient drive at the output of the test sequence generator to drive the load at the input of the system. As shown in Fig. 6.15 these buffers are implemented on the input side of the output enable switch to reduce the loading during the normal operation of the system. Fig. 6.16 shows the simulation result for

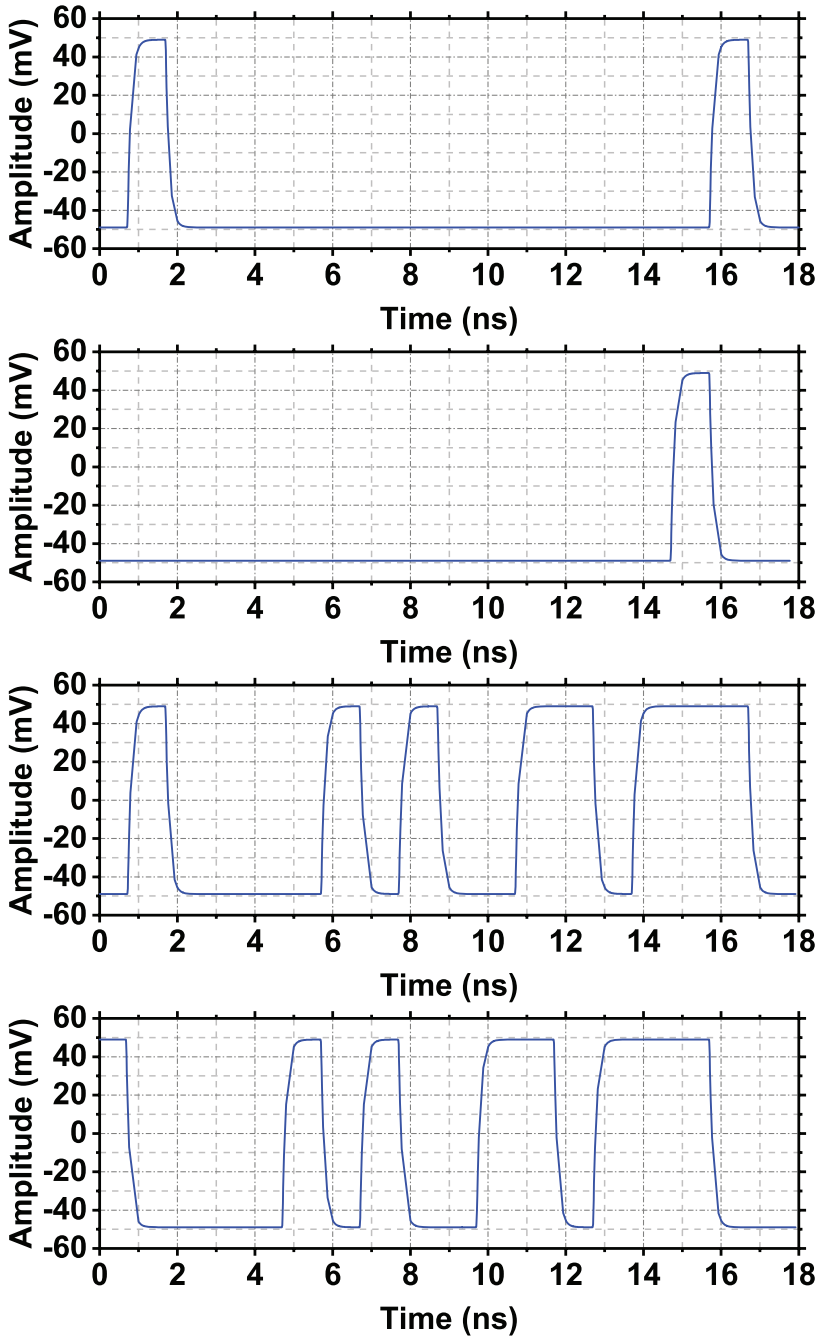

Figure 6.16. Time domain simulation results of the output of the test sequence generator block when (a) ϕ_1 of the pulse generator, (b) ϕ_3, and (c) first phase of the PRBS, are selected.

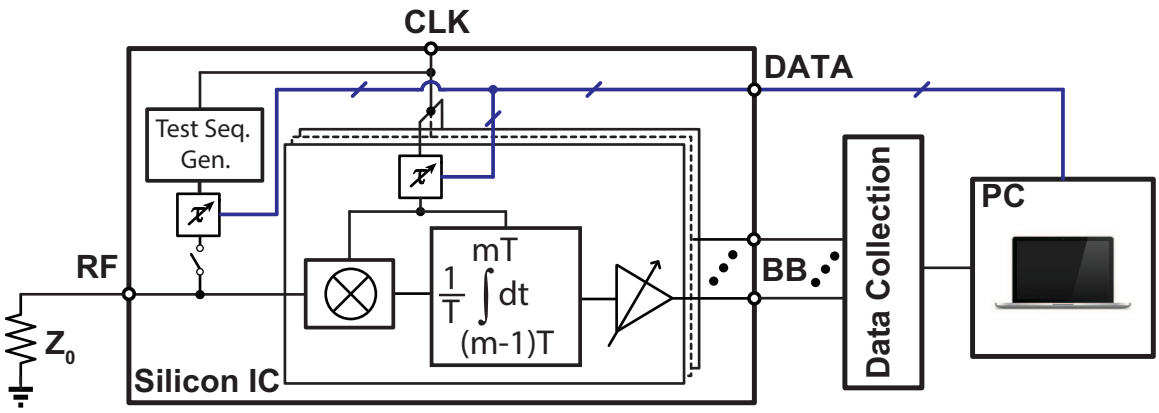

Figure 6.17. Closed loop system employed for calibration of timing skews among channels.

four different test sequences generated by the circuit at a clock frequency of 1 GHz and 100 Ω differential loading along with a 2 pf capacitive load.

6.5.1 Calibration of Timing Mismatches Using the Proposed Delay Blocks

In this section, a step-by-step calibration procedure to address the timing skew between the reference clock of each channel is discussed. This could be carried out, employing the closed loop system shown in Fig. 6.17. In this setup, the test sequence generator is used as a reference signal for calibration of timing skews among the channels. By assuming the timing of the clock in Channel 1 as the reference, the timing skew of other channels can be calibrated with respect to this reference.

For binary values of 1 and -1, by knowing that

$$V_{\text{out}}(\tau) = \Sigma_{\text{t=0}}^{T_s} P(t) \times P(t-\tau) = \begin{cases} 1 & \tau = 0 \\ < 1 & \tau \neq 0 \end{cases}, \tag{6.10}$$

where P is the corresponding sequence and τ is the delay value and programming the test sequence generator and the delay blocks, the calibration procedure can be done. From (6.10) it can be seen that when the delay is matched between the test sequence with the LO of the corresponding channel, the PRBS signals align (see Fig. 6.18(a))

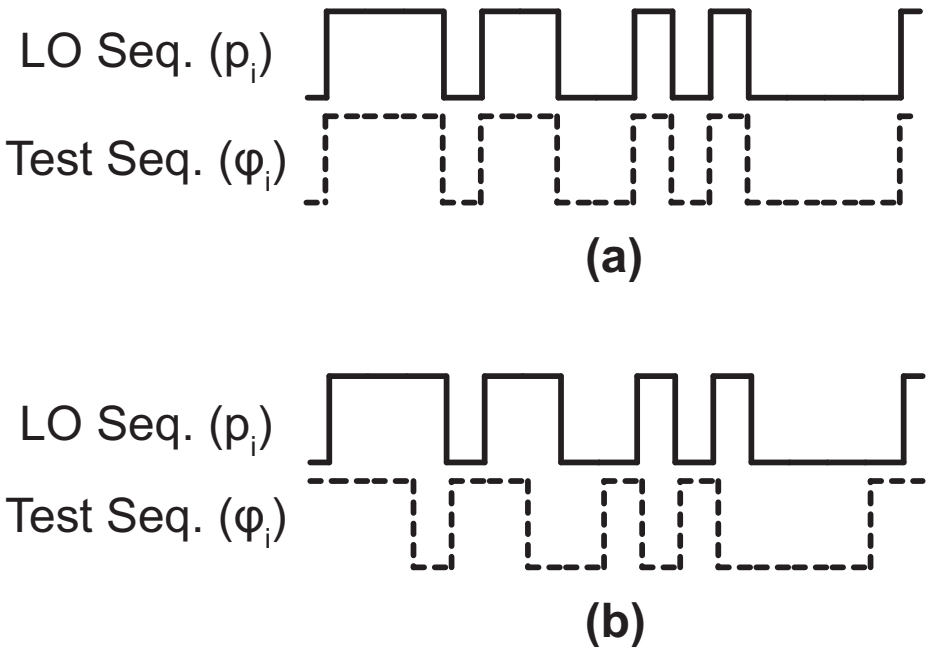

Figure 6.18. Timing diagram of the test sequence at the input of channel 1 along with the LO sequence of Channel 1 for (a) when no delay and (b) a non-zero delay, between the two sequences.

and produce a maximum signal at the output. However, in the non-ideal case, there exists a non-zero delay which can result in mismatch between the two sequences (see Fig. 6.18(b)). This will result in the reduction of the signal at the output of the channel after integration. As a result, an optimization procedure can be employed where the objective function is defined as

$$\begin{cases} max.V_{\text{out}}(\tau) \\ s.t.\ \tau \in [0\ T_{\text{s}}] \end{cases} \tag{6.11}$$

. Keeping this in mind the calibration procedure can be performed as follows

- First, the test sequence generator is programmed to produce the PRBS with the same phase as that of Channel 1. Then, the delay setting of the variable delay block at the output of the test sequence generator is swept. At each state,

the baseband output of the channel is measured and stored. The delay value setting that maximizes the output is selected as the correct value. This delay setting is selected for the delay block and kept for the rest of system operation.

- Next, the test generator is programmed to produce the PRBS with the same phase as that of channel 2. Then the delay block for the clock generation of this channel is swept to maximize the baseband output signal. This value is then selected as the correct delay setting for this channel. This step is repeated for all other channels to find the appropriate timing delay.

The timing of the test sequences is calibrated to the first channel through the first step. Therefore, the calibration of signals in other channels with respect to this sequence ensures matched timing between all channels.

To test the proposed calibration scheme, a Matlab Simulink model similar to that shown in Appendix C was developed for a seven channel system. Random timing delay values with the same resolution as the clock were assigned to channels 2 to 7 and the output of test sequence generator with respect to channel 1. Fig. 6.19(a) shows the spectrum of the reconstructed signal for a sine wave input with normalized frequency of 0.252, when the random timing delays are applied to channels. As can be seen, the presence of the timing delays, results in spurious tones with significant power at the output. A Matlab program was developed to implement the proposed calibration scheme. The program was used to calibrate the timing delays introduced in the Simulink Model. The resulting delay settings for each of the programmable delay blocks were used in the system and Fig. 6.19(b) shows the spectrum of the reconstructed signal for a sine wave input with normalized frequency of 0.252. Since the resolution of the delay errors and the delay generators are the same in this system a perfect reconstruction of the signal is achieved. In a physical implementation of the system the achieved SFDR will be limited based on the resolution of the delay blocks

as predicted by (6.8). Nevertheless, these results demonstrate the effectiveness of the proposed calibration scheme.

A significant advantage of the proposed calibration scheme is its insensitivity to any gain mismatches among channels. This is due to the fact that each channel delay is optimized based on its own output. To verify this, random gain mismatches with zero mean and standard deviation of 0.001 were added to the system model and calibration of the timing skews was carried out with the presence of these errors. Prior to the calibration the timing skews were the dominant factor and the spectrum of the reconstructed signal was similar to that of Fig.6.19(a). However, after performing timing skew calibration, the gain mismatches were left as the dominant factor and the SFDR was improved to about 52 dB as shown in Fig.6.20. In addition, the proposed technique results in the calibration of the timing delay between the sequence generator and all channels. This will enable more accurate matrix calibrations employing the PRBS or pulses as discussed earlier.

6.5.2 Other Mechanisms of Timing Skew

While the proposed calibration technique ensures matched timing between the reference clocks of all channels, it does not address some of the other possible timing mismatches in the system. Some of these effects will be discussed in this section.

Another aspect of timing errors that can limit the system performance is the skew between the ADC channels. To analyze this effect, the output of each amplifier can be assumed to have a first order step response in the form of

$$V_{out} = V_0(1 - e^{-t/\tau}), \tag{6.12}$$

where τ is the time constant and V_0 is the ideal final value of the output. Then the timing error at each ADC channel (ΔT_{ADC}) results in a voltage error in the sampled value which can be written as

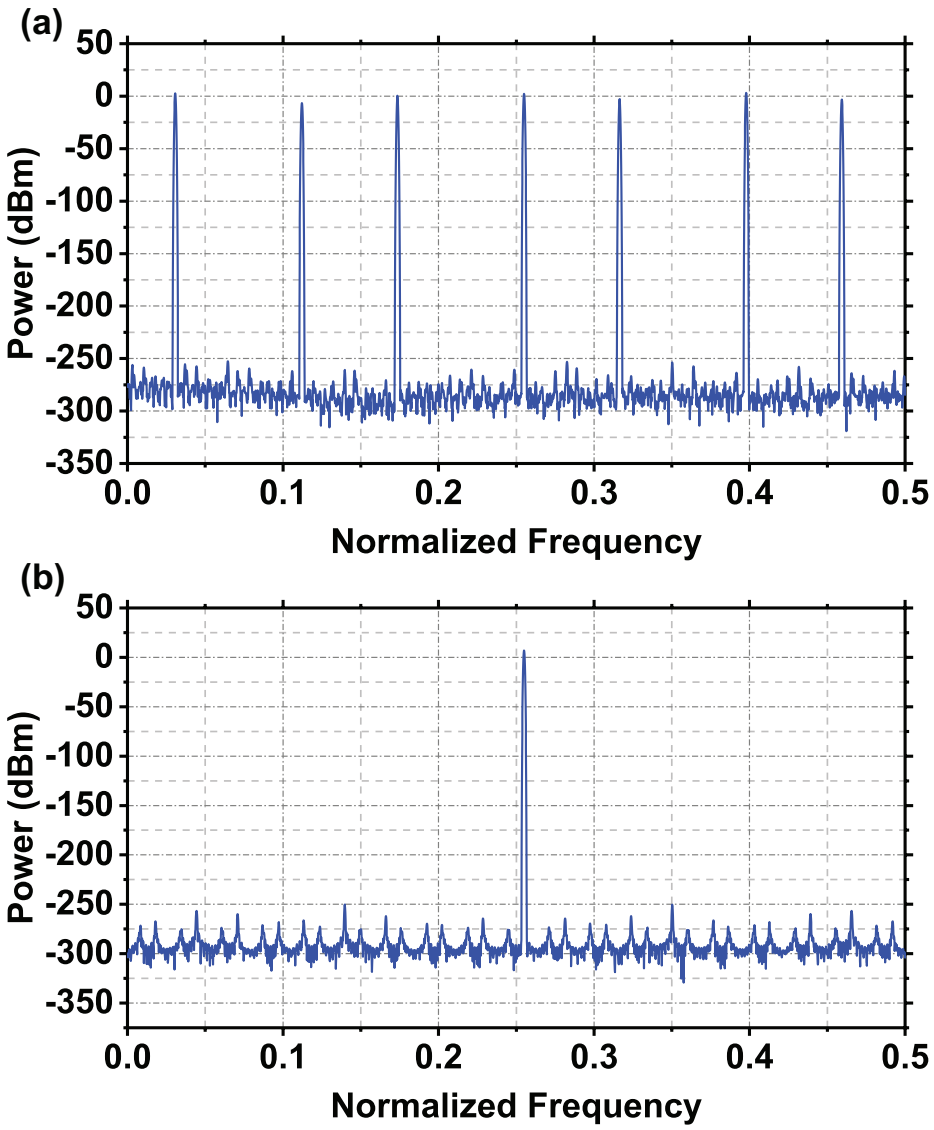

Figure 6.19. Matlab simulation result for the spectrum of the reconstructed signal for a sine wave input at 255 MHz for (a) a system with random timing skew among four channels, (b) after calibration of timing skews.

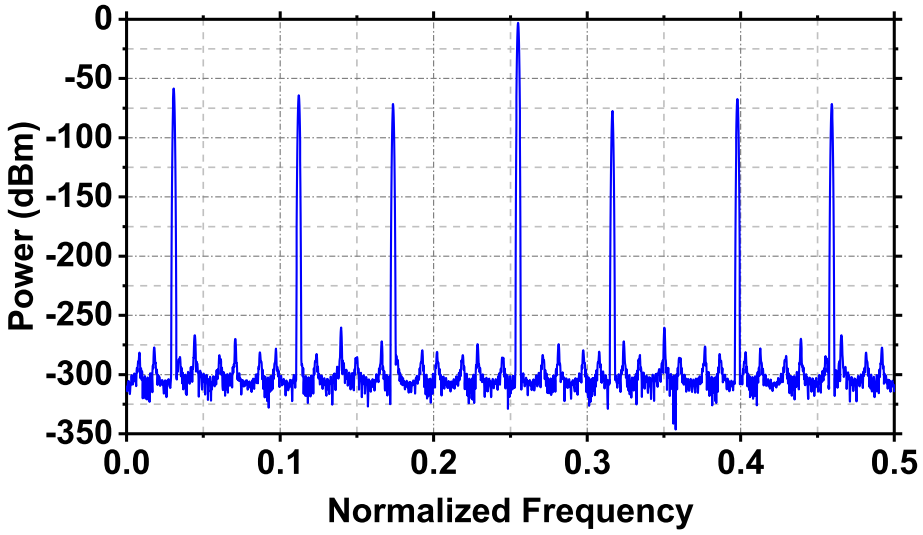

Figure 6.20. Matlab simulation result for the spectrum of the reconstructed signal for a sine wave input after calibration of the timing skews with the presence of gain mismatches among channels.

$$\Delta V_{out} = \frac{V_0}{\tau} e^{-t_0/\tau} \Delta T_{\mathrm{ADC}}, \tag{6.13}$$

where t_0 is the ideal sampling time. This voltage error results in the scaling of the output signal and can be studied as a gain mismatch effect with a value of $(\frac{1}{\tau} e^{-t_0/\tau} \Delta T_{\mathrm{ADC}})$ similar to those studied in Chapter 3. Calibration of gain mismatches can be used to address this issue.

The mismatch in devices on the clock path can also lead to variations in duty cycles of the clocks among different channels. This effect can be studied by considering the sampling procedure. The sampling circuit can be modeled as a first order RC system with a step response of

$$V_{\mathrm{S}} = V_{\mathrm{in}}(1 - e^{-\Delta t/\tau}), \tag{6.14}$$

where V_{S} is the sampled signal, V_{in} is the input signal, τ is the time constant of the circuit and Δt is the switch on-time. The change in duty cycle would result in variation of Δt. This will in turn result in the final value of the sampled signal to have an error. Therefore, the duty cycle variation has a similar effect to that of ADC

timing skews and results in scaling of the sampled signal which can be modeled as a gain error and addressed accordingly.

The procedures introduced in this chapter are designed to address inter-channel mismatches. However, intra-channel mismatches can also result in degraded system performance. As the elements in each channel can be implemented in close proximity process variations are expected to be smaller and are not addressed in this dissertation. However, future work may be done to quantify the effect of such mismatches and further calibration technique may be employed to reduce such effects.

6.6 Summary

In this chapter calibration procedures for addressing systematic errors including DC offsets, gain mismatches, and timing skews were introduced. It was discussed that the first two sources of error can be compensated in digital domain. This was carried out by introducing a set of known input signals to extract the effective matrices. On the other hand, calibration of timing skews should be addressed through the addition of programmable delay elements to the clock path.

The required circuitry for enabling matrix calibration by generating PRBS as test sequence was introduced. The circuit was implemented as part of the prototype IC and the effectiveness of the calibration procedure was studied through measurements of two fabricated integrated circuits. While performance enhancement was observed for one IC with the use of calibration, it was observed that the SFDR performance was limited to values between 31-38 dB. In addition, this particular IC had worse initial SFDR performance due to larger variations. It was observed that for the second IC which had a better SFDR performance to begin with the enhancement due to calibration was minimal. It was discussed that this limited performance enhancement can be due to the lack of timing skew calibration which also limited the effectiveness

of the proposed gain calibration scheme due to timing errors between test sequence generator and different channels.

Alternative circuit topologies were proposed to further enhance the system performance. Programmable delay blocks were introduced at each channel to enable the calibration of timing skews. These delay elements were implemented with a resolution of 14 ps which would ensure that spurious tones due to the timing skews will be 40 dB below the message tone. A timing skew calibration technique was proposed to enhance the SFDR performance of the system. Matlab Simulink models were developed to demonstrate the effectiveness of the proposed calibration technique. Monte Carlo simulations demonstrated that SFDR limitations due to both gain mismatches and timing skews are in the same order. As such, both may need to be addressed through calibration techniques. An advantage of using the test sequence generator proposed in this chapter is the fact that it can be used for both gain and timing skew calibration. The implementation of the timing skew calibration enables more accurate gain calibration through ensuring correct timing between sequence generator and LO signals. Thus, a complete calibration scheme should employ both techniques in the order of timing skew first and gain calibration second. Further implementation and performance enhancement of these techniques is beyond the scope of this dissertation and will be left for future work.

CHAPTER 7

CONCLUSION AND FUTURE WORK

In this dissertation a new approach to extending the blocker tolerance of wideband receivers was introduced. It was shown that the combination of passive mixer first approach and the use of a library of pseudo random binary sequences (PRBS) as LO signals may be employed to further enhance the linearity of wideband receivers. The proposed technique while enhancing the linearity of the system does not degrade the noise performance and thus improves the overall signal-to-noise-and-distortion-ratio (SNDR). The use of all possible shifted versions of the PRBS at each LO signal allows for the full reconstruction of the signal in digital domain through simple multiplication and summation of channel outputs. The employment of multiple channels to enable the full signal reconstruction can lead to errors which are due to property mismatches among different channels. These mismatches stem from process variation in the integrated circuit and thus require careful attention to reduce their effects through implementation techniques and calibration procedures.

The measurement results of the fabricated integrated circuit are promising and demonstrate good agreement with the theoretical analysis. Comparison with the sate-of-the-art shows that the proposed architecture can achieve very high in-band IIP3 of better than 5.8 dBm over a wide instantaneous bandwidth of 40-300 MHz. While the total power consumption is increased due to the required load drive of the baseband amplifier, the prototype IC still achieves comparable or better power per instantaneous bandwidth compared to state-of-the-art receivers. Further enhancement can be achieved by integrating the ADCs on-chip to relax the required driving capability

of the output stages. These results demonstrate the effectiveness of the proposed architecture in achieving large IIP3 values over a wide instantaneous bandwidth. This is a significant result as future generation of wireless system rely on wider operational bandwidths in areas with densely occupied spectrum that can contain large blockers and interferers.

7.1 Future Work

While the effectiveness of the proposed architecture was demonstrated through a prototype IC, this design by no means is optimized. Therefore, further investigations in the design of different circuit blocks are required to enhance the overall performance. As an example, the use of an active integrator instead of the switched-capacitor approach may prove beneficial. In addition, technology nodes with shorter gate lengths can be used to enhance operation frequency as well as reducing the loss in the sampling switches.

As an instance, to further enahnce the performance of the RF section of the system different flip-flop architectures can be studied. As the flip-flops are used both in PRBS and non-overlapping clock generation they play a critical role in the operational speed of the overall system. In [74] a comparison between different flip-flop architectures are presented. It is showed that hybrid latch flip-flop architecutre can achieve higher operational speed compared to others. The schematic diagram of the HLFF circuit is shown in Fig. 7.1 [75]. The hybrid nature of this architecture stems from the transparent operation on the transition of the clock. This is achieved by the delay generated through the three series inverters at the input.

One of the main advantages of the HLFF is the lower sensitive to clock skew which stems from the hybrid structure employed in the design [75]. This reduces the sensitivity of the system to limited slew rate in the clock path. Through Cadence simulation it was verified that these flip-flops can be operated at clock frequencies as

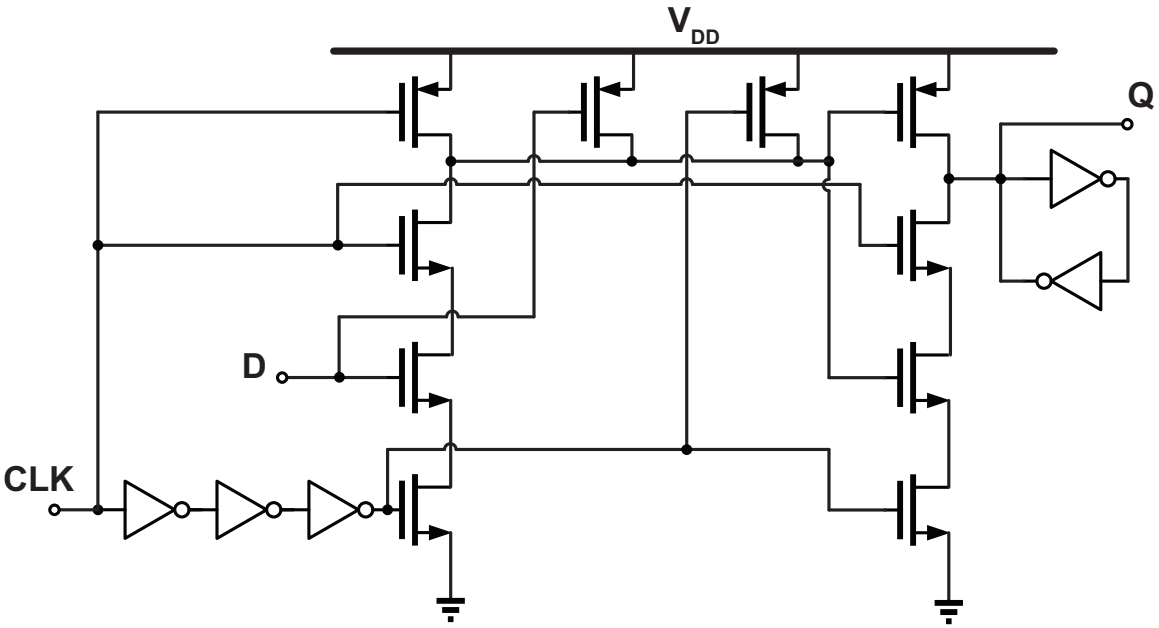

Figure 7.1. Schematic diagram of the hybrid lath flip-flop circuit used to increase the operating speed of the system.

high as 4 GHz. One drawback of this topology is the slightly higher dynamic power consumption of the device. If further power optimization is required, the use of other flip-flop topologies such as the ones proposed in [76–79] can be investigated.

Moreover, other binary sequences such as those discussed in [80] or combinations of different sequences can be studied to replace PRBS signals for possible improvement in the overall system performance. The possibility of using the proposed architecture to receive signals centered at higher frequency can also be investigated. This may potentially be achieved in two ways. First, a down conversion mixer may be employed to move the center frequency of the message signal to baseband which is then processed by the system proposed in this dissertation. Second, by solely using matching networks at the input of the system to shift the power match to higher operational frequencies. The latter effectively creates a filtering response at higher Nyquist zones and requires higher operational bandwidth at the sampling switches.

APPENDIX A

PROPERTIES OF PRBS AND MATRIX OF PRBSS

The technique proposed in this dissertation employs pseudo-random-bit-sequences (PRBS) as local oscillator (LO) signals in a RF receiver. This is done in order to reduce the effective amplitude of the input signals as well as enabling wideband operation of the system. Therefore, the main properties of these signals are reviewed in this chapter to provide sufficient background for the analysis of the system operation presented in this document. A PRBS is a sequence of binary values that exhibits properties close to that of random numbers [81]. One main advantage of PRBS over random values is its periodicity. These sequences are generated through deterministic algorithms which create fixed sets for a defined length. Due to their deterministic nature these sequences are commonly used for hardware implementations, where signals with similar properties to random signals are required.

These sequences have several important properties including [81]:

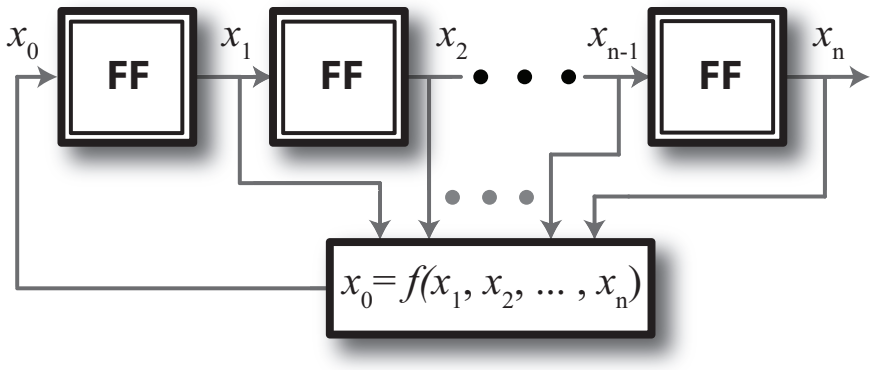

Figure A.1. A schematic diagram of an n-bit LFSR.

- For a PRBS of length N the number of 1s and -1s only differ by one. Meaning for a large N the probability of 1 and -1 is close to 0.5. For a truly random binary value this probability is 0.5.

- The auto-correlation of each sequence with a shifted version of itself is minimal. For a binary sequence S(n) with length of N, the auto-correlation function is defined as

$$C(m) = \frac{1}{N}\sum_{i=1}^{N} S(n)S(n+m). \tag{A.1}$$

  It can be shown that for a PRBS of length N with (N-1)/2 elements of +1 and (N+1)/2 elements of -1, the auto-correlation function is two valued and can be derived as

$$C_{\text{PRBS}}(m) = \begin{cases} 1 & m = 0 \\ -1/N & 0 < m < N \end{cases} \tag{A.2}$$

These properties make PRBS a close approximation of a binary random variable while exhibiting periodic behavior. (A.2) shows that a PRBS is approximately orthogonal to all shifted versions of itself. Hence, a set of N PRBSs of length N can be used to form a set of vectors that are each minimally correlated with each other. Such a set could be used to project an input signal to N different spaces that are approximately orthogonal to each other. This property will prove critical in enabling the reconstruction of the message signal in the proposed technique and will be discussed in the next chapter.

PRBS signals have maximum lengths of $2^n - 1$ where $n = 1, 2, 3, ...$ In most mathematical literature these are called maximum length sequences or m-sequences. These sequenes have been extensively studied in literature for their use in communication, coding, fault detection, and so on [40, 82–85] . For the purpose of this document all PRBSs are assumed to be maximum length. Each maximum length PRBS sequence for a defined length can be generated by utlizing a linear feedback

Table A.1. Different number of storage elements in a LFSR with the corresponding PRBS length one possible characteristic polynomial [87].

n	Maximum Length of PRBS (N)	characteristic polynomial (f)
2	3	$x^2 + x + 1$
3	7	$x^3 + x + 1$
4	15	$x^4 + x^3 + 1$
5	31	$x^5 + x^3 + 1$
6	63	$x^6 + x^5 + 1$
7	127	$x^7 + x^4 + 1$
8	255	$x^8 + x^4 + x^3 + x^2 + 1$
9	511	$x^9 + x^5 + 1$
10	1023	$x^10 + x^7 + 1$

shift register (LFSR) which consists of n storage elements and a processing block in a feedback loop as showed in Fig. A.1 [81, 86]. The function f can be written as [81]:

$$f(x_1, x_2, ..., x_n) = c_1x_1 \oplus c_2x_2 \oplus ... \oplus c_nx_n, \tag{A.3}$$

where c_is are constants with valuess of 1 or 0. The function f ,that generates the feedback input to the shift register changes for different values of n. This function is defined through its characteristic polynomial. The power of each term in the polinomial corresponds to the element along the loop which its output should be taken. Several polynomial functions may exist for each maximum PRBS length and Table A.1 shows an example for each PRBS length [87].

A.1 PRBS Matrix

In the discussion of the proposed technique it will prove helpful to describe the system operation through a matrix representation. To do so, a N by N matrix ($\mathbf{P}$) can be formed using N shifted versions of a PRBS with each row including one of the shifted versions of the same PRBS. An example of such a matrix for N=7 can be written as

$$P = \frac{1}{7}\begin{bmatrix} -1 & -1 & -1 & 1 & 1 & -1 & 1 \\ 1 & -1 & -1 & -1 & 1 & 1 & -1 \\ -1 & 1 & -1 & -1 & -1 & 1 & 1 \\ 1 & -1 & 1 & -1 & -1 & -1 & 1 \\ 1 & 1 & -1 & 1 & -1 & -1 & -1 \\ -1 & 1 & 1 & -1 & 1 & -1 & -1 \\ -1 & -1 & 1 & 1 & -1 & 1 & -1 \end{bmatrix} \tag{A.4}$$

In this document such a matrix is referred to as the PRBS matrix. This matrix and its inverse exhibit critical properties that will be discussed next.

A.1.1 Inverse of the PRBS Matrix

P is a square matrix, hence its invertibility can be studied. The inverse of this N by N matrix can be found by taking advantage of some of the PRBS properties. First, the sum of all elements of a PRBS is equal to 1. Second, multiplication of any square matrix with its inverse yields the identity matrix (**I**). The latter requires that

$$\sum_{n=1}^{N} \mathbf{p}_i[n]\hat{\mathbf{p}}_k[n] = \begin{cases} 1 & i = k \\ 0 & i \neq k \end{cases} \tag{A.5}$$

where $\mathbf{p}_i$ is the ith row of the **P** matrix and $\hat{\mathbf{p}}_k$ is the kth column of the inverse matrix($\hat{\mathbf{P}}$). Each column of the inverse matrix ($\hat{\mathbf{p}}_k$) can be expressed as a linear function of the corresponding row of the **P** ($\mathbf{p}_i$) in the form of

$$\hat{\mathbf{p}}_k[n] = \alpha \mathbf{p}_i[n]^{\mathbf{T}} + \beta\overline{\mathbf{1}}. \tag{A.6}$$

where $\overline{\mathbf{1}}$ is a column vector of length N having all entries equal to unity. Replacing (A.6) in (A.5) and using the autocorrelation properties of a PRBS gives

$$N\alpha - \beta = 1, \tag{A.7}$$

$$-\alpha - \beta = 0. \tag{A.8}$$

Leveraging these, α and β can be found as

$$\alpha = \frac{1}{N+1}, \beta = \frac{-1}{N+1}. \tag{A.9}$$

Therefore, each column of the inverse matrix is a scaled and offseted version of the corresponding row of the **P** matrix. For a PRBS with binary values of +1 and -1 the inverse matrix columns would have binary values of 0 and -2/(N+1).

A.2 Power Spectral Density of a Repeating PRBS

In the study of the proposed technique it will prove beneficial to use the power spectral density (PSD) of a repeating normalized PRBS. It will be discussed in Chapter 2 that the PSD of each column of the inverse matrix is required to find the effect of system nonidealities and noise performance. Thus, this section aims to find a closed form expression for the PSD of such sequence ($\hat{\mathbf{p}}_k$), that has the form of (A.6), as a function of N.

First, it should be noted that the PSD of a discrete-time sequence can be found by taking the discrete Fourier transform (DFT) of its autocorrelation function. Leveraging the results of (A.2) and (A.9), the autocorrelation function of $\hat{\mathbf{p}}$ can be found as

$$C_{\hat{\mathbf{p}}}(\tau) = \frac{2N^2}{N+1}\delta(\tau) + \frac{N^2}{N+1}\sum_{k=1}^{(N-1)}\delta(\tau - kTs). \tag{A.10}$$

Taking the DFT of the above equation would give the PSD of the PRBS as

$$P_{\hat{\mathbf{p}}}(f) = 1\delta(f) + \frac{1}{N+1}\sum_{k=1}^{N}\delta(f \pm kf_s). \tag{A.11}$$

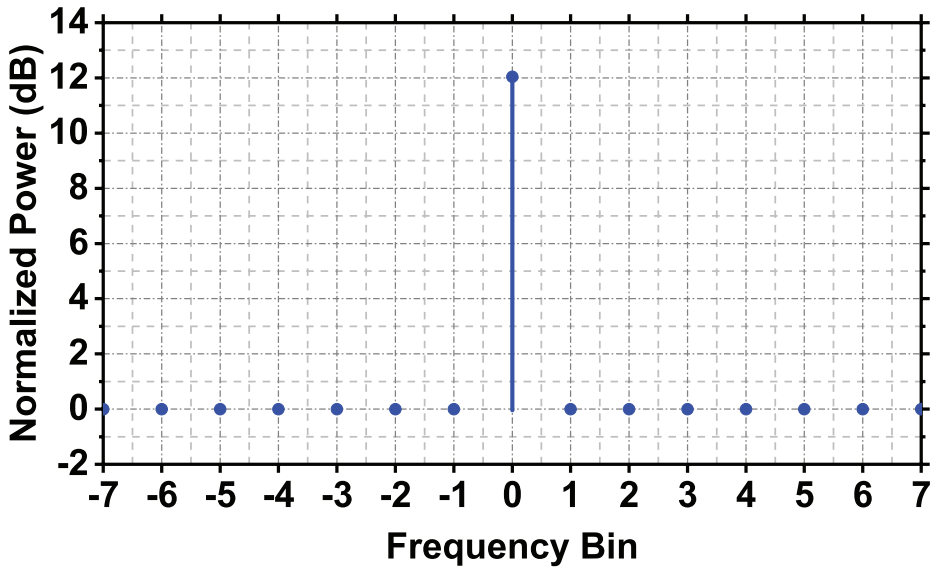

Figure A.2. The spectrum of the inverse PRBS normalized to the power at non-zero frequency bins.

This shows that each column of the inverse matrix has N+1 times higher power at baseband. This can also be seen in Fig. A.2 where the normalized spectrum of the inverse PRBS is plotted.

A.3 Fourier Series Analysis

Another aspect of the PRBS matrix that will prove helpful in the analysis of the proposed technique is the Fourier series of each individual PRBS. The Fourier series of the normalized ith row with length N can be written as [81, 88]

$$p_i[n] = -\frac{1}{N^2} + \frac{2\sqrt{N+1}}{N^2} \sum_{k=1}^{(N-1)/2} \cos(\frac{2\pi k\,(n-i)}{N} + \phi_k), \tag{A.12}$$

where ϕ_k is the phase of $\mathbf{p}_N$, and n is an integer number corresponding the sample number ($n \in [0N-1]$) [1]. (A.12) shows that the PRBS has less signal power at DC

[1]for the purpose of this document that last row of the matrix is assumed to be the reference PRBS where other rows are shifted versions of it.

which would imply that the inverse should have higher power at DC. This is consistent with result in (A.11). In addition, (A.12) shows a constant phase progression among shifted versions of the PRBS which distinguishes different rows and minimizes the correlation among baseband samples.

APPENDIX B

MATLAB CODES USED FOR DATA PROCESSING

This chapter presents some of the main Matlab codes used in this work for processing the signal.

The Matlab code used to process the data from the measurements and produce the fully reconstructed RF signal:

```
function [ Output,YTc,Y ] = TIP( adcS,adcM,f,r,t)
% adcS and adcM are the data sets collected by the two ADCs,
    f is the sampling frequency, and  r and t variables are
    used to compensate for any mismatch in the data
    acquisition trigger between the two boards (usually within
     1 or 2 samples)
% Scaling the data collected from the ADCs to the full ADC
    swing and synchronizing the outputs of the two FPGA boards
     and forming a matrix of measurements.
Y(1,:)=(((adcS(t:end-r+1,1)'-mean(adcS(:,1)))/2^13));
Y(2,:)=-1*(((adcM(r:end-t+1,8)'-mean(adcM(:,8)))/2^13));
Y(3,:)=(((adcS(t:end-r+1,2)'-mean(adcS(:,2)))/2^13));
Y(4,:)=-1*(((adcM(r:end-t+1,6)'-mean(adcM(:,6)))/2^13));
Y(5,:)=(((adcS(t:end-r+1,3)'-mean(adcS(:,3)))/2^13));
Y(6,:)=-1*(((adcM(r:end-t+1,5)'-mean(adcM(:,5)))/2^13));
Y(7,:)=(((adcS(t:end-r+1,4)'-mean(adcS(:,4)))/2^13));
Y(8,:)=(((adcS(t:end-r+1,5)'-mean(adcS(:,5)))/2^13));
```

```
Y(9,:)=-1*(((adcM(r:end-t+1,7)'-mean(adcM(:,7)))/2^13));
Y(10,:)=(((adcS(t:end-r+1,6)'-mean(adcS(:,6)))/2^13));
Y(11,:)=-1*(((adcM(r:end-t+1,4)'-mean(adcM(:,4)))/2^13));
Y(12,:)=(((adcS(t:end-r+1,7)'-mean(adcS(:,7)))/2^13));
Y(13,:)=-1*(((adcM(r:end-t+1,2)'-mean(adcM(:,2)))/2^13));
Y(14,:)=(((adcS(t:end-r+1,8)'-mean(adcS(:,8)))/2^13));
Y(15,:)=-1*(((adcM(r:end-t+1,3)'-mean(adcM(:,3)))/2^13));
YTc=Y;
% Removing the DC periodic DC offsets
for j=1:15
    YTc(j,1:2:end)=Y(j,1:2:end)-mean(Y(j,1:2:end));
    YTc(j,2:2:end)=Y(j,2:2:end)-mean(Y(j,2:2:end));
end
% Providing the measured data for reconstruction of the input
    signal
[Output]=FP(YTc);
% plotting the spectrum of the reconstructed signal and
   finding the SFDR value.
sfdr(Output,f)
end
```

The Matlab code used to process a set of measurements and reconstruct the full length RF input.

```
function [Xout] = FP(D)
% Generate the P matrix used on the chip
PRBSr=[1 1 1 -1 1 1 -1 -1 1 -1 1 -1 -1 -1 -1 ]/15;
PRBSr=circshift(PRBSr',1)';
P(1:15,1:15)=0;
```

```
for i=1:15
    P(i,:)=PRBSr;
    PRBSr=circshift(PRBSr',1)';
end
% Reconstruct the RF input signal by using the inverse matrix
for i=1:length(D(1,:))
    Xout((1+(i-1)*15):(15+(i-1)*15))=P\D(:,i);
end
end
```

APPENDIX C

BLOCK DIAGRAMS OF THE SIMULINK MODEL

In this appendix the schematic diagrams of all sub-blocks used to implement the behavioral model of the system in Simulink are presented. Each delay block generates a unit delay and the total timing of the simulation is set to 150000 units wit unit steps.

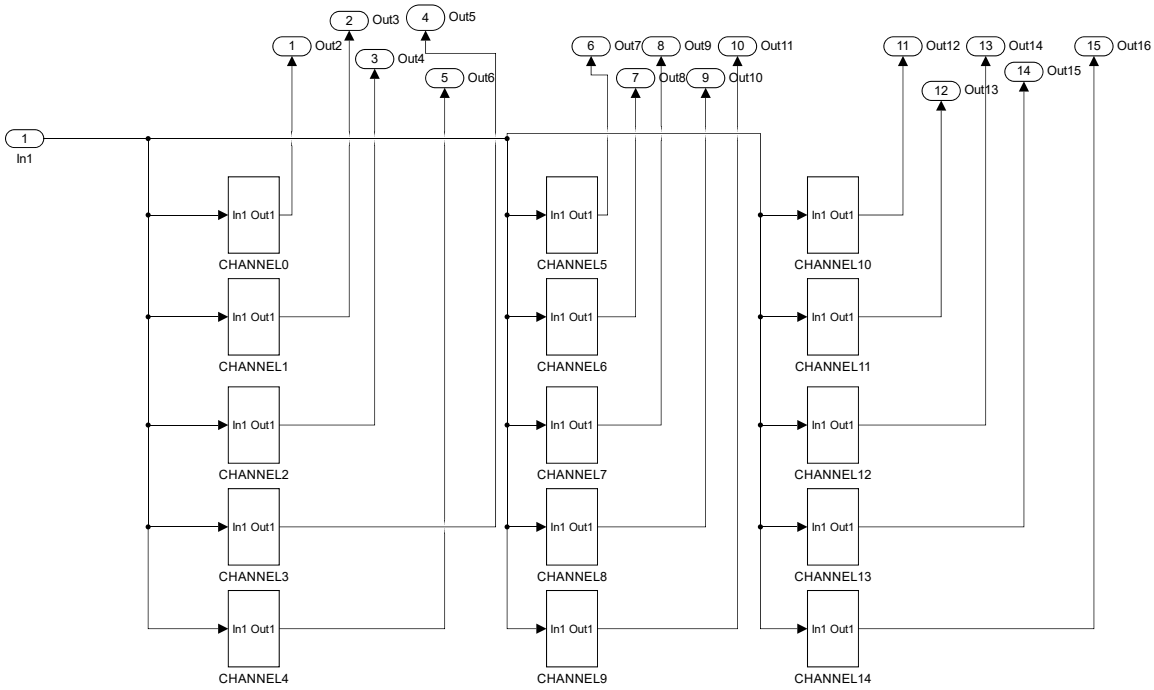

Figure C.1. Top level diagram of the Simulink model for the 15 channel system.

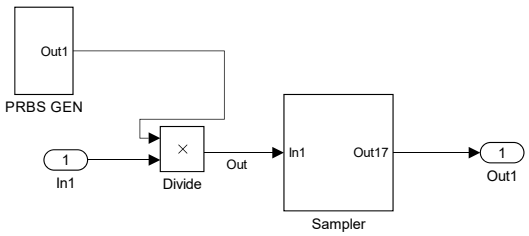

Figure C.2. Schematic diagram of each channel.

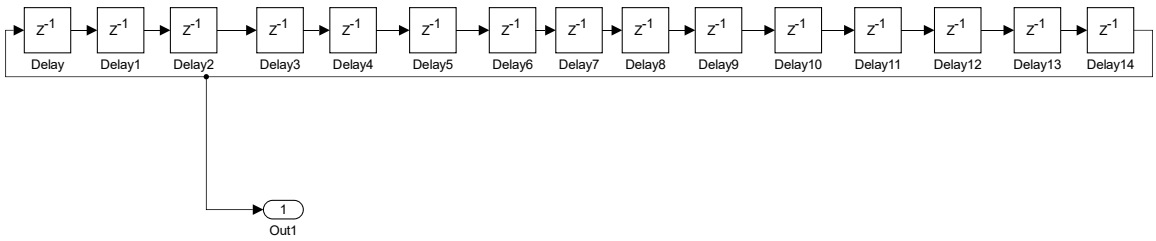

Figure C.3. Schematic diagram of the PRBS generator. The initial value of delay elements for each channel was set based on the PRBS.

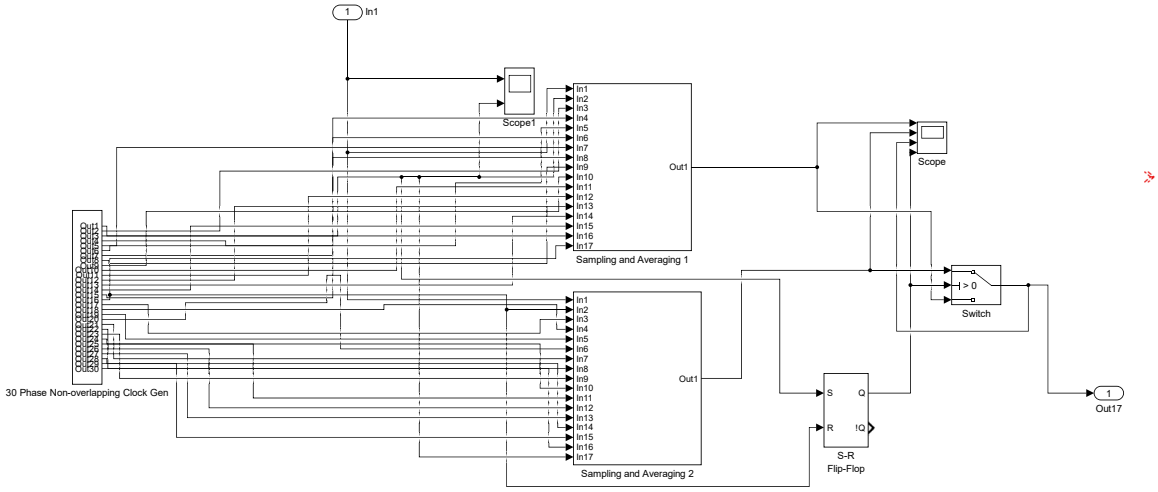

Figure C.4. Schematic diagram of the sampler.

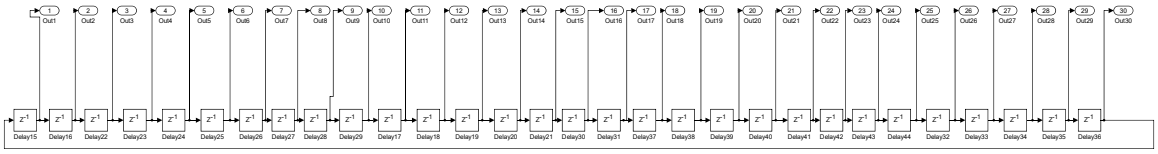

Figure C.5. Schematic diagram of the 30 phase non-overlapping clock generator. The initial value for all delay elements is set to 0 except the last element for which it is set to 1.

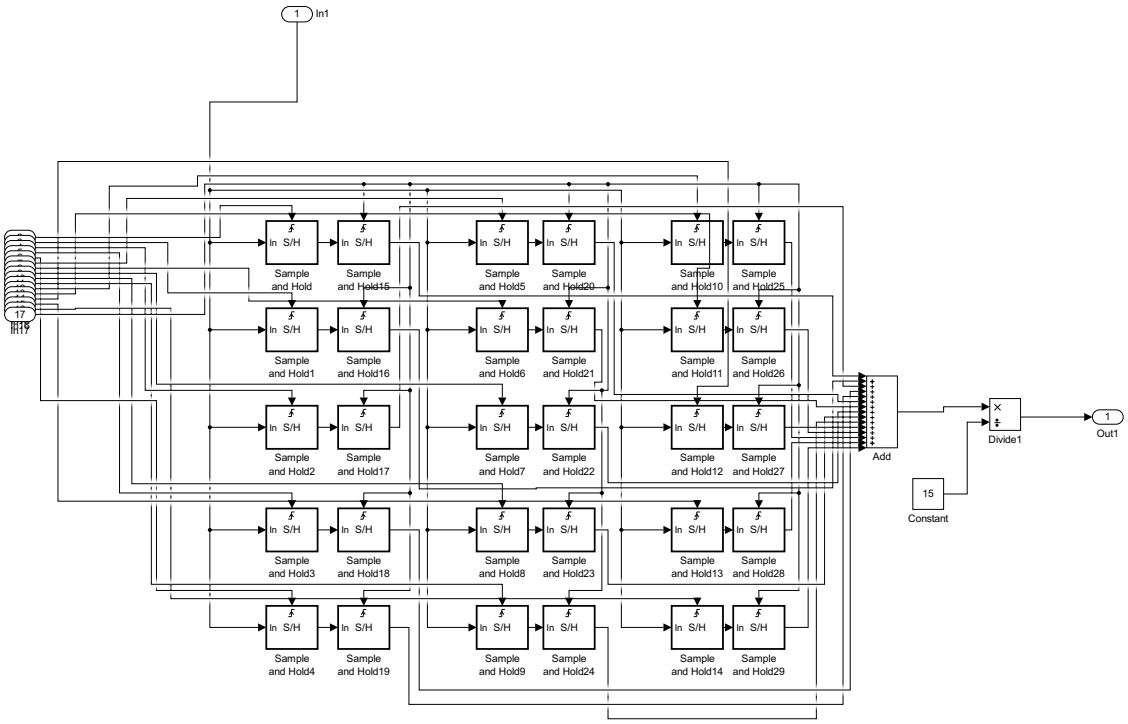

Figure C.6. Schematic diagram of the sampling and averaging block.

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