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# SILICON-GERMANIUM HETEROJUNCTION BIPOLAR TRANSISTORS FOR LARGE-SCALE LOW-POWER CRYOGENIC SENSING SYSTEMS

Shirin Montazeri

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**SILICON-GERMANIUM HETEROJUNCTION BIPOLAR  
TRANSISTORS FOR LARGE-SCALE LOW-POWER  
CRYOGENIC SENSING SYSTEMS**

A Dissertation Presented

by

SHIRIN MONTAZERI

Submitted to the Graduate School of the  
University of Massachusetts Amherst in partial fulfillment  
of the requirements for the degree of

DOCTOR OF PHILOSOPHY

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Electrical and Computer Engineering

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## DEDICATION

*To my inspiring parents, Nasrin and Mohammadreza, for their love, support, and encouragement throughout my life and to my sister and brother, Zarin and Amirhossein, for always being there for me. And to my colleague, best friend, and my husband, Mohammad, who has supported me wholeheartedly throughout this journey.*

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## ABSTRACT

# SILICON-GERMANIUM HETEROJUNCTION BIPOLAR TRANSISTORS FOR LARGE-SCALE LOW-POWER CRYOGENIC SENSING SYSTEMS

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Cryogenic low noise amplifiers (LNAs) are one of the key components in many emerging applications such as radio astronomy or quantum computing in which a weak incoming signal needs to be read out. There have been extensive studies on the feasibility of leveraging silicon-germanium (SiGe) heterojunction bipolar transistors (HBTs) to implement cryogenic LNAs in the past.

The deployment of such LNAs in the future large-scale systems in radio astronomy or quantum computing is contingent upon the possibility of developing LNAs with reduced DC power dissipation to enable the cooling of a large number of array elements inside a cryogenic cooler. In this dissertation, we focus on the cryogenic operation of SiGe HBTs at reduced supply voltages for the implementation of ultra-low-power LNAs and their applications for scalable receiver systems. In addition,

the limitations of the SiGe HBT cryogenic models for the operation at high current densities are investigated. This dissertation is divided into three main sections:

1. **SiGe HBTs at Low Supply Voltages:** The fundamental principals of the operation of SiGe HBTs and their noise performance at cryogenic temperatures are described and the underlying limitations on the low-power operation of these devices are investigated. A theoretical explanation for the operation at low supply voltages is explored and a cryogenic device model is developed based on measurements at a wide range of bias points and temperatures.
2. **SiGe HBT Models at High Current Densities:** The SiGe HBT small-signal and noise models are studied at high injection. The objective is to define the limitations of the models in predicting the noise and small signal performance of a device operating at high current densities. A systematic approach is proposed to implement and study several cryogenic monolithic microwave integrated circuit (MMIC) SiGe low noise amplifiers (LNAs) operating at a wide range of current densities.
3. **Applications:** Several applications of SiGe HBTs operating at low supply voltages are discussed in this section. The design, implementation, and experimental results of ultra low-power MMICs as well as discrete transistor cryogenic LNAs are described as verification of the theory and models developed in the first part of this dissertation. The low-power amplifiers were incorporated into a superconductor-insulator-superconductor (SIS) heterodyne receiver system for THz astronomy applications and results are presented in this dissertation.



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# CHAPTER 1

## BACKGROUND MATERIAL AND MOTIVATION

This dissertation is focused on determining the fundamental limits on the cryogenic operation of silicon-germanium (SiGe) heterojunction bipolar transistors (HBTs) and their applications in highly-scaled cryogenic sensing systems. The dissertation is divided into three main sections:

1. **Operation of SiGe HBTs at Low Supply Voltages** (Chapters 3-6): The fundamental principals of the operation of SiGe HBTs and their noise performance at cryogenic temperatures are described and the underlying limitations of the low-power operation of these devices are investigated. A theoretical explanation for the operation at low supply voltages is explored and a cryogenic device model is developed based on measurements at a wide range of bias points and temperatures.
2. **SiGe HBT Models at High Current Densities** (Chapters 7): SiGe HBT models at high current densities are studied. The objective is to define the limitations of the models in predicting the noise and small signal performance of a device operating at high current densities. In this section, a systematic approach is proposed to implement and study several cryogenic monolithic microwave integrated circuit (MMIC) SiGe low noise amplifiers (LNAs) operating at a wide range of current densities.
3. **Applications** (Chapters 8-9): Several applications of SiGe HBTs operating at low supply voltages are discussed in this section. The design, implementation,



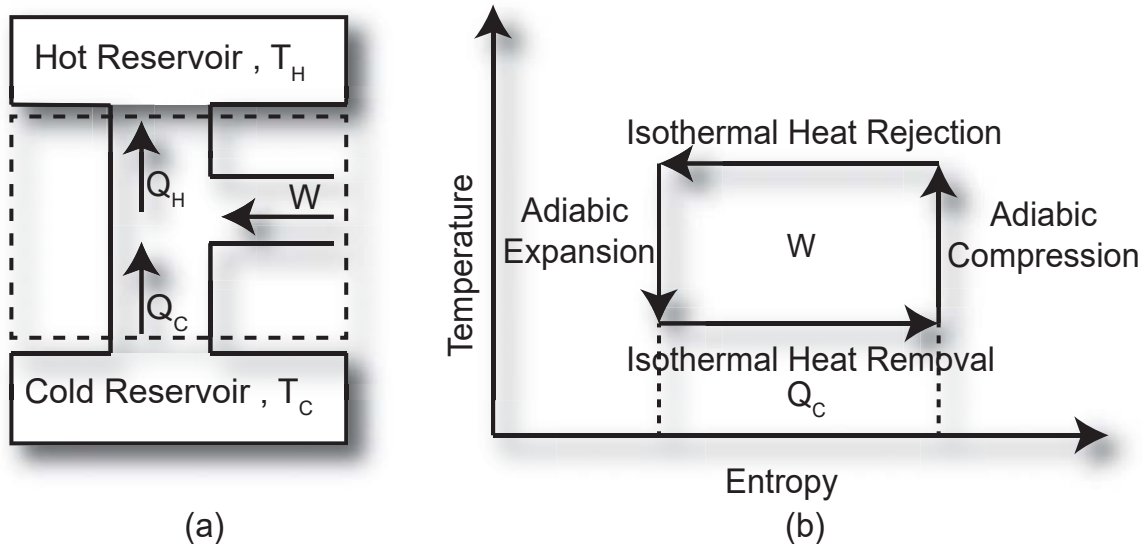
and experimental results of ultra low-power MMICs as well as discrete transistor cryogenic LNAs are described as a verification of the theory and models developed in the first section of this dissertation. The low-power amplifiers were incorporated into a superconductor-insulator-superconductor (SIS) heterodyne receiver system for THz astronomy applications and results are presented in this section.

Background materials and the need for the implementation of extremely low-power LNAs for scalable cryogenic systems are explained in the rest of this chapter.

## 1.1 Motivation

Ultra-sensitive cryogenically cooled experimental systems operate with sensitivities close to the limits of fundamental physics. Cryogenic microwave low noise amplifiers (LNAs) are one of the enabling components in such highly-accurate systems. Recently, there have been a number of emerging applications in which the power consumption of available cryogenic LNAs constrains the scalability of these systems. In particular, ultra low-power cryogenic low noise amplifiers are required to enable the implementation of large-scale heterodyne receivers for THz astronomy applications using large arrays of superconductor-insulator-superconductor (SIS) or hot-electron bolometer (HEB) mixers followed by arrays of LNAs in a single cryocooler [1–4]. In addition, microwave quantum computing could also benefit from the power-constraints LNAs in order to implement large-scale readout sensors in a single cooler [5, 6].

The rate of collecting data in these sensitive systems relies upon the capability of scaling cryogenic electronics to a large number of pixels in a single cryogenic cooler. However, the power handling requirement of a compact integrated array in a single cooler proves to be an issue in achieving the desired large-scale integration. Developing extremely low-power electronics can address this issue and significantly improve the scalability of such instrumentation.



**Figure 1.1.** (a) Carnot refrigeration cycle. (b) Temperature-Entropy plot for the Carnot refrigeration cycle. Figure after [7]

To better understand the trade-off between the scalability of such systems and the power dissipation of cryogenic electronics, first, we briefly review the limited heat lifting capability of available cryocoolers in this chapter. Next, we describe the need for LNAs with reduced power consumption for large-scale terahertz telescopes as well as quantum computing applications.

## 1.2 Heat Capacity of Cryostats and Demand for Low-Power LNAs

Cryocoolers are commonly used to reduce the temperature of electronic circuits much lower than room temperature. This would enable ultra-sensitive measurements that are required for quantum computers, terahertz receivers, medical instruments, and many experiments in physics [8]. In an ideal scenario, the refrigeration process of a closed-cycle system can be described and characterized based on the Carnot principal which explains a theoretical thermodynamic cycle [7–10]. As shown in

Fig.1.1(a), to extract a given amount of heat ( $Q_C$ ) from the cold environment and transport it to the hot environment, a certain amount of work (W) is needed. This minimum required work corresponds to the area contained between the isothermal and adiabatic transformation in a Carnot cycle as shown in Fig.1.1(b) [7–10].

The performance of an ideal refrigerator could be quantified using the coefficient of performance (COP) formula for a Carnot cycle in an steady state operation mode as [7, 9, 10]

$$COP_{Carnot} = \frac{T_C}{T_H - T_C}, \quad (1.1)$$

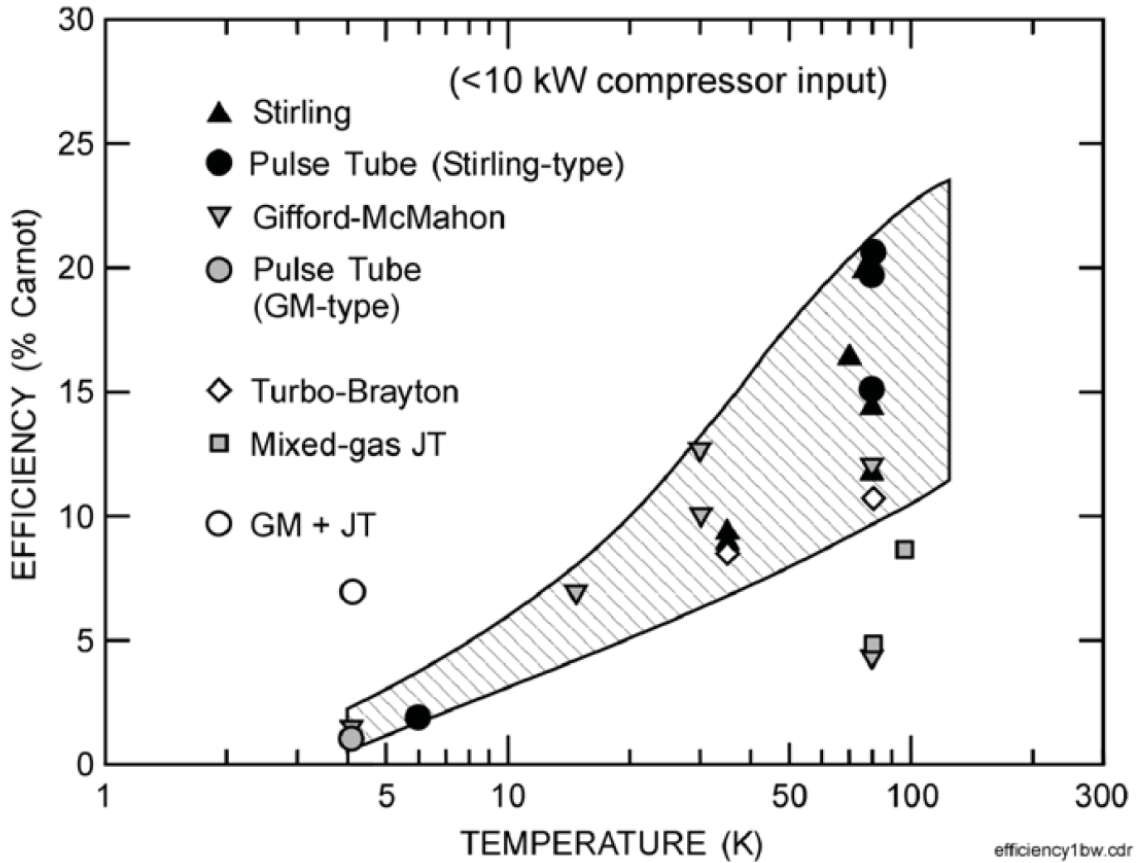
where  $T_C$  and  $T_H$  are the temperature of the cold and hot reservoirs in the Carnot system, respectively. The COP of any system operating between two temperatures of  $T_C$  and  $T_H$  cannot exceed that of an ideal Carnot cycle.

An ideal Carnot refrigerator cannot be practically realized with available cryogenic refrigerators. The efficiency of a practical refrigerator can be written as a function of the  $COP_{Carnot}$  as [7, 9, 10]

$$\eta = \frac{COP}{COP_{Carnot}}. \quad (1.2)$$

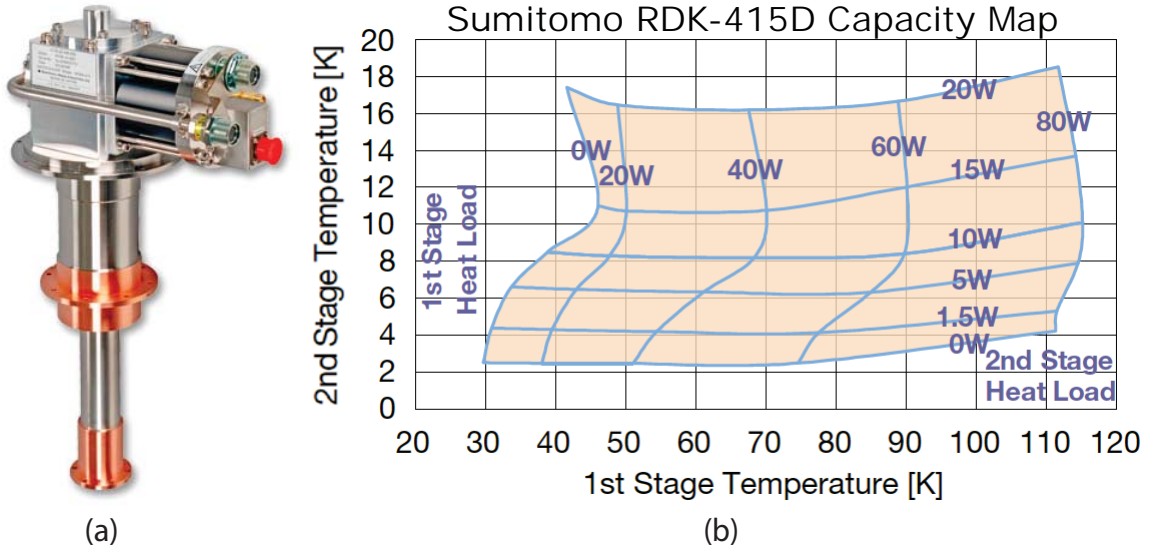
Fig.1.2 presents the efficiency of different types of cryocoolers as a function of the cold end temperature which shows a significant efficiency degradation with cooling [11].

The current state-of-the-art cryocoolers that reach to 4 K have the heat lift capacity of approximately 1.5 W as shown in Fig.1.3 [12]. Assuming that half of the heat lift capacity of the cooler is spent for the cooling of the window, wires, cables, and interconnects inside the cryostat, approximately 750 mW of the power can be dissipated by the electronic circuits inside the cooler. When implementing an array of cryogenic sensors, the heat lift capacity puts a limit on the number of pixels that can fit inside a cooler while maintaining the proper operating temperature. Assuming that 750 mW is mainly dissipated by the low noise amplifiers, the number of LNAs inside a cooler is calculated to be  $750 \text{ mW}/P_{DC,LNA}$ , in which  $P_{DC,LNA}$  is the DC power of each amplifier.



**Figure 1.2.** Efficiency of small cryocoolers as a function of the cold end temperature. Figure reproduced from [11].

One approach to increase the heat lifting capacity of a cryocooler could be the integration of multiple coolers inside a single fridge. However, the limited efficiency of the cryocoolers at 4 K (See Fig.1.2) makes it impractical to integrate many coolers due to the significant increase in the electrical power and cooling equipment. Thus, for a practical large-scale integration of cryogenic systems, microwatt level LNAs are desired to enable larger information capacity.

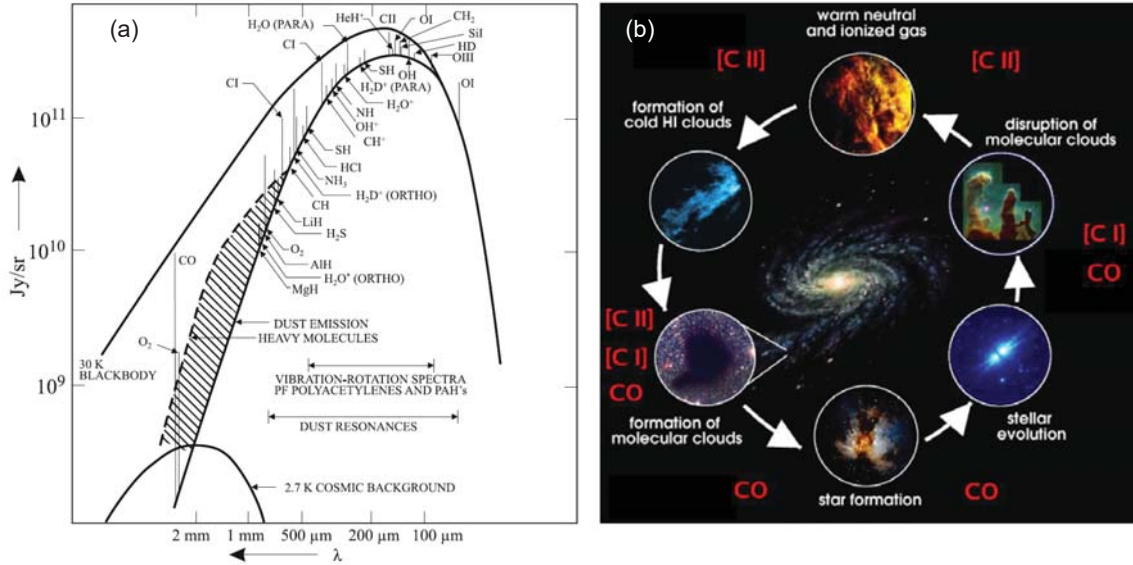


**Figure 1.3.** (a) RDK-415D. (b) Sumitomo RDK-415D Capacity Map. Figure reproduced from [12].

### 1.3 Need for Highly-Scalable Receivers in Terahertz Astronomy

The terahertz region of the electromagnetic spectrum ranges from 0.3 to 10 THz. Historically speaking, astronomers were some of the first scientists who started working on the terahertz detection as it could provide them with valuable information about the fundamentals of the universe, such as the formation of stars and galaxies, the evolution of the interstellar medium, the physics of the Big Bang, the origin of the dark matter and dark energy, and many more similar questions [13–15]. These phenomena could be better understood by using sub-millimeter-wave heterodyne instrumentation which enables the detection of the unique spectral content of interstellar molecules and atoms at terahertz frequencies.

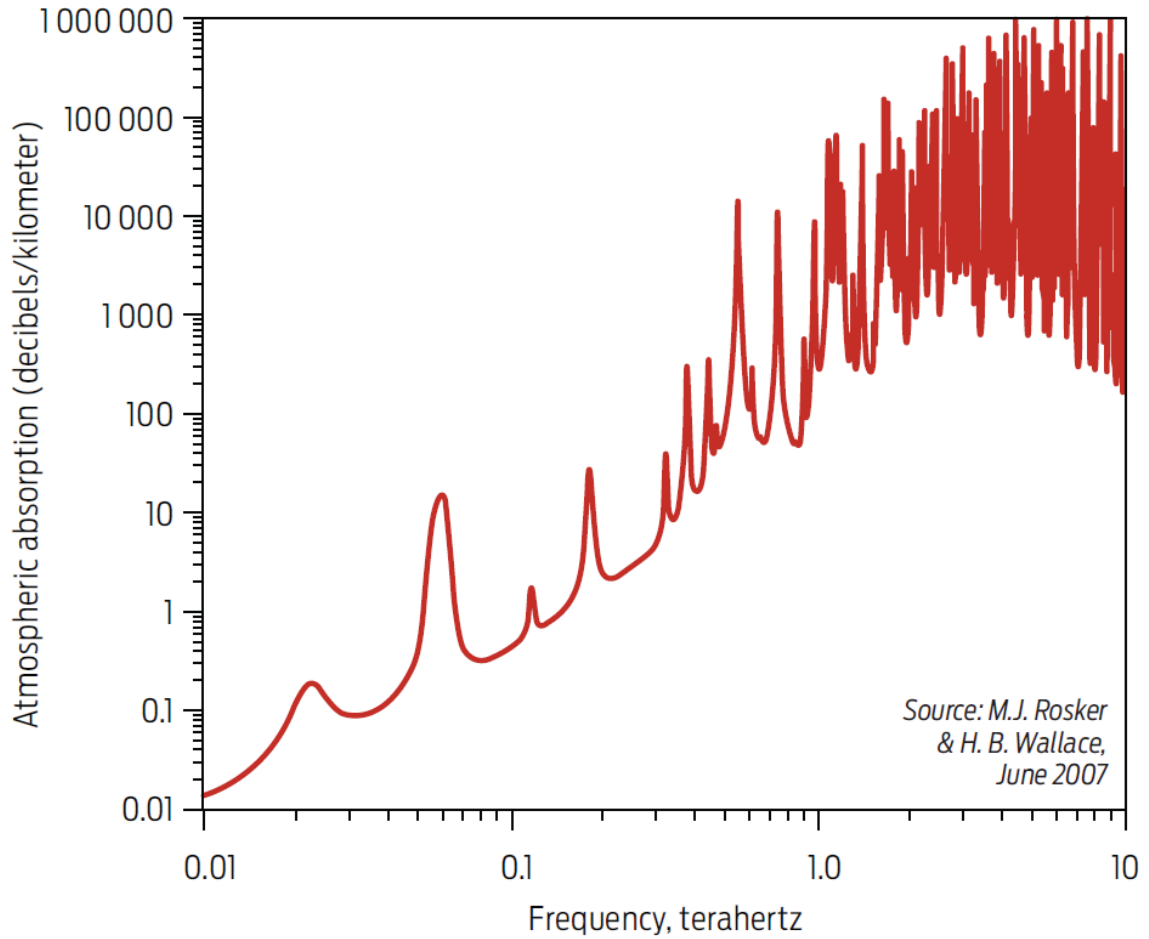
It is believed that approximately 50% of the luminosity of the universe and 98% of all the photons emitted since the Big Bang exist in the terahertz frequency range [16]. Accessing this radiation would provide scientists with information about the properties of the universe [16]. Fig.1.4(a) presents the radiation spectrum of



**Figure 1.4.** (a) Radiation spectrum of a 30K blackbody, interstellar dust and key molecular line emissions in the THz range. Figure reproduced from [17], ©1992 IEEE. (b) Life cycle of the interstellar medium. Figure reproduced from [18].

a 30 K black-body as well as the interstellar medium and the 2.7 K cosmic microwave background [17], showing key molecular line emissions in the terahertz range which correspond to different phases of the interstellar life cycle (See Fig.1.4(b)). Terahertz spectroscopy is commonly used for spectral characterization of the rotational and vibrational resonances and the detection of thermal emission lines of these molecules [14]. Besides the interstellar thermal emission, the optical radiations from the distant galaxies are also red-shifted to terahertz band. Analyzing these signals could reveal additional information about the early universe.

For a long period of time, ground-based terahertz astronomy was considered very challenging, if not impossible, due to the severe atmospheric absorption [19]. Fig.1.5 shows the atmospheric attenuation as a function of frequency which is primarily due to the water vapor and oxygen in the air [20]. Due to this challenge, there has been a great effort put into the development of airborne and space-based telescopes. However, ground-based telescopes have several advantages over the two other types.



**Figure 1.5.** Atmosphere attenuation due to the water vapor and oxygen in the air. Figure reproduced from [20], ©2007 IEEE

They can be made much larger than the size that is feasible for the space or airborne applications. Ground-based telescopes are usually less expensive and they are easier to service in comparison to satellites. In addition, they can provide more observing time in comparison to observation from an aircraft [19]. Consequently, the improvement of ground-based telescopes is of great interest to astronomers.

The detection at terahertz frequencies is commonly accomplished using coherent detectors based on the heterodyne scheme which preserves the amplitude and phase of the incoming signal for a high resolution detection. As shown in Fig.1.6, the RF

input signal is down-converted to an intermediate frequency using a mixer and then is amplified using a low noise amplifier.

The noise temperature of several different types of mixers operating in the terahertz range are shown in Fig.1.7. SIS mixers yield the best noise performance for frequencies below 2 THz which makes them a very attractive choice for receivers operating in this frequency range [21].

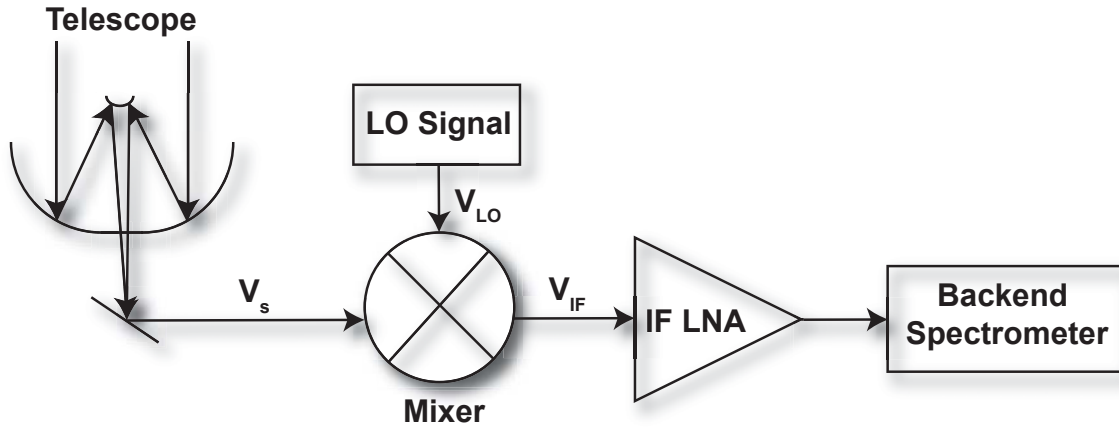
The energy of a photon is directly proportional to the frequency and can be calculated as  $E = hf$ , where  $h$  is the plank's constant and  $f$  is the frequency. The photon energy associated with terahertz radiation is lower than the optical photons which makes their detection more challenging.

The sensitivity of a terahertz heterodyne receiver system can be quantified using the radiometer equation. Ignoring gain variations in the system, fluctuations in the noise measurement can be approximately written as

$$\delta T \approx \frac{T_{SYS}}{\sqrt{B \times \tau}}, \quad (1.3)$$

where  $T_{SYS}$  is the system noise temperature including both the receiver noise and the sky noise temperature,  $B$  is the system bandwidth, and  $\tau$  is the integration time. For ground-based terahertz telescopes,  $T_{SYS}$  is usually dominated by the sky noise due to the severe atmospheric attenuation. Therefore, in order to increase the receiver sensitivity for a given spectral resolution, much larger integration time is required. However, the beam-width of an antenna at terahertz frequencies is much narrower than that of a same-size antenna operating at millimeter or radio waves. Consequently, the narrow beamwidth at terahertz frequencies in tandem with the long dwell time required for a given spectral resolution, make it impractical to carry out a large-scale survey of the sky. To overcome this issue, heterodyne receivers containing several pixels operating in parallel are required. This would increase the throughput of such systems to enable a high-resolution large-scale survey of the sky.





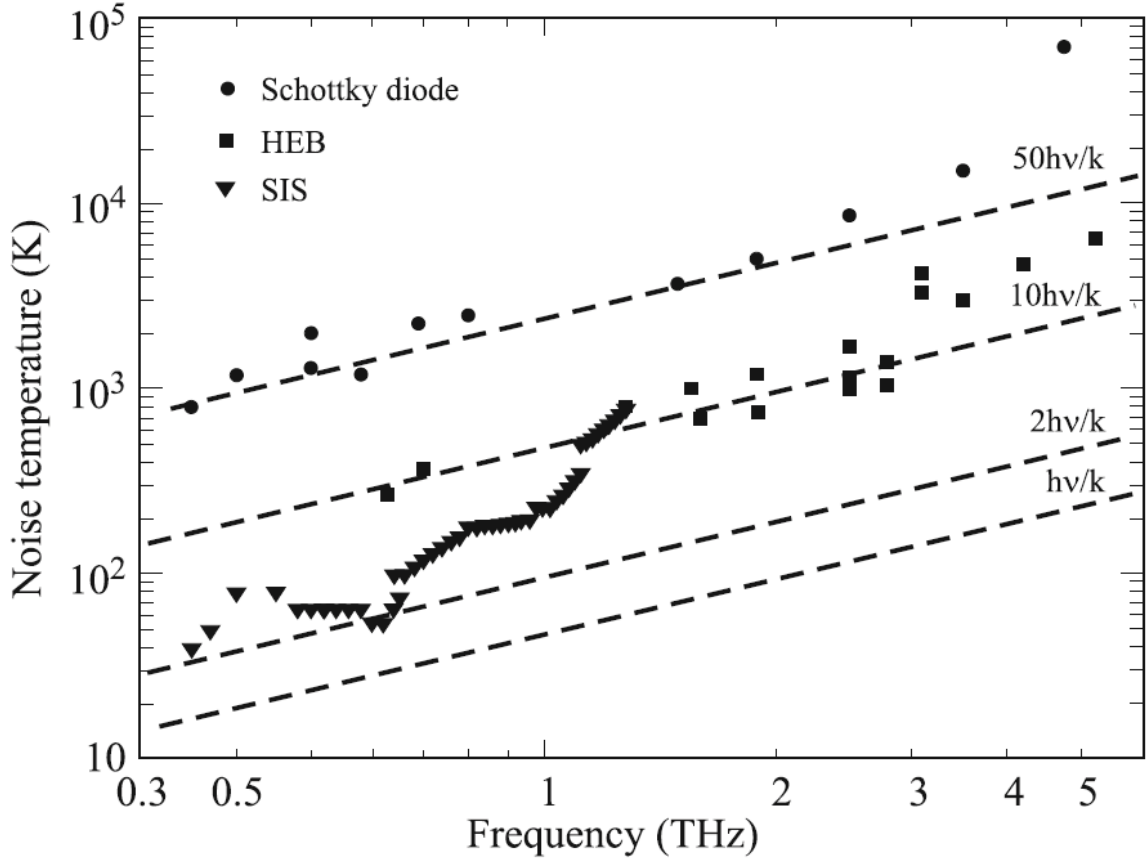
**Figure 1.6.** A block diagram of a standard heterodyne spectrometer.

The current state-of-the-art focal plane array (FPA) is SuperCam containing 64 pixels operating at 350 GHz [1]. It has been reported that the SuperCam can accomplish surveys in one month that would take approximately six years using a single pixel receiver [18]. Fig.1.8 shows a photo of the beam footprints on a galactic object (Horsehead Nebula) at 345 GHz for the 64-pixel SuperCam [22]. The reported angular resolution of the SuperCam is 0.38 arcminute<sup>1</sup>. With 64 pixels operating in parallel, SuperCam can cover approximately 25 square arcminutes in the sky. The number of square arcminutes in a complete sphere, like the sky, is calculated to be 148 million. Thus, the 64-pixel SuperCam is able to cover a very small fraction of the whole sky ( $3.4 \times 10^{-5}$  percent of the sky hemisphere). Consequently, kilo-pixel heterodyne focal plane arrays are desired to enable practical wide-ranging imaging of the celestial objects in the sky in a reasonable amount of time, which would be used to study the evolution of the cosmos, molecular clouds, the origin of dark matter and dark energy, and many other fundamental questions about the universe [2, 23, 24].

The number of elements in an array determines the information capability of the system and the speed improvement of a survey of galactic objects. Although the

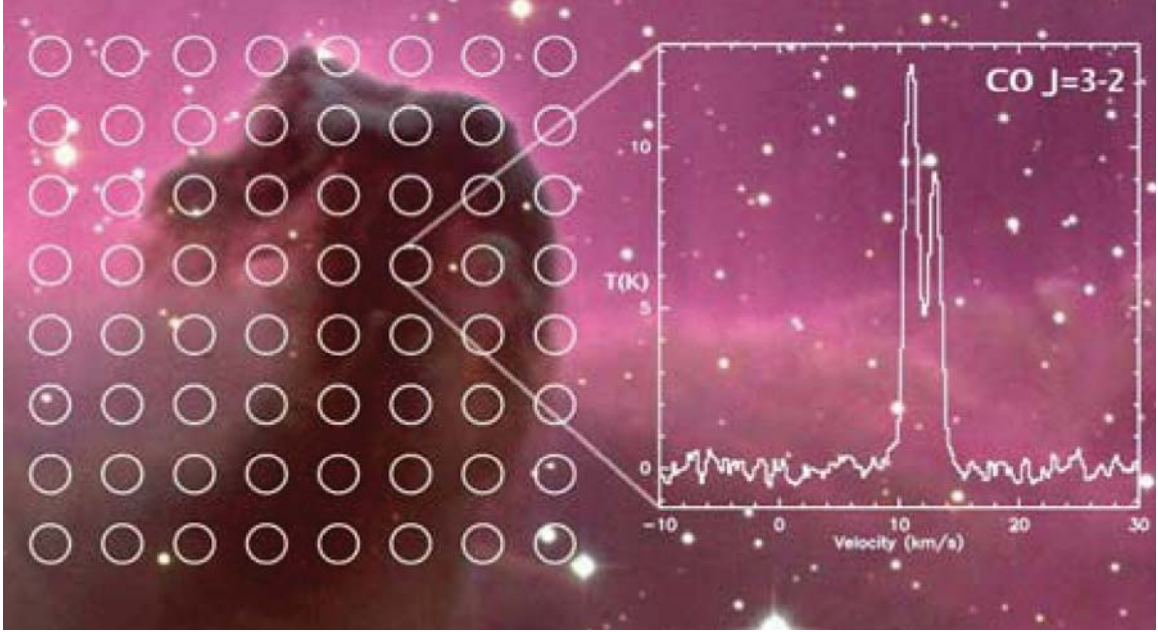
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<sup>1</sup>One arcminute is equal to 1/60 of a degree.



**Figure 1.7.** Noise temperature of Schottky diode mixers, SIS mixers and HEB mixers operating in the terahertz spectral band [21] ©2008 IEEE.

scientific impact of developing such large-scale terahertz heterodyne FPAs are expected to be significant, they have been slow to develop due to various mechanical and thermal challenges associated with their implementation [2]. The finite heat lifting capacity of available cryocoolers (described in Section 1.2) is one of the limiting factors in achieving the desired large-scale integration. The power handling requirement of coolers creates a high demand for low-power electronics which would enable the implementation of practical large-scale cryogenic FPAs inside a single cooler.

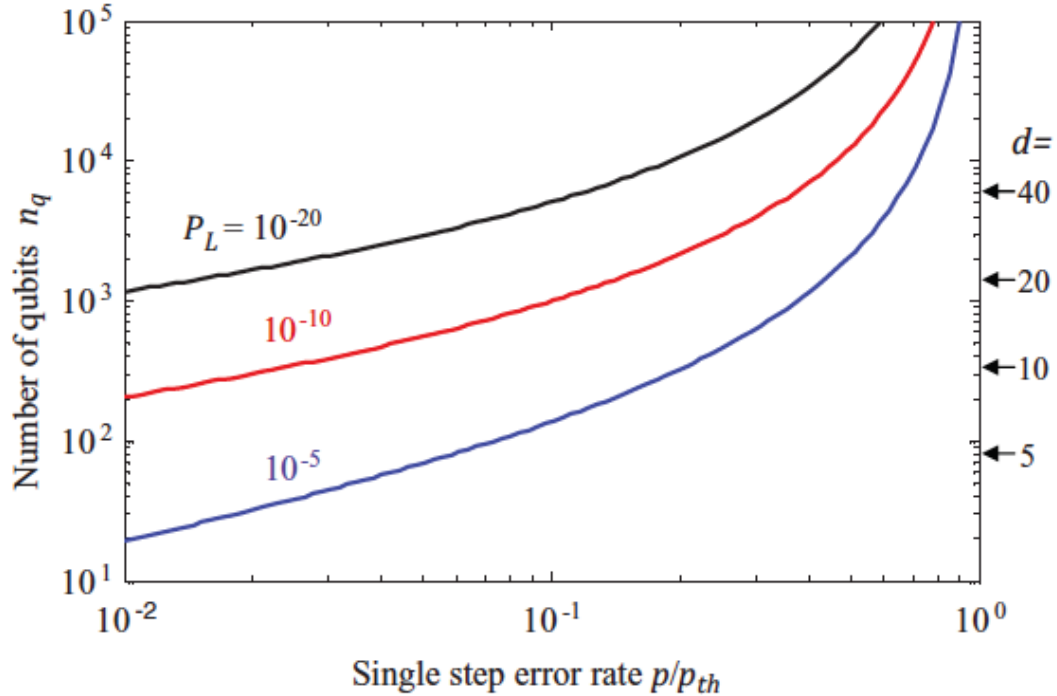


**Figure 1.8.** Beam footprint of the 64-pixel SuperCam operating at 345 GHz on the Horsehead Nebula. Each beam measures a high resolution spectrum. A small portion (15%) of the beam footprint is shown at right. Figure reproduced from [22].

## 1.4 Cryogenic LNAs for Quantum Computing

Quantum computers can solve certain problems that cannot be solved using conventional classic computers in a reasonable amount of time such as factoring very large numbers which could be used in cryptosystems using Shors algorithm [25, 26], searching large-unstructured data sets which can be done using Grovers search algorithm [27, 28], quantum simulation [29], machine learning, and several other applications.

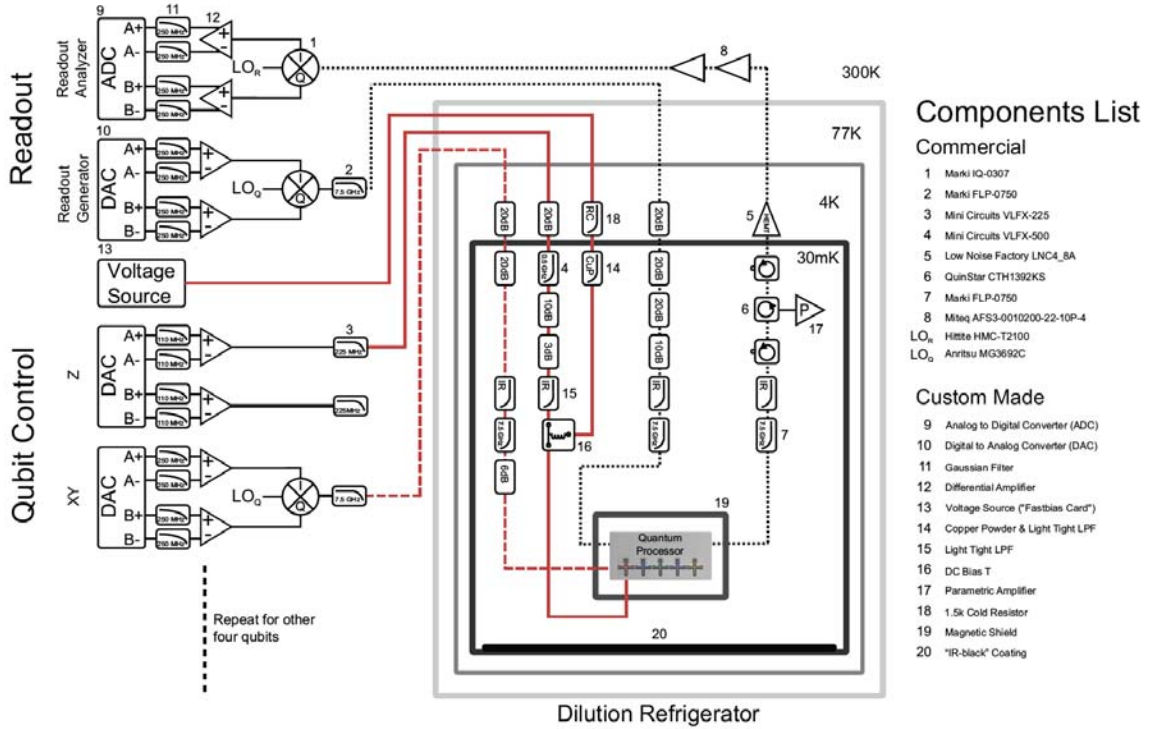
Quantum computers make use of quantum bits to store information. Quantum bits (commonly referred as qubits) store a linear superposition of both '0' and '1' states using the principles of quantum mechanics. Physical qubits have limited fidelity and several qubits are required to protect a single qubit against general errors [30–35]. Quantum computation is made possible by the theory of the fault-tolerant computation which in principle could be described as protecting the qubits from errors



**Figure 1.9.** Estimated number of physical qubits per logical qubit as a function of the single-step error rate  $p$  which is normalized to the threshold error rate  $p_{th}$ . Different curves correspond to different target logical error rates  $P_L$ . Figure reproduced from [38].

and any noise in the quantum operation as well as the stored information [30–35]. Due to the finite fidelity, quantum error correction (QEC) is required, just like classical error correction, for the data transmission over a noisy channel [30–35]. Before the discovery of QEC methods, quantum computing seemed to be impossible [36,37]. Error corrections are specially important in quantum computers as the large-scale quantum interference in efficient quantum algorithms are very sensitive to the noise in the computer and unwanted coupling from the computer to the outside world [30–35]. This makes the error correction an essential part of the large-scale quantum computers.

There exists a tradeoff between the error tolerance and the number of the physical qubits required for the implementation of a quantum computer [38]. Fig.1.9 shows the number of physical qubits per logical qubit required for three values of logical error



**Figure 1.10.** Qubit control and readout system. Figure reproduced from [39].

rate  $P_L$  [38]. It can be concluded that the number of physical qubits ( $n_q$ ) increases rapidly as the single step error rate ( $p$ ) approaches the threshold error rate ( $p_{th}$ ) [38].

To make quantum error correction a reality, a large number of qubits need to be readout simultaneously using large-scale readout arrays which includes many low noise amplifiers in a single cryocooler. An example qubit control and readout system is shown in Fig.1.10 [39]. The system consists of quantum limited parametric amplifiers followed by cryogenic LNAs to provide extremely sensitive S-parameter measurements [39]. To readout a large number of physical qubits for error correction, arrays of ultra-low-power consumption cryogenic semiconductor LNAs are required to make the implementation of future large-scale quantum computers feasible.

## 1.5 Status of Solid-State Cryogenic Low Noise Amplifiers

Radio astronomy was one of the fields which pioneered the demand for cryogenic low noise amplification. Cosmic signals coming towards the earth are buried under the noise floor of most room temperature receiver systems. The cooling of electronic circuits is a common approach to increase the sensitivity of such receivers enabling the detection of weak cosmic signals.

From the early 1980s, the majority of cryogenic low noise amplifiers were built around the Gallium-Arsenide field effect transistors (GaAs FETs) with remarkable noise performance [40–42]. However, there exist some fundamental issues with the GaAs FETs. It is known that the performance of these devices is ultimately limited due to the limited mobility of the carriers in a doped GaAs FET channel [43].

High electron mobility transistors (HEMTs) started emerging as an alternative to implement cryogenically cooled amplifiers. A two-dimensional electron gas in the undoped semiconductor of a HEMT device results in a very high mobility and made it an attractive choice for the next generation of cryogenic amplifiers [43]. In early 1980s, the first results of a HEMT device was reported as a function of temperature by a group from the Fujitsu Lab [44]. The results confirmed the improvement in the noise and gain of the device with cooling. Two years later, through a collaboration between NRAO, GE, and JPL, the cryogenic performance of a quarter micron HEMT technology was reported for frequencies between 3 to 23 GHz with a noise temperature in the range of 3.5 to 27.5 K [45]. The work continued and three years later a noise temperature of less than 2 K was achieved for HEMT devices operating at low frequencies [46]. Despite the promising results achieved leveraging the HEMT technology at cryogenic temperatures, there are several limiting aspects associated with the HEMTs. These devices mostly have a high optimum impedance, high power consumption, flicker noise, gain fluctuations due to surface traps, and their incom-

patibility with commercially available CMOS technologies for the implementation of large system on chips (SoC) [47].

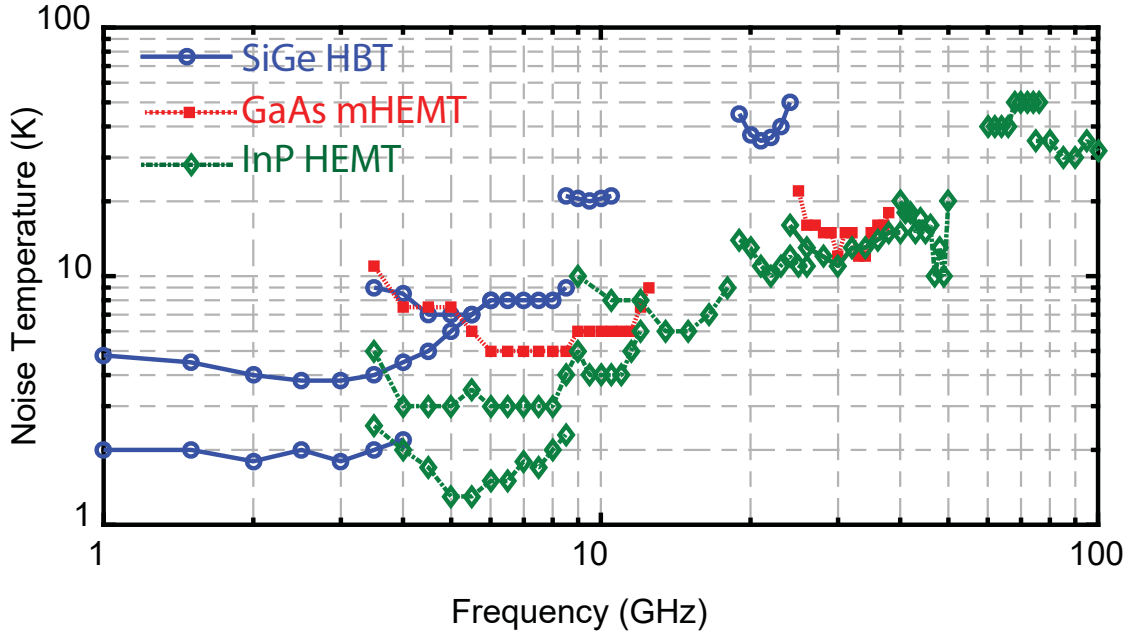
Recently, silicon-germanium (SiGe) heterojunction bipolar transistors (HBTs) emerged as an alternative device for cryogenic amplifiers. The idea of heterojunction transistors was initially introduced by Kroemer [48] in 1957, and the first example of a working SiGe HBT device was reported in 1987 [49]. SiGe HBT technology has developed fairly quickly in a BiCMOS technology platform that provides a very high yield and makes it an attractive option for the implementation of large scale systems.

The possibility of operating such devices at cryogenic temperatures was first investigated in early 1990s [50, 51] and the work continued on the next generations of SiGe HBT devices [52–54]. The first SiGe based cryogenic LNA was designed and implemented in 2007 [55]. Following that, a more detailed study of the small signal and noise performance of SiGe HBT devices at cryogenic temperatures was carried out for devices from different foundries and results were published in 2009 [56]. The promising results reported in [56] prove the feasibility of using commercial SiGe HBTs for the implementation of cryogenic low noise amplifiers.

Fig.1.11 summarizes the noise performance of several state-of-the-art cryogenic LNAs in different technology processes which shows that SiGe HBTs offer a competitive noise performance at frequencies below 10 GHz. However, at high frequencies, the HEMT LNAs present a better noise performance due to the high  $f_{max}$  of InP HEMT and GaAs mHEMT devices.

Currently, the promising performance of SiGe LNAs at cryogenic temperatures at the intermediate frequencies has made them an extremely attractive option for cryogenic applications due to their high yield and compatibility with the commercial CMOS technology platform for large scale SoCs. However, very limited results have been reported in the literature so far on the operation of SiGe HBTs at low DC power dissipation.





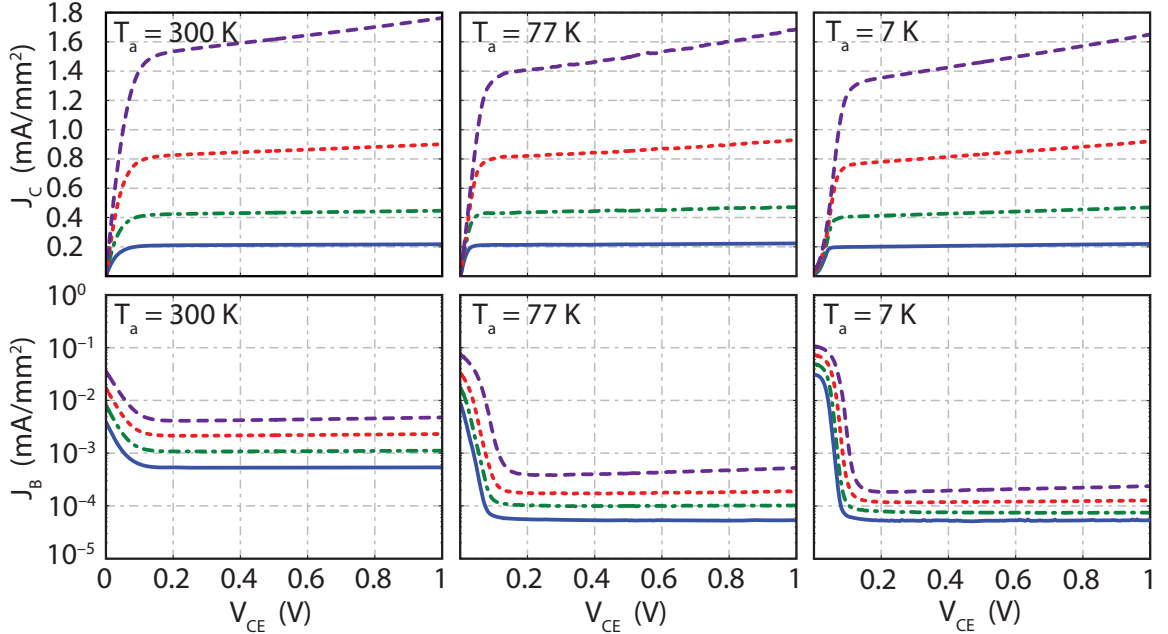
**Figure 1.11.** Noise performance of state-of-the-art cryogenic LNAs. Data was taken from [56–69].

In this work, a detailed study of the fundamental limits on the operation of SiGe HBTs at low supply voltages for low-power purposes was carried out and results were published in [70]. Leveraging those result, several ultra-low-power cryogenic LNAs were implemented and characterized at cryogenic temperatures [67, 68]. Later, ultra-low-power LNAs were designed and incorporated into a superconductor based heterodyne receivers for THz astronomy applications [71–73].

## 1.6 Open Issues

Currently, LNAs employing InP high electron mobility transistors (HEMTs) with more than 4 mW DC power dissipation are typically used for cryogenic applications [56, 66, 74–77]. This relatively high power consumption makes it impractical to implement scalable cryogenic sensors in a single cooler due to the limited capability of the commercially available cryogenic refrigerators as described in Section 1.2.





**Figure 1.12.** Measurement results of the base and collector current densities as a function of collector to emitter voltage for a GF BiCMOS8HP SiGe HBT device. Different curves represent currents at different base-emitter bias voltages [70], ©2016 IEEE.

Practical scalable FPAs require LNAs with sub-milliwatt power dissipation to meet the heat lifting limitations of the cryocooler containing hundreds or thousands of terahertz heterodyne receiver elements. This would be approximately a ten times improvement in the power consumption over the current state-of-the-art commercially available InP HEMT cryogenic LNAs. Despite the great demand for low-power amplifiers in most cryogenic instrumentation, there was very limited work done on the power constrained cryogenic LNAs in the past. In this work, we investigate the possibility of developing microwatt level SiGe HBT LNAs for cryogenic applications.

SiGe HBTs are targeted in this research due to their promising potential for low-power operations. These devices demonstrate a favorable performance at a wide range of supply voltages. Fig.1.12 shows DC I–V curves of a SiGe HBT at three different temperatures as a function of the supply voltage. The measurement results present an ideal DC performance for voltages as low as 200 mV.

Typically, there exists a strong trade-off between the power consumption and the overall performance of a low noise amplifier. Consequently, the implementation of ultra-low-power SiGe amplifiers requires two main questions to be answered:

- What is the lowest supply voltage at which a SiGe HBT can operate under cryogenic conditions?
- What happens to the noise and small signal performance of a device when operating at low supply voltages?

The first goal of this research is to determine and achieve the fundamental limits on the low power operation of the silicon based integrated circuitry. The objective is focused on modeling and fully characterizing SiGe HBTs at a wide range of bias points at cryogenic and room temperatures and using the models to design and demonstrate broadband ultra-low-power (ULP) LNAs for microwave applications.

Leveraging the small-signal and noise models, we try to design and implement low-power cryogenic LNAs to be integrated with superconductor mixers for THz astronomy applications. The goal is to demonstrate the feasibility of implementing ultra-low-power heterodyne receivers for the deployment in the future many-pixel THz cameras.

Modern high speed systems require circuits operating at high current densities to achieve a high unity gain cutoff frequency. The final goal of this work is to understand the limitations of the small-signal and noise models at high current densities. The objective is to develop a systematic experiment to study the model limitations for a device operating in the high injection region.

This research aims to address problems pertaining to the theory, development, device modeling and its limitations at low supply voltages as well as high injection region, cryogenic circuit design, and measurement of cryogenic LNAs. It is expected that the resulting models, circuits and systems would significantly impact the ca-

pabilities of future sensitive cryogenic receivers and will be of great interest to the scientists in the field.

## 1.7 Contributions

The major contributions presented in this dissertation are as follows:

- **Device Modeling:** Theory of the SiGe HBT operation at low supply voltages was investigated. Several devices from different technology runs and foundries were measured at different physical temperatures over a wide range of operating points. Small-signal and noise parameters were extracted from the measurements and models were developed. The results of this work were published in the *IEEE Transactions on Microwave Theory and Techniques* [70]. In addition, the prediction of the SiGe HBT model at high current densities were investigated. Several different cryogenic low noise amplifiers were designed and optimized for operation at various current densities and model predictions were compared to cryogenic measurements to investigate model limitations at high current density.
- **Design and Implementation:** Several low noise amplifiers with different bandwidth and noise specifications were designed using the models developed in this work. Proof-of-concept discrete transistor LNAs as well as integrated circuit amplifiers were implemented and results were compared to simulations to verify the models at low supply voltages. The results of a 4-8 GHz MMIC LNA with microwatt level power consumption using the GF BiCMOS8HP technology were accepted to the *2017 International Microwave Symposium (IMS2017)* and was presented in June 2017 [67]. A 2-4 GHz integrated cryogenic LNA using the TowerJazz SCB18H3 technology process was also designed and implemented which provides the lowest noise temperature for a low power LNA. The

result of this work was accepted to the *2018 International Microwave Symposium* (IMS2018) [68] and was presented in June 2018.

- **System Implementation:** An ultra-low power SIS-based heterodyne receiver system was implemented for the first time through a collaborative work with the Harvard Smithsonian Center for Astrophysics (CFA). The ultra-low-power IF low noise amplifier used in the receiver chain was designed, implemented and characterized using discrete SiGe HBTs. The LNA characterization and performance verification were carried out and the complete system assembly, measurements, and characterization at terahertz frequencies were accomplished. The results of this collaborative work were published at the *26th International Symposium on Space and Terahertz Technology* [71], in the *IEEE Transactions on Terahertz Science and Technology* [72], and in the *IEEE Transactions on Applied Superconductivity* [73].

## CHAPTER 2

### A REVIEW OF THE FUNDAMENTALS OF SIGE HBTs

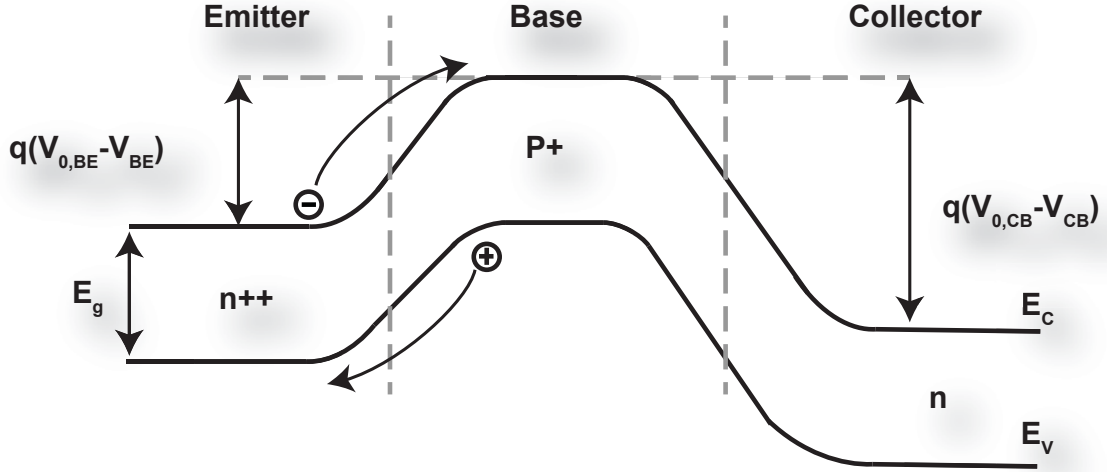
Silicon-germanium (SiGe) heterojunction bipolar transistors (HBTs) have emerged as a technology of choice in several radio-frequency (RF), microwave, and millimeter wave integrated circuits. The possibility of leveraging these devices at extreme environments has been extensively studied in the past [56, 78, 79]. To gain insight into the theory of operation of SiGe HBTs, first, we briefly discuss the properties of these devices in this chapter. We will continue the discussion by looking at the noise sources in a SiGe device and modeling them theoretically. The chapter will be concluded with examining the performance of SiGe HBTs at cryogenic temperatures and the limitations associated with the operation at the high injection region.

#### 2.1 Silicon-Germanium Heterojunction Bipolar Device Physics

In order to understand the fundamentals of SiGe HBTs, first, we look at the basic operating principals of silicon bipolar junction transistors (BJTs) and their fundamental limitations. Next, we will extend the concept to the silicon-germanium heterojunction bipolar transistors (HBTs) and briefly discuss some of the unique features of SiGe HBTs.

##### 2.1.1 Limitations of Si BJTs

In order to gain insight into the BJT operation, we start with the energy band diagram for a standard BJT device as shown in Fig.2.1. The emitter of a BJT device is heavily doped resulting in a large number of electrons in the emitter region which can



**Figure 2.1.** The energy band diagram of a Si BJT device under the forward active operation. Figure after [80].

cross the emitter-base potential barrier when gaining enough energy [80]. Assuming a very narrow base region, the electric field in the base pushes these electrons to the collector region [80]. The DC current gain for a Si BJT can be calculated in a simplified form as [78, 80]

$$B_{DC,BJT} \approx \frac{\mu_{nb} L_{PE} N_{DE}^+}{\mu_{pe} W_B N_{AB}^-}, \quad (2.1)$$

where  $\mu_{nb}$  and  $\mu_{pe}$  are the minority carrier mobilities in the base and emitter regions.  $W_B$  is the width of the base and  $L_{PE}$  is the diffusion length in the emitter. The  $N_{DE}^+$  and  $N_{AB}^-$  are the ionized donor and acceptor concentrations in the emitter, respectively. It can be concluded from Eq.2.1 that the higher the ratio of the doping in the emitter to the base, the better DC current gain that could be achieved from a BJT. However, in a BJT device, this ratio cannot be arbitrary high as the base sheet resistance of a BJT is coupled to the DC current gain through the base doping as shown below [81, 82].

$$R_{B,sheet} = \frac{1}{q\mu_{pb}N_{AB}^-W_B}(\Omega/square) \quad (2.2)$$

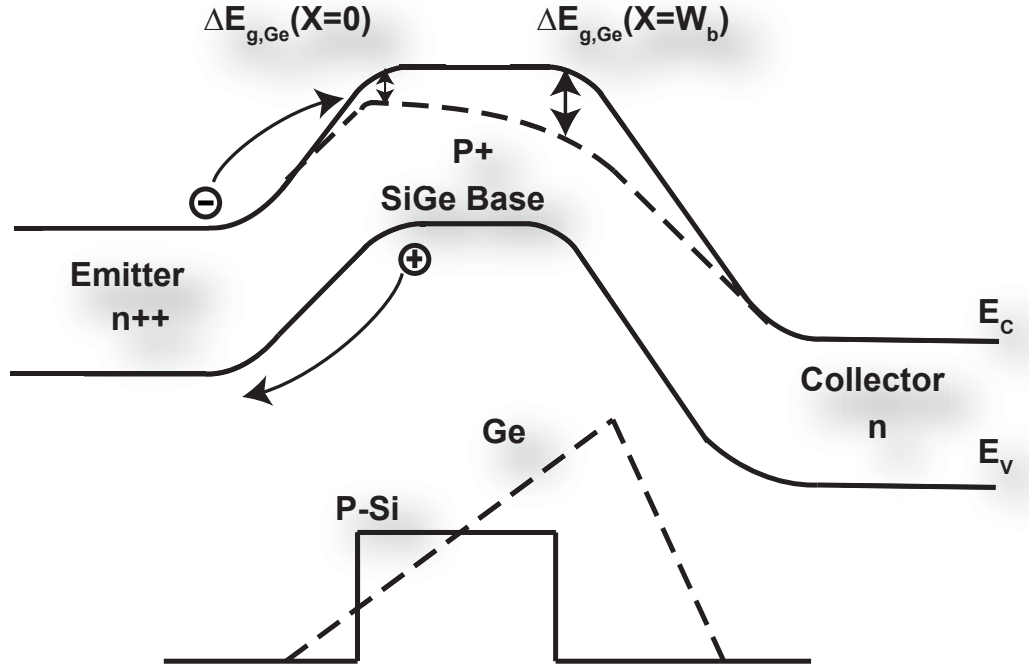
Consequently, there exists a direct trade-off between the base resistance and the DC current gain of a Si BJT device with respect to the doping of the base region as shown in Eq.2.1 and Eq.2.2. This issue has been solved through the band engineering in the heterojunction bipolar transistors which was initially introduced by Kroemer [48] in 1957. The details of the operating principles of the heterojunction transistors are described in the next section.

### 2.1.2 Fundamentals of SiGe HBTs

As discussed in the previous section, the trade-off between the base resistance and the DC current gain of Si BJTs ultimately limits their performance. In 1957, Herbert Kroemer introduced the idea of bandgap engineering and the implementation of heterojunction bipolar transistors to mitigate the tradeoff that existed in Si BJTs [48]. Kroemer showed that if the electrons in the emitter region see a smaller barrier than the holes back injected from the base to the emitter, then, the resulting DC current gain would be exponentially higher than that of a Si BJT [48].

An example band diagram of a typical SiGe HBT along with an example triangular base Ge profile are shown in Fig.2.2. Germanium has a band gap of 0.67 eV which is lower than that of pure Si (1.1 eV). Thus, adding germanium to the base content reduces the bandgap of the alloy compared to the silicon in the base region and lowers the conduction band while maintaining the valence band [78]. Therefore, electrons in the emitter see a smaller potential barrier than the holes back injected to the base which results in a significant improvement in the DC gain of SiGe HBTs compared to that of a Si BJT device [78].

The first working SiGe HBT was implemented in 1987 [83]. SiGe HBT technology has developed rapidly since then and currently there are a large number of companies worldwide providing commercial SiGe HBT technologies processes such as IBM BiC-

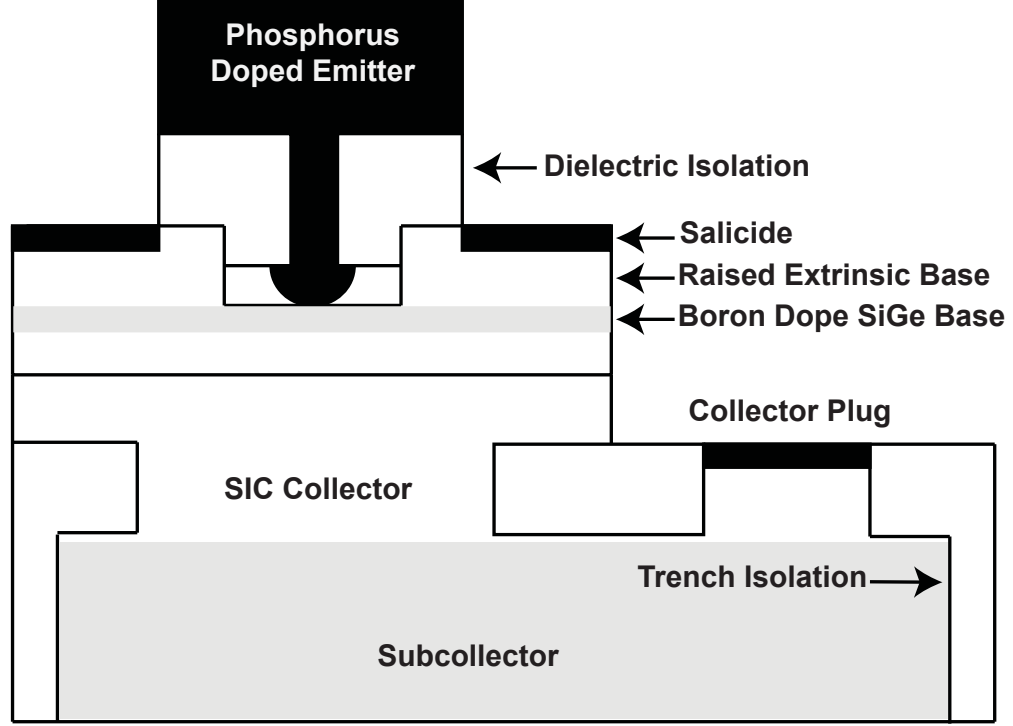


**Figure 2.2.** An example energy band diagram of a graded base SiGe HBT biased at forward active region. Figure reproduced from [79], ©2005 IEEE.

MOS8HP, ST BiCMOS9MW, JAZZ SBC18H3, etc [84–86]. Fig.2.3 shows an example structure of a SiGe HBT device.

Each foundry has their own unique recipe to fabricate a SiGe HBT, however, there are some main common steps in the process which are named in here [78]. The SiGe HBT fabrication starts with the implementation of an  $n^+$  subcollector (which allows the integration of CMOS with SiGe) and a  $p^-$  substrate. Then, a lightly doped  $n$  type collector epi is implemented at high temperatures [78]. Following that, the fabrication of deep trenches, filled with poly silicon, are carried out in order to isolate the subcollector of the device from the adjacent ones. The shallow trench isolations filled with oxide are also deployed for the local isolations between different parts inside the device. The local collector implementation is carried out through the self aligned selectively implanted collector (SIC) [78]. Next step is the fabrication of the composite SiGe epi layer and employing an emitter-base self aligned scheme





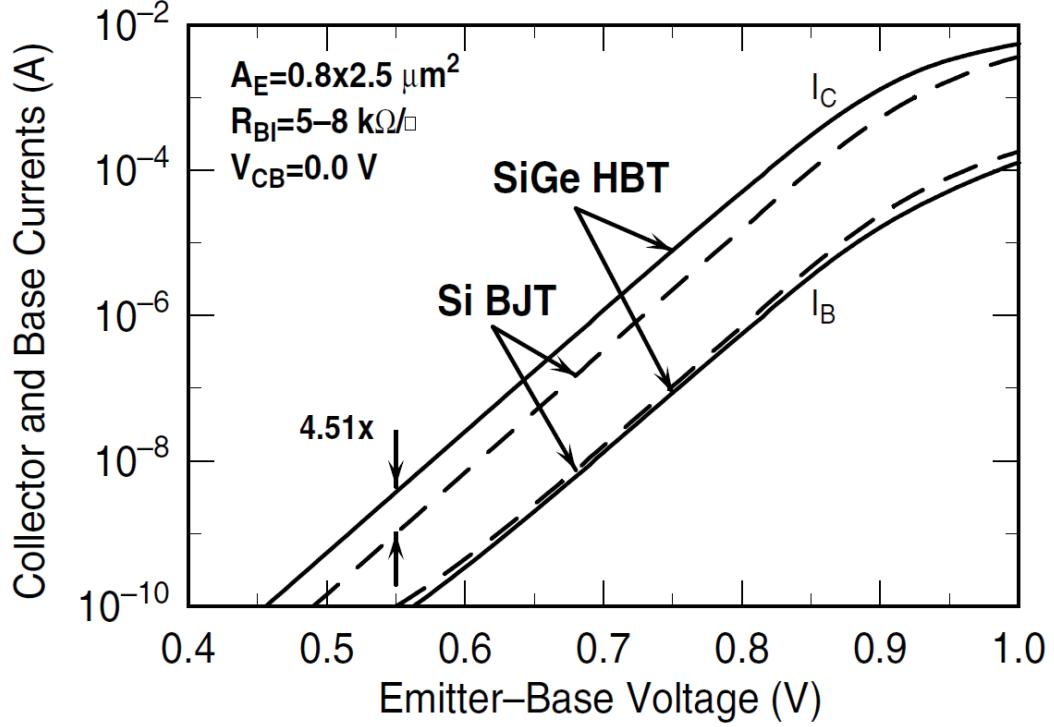
**Figure 2.3.** A schematic diagram of a GF BiCMOS8HP SiGe HBT. Figure reproduced from [87], ©2002 IEEE.

using emitter spacers. The implementation of poly-silicon extrinsic base contacts and a silicided extrinsic base is carried out afterwards. Finally, the fabrication of a heavily doped polysilicon emitter and the deployment of back-end-of-the-line (BEOL) metalization concludes the fabrication process [78].

Now that we have a good understanding of a SiGe HBT structure, let's look at the terminal characteristics of these devices. The collector current density of a SiGe HBT can be written as [56, 78]

$$J_C = \frac{q\mu_{nb,Si}}{N_{AB}^- W_b} (e^{qV_{BE}/kT_a} - 1) n_{io,Si}^2 e^{\Delta E_g^{app}/kT_a} \tilde{\chi} \tilde{\eta} \frac{\Delta E_{g,Ge(grade)}/kT_a e^{\Delta E_{g,Ge(0)}/kT_a}}{1 - e^{-\Delta E_{g,Ge(grade)}/kT_a}}, \quad (2.3)$$

where  $n_{io,Si}$  is the intrinsic carrier concentration in silicon,  $\mu_{nb,Si}$  is the electron mobility, and  $\tilde{\eta} = \frac{\mu_{nb,SiGe}}{\mu_{nb,Si}}$ . The effective density-of-states ratio is defined as  $\tilde{\chi} =$



**Figure 2.4.** Collector and base current of a SiGe HBT in comparison with a Si BJT as a function of  $V_{BE}$  voltage. Figure reproduced from [78].

$\frac{(N_C N_V)_{SiGe}}{(N_C N_V)_{Si}} < 1$  [78, 88], where  $N_C$  and  $N_V$  are the conduction and valence band density of states, respectively. The base current of a SiGe HBT is expected to be similar to that of a Si BJT device. Consequently, the ratio of the DC current gain of a SiGe HBT to a Si BJT can be calculated as [78]

$$\frac{B_{DC,SiGe}}{B_{DC,Si}} \approx \tilde{\chi}\tilde{\eta}\Delta E_{g,Ge(grade)}/kT_a \times \frac{e^{\Delta E_{g,Ge(0)}/kT_a}}{1 - e^{-\Delta E_{g,Ge(grade)}/kT_a}}. \quad (2.4)$$

It can be concluded from Equation.2.4 that the DC current gain improves when incorporating germanium content in the base of a SiGe HBT device. Fig.2.4 shows a comparison between the collector and base current of a SiGe HBT and a Si BJT which confirm the superior DC current gain of SiGe HBTs [79].

In addition to the DC current gain improvement, it is also shown in [89, 90] that incorporating germanium into the base improves the Early effect exponentially as shown in the equation below.

$$V_A \propto \frac{N_{AB}^-}{C_{jc}} \frac{e^{\Delta E_{g,Ge(grade)}/kT_a} - 1}{\Delta E_{g,Ge(grade)}/kT_a}, \quad (2.5)$$

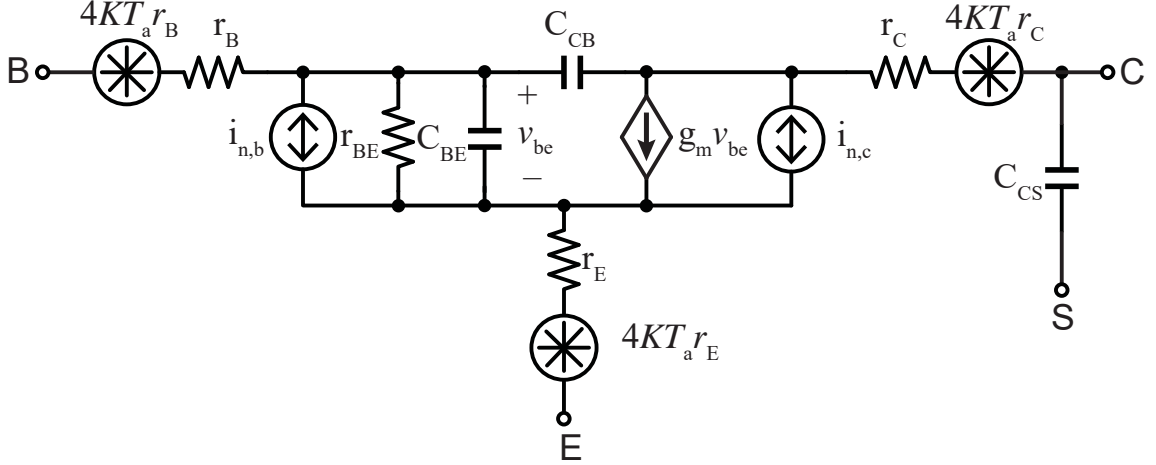
where  $N_{AB}^-$  is the ionized acceptor concentrations in the emitter,  $k$  represents the Boltzman constant,  $T_a$  is the ambient temperature, and  $\Delta E_{g,Ge(grade)}$  is the conduction band offset across the neutral base from the graded profile. The exponential dependence of the Early voltage on the band offset was experimentally verified and reported in [91].

## 2.2 Sources of Noise in SiGe HBTs

There exists several sources of noise in a SiGe HBT which two of them mainly dominates the broadband microwave noise performance: 1) Thermal noise associated with the parasitic resistances of the device and 2) Shot noise sources which arise from the diffusion currents across the potential barriers in a SiGe HBT. Fig.2.5 shows a simplified small-signal and noise model for a SiGe HBT which includes the shot noise sources associated with the DC currents as well as the thermal noise due to the parasitic resistances. In this section, a brief summary of these two noise sources are described and incorporated into a simple noise model for an HBT.

### 2.2.1 Thermal Noise

Thermal noise arises from the random motion (Brownian motion) of charge carriers which are thermally excited. This phenomena happens regardless of any bias voltage or electric field applied to a conductor and results in the generation of a current [92,93]. Thermal noise decreases when reducing the temperature of the conductor. For a



**Figure 2.5.** A standard SiGe HBT small signal and noise model.

conductor at the physical temperature of  $T_a$ , the thermal available noise power can be written as [93, 94]

$$N_{\Delta f} = \frac{hf}{e^{hf/kT_a} - 1} \Delta f, \quad (2.6)$$

where  $h$  is the Plank's constant,  $k$  is the Boltzman's constant,  $T_a$  is the ambient temperature, and  $\Delta f$  is the desired bandwidth. The available power can be assumed to be constant for the case in which  $hf \ll kT_a$ , which translates into  $f \ll 20.8T_a$ . Thus, the thermal noise power can be simply treated as a frequency independent parameter, called white noise, for the frequencies below approximately 100 GHz at an ambient temperature of 5 K. Consequently, for a resistor with a value of  $R$ , the power spectral density (PSD) of the thermal noise at temperature  $T_a$  can be simply written as [93, 94]

$$S_V = 4kT_a R \text{ (V}^2/\text{Hz)}, \quad (2.7)$$

where  $k$  is the Boltzman's constant and  $T_a$  is the ambient temperature.

### 2.2.2 Shot Noise

Shot noise occurs when electric charges have enough energy to pass a potential barrier [95]. Shot noise sources can be assumed to be frequency independent at low

frequencies where the phase delay in the junction is negligible<sup>1</sup>. The spectral density of a shot noise source can be written as  $\overline{|i|^2} = 2qI$ , where  $q$  is the charge of an electron and  $I$  is the DC current passing through the junction.

In the base-emitter junction of a SiGe HBT device, there are two types of carriers passing through a potential barrier which create shot noises. First, the electrons traveling from the emitter to the base region resulting in a current called  $I_{En}$ . Second, the hole current ( $I_{Ep}$ ) back injected from the base to the emitter region. These two sources of shot noise are fully uncorrelated. Thus, the total shot noise at the base-emitter junction can be formulated as [98]

$$\overline{|i_{n,e}|^2} = 2qI_E, \quad (2.8)$$

where  $I_E = I_{Ep} + I_{En}$ .

The electrons passing from the base to the collector junction create additional shot noise in a SiGe device. The collector current is simply a delayed version of the electron current passing through the base-emitter junction ( $I_{En}$ ). Thus these two sources are fully correlated and can be written as [96]

$$\overline{|i_{n,c}|^2} = \overline{|i_{n,e}e^{-j\omega\tau_n}|^2}, \quad (2.9)$$

where  $\tau_n$  is the transit time associated with the transport of emitter-injected electron shot noise current, and includes both the transit time in the base and the transit time in the collector-base junction [96].

For a SiGe HBT, the common-emitter representation of the shot noise sources can be rewritten as [99].

$$\overline{|i_{n,b}|^2} = \overline{|i_{n,c}|^2} + \overline{|i_{n,e}|^2} - 2\Re\{\overline{i_{n,e}^* i_{n,c}}\}, \quad (2.10)$$

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<sup>1</sup>This assumption could be violated at very high frequencies [96, 97].

$$\overline{|i_{n,c}|^2} = 2qI_C, \quad (2.11)$$

and the correlation between the base and collector current spectral densities can be formulated as [99]

$$\overline{|i_{n,b}^* i_{n,c}|} = \overline{|i_{n,e}^* i_{n,c}|} - \overline{|i_{n,c}|^2}, \quad (2.12)$$

where  $i_{n,e}$ ,  $i_{n,c}$ , and  $i_{n,b}$  are the total emitter, collector, and base noise current power spectral densities, respectively.

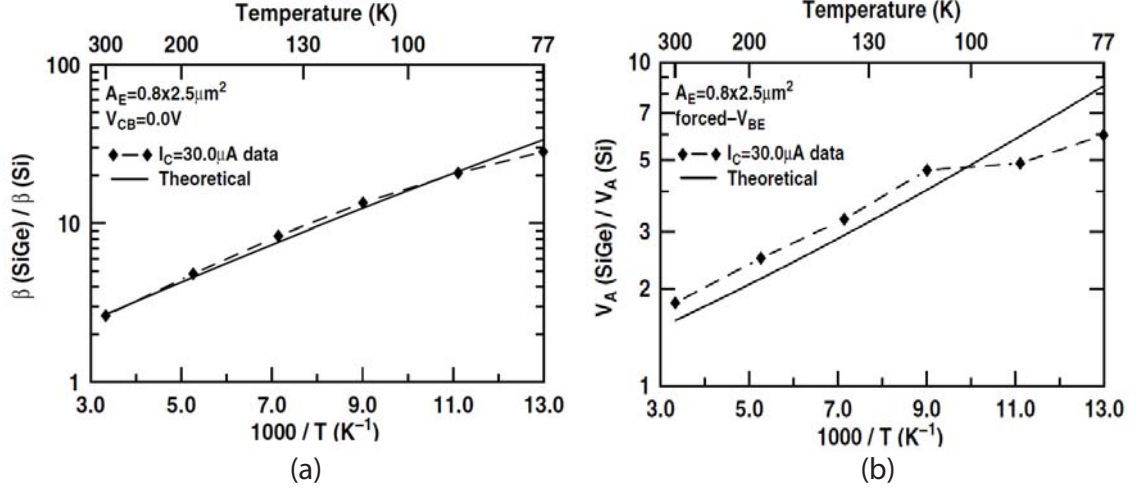
### 2.3 SiGe HBTs at Cryogenic Temperatures

So far, we have briefly described the fundamentals of SiGe HBTs as well as the sources of noise and presented the standard SiGe HBT noise model. In this section, the performance of SiGe HBTs with cooling is presented and some specific properties of these devices at cryogenic temperature are reviewed.

There have been several studies carried out on the characteristics of SiGe HBTs at low temperatures in the past [56, 78, 79] and it turned out the device behavior changes favorably with cooling. As it was shown in the earlier sections, the current gain ratio of a SiGe HBT with respect to a Si BJT device can be calculated as [78]

$$\frac{B_{DC,SiGe}}{B_{DC,Si}} \approx \tilde{\chi}\tilde{\eta}\Delta E_{g,Ge(grade)}/kT_a \times \frac{e^{\Delta E_{g,Ge(0)}/kT_a}}{1 - e^{-\Delta E_{g,Ge(grade)}/kT_a}}, \quad (2.13)$$

which shows that the DC current gain of a SiGe HBT should increase quasi exponentially with cooling in comparison with a Si BJT device. This improvement is a function of the Ge content in the base and is technology dependent. In [78], the DC current gain ratio was calculated and compared to measurements as a function of temperature which confirmed the DC current gain improvement for SiGe HBTs with cooling (See Fig.2.6.(a)).



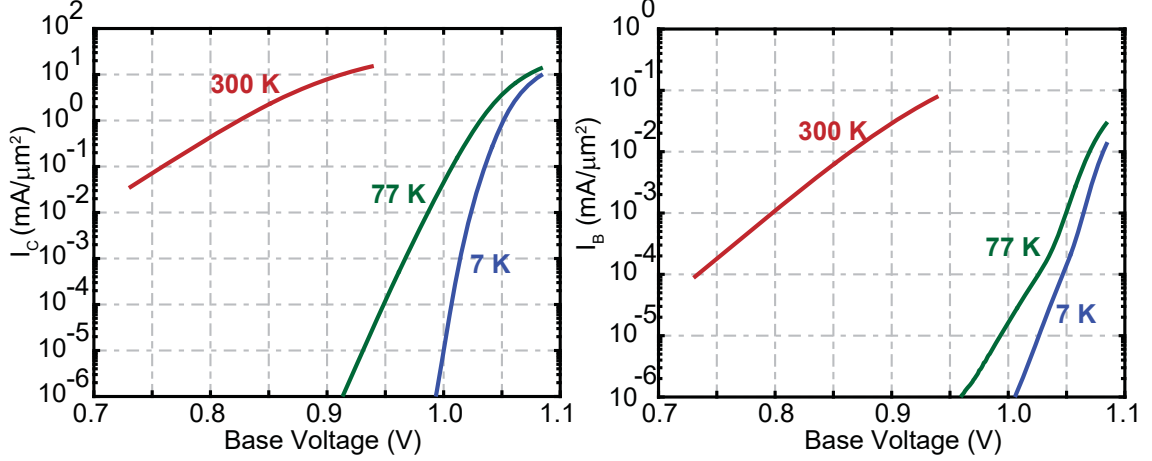
**Figure 2.6.** (a) DC current gain ratio of a SiGe HBT and a Si BJT as a function of temperature. (b) The Early voltage ratio of a SiGe HBT and a Si BJT as a function of temperature. Figure reproduced from [79], ©2005 IEEE.

In addition, the Early voltage of a SiGe HBT is also expected to increase with cooling as shown in the equation below. [78]

$$\frac{V_{A,\text{SiGe}}}{V_{A,\text{Si}}} \approx e^{\Delta E_{g,\text{Ge(grade)}}/kT_a} \times \frac{1 - e^{-\Delta E_{g,\text{Ge(grade)}}/kT_a}}{\Delta E_{g,\text{Ge(grade)}}/kT_a}. \quad (2.14)$$

The Early voltage is expected to increase exponentially with the cooling of SiGe HBTs. The theoretical calculations are compared to measurements for a SiGe HBT and a Si BJT device and results are shown in Fig.2.6.(b) [78].

The transconductance ( $g_m$ ) of a SiGe HBT also changes favorably with cooling. The improvement in the transconductance of a SiGe HBT was verified in this work through device measurements at three different temperatures of 7, 77, and 300 K for an  $18 \times 0.12 \mu\text{m}^2$  GF BiCMOS SiGe HBT. The Gummel curves for the collector and base current densities are shown in Fig.2.7. It is apparent from the figures that the slope of the gummel curves, which corresponds to the device transconductance, increases when cooling down a device from room temperature to 7 K.



**Figure 2.7.** Gummel curves for a GF BiCMOS8HP SiGe HBT device with a size of  $18 \times 0.12 \mu\text{m}^2$  operating at 7, 77, 300 K temperatures.

The unity gain cutoff frequency ( $f_t$ ) and the maximum frequency of the oscillation ( $f_{max}$ ) of a SiGe HBT can be written as [100]

$$f_t \approx \frac{g_m}{2\pi(C_{BE} + C_{CB})}, \quad (2.15)$$

and

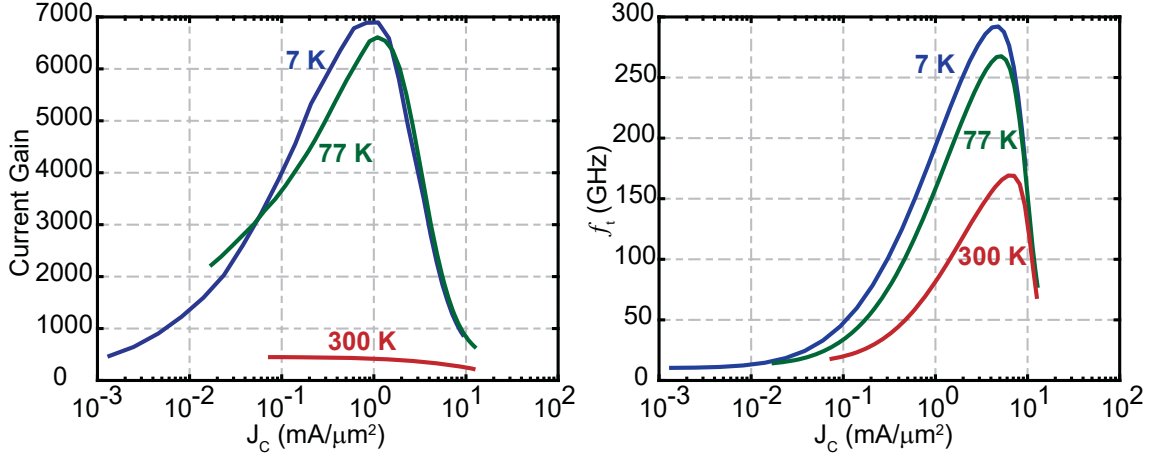
$$f_{max} \approx \sqrt{\frac{f_t}{8\pi r_b C_{CB}}}, \quad (2.16)$$

which both are expected to increase with cooling due to the improvement in  $g_m$  of the device. The improvement in the DC current gain ( $\beta_{DC}$ ) and the unity cutoff frequency ( $f_t$ ) of an  $18 \times 0.12 \mu\text{m}^2$  GF BiCMOS SiGe HBT was investigated experimentally<sup>2</sup> in this study and results are shown in Fig.2.8. The current gain improves by approximately a factor of 15 and the unity gain cutoff frequency increases by a factor of 2 when cooling from the room temperature down to 7 K.

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<sup>2</sup>Further measurement results are presented in Chapter 6.





**Figure 2.8.** (a) DC current gain of a SiGe HBT device with a size of  $18 \times 0.12 \mu\text{m}^2$  as a function of collector current density at three temperatures of 7, 77, 300 K. (b) Unity gain cutoff frequency of a SiGe HBT device with a size of  $18 \times 0.12 \mu\text{m}^2$  as a function of collector current density at three temperatures of 7, 77, 300 K.

## 2.4 SiGe HBTs Operating at High Injection Region

In modern circuits, SiGe HBTs need to be biased at high current densities to achieve maximum  $f_t$  and  $f_{max}$ . However, there are several limiting factors in operating at high currents which constrains the device performance. We will briefly discuss some of these limitations in this chapter. In general, high injection operation of a SiGe HBT is referred to a case in which the concentration of local minority carriers in a region exceeds the ionized doping level [78]. For a modern SiGe HBT device, the onset of high injection state occurs for current densities above  $1 \text{ mA}/\mu\text{m}^2$  [78].

The Gummel curves shown in Fig.2.7 presents the experimental data taken for a SiGe HBT which shows the transition of the collector current from its ideal behavior which manifests itself above  $1 \text{ mA}/\mu\text{m}^2$  collector current densities. Besides the impact on the DC currents, there are other non-idealities in a SiGe device performance at high currents which are explained in the following sections.

### 2.4.1 Kirk Effect

Kirk effect is a device non-ideality at high current densities which occurs when the minority carriers in the collector-base space charge region exceeds the doping charge in that area. This phenomena pushes the base out to the collector region which effectively widens the width of the base [101] (See Fig.2.9). The collector current density of a SiGe HBT is inversely proportional to the base width and widening of the base due to the Kirk effect directly impacts  $J_C$ . In addition, the base transit time degrades with the widening of the base ( $\tau_b \approx 1/W_b^2$ ) resulting in a reduction in DC current gain and the unity cut off frequency of the device [78].

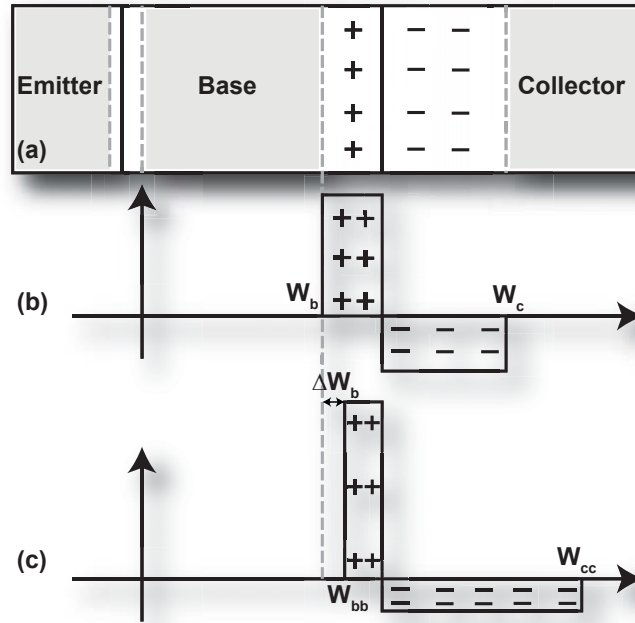
The current density at which the onset of Kirk effect happens can be written as [78]

$$J_{C,Kirk} \approx q\nu_s N_{dc} \left(1 + \frac{2\epsilon(V_{CB} + \phi_{bi})}{qN_{dc}W_{epi}^2}\right), \quad (2.17)$$

where  $q$  is the charge of an electron,  $\nu_s$  is the electron saturation velocity,  $W_{epi}$  is the thickness of the collector epi-layer,  $\phi_{bi}$  is the collector-base built-in potential, and  $N_{dc}$  represents the doping of the collector. From Eq.2.17, it is clear that increasing the doping of the collector pushes the onset of the kirk effect to higher currents. However, increasing  $N_{dc}$  results in a degradation of collector-base breakdown voltage which presents a fundamental tradeoff in the performance of a SiGe HBT device that is commonly referred to as "Johnson-Limit" [102].

### 2.4.2 High Injection Heterojunction Barrier Effect (HBE)

When a SiGe HBT operates at high current densities, an excess electron barrier occurs on the conduction band at the collector-base region which results in the accumulation of more electrons in the base area. This phenomena is negligible at low current densities. However, at high injection, it causes significant degradation in  $f_t$  and  $f_{max}$  of a device [103–105]. Fig.2.10 shows simulated conduction band at the



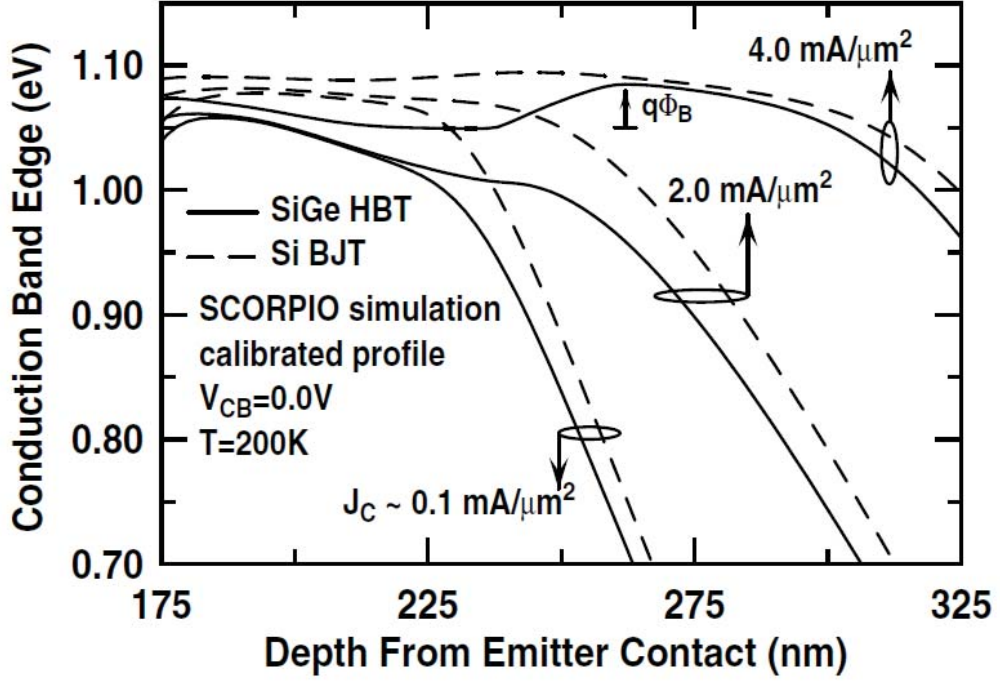
**Figure 2.9.** Space-charge distribution in the base-collector junction showing the widening of the base at high current densities. Figure after [80].

base-collector region for different current densities which highlights the high-injection-induced barrier at high current densities [78].

Heterojunction barrier effect (HBE) is mainly determined by the collector doping ( $N_{dc}$ ) and the germanium induced band offset at the collector-base junction. Increasing ( $N_{dc}$ ) results in pushing the HBE effect to the higher current densities, however, decreasing the breakdown voltage of the device which results in a fundamental trade-off in the design of SiGe HBTs. Changing the Ge profile can be helpful in pushing the onset of HBE effect to higher currents, however, it can reduce the film stability [78]. The effect of HBE on the device performance is expected to become more significant with reducing the temperature [78].

### 2.4.3 Webster Effect

At high injection operation, the number of minority carriers in the base is comparable with the majority ionized impurity concentration. In this case, the number of



**Figure 2.10.** Simulated conduction band showing the barrier effect at high current densities. Reproduced from [78].

holes in the valence band increases to compensate for the large amount of minority carriers in the base at high injection. This phenomena results in the degradation of the current gain of a device biased at high injection region and was first reported by Webster in 1954 [106].

#### 2.4.4 Carrier-to-Carrier Scattering

The mobility of the carriers in the silicon depends on different scattering mechanisms one of which is the carrier-to-carrier scattering. This phenomena becomes important when there exists a high carrier concentration in the silicon [107]. This effect was first studied by Dorkel and Leturcq in 1981 [107]. The carrier mobility due to the carrier-to-carrier scattering can be expressed as

$$\mu_{ccs} = \frac{2 \times 10^{17}}{\sqrt{np}} \frac{T_a^{3/2}}{\ln(1 + 8.28 \times 10^8 T_a^2 (np)^{-1/3})} \quad (2.18)$$

where  $n$  and  $p$  are the number of electrons and holes in  $cm^{-3}$ .

At low injection level,  $pn \ll N^2$  which results in a high  $\mu_{ccs}$  value. Therefore, the carrier-to-carrier would not be a limiting factor in the total mobility of the carriers at low current densities [107–109]. On the other hand, the  $\mu_{ccs}$  starts degrading at high injection region which could constraint the total carrier mobility [107].

## 2.5 Summary

In this section, the fundamentals of a SiGe HBT was briefly described. It was shown that SiGe HBTs can provide a better performance over the Si BJT devices leveraging the band engineering technique in the device fabrication. The improvement in the performance of a SiGe HBT by cooling down a device to cryogenic temperatures was reviewed. The experimental results from the literature show significant improvements in the DC current gain of a device as well as the unity gain cutoff frequency. This chapter was concluded with a brief discussion on the second order effects manifesting at high current densities. There are several physical mechanisms which contributes to the performance degradation at high current densities such as Kirk effect, heterjunction barrier effect, Webster effect, and carrier-to-carrier scattering.

## CHAPTER 3

### THEORY OF SIGE HBT OPERATION AT LOW SUPPLY VOLTAGES

Low-power cryogenic low noise amplifiers (LNAs) are required in many emerging applications as described in Chapter 1. LNAs are typically designed for operation at a specific current density at which the minimum noise for the device is achieved. Consequently, to reduce the power dissipation of cryogenic LNAs, lowering the supply voltage is the only degree of freedom. As mentioned earlier in Section 1.6, the DC-IV curves of SiGe HBTs show an ideal behavior even for supply voltages as low as 100 mV for current densities below  $2 \text{ mA}/\mu\text{m}^2$  in the medium injection regime. Here, we investigate the theory behind the trade-off between the power dissipation and the overall performance of a device operating near the saturation region for low-power purposes. This chapter summarizes parts of the results published in [70].

#### 3.1 Excess Shot Noise at Low Supply Voltages

One of the important consequences of operating a SiGe HBT at low supply voltages is the generation of excess shot noise due to the carriers passing the base-collector junction. The base-collector junction biased at near saturation region acts as a near forward bias junction. This would allow the mobile electrons to diffuse from the collector to the base and holes from the base to the collector. Therefore, the DC current of a SiGe HBT device biased at near saturation region can be written as

$$I_B = I_{BF} + I_{BR}, \quad (3.1)$$

and

$$I_C = I_{CF} - I_{CR} - I_{BR}, \quad (3.2)$$

where  $I_{BF}$  is the base current due to the holes traveling from the base to the emitter and  $I_{BR}$  is the extra DC current due to the holes going from the base to the collector when the junction is weakly forward biased. Similarly,  $I_{CF}$  and  $I_{CR}$  are the forward and reverse collector currents, respectively. Plugging Eq.3.1 and Eq.3.2 into the shot noise equations described earlier in Section.2.2.2, the shot noise sources in a SiGe HBT can be re-written as

$$\overline{|i_{n,b}|^2} = 2q (I_{BF} + I_{BR}) \Delta f = 2qI_B\Delta f, \quad (3.3)$$

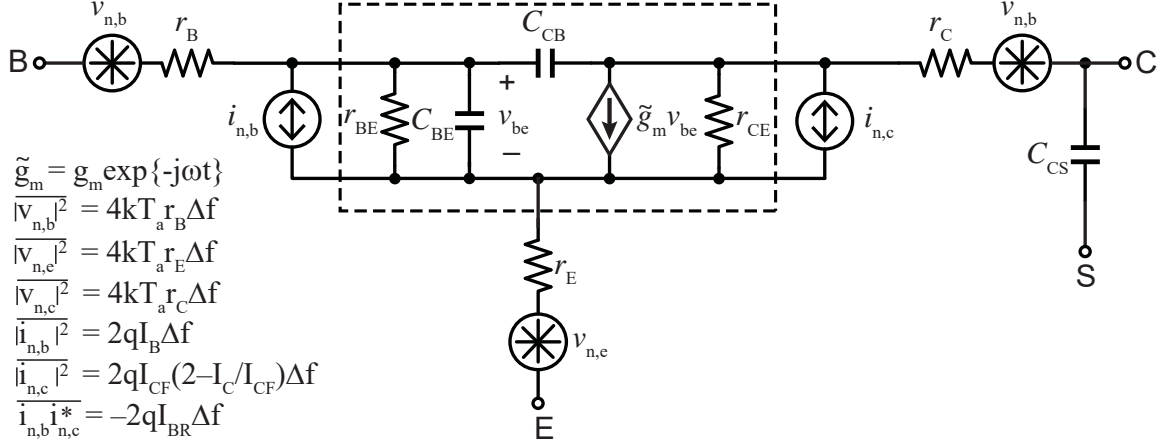
$$\overline{|i_{n,c}|^2} = 2q (I_{CF} + I_{CR} + I_{BR}) \Delta f = 2qI_{CF} \left( 2 - \frac{I_C}{I_{CF}} \right) \Delta f, \quad (3.4)$$

$$\overline{i_{n,b}i_{n,c}^*} = -2qI_{BR}\Delta f. \quad (3.5)$$

Eq.3.3, Eq.3.4, and Eq.3.5 are valid for the operation at forward active as well as near saturation regime for frequencies well below  $f_t$  at which the correlation between the base and collector shot noise sources can be neglected [96, 110].

### 3.2 Theoretical Noise Performance at Low Supply Voltages

A standard small signal and noise model for a SiGe HBT is shown in Fig.3.1 in which the shot noise sources capture the forward active as well as the effect of near saturation operations. The intrinsic SiGe HBT parameters are shown inside the dashed box. The model can be used for frequency ranges up to 40 GHz with a good accuracy for devices with  $f_t \gg 40$  GHz. For higher frequency modeling, the correlation between the shot noise sources needs to be taken into account and a higher order model with capacitance splitting methods can be used [111].



**Figure 3.1.** A general HBT small-signal noise model. In the forward-active mode of operation,  $I_C = I_{CF}$  and  $I_B = I_{BF}$  and the model simplifies to the standard HBT noise model. Inside the dashed-box is the intrinsic SiGe HBT. Figure reproduced from [70], ©2016 IEEE.

The noise parameters and associated gain of a SiGe HBT can be calculated using the equivalent two port model presented in Fig.3.1. The Y-parameters of the intrinsic two-port network (shown inside the dashed box) can be calculated as below.

$$\begin{bmatrix} 1/r_{BE} + j\omega(C_{BE} + C_{CB}) & -j\omega C_{CB} \\ g_m - j\omega C_{CB} & -j\omega C_{CB} \end{bmatrix}$$

The chain representation of the SiGe HBT can be used to calculate the noise parameters of the device as shown in Fig.3.2. The spectral densities of the input referred noise sources can be written as [78]

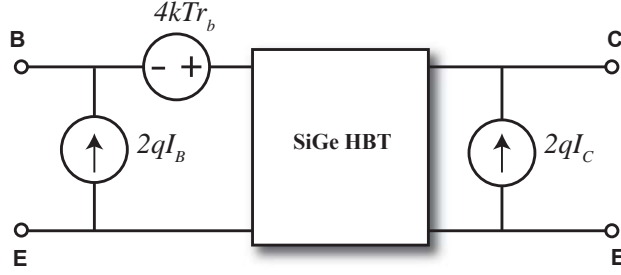
$$S_{in} = \overline{|i_{nc}|^2} \frac{|Y_{11}|^2}{|Y_{21}|^2} + \overline{|i_{nb}|^2}, \quad (3.6)$$

$$S_{v_n} = 4kT_a r_b + \frac{\overline{|i_{nc}|^2}}{|Y_{21}|^2}, \quad (3.7)$$

and,

$$S_{i_n v_n^*} = \overline{|i_{nc}|^2} \frac{Y_{11}}{|Y_{21}|^2}. \quad (3.8)$$





**Figure 3.2.** The two port representation of a noisy network.

Substituting the Y-parameters of the two port network in to the equations results in

$$S_{in} = 2qI_{CF}\left(2 - \frac{I_C}{I_{CF}}\right)\left(\frac{1}{\beta_{DC}} + \left(\frac{\omega}{\omega_t}\right)^2\right), \quad (3.9)$$

$$S_{v_n} = 4kT_a r_b + 2qI_{CF}\left(2 - \frac{I_C}{I_{CF}}\right)\frac{1}{g_m^2}, \quad (3.10)$$

and

$$S_{i_n v_n^*} = 2qI_{CF}\left(2 - \frac{I_C}{I_{CF}}\right)\frac{1}{g_m \beta_{DC}} + j2qI_{CF}\left(2 - \frac{I_C}{I_{CF}}\right)\left(\frac{1}{g_m}\right)\left(\frac{\omega}{\omega_t}\right)^2. \quad (3.11)$$

Using the noise spectral densities, the noise parameters can be formulated as [78, 112, 113]

$$R_N = \frac{S_{v_n}}{4kT_0}, \quad (3.12)$$

$$G_{OPT} = \sqrt{\frac{S_{in}}{S_{v_n}} - \frac{(\Im\{S_{i_n v_n^*}\})^2}{S_{v_n}^2}}, \quad (3.13)$$

$$B_{OPT} = -\frac{\Im\{S_{i_n v_n^*}\}}{S_{v_n}}, \quad (3.14)$$

$$NF_{MIN} = 1 + 2R_n\left(G_{OPT} + \frac{\Re\{S_{i_n v_n^*}\}}{S_{v_n}}\right), \quad (3.15)$$

and,

$$G_{ASSOC} = \left| \frac{Y_{21}}{Y_{11} + Y_{OPT}} \right|^2 \frac{G_{OPT}}{G_{OUT}}, \quad (3.16)$$

where

$$G_{OUT} = \Re \left\{ Y_{22} - \frac{Y_{12}Y_{21}}{Y_{11} + Y_{OPT}} \right\}. \quad (3.17)$$

Now, substituting Eq.3.9–3.11 into Eq.3.12–3.16 provides the noise parameters and the associated gain as

$$T_{MIN} \approx n_{cF} T_a \left[ g_{mF} r_B \left( 2 - \frac{I_C}{I_{CF}} \right) \left( \frac{f}{f_t} \right)^2 + \sqrt{\frac{1}{\beta_F} \frac{I_B}{I_{BF}} \left[ \frac{I_{CF}}{I_C} \left( 2 \frac{I_{CF}}{I_C} - 1 \right) + \frac{2g_{mF} r_B}{n_{cF}} \right] + \frac{2g_{mF} r_B}{n_{cF}} \left( 2 - \frac{I_C}{I_{CF}} \right) \left( \frac{f}{f_t} \right)^2} \right], \quad (3.18)$$

$$R_{OPT} \approx \frac{\beta_F}{g_{mF} (I_B/I_{BF} + \beta_F (2 - I_C/I_{CF}) (f/f_t)^2)} \times \left[ (1/\beta_F) (I_B/I_{BF}) \left[ (I_{CF}/I_C) (2(I_{CF}/I_C) - 1) + (2g_{mF} r_B/n_{cF}) \right] + (2g_{mF} r_B/n_{cF}) (2 - (I_C/I_{CF})) (f/f_t)^2 \right]^{1/2}, \quad (3.19)$$

$$X_{OPT} \approx \frac{\beta_F}{g_{mF}} \frac{I_{CF}}{I_C} \frac{f}{f_t} \frac{2 - I_C/I_{CF}}{(I_B/I_{BF}) + \beta_F (2 - I_C/I_{CF}) (f/f_t)^2}, \quad (3.20)$$

$$R_N \approx \frac{T_a}{T_0} \left( r_B + \frac{n_{cF}}{2g_{mF}} \frac{I_{CF}}{I_C} \left( 2 \frac{I_{CF}}{I_C} - 1 \right) \right), \quad (3.21)$$

and

$$G_{ASSOC} \approx \frac{f_t}{f} \frac{n_{cF}/2}{2\pi f C_{CB} r_B} \times \sqrt{\frac{1}{\beta_F} \frac{I_B}{I_{BF}} \left( \frac{I_{CF}}{I_C} \left( 2 \frac{I_{CF}}{I_C} - 1 \right) + \frac{2g_{mF} r_B}{n_{cF}} \right) + \frac{2g_{mF} r_B}{n_{cF}} \left( 2 - \frac{I_C}{I_{CF}} \right) \left( \frac{f}{f_t} \right)^2}, \quad (3.22)$$

where  $n_{cF}$  is the ideality factor ( $n_{cF} = \frac{I_C}{g_{mF} V_T}$ ),  $g_{mF}$  is the forward active transconductance, and  $B_F$  is the forward active DC current gain. The expressions were derived assuming a high DC current gain and  $g_m \gg \omega C_{CB}$ .

### 3.3 Sources of the Noise Degradation at Low Supply Voltages

The noise parameters of a SiGe HBT were derived in the previous section. Equations (3.18)–(3.22) are valid for both the forward active and near saturation operation. The minimum noise temperature of a SiGe HBT at low frequency can be simplified as

$$T_{MIN} \approx n_{cF} T_a + \sqrt{\frac{1}{\beta_F} \frac{I_B}{I_{BF}} \left[ \frac{I_{CF}}{I_C} \left( 2 \frac{I_{CF}}{I_C} - 1 \right) + \frac{2g_{mF} r_B}{n_{cF}} \right]}, \quad (3.23)$$

where the only bias dependent parameters in the equation are  $I_C$  and  $I_B$ . As the device enters the saturation region, the DC current gain reduces significantly which is expected to manifest itself as a sharp degradation in the  $T_{MIN}$  profile at low  $V_{CE}$  voltages.

At high frequencies,  $T_{MIN}$  is proportional to  $n_{cF} T_a g_{mF} r_B (2 - I_C/I_{CF})(f/f_t)^2$ . When a device enters the saturation region, the unity gain cutoff frequency is expected to degrade rapidly due to the increase in the  $C_{CB}$  capacitance which results in an increase in the high frequency minimum noise temperature at low  $V_{CE}$  voltages.

In addition, the optimum impedance of a SiGe HBT is expected to be purely resistive at very low frequencies and can be approximated as

$$R_{OPT} \approx \frac{I_{CF}}{g_{mF}} \frac{1}{I_B} \sqrt{\frac{1}{\beta_F} \frac{I_B}{I_{BF}} \left[ \frac{I_{CF}}{I_C} \left( 2 \frac{I_{CF}}{I_C} - 1 \right) + \frac{2g_{mF} r_B}{n_{cF}} \right]}, \quad (3.24)$$

which is expected to decrease significantly as the device enters the saturation region due to the degradation of the DC current gain and the significant increase in the base current itself.

On the other hand, the noise resistance of the SiGe HBT is independent of frequency and presents a bias dependent behavior. In equation 3.21, it is shown that the  $R_N$  is proportional to  $1/I_C$  and it is expected to rise significantly as the device enters the saturation region due to the degradation of the collector current.

The associated gain of a SiGe HBT is proportional to the unity gain cutoff frequency as shown in equation 3.22. Thus, it is expected that the gain decreases sharply with the supply voltage reduction.

### 3.4 Summary

The equations derived in this section present the dependence of the noise and gain performance as a function of DC and AC terminal characteristics at forward active operation as well as near-saturation region. The theoretical behavior of a SiGe HBT at reduced supply voltages was investigated based on the equations.

So far, we have developed a theoretical basis for describing the operation at near saturation. Now, it would be helpful to investigate the terminal behavior of SiGe HBTs as a function of supply voltages through cryogenic measurements to gain insight into the dependence of the noise performance on the  $V_{CE}$  voltage. In the next chapters, the cryogenic measurement setup as well as the experimental results are presented.

## CHAPTER 4

# DEVICE DESCRIPTIONS AND CRYOGENIC MEASUREMENT SETUP

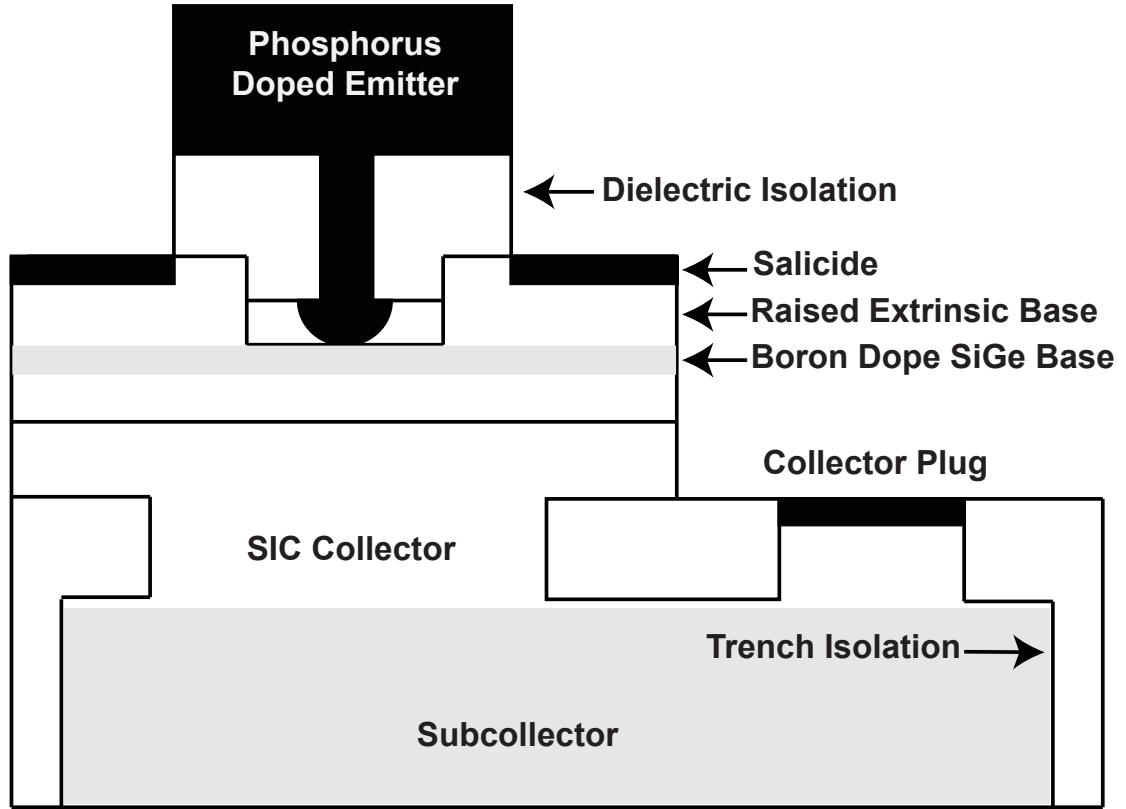
The physical structure of a SiGe HBT plays an important role in the noise performance of the device. For instance, the germanium content in the base directly influences the DC current gain,  $\beta_{DC}$ , and the unity gain cut-off frequency,  $f_t$ , which are desired to be maximized to achieve the best noise performance. Each foundry has its own unique procedure and optimization methods for the fabrication of these devices. Thus, careful study of SiGe HBTs from each fabrication process is required prior to designing circuits for the cryogenic operation.

Currently, there are several different foundries offering the BiCMOS technology processes such as IBM BiCMOS8HP, JAZZ SBC18H3, etc. An extensive study was carried out previously on the feasibility of employing these technologies in the cryogenic applications [56] and it was shown that commercial SiGe HBTs can provide competitive cryogenic performance in comparison with the HEMT devices.

In this work, we selected SiGe HBTs from the GF BiCMOS8HP as well as the TowerJazz SBC18H3 technology platforms for our studies. In this chapter, some of the unique features of these technologies are described and the details of the measurement setup used for the characterization of these devices at cryogenic temperatures are presented.

### 4.1 GF BiCMOS8HP Technology Process

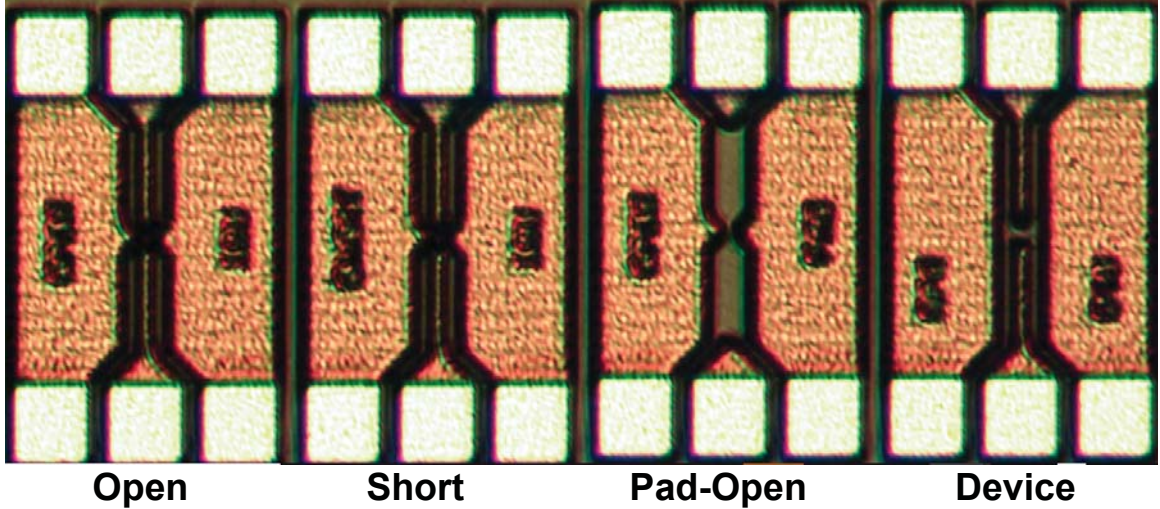
Silicon-germanium transistors from the Global Foundries BiCMOS8HP technology platform were used in this study to be characterized at cryogenic temperatures at



**Figure 4.1.** The device structure of a GF BiCMOS8HP SiGe HBT. Figure reproduced from [87], ©2002 IEEE.

both forward active and near saturation region. The BiCMOS8HP technology provides  $0.12 \mu\text{m}$  SiGe devices which are integrated with the  $0.13 \mu\text{m}$  CMOS technology node. The reported  $f_t$  and  $f_{MAX}$  of these devices for room temperature operation are 200 GHz and 280 GHz, respectively [85]. Fig.4.1 shows a device structure of a GF BiCMOS8HP SiGe HBT device [87].

In this process, the base is grown using a boron-dope SiGe alloy with carbon doping and %25 germanium content through a conventional nonselective UHV-CVD batch process [87]. This raised extrinsic base is formed self-aligned to a disposable mandrel used to define the emitter area. A phosphorus-doped polysilicon emitter is formed by deposition and annealing. The narrowing of the emitter and the emitter to



**Figure 4.2.** A photo of a GF SiGe HBT device from the BiCMOS8HP technology process along with the de-embedding structures.

extrinsic base spacer dimension in this technology helps lowering the base resistance of SiGe HBTs [87].

SiGe HBT transistors were taped out in the GF BiCMOS8HP technology platform for the characterization at cryogenic temperatures and Fig.4.2 shows a picture of the SiGe chip with a size of  $18 \times 0.12 \mu m^2$  along with the short, open, and pad-open de-embedding structures.

## 4.2 TowerJazz SBC18H3 Technology Process

SiGe HBTs from the TowerJazz SBC18H3 technology process were also studied in this work. The  $f_t$  and  $f_{MAX}$  reported for this technology for the room temperature operation are 240 and 270 GHz, respectively. The SBC18H3 technology provides  $0.13 \mu m$  SiGe devices as an add-on to a  $0.18 \mu m$  technology node. Table 4.1 shows a comparison between the SiGe HBTs from the GF BiCMOS8HP and the TowerJazz SBC18H3 processes and their characteristics.

In the SBC18H3 technology, a direct patterning of the emitter is featured by leveraging a sacrificial emitter to align to the extrinsic base and later replaced by an

**Table 4.1.** Transistor Metrics.

	JAZZ	IBM
	SBC18H3	BiCMOS8HP
$F_t/F_{\max}(GHz/GHz)$	240/270	200/280
Tech Node (nm)	0.18	0.12
BL Sub-Collector	Yes	Yes
FSA Extrinsic Base	Yes	Yes
Ge Content	30%	30%
Ge Profile	Triangular	Trapezoidal

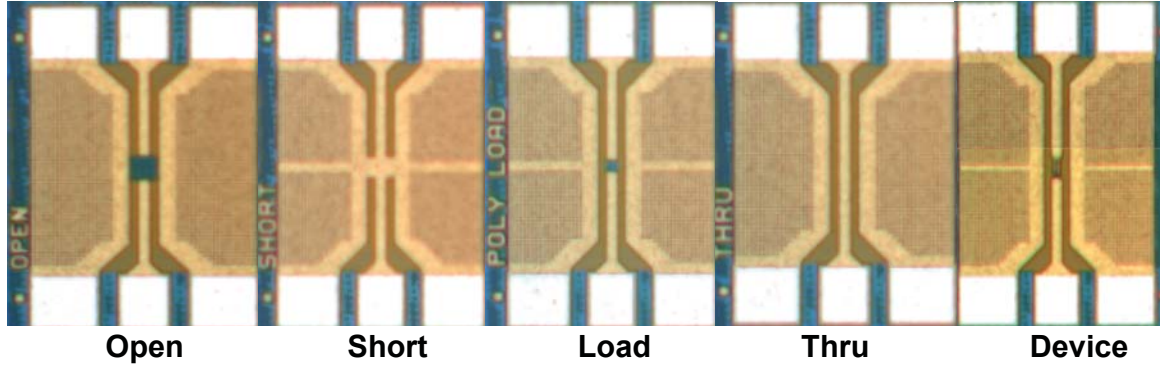
in-situ doped emitter. This technique enables controlling the emitter size more accurately which results in a low extrinsic base resistance compared to quasi-self-aligned (QSA) devices [114]. Poly-silicon-filled deep trench and oxide-filled shallow trench isolation are also available in this technology which could reduce the the substrate to collector capacitance ( $C_{CS}$ ) by a factor of 4 for a minimum size NPN device [114]. The germanium content in this technology has a triangular distribution with a peak of 30% [114, 115].

SiGe HBT transistors were taped out for the characterization at cryogenic temperatures and Fig.4.3 shows a picture of the SiGe chip along with the de-embedding structures.

### 4.3 Cryogenic Measurement Setup: Wafer Probe Measurements

Cryogenic measurements were carried out using a closed-cycle cryogenic probe station (Lakeshore CRX-4K) [116]. A block diagram of the on-wafer measurement setup is shown in Fig.4.4. In order to cool down the chamber, first a strong vacuum pump is connected to the chamber to lower the pressure and prevent icing. A Sumitomo F-70 compressor was used to circulate helium to the chamber and reduce the ambient temperature to 4 K [117]. The Cascade Microtech probes [118] were mounted on the probe holders inside the chamber which were heat sunk to the chuck to reduce the





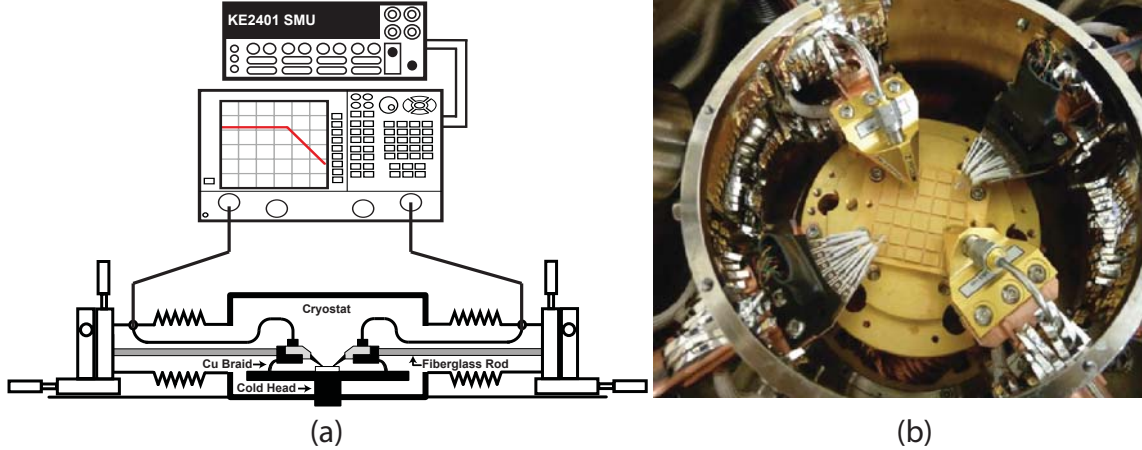
**Figure 4.3.** A photo of a transistor from the TowerJazz SBC18H3 technology process along with the on-wafer calibration structures.

thermal conduction between the probe tips and the chuck. Stainless steel cables were used for the input and output RF signals to minimize the thermal gradient between the room temperature and the chamber. The device under test sits on the chuck using vacuum grease to hold it down for measurements. A photo of the cryogenic probe station is shown in Fig.4.4.

The DC measurements were done using the Keithley 2612 dual SMU [119] which was connected to the vector network analyzer’s internal bias tee. The RF measurements were carried out using a Keysight N5247A PNA-X vector network analyzer (VNA) [120] over the 0.01-67 GHz frequency range. An LRRM [121] calibration was done using a CSR8 impedance standard substrate [122] to bring the reference plane of the measurements to the probe tips. Later, an open/short/pad-open de-embedding was carried out to remove the effect of the feedline and pad parasitics of a device and to bring the reference plane of the measurements to the input of the DUT.

#### 4.4 Cryogenic Measurement Setup: Cold Attenuator Method

Once the on-wafer measurements and modeling is carried out and low noise amplifiers are designed and implemented and packaged, the performance of the packaged amplifier should be characterized inside a chamber using the cold attenuator



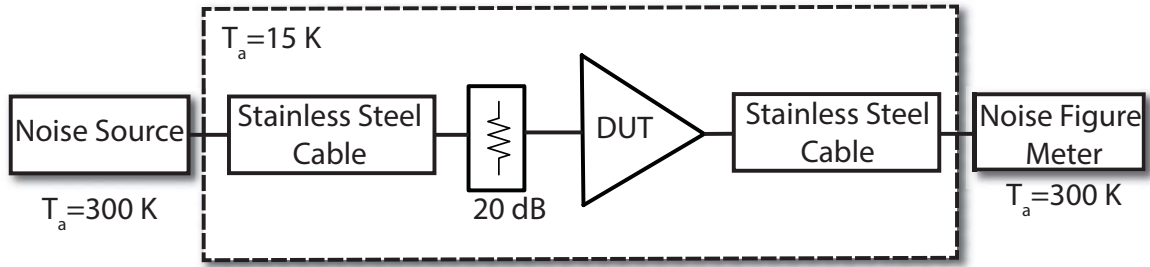
**Figure 4.4.** (a) A Block diagram of the on-wafer probe-station test setup. (b) A photo of the cryogenic probe-station with the probes assembled on the arms inside the chamber.

method [123]. A block diagram of an example cold attenuator measurement setup is shown in Fig.4.5 which includes a noise source mounted at room temperature followed by a 20 dB attenuator which is mounted inside the cryogenic chamber. The DUT is mounted after the attenuation and the output signals transitions to the room temperature and finally goes to the noise figure meter. The cold attenuator method solves the issue of uncertainty in the determination of the ENR of the noise source that exists in a conventional Y-factor measurement technique [123]. The 20 dB attenuator used in this technique also helps the input impedance to remain at  $50 \Omega$ .

The Y-factor formula for the cold attenuator method can be written as below [123] in which  $L$  is the attenuation value in linear units and  $T_l$  is the temperature of the attenuator.

$$Y = \frac{T_{hot}/L + T_l(L - 1)/L + T_e}{T_{cold}/L + T_l(L - 1)/L + T_e} \quad (4.1)$$

In the cold attenuator method, the loss before the attenuation needs to be determined accurately. For this reason, the cold attenuator system used for this study was calibrated using several low noise amplifiers from NIST and Caltech and it was



**Figure 4.5.** A schematic diagram of a noise measurement setup using the cold attenuator method.

calculated that the loss at the input of the system requires an offset of 2 K to be added to the absolute temperature of the cooled 20 dB attenuator.

## 4.5 Summary

In this section, several properties of the SiGe HBT devices used in this study were reviewed. Some unique features of the GF BiCMOS8HP as well as the TowerJazz SBC18H3 technology were presented. In addition, the measurement setup used for the characterization of those devices were described. The on-wafer and the cold attenuator setup for the measurement of the circuits and packaged LNAs were presented in detail.

## CHAPTER 5

### SMALL-SIGNAL MODEL EXTRACTION PROCEDURE

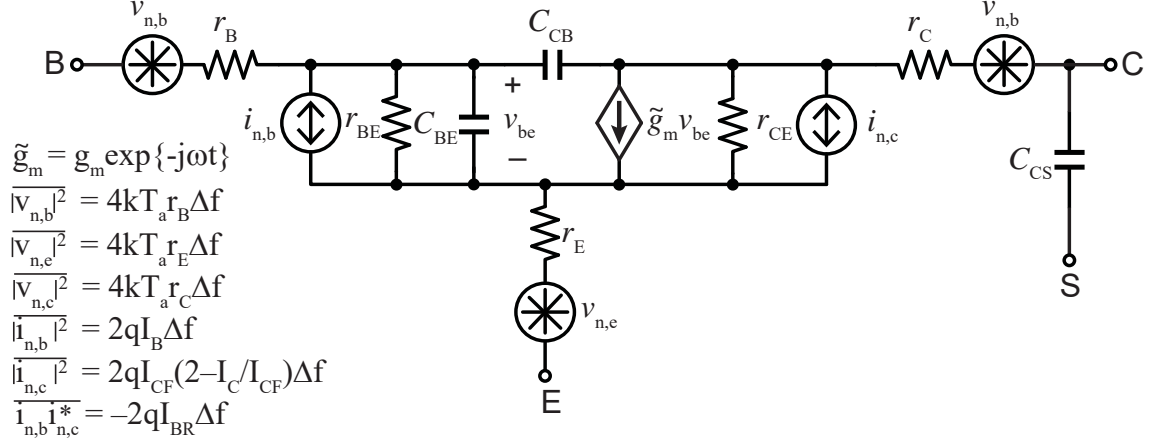
Small-signal and noise models were extracted as a function of current density and the collector to emitter voltages. The extracted models were later used to investigate the behavior of the noise parameters as a function of  $V_{CE}$  voltages as well as model predictions at high current density operations. In this chapter, the parameter extraction procedure is described in detail.

#### 5.1 SiGe HBT Standard Small-Signal Model

A standard SiGe HBT small-signal and noise model that is used in this work is shown in Fig.5.1. The model parameters were extracted using the DC as well as the active bias measurements. The collector and emitter resistances ( $r_E, r_C$ ) can be determined through several different methods such as open-collector, Gummel curves, and active sweep measurements. The collector to substrate capacitor ( $C_{CS}$ ) was calculated using the off-bias measurements at which the base-emitter voltage was set to zero. After subtracting the  $r_E$ ,  $r_C$ , and  $C_{CS}$  from the two port S-parameter measurements, the intrinsic device parameters can be calculated. The detailed parameter extraction procedure is described in the following sections.

#### 5.2 Determination of $C_{CS}$ and $C_{CB}$

The collector to substrate and the collector to base capacitors ( $C_{CS}$  and  $C_{CB}$ ) can be extracted using the off-bias measurement in which the collector voltage is swept while the base voltage is held at zero and the scattering parameters of the device



**Figure 5.1.** A general HBT small-signal noise model. In the forward-active mode of operation,  $I_C = I_{CF}$  and  $I_B = I_{BF}$  and the model simplifies to the standard HBT noise model.

is measured. In this case, the  $g_m$  and  $g_{BE}(= 1/r_{BE})$  can be neglected and a two port representation of a SiGe HBT can be simplified as shown in Fig.5.2. Using the Y-parameters of the two port network in Fig.5.2,  $C_{CS}$  and  $C_{CB}$  can be found as [56]

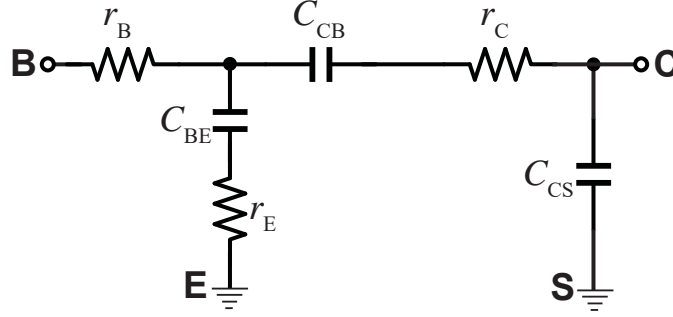
$$C_{CS} = \lim_{\omega \rightarrow 0} \frac{\Im(Y_{12} + Y_{22})}{\omega} \quad (5.1)$$

and

$$C_{CB} = - \lim_{\omega \rightarrow 0} \frac{\Im(Y_{12})}{\omega}. \quad (5.2)$$

### 5.3 Determination of Emitter and Collector Resistances

Several methods are reported in the literature for the extraction of the emitter resistance in a SiGe HBTs. Some techniques use the DC-IV curves of a device operating in the forward active region, whereas, others use the data when the device is biased in the saturation regime. Each method has its own benefits and shortcomings. In this section, we look at three different techniques for the extraction of the emitter resistance at cryogenic temperatures.



**Figure 5.2.** An equivalent two-port circuit model for the off-bias measurement.

### 5.3.1 Emitter Resistance Using Gummel Curves

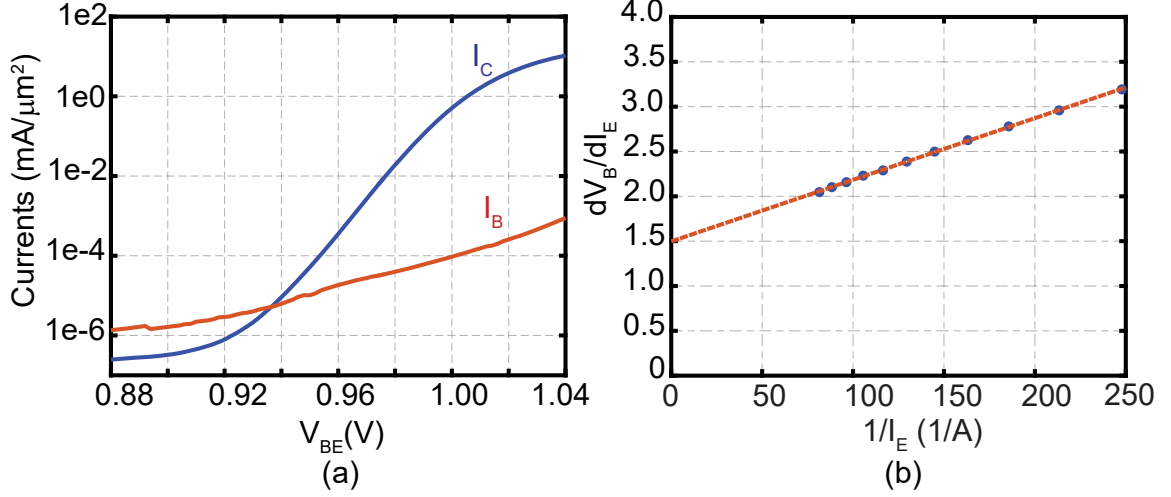
One approach to extract the emitter resistance is using the Gummel curves for a SiGe HBT. The collector and the base current of a SiGe HBT are proportional to the  $\exp(qV_{BE}/kT)$  at low current densities. However, they start deviating from the ideal form once the device enters the high injection region as shown in Fig.5.3. The deviation of the base current from the ideal behavior could be attributed to the emitter resistance of the device [124]. The base voltage can be written as

$$V_B = I_E \times r_e + n_C(kT_a/q) \times \ln(I_E/I_{C0}), \quad (5.3)$$

where  $I_{C0}$  is the saturation current. The emitter resistance can be found by taking a derivative of equation 5.3 with respect to the emitter current and extrapolating the results for the  $1/I_E$  approaching zero<sup>1</sup>. Fig.5.3 shows an example extraction data of the emitter resistance using the Gummel curves for a SiGe HBT with a size of  $10 \times 0.13 \mu m^2$  from the TowerJazz SBC18H3 technology platform. The extracted emitter resistance was calculated to be approximately  $1.5 \Omega$  using this extraction technique.

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<sup>1</sup>Current crowding effect is neglected in this method [125].



**Figure 5.3.** Emitter resistance extraction using the Gummel curve data for a SiGe HBT from the TowerJazz SBC18H3 technology with a size of  $1.3 \mu m^2$ . The extrapolation was done at  $V_{BE}$  between 1.02 and 1.04 V where the collector current is nonlinear.

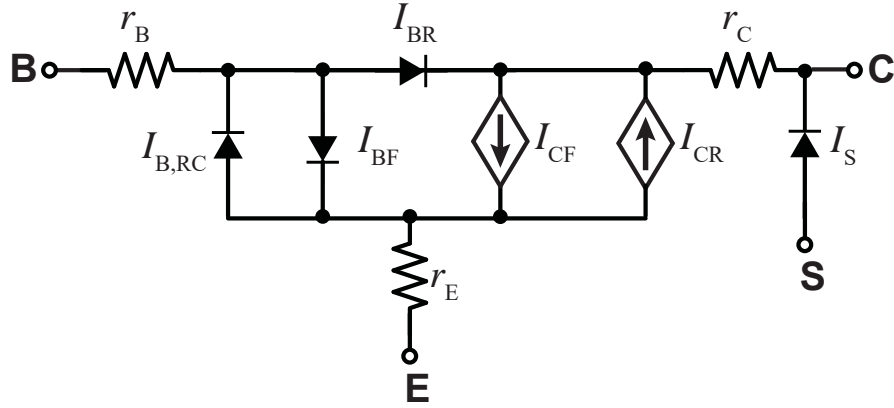
### 5.3.2 Emitter and Collector Resistance Extraction Using Open-Collector Method

The emitter and collector resistances can be extracted using the open-collector method [126]. In this method, the collector and the base currents are swept using current sources and the collector voltage is recorded. The p-n junctions in an HBT are both in forward active mode when biased for an open-collector measurement. A schematic diagram of a SiGe HBT is shown in Fig.5.4 for an open-collector measurement setup. The collector voltage ( $V_C$ ) can be written as [127, 128]

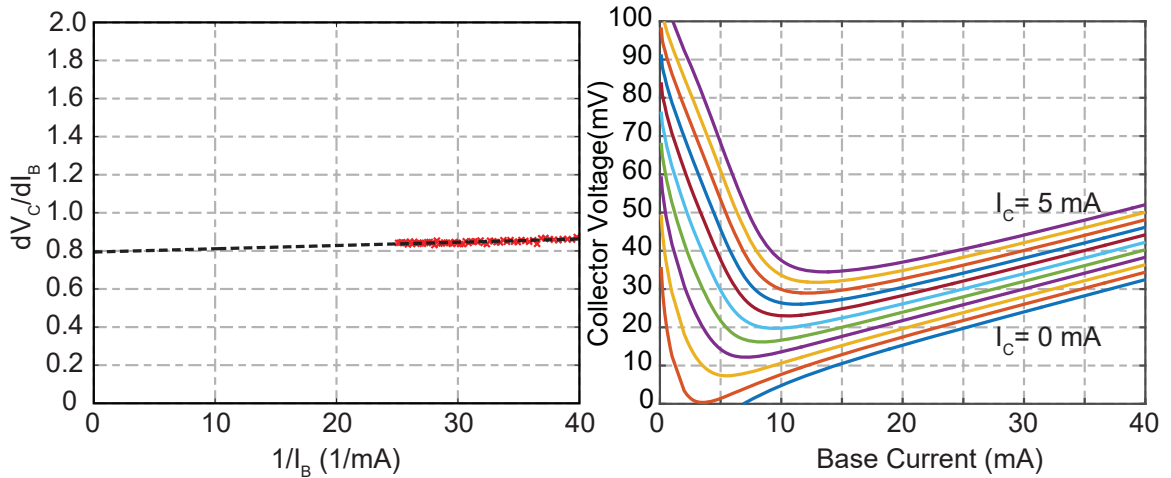
$$V_C = I_C \times (r_e + r_c + r_{cable}) + I_B \times r_e + V_T \times \ln\left(\left(\frac{I_C + I_B}{I_{C0}}\right)^{n_c} \left(\frac{I_{BR0}}{I_B}\right)^{n_{br}}\right), \quad (5.4)$$

where  $I_{BR0}$  is the the saturation base reverse current and  $n_{br}$  is the ideality factor associated with that. Now, the derivative of  $V_C$  with respect to  $I_B$  assuming that  $I_C = 0$  can be found as

$$\frac{dV_C}{dI_C} \approx r_e + \frac{V_T}{I_B} (n_c - n_{br}). \quad (5.5)$$



**Figure 5.4.** An equivalent circuit model of a SiGe HBT biased for open-collector measurement.



**Figure 5.5.** (a) Emitter resistance extraction using the open-collector method for a  $0.12 \times 18 \mu m^2$  SiGe HBT. (b) Collector resistance extraction using the open-collector method for a  $0.12 \times 18 \mu m^2$  SiGe HBT

Consequently, the emitter resistance can be approximately calculated by fitting a line to the equation 5.5 with respect to  $1/I_B$  and finding the intercept of the line with the y axis. Fig.5.5. (a) shows an example plot for the emitter resistance extraction for a  $0.12 \times 18 \mu m^2$  SiGe HBT from the GF BiCMOS8HP technology. The extracted emitter resistance was found to be approximately  $0.8 \Omega$  using the open-collector extraction method.



The collector resistance could be also extracted upon the knowledge of  $r_e$  using the open-collector method. Fig.5.5. (b) shows the collector voltage as a function of base current for several collector currents. Using Eq.5.4, the derivative of  $V_C$  with respect to  $I_C$  for a non-zero  $I_C$  current can be written as

$$\frac{dV_C}{dI_C} \approx r_e + r_c + r_{cable} + \frac{n_C V_T}{I_B + I_C}. \quad (5.6)$$

Thus, the collector resistance can be approximated at high collector currents as

$$r_c = \frac{dV_C}{dI_C} - r_e - r_{cable}, \quad (5.7)$$

where  $r_{cable}$  is the resistance of the cables in the open-collector measurement setup. The detail of the cable resistance measurement is described in Appendix.A.

### 5.3.3 Emitter and Collector Resistance Extraction Using Active-Sweep Data

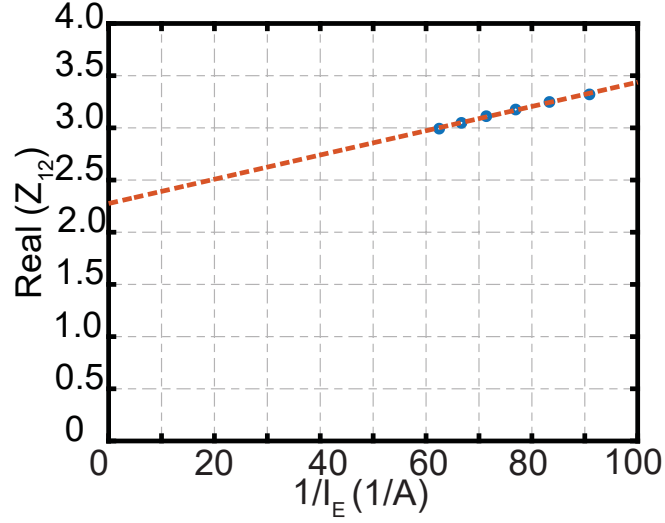
The emitter and collector resistances could be calculated using the scattering parameters of a SiGe HBT. The device should be biased at high currents and the emitter and collector resistances can be simply calculated at low frequencies as [129–131]

$$r_e = \lim_{1/I_E \rightarrow 0} \Re\{Z_{12}\}, \quad (5.8)$$

and

$$r_c = \lim_{1/I_E \rightarrow 0} \Re\{Z_{22} - Z_{12}\}, \quad (5.9)$$

respectively. Fig.5.6 shows an example plot for the extraction of the emitter resistance through the active sweep measurement. The extracted resistance was calculated to be approximately  $2.2\Omega$  for a SiGe HBT with a size of  $10 \times 0.13 \mu m^2$  from the TowerJazz SBC18H3 technology.



**Figure 5.6.** (a) Emitter resistance extraction using the active sweep method for a  $10 \times 0.13 \mu\text{m}^2$  SiGe HBT from the TowerJazz SBC18H3 technology.

## 5.4 Determination of Intrinsic Device Parameters

Once the emitter and collector resistances and the collector to substrate capacitance are extracted, they can be subtracted from the scattering parameters of the SiGe HBT. The remaining S-parameter data can be used to extract the intrinsic device parameters. First, a bias dependant base resistance can be calculated using the Z-matrix of the intrinsic device as written below [132].

$$r_b = \Re\{Z_{11} - Z_{12}\}. \quad (5.10)$$

After removing the base resistance from the Y-parameter data, the transconductance ( $g_m$ ), its associated delay time ( $\tau$ ), the base-emitter capacitance ( $C_{BE}$ ), and the base-emitter conductance ( $g_{BE}$ ) can be found as below.

$$g_m = |Y_{21} - Y_{12}|, \quad (5.11)$$

$$\tau = \frac{-\angle(Y_{21} - Y_{12})}{\omega}, \quad (5.12)$$

$$g_{BE} = \frac{g_m}{B_{AC}} = \frac{dI_B}{dV_{BE}}, \quad (5.13)$$

$$C_{BE} = \Im\{Y_{11} + Y_{12}\}, \quad (5.14)$$

and,

$$C_{CB} = -\frac{\Im\{Y_{12}\}}{\omega}. \quad (5.15)$$

Using the equations above, all the intrinsic small signal parameters of a SiGe HBT can be determined.

## 5.5 Summary

In this chapter, the small-signal model extraction procedure was described. The collector to substrate and collector to base capacitors were extracted using the off-bias measurement method. Three different techniques were reviewed for the emitter and collector resistance calculations and example results were presented for each method. Finally, the intrinsic parameter extraction was described using the active bias measurement data.

In the next chapter, the extracted noise parameter results are presented over a wide range of current densities at three different temperatures of 7, 77, 300 K along with the agreement between the extracted model and measurements.

## CHAPTER 6

# SIGe HBT CHARACTERIZATION AND MODELING RESULTS

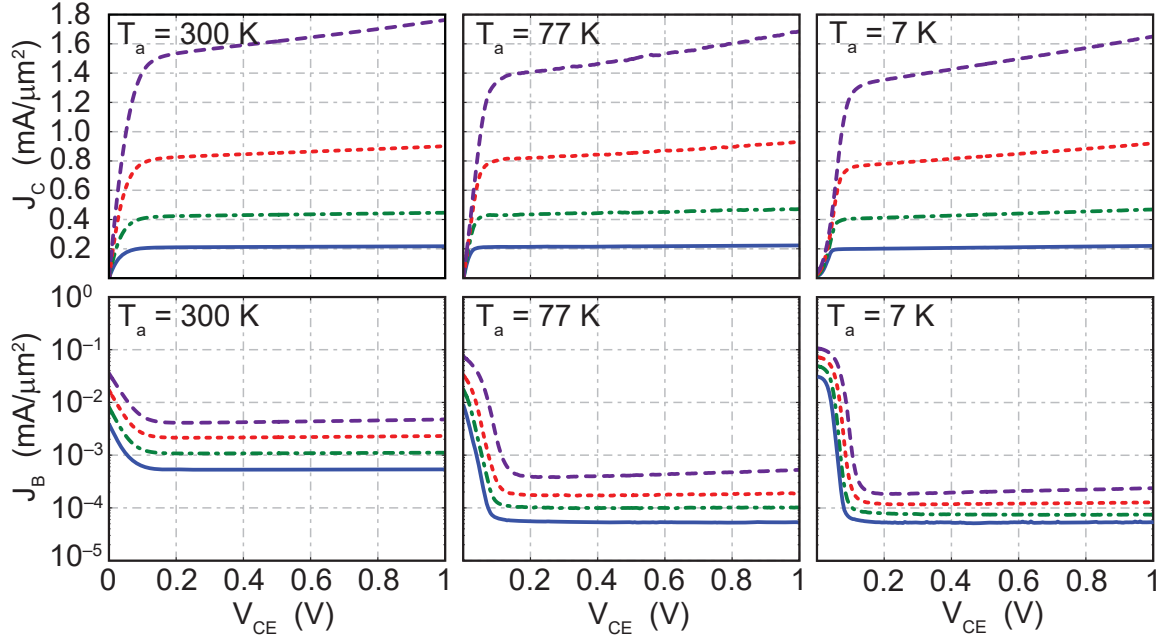
In this work, SiGe HBTs from the Global Foundries (GF) BiCMOS8HP as well as the TowerJazz SBC18H3 technology processes were selected to be modeled at cryogenic temperatures. In this chapter, we focus on the characterization and modeling results of the GF SiGe HBT devices as a function of supply voltages. The content of this chapter summarizes the results published in [70].

### 6.1 Measurements and Small-Signal Modeling Results

The DC and RF characteristics of a  $18 \times 10 \mu m^2$  SiGe HBT were measured using on-wafer measurements at 7, 77 and 300 K in a cryogenic probe-station setup described in 4.3. In this section, the measurements and small-signal modeling results are presented.

#### 6.1.1 DC Characteristics

The DC characteristics of a SiGe HBT were measured at 7, 77, 300 K temperatures and measurement results are presented in Fig.6.1. The collector and base current densities were measured as a function of collector to emitter voltage ( $V_{CE}$ ) over a wide range of base to emitter voltages ( $V_{BE}$ ). The collector current densities shown in Fig.6.1 cover a range of 0.2–2.8 mA/ $\mu m^2$ . An ideal behavior was observed for the collector and base current densities at all temperatures for collector to emitter voltages from 1 V down to approximately 100 mV. A sharp degradation of the collector current was observed at approximately 50-100 mV  $V_{CE}$  voltage which is due to the



**Figure 6.1.** Collector/base current densities as a function of collector-emitter voltage at 300 K (left), 77 K (center), and 7 K (right). Different curves show the currents at different base-emitter bias voltages [70], ©2016 IEEE.

transition of the base-collector junction from the reverse bias to the forward bias. A significant rise in the base current profile was also observed in the same collector to emitter voltage range which presents the transition of the device operation from the forward active to the saturation mode. A slight slope was observed on the  $J_C$  plots at high current densities due to the Early effect [133,134].

### 6.1.2 AC Characteristics

The scattering parameters of the SiGe HBT device were measured at 300, 77, 7 K using an Agilent N-5247A vector network analyzer (VNA). The measurement was carried out between 0.01 to 67 GHz frequency range. The parasitic effects due to the pads and feedline structures were de-embedded from the measurement results using the open/short/pad-open de-embedding technique described in [135].

The unity gain cut off frequency ( $f_t$ ) and the maximum frequency of oscillation ( $f_{max}$ ) of the device were then calculated from the measurement data by extrapolating the ac current gain and the unilateral gain as [136]

$$h_{21} = \frac{Y_{21}}{Y_{11}}, \quad (6.1)$$

and

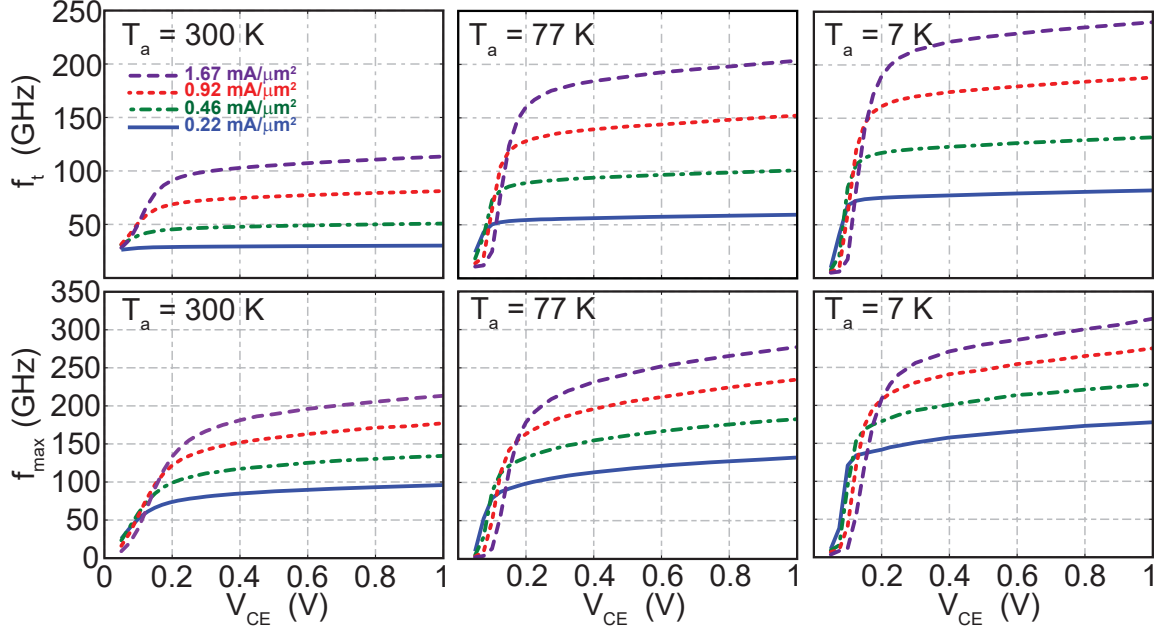
$$U = \frac{|Y_{21} - Y_{12}|^2}{4(\Re\{Y_{11}\}\Re\{Y_{22}\} - \Re\{Y_{21}\}\Re\{Y_{12}\})}. \quad (6.2)$$

The calculated  $f_t$  and  $f_{max}$  from the measurement data are shown in Fig.6.2. The measurements were carried out over a wide range of current densities and supply voltages. It is observed that the  $f_t$  and  $f_{max}$  of the device increases significantly with cooling which is due to the improvement in the transconductance ( $gm$ ) of the device. The measurement results are consistent with the theory described in section 2.3 as well as the data reported previously for SiGe HBTs at cryogenic temperatures [53, 56, 137, 138]. A positive slope on the  $f_t$  and  $f_{max}$  curves were observed which is due to an increase in  $C_{CB}$  as a function of  $V_{CB}$  voltage.

### 6.1.3 Non-Linearity of SiGe HBTs

Typically, cryogenic low noise amplifiers operate at very weak input signal levels. However, there are some emerging applications in which the linearity of cryogenic LNAs proves to be critical. For instance, in microwave kinetic inductance detectors (MKIDs) [139], the outputs of all elements of an array combine together prior to amplification which creates a necessity of high linearity tolerance for cryogenic LNAs.

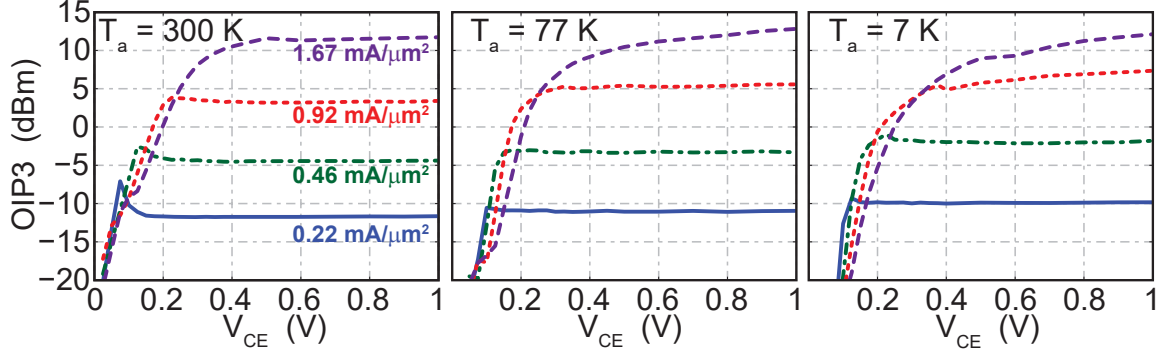
Here, the non-linearity of the SiGe HBT device was characterized as a function of the collector-emitter voltage to investigate any probable impact of the near saturation operation on the linearity. The output referred third order intermodulation intercept



**Figure 6.2.** Unity current gain cutoff frequency/maximum frequency of oscillation versus collector–emitter voltage at 300 K (left), 77 K (center), 7 K (right) [70], ©2016 IEEE.

( $OIP3$ ) was measured<sup>1</sup> at 300, 77, 7 K temperatures using the Agilent N-5247A VNA and example results are shown in Fig.6.3. The measurement data was taken at 3 GHz and were referenced to the bondpads of the transistor test structure. The general behavior is expected to be weakly dependent on frequency. Fig.6.3 shows that for current densities in the low injection region (below  $1 \text{ mA}/\mu\text{m}^2$ ), the  $OIP3$  is weakly dependent on the collector to emitter voltage. However, at higher current densities,  $OIP3$  degradation was observed at higher  $V_{CE}$  voltages. If the linearity is not critical in a design, a SiGe HBT can operate at  $V_{CE}$  voltages as low as 200 mV even at medium injection region.

<sup>1</sup>This measurement was carried out by my colleague, Hakan Coskun.



**Figure 6.3.** Output-referred third-order inter-modulation intercept at 300 K (left), 77 K (center), and 7 K (right). Measurement data taken at 3 GHz and referenced to the bondpads of the test structure. The general behavior is only weakly frequency dependent [70], ©2016 IEEE.

#### 6.1.4 Extracted Small-Signal Model

The small signal parameters of the SiGe HBT device at 300, 77, and 7 K temperatures were extracted using the extraction procedure described in Chapter 5. The model parameters are shown in Table.6.1– 6.3 for selected bias points.

The extracted small signal model of the SiGe HBT was compared to measurement data and results are shown in Fig.6.4 for a selected current density of  $J_{CF0}=0.46$  mA/ $\mu\text{m}^2$  at three different  $V_{CE}$  voltages ranging from the forward active to the near saturation operation. An excellent agreement between the extracted model and the measurement data was observed for frequencies between 0.01-40 GHz for forward active and near saturation region.

## 6.2 Noise Parameters Modeling Results

Noise parameters of the SiGe HBT device could be found using the noise parameter extraction procedure described in [56]. Here, we present the extracted noise parameters as a function of supply voltages to study the ultimate limitations on the noise performance at low  $V_{CE}$  voltages.



**Table 6.1.** Extracted Model Parameters at Selected Bias Points 7 K temperature. Units–Voltage: V, Current: mA/ $\mu\text{m}^2$ , Resistance:  $\Omega \cdot \mu\text{m}^2$ , Conductance: mS/ $\mu\text{m}^2$ , Capacitance: fF/ $\mu\text{m}^2$ , Delay: ps. [70], ©2016 IEEE.

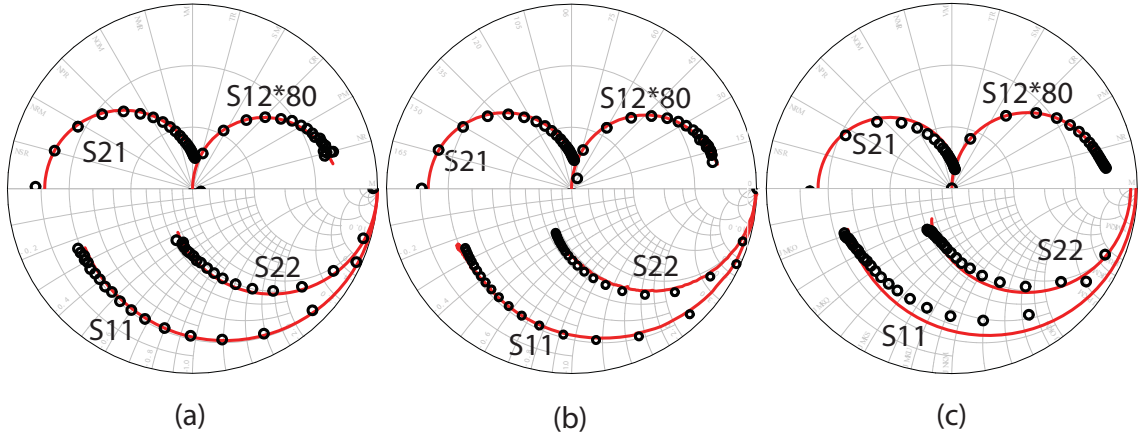
$T_a = 7 \text{ K}$					$R_E = 1.7$			$R_C = 6.7$				
$V_{CE}$	$J_{CF}$	$J_C$	$J_{BF}$	$J_B$	$R_B$	$r_{be}$	$r_{ce}$	$g_m$	$C_{BE}$	$C_{CB}$	$C_{CS}$	$\tau$
1.00	0.22	0.22	3.9e-5	3.9e-5	10.6	227k	43k	34	51	13	2	0.8
0.20	0.20	0.20	3.9e-5	4.1e-5	10.2	222k	43k	31	51	14	2	0.9
0.15	0.20	0.20	3.9e-5	4.4e-5	10.4	210k	43k	31	51	14	2	0.9
0.10	0.20	0.20	3.9e-5	5.0e-5	11.4	151k	43k	31	56	16	2	1.1
1.00	0.47	0.47	7.2e-5	7.2e-5	12.5	121k	14k	65	60	13	2	1.0
0.20	0.41	0.41	7.2e-5	7.2e-5	12.3	136k	14k	59	60	15	2	1.0
0.15	0.41	0.41	7.2e-5	7.3e-5	12.5	121k	14k	59	62	15	2	1.1
0.10	0.40	0.40	7.2e-5	9.3e-5	15.4	41k	14k	56	79	21	2	1.5
1.00	0.92	0.92	1.3e-4	1.3e-4	15.3	52k	6k	116	74	13	2	1.1
0.20	0.77	0.77	1.3e-4	1.3e-4	14.7	76k	6k	104	75	15	2	1.3
0.15	0.76	0.76	1.3e-4	1.3e-4	15.8	60k	6k	102	83	17	2	1.4
0.10	0.76	0.75	1.3e-4	3.2e-4	15.6	7k	1k	86	156	53	2	1.8
1.00	1.65	1.65	2.6e-4	2.6e-4	18.1	19k	3k	188	92	13	2	1.2
0.20	1.34	1.34	2.6e-4	2.6e-4	17.7	28k	3k	156	102	17	2	1.5
0.15	1.32	1.32	2.6e-4	2.6e-4	19.0	19k	3k	154	134	24	2	1.8
0.10	1.30	1.24	2.6e-4	2.1e-3	19.4	0.3k	0.3k	116	535	244	2	1.9

**Table 6.2.** Extracted Model Parameters at Selected Bias Points 77 K temperature.

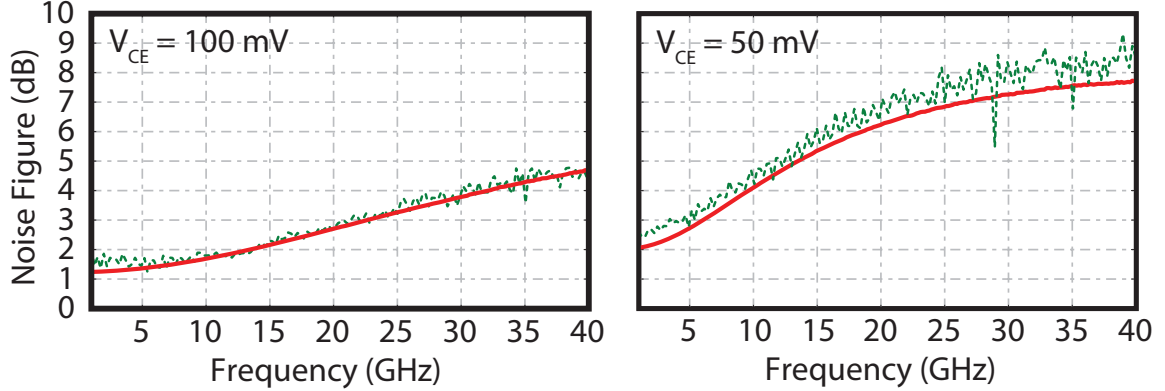
$T_a = 77 \text{ K}$					$R_E = 1.7$			$R_C = 7.3$				
$V_{CE}$	$J_{CF}$	$J_C$	$J_{BF}$	$J_B$	$R_B$	$r_{be}$	$r_{ce}$	$g_m$	$C_{BE}$	$C_{CB}$	$C_{CS}$	$\tau$
1.00	0.22	0.22	4.4e-5	4.4e-5	9.5	205k	82k	21	43	13	5	0.5
0.20	0.20	0.20	4.4e-5	4.6e-5	9.3	201k	82k	20	43	18	6	0.5
0.15	0.20	0.20	4.4e-5	4.6e-5	9.5	186k	82k	20	44	19	7	0.6
0.10	0.20	0.20	4.4e-5	5.6e-5	10.0	153k	82k	20	45	21	7	0.6
1.00	0.46	0.46	8.3e-5	8.3e-5	11.4	106k	22k	42	49	13	5	0.6
0.20	0.43	0.43	8.3e-5	8.3e-5	11.0	116k	22k	40	50	18	6	0.6
0.15	0.42	0.42	8.3e-5	8.8e-5	11.0	112k	22k	40	50	19	7	0.6
0.10	0.42	0.42	8.3e-5	1.0e-4	12.1	66k	22k	39	57	26	7	0.8
1.00	0.98	0.98	1.6e-4	1.6e-4	13.4	52k	7k	77	59	13	5	0.6
0.20	0.78	0.78	1.6e-4	1.6e-4	13.2	67k	7k	70	59	19	6	0.7
0.15	0.77	0.77	1.6e-4	1.6e-4	13.2	63k	7k	70	63	20	7	0.7
0.10	0.76	0.76	1.6e-4	2.5e-4	16.5	15k	2k	65	100	49	7	1.0
1.00	1.65	1.65	3.2e-4	3.2e-4	16.2	22k	3k	130	73	13	5	0.7
0.20	1.37	1.37	3.2e-4	3.2e-4	15.3	37k	3k	115	76	19	6	0.8
0.15	1.35	1.35	3.2e-4	3.2e-4	16.6	26k	3k	110	96	26	7	1.0
0.10	1.33	1.32	3.2e-4	9.3e-4	17.1	3k	0.5k	89	319	208	7	2.0

**Table 6.3.** Extracted Model Parameters at Selected Bias Points at 300 K temperature.

$T_a = 300$ K					$R_E = 2.6$			$R_C = 10.2$				
$V_{CE}$	$J_{CF}$	$J_C$	$J_{BF}$	$J_B$	$R_B$	$r_{be}$	$r_{ce}$	$g_m$	$C_{BE}$	$C_{CB}$	$C_{CS}$	$\tau$
1.00	0.22	0.22	4.6e-4	4.6e-4	8.6	43k	110k	8	35	13	6	0.5
0.20	0.21	0.21	4.6e-4	4.6e-4	7.3	45k	56k	8	35	19	7	0.5
0.15	0.21	0.21	4.6e-4	4.6e-4	7.3	43k	22k	8	35	21	8	0.5
0.10	0.21	0.21	4.6e-4	5.6e-4	7.0	37k	5k	8	35	25	8	0.5
1.00	0.46	0.46	1.1e-3	1.1e-3	9.7	20k	32k	17	40	13	6	0.5
0.20	0.44	0.44	1.1e-3	1.1e-3	8.4	22k	16k	16	39	19	7	0.5
0.15	0.44	0.44	1.1e-3	1.1e-3	8.2	20k	9k	16	39	22	8	0.5
0.10	0.44	0.42	1.1e-3	1.5e-3	7.8	18k	2k	16	39	30	8	0.6
1.00	0.94	0.94	2.2e-3	2.2e-3	11.2	10k	10k	33	48	14	6	0.5
0.20	0.86	0.86	2.2e-3	2.2e-3	9.5	12k	7k	31	46	21	7	0.6
0.15	0.85	0.85	2.2e-3	2.2e-3	9.3	11k	3k	30	45	25	8	0.6
0.10	0.85	0.81	2.2e-3	2.6e-3	8.7	8k	0.8k	29	45	41	8	0.6
1.00	1.68	1.68	3.5e-3	3.5e-3	13.4	7k	4k	57	58	14	6	0.5
0.20	1.46	1.46	3.5e-3	3.5e-3	11.0	8k	2k	51	54	18	7	0.6
0.15	1.44	1.44	3.5e-3	3.5e-3	10.4	8k	1k	50	54	31	8	0.7
0.10	1.43	1.35	3.5e-3	4.1e-3	9.4	4k	0.2k	46	55	67	8	0.8



**Figure 6.4.** Comparison of measured and modeled scattering parameters at 7 K physical temperature for  $J_{CF0} = 0.46$  mA/ $\mu\text{m}^2$  at (a)  $V_{CE} = 500$  mV, (b)  $V_{CE} = 200$  mV, and (c)  $V_{CE} = 100$  mV. Solid lines and markers correspond to the model and measurement, respectively. Data provided from 0.01–40 GHz [70], ©2016 IEEE.



**Figure 6.5.** Room temperature  $50 \Omega$  noise figure referenced to the bondpads of the HBT test structure. For these measurements,  $J_{CF0} = 0.92 \text{ mA}/\mu\text{m}^2$ . (left)  $V_{CE}=100 \text{ mV}$  and (right)  $V_{CE}=50 \text{ mV}$ . Solid and dashed lines correspond to the model and measurement, respectively [70], ©2016 IEEE.

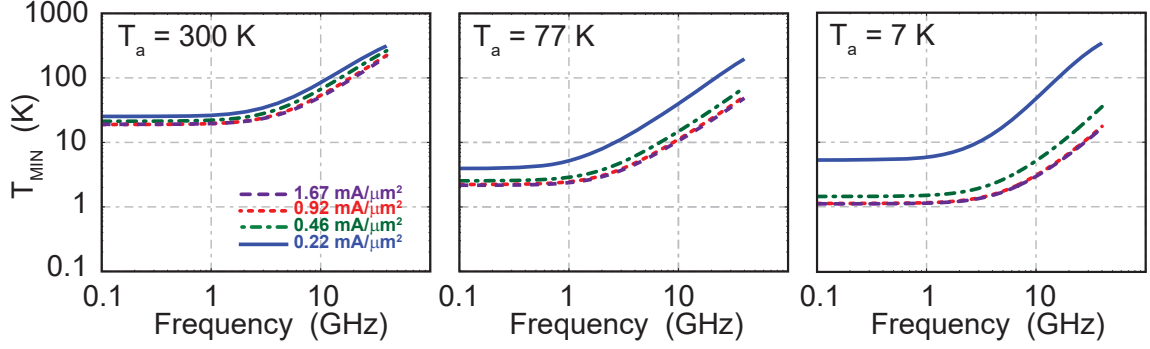
### 6.2.1 Noise Model Agreement with Measurements at Room Temperature

To verify the noise and small signal model at room temperature, first, the noise figure of the SiGe HBT device was measured on wafer using the vector-corrected cold source method [140] and results were compared to model simulations as shown in Fig.6.5. Excellent agreement was observed between simulations and measurements of the noise figure at  $V_{CE}$  as low as 50 mV at room temperature.

After verification of the noise model at room temperature, the noise parameters of the SiGe HBT were extracted as a function of  $V_{CE}$  voltage over a range of current densities and results are described in the following sections.

### 6.2.2 Minimum Noise Temperature

First, the minimum noise temperature ( $T_{MIN}$ ) of the SiGe HBT device was extracted as a function of frequency over a range of current densities. The extracted  $T_{MIN}$  results are shown in Fig.6.6 for the device operating at  $J_{CF0}=0.46 \text{ mA}/\mu\text{m}^2$ . The minimum noise temperature of the device improves by a factor of 15 when cryogenically cooled to 7 K. This result is consistent with the data previously reported in [56, 141].

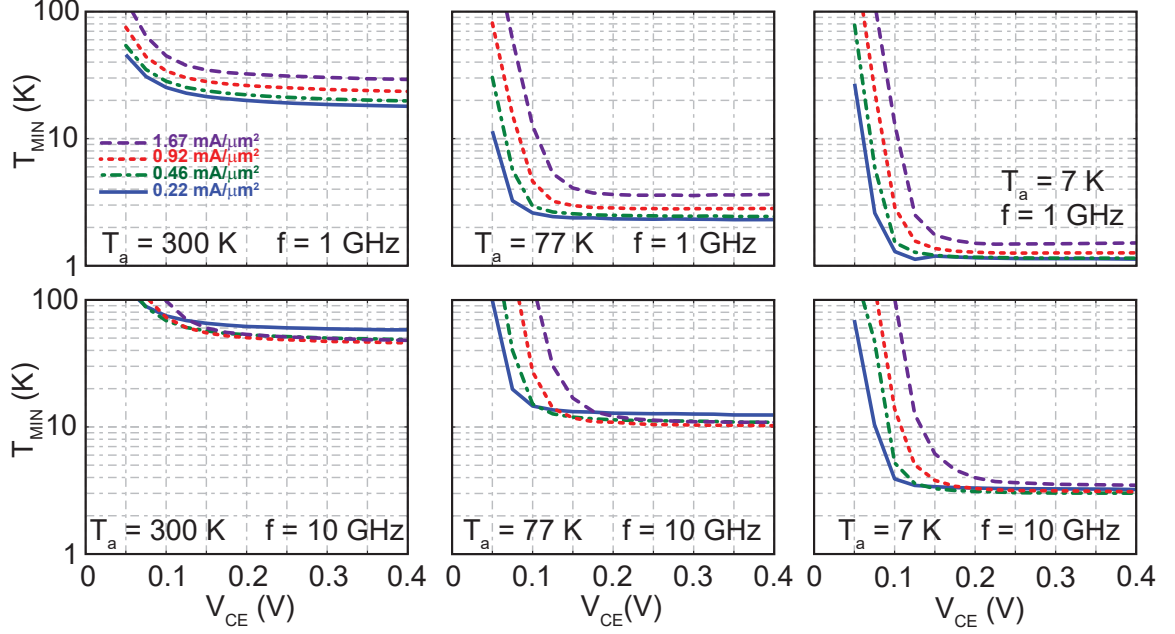


**Figure 6.6.** Minimum noise temperature as a function of frequency at (left) 300 K, (center) 77 K, and (right) 7 K physical temperature. These data correspond to a bias point of  $J_{CF0} = 0.46 \text{ mA}/\mu\text{m}^2$  [70], ©2016 IEEE.

Next, the minimum noise temperature ( $T_{MIN}$ ) was extracted as a function of  $V_{CE}$  voltage at several different current densities. The results are presented in Fig.6.7 for 300, 77, 7 K temperatures at two spot frequencies of 1 GHz and 10 GHz. In Chapter 3, the minimum noise temperature ( $T_{MIN}$ ) of a SiGe HBT was derived as

$$T_{MIN} \approx n_{cF} T_a \left[ g_{mF} r_B \left( 2 - \frac{I_C}{I_{CF}} \right) \left( \frac{f}{f_t} \right)^2 + \sqrt{\frac{1}{\beta_F} \frac{I_B}{I_{BF}} \left[ \frac{I_{CF}}{I_C} \left( 2 \frac{I_{CF}}{I_C} - 1 \right) + \frac{2g_{mF} r_B}{n_{cF}} \right] + \frac{2g_{mF} r_B}{n_{cF}} \left( 2 - \frac{I_C}{I_{CF}} \right) \left( \frac{f}{f_t} \right)^2} \right]. \quad (6.3)$$

It is expected that the minimum noise figure is independent of the  $V_{CE}$  voltage until the point at which the bias dependent parameters ( $f_t$ ,  $I_C$ ,  $I_B$ ,  $C_{CB}$ , and  $r_B$ ) start degrading which was measured to occur at approximately 200 mV. A sharp rise was observed for the  $T_{MIN}$  at lower  $V_{CE}$  voltages due to the degradation of the DC current gain and unity gain cutoff frequency at saturation region. From Fig.6.7, it could be concluded that SiGe HBTs can operate at  $V_{CE}$  voltages as low as 200 mV when biased at low injection region without any significant impact on their minimum noise performance.



**Figure 6.7.** Minimum noise temperature at 1 GHz and 10 GHz for physical temperatures of (left) 300 K, (center) 77 K, and (right) 7 K [70], ©2016 IEEE.

### 6.2.3 Optimum Generator Impedance

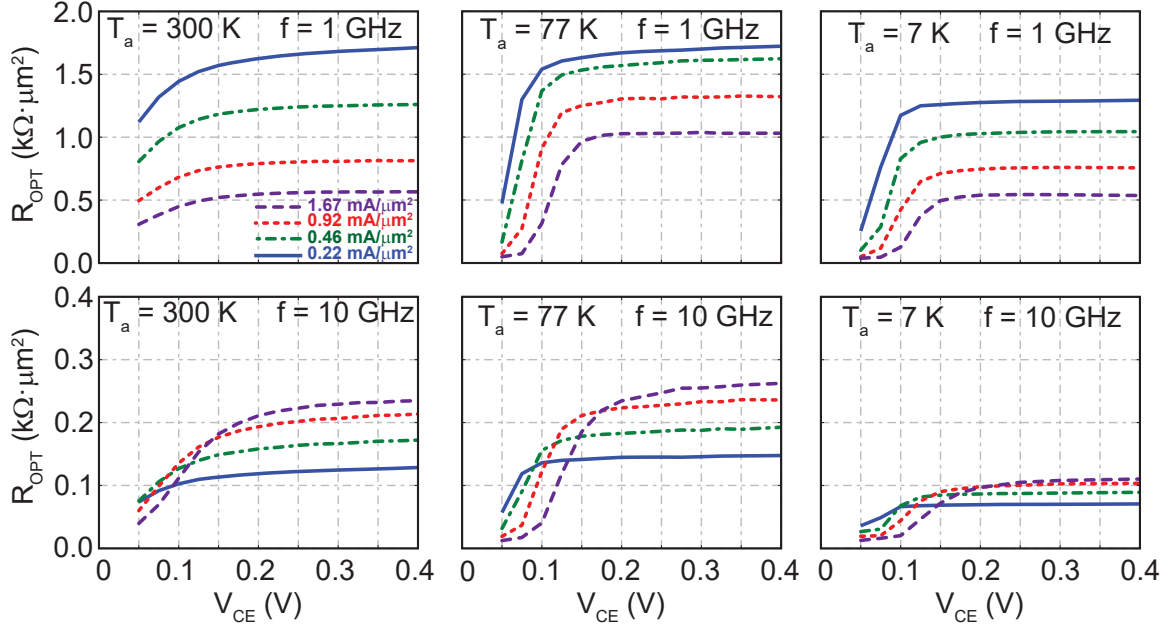
The optimum generator impedance of the device was also extracted as a function of  $V_{CE}$  voltage for several current densities at 300, 77, 7 K temperature at 1 GHz and 10 GHz frequencies. The real and imaginary part of the calculated optimum generator impedance as a function of supply voltages are shown in Fig.6.8 and Fig.6.9.

The optimum impedance of the SiGe HBT was derived for the forward active as well as the near saturation operation in Chapter 3 as

$$\begin{aligned}
 R_{\text{OPT}} \approx & \frac{\beta_{\text{F}}}{g_{\text{mF}}(I_{\text{B}}/I_{\text{BF}} + \beta_{\text{F}}(2 - I_{\text{C}}/I_{\text{CF}})(f/f_{\text{t}})^2)} \\
 & \times [(1/\beta_{\text{F}})(I_{\text{B}}/I_{\text{BF}})[(I_{\text{CF}}/I_{\text{C}})(2(I_{\text{CF}}/I_{\text{C}}) - 1) + (2g_{\text{mF}}r_{\text{B}}/n_{\text{cF}})] \\
 & + (2g_{\text{mF}}r_{\text{B}}/n_{\text{cF}})(2 - (I_{\text{C}}/I_{\text{CF}}))(f/f_{\text{t}})^2]^{1/2}, \quad (6.4)
 \end{aligned}$$

and

$$X_{\text{OPT}} \approx \frac{\beta_{\text{F}}}{g_{\text{mF}}} \frac{I_{\text{CF}}}{I_{\text{C}}} \frac{f}{f_{\text{t}}} \frac{(2 - I_{\text{C}}/I_{\text{CF}})}{(I_{\text{B}}/I_{\text{BF}}) + \beta_{\text{F}}(2 - I_{\text{C}}/I_{\text{CF}})(f/f_{\text{t}})^2}. \quad (6.5)$$

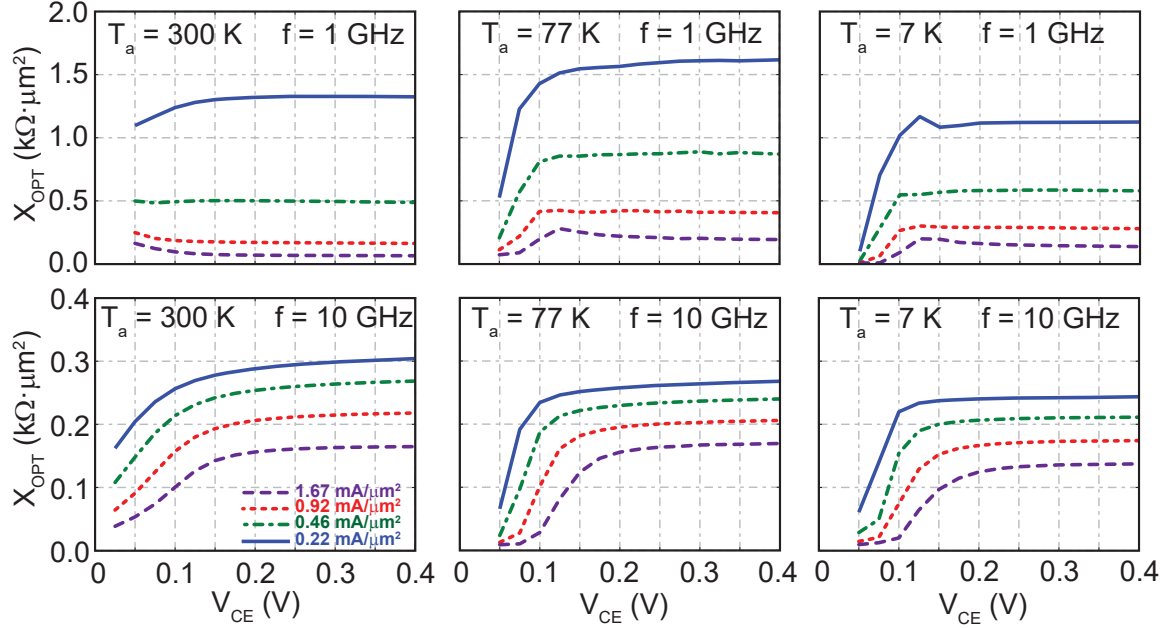


**Figure 6.8.** Optimum generator resistance at 1 GHz and 10 GHz for physical temperatures of (left) 300 K, (center) 77 K, and (right) 7 K [70], ©2016 IEEE.

Thus, a SiGe HBT is expected to have a weak dependence on the collector-emitter voltage for the forward active region and it starts degrading rapidly once the device enters the saturation region. Measurement results presented in Fig.6.8 and Fig.6.9 show that the optimum impedance starts degrading at  $V_{CE}$  voltages approximately equal to 200 mV which is consistent with the theory presented in Chapter 3. The reduction of the impedance at cryogenic temperature is more pronounced than the room temperature results which is due to the sharper reduction of the base current at cryogenic temperatures at saturation region in comparison with that of the room temperature.

#### 6.2.4 Noise Resistance

The noise resistance of the device was extracted as a function of  $V_{CE}$  and results are shown in Fig.6.10 for several current densities at 1 and 10 GHz frequency points. The noise resistance equation was also derived earlier in Chapter 3 as



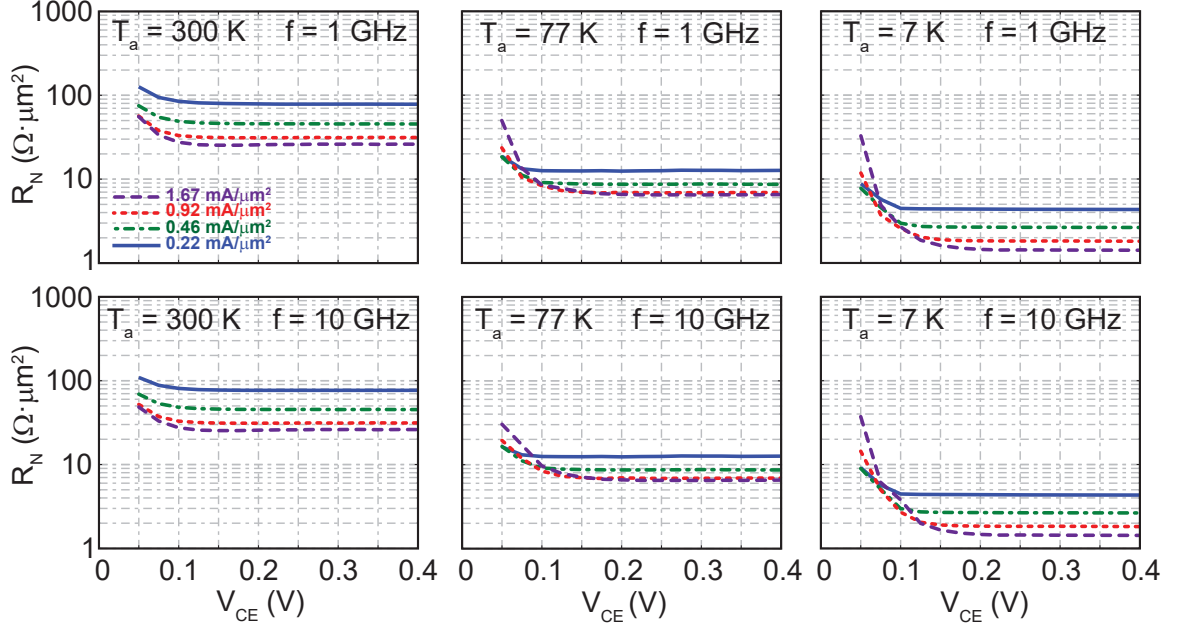
**Figure 6.9.** Optimum generator reactance at 1 GHz and 10 GHz for physical temperatures of (left) 300 K, (center) 77 K, and (right) 7 K [70], ©2016 IEEE.

$$R_N \approx \frac{T_a}{T_0} \left( r_B + \frac{n_{cF}}{2g_{mF}} \frac{I_{CF}}{I_C} \left( 2 \frac{I_{CF}}{I_C} - 1 \right) \right). \quad (6.6)$$

The measurement results are consistent with equations 6.6 which shows the frequency-independent behavior of  $R_N$  at forward active region. The noise resistance is also independent of the collector to emitter voltage at forward active region and starts rising as the device enters the saturation region which is due to the rapid drop in  $I_C$ .

### 6.2.5 Associated Gain

The associated gain ( $G_{ASSOC}$ ) of the SiGe HBT was extracted from the model. The associated gain is calculated for the case in which the DUT is matched to the optimum noise impedance at the input and for the power match at the output. The  $G_{ASSOC}$ s was extracted with respect to the collector to emitter voltage at several current densities and temperatures for 1 GHz and 10 GHz frequency points. The results are shown in Fig.6.11.



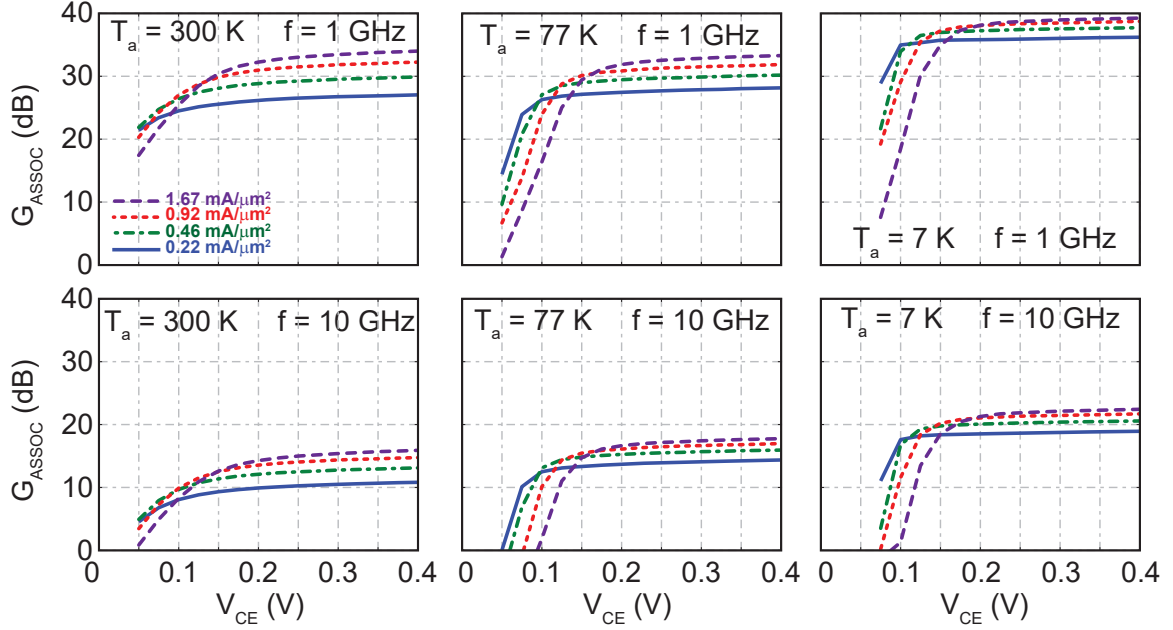
**Figure 6.10.** Noise resistance at 1 GHz and 10 GHz for physical temperatures of (left) 300 K, (center) 77 K, and (right) 7 K [70], ©2016 IEEE.

In Chapter 3, The  $G_{ASSOC}$  was calculated for the forward active and near saturation operation as

$$G_{ASSOC} \approx \frac{f_t}{f} \frac{n_{cF}/2}{2\pi f C_{CB} r_B} \times \sqrt{\frac{1}{\beta_F} \frac{I_B}{I_{BF}} \left( \frac{I_{CF}}{I_C} \left( 2 \frac{I_{CF}}{I_C} - 1 \right) + 2 \frac{g_{mF} r_B}{n_{cF}} \right) + 2 \frac{g_{mF} r_B}{n_{cF}} \left( 2 - \frac{I_C}{I_{CF}} \right) \left( \frac{f}{f_t} \right)^2}, \quad (6.7)$$

which predicts the gain to be independent of the  $V_{CE}$  voltage for the forward active region and starts degrading at low supply voltages when the device enters the saturation region. The measurement results presented in Fig.6.11 are consistent with the theory described in Chapter 3. The degradation in the gain at low supply voltages is due to the drop in the  $f_t$  and the increase of  $C_{CB}$  of the device operating in saturation. It is also important to note that the associated gain of the device at forward active region is higher than 10 dB which results in the cascaded noise temperature to





**Figure 6.11.** Associated gain at 1 GHz and 10 GHz for physical temperatures of (left) 300 K, (center) 77 K, and (right) 7 K [70], ©2016 IEEE.

be approximately equal to the minimum noise temperature which makes it practical to make high gain LNAs with noise temperature approaching the  $T_{MIN}$  [141].

### 6.3 Summary

In this chapter, the experimental results of a SiGe HBT operating at 7, 77, and 300 K temperatures were presented. A small-signal and noise model were developed based on the measurement data and it was concluded that the noise parameters and the associated gain of a SiGe HBT device is almost independent of the collector to emitter voltage. Based on the value of the current density, the  $V_{CE}$  voltage could be selected as low as 100 to 200 mV without any significant impact on the noise performance while dissipating minimal DC power.

Using the small-signal and noise models developed in this chapter, low noise amplifiers with microwatt level DC power consumption could be designed and implemented which will be discussed in the later chapters of this dissertation.

## CHAPTER 7

### LIMITATIONS OF SIGE HBT NOISE MODEL AT HIGH INJECTION REGION

Modern high-speed integrated SiGe HBT circuits require devices to operate at high current densities to achieve higher unity-gain cutoff frequencies ( $f_t$ ). However, several physical mechanisms can cause severe degradation in the device performance at high current densities which impacts the  $g_m$ ,  $\beta$ , and  $f_t$  of the device significantly and ultimately degrade the noise performance [78, 101]. Thus, careful study of the noise and small signal performance of SiGe HBTs are required prior to designing circuits operating at high injection region.

High injection occurs when the number of mobile carriers becomes comparable or exceeds the number of ionized doping levels in the base, collector, or emitter of a SiGe HBT. The onset of this phenomena is a function of doping concentration and typically happens at current densities above  $1 \text{ mA}/\mu\text{m}^2$  in a modern SiGe HBT [78].

So far, there has been a number of SiGe HBT LNAs reported in the literature which operate at current densities below  $1 \text{ mA}/\mu\text{m}^2$  presenting a good match between the models and measurements [68, 70, 141]. However, at current densities above  $1 \text{ mA}/\mu\text{m}^2$ , the standard SiGe HBT models predict an optimistic noise performance resulting in a disagreement between the measurements and simulations [67, 142].

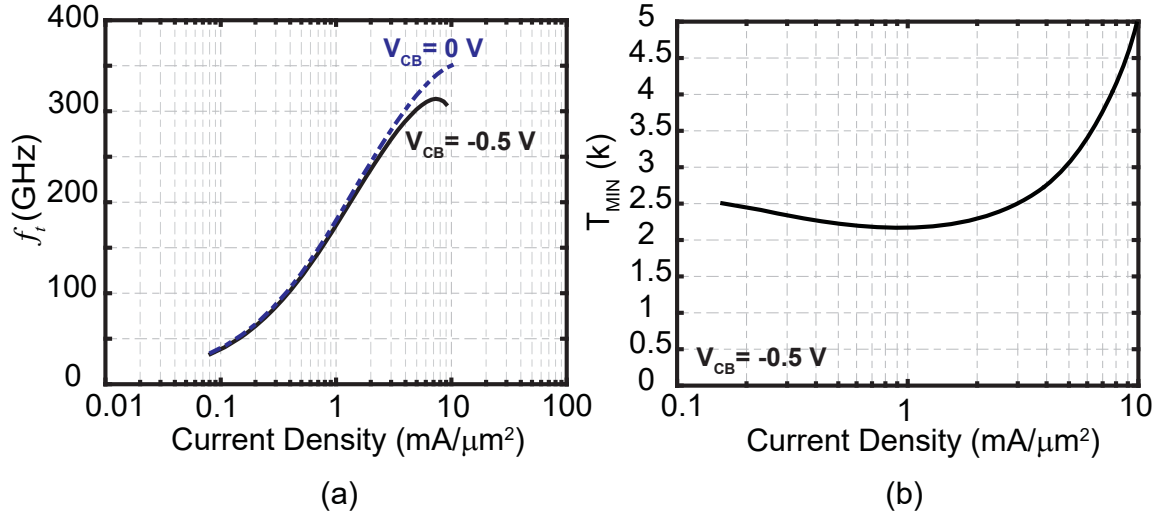
In this chapter, we try to systematically understand the cause of the possible disagreement between the noise model predictions and measurements at current densities above  $1 \text{ mA}/\mu\text{m}^2$ . To do so, SiGe devices from the TowerJazz SBC18H3 technology process were selected for this study. First, the small signal and noise models were

developed over a wide range of current densities. Leveraging these models, several SiGe HBT LNAs were designed, optimized, and implemented for operation at various current densities and measurement results were compared to model simulations. In addition, several de-embedding structures were designed and implemented to enable an accurate measurement of the passive components in the amplifier signal path so as to prevent any error in the modeling of the matching networks in the simulations. The details of the modeling, design, implementation, and the interpretation of the results follow in the next sections.

## 7.1 Noise Prediction at High Current Densities

Leveraging the small-signal and noise model standard extraction techniques described in Chapter 5, we were able to develop models that could predict the noise performance of SiGe HBT amplifiers within 1 K of the measurements for the low injection operation (See Chapter 8). However, there could be several possible reasons which may result in a disagreement between the models and experimental results at high current densities. Some possible causes of the model limitations could be due to unknown noise sources appearing at the high injection operation, the onset of higher order effects at high current densities such as Kirk effect [101] which are not fully captured in the standard model (See Chapter 2), possible bias dependent behavior of the emitter and collector parasitic resistances at high currents, self-heating, any inaccuracy in the parameter extraction procedure, or other effects that are neglected in the model.

To understand the root cause of the SiGe HBT model limitations at high current densities, first, we modeled a SiGe HBT at a wide range of current densities and examined the sensitivity of the models to the parasitic resistances. The emitter resistance acts as a degeneration for a SiGe HBT and has a significant impact on the device modeling. In particular, the intrinsic transconductance ( $g_m$ ) of an HBT is



**Figure 7.1.** (a) The unity gain cutoff frequency as a function of current density for a SiGe HBT device biased at  $V_{CB}=0 \text{ V}$  and  $V_{CB}=-0.5 \text{ V}$  at 7 K ambient temperature. (b) Modeled minimum noise temperature of the SBC18H3 device at 3 GHz as a function of current density.

proportional to the  $1/(1 - GM \times r_e)$ , where  $GM$  is the extrinsic transconductance of the device. Thus, an accurate extraction of the emitter resistance is expected to become important especially at high current densities where the  $GM$  is large. In addition, as shown in Chapter 5, the emitter resistance is the first parameter that is subtracted from the S-parameter data and any error associated with that could propagate to the extraction of the intrinsic device parameters and leads to an inaccurate model. Consequently, we expect that errors in the emitter resistance extraction could be one of the contributing factors in the model inaccuracy at high current densities.

The SiGe HBT models were used to design six different LNAs providing similar frequency responses while operating at different current densities with different input transistor sizes. The performance of these LNAs were characterized and results were compared to the models to investigate the possible reasons for any mismatch between the model/measurement data at high currents.

## 7.2 SiGe HBT Extracted Device Parameters

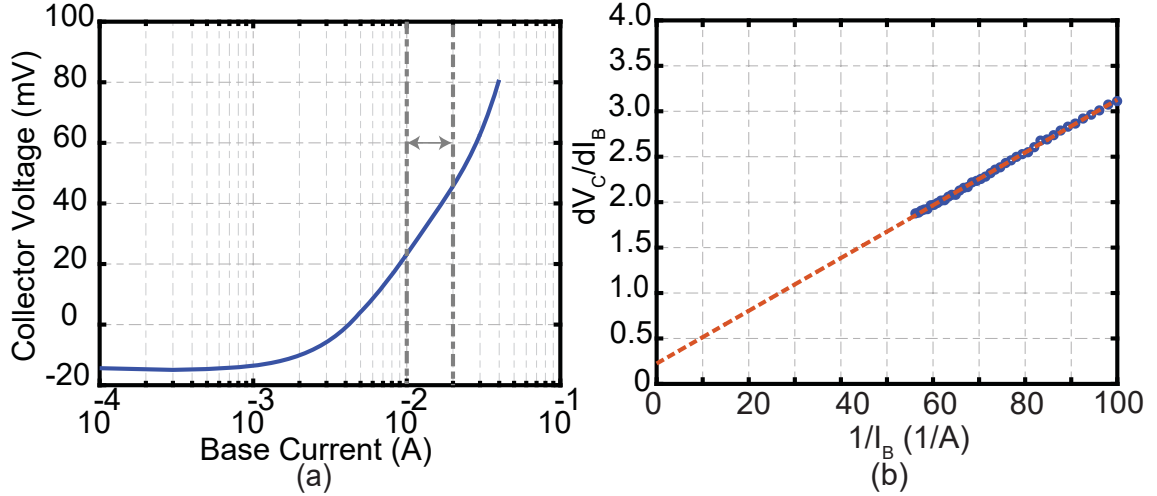
SiGe HBT devices from the SBC18H3 technology process were modeled at cryogenic temperatures. A schematic diagram of the standard SiGe HBT small signal and noise model was presented in Chapter 2 (See Fig. 2.5). The model parameters were extracted for a  $10 \times 0.13 \mu\text{m}^2$  HBT operating at 7 K temperature. The measurements were carried out using the cryogenic probe station setup described in Chapter 4. Using the on-wafer measurement results, the unity gain cutoff frequency was extrapolated for a device biased at base-collector voltages ( $V_{CB}$ ) of 0 V and -0.5 V as shown in Fig.7.1.(a). The measurement results show that the device can provide a peak  $f_t$  of more than 300 GHz at 7 K temperature at current densities between 6 to  $8 \text{ mA}/\mu\text{m}^2$  when biased at  $V_{CB} = -0.5 \text{ V}$  which is the operating point selected for the rest of the measurements in this chapter. The  $f_t$  of the device rolls off significantly for higher current densities due to the Kirk effect [101].

The model parameters were determined following the approach described in Chapter 5. The extracted parameters for a  $10 \times 0.13 \mu\text{m}^2$  device operating at  $J_C = 0.9 \text{ mA}/\mu\text{m}^2$  and  $V_{CC} = 500 \text{ mV}$  are shown in Table.7.1.

The emitter resistance was extracted using the three methods described in Chapter 5. The open-collector technique was carried out using the DC measurement of the collector voltage as a function of the base current for the case in which the collector current was set to zero. Fig.7.2 shows the measurement results. The resistance value was calculated by the extrapolation of the  $dV_C/dI_C$  for the base currents approaching infinity. The base current selected<sup>1</sup> for the extrapolation was in the range of 10– $18 \text{ mA}/\mu\text{m}^2$ . Using the open-collector method, the extracted  $r_e$  value was calculated to be  $0.2 \Omega$  for a device with a size of  $10 \times 0.13 \mu\text{m}^2$ .

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<sup>1</sup>At higher base currents, a change in the slope of the  $V_C$  as a function of  $I_B$  was observed which could be attributed to the excess injection effect which could result in an error in the resistance extraction [143].

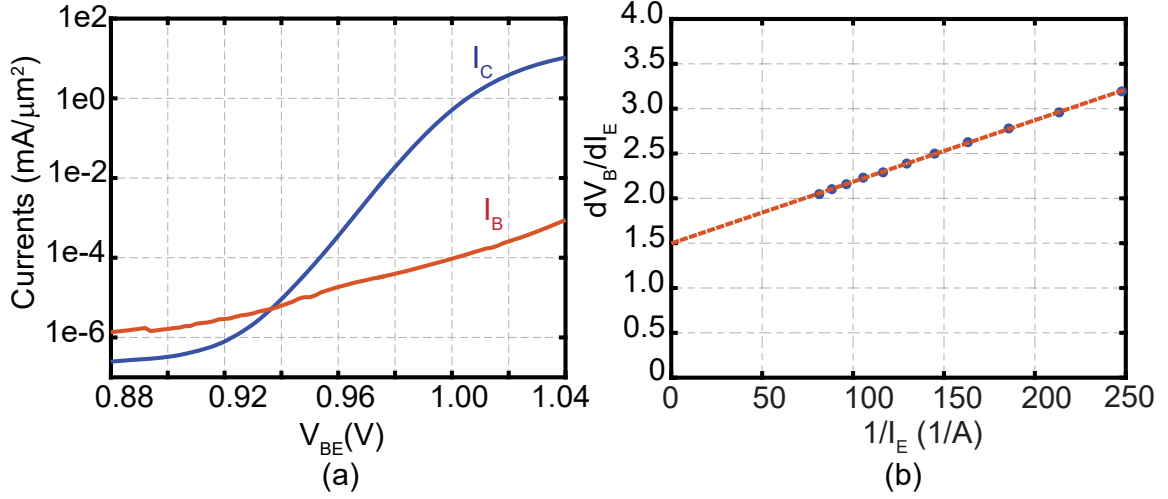


**Figure 7.2.** Emitter resistance extraction using the open-collector method for a  $0.13 \times 10 \mu\text{m}^2$  SiGe HBT. (a) Collector voltage as a function of base current. The specified area on the plot shows the extrapolation range of the base current. (b) Data extrapolation to calculate the emitter resistance value.

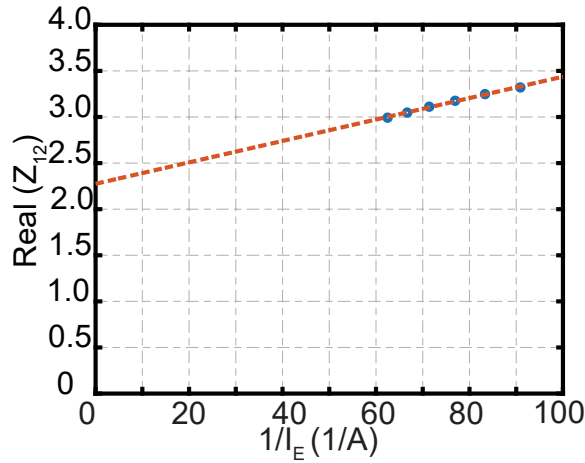
The emitter resistance was also extracted using the Gummel data. Fig.7.3 shows the base and collector currents as a function of the base-emitter voltage. The  $r_e$  was extracted for the  $V_{BE}$  in the range of 1.02–1.04 V by extrapolating the  $dV_B/dI_E$  for the  $1/I_E$  approaching zero. The resistance value was calculated to be  $1.5 \Omega$ .

In addition, the active sweep measurement data was used for the emitter resistance extraction as described in Chapter 5. Fig.7.4 shows the measurement data and the emitter resistance was found to be  $2.2 \Omega$ .

Unlike the emitter and collector resistances, the base resistance ( $r_B$ ) is expected to be bias dependent [129] and the value is extracted using the S-parameters of the device in forward active mode. First,  $r_B$  was extracted using the Y-parameters of the two-port network using  $\lim_{\omega \rightarrow \infty} R(\frac{1}{Y_{11}})$  which is insensitive to the error in the substrate capacitor extraction. It was found that the extracted base resistance increases with current density which is not a physically meaningful phenomena and is due to the added non-quasi static resistance value to the extracted  $r_B$  [144]. Thus, the base resistance was extracted using an alternative method leveraging the Z-parameters of



**Figure 7.3.** Emitter resistance extraction using the Gummel curve data for a SiGe HBT from the TowerJazz SBC18H3 technology with a size of  $1.3 \mu m^2$ . (a) Collector and base currents as a function of base-emitter voltage. (b) Data extrapolation to calculate the emitter resistance value.

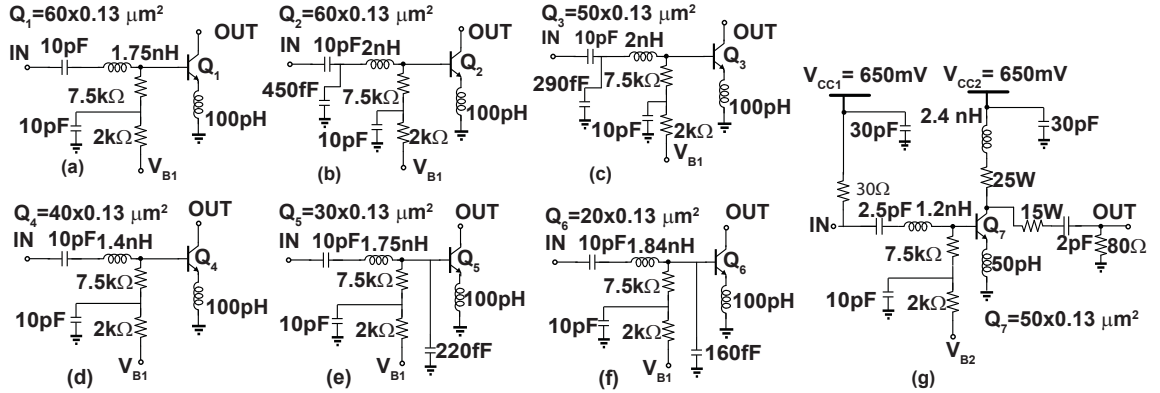


**Figure 7.4.** (a) Emitter resistance extraction using the active sweep method for a  $0.12 \times 18 \mu m^2$  SiGe HBT.

the device. The  $r_B$  could be calculated as  $\Re\{Z_{11} - Z_{12}\}$  after subtracting the extracted  $C_{CS}$ ,  $r_e$ , and  $r_C$  from the two port S-parameter data. Extraction of  $r_B$  using the Z-parameter method is susceptible to the errors associated with the  $r_e$  and  $C_{CS}$  at low

**Table 7.1.** Extracted Model Parameters for a  $10 \times 0.13 \mu\text{m}^2$  SiGe HBT Operating at  $J_C = 0.9 \text{ mA}/\mu\text{m}^2$  and  $V_{CC} = 500 \text{ mV}$  at Cryogenic Temperature.

Method	$R_B$	$R_E$	$R_C$	$C_{CB}$	$C_{CS}$	$C_{BE}$	$g_m$	$\tau$
	$\Omega$	$\Omega$	$\Omega$	fF	fF	fF	S	pS
Open Collector	6.5	0.2	7.4	25.5	12.5	69.7	0.12	1.5
Gummel Data	6.4	1.5	6.1	26.9	12.5	94	0.43	3.9
Active Sweep	6.4	2.3	1.2	26.9	12.5	121.7	0.55	5.6



**Figure 7.5.** (a-f) Schematic diagrams of the first stage of the SiGe Jazz LNAs. (g) Schematic diagram of the second stage of the amplifiers. The second stage was designed to operate at  $0.3 \text{ mA}/\mu\text{m}^2$ . All the passive components in the first and second stages are implemented on chip.

current densities where  $g_m < 100 \text{ mS}$ . However, it can provide a good estimate<sup>2</sup> of the base resistance at high currents [56].

Once the model parameters were extracted, the minimum noise temperature ( $T_{MIN}$ ) of the SiGe HBT was calculated. The results are presented in Fig.7.1.(b) as a function of current density showing that  $T_{MIN}$  stays less than 2.5 K for current densities between  $0.1$  to  $3 \text{ mA}/\mu\text{m}^2$ .



### 7.3 SiGe HBT LNAs Operating at Various Current Densities

Leveraging the small signal and noise models described in the previous section, six different two-stage low noise amplifiers were designed for a frequency range of 2-4 GHz and were optimized for operation at various current densities. The amplifiers were designed for current densities of 0.3, 0.5, 1, 2, 4, and 6 mA/ $\mu\text{m}^2$  corresponding to an  $f_t$  in the range of approximately 100 to 300 GHz. The design was carried out such that the second stages of all the LNAs were identical and operating at 0.3 mA/ $\mu\text{m}^2$ . The first stages were optimized to achieve a good noise match in the 2-4 GHz frequency range leveraging slightly different matching networks for LNAs biased at different operating points.

The input matching network of each LNA was designed such that the amplifiers were matched to the optimum noise impedance at the desired frequency band so that the overall noise could be estimated to be equal to the minimum noise temperature of the LNA. Fig.7.5.(a-f) shows the first stage of the six LNAs with the input matching networks associated with each design.

The interstage matching networks were identical for all amplifiers and were designed to shape the gain at the 2-4 GHz frequency range. The second stage and the output matching network, which are identical in all six LNAs, were optimized to provide further amplification and a 50  $\Omega$  match to the output of the LNA. Fig.7.5. (g) shows a schematic diagram of the second stage of the amplifiers.

The LNAs were implemented using the TowerJazz SBC18H3 technology and Fig.7.6 shows a photo of the chips. Several de-embedding structures were also designed for the input matching networks so that their exact scattering parameters could be measured on wafer and included in the simulation files in order to prevent any inaccuracy in the noise prediction from the passive element models.

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<sup>2</sup>The error in the extraction of a 1  $\Omega$  base resistance is within %10 for the case in which  $\epsilon_{CS}/C_{CB} = 0.01$  as described in [56].

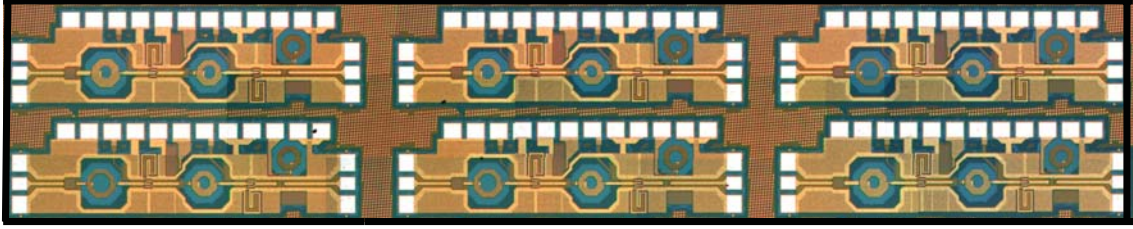


Figure 7.6. A photo of the integrated circuit LNAs and de-embedding structures using the TowerJazz SBC18H3 technology.

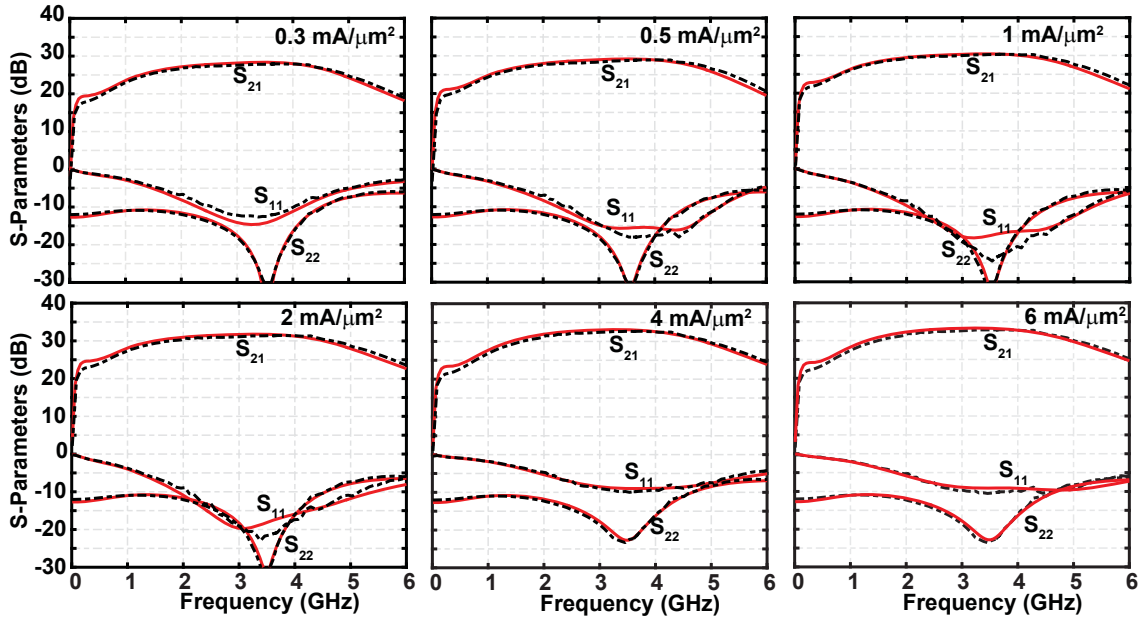
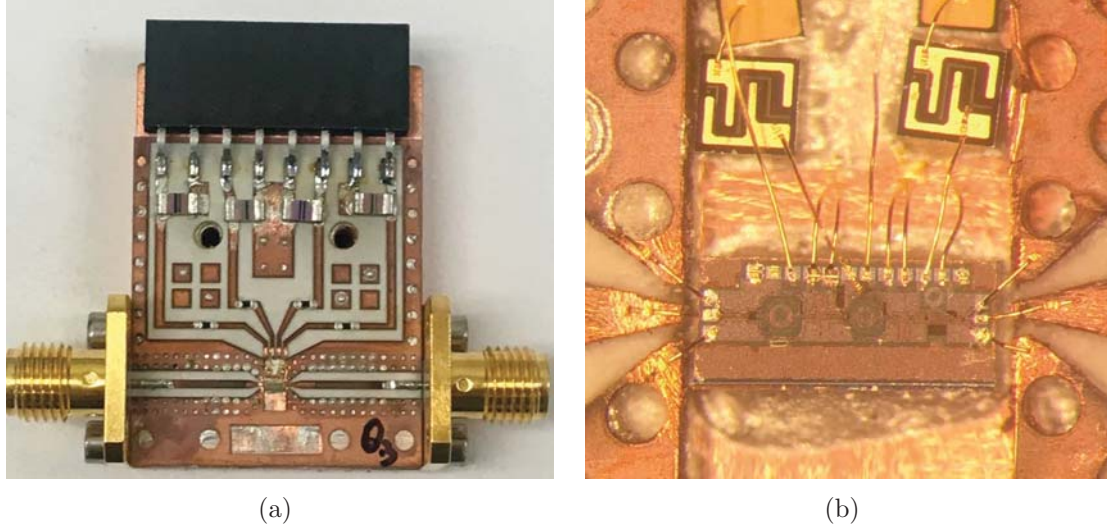


Figure 7.7. Scattering parameter measurements at 7 K temperature.

## 7.4 Experimental Results

Prior to the noise measurement, the LNAs were first tested on wafer. The scattering parameters of the LNAs were measured at 7 K temperature along with the de-embedding structures. Measurement results were compared to the small-signal model predictions shown in Fig.7.7. An excellent agreement was observed between measurements and simulations for all the amplifiers.

After on-wafer measurements, the amplifiers were packaged in six identical copper blocks. Fig.7.8 shows a photo of one of the packaged LNAs as well as a close up picture



**Figure 7.8.** (a) The LNA assembly. (b) A photo of the LNA chip mounted inside a cutout on the printed circuit board.

of the amplifier IC mounted on the copper block. A printed circuit board was fabricated using the Rogers RT/Duroid 6002 laminate substrate. The board was patterned using an LPKF ProtoLaser machine [145]. The LNAs include on-chip input/output matching networks and no off-chip matching was needed. Input and output  $50\ \Omega$  grounded co-planar wave-guides (GCPW) were implemented on the PCB for the signal path. The DC bias lines were bypassed using  $68\ fF$  wire bondable and  $1\ \mu F$  surface mount thick film capacitors along with  $10\ \Omega$  resistors between them to prevent any resonance in the bypass network. The input and output SMA connectors were bolted to the copper block to facilitate the cryogenic measurements. The packaged LNAs were tested one by one inside a cryostat at  $16.5\ K$  temperature. The noise measurement was carried out using the cold attenuator method [123] described in Chapter 4.

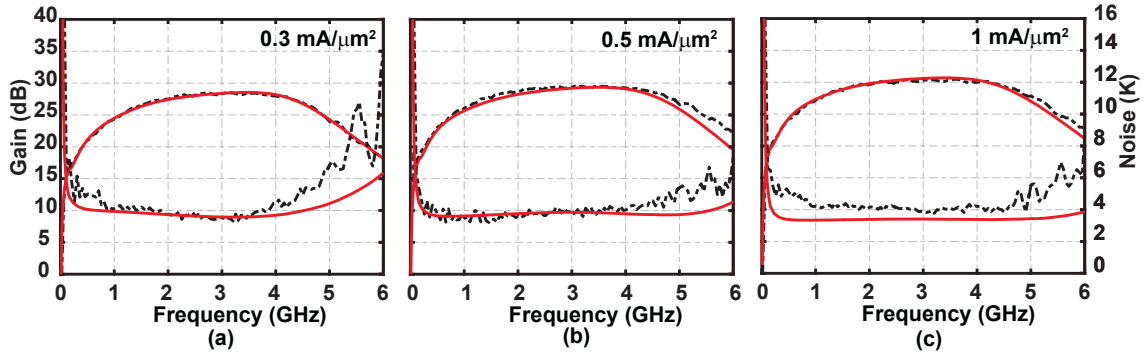
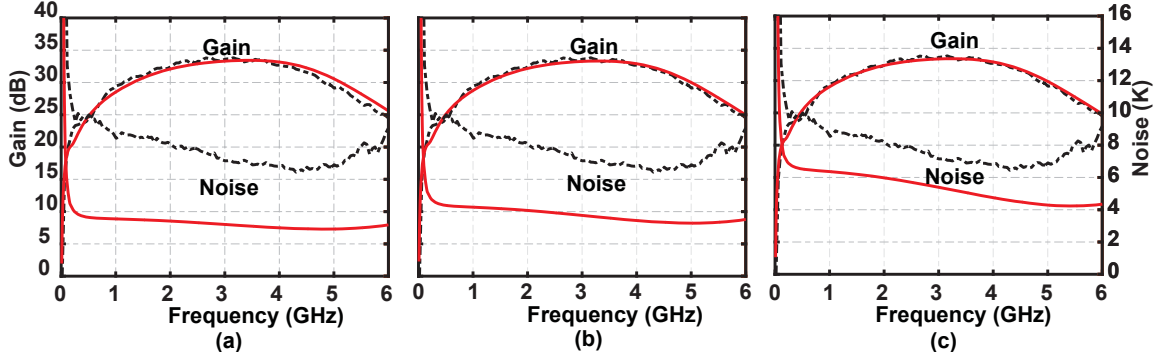


Figure 7.9. Gain and noise temperature of the LNAs at 16.6 K physical temperature.

## 7.5 Discussion

The measurement data was compared to the extracted models for the three different cases of emitter resistance extraction (Gummel curves, open-collector method, and the active sweep measurements). It was found that for the current densities below  $1 \text{ mA}/\mu\text{m}^2$ , the model is not very sensitive to the emitter resistance values extracted from the three different methods. This result is consistent with our hypothesis described in Section 7.1. An agreement within 1.5 K was achieved between the simulations and measurements for the LNAs operating at 0.3, 0.5, and  $1 \text{ mA}/\mu\text{m}^2$  using all three models. Fig.7.9 shows an example comparison between the measurements and simulations for the model with the open-collector extraction technique for the calculation of the  $r_e$ .

The emitter resistance value plays a significant role in the noise prediction for the LNAs operating at currents above  $1 \text{ mA}/\mu\text{m}^2$  as it directly impacts the extraction of the transconductance ( $g_m$ ) as described in Section 7.1. The measurement/model comparison plots for the three different models with various emitter resistance extraction techniques are shown in Fig.7.10. The  $r_e$  extracted from the active sweep measurement as well as the Gummel curve provide a larger value ( $2.2 \Omega$  and  $1.8 \Omega$ , respectively) than the open-collector method ( $0.2 \Omega$ ) which results in an over estimation of the device transconductance ( $g_m$ ). The expected noise temperature from



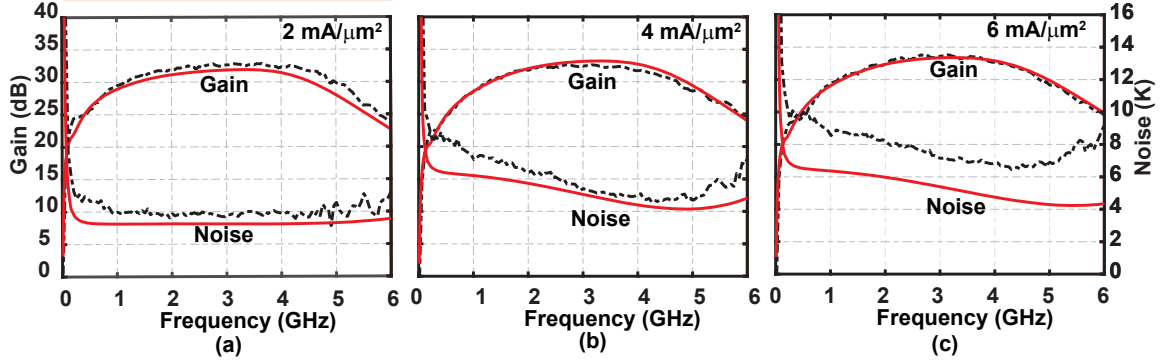
**Figure 7.10.** Gain and noise temperature of the LNA operating at  $J_C = 6mA/\mu m^2$  at 16.6 K physical temperature. Emitter resistance extracted using the (a) active sweep data. (b) Gummel curves (c) open-collector method.

these two models are approximately 4 K lower than the measurements as shown in Fig.7.10.(a–b). On the other hand, the open-collector method provide a smaller value for the emitter resistance which result in a better match within 2 K between simulation and measurements. Although a better agreement is achieved using this method, it is believed that the emitter resistance extraction may only be a part of the issue associated with the models at high current densities. More investigation is needed to understand other contributing factors to the model/measurement disagreement at high injection operation.

The measurement data was compared to the model with the  $r_e$  extracted from the open-collector data for the LNAs operating above  $1 mA/\mu m^2$  and results are shown in Fig.7.11. An excellent agreement at current densities below  $4 mA/\mu m^2$  was observed and at higher current densities, the model prediction is within 2 K of the measurement results.

## 7.6 Summary

In this chapter, the standard SiGe HBT noise model was studied at high current densities to investigate any probable reasons for the inaccuracy of the models at high injection region. Several SiGe HBT low noise amplifiers were designed and



**Figure 7.11.** Gain and noise temperature of the LNAs at 16.6 K physical temperature.

implemented leveraging the SBC18H3 technology process for the operation at current densities ranging from 0.3 to  $6 \text{ mA}/\mu\text{m}^2$ . Different methods for the emitter resistance extraction were used and we found the open-collector method provides a better match between the models and measurements. Further investigation is needed to understand the physical limitations of the other extraction techniques at high current density operations.

## CHAPTER 8

# ULTRA LOW-POWER CRYOGENIC LOW NOISE AMPLIFIERS

In this chapter, the design and implementation of several different low-power low noise amplifiers are described. The amplifiers were designed leveraging the custom cryogenic models presented in Chapter 6–7. Discrete transistor LNAs as well as integrated circuit amplifiers were designed and implemented and the measurement results are compared to simulations to validate the models developed in Chapter 6–7. The content of this chapter summarizes part of the results published in [70], [67], and [68].

### 8.1 Example Design: A Proof-of-Concept Low-Power Discrete Transistor SiGe LNA

SiGe HBTs are expected to be able to operate at near saturation region with no significant impact on their noise and small signal performance while running from a very low supply voltage as described in Chapter 6. To validate this finding, a proof-of-concept low noise amplifier was designed and implemented using discrete SiGe HBTs from the GF BiCMOS8HP technology process. The details of the design procedure, implementation, and measurement results will follow in this section.

#### 8.1.1 LNA Design

Leveraging the SiGe HBT models developed in Chapter 6, a two stage low noise amplifier was designed as a proof of concept using discrete SiGe HBT transistors from

the GF BiCMOS8HP technology process. The amplifier was designed<sup>1</sup> to operate at 1.8 to 3.6 GHz frequency range [70]. A schematic diagram of the LNA is shown in Fig.8.1. The design of the LNA was carried out using the NI AWR design environment. The gain of the LNA was expected to be better than 27 dB and the noise was simulated to be less than 5 K over the entire frequency band.

The first stage transistor was sized to be  $3 \times 18 \times 0.12 \mu m^2$  carrying 0.75 mA DC current to provide an optimum impedance close to  $50 \Omega$ . The first stage transistor was inductively degenerated to provide a real impedance at the input to help with the simultaneous noise and power match. An input matching was designed to provide noise and power match over the desired frequency range using transmission lines. The base of the input transistor was designed to be biased through a shunt stub that was placed for the input matching purpose. The base DC voltage line was DC decoupled through  $33 fF$  and  $1 \mu F$  wire bondable and surface mount capacitors, respectively. The collector of the first stage was terminated with a  $68 \Omega$  shunt resistor followed by an interstage matching network which helps shaping the gain at high frequencies.

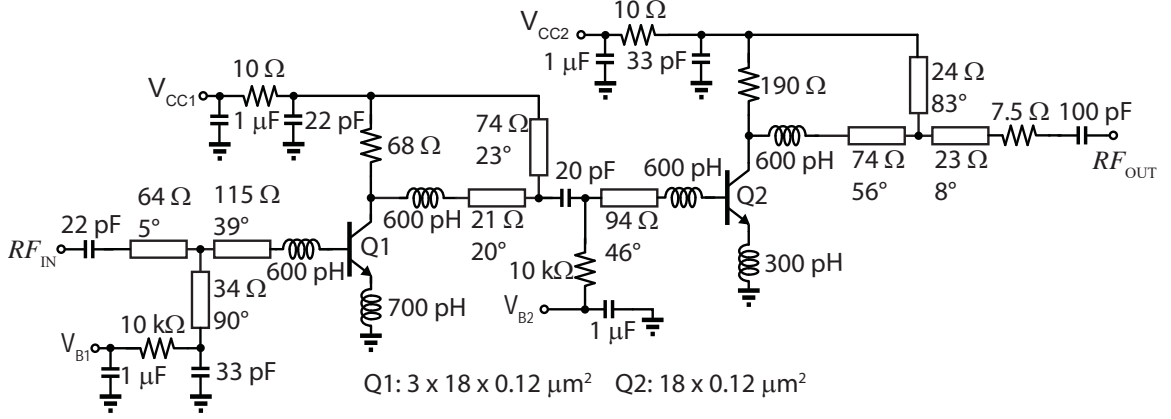
The second stage transistor was sized to be  $1 \times 18 \times 0.12 \mu m^2$  operating at 0.68 mA DC current. The base of the second stage transistor was biased through a  $10 k\Omega$  shunt resistor which was DC decoupled using a surface mount  $1 \mu F$  capacitor. The output matching network was designed to provide  $50 \Omega$  impedance at the output.

Realistic bond wire inductance values were taken into account for the connections between the transistors and the input/output transmission lines and were absorbed into the design of the matching networks. The collector of the first and second stage transistors were biased through a bypass network including a  $33 fF$  and a  $1 \mu F$  capacitor with a  $10 \Omega$  resistor in between to damp any probable resonance between them.

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<sup>1</sup>The design and implementation of this amplifier was carried out by Wei-Ting Wong.



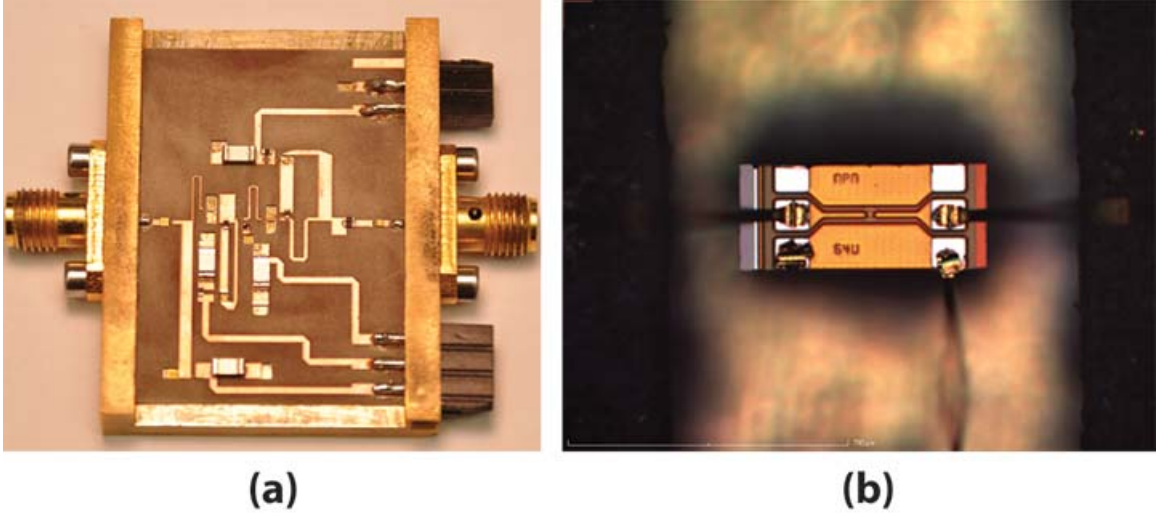


**Figure 8.1.** Schematic diagram of the SiGe LNA. Discrete transistors from the GF BiCMOS8HP process were used. All inductors were realized using bond wires. The  $1 \mu\text{F}$  capacitors were realized using thick-film surface mount devices, whereas all other capacitances were implemented with thin-film bond-able metal-insulator-semiconductor capacitors. Standard surface mount resistors were employed for biasing and damping purposes [70], ©2016 IEEE.

### 8.1.2 Experimental Results

The amplifier was implemented using the discrete SiGe HBT devices from the GF BiCMOS8HP process. A Photo of the assembly is shown in Fig.8.2. The matching networks were implemented on an RT/Duroid printed circuit board. The SiGe HBT transistors were mounted in the cutouts on the PCB and were connected to the transmission lines on the board using gold bond wires. Fig.8.2.(b) shows a close up picture of the SiGe HBT inside the package wire bonded to the PCB.

Once the assembly was done, the LNA was mounted inside a cryostat for testing at cryogenic temperatures. Fig.8.3 shows a block diagram of the measurement setup. The cryostat has two channels, one for the scattering parameters measurement and the other featured for the noise measurement using the cold attenuator method [123]. The cryostat was previously calibrated for the input loss, as described in Section.4.4, and is believed to provide an accuracy in the range of  $\pm 1 \text{ K}$ . Everything within the cryostat was heatsunk to the 15 K cold plate using indium foil and oxygen-free high

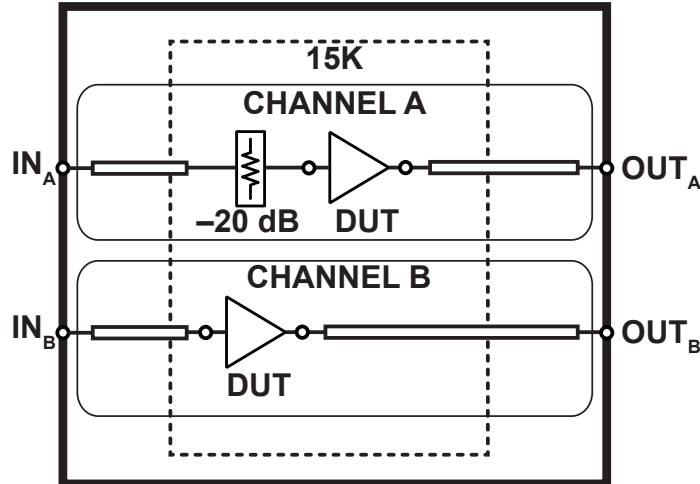


**Figure 8.2.** (a) The LNA assembly. (b) A close up photo of the first stage transistor mounted in a cutout in the pcb for well controlled wirebond lengths [70], ©2016 IEEE.

thermal conductivity copper heat straps. Temperature sensors were mounted on the LNA and the attenuator for accurate temperature readings.

The measurement was performed at a physical temperature of 15 K and the LNA was initially biased at  $I_{C1}=0.75$  mA,  $I_{C2}= 0.68$  mA,  $V_{CC1} = V_{CC2}=200$  mV which corresponds to  $290 \mu\text{W}$  DC power dissipation. The experimental results are shown in Fig.8.4 along with simulations. The amplifier provided more than 27 dB of gain and a noise temperature in the range of 3.4 to 5 K over the desired frequency band. A good agreement between simulations and models were obtained.

To validate the cryogenic models developed at low  $V_{CE}$  ranges (described in Chapter 6), the amplifier was tested over a wide range of supply voltages starting from 500 mV down to 75 mV and the noise and gain were compared to model predictions at 2.5, 3, and 3.5 GHz frequency points. Fig.8.5 shows measurements results along with simulations. From the results, it could be concluded that the noise and gain are insensitive to supply voltages down to 125 mV which corresponds to  $180 \mu\text{W}$  DC power. In addition, excellent agreement between model predictions and measurements were



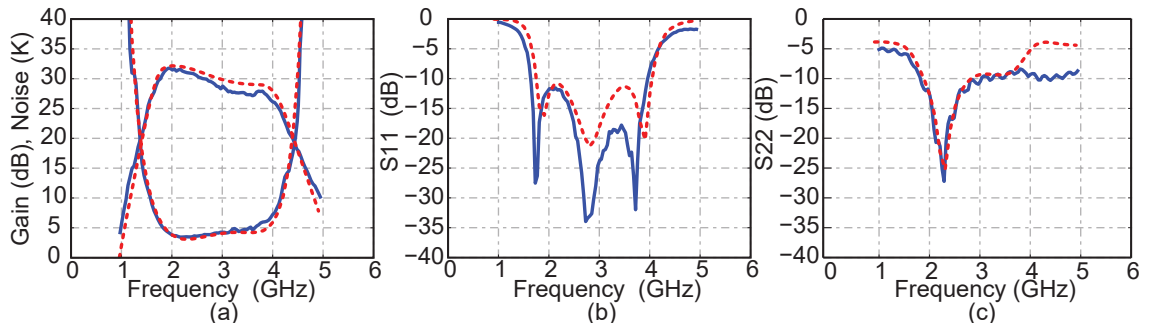
**Figure 8.3.** Cryostat block diagram. Channel A was used to measure the gain and noise temperature using a noise figure analyzer. Channel B was used for scattering parameter measurements [70], ©2016 IEEE.

observed which confirms the validity of our models for both forward-active and near saturation regions.

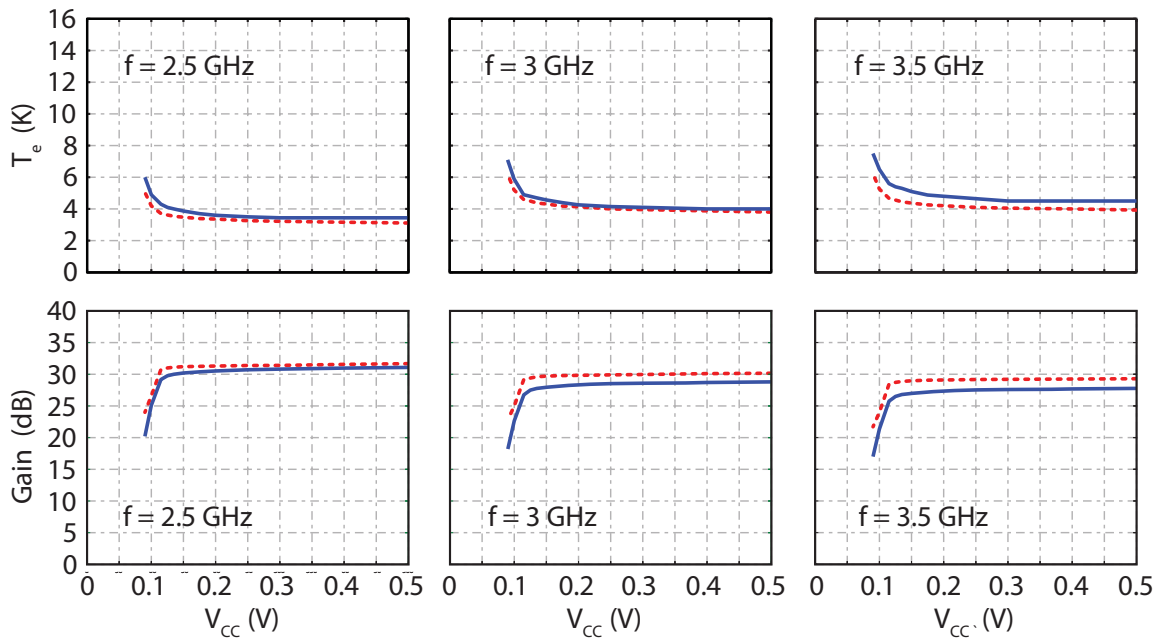
The performance of the discrete SiGe LNA is compared to the state-of-the-art discrete cryogenic amplifiers in Table.8.1. The LNA in this work provides comparable noise and gain performance while presenting an order of magnitude reduction in DC power over the state of the art.

## 8.2 Example Design: A Sub-milliwatt 4-8 GHz SiGe Cryogenic Low Noise Amplifier

While the demonstration of the discrete transistor low-power LNA described in the previous section is an important step towards scalable cryogenic receivers, integrated low-power cryogenic LNAs are desired to enable the implementation of large-scale systems such as THz kilo-pixel heterodyne cameras [2]. In this section, the design, implementation, and characterization of a sub-milliwatt 4-8 GHz SiGe cryogenic LNA



**Figure 8.4.** Amplifier performance at  $290 \mu\text{W}$  power consumption and at 15 K physical temperature. The solid lines are measurement results and the dashed lines are simulations. (a) Gain and noise temperature, (b) input reflection coefficient, and (c) output reflection coefficient [70], ©2016 IEEE.



**Figure 8.5.** Noise temperature and gain of ultra-low-power amplifier as a function of supply voltage at 15 K physical temperature and at (left) 2.5 GHz, (center) 3 GHz, and (right) 3.5 GHz. The solid lines are measurement results and the dashed lines are simulations [70], ©2016 IEEE.

**Table 8.1.** State-of-the-art Cryogenic Low Noise Amplifiers [70], ©2016 IEEE.

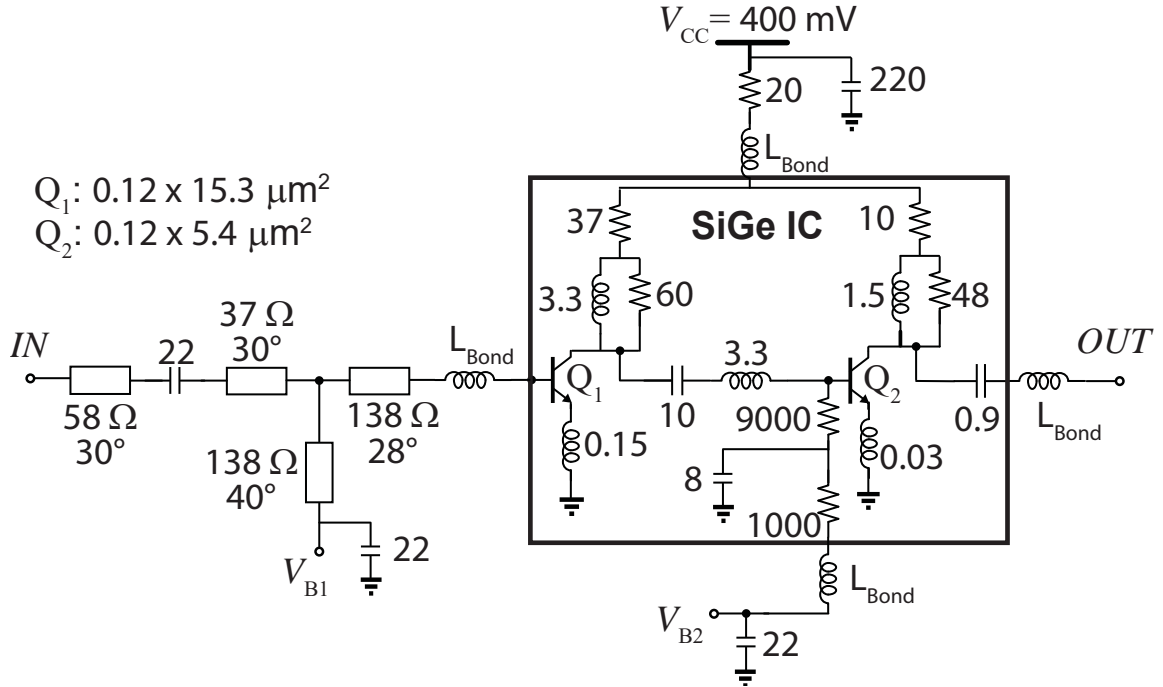
	Technology	$f_{\text{RF}}$ (GHz)	$S_{21}$ (dB)	$T_a$ (K)	$T_e$ (K)	$P_{\text{DC}}$ ( $\mu\text{W}$ )
[77]	InP HEMT	4–8	40	6	2.1	4,000
[146]	InP HEMT	1–12	> 37	12	4–8	15,000
[63]	InP HEMT <sup>†</sup>	4–8	44	10	1–2	4,200
[147]	InP HEMT <sup>†</sup>	4–8	> 27	15	1.7	3,000
[66]	SiGe HBT	0.1–5	> 30	15	4–5	20,000
[148]	SiGe HBT	0.3–5	15–18	4	8–17	2,000
[148]	SiGe HBT	0.3–8	18–25	19	6–12	8,200
[149]	SiGe HBT	0.3–4.5	> 30	17	3.5–5	4,900
[150]	SiGe HBT <sup>†</sup>	0.1–0.5	> 22	24	6	2,000
This work [70]	SiGe HBT	1.8–3.6	>27	15	3.4–5	290

<sup>†</sup> While lower power consumption were reported in these articles, the power savings came at a significant drop in performance (i.e., gain and/or noise). The numbers reported here are limited to those in which the performance was insensitive to DC power.

MMIC are described. The state-of-the-art LNA was designed leveraging the models developed in Chapter 6.

### 8.2.1 Design Procedure

A two stage integrated circuit low noise amplifier with sub-milliwatt DC power consumption was designed for the 4–8 GHz frequency range. A schematic diagram of the LNA design is shown in Fig.8.6. The input matching network was designed to be implemented off-chip to minimize losses. The base of the first stage transistor was biased through a shunt stub employed at the off-chip input matching network. The base bias path was AC grounded using a 22 pF capacitor. The first stage transistor was inductively degenerated to improve the power match leveraging an on-chip transmission line with the inductance of 0.15 nH. The size of the input transistor was selected to be  $0.12 \times 15.3 \mu\text{m}^2$  operating at a DC current of 1.1 mA to provide an optimum noise impedance of approximately  $50 \Omega$  over the desired frequency range.

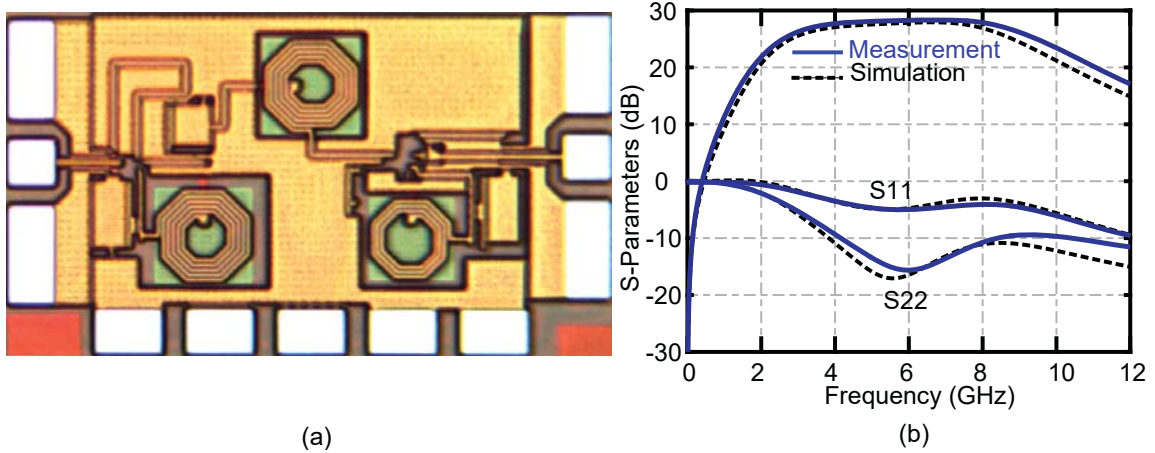


**Figure 8.6.** A schematic diagram of the low noise amplifier. The units are as follows: Resistors in  $\Omega$ , Inductors in nH, Capacitors in pF. The electrical length of the transmission lines is specified at 6 GHz [67], ©2017 IEEE.

The interstage matching network was designed to flatten the gain over the 4–8 GHz range. The base of the second stage transistor was biased through a low pass resistive network which was AC grounded using a 22 pF capacitor off chip. The second stage transistor size was selected to be  $0.12 \times 5.4 \mu\text{m}^2$  operating at 0.8 mA which provides further amplification for the LNA.

The output matching network was designed to provide a 50  $\Omega$  output impedance. The shunt resistor at the collector of the transistor was employed to ensure stability. The collector of the first and second stage transistors shared the DC voltage of 400 mV.

The LNA was simulated in the NI AWR design environment using the SiGe HBT cryogenic models described in Chapter 6. The amplifier was simulated to provide 30 dB gain and less than 6 K noise temperature across 4–8 GHz frequency band.



**Figure 8.7.** (a) Die photograph. The input and output signal pads are placed on the left and right side, respectively. The bias pads are located at the bottom of the IC. The chip dimensions are  $0.9 \text{ mm} \times 0.5 \text{ mm}$  [67]. (b) On-wafer scattering parameters of the amplifier at room temperature. Solid lines are measurements and dashed lines are simulation results [67], ©2017 IEEE.

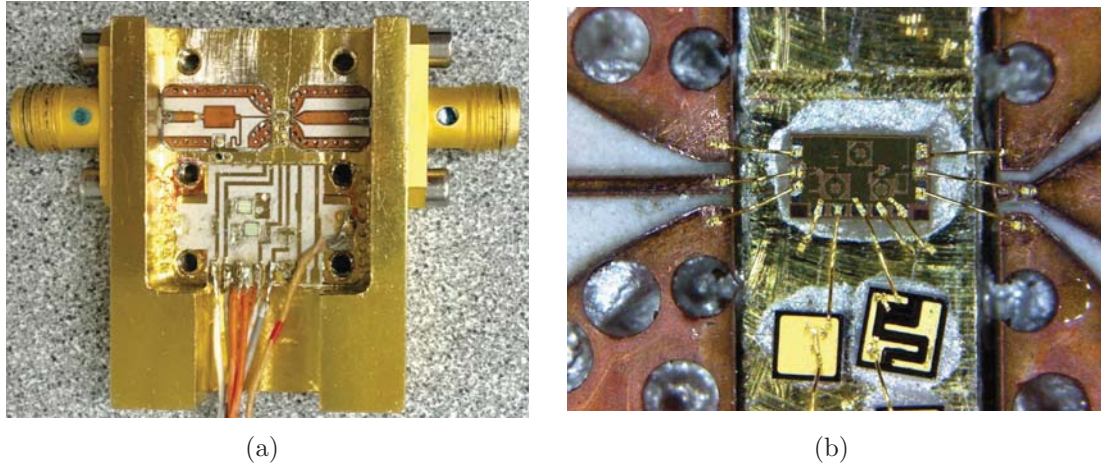
### 8.2.2 Measurement Results

The LNA was implemented in the GF BiCMOS8HP technology platform. A photo of the LNA chip is shown in the Fig.8.7.(a). The input and output are on the left and right side, respectively. The DC bias pads are placed on the bottom of the LNA chip. The dimensions of the chip are  $0.9 \text{ mm} \times 0.5 \text{ mm}$  [67].

The amplifier was first measured on wafer to verify the performance at room temperature. Fig.8.7 shows the on-wafer measurements along with simulations. Excellent agreement was observed between the measurements and simulations.

The LNA was later packaged for further testing in a cryogenic environment. Fig.8.8 shows a photo of the assembly and a closeup picture of the amplifier IC inside the module. SMA connectors were mounted at the input and output of the module to facilitate the measurements. The off-chip input matching network was implemented using the RT/Duroid 6002 substrate with a thickness of  $500 \mu\text{m}$ . The substrate was patterned using a LPKF ProtoLaser machine [145]. Fig.8.9 shows the RT/Duroid





**Figure 8.8.** The LNA assembly. (a) A photograph of the LNA package. (b) A close up picture of the LNA chip mounted inside the package [67], ©2017 IEEE.

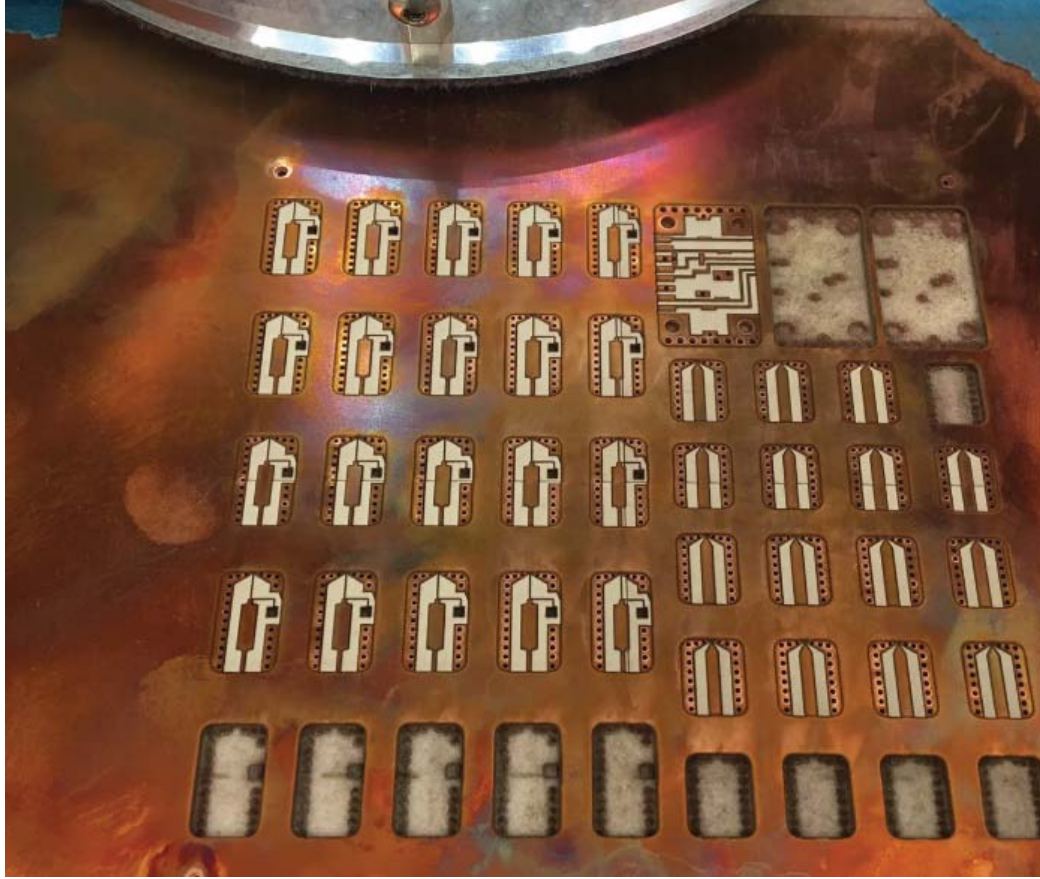
6002 substrate mounted inside the LPKF ProtoLaser machine for the patterning of the matching networks.

The packaged amplifier was first tested at room temperature and measurement results are presented in Fig.8.10. More than 25 dB of gain and less than 1.5 dB noise figure was achieved over the desired frequency band. The noise measurement was approximately 0.5 dB higher than simulation results which could be due to the optimistic models used for the off-chip input matching components. In addition, the packaging that was used in this work was initially designed for a longer chip, so, relatively long bond wires were needed to connect this IC to the input/output PCBs. These long bond wires could also contribute to the higher measured noise temperature.

The input and output return losses were also measured at room temperature. Fig.8.11 shows better than 12 dB return loss for the input and output which matches well with the simulations.

After performance verification at room temperature, The LNA was mounted inside a cryostat (shown earlier in Fig.8.3) configured to measure noise using the cold

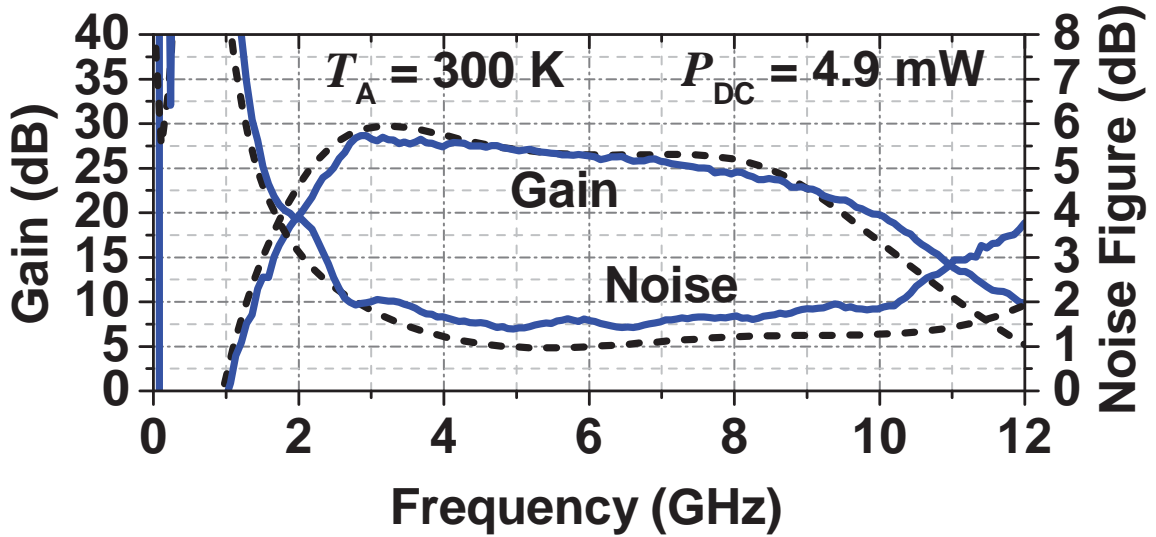




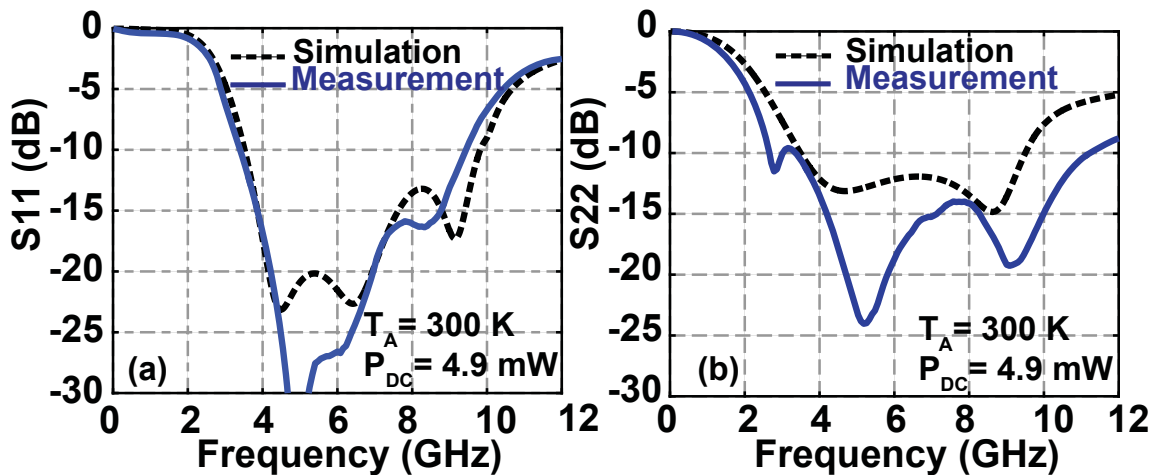
**Figure 8.9.** An RT/Duroid 6002 substrate mounted inside the LPKF ProtoLaser machine for the patterning of the matching networks.

attenuator method [123] described in Section 4.4. The amplifier was biased at  $580 \mu\text{W}$  DC power and the scattering parameters of the LNA were measured at physical temperature of 18 K. Results are compared to simulations in Fig.8.12. The input and output return losses were measured to be better than 11 and 12 dB over the desired frequency range. The ripples on the measurement results are due to the long cables used inside the cryostat for the thermal isolation at the input and output of the DUT, which were not de-embedded from these measurement results. The VNA calibration was carried out at the input and output connectors at the surface of the cryostat wall.

In the second round of cool downs, the amplifier was mounted on the second channel of the cryostat for the noise measurement. The gain and noise temperature were

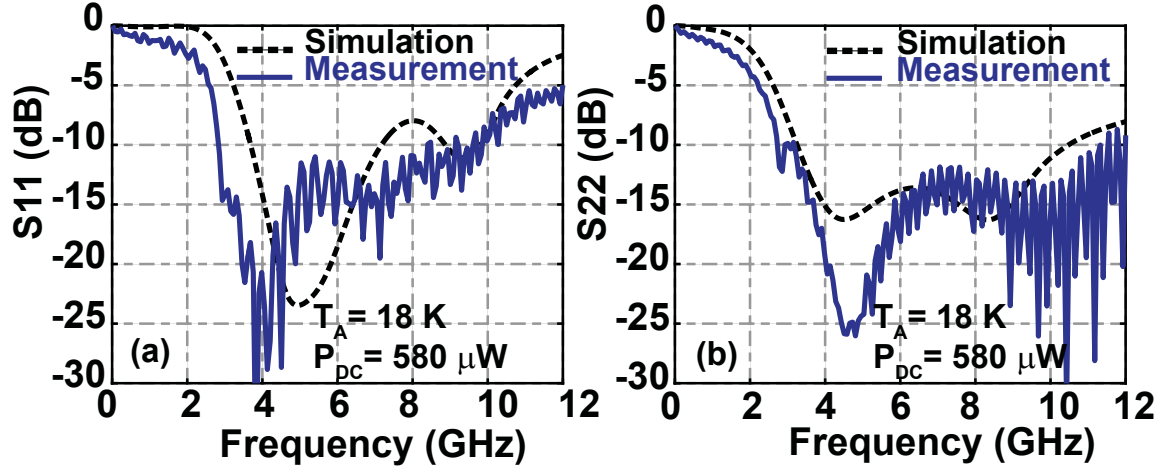


**Figure 8.10.** Gain and noise figure measured at room temperature. The amplifier was biased at three times higher current density at room temperature in comparison to 18 K in order to achieve the same transconductance for the transistors. Solid lines are measurements and dashed lines are simulations [67], ©2017 IEEE.



**Figure 8.11.** Scattering parameters of the packaged amplifier at room temperature. Solid lines are measurements and dashed lines are simulation results. (a) Input reflection coefficient. (b) Output reflection coefficient [67], ©2017 IEEE.

measured at 18 K physical temperature. LNA was biased at two different operating points and two sets of data were recorded at  $580 \mu\text{W}$  and  $760 \mu\text{W}$  DC power as shown in Fig.8.13. The first data set was taken for the LNA biased at  $I_{C1}=1.1 \text{ mA}$  and

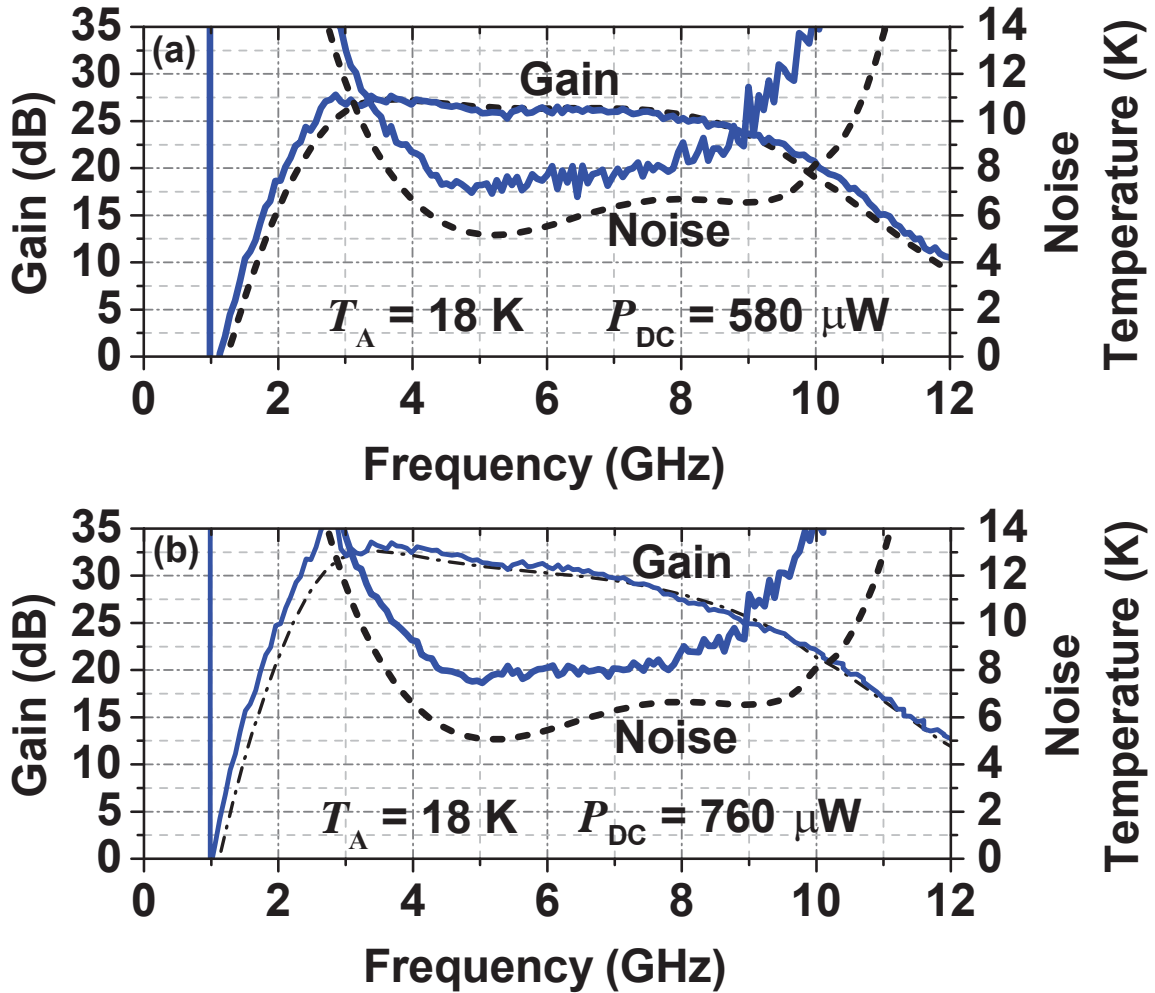


**Figure 8.12.** Scattering parameters of the packaged amplifier at 18 K physical temperature. Solid lines are measurements and dashed lines are simulation results. (a) Input reflection coefficient. (b) Output reflection coefficient [67], ©2017 IEEE.

$I_{C2}=0.8$  mA and  $V_{CC}=0.4$  mV. The average noise temperature at this bias point was measured to be 8 K and the average gain was 30 dB. The second data set was recorded at  $I_{C1}=1.1$  mV and  $I_{C2}=0.35$  mA and  $V_{CC}=0.4$  mV. The average value of the gain and noise at this bias point were found to be 7.6 K and 26.1 dB, respectively.

The noise temperature of the LNA was measured to be approximately 1-2 K higher than simulations. This could be due to the long bond wires at the input and output of the chip connecting to the PCBs which are not accurately modeled in the simulations. It also could be due to the optimistic models that were used for the off-chip components in the assembly.

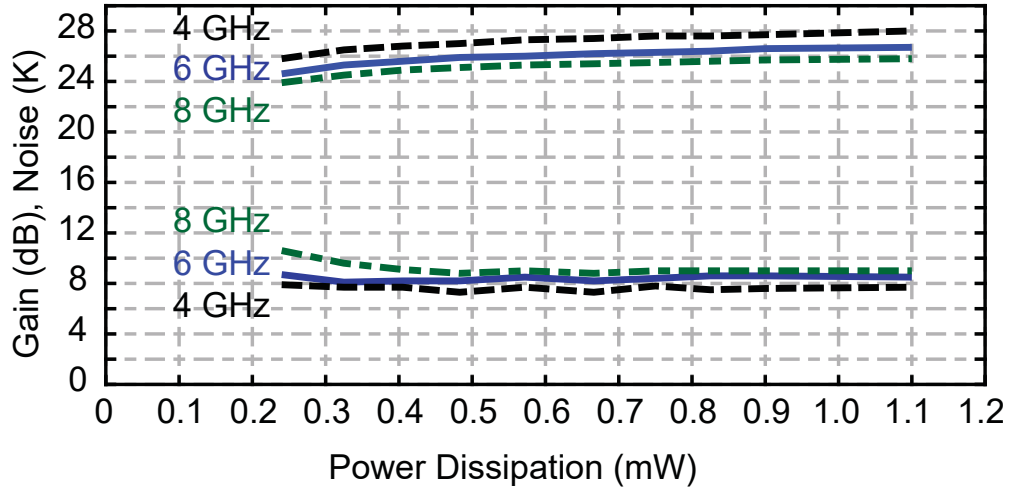
Further testing was done to investigate the dependence of the LNA noise performance with respect to power consumption. The LNA base voltages were kept constant to provide 1.1 mA and 0.35 mA current for the first and second stage at the nominal  $V_{CC}$  voltage, respectively. Then the supply voltage was swept from 700 mV to 200 mV. The total current changes between 1.5 mA to 1.2 mA over this range of supply voltages. The noise and gain results are shown in Fig.8.14. The noise performance stays constant below 6 GHz for DC powers as low as 230  $\mu$ W. At frequencies



**Figure 8.13.** Gain and noise temperature measured at 18 K physical temperature. Solid lines are measurements and dashed lines are simulation results. (a) The LNA was biased at  $580 \mu\text{W}$  DC power. (b) The LNA was biased at  $760 \mu\text{W}$  nominal power consumption [67], ©2017 IEEE.

above 6 GHz, noise increases marginally for DC power levels below  $400 \mu\text{W}$ . The gain was measured to roll off about 2 dB when the DC power was reduced by a factor of approximately 5 from  $1.1 \text{ mW}$  to  $230 \mu\text{W}$ . These results are very promising as they show that the LNA can operate at DC power levels below  $500 \mu\text{W}$  without any significant impact on the performance.

The performance of this LNA is compared to the state-of-the-art integrated cryogenic amplifiers in Table.8.2. The integrated LNA in this work provides a noise and



**Figure 8.14.** Noise temperature and gain as a function of power dissipation at 4, 6, and 8 GHz frequency points. The collector voltage was swept from 700 mV to 200 mV for fixed base voltages [67], ©2017 IEEE.

**Table 8.2.** STATE-OF-THE-ART CRYOGENIC MMIC LOW NOISE AMPLIFIERS [67], ©2017 IEEE.

	Technology	Frequency GHz	Gain dB	Noise K	$P_{DC}$ mW
[74]	InP HEMT	0.5-13	38-44	3-7	15
[151]	InPHEMT	4-12	27	13	5.7
[75]	mHEMT	4-12	31	5.3	8
[152]	mHEMT	4-12	26	8	12
This work [67]	SiGe HBT	4-8	26	8	0.58

gain that is comparable to the state of the art while dissipating approximately 10 times lower DC power. This promising result confirms the possibility of designing integrated circuits cryogenic LNAs with sub-milliwatt DC power that could be used in large-scale cryogenic systems.

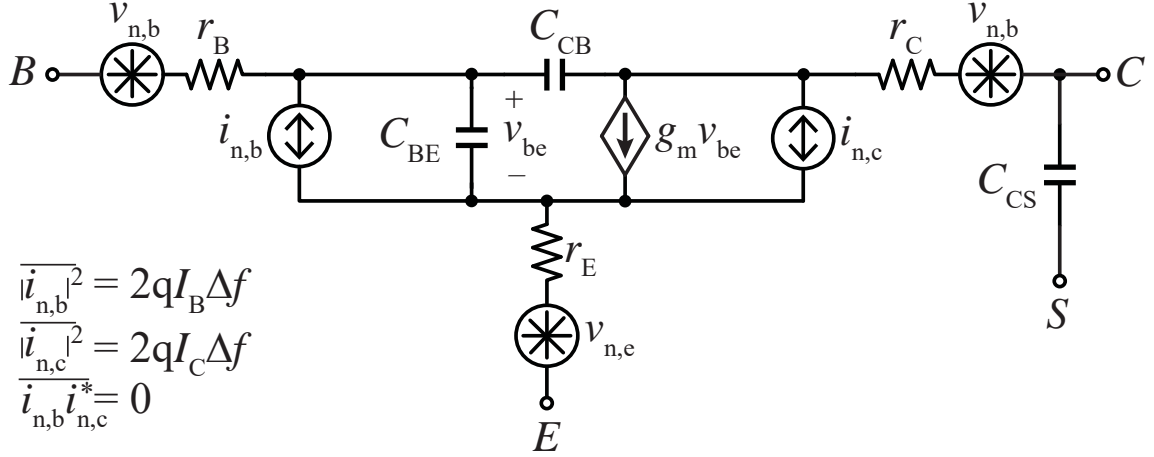
### 8.3 Example Design: A 2-4 GHz SiGe Cryogenic Low Noise Amplifier Using the TowerJazz SBC18H3 Technology process

So far, we have shown the possibility of developing low-power SiGe LNAs using the GF BiCMOS8HP technology processes. In this section, we consider the use of the TowerJazz SBC18H3 technology platform for the implementation of cryogenic LNAs. The HBTs available in the SBC18H3 process have been optimized for room temperature RF noise performance [153]. Here, we investigate their performance at cryogenic temperatures. The content of this section summarizes the results published in [68].

First, the small signal and noise model were extracted based on the standard model for SiGe HBTs shown in Fig.8.15. The parameter extraction was carried out using the techniques described in Section 6 for a SiGe HBT device with a size of  $10 \times 0.13 \mu\text{m}^2$  at a physical temperature of 7 K using a cryogenic probe-station measurement setup presented in Section. 4.3. The collector to substrate ( $C_{CS}$ ) and collector to base ( $C_{CB}$ ) capacitors were extracted using the off-bias measurement techniques (See Sec. 6). Then, the emitter and collector resistances were calculated using the open-collector method and the remaining parameters were extracted using the S-parameter measurements [56].

The on-wafer Sparameter measurement setup was calibrated using the CSR-8 calibration standards [122] to calibrate the reference plane of the measurements to the probe tips. After the device measurement, the data was de-embedded using standard open/short de-embedding procedure described in [154] to remove the effect of bond-pads and feedlines in the device structure.

Using the extracted parameters, a noise model was developed for the SiGe HBT and the minimum noise temperature ( $T_{MIN}$ ) was calculated with respect to the current density at a physical temperature of 16.5 K as shown in Fig.8.16. The  $T_{MIN}$  curve



**Figure 8.15.** SiGe HBT small-signal noise model [68], ©2018 IEEE.

**Table 8.3.** Extracted Model Parameters at cryogenic temperatures.

	$r_B$	$r_E$	$r_C$	$C_{CB}$	$C_{CS}$	$C_{BE}$	$gm$	$\tau$
	$\Omega$	$\Omega$	$\Omega$	fF	fF	fF	S	pS
First stage	1.4	0.35	0.8	154	42	445	0.39	0.5
Second stage	1.7	0.35	0.8	128	35	368	0.31	0.5

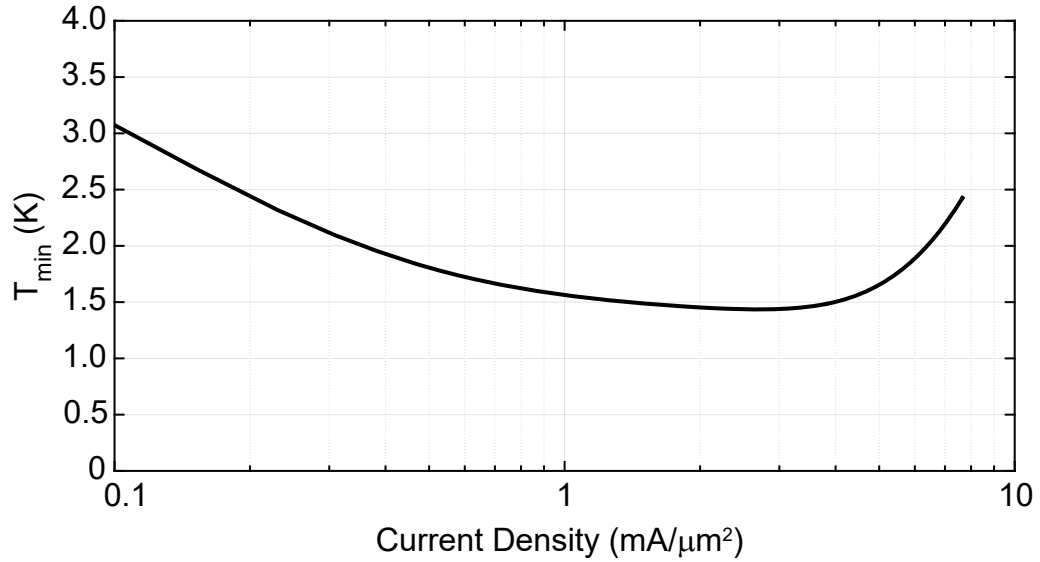
shows a minimum of less than 2 K at current densities between 0.4 to 6 mA/ $\mu\text{m}^2$  at 3 GHz frequency point [68].

### 8.3.1 Design

A schematic diagram of the amplifier is shown in Fig.8.17. The first stage transistor size was selected to be 0.13  $\mu\text{m} \times 60 \mu\text{m}$  with a DC current of 2.5 mA and the second stage transistor size was 0.13  $\mu\text{m} \times 50 \mu\text{m}$  with 2 mA DC current. The extracted small signal parameters of the first and second stage transistors are reported in Table.8.3.

The LNA was designed with on-chip input and output matching networks. The input of the LNA was AC coupled using a 10 pF capacitor. A series 1.75 nH inductance was used to help with the input matching. The base of the first stage transistor was



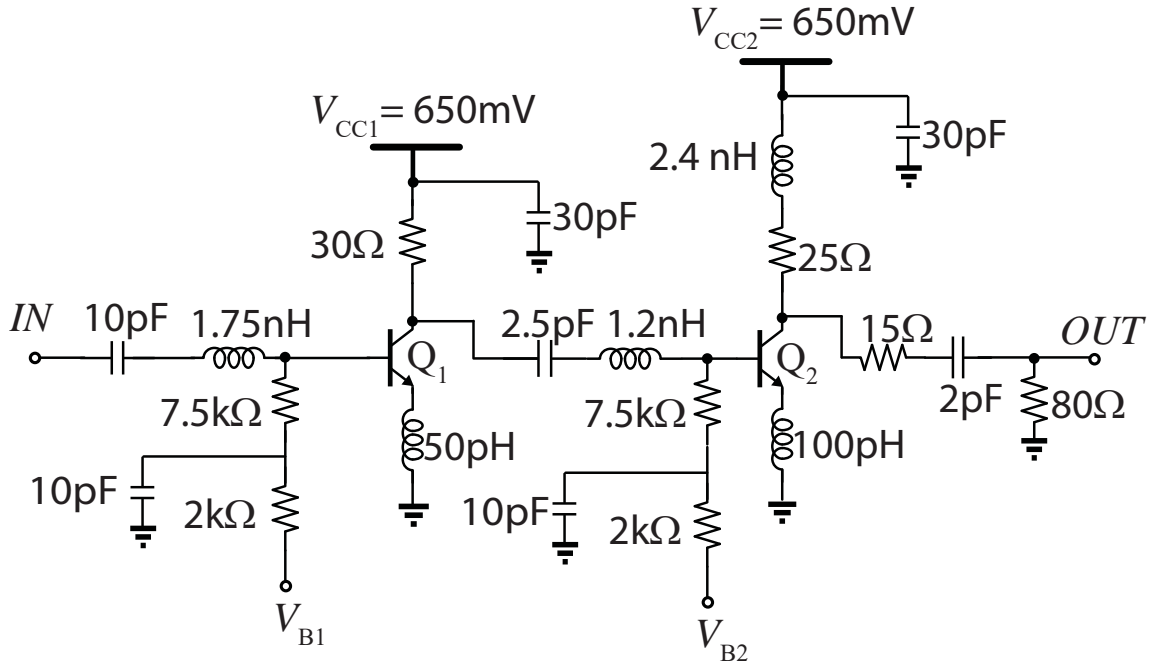


**Figure 8.16.** Modeled minimum noise temperature ( $T_{MIN}$ ) of the SBC18H3 device at 3 GHz as a function of current density at a physical temperature of 16.5 K [68], ©2018 IEEE.

biased through a low pass resistive network on chip. The first stage transistor was sized to be  $0.13 \times 60 \mu m^2$  to provide a near  $50 \Omega$  optimum noise impedance. A degeneration inductance was employed in the design to help with simultaneous noise and power match. The collector of the first stage transistor is biased through a  $30 \Omega$  resistor and a  $30 \text{ pF}$  bypass capacitor. The LNA was designed to run from a  $650 \text{ mV}$  supply voltage to provide the transistors with enough headroom to operate at forward active region. The first stage was designed to operate at  $2.5 \text{ mA}$  DC current corresponding to  $0.35 \text{ mA}/\mu m^2$  which was selected as a trade-off between noise and DC power.

The interstage matching network consists of an AC coupling capacitor in series with a  $1.2 \text{ nH}$  inductor which helps shaping the gain at high frequencies. The base of the second stage transistor was biased through a resistive low pass filter similar to that of the first stage.





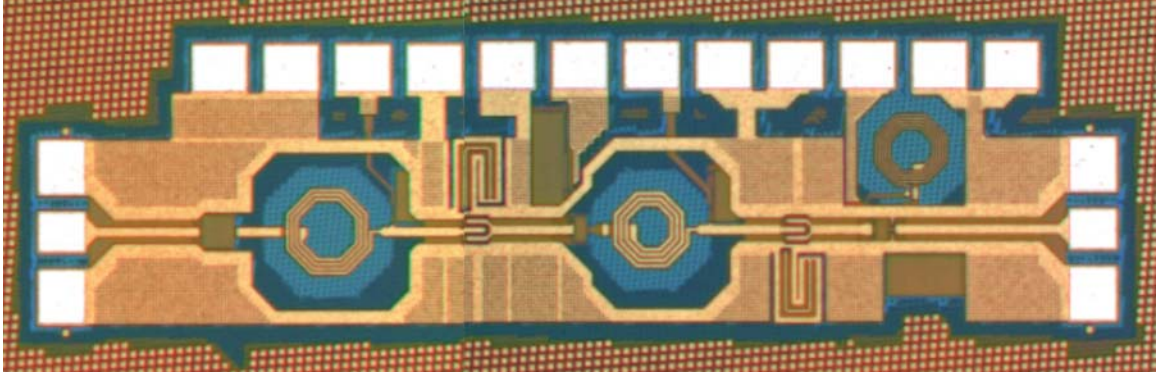
**Figure 8.17.** Schematic diagram of the MMIC SiGe LNA [68], ©2018 IEEE.

The second stage transistor was sized to be  $0.13 \times 50 \mu\text{m}^2$  with a DC current of 2 mA. The output matching network is designed to provide a  $50 \Omega$  impedance at the output. The shunt resistor at the output is used to ensure stability.

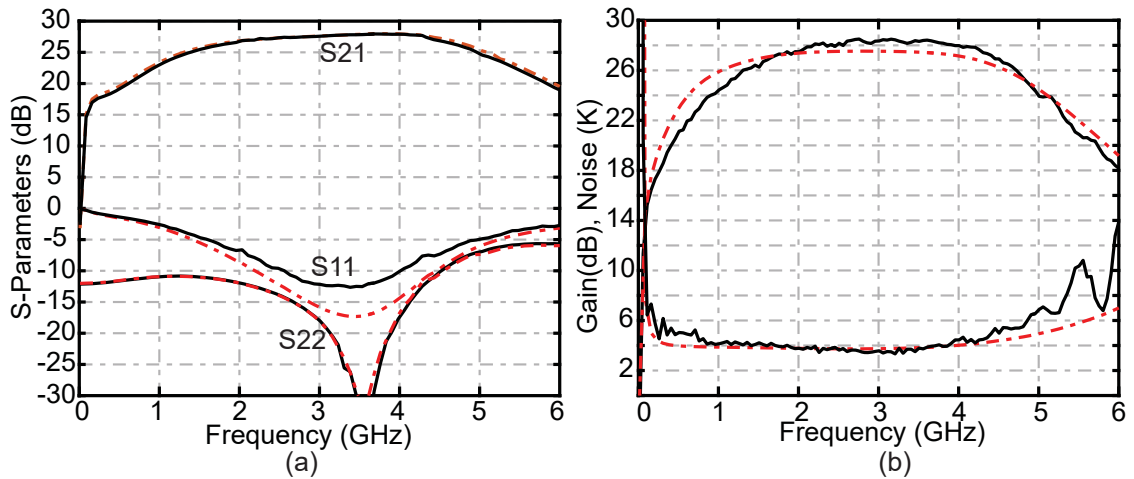
### 8.3.2 Measurement Results

The amplifier was implemented in the TowerJazz SBC18H3 technology process and a die photo of the chip is shown in Fig.8.18. The chip dimensions are  $1.5 \text{ mm} \times 0.4 \text{ mm}$ . The input and output signal pads are placed on the left and right sides, respectively. The DC bias pads are located at the top row.

Before packaging, the LNA was tested on wafer to ensure the functionality and comparison with the model predictions. The amplifier was measured inside a cryogenic probe station and S-parameters were measured at 7 K ambient temperature and results are shown in Fig.8.19. (a) along with model predictions. Excellent agreement between simulations and measurements were obtained.

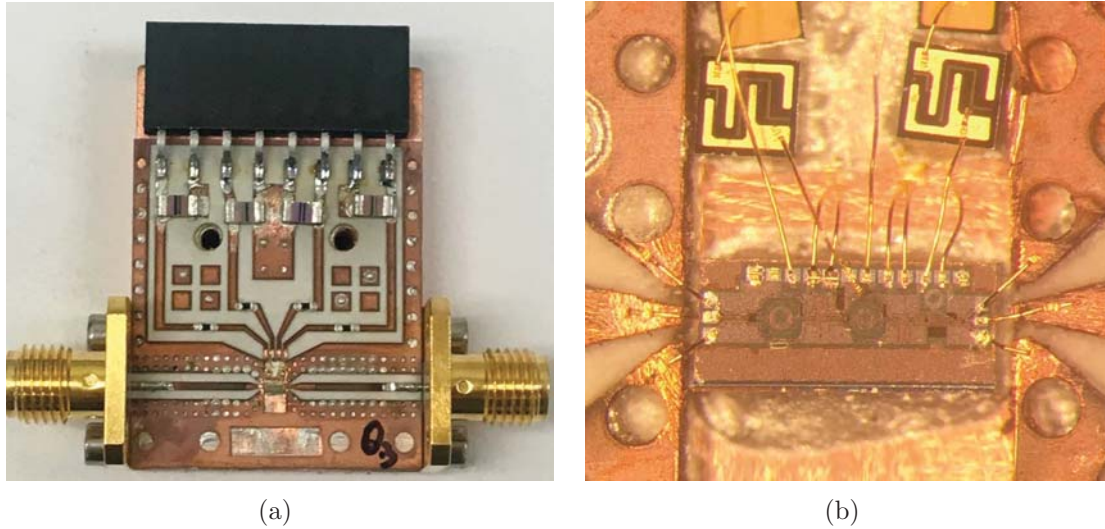


**Figure 8.18.** Die photograph. The chip dimensions are  $1.5 \text{ mm} \times 0.4 \text{ mm}$  [68], ©2018 IEEE.



**Figure 8.19.** (a) On-wafer scattering parameters at 7 K temperature. Black solid lines are measurement results and red dashed lines are simulation results carried out using the models extracted in this work [68]. (b) Gain and noise temperature at a physical temperature of 16.5 K. Black solid lines are measurement results and dashed red lines are simulation results obtained using the models developed in this work [68], ©2018 IEEE.

After on-wafer measurements, the LNA was packaged in a copper housing as shown in Fig.8.20. A printed circuit board (PCB) was designed to provide the DC bias and signal paths for the input and output of the chip. The PCB was implemented using an RT/Duroid 6002 substrate with a thickness of  $250 \mu\text{m}$ . The input and output of the IC were directly connected to the  $50 \Omega$  co-planar wave-guide transmission lines which



**Figure 8.20.** (a) The LNA assembly. (b) A photo of the LNA chip mounted inside a cutout on the PCB [68], ©2018 IEEE.

were connected to SMA connectors on the opposite end to facilitate the cryogenic measurements. Fig.8.20. (b) shows a closeup picture of the LNA IC which was wire bonded to the PCB.

Next, the packaged LNA was mounted inside the cryostat and the noise and gain were measured using the cold attenuator method [123]. Fig.8.19. (b) presents the noise temperature and gain of the amplifier at 16.5 K ambient temperature. A gain of more than 28 dB and noise temperature of 3.3 to 4 K over the 2 to 4 GHz frequency range was obtained while the LNA dissipated less than 3 mW of DC power. To the best of our knowledge, this is the lowest noise temperature reported for a low-power SiGe LNA to date [68].

The amplifier performance is compared to the state-of-the-art cryogenic MMIC LNAs in Table.8.4. The LNA performance is comparable to the state of the arts while consuming lower DC power consumption. The promising results obtained in this work validates the possibility of using the TowerJazz SBC18H3 technology process for the

**Table 8.4.** State-of-the-art cryogenic MMIC LNAs [68], ©2018 IEEE.

	Technology	Frequency GHz	Gain dB	Noise K	P <sub>DC</sub> mW
[155]	InP HEMT	2–5	>27	1.3-2	12
[66]	SiGe HBT	0.1–5	>30	4-5	20
[69]	SiGe HBT	0.3–3	>22	2.8	32
[148]	SiGe HBT	0.5-4	>25	6-8	8.3
This work	SiGe HBT	2–4	28	3.3-4	3

implementation of cryogenic low noise amplifiers with competitive noise performance in comparison with the other technologies.

## 8.4 Summary

In this chapter, the design and implementation of several low-power discrete and integrated circuit SiGe low noise amplifier has been presented. It has been shown that the SiGe LNAs can operate at low supply voltages near saturation region with little to no significant impact on their noise and gain performance. LNAs with sub-milliwatt level power dissipation were designed and implemented. The amplifiers were designed leveraging the cryogenic SiGe HBT models developed in Chapter 6 and excellent agreement between measurements and models were obtained.

The implementation of such low-power cryogenic amplifiers can provide a significant improvement in the scalability of scientific cryogenic instrumentation. For instance, a power consumption of  $300\ \mu\text{W}$  presented in Section.8.1, could translate into the implementation of a practical 1,000 element dual-polarization THz receiver system that is cooled using a 4.2 K cryogenic cooler with 1.5 W heat capacity.

In the next chapter, we focus on the implementation of cryogenic sensing systems build around these low-power SiGe LNAs for THz astronomy applications.

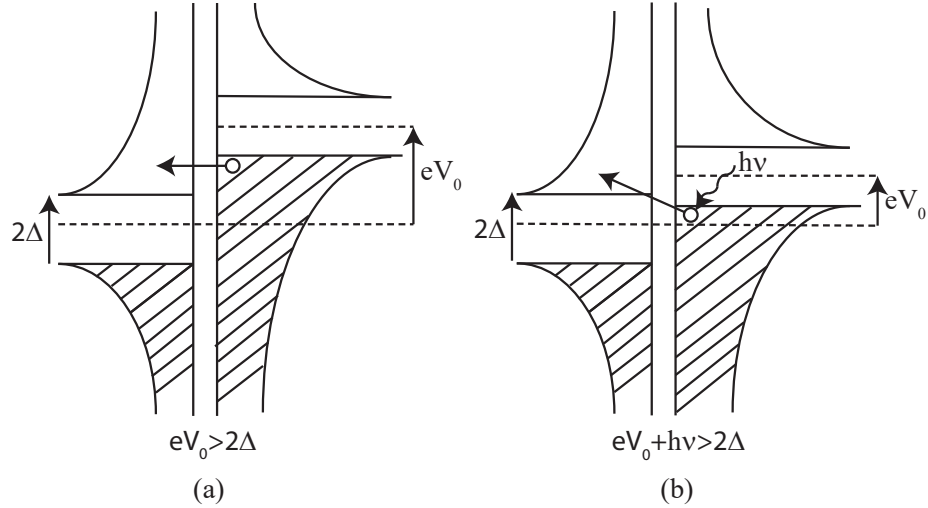
## CHAPTER 9

### SUPERCONDUCTOR-INSULATOR- SUPERCONDUCTOR BASED RECEIVERS UTILIZING ULTRA-LOW-POWER SIGE LNAs

In this chapter, the design and implementation of several cryogenic low noise amplifiers with sub-milliwatt power dissipation optimized for a direct connection to superconductor-insulator-superconductor (SIS) mixers are described. As a first attempt, we designed and implemented a SiGe LNA with  $720\ \mu\text{W}$  DC power and directly connected it to an SIS mixer and characterized the noise. Although a promising system noise performance was achieved, the resulting system was narrow band.

In the second step, we re-designed and optimized the amplifier for a larger bandwidth of 3–6 GHz while dissipating  $100\ \mu\text{W}$  DC power. We characterized the receiver system and achieved a noise temperature within 15 K of the baseline results using the previously reported conventional system that dissipated 15 mW power. Although the low-power system was wideband this time, the gain was low and a second cryogenic amplifier was needed to be mounted after the integrated SIS-mixer/SiGe-LNA receiver so as to prevent the noise contribution of the warm IF chain outside the cryostat.

Knowing that achieving a good noise performance over a wide IF bandwidth is possible leveraging the microwatt SiGe LNAs, the final step was to re-design the amplifier with enough gain to suppress the effect of the warm IF while maintaining the same level of power dissipation and bandwidth. Thus, we implemented an SIS-mixer/SiGe-LNA system with 30 dB gain and  $300\ \mu\text{W}$  DC power operating at an IF frequency of 4–8 GHz. The final system achieved a noise temperature within



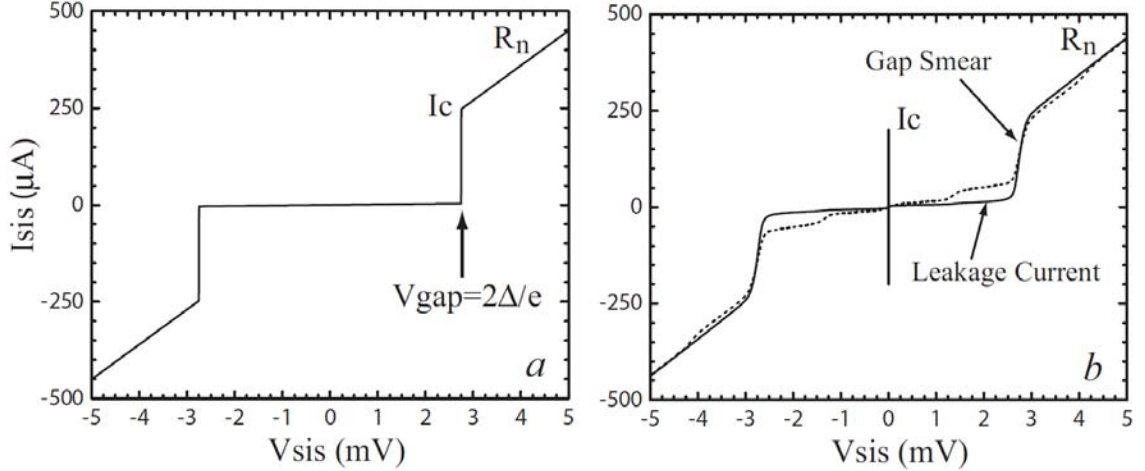
**Figure 9.1.** (a) Density of states with respect to the energy for quasi-particle tunneling. (b) photon assisted tunneling. Figure after [156].

5 K of the previously reported baseline results while dissipating approximately five orders of magnitude lower DC power. The detail of the design, implementation, characterization, system integration, and measurement results are presented in this chapter. The content of this chapter summarizes the results published in [71–73].

## 9.1 Fundamentals of Superconductor-Insulator-Superconductor Mixers

Superconductor-insulator-superconductor (SIS) mixers are physically two layers of superconductors separated with a layer of insulator in between. These devices operate based on the quantum mechanical properties of the material and tunneling of the quasi-particle electrons through the insulator layer. The quantum theory of SIS mixers was initially investigated by Tucker and Millea in 1978 [157] and the next year by Tucker in [158]. The quantum theory predicts the quantum limited noise of SIS mixers as well as the RF to IF conversion gain.

Fig.9.1 shows the band diagram of an SIS junction and explains the photon assisted tunneling of quasi-particles which is the basis of the SIS mixer theory. This



**Figure 9.2.** (a) Ideal high-current density AlN-barrier SIS I/V curve at 0 K. (b) The actual measured I/V curve. Figure reproduced from [156].

phenomena was first discovered by Dayem and Martin in 1962 [159] and later was theoretically explained by Tien and Gordon in 1963 [160].

Electrons are bound together as cooper pairs with a binding energy of  $\Delta$  in a superconductor material. The minimum energy required for the excitation of cooper pairs above the ground state is  $2\Delta$ . This energy is known as superconducting energy gap and is required to break cooper pairs into quasi-particles which enables the mixing behavior of SIS junctions.

Photon assisted tunneling of quasi-particles is the fundamental basis of the SIS mixing theory. This phenomena occurs when the energy of a photon received by an SIS junction added to the DC voltage applied to the junction becomes greater than  $2\Delta$ . This would result in a very nonlinear behavior in the device which leads to a frequency mixing properties of the junction. An ideal I-V curve of an SIS junction is shown in Fig.9.2(a). The sharp rise in the IV curve at the gap voltage is due to the tunneling of quasi particles through the insulator barrier. Fig.9.2(b) shows an I-V curve of an AlN SIS junction. The solid curve shows the DC IV curves when the junction is not pumped with LO signal. The dashed line presents the photon-



assisted tunneling current when the junction is pumped with an LO frequency of 345 GHz [156]. The stepped region appearing on the pumped IV curve is called the "photon step" [161]. The output power is expected to be maximized when the junction is biased at the center of the photon step [161]. The sharpness of the gap is found to be related to the conversion gain of the mixer [156].

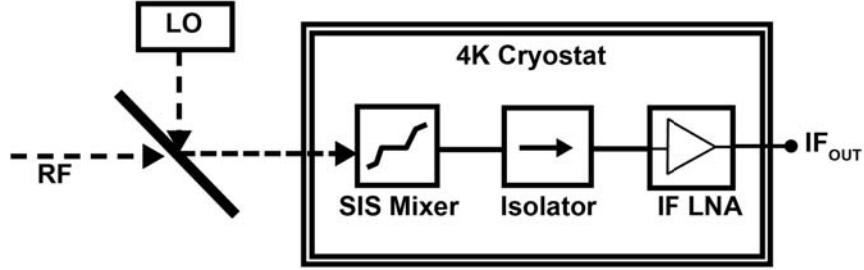
Unlike the quasi-particle tunneling, the cooper pair tunneling through an SIS junction is not desired in a superconductor mixer. The DC current due to the cooper pair tunneling is called the "DC Josephson effect" discovered by Josephson in 1962 [162] which earned him a Nobel prize in 1973. This phenomena results in the appearance of multiple steps on the DC-IV curve of a pumped SIS junction called "Shapiro Steps" [163]. Biasing the device at these steps results in an unstable behavior and excess noise in the mixer. To prevent the cooper pair tunneling in a quasi-particle SIS mixer, magnetic fields could be applied to the junction to suppress this effect [161,164].

Quasiparticle tunneling through an SIS junction arises from the quantum nature of the material. The properties of an SIS junction could be characterized based on its quantum mechanical behavior. Further detailed calculation of current and noise and mixing behavior could be found in [157,158].

## 9.2 Superconductor-Insulator-Superconductor Receivers

Large-scale heterodyne receivers are desired for the observation of galactic objects in the sub-millimeter frequency range [2, 23, 24]. As discussed in Chapter 1, SIS based receivers could provide sensitivity close to the quantum limit which makes them a suitable choice for the implementation of sub-millimeter heterodyne systems. Conventional SIS based receivers contain SIS mixers followed by an isolator and a cryogenic low noise amplifier (See Fig.9.3). The output impedance of an SIS mixer is typically variable and is a function of the bias, pump power, and the frequency and is usually greater than the  $50\ \Omega$  which most of LNAs are matched to. Thus, using





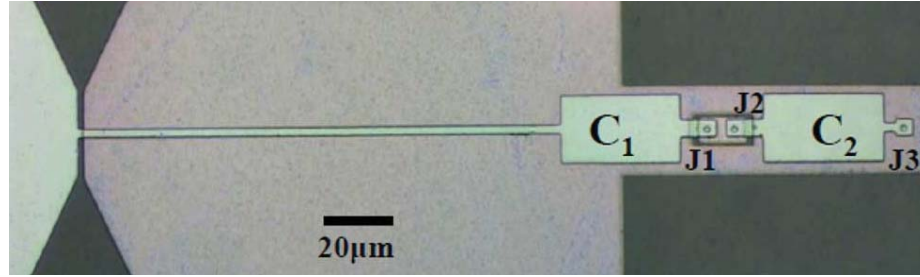
**Figure 9.3.** Conventional implementation of THz receiver systems.

an isolator between the SIS mixers and the  $50\ \Omega$  cryogenic LNAs is necessary for the receiver chain to be practical [165, 166].

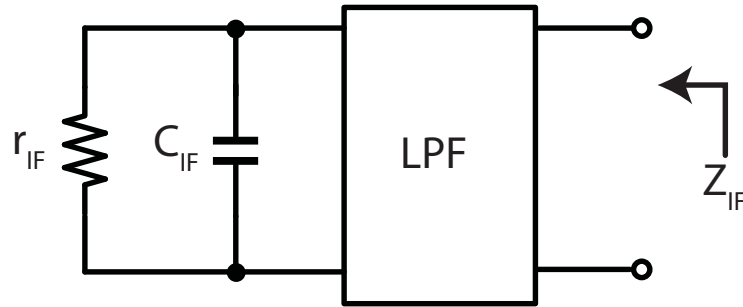
The SIS based receivers are desired to be scalable in order to enable wide-ranging astronomical surveying in a reasonable amount of time as described in Chapter 1. The current state-of-the-art SIS mixer FPA is Supercam, a 64 pixel array operating at 350 GHz using low noise amplifiers with 8 mW of power dissipation [1].

There are many challenges associated with the scaling of such systems to kilopixel elements one of which is the power dissipation of available cryogenic LNAs. In order to practically implement a thousand receivers inside a single cryogenic cooler, the power dissipation of cryogenic LNAs need to be reduced to microwatt levels. In addition, for a tighter integration of a receiver array, it is beneficial to remove the bulky isolator from the receiver chain and design and optimize LNAs for a direct connection to SIS mixers.

In the previous chapter, we proved the possibility of implementing stand-alone microwatt level cryogenic LNAs matched to  $50\ \Omega$  impedance at the input. In this chapter, the details of the design, implementation, and characterization of SiGe LNAs designed for a direct connection to an SIS mixer is described and system integration and characterization along with simulation results are presented.



(a)



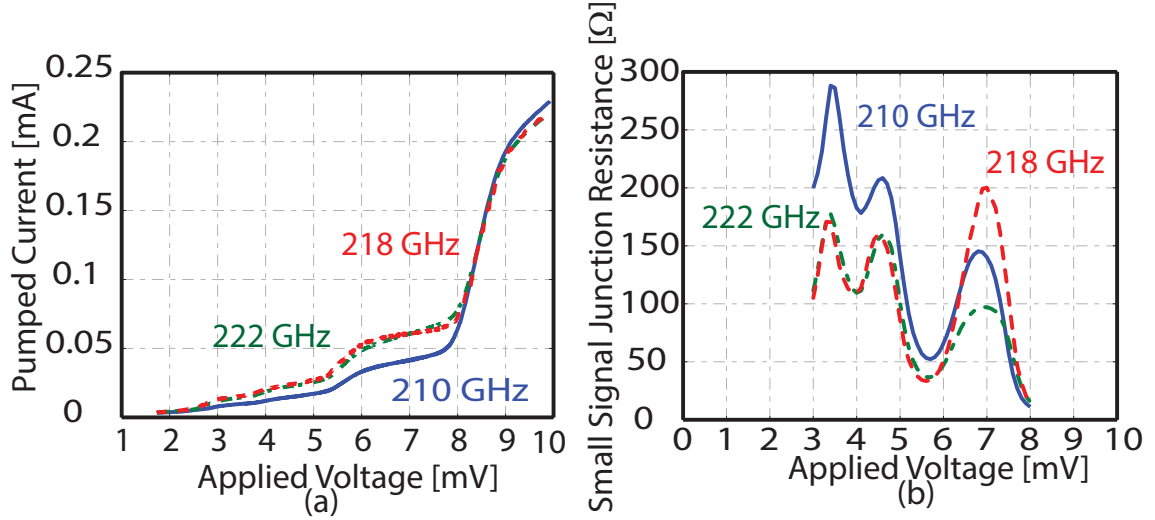
(b)

**Figure 9.4.** (a) Micrograph of the intrinsic SIS mixer used in this work. Reproduced with permission from [167], ©2013 IEEE. (b) Equivalent IF circuit model of the intrinsic SIS mixer [72], ©2016 IEEE.

### 9.3 SIS Mixer Equivalent Model

In order to design an LNA that is matched to the output of an SIS mixer, first, an equivalent circuit model for the SIS junction needs to be developed. The SIS mixer used in this work is based on a distributed series array of three SIS junctions reported in [167]. A micrograph of the intrinsic mixer circuit employed in this work appears in Fig. 9.4(a). Determination of the IF impedance of the SIS is required for the design and optimization of a low noise amplifier directly connected to the output of the SIS mixer. The output impedance of an SIS mixer can be modeled as a parallel RC network shown in Fig.9.4(b) which captures the intrinsic SIS mixer model consisting of the SIS junctions and the tuning networks.

An estimate of the real component of the intrinsic mixer IF output impedance ( $r_{IF}$ ) can be obtained from DC IV measurements and depends upon the LO pump power



**Figure 9.5.** SIS mixer properties. (a) Pumped IV curve for local oscillator frequencies of 210, 218, and 222 GHz. (b) Corresponding small-signal output resistance [71], ©2015 IEEE.

and frequency as well as the bias point of the SIS mixer (See Fig.9.5). When biased at 7 mV for maximum sensitivity (at the center of the photon step) and pumped at frequencies in the range of 210 to 222 GHz, these mixers have a nominal IF output resistance varying from 100 to 200  $\Omega$  as shown in Fig.9.5.

The equivalent IF circuit appears in Fig. 9.6(a) and consists of the three SIS junctions as well as a pair of lumped capacitances to ground corresponding to the impedance transformers labeled  $C_1$  and  $C_2$  in Fig. 9.4(a). The junction specific capacitance for these devices is approximately 85 fF/ $\mu\text{m}^2$ , the diameter of the circular junctions is  $1.8 \pm 0.1 \mu\text{m}$ , and each junction has an additional parasitic capacitance of approximately 5 fF. Thus,  $C_j$  is estimated to be in the range of 195–245 fF. The values of  $C_1$  and  $C_2$  can be determined from the dimensions of the thin-film microstrip matching networks and are approximately  $210 \pm 21$  and  $140 \pm 14$  fF, respectively. Thus, the total effective IF capacitance of the intrinsic SIS mixer is estimated to be in the range of 260 to 325 fF. For design purposes, a value of 300 fF was assumed.

The terminals of the mixer chip connect to the intrinsic SIS mixer through a pair of stepped-impedance lowpass filters, as shown in Fig. 9.6(b). This embedding network was modeled using Ansys High Frequency Structure Simulator (HFSS)<sup>1</sup> and the resulting two-port network was used to complete the model of the mixer IF output impedance. The reference plane for the SIS IF output-impedance model is at the interface between the LNA printed circuit board (PCB) and the mixer chip.

## 9.4 First Generation of the Low-Power SiGe-LNA/SIS-Mixer Receiver

Using the equivalent IF impedance of the SIS mixer described in the previous section, a low-power SiGe LNA was designed and optimized for a direct connection to the SIS mixer. Here, the details of the design, implementation, and system integration of the first generation of a low-power SiGe-LNA/SIS-Mixer receiver are presented. This section summarizes the results reported in [71].

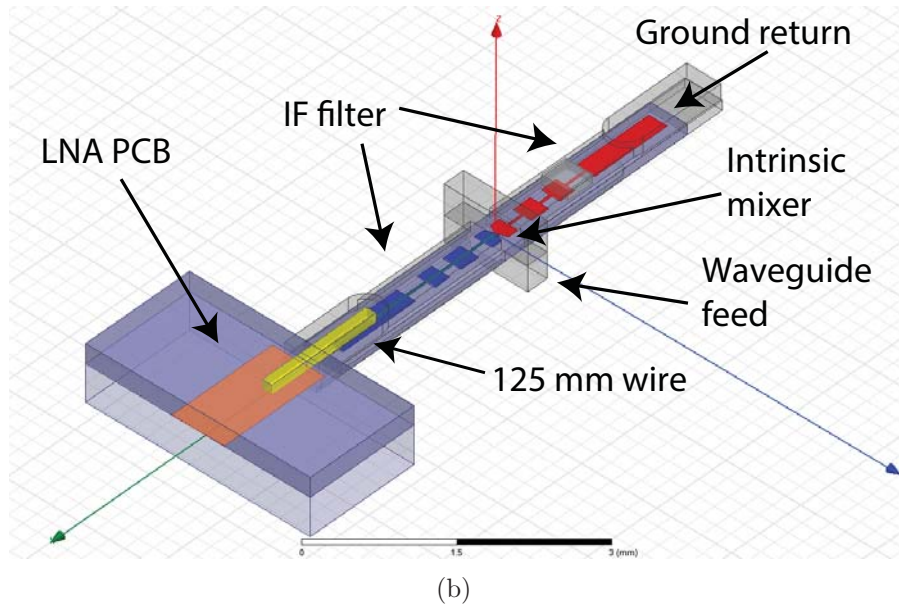
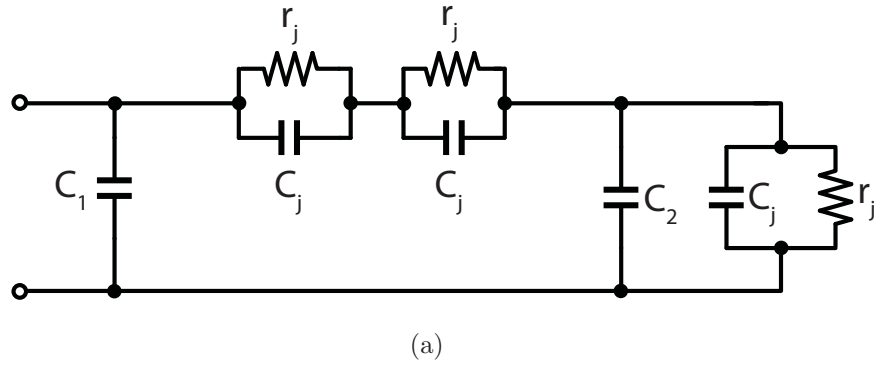
### 9.4.1 SiGe LNA Design

As an initial demonstration of low power SIS base receivers, a two-stage SiGe LNA was designed using SiGe HBT device models presented in Chapter 6. A schematic diagram of the amplifier is shown in Fig.9.7. The SIS mixer IF impedance model was inserted into the LNA simulations to serve as the generator impedance and the amplifier was optimized for noise when driven from the SIS mixer model.

A low noise amplifier designed for a large generator impedance has pros and cons. For a given transistor technology, the optimum generator impedance is inversely proportional to the device periphery. As low-noise devices are typically biased at a fixed current density to realize the minimum noise, a smaller transistor periphery

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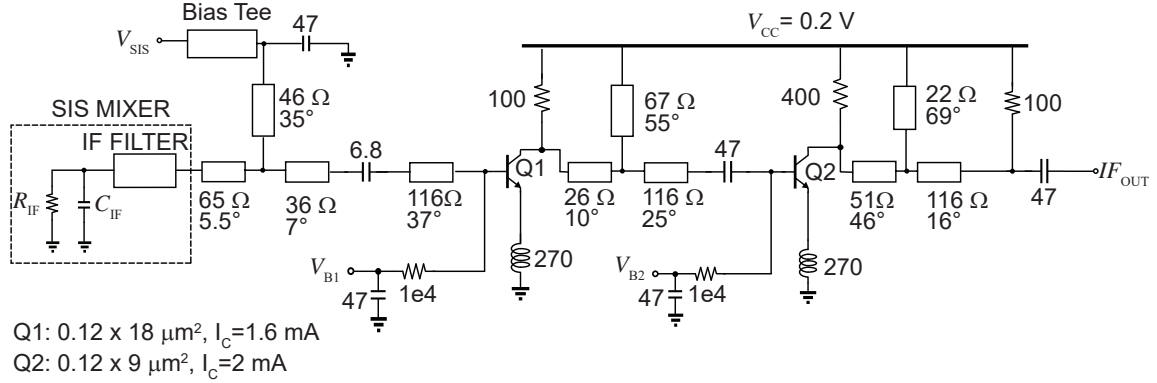
<sup>1</sup>The HFSS simulations of the embedding network was carried out by one of our collaborators, Dr. Paul Grimes.



**Figure 9.6.** (a) Equivalent output impedance model of an SIS mixer. (b) CAD drawing of mixer chip embedded in the waveguide mixer block, including transition to LNA PCB [72], ©2016 IEEE.

corresponds to a lower overall current, which translates to a decrease in power consumption. On the other hand, realizing a broadband matching network given a high generator impedance requires large reactances, which are not easy to realize using transmission line components.

Here, an input matching network was employed to transform the generator impedance to the optimum impedance for the noise match at the input stage. A shunt transmission line was employed in the input network to serve as the matching and was used as a path to bring DC bias to the SIS junction. This path was AC coupled from the

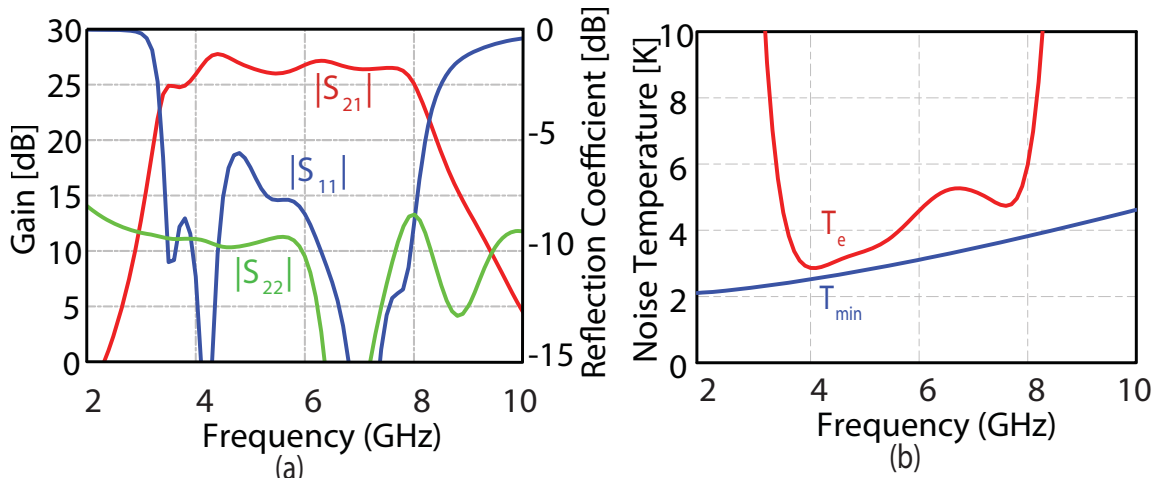


**Figure 9.7.** Low noise amplifier schematic diagram. Units: Capacitance-pF, Resistance-ohm, Inductance-pH. Quoted electrical lengths were calculated at 6 GHz frequency point [71], ©2015 IEEE.

base of the first stage transistor to isolate the SIS mixer bias from the LNA bias. A commercial surface mount bias-tee (Marki BT-0014SM-2) was incorporated to further filter the DC bias for the SIS junction. The base of the LNA first stage transistor was biased through a 10 kΩ shunt resistor. The first stage transistor was biased at 1.6 mA DC current and was degenerated to help with the power match at the input. The degeneration inductance was realized using bond wires from the emitter of the SiGe HBT to the ground of the circuit.

The second stage was designed to improve the LNA gain and provide a 50 Ω output impedance. The base of the second stage transistor was also biased through a 10 kΩ resistor. The second stage transistor was biased at 2 mA DC current. The amplifier was designed to operate at the frequency band of 4-8 GHz at a total DC current of  $I_C=3.6 \text{ mA}$  and  $V_{CC}=200 \text{ mV}$  which corresponds to a DC power consumption of 720 μW.

The LNA was simulated using the NI AWR design environment and results are presented in Fig.9.8. The gain was simulated to be better than 25 dB and the noise better than 6 K. The input return loss was expected to be better than 7 dB over the desired frequency range. To investigate the sensitivity of the amplifier noise to the



**Figure 9.8.** Simulated performance of amplifier driven from  $150 \Omega$  generator impedance. The simulation also considers the  $270 \text{ fF}$  SIS capacitance as well as the series embedding network. (a) Scattering parameters (b) noise performance [71], ©2015 IEEE.

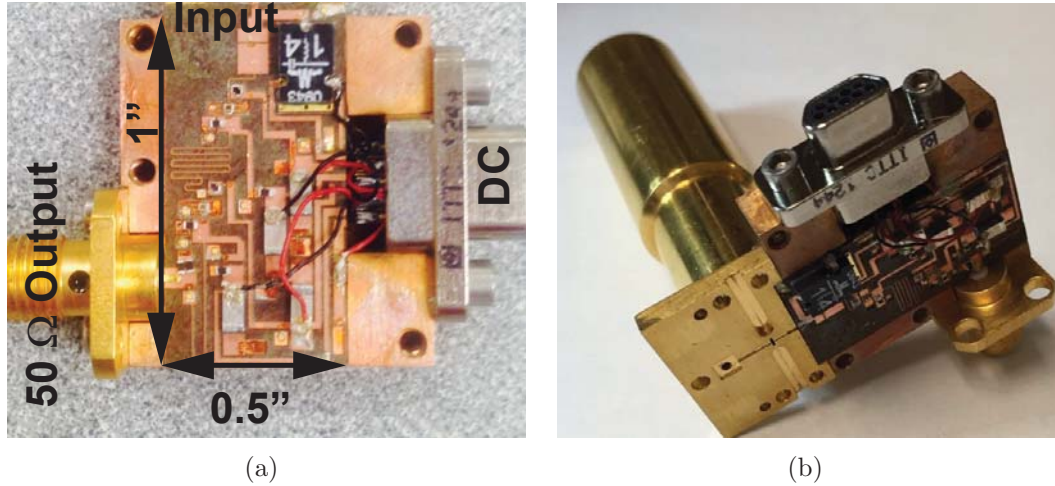
output impedance of the SIS mixer, the real part of the generator impedance was swept from  $100$  to  $200 \Omega$  in simulations and the noise performance was changed by less than  $1 \text{ K}$  over the majority of the frequency band.

#### 9.4.2 Measurement Results

The amplifier was implemented using discrete SiGe HBT transistors from the GF BiCMOS8HP process along with the surface mount and wire bondable passive components. A photo of the LNA assembly is shown in Fig.9.9(a). The housing was designed to mate with the SIS mixer block. The DC voltage was provided to the LNA through a Micro-D DC connector and a SMA connector was mounted at the output.

The LNA input was directly bolted to the SIS mixer block and the electrical contact between the SIS junction and the LNA was done using a  $1 \text{ mm}$  long BeCu wire that was soldered on the LNA PCB board from one side and was pressure-contacted to the SIS junction on the opposite side. A photo of the hybrid SIS-mixer/SiGe-LNA is shown in Fig.9.9(b).



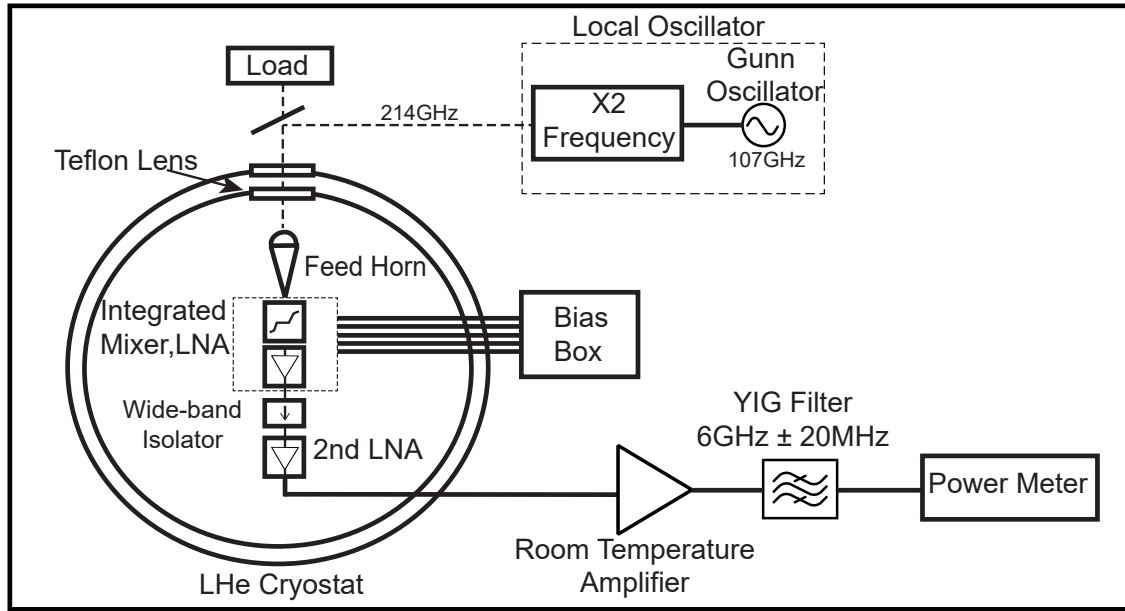


**Figure 9.9.** (a) Close-up of assembled low-noise amplifier. (b) Hybrid mixer/amplifier module. The mixer chip connects directly to the LNA via a 0.125 mm, 1 mm long wire [71], ©2015 IEEE.

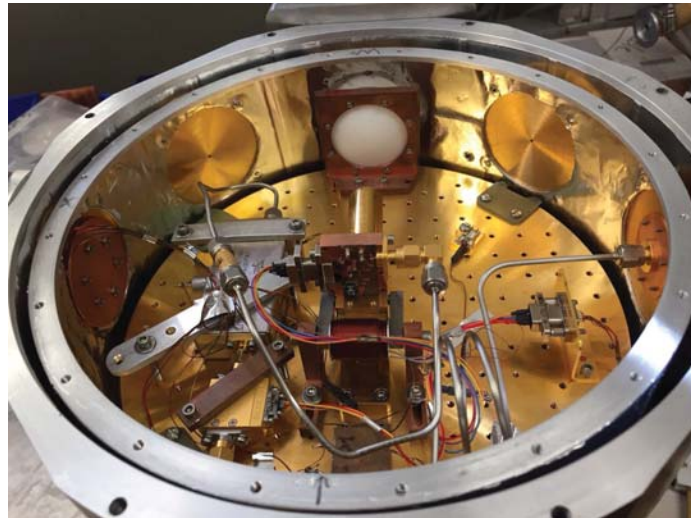
The hybrid assembly was mounted inside a liquid helium cryostat that was configured for the Y-factor measurement. A schematic diagram of the measurement setup is shown in Fig.9.10. A 214 GHz local oscillator signal was provided to the mixer using a Gunn oscillator followed by a frequency doubler. Inside the cryostat, the incoming signal was passed through a feed-horn to reach the SIS mixer. The downconverted signal goes directly to the SiGe LNA connected to the mixer. The out-coming signal then passed through a wide-band cryogenic isolator and a second cryogenic LNA (LNF-LNC4-16A) for further amplification. Then, the signal went outside the cryostat and was amplified using a room temperature amplifier (Minicircuits ZVA-183,2-18 GHz) followed by a 40 MHz YIG filter and finally entered a power meter. A photo of the setup inside the cryostat is shown in Fig.9.11.

The system was measured using the Y-factor method using ambient temperature and liquid nitrogen temperatures as the hot and cold loads, respectively. The output power was measured at an IF frequency of 6 GHz and the results are presented in Fig.9.12.(a) for both hot and cold loads. The double side band noise temperature was calculated from the output powers at hot and cold loads and the the result is



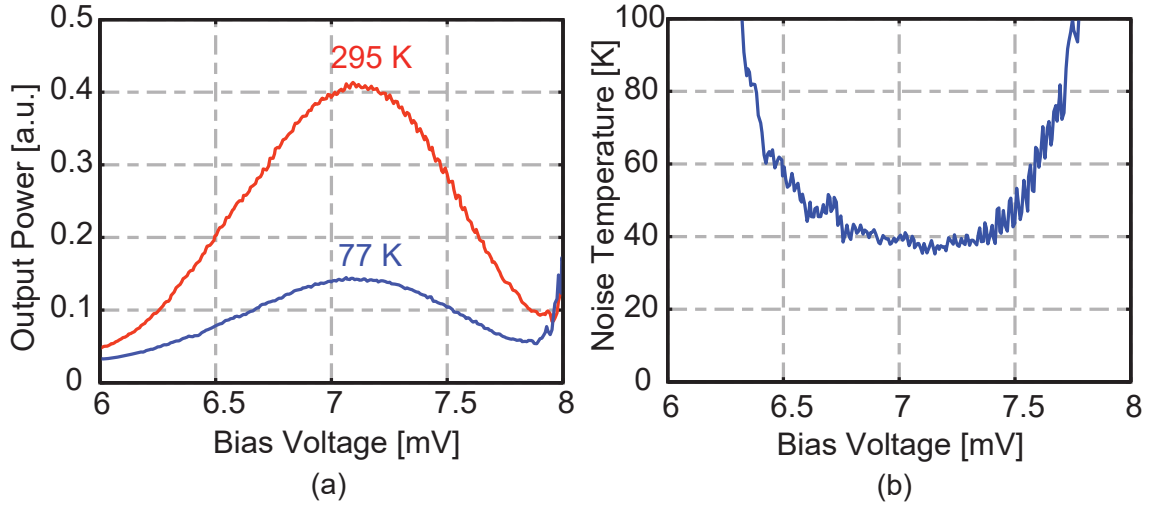


**Figure 9.10.** Block diagram of the measurement setup [72], ©2016 IEEE.



**Figure 9.11.** Photograph of the measurement setup [71], ©2015 IEEE.

shown in Fig.9.12.(b). The double side-band noise temperature of the receiver was calculated to be better than 40 K when the SIS junction is biased at 7 mV DC bias and the LNA was dissipating only  $720 \mu\text{W}$ . The noise measurement was carried out at an IF frequency centered at 6 GHz with a 40 MHz bandwidth. The noise temperature



**Figure 9.12.** (a) Output power measurement at 77 K and 295 K loads. (b) Double-sideband system noise temperature. These measurements are for an LO frequency of 214 GHz and an IF frequency of 6 GHz [71], ©2015 IEEE.

was also measured as a function of the SIS mixer bias and results are shown in Fig.9.12. (b). The minimum noise occurs when the mixer is biased at 7 mV DC voltage which corresponds to the center of the photon step on the DC-IV curve.

The results achieved in this preliminary implementation of a low power THz system show the possibility of implementing microwatt level SIS based receivers with noise temperatures comparable to conventional approaches with much higher DC power dissipation [166]. Although the results are very promising, the system is still very narrow band. In the next section, the implementation of a broadband low-power SIS receiver is described.

## 9.5 A 220 GHz SIS Mixer Integrated with a Microwatt SiGe Amplifier

In the previous section, the implementation of a narrow band SIS based receiver at a spot frequency of 6 GHz was reported. Here, we re-designed the LNA and optimized it for a wider IF bandwidth of 3-6 GHz. The SIS mixer used in this experiment is

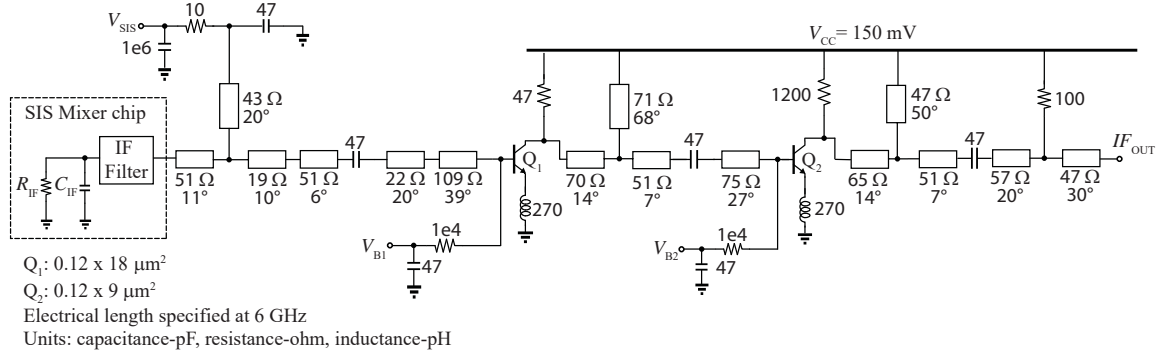
the same as that of the previous section and the IF impedance was described in Section 9.3. The details of the design, implementation, and system measurements are presented in this section which summarizes the results reported in [72].

### 9.5.1 IF Amplifier Design and Optimization

The amplifier was designed and optimized for the frequency range of 3-6 GHz. A schematic diagram of the two-stage LNA is shown in Fig.9.13. The amplifier was designed using the SiGe HBT cryogenic device models described in Chapter 6 and was optimized to operate at its nominal performance when driven by the IF impedance of the SIS mixer.

The input matching network was designed such that the intrinsic mixer capacitance ( $C_{IF}$ ) and the IF filter were absorbed into the matching network. The matching network was optimized to present the transistor with an impedance near the noise optimum impedance in the range of 3 to 6 GHz frequency. A shunt stub was included at the input to permit bias to be applied directly to the SIS junctions and was shorted to the ground using a 47 pF capacitor. To ensure broadband supply bypassing, a pair of capacitors were employed on the SIS bias line, with a 10  $\Omega$  damping resistor included to prevent resonances between the capacitors. The first stage transistor was inductively degenerated to help with the simultaneous power and noise match. The base bias was provided through a 10 k $\Omega$  resistor to prevent parasitic loading of the RF input line. The first stage transistor size was selected to be  $0.12 \times 0.18 \mu m^2$  and was biased at approximately  $0.2 \text{ mA}/\mu m^2$ . At cryogenic temperatures, the required base voltage is in the range of 1 V and the expected base current is on the order of 100 nA.

The inter-stage and output matching networks were designed to flatten the gain. A 47  $\Omega$  resistor was incorporated into the design of the inter-stage network to ensure unconditional stability and a 100  $\Omega$  resistor was included in the output matching



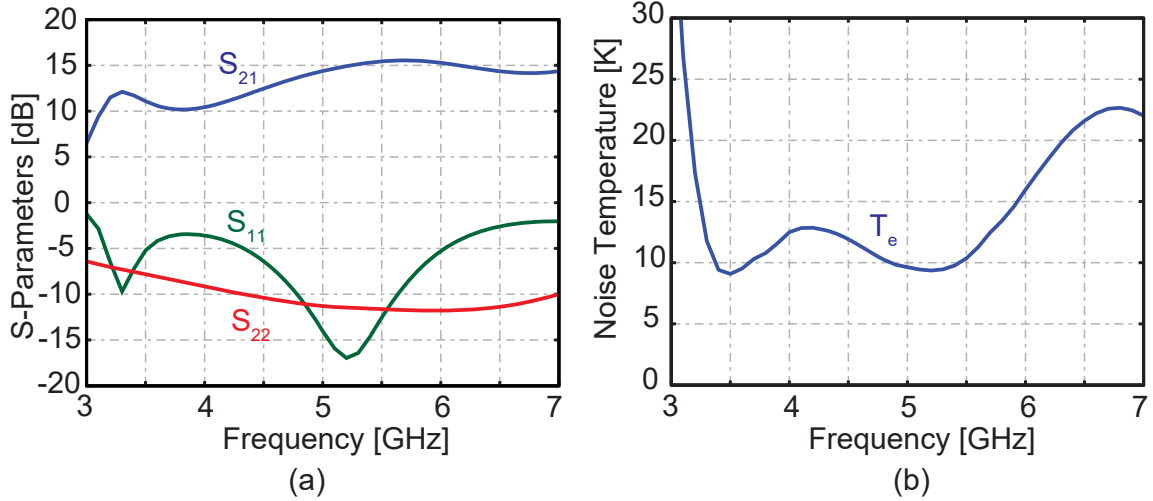
**Figure 9.13.** Schematic diagram of the low noise amplifier [72], ©2016 IEEE.

network both to improve the stability and output match. Additional bypassing (not shown in Fig. 9.13) was employed on the  $V_{CC}$  lines to ensure that the supply appeared as an ideal RF short to ground.

The LNA was simulated in NI AWR design environment and the gain and noise appear in Fig. 9.14. The simulation was carried out for the LNA driven by the equivalent model of the mixer. The amplifier was designed to run from a 150 mV collector voltage to minimize the power dissipation without impacting the noise. The amplifier was predicted to have greater than 10 dB gain and less than 16 K noise temperature over the entire 3.3 to 6 GHz frequency range while dissipating only  $90 \mu\text{W}$  DC power.

### 9.5.2 Experimental Results

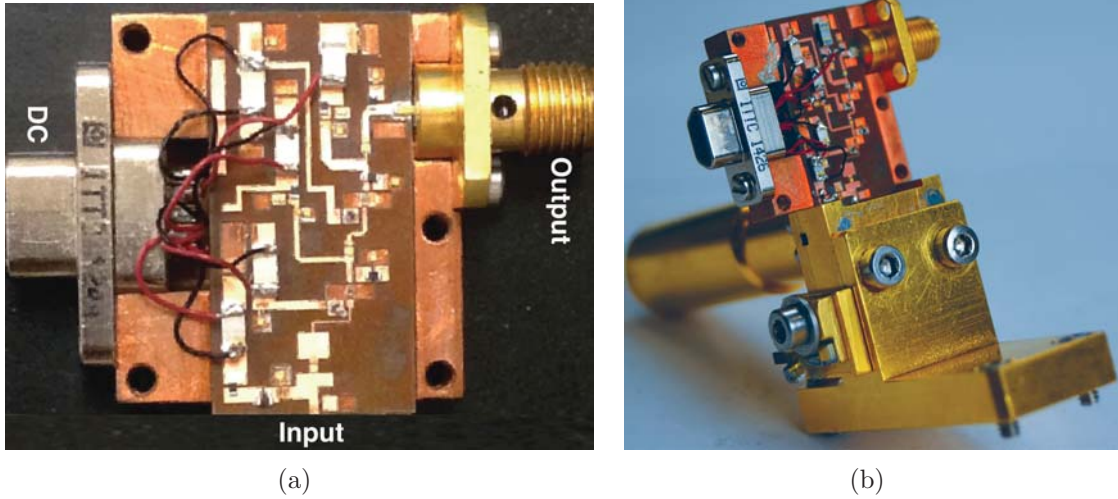
The LNA was implemented using discrete transistor from the GF BiCMOSH8P technology process together with wire bondable and surface mount resistors and capacitors. A photo of the amplifier assembly is shown in Fig.9.15(a). The matching networks were implemented on a printed circuit board (PCB) that was fabricated in house using an LPKF ProtoLaser machine [145]. A Rogers/Duroid 6002 laminate material with the thickness of  $250 \mu\text{m}$  and with the size of 12.7 mm by 25.4 mm was used for the implementation of the PCB. The board was mounted on a copper block



**Figure 9.14.** Simulated performance of the LNA driven from a  $200 \Omega$  generator impedance. The simulation also considers the  $300 \text{ fF}$  SIS capacitance and the series embedding network. The bias point for this simulation is  $I_{C1}=0.4 \text{ mA}$ ,  $I_{C2}=0.2 \text{ mA}$ , and  $V_{CC}=150 \text{ mV}$ . (a) Scattering parameters and (b) noise temperature [72], ©2016 IEEE.

that was machined and used in the experiments described in the previous section. The copper block was designed to be directly bolted to the SIS mixer module. The wire bondable capacitors were realized using thin-film metal-insulator-semiconductor (MIS) capacitors. The larger  $1 \mu\text{F}$  bypass capacitors were realized using thick film capacitors which have been characterized and found to be stable at cryogenic temperatures. All inductors were implemented using  $25 \mu\text{m}$  diameter bond wires, with an assumed inductance of  $1 \text{ nH/mm}$ . A SMA connector was mounted at the output of the amplifier enabling the connection to the output cables. A micro-D DC connector was also used to provide DC bias to the circuit. The amplifier block was then connected to the mixer block and a photo of the integrated SIS-mixer/SiGe-LNA is shown in Fig.9.15(b).

The hybrid circuit was then mounted inside a liquid helium cryostat for further testing at cryogenic temperatures. The liquid helium cryostat was configured for Y-



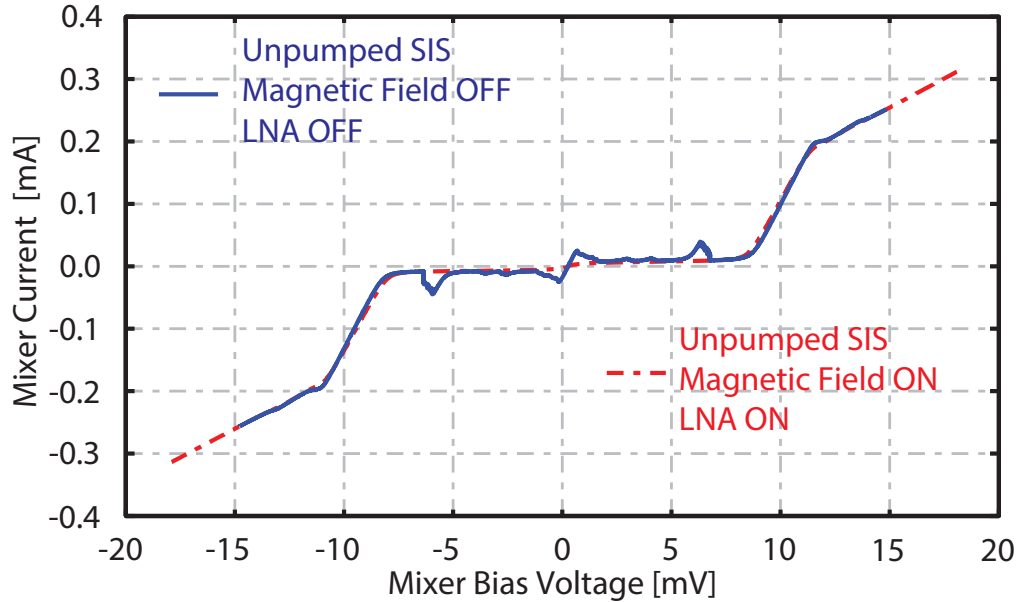
**Figure 9.15.** (a) Photograph of the assembled low-noise amplifier. The dimensions of the PCB are 12.7 mm by 25.4 mm. (b) Photograph of the integrated mixer/LNA assembly. The bias for the mixer is supplied through the micro-D connector on the LNA block [72], ©2016 IEEE.

factor measurements. The measurement setup used this experiment is identical to the one presented in Fig.9.10.

DC bias was applied to the SIS mixer through a programmable room temperature bias box, whereas Keithley 2401 Sourcemeters (not shown) were employed to bias and monitor the LNA. A tunable frequency-multiplied LO source was quasi-optically coupled to the beam of the SIS mixer through a room temperature wire grid and the diplexed RF/LO signal entered the cryostat through a 0.5 mm thick teflon window. At the output of the mixer/LNA block, an isolator followed by an additional cryogenic low noise amplifier<sup>2</sup> (Low Noise Factory model LNF-LNC-4\_16A [168]) was employed to further amplify the IF signal prior to exiting the cryostat. It should be noted

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<sup>2</sup>Due to the relatively low gain of the SiGe LNA, deployment of a second stage cryogenic LNA is necessary in our measurement setup to suppress the noise of the warm IF chain outside of the cryostat. The commercially available cryogenic LNA used for this purpose dissipates 15 mW DC power. In the next section of this dissertation, we present the results of a high-gain low-power LNA integrated with an SIS mixer which eliminates any need for the use of a second stage power-hungry cryogenic LNA.

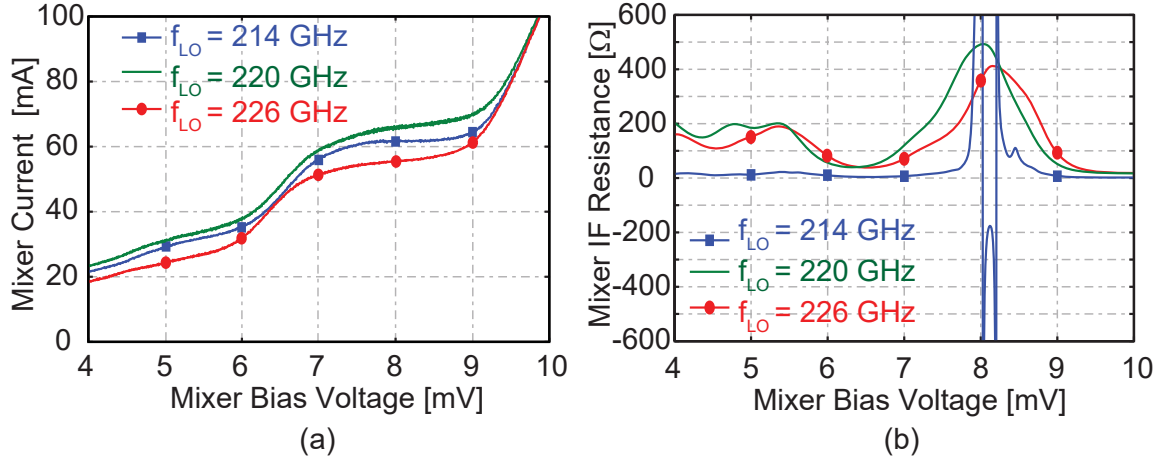


**Figure 9.16.** Mixer current–voltage characteristics with the LO signal disabled. The blue line is the baseline I–V curve taken while the SIS magnetic bias was disabled and the LNA was powered down. The red curve was measured with the SIS magnetic bias enabled and the LNA powered. A series resistance of approximately  $15\ \Omega$  has not been de-embedded from the measurement [72], ©2016 IEEE.

that the isolator was already installed in the test-bed used for these experiments and was therefore included in the IF signal chain. However, since the output of the SiGe amplifier is matched to  $50\ \Omega$ , the isolator was not critical in achieving the results presented below. The performance of both the isolator and the second-stage amplifier deteriorate below 4 GHz, limiting the measurement accuracy in this frequency range. An additional amplifier was employed at room temperature. Finally, the IF signal was band-limited to 40 MHz using a YIG tuned bandpass filter before power detection using a commercial power meter. A set of baseline measurements were also carried out in which the output of the SIS mixer block was directly connected to the isolator through a SMA adapter, in the absence of the integrated SiGe LNA.

Once the measurement setup was ready, the receiver was cooled down to 4 K. First, the DC-IV curve of the SIS mixer was measured for a case in which LO signal





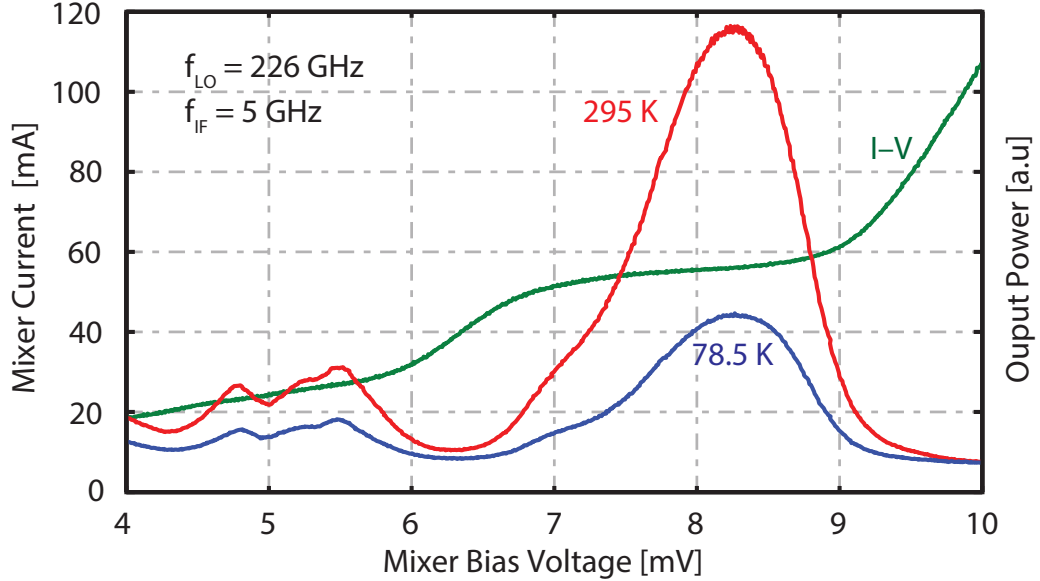
**Figure 9.17.** DC properties of the SIS mixer when pumped at 214, 220, and 226 GHz. (a) Pumped I–V curves and (b) incremental resistances [72], ©2016 IEEE.

was off. Fig.9.16 shows the DC-IV curves and no interaction between the SIS mixer and the LNA was observed while the LNA was biased at its nominal points<sup>3</sup>.

Later, the LO pump was applied to the junction and the DC-IV curves were recorded. Fig.9.17. (a) shows the pumped IV curves at three LO frequencies of 214, 220, and 226 GHz. The center of the photon steps happens at 8 mV which is the nominal bias for the SIS mixer since the output power of the SIS mixer maximizes at this bias point. A spline-fit was applied to the IV curves to enable extraction of IF resistance from these results. Fig.9.17. (b) shows the  $r_{IF}$  for three different LO frequencies. From these measurement results, the IF resistance of the SIS mixer is approximately 400 to 500  $\Omega$  which is much higher than 100 to 200  $\Omega$  which the LNA was initially designed for based on the preliminary calculations in Section.9.3. Thus, it is expected that the LNA performance may degrade from simulations as it is driven with a much higher impedance than the range it was designed for.

<sup>3</sup>However, when the amplifier was biased for higher power, pumping of the SIS mixer was observed. This may be attributed to bias oscillation of the module or amplifier instability associated with a potential resonance between the module bypass capacitors and the cryostat feedthrough capacitors. No such pumping was observed at the lower bias level (less than 150  $\mu$ W) used in our experiment.

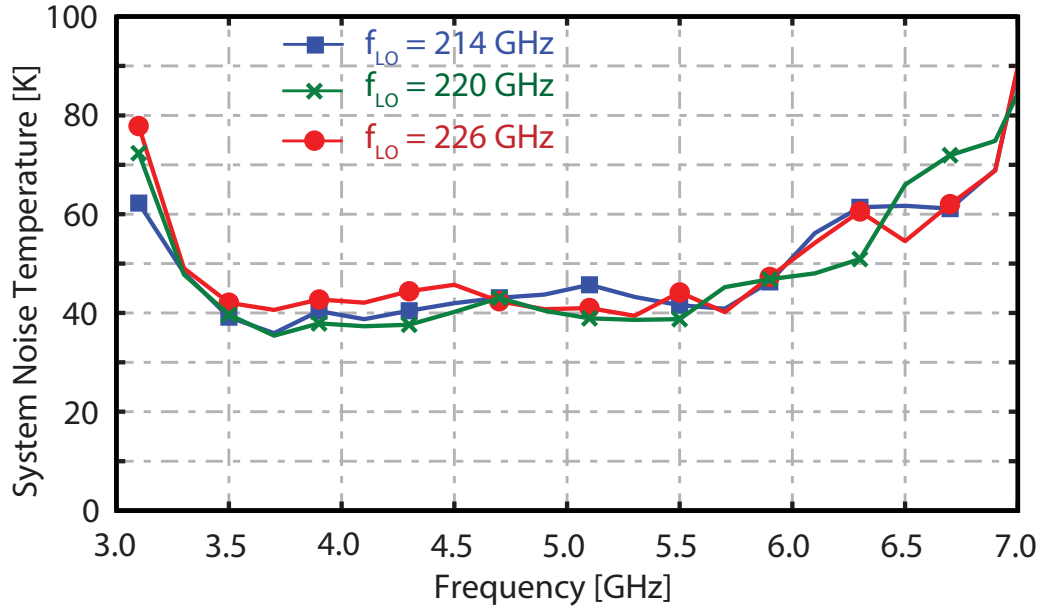




**Figure 9.18.** Output power measured with 295 K and 78.5 K loads with the LO signal tuned to 226 GHz. Also shown is the pumped IV curve. These data were recorded with the low noise amplifier biased for a power dissipation of  $68 \mu\text{W}$  ( $I_{C1} = 0.25 \text{ mA}$ ,  $I_{C2} = 0.2 \text{ mA}$ , and  $V_{CC} = 0.15 \text{ V}$ ) [72], ©2016 IEEE..

The SIS differential resistance was found to be negative at 214 GHz. This phenomena happens commonly in SIS mixers and is due to the tuning circuit being inductive at frequencies slightly below the center of the tuning resonance. Further discussion regarding the operation of LNAs with negative generator impedance could be found in [169].

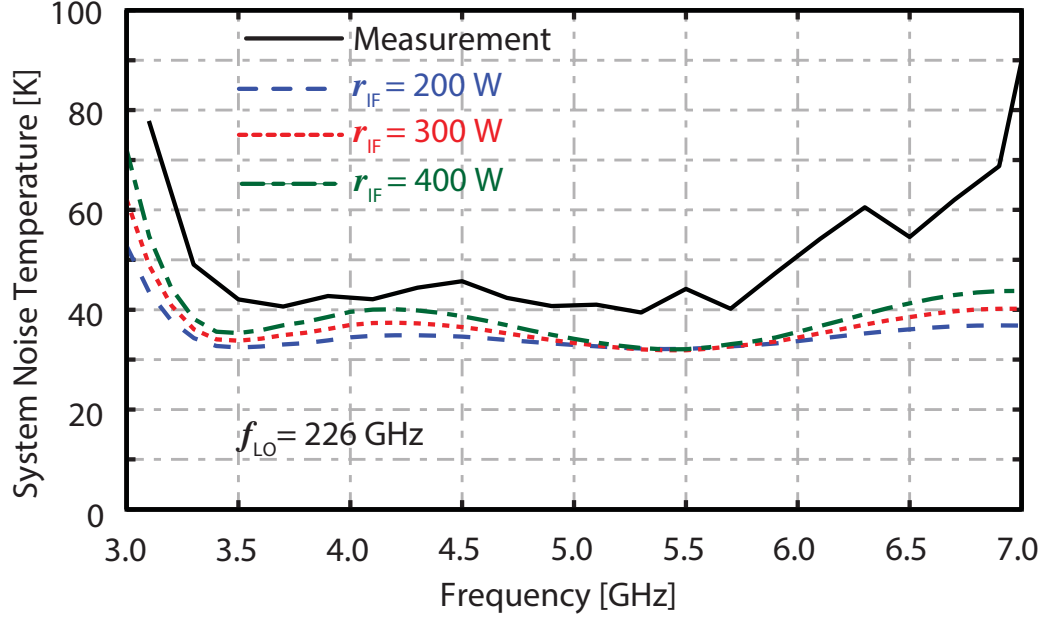
After the DC measurement, the double-sideband (DSB) noise temperature of the SIS-mixer/SiGe-LNA receiver was measured using the Y-factor method. Ambient temperature and liquid nitrogen loads were applied to the input of the setup as the hot and cold loads for the Y-factor measurements, respectively. The measurements were performed at an IF frequency range of 3 to 7 GHz with 200 MHz frequency spacing. Fig.9.18 shows the output power as well as the I-V curve of the receiver at the LO frequency of 226 GHz. The peak of the output power occurs at approximately 8 mV which is near the photon step as expected.



**Figure 9.19.** Double-sideband system noise temperature with the LNA biased at a power dissipation of  $90 \mu\text{W}$  ( $I_{C1} = 0.4 \text{ mA}$ ,  $I_{C2} = 0.2 \text{ mA}$ , and  $V_{CC} = 0.15 \text{ V}$ ) [72], ©2016 IEEE.

Next, the mixer was biased at approximately 8 mV DC voltage and the DSB noise temperature of the system was calculated using the Y-factor data. Results are presented in Fig.9.19 for the LO frequencies of interest. The LNA was biased at  $90 \mu\text{W}$  DC power for all these measurements. Based on knowledge of the gain of individual components in the IF path, the gain of the SiGe amplifier was estimated to be 16 dB at 5 GHz. This gain is consistent with the simulation results shown in Fig. 9.14. A double side-band noise temperature of less than 50 K was obtained for the system over the 3.3-6 GHz frequency range for three different LO frequencies (See Fig.9.19).

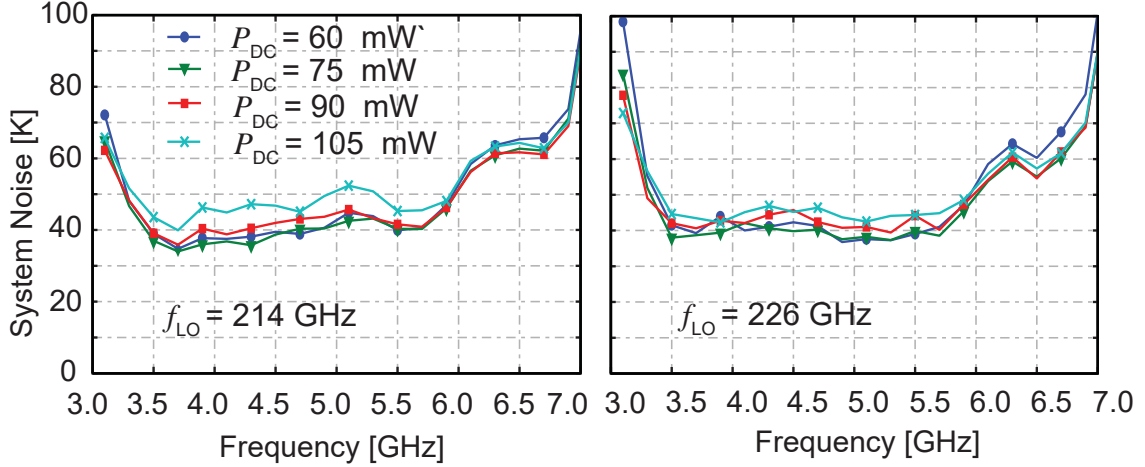
The system noise temperature measured for an LO frequency of 226 GHz was compared to simulation results for a range of values of  $r_{IF}$  (see Fig. 9.20). For these simulations a room temperature optics loss of 0.2 dB was assumed and the mixer DSB noise temperature and gain were taken as 12.5 K and 3 dB, respectively. It can be



**Figure 9.20.** Simulated and measured system noise temperature for a local oscillator frequency of 220 GHz. The simulated bias point of the low noise amplifier corresponds to a power dissipation of  $90 \mu\text{W}$  ( $I_{C1} = 0.4 \text{ mA}$ ,  $I_{C2} = 0.2 \text{ mA}$ , and  $V_{CC} = 0.15 \text{ V}$ ). A room temperature optical loss of 0.2 dB and a mixer gain/noise temperature of 3 dB/12.5 K were assumed.  $C_{IF}$  was set to 300 fF and  $r_{IF}$  was swept from 200 to 400  $\Omega$  in 100  $\Omega$  steps [72], ©2016 IEEE.

seen that the disagreement between simulation and measurement is below 25% over the majority of the frequency range.

Next, the possibility of operating the receiver at lower DC power consumption was also investigated. The LNA DC power was swept from  $100 \mu\text{W}$  down to  $60 \mu\text{W}$  and the receiver noise temperature is shown in Fig.9.21 for LO frequencies of 214 and 226 GHz. For these measurements, the current of the first stage was swept and the  $V_{CC}$  and the bias point of the second stage was held constant at 150 mV and 0.2 mA, respectively. Remarkably, the DC power reduction to  $60 \mu\text{W}$  did not have a significant impact on the noise performance. The gain was simulated to drop by 2 dB when decreasing the DC power from 90 to  $60 \mu\text{W}$ . It should be noted that at such a low power consumption linearity may be a concern. However, as shown in [70],

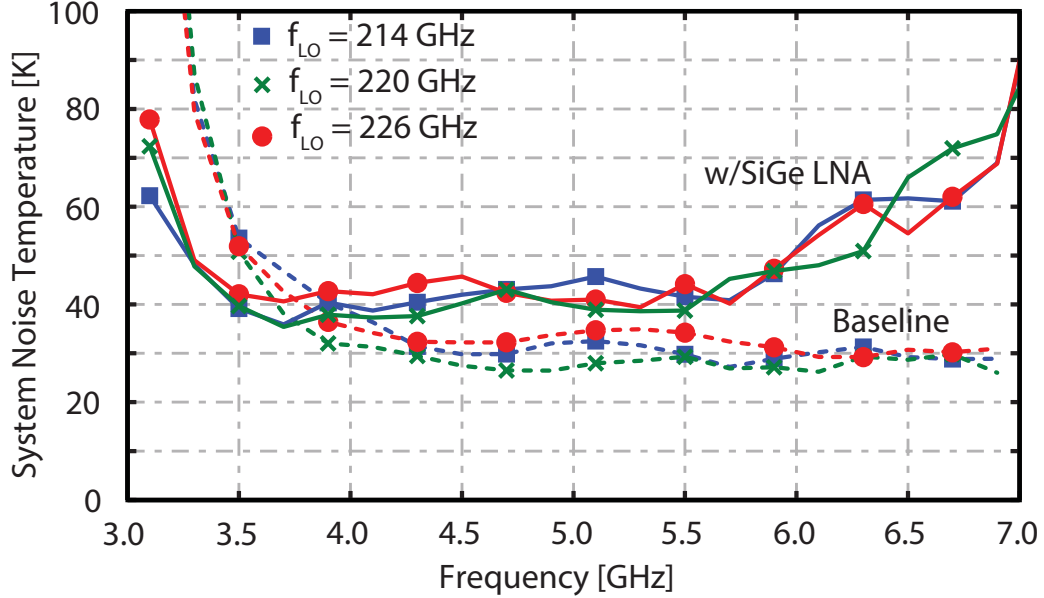


**Figure 9.21.** DSB noise temperature as a function of power consumption for local oscillator frequencies of 214 GHz and 226 GHz. The power was reduced by adjusting the first-stage bias current while keeping  $V_{CC}$  and  $I_{C2}$  fixed at 0.15 V and 0.2 mA, respectively [72], ©2016 IEEE.

the linearity is not impacted through operation at low  $V_{CC}$ , provided the HBTs are not in deep-saturation.

A baseline measurement was carried out in a second cool down using the SIS mixer in the conventional receiver setup reported in [166]. In this case, the SIS mixer was followed by an isolator and a commercial cryogenic LNA with 15 mW of DC power. Results are compared to our low-power SiGe-LNA/SIS-mixer receiver in Fig.9.22. The low-power receiver provides a double side band noise temperature within 15 K of the baseline measurement data.

The results presented in this section proved the feasibility of implementing a broad-band low-power SIS based receivers leveraging cryogenic SiGe LNAs. In the next step, we tried to improve the performance of the LNA by increasing the gain and bandwidth of the amplifier while maintaining the same level of noise and power dissipation so that there is no need for any further cryogenic amplification in the receiver chain after the integrated SIS-Mixer/SiGe-LNA circuit. In the next section, the design and



**Figure 9.22.** Comparison of baseline high-performance system with the system employing the proposed ultra-low-power SiGe IF amplifier [72], ©2016 IEEE.

implementation of an SIS receiver with a higher gain and better noise performance while still dissipating microwatt level DC power is described.

## 9.6 A High-Gain Low-Noise SIS Receiver Utilizing a 300 $\mu$ W SiGe IF LNA

Thus far, we described the implementation of a microwatt level SiGe LNA integrated with an SIS mixer and characterized the receiver performance. The noise temperature of the chain was competitive with the conventional receivers, however, due to low gain of the amplifier (10 dB) presented in the previous section, a second stage of cryogenic amplification was required to suppress the noise contribution of the warm IF network. Since this amplifier consumed 15 mW, the overall power consumed by the cryogenic electronics was still quite high. Demonstrating that a high-gain receiver can be realized without requiring any power-hungry cryogenic electronics is an important step towards scaling such systems towards the thousand-element level.

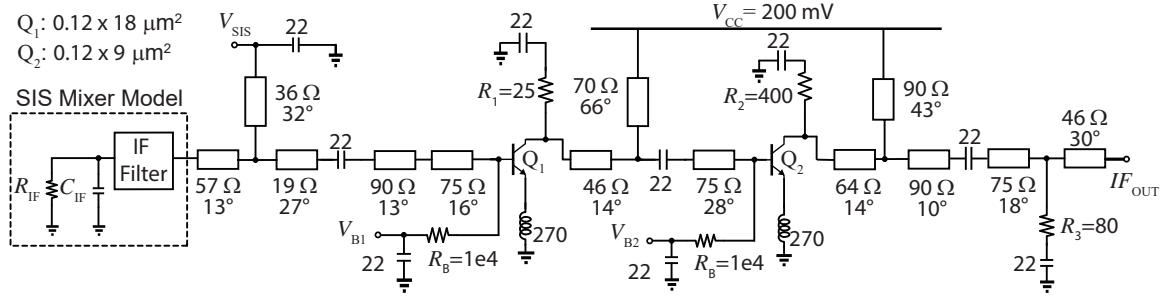
In this section, the SiGe LNA is re-designed and optimized to achieve higher gain and better noise performance while still dissipating microwatt level DC power. The details of the design, characterization of the amplifier, and the system integration will follow in the next sections. The content of this section summarizes the results reported in [73].

### 9.6.1 LNA Design and Optimization

A two stage LNA was designed and optimized for direct connection to an SIS mixer. The mixer used in this study consisted of a distributed series array of three SIS junctions [166], similar to the mixers presented in the previous sections. The output impedance of the SIS mixer was modeled as a  $150\ \Omega$  resistor in parallel with a  $300\ \text{fF}$  capacitor. The resistance was calculated using the DC-IV curve of the SIS junction and the capacitance was approximated based on the geometry of the junctions and the tuning circuits on the mixer chip as described in Sec.9.3.

The LNA was designed leveraging the SiGe HBT transistor models presented in Section 6. A schematic diagram of the amplifier is shown in Fig.9.23. The amplifier was designed to be implemented using discrete SiGe HBT transistors from the GF BiCMOS8HP technology platform.

The LNA was simulated with a generator impedance equal to the IF impedance of the SIS junction. The input matching network was designed to provide a noise match at the input while maintaining a good power match. The first stage transistor was inductively degenerated in order to improve the power match. A shunt stub at the input matching network was AC grounded using a  $22\ \text{pF}$  capacitor and was utilized to bring DC voltage to the SIS junction. The SIS junction was AC coupled to the input of the LNA using a series  $22\ \text{pF}$  capacitor in the signal path. The base of the first stage transistor was biased through a  $10\ \text{k}\Omega$  shunt resistor. The size of the first



**Figure 9.23.** Schematic diagram of the amplifier. Electrical length is specified at 6 GHz. Units are as follows: Capacitors-pF, Resistance-Ohm, Inductance-pH [73], ©2017 IEEE.

stage transistor was selected to be  $0.12 \times 18 \mu m^2$  and the DC current was 1.4 mA which was a compromise between DC power consumption and noise performance.

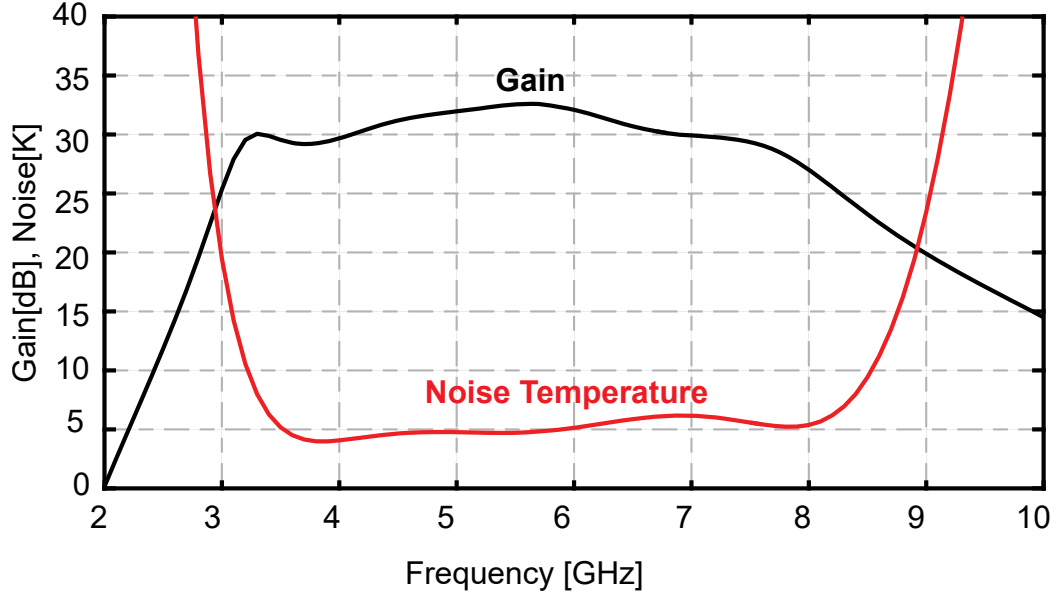
The inter-stage matching network was designed to flatten the gain at the high end of the frequency band. The  $R_1, R_2, R_3$  shunt resistors were employed into the design to ensure stability. The base of the second stage transistor was biased through a shunt 10 kΩ resistor. The second stage transistor size was elected to be  $0.12 \times 9 \mu m^2$  operating at a DC current of 1 mA.

The second stage of the amplifier was designed to provide further gain. The output matching network was designed to provide 50 Ω impedance at the output of the LNA. The amplifier was designed to operate at supply voltages in the range of 150 mV to 400 mV corresponding to DC current of 2 to 2.4 mA.

The amplifier was simulated in the NI AWR design environment and was designed to provide 30 dB gain and less than 7 K noise temperature over the 4–8 GHz frequency band. Fig.9.24 shows simulated results for the LNA driven by the SIS mixer model.

### 9.6.2 Measurement Results

The LNA was assembled using discrete SiGe HBT devices from the GF BiCMOS technology process. The amplifier was packaged in a module that was previously designed to mate with the SIS mixer block. Fig.9.25 shows a close up picture of the



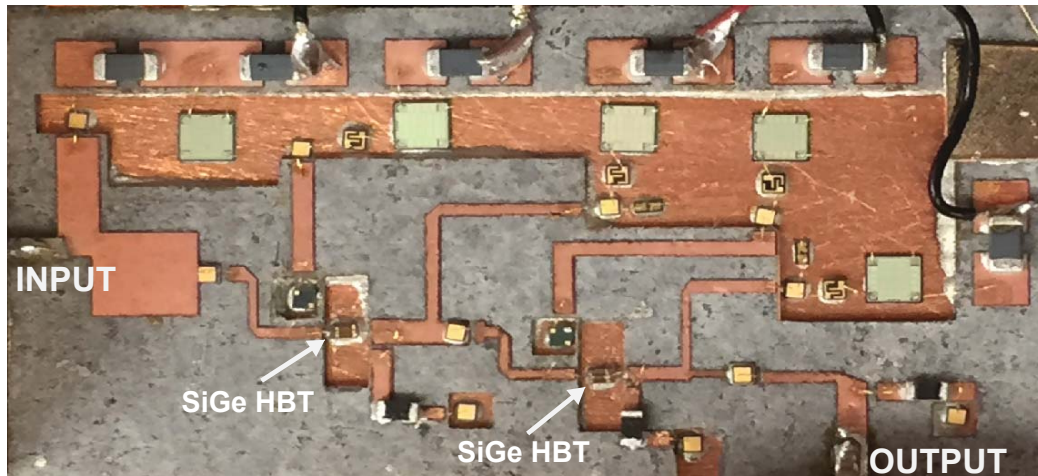
**Figure 9.24.** Simulated noise and gain of the LNA driven from the SIS mixer equivalent model. The amplifier was biased at  $I_{c1}=1.4$  mA,  $I_{c2}=1$  mA, and  $V_{cc}=200$  mV [73], ©2017 IEEE.

assembly. The matching networks were implemented on a 0.25 mm thick RT/Duroid 6002 substrate with the size of 13 mm  $\times$  26 mm. The resistors and capacitors in the amplifier design were implemented using wire bondable and surface mount components. The SiGe HBT transistors were mounted inside the cutouts on the PCB and were wire bonded to the circuit board. Ferrite beads were also incorporated into the assembly on the DC lines between the bypass capacitors to prevent any probable resonance between them.

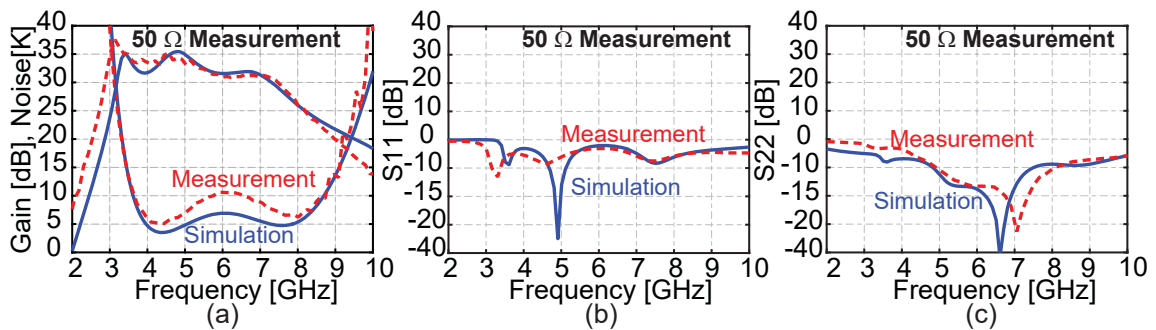
### 9.6.3 LNA Characterization

The LNA performance was first verified prior to integration with the SIS mixer. The amplifier was measured inside the cryostat in a  $50\ \Omega$  environment and results are shown in Fig. 9.26. A SMA connector was mounted at the input of the LNA module to enable measurement of the amplifier prior to the connection to the SIS mixer. The LNA was then mounted inside the cryostat and the gain and noise and



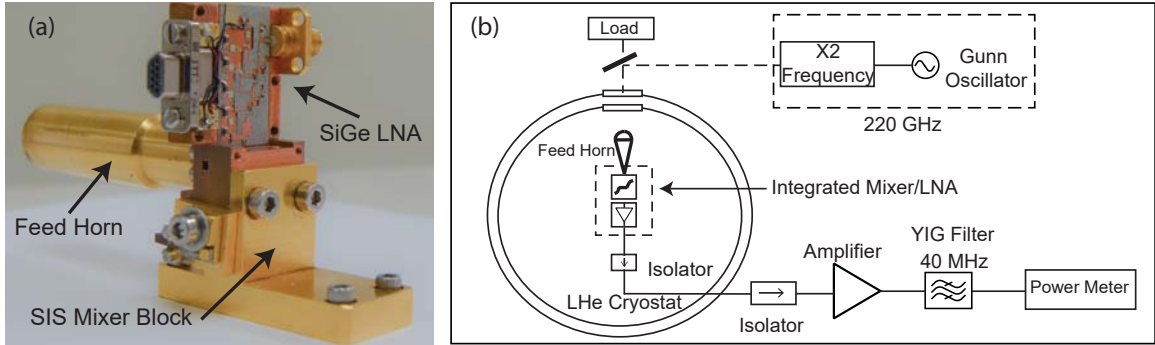


**Figure 9.25.** A photograph of the assembled LNA circuit [73], ©2017 IEEE.



**Figure 9.26.** LNA performance in a 50- $\Omega$  environment. Dashed lines are measurement results and solid lines are simulations. The amplifier was biased at  $I_{c1}=1.4$  mA,  $I_{c2}=1$  mA, and  $V_{cc}=200$  mV (a) Gain and noise temperature at 15 K temperature. (b) Input return loss of the LNA at 50- $\Omega$  generator impedance. (c) Output return loss of the LNA [73], ©2017 IEEE.

scattering parameters were measured at 15 K physical temperature. Fig. 9.26 shows the measurement results agree well with the simulations. The 3 dB difference between the simulated noise and measurements at the middle of the band could be due to the discontinuity between the input SMA connector and the PCB which was not modeled in the simulations.

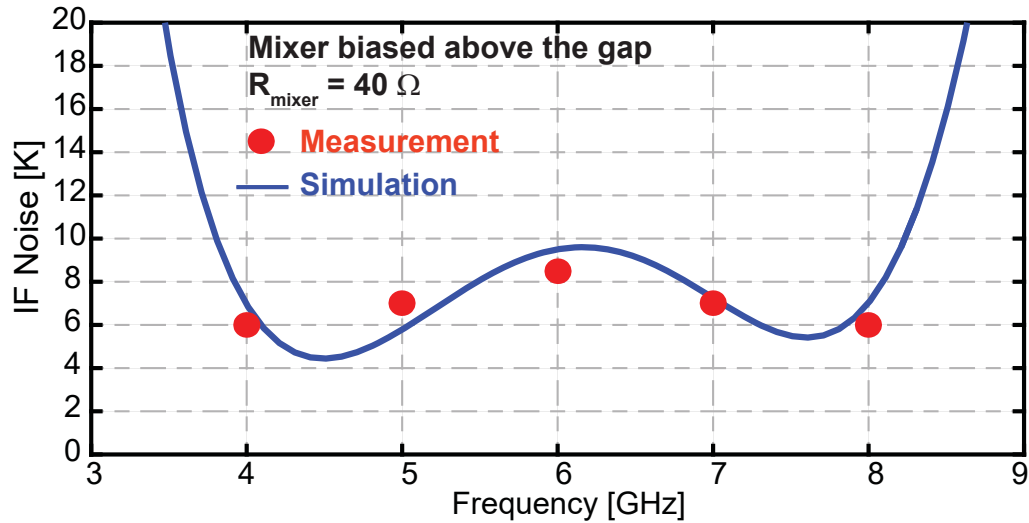


**Figure 9.27.** (a) A photo of the LNA block directly connected to the Mixer block. (b) A block diagram of the measurement setup [73], ©2017 IEEE.

#### 9.6.4 Receiver Performance

After the characterization of the LNA, the SMA connector at the input of the LNA was removed and the LNA module was directly bolted to the mixer block. The electrical contact between the mixer and the amplifier was made via pressure contact using a 1 mm long BeCu wire with a diameter of 0.125 mm. A photograph of the assembly is shown in Fig.9.27. (a). The SiGe-LNA/SIS-Mixer assembly was mounted inside a liquid helium cryostat for testing at 4 K. A schematic diagram of the measurement setup is presented in Fig.9.27. (b). The measurement setup was configured for Y-factor measurement. A local oscillator signal of 220 GHz was generated using a Gunn oscillator and a frequency doubler. A wire grid polarizer was used as an LO coupler to combine the LO and signal beams. The combined beam was focused by a cold Teflon lens onto the corrugated feed horn of the SIS mixer block. The downconverted signal coming out of the cryostat was further amplified using a room temperature amplifier that was followed by a 4–8 GHz isolator. The output signal was then guided to a YIG filter with a bandwidth of 40 MHz followed by a power meter. The room temperature IF chain was characterized and the gain measured to be 40 dB with a noise temperature of 270 K.

Prior to system measurements, the performance of the LNA was verified using the SIS mixer shot noise method as described in [170]. The SIS mixer was biased above

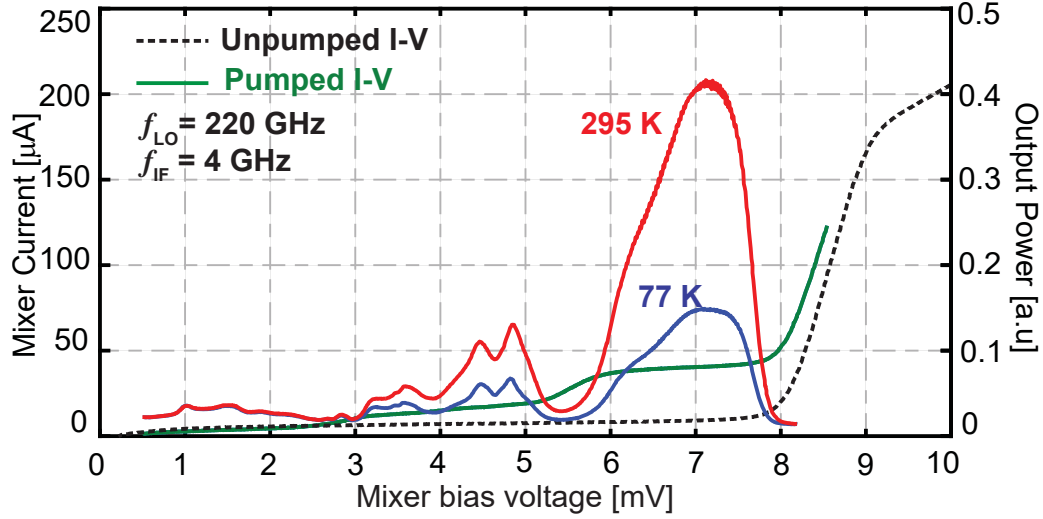


**Figure 9.28.** The IF noise obtained from the shot noise experiment compared to simulation. The LNA was biased at  $I_{c1}=1.2$  mA,  $I_{c2}=0.8$  mA, and  $V_{cc}=150$  mV [73], ©2017 IEEE.

the gap at 12 mV DC bias to avoid quantum susceptance associated with the junctions and the differential resistance of the SIS mixer at this bias point was measured to be approximately  $40 \Omega$ . The IF noise of the LNA was measured at an IF frequency of 4 to 8 GHz. Fig.9.28 shows the simulation along with measurements. The simulation was carried out assuming a generator impedance of  $40 \Omega$ , which is based on the calculated output impedance of the SIS mixer during the shot noise measurement. Excellent agreement between simulation and measurements were obtained using the SIS shot noise method.

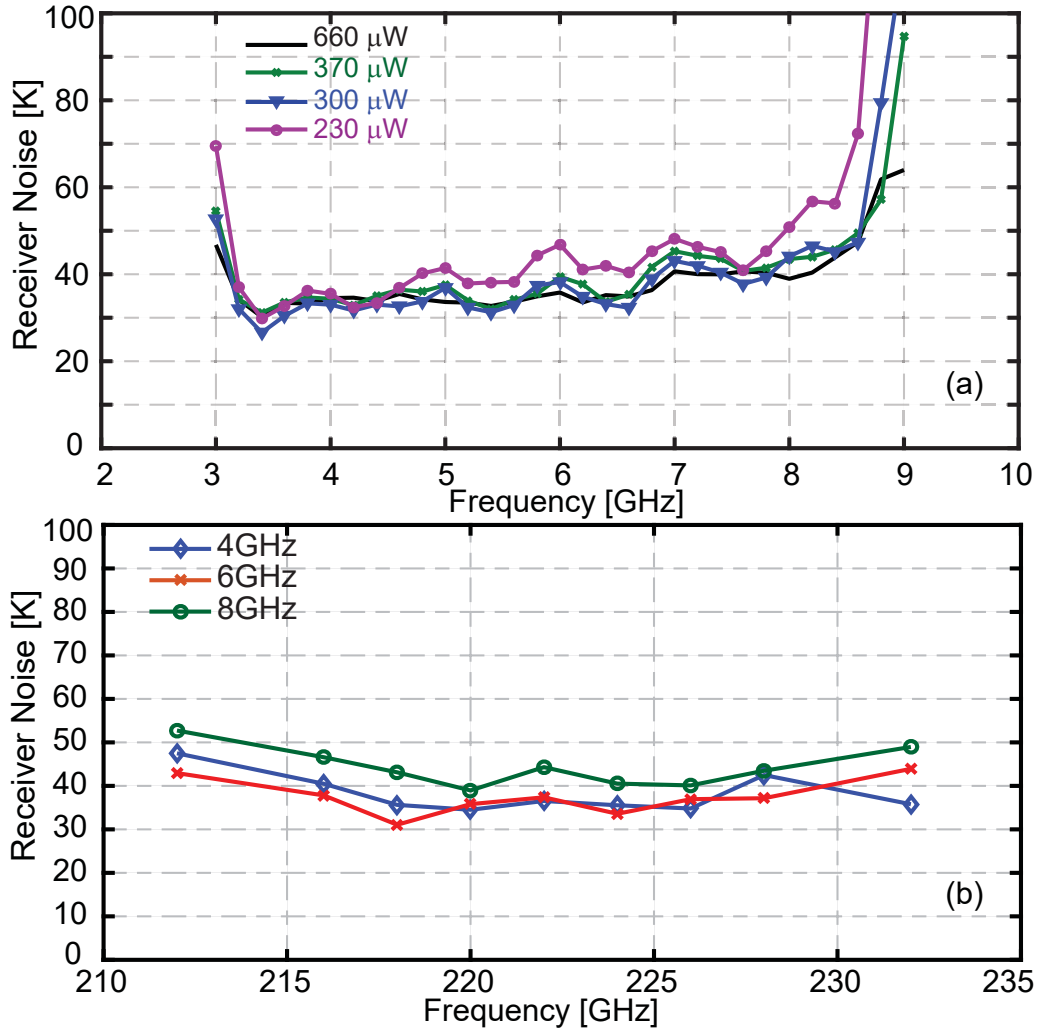
After characterizing the LNA using the SIS mixer shot noise method, the DC characteristics of the SIS mixer were measured. In Fig.9.29, the dashed line shows the unpumped DC I-V curve of the SIS mixer. No interaction between the SIS mixer and the LNA was observed in the DC-IV curves.

Next, the SIS mixer was pumped with a 220 GHz LO signal and the RF performance was measured. The cryogenic SiGe LNA attached to the SIS mixer was biased for a power consumption of  $300 \mu\text{W}$  to achieve the nominal performance. Fig.9.29



**Figure 9.29.** The SIS mixer DC and RF characteristics. The dashed line shows the unpumped I-V curve and the green solid line shows the pumped I-V curve with a 220 GHz LO signal. The hot and cold load measurement was carried out using a room temperature and liquid nitrogen load. The LNA was biased at  $I_{C1}=1.2$  mA,  $I_{C2}=0.8$  mA, and  $V_{CC}=150$  mV [73], ©2017 IEEE.

shows the output power of the receiver chain at an IF frequency of 4 GHz for the liquid nitrogen and ambient temperature loads at the input of the receiver. The peak of the output power was measured at the center of the photon step, which was located at a mixer bias voltage of approximately 7 mV. Through the Y-factor measurement, the double side band (DSB) noise temperature of the receiver was measured and results are presented in Fig.9.30. The measurement was made with the LNA biased at different DC power levels ranging from 660–230  $\mu$ W. The noise temperature stayed between approximately 30 K to 40 K when the DC power was swept from 660  $\mu$ W down to 300  $\mu$ W. A marginal increase in the noise temperature was observed when the DC power was reduced to 230  $\mu$ W. The noise temperature achieved in this work is within 5 K of a baseline measurement using a commercial LNA that dissipated 15 mW of power. The obtained result are very promising as they show a receiver that can operate at microwatt DC power levels while providing competitive noise performance in comparison to conventional SIS receivers.



**Figure 9.30.** Receiver performance when LNA was biased at  $I_{C1}=1.2$  mA,  $I_{C2}=0.8$  mA, and  $V_{CC}=150$  mV which corresponds to  $300 \mu\text{W}$  DC power. (a) Double side-band system noise temperature of the low power SiGe-LNA/Mixer at  $f_{LO}= 220$  GHz at different power levels for the LNA. (b) Receiver noise temperature over the range of 212-232 GHz local oscillator frequency and IF spot frequencies of 4, 6, and 8 GHz [73], ©2017 IEEE.

The performance of the SiGe-LNA/SIS-mixer receiver was also characterized at different LO frequencies and results are shown in Fig.9.30. (b). The local oscillator frequency was swept from 212 to 232 GHz and the noise temperature was measured at IF frequencies of 4, 6, and 8 GHz. The results shows that the noise varies  $\pm 5$  K over this band.

**Table 9.1.** State-of-the-art SIS receivers [73], ©2017 IEEE.

	$T_{RX}$ K	$BW$ MHz	$LNAP_{DC}$ mW	$G$ dB	$\alpha$ $MHz/mW \cdot K^2$
[1]	75	2000	8	32	$\sim 0.023$
[172]	16-20	6000	7.7	35	$\sim 0.39$
[173]	43	6000	20	25	$\sim 0.063$
[174]	45-57	8000	8.2	30-35	$\sim 0.16$
This work [73]	27-47	5500	0.3	30	$\sim 1.6$

The improvement in measurement time that may be achieved using an FPA can be determined by considering number of pixels and the bandwidth and sensitivity of each pixel in comparison to that of a single pixel receiver. A metric which may be used to evaluate the scalability of a single pixel is  $\alpha = B_{MHz}/(T_{SYS}^2)(P_{LNA,mW} + P_{IF\ cable,mW})$ , where  $B_{MHz}$  is the IF bandwidth in MHz,  $T_{SYS}$  is the system noise temperature and is equal to the receiver noise temperature plus the antenna noise temperature,  $P_{LNA,mW}$  is the power consumption of the IF LNA in mW, and  $P_{IF\ cable,mW}$  is the power consumption in mW associated with cooling the IF cable. This metric is appropriate for comparison of different results since it quantifies the ratio of integration time to overall DC power consumption.

The performance of the integrated SIS-Mixer/SiGe-LNA module is compared to other published results in Table 9.1. Assuming an antenna temperature of 25 K and 0.6 mW for  $P_{IF\ cable,mW}$  [171],  $\alpha$  was computed for each of the results. The value of 1.6 MHz/K<sup>2</sup>mW reported here is four times higher than the next best result. Thus, the results presented in this work represent a significant step forward in terms of developing the technology required to make scaled THz focal plane arrays practical.

## 9.7 Summary

Modern sub-millimeter SIS based receivers can achieve noise temperatures close to the fundamental quantum limit. The only way to increase the throughput of

these system is to increase the number of elements in a receiver. Consequently, the implementation of large-scale focal plane arrays are desired to enable wide-ranging astronomical surveys in a reasonable amount of time using SIS based receivers.

In this chapter, we described some challenges associated with the implementation of compact SIS based receivers and we demonstrated that the power consumption of cryogenic LNAs should not be a barrier in the future adoption of this technology in practical large-scale SIS receivers. The details of the design and implementation of an ultra low-power SiGe-LNA/SIS-mixer receiver with high gain and comparable noise performance with the state of the art was presented for an IF bandwidth of 4 to 8 GHz.

A logical future step should be focused on leveraging ultra low-power integrated circuit cryogenic LNAs, similar to that described in Chapter 8, in the design of SIS based receivers to achieve a much more impact integration to implement many pixel focal plane array inside a single cryogenic cooler.

## CHAPTER 10

### CONCLUSION AND SUGGESTED FUTURE WORK

#### 10.1 Summary and Conclusions

Low-power cryogenic low noise amplifiers are desired for the implementation of large-scale cryogenic sensing systems. Recently, SiGe HBT cryogenic LNAs have emerged as an attractive choice for the implementation of cryogenic amplifiers. In the first part of this dissertation, we investigated the fundamental limits of SiGe HBT operation at cryogenic temperatures at reduced supply voltages for low power purposes. A theoretical basis was developed for describing the noise performance of the devices near saturation region. Next, small signal and noise models were developed for SiGe HBTs at different temperatures over a wide range of bias points and the validity of these models were verified at low supply voltages through experimental measurements. Leveraging these models, several ultra low-power cryogenic LNAs were designed and implemented. The promising results achieved in this study demonstrates the possibility of designing cryogenic low noise amplifiers with microwatt level DC power consumption. The adoption of this technology could be beneficial for the future large-scale sensing systems for Quantum computing and THz astronomy applications.

Modern high speed integrated circuits are desired to operate at high current densities to achieve a higher unity gain cutoff frequency. However, several physical mechanisms appear at high current density operation which could limit the device performance and are not fully captured in the standard small-signal and noise models.



Unfortunately, there has been very limited work done on the cryogenic noise model limitations at high injection region in the past.

Using a systematic approach, some limitations of the standard noise model were investigated in this work for the operation at high current densities. The results of our experiment show that an accurate extraction of the device model parameter plays a significant role in the model predictions at high current densities. In particular, an accurate extraction of the device transconductance is contingent upon the emitter parasitic resistance value. Further study is required to investigate and propose a more accurate extraction technique for a device operating at high current densities. We believe that an accurate extraction of the device parameter is only a part of the model limitation at high currents and there could be other contributing factors which should be studied in further detail in future.

As a final step, several low-power SiGe LNAs were designed and optimized for a direct connection to superconductor-insulator-superconductor mixers for THz astronomy applications. To the best of our knowledge, this is the first implementation of an SIS based heterodyne receiver that dissipates microwatt level DC power. The promising results achieved in this work show the feasibility of implementing ultra low-power SIS based heterodyne receiver elements which could be deployed in the development of future kilo-pixel level arrays. We demonstrated that the power dissipation of cryogenic low noise amplifiers should not be a barrier in scaling up the number of elements in a large-scale cryogenic sensing system.

## 10.2 Suggestions of Future Research

Large-scale THz heterodyne receivers are desired for the wide-ranging astronomical surveys which could provide information about the fundamentals of the universe. In this dissertation, we addressed some of the issues associated with the scaling of heterodyne receivers one of which is the DC power consumption of cryogenic LNAs.

However, there exists many other challenges on the way of the implementation of kilo-pixel arrays which need to be solved to make that practical.

Scaling up the number of array elements require thousands of amplifiers to be biased simultaneously. To have a practical array, a robust biasing circuitry needs to be implemented for the low noise amplifiers so that all the LNAs could be biased using a reasonable number of source meters. Such biasing circuits needs to be extremely low noise so as not to degrade the noise performance of the amplifier. In addition, the power consumption of the biasing circuitry needs to be minimal in order to enable practical array scaling. Thus, the future work could be focused on the integration of a low-power low-noise servo biasing circuitry into the integrated LNAs for the future implementation of low-power SIS based arrays.

The sensitivity of a THz receiver is a function of the system noise temperature. As discussed in Chapter 1, the superconductor based mixers can achieve an extremely low noise temperature close to the quantum limit. Thus, the noise temperature of the low noise amplifier dominates the receiver noise. To implement systems with a higher sensitivity, low noise amplifiers with lower noise temperatures are desired while dissipating micro-watt level DC power. Future work could be focused on the development of ultra low-noise amplifiers with microwatt level DC power consumption.

Cryogenic circuits are desired to operate at high current densities in the high speed integrated circuits to achieve a higher unity gain cutoff frequency. In this dissertation, we looked at the sensitivity of the models to the device parameter extraction and found that the model accuracy is highly sensitive to the parasitic resistance extraction method as well as the transconductance of the device. Leveraging several different approaches for the extraction of the emitter resistance, we were able to obtain a model that predict the noise within 2K of the measurement results. All different techniques we used in this work assume that the emitter parasitic resistance is a bias independent parameter. However, we think that there could be a bias dependent

component associated with the emitter resistance at high current densities. Future work could be focused on the development of new extraction techniques for the emitter resistance at high current densities. In addition, we believe that the accuracy of the parameter extraction is only a part of the reason that noise models do not match very well at high current densities. There could be other factors contributing to the optimistic noise prediction of the models at high injection region which are not captured in the standard model. Further investigation is required to incorporate other physical mechanisms that appear at high currents into the standard model.

Finally, in the noise models presented in this dissertation, the correlation between the shot noise sources in a SiGe HBT is neglected. This assumption is valid at frequencies below 10 GHz, however, it could lose validity at higher frequencies. A detailed study of the correlation between the shot noise sources is required to enable development of noise models with good accuracy at frequencies above 10 GHz.

## APPENDIX

### EXTRACTION OF CABLE RESISTANCES

In order to accurately extract the emitter and collector resistances through a DC measurement technique, such as the open-collector or the Gummel-curve method, the DC resistance of the cables should be determined first. To do so, the input and output probes should be landed on a Short structure and the Z-parameter of the two port network should be calculated through a DC measurement. Fig.A.1 shows an example diagram of the measurement setup in which the Z matrix can be calculated as

$$Z_{11} = Z_1 + Z_2 + Z_5, \quad (\text{A.1})$$

$$Z_{12} = Z_5, \quad (\text{A.2})$$

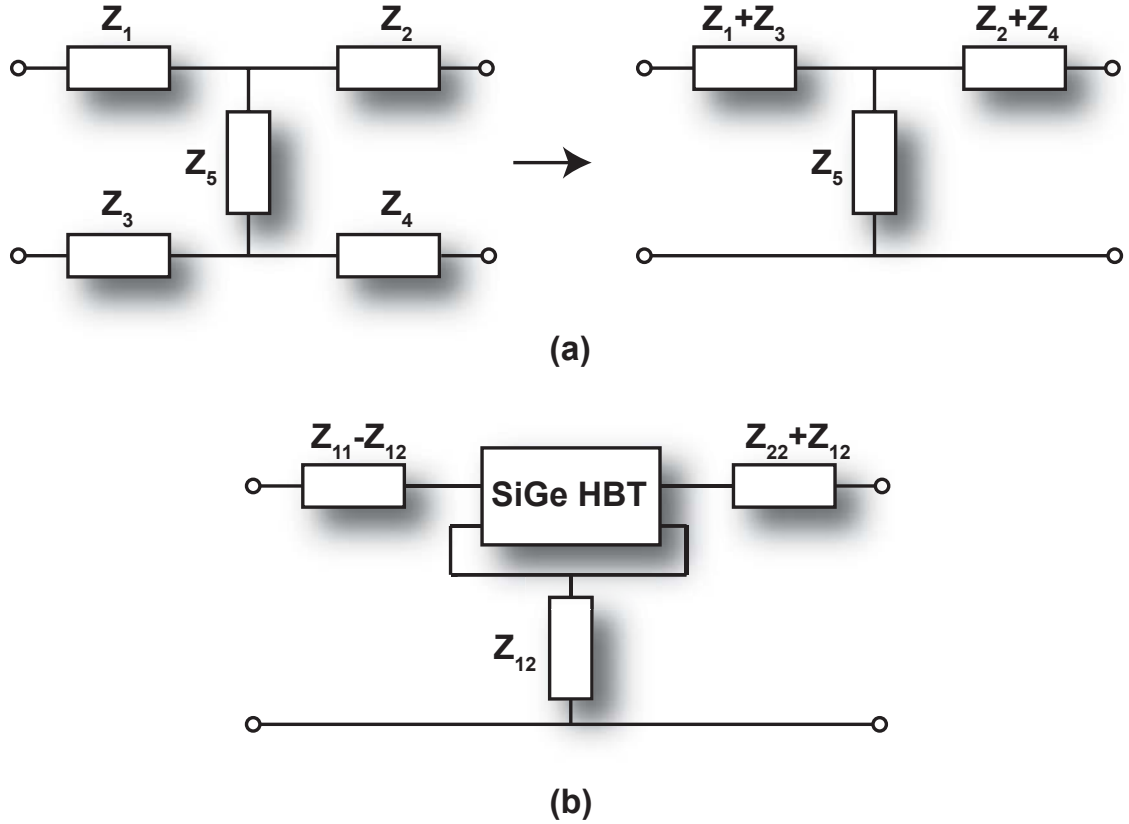
$$Z_{21} = Z_5, \quad (\text{A.3})$$

$$Z_{22} = Z_2 + Z_4 + Z_5. \quad (\text{A.4})$$

The value of the Z-parameters can be calculated through a DC measurement using the equations below.

$$Z_{11} = \left. \frac{dV_1}{dI_1} \right|_{I_2=0}, \quad (\text{A.5})$$

$$Z_{12} = \left. \frac{dV_1}{dI_2} \right|_{I_1=0}, \quad (\text{A.6})$$



**Figure A.1.** (a) An equivalent two port network for deembedding the cable resistance. (b) An equivalent two port network for deembedding the cable resistance.

$$Z_{21} = \left. \frac{dV_2}{dI_1} \right|_{I_2=0}, \quad (\text{A.7})$$

$$Z_{22} = \left. \frac{dV_2}{dI_2} \right|_{I_1=0}. \quad (\text{A.8})$$

Once the  $Z$  network of a short structure is calculated, the shunt and series resistance of the cable should be subtracted from the emitter, collector, and the base resistance extraction as shown in Fig.A.1.(b).

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