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Distributed Element Designs for a Wireless System

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Distributed Element Designs for a Wireless System

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Abstract

A prototype binary frequency shift keying (BFSK) RF link operating in the 2.4 GHz ISM band was identified as a need for a potential undergraduate engineering laboratory activity. This system would be used to showcase various RF circuit engineering principles and techniques such as controlled trace impedances, frequency mixing, voltage-controlled oscillators, distributed element filters, and power splitters. This investigation focused on designing a prototype system that put a priority on ease of measurement and circuit tuning to help foster a more hands on approach. Each major circuit element was broken into separate PCBs to increase the modularity of the design and allow for each of them to be measured independently of the system. All schematic capture and layout was performed in Altium Designer. The RF system was able to transmit up to 60 cm with an input power of 0 dBm without any dedicated amplification. The use of a distributed element 2.4 GHz bandpass filter was used as an opportunity to investigate the impact on filter performance that different substrates and filter subtypes had on the overall filter design. Four substrates of various thickness, 50 to 62 mils, and dielectric constants, ε_r = 3.55 to 10.2, were used for stepped impedance, edge-coupled, hairpin, and elliptic filters. All 16 of the filters were designed using Genesys 2015, laid out using Altium 2015, and routed on a LPKF ProtoMat S103 circuit board router. It was found that the stepped impedance and elliptic filters required traces less than 2 mils wide which are not easily manufacturable. Only the edge-coupled and hairpin designs were built. Out of these eight designs, the substrates with the lower dielectric constants performed the closest to their simulated results. However, this could have been due to unanticipated challenges when routing the higher dielectric materials that was not present for the lower dielectrics.

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Chapter 1: Problem Description and Filter/RF Link Overviews

1.1 Introduction

The advent of the Internet of Things (IoT) has brought a widespread adoption and integration of devices that utilize different wireless communication technologies such as Wi-Fi, Bluetooth, RFID, and near-field communications. This has created a new set of challenges for engineers when designing efficient products with shrinking footprints. This increased demand for higher performing wireless devices has driven up data rates causing an upward shift in their frequency of operation. The radio frequency (RF) circuits implemented in these devices must be tightly designed and fully understood by engineers to help reduce time between design iterations and testing. However, the challenges of high frequency designs can be difficult to convey without hands on measurements and experience. To help demonstrate different RF engineering principles, a 2.4 GHz Binary Frequency Shift Keying (BFSK) system with distributed element filters was developed and proven as a potential lab for junior and senior level electrical engineering students at Grand Valley State University (GVSU).

This link consisted of a transmit circuit operating in the 2.4 GHz ISM, a receiver circuit, and a detector that differentiates between the presence of a “low” or “high” channel. The RF link was implemented with a modular design and multiple tunable values. System elements such as the transmitter, receiver, filtering, splitter, and detector are all contained on separate Printed Circuit Boards (PCBs). This allows the response of each circuit to be measured and demonstrate how it contributes to the functionality of the system. For the distributed element filter, multiple substrates and topologies were compared to better demonstrate what impact those choices have on the design and performance.

1.2 RF Link Overview

While there are many ways to implement an RF circuit, most of them can be simplified down to a block diagram similar to what is shown in Figure 1-1.

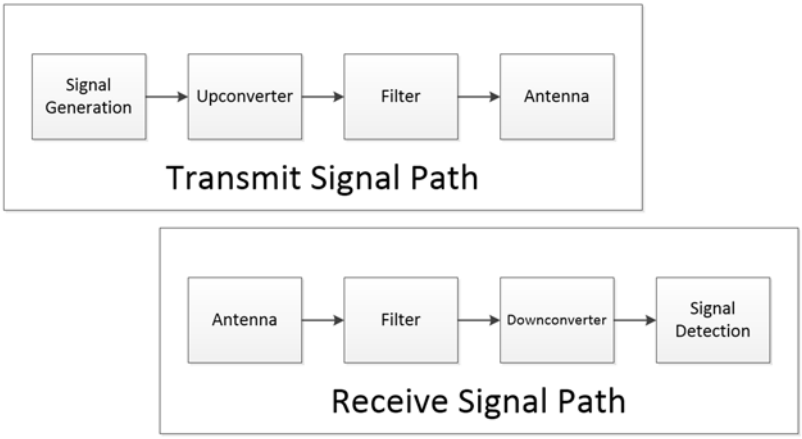


Figure 1-1 - Simplified RF Link Block Diagram

Since this investigation focuses on a BFSK system, the signal detection can be broken down even further as shown in Figure 1-2.

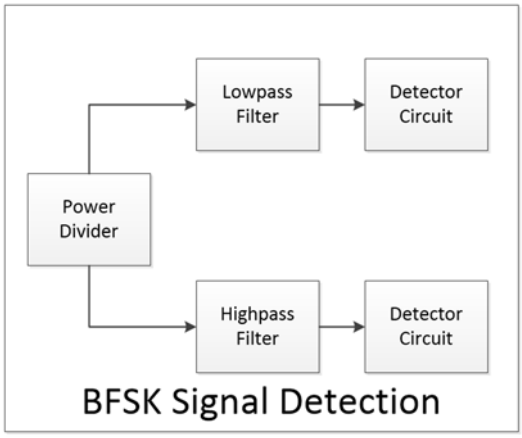


Figure 1-2 - BFSK Detection Simplification

In this thesis, each block shall consist of a separate PCBs to allow the students to evaluate the individual contribution of that block with respects to the overall system. The system uses a

BFSK signal with a digital 0 represented by an 60 MHz frequency and a digital 1 represented by an 80 MHz frequency. A complex bit pattern would have been excessive as the focus of the investigation was the RF circuit and not the modulation of the signal. These two signals are synthesized as an 200 and 180 MHz intermediate frequency (IF) as shown in Figure 1-1 in the signal generation block, and are mixed with a 2600 MHz local oscillator (LO) in the upconverter block in order to bring the transmitted signal into the 2.4 GHz ISM band.

A frequency mixer is required to achieve the different IF and RF frequencies present in the design. A mixer generates a signal that is mathematical sum and difference the IF and LO frequencies [1]. This is shown in equation (1) below.

$$f_{RF} = f_{LO} \pm f_{IF} \tag{1}$$

Where the sum is considered to be the upper sideband (USB) and the difference is the lower sideband (LSB) [2]. Due to the simple BSFK modulation used in the RF system there was no strong need to control the sidebands or to design around them as only one frequency, 60 or 80 MHz would be present at a time.

The filtering of the transmit and receive signals was done using a 5th order 300 MHz wide distributed element bandpass filters centered around 2.45 GHz. These filters are used to help stop the transmission of unwanted noise generated as byproducts from the frequency mixing steps as well as to remove any noise from external sources such as Wi-Fi or Bluetooth devices.

The receiver circuit used a 2.34 GHz LO signal to mix back down to the desired 60 and 80 MHz baseband frequencies. A resistive power divider was used to split the signal into the separate 60 MHz and 80 MHz detector circuits. A simple LED indicator in the detector circuit will be used to verify the presence of either the high or low bit. A successful transmission of

either frequency will result in the LED turning on. Due to the BFSK modulation, only one LED is active at a time. The more complex and tunable circuits, such as the transmitter and receiver, uses potentiometers to help illustrate their operation. This will take the form of a multi-turn potentiometer that will be used to control the input voltage to the VCO and manually adjust the frequency output. A trimmer resistor is also used in the detector circuits to set the trigger voltage level for when the LED indicator turns on.

1.3 Distributed Element vs. Lumped Element Filters Methods

When designing IF filters for a wireless system, lumped element filters are commonly used. At these lower frequencies components behave closer to their ideal characteristics and parasitic effects aren't as dominate, or not even present at all. However, when filtering the frontend of a wireless system at RF and microwave frequencies, distributed element filters start to become a more practical choice. At higher frequencies, the phase shift through traces and components require distributive analysis as the lumped element models start to break down. Generally, this transition from lumped to distributed element task place when frequencies rise above the VHF band of 30-300 MHz, or wavelengths of 1m or less in freespace. For the RF system described in this thesis, distributed element filters will be used to filter the transmit and receive signals in the 2.4 GHz ISM band, see Figure 1-1, while lumped element filters will be used to discriminate between the 60 MHz and 80 MHz frequencies before the detectors, see Figure 1-2.

Distributed element filters have a set of drawbacks and pitfalls. Tolerancing in the dielectric and fabrication of the filter elements can lead to poor and unwanted filter performance. Variations in dielectric constants for a given substrate can cause large shifts in the characteristic impedances of a trace and fundamentally change the frequencies a filter operates at. Designs

with very small physical spacing or filter elements are more sensitive to changes in the filter's layout as this has a greater effect on the element's characteristic impedance [3]. Another less obvious pitfall to distributed element filters is that not all filter topologies are suitable for every filter type. Bandpass filters tend to favor designs with strong coupling between filter elements as seen in parallel-coupled line topologies [4]. Similarly, a true high-pass filter can be difficult to implement. At some point the frequency content of an applied signal will be outside the operational range of the high-pass filter, and its elements will no longer be resonant, and an unfavorable frequency response will be present. To compensate for this, a broad-band bandpass filter is used instead with a bandwidth that is well above any frequencies of interest [4].

One large difference between distributed element filters and lumped element filters is how he PCB substrate affects the filter performance. For distributed element filters the PCB substrate and layer stackup needs to be considered as an additional design parameter of the filter. Understanding the impact of this choice is critical for rapid prototyping and efficient use of PCB space. For this investigation, four different bandpass distributed element filter topologies on four different PCB substrates of different thicknesses and dielectric constants were explored. Keysight Genesys was used to simulate the designs as well as optimize them against the same criteria. Controlling against a specified filter performance across all 16 designs simplified observations for determining the impact on the physical realization and measured performance.

1.4 Objectives

The main objective of this investigation was to develop hardware that could potentially be used in an undergraduate electrical engineering lab activity and to investigate the effects that PCB substrate have on distributed element filter performance. The complete objectives of this investigation were:

- Produce a working BFSK RF Link
- Contrast various filtering techniques such as hairpin, coupled lines, or stepped-impedance designs.
- Contrast various substrate materials to help improve designs

These objectives are shown to be accomplished throughout different sections of this investigation. Research involving different distributed element designs applicable to the RF system and the filters are presented in Chapter 2: Research. The design choices highlighted in the research portion are used to design, implemented, simulated, fabricated, and measured the distributed element filters are shown in Chapter 3: Distributed Element Filter Circuits. A detailed description of the RF system architecture and their measurements are highlighted in Chapter 4: Additional RF Circuits and Systems.

Chapter 2: Research

2.1 RF Circuit Research

Two distributed element circuit designs that have potential use in the RF system are a Wilkinson power divider and an 180° ring hybrid junctions. However, before either of these designs can be implimented they needed to be fully explored to make sure that they would be correct choices for the RF link and fit within the scope of the investigation.

A power divider is needed as part of the BFSK modulation scheme, as shown in Figure 1-2. A Wilkinson power divider was considered due to their low insertion loss and high output isolation. Their construction requires two quarter wave-length segments with a trace impedance of $\sqrt{2}Z_0$ as well as a parallel $2Z_0$ resistor between the output ports, where Z_0 is the desired characteristic impedance [1]. At the RF frequencies of 2.4 GHz, those quarter wave-length traces would be approximately 17.5 mm on FR-4. However, since this circuit would be used with an IF frequency of 60 and 80 MHz, a trace length of roughly 500mm would be needed. Due to the excessive required length, a distributed Wilkinson power divider was found to be highly impractical. Instead, a simpler, but lossy, three-port resistive divider was deemed the better option and the total 6 dB nominal loss would have to be incorporated into the system and accounted for [2]. A lumped-element Wilkinson splitter was not fully explored for its lack of distributed elements.

Frequency mixing is also required as it is the core element of the upconverter and downconverter, see Figure 1-1. To implement the downconverter as a distributed element circuit for the receiver, a ring hybrid junction was investigated. The generalized layout required for the circuit is shown in Figure 2-1.

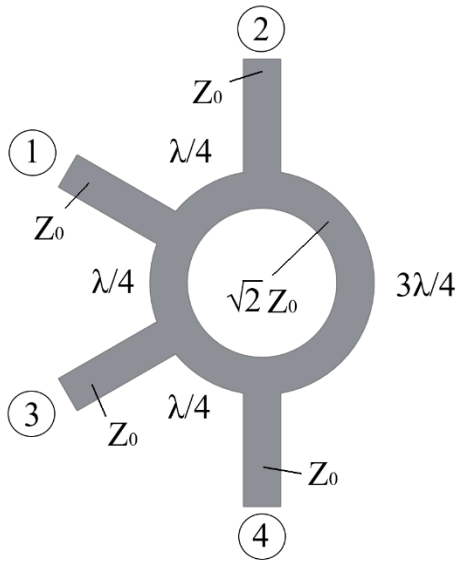


Figure 2-1 - 180° Ring Hybrid Junction

The 180° ring hybrid junction, or rat-race, is a four-port network that utilizes phase shifts to isolate, split, or combine inputs [1]. The trace length between ports 2 and 1, 1 and 3, and 3 and 4 are each λ/4 while the separation between ports 2 and 4 is 3λ/4. For use as a mixer, the RF and LO signals are applied at ports 2 and 3 with the USB appearing at port 1 and LSB at port 4 [2]. The potential frequency range of this circuit if implemented for the receiver would be roughly 2200 MHz to 2600 MHz based on the voltage-controlled oscillator's (VCO) tunable frequency range. The selection process and characteristics of the VCO are discussed further in section 4.3. This frequency range would give a bandwidth 400 MHz, or 16.7%. This is under the 20% standard guidance for the maximum bandwidth of a practical ring hybrid junction design [1]. However, due to the uncontrolled and possibly nonuniform dielectric material that could be used it was determined that using a ring hybrid junction design could take multiple revisions before it worked as designed through the required frequency range. The priority of the investigation was to focus on creating a working prototype RF system. However, this leaves the

use of a ring hybrid junction as an area of potential future work, as it could be used to expand the teaching potential of the design.

2.2 Importance of PCB Selection

For the distributed element filters used to filter the transmit and receive signals as shown in Figure 1-1, a deliberate and well-informed decision had to be made on which PCB substrate to select. While there are plenty of tunable parameters for distributed element filters, one aspect that affects all portions of the design is the PCB substrate. The thickness of the substrate and its dielectric constant impacts everything from the realized size of the filter all the way through to its frequency response. The dielectric constant and thickness of the substrate are approximately static values throughout a design and directly used when calculating the characteristic impedances of a trace. To better understand how the parameters of a substrate affect distributed element filter performance, the equations used to find the characteristic impedance of a microstrip was investigated. Since the characteristic impedance of the individual filter elements are tuned to correspond to the equivalent discrete element counterparts a parallel can be formed to microstrips [2]. While the comparison between distributed filter elements and microstrip impedances is not meant to be a mathematical equivalency, it can be used to help estimate what impact a substrate will have on a distributed element filter.

To calculate the characteristic impedance of a microstrip trace, the effective dielectric constant of the PCB substrate material needs to be found first. The effective dielectric constant of a microstrip line, ϵ_e, is shown in equation 2 [2].

$$\epsilon_e = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \frac{1}{\sqrt{1 + 12\,d/w}} \tag{2}$$

Where ϵ_r is the relative dielectric constant of the substrate material, d is its highth or the distance between the microstrip and its reference plane, and w is the width of the trace. The effective dielectric constant can then be used to find the characteristic impedance of the microstrip. However, in order to derive a closed form expression an assumption of width to height must be made, resulting in two equations as shown equation 3 [2].

$$Z_0 = \begin{cases} \frac{60}{\sqrt{\epsilon_e}} \ln\left(\frac{8d}{W} + \frac{W}{4d}\right) & \text{for } W/d \leq 1 \\ \frac{120\pi}{\sqrt{\epsilon_e}[W/d + 1.393 + 0.667 \ln(W/d + 1.444)]} & \text{for } W/d \geq 1 \end{cases} \tag{3}$$

The first equation is used for narrow traces while the second equation is used for wide traces. Both equations 2 and 3 assume infinite structures for traces, reference plane, and a homogeneous dielectric.

Based on equations 2 and 3, there are no other factors contributing to a microstrip's characteristic impedance outside of dielectric constant, trace width, and separation from the reference plane. Once a PCB substrate has been selected only trace width and separation from the reference plane are left, and for most purposes separation from the reference plane will only have one or a limited number of choices.

While equations 2 and 3 can't be used to represent the characteristic impedance of a distributed element filter with 100% accuracy, since it ignores parasitics and doesn't account for their complex topologies, it does give some insight into what factors contribute to the performance of the filter and how substrates with different dielectric constants and thickness would require different designs to achieve the same response. What equation 2 and equation 3

do show is that substrates with lower dielectric constants would need to be thinner than substrates with higher dielectric constants in order to implement distributed element filters with the same width traces. A more practical implementation of this idea would be that PCBs of the same thickness would require wider traces for low dielectric substrates and thinner tracers on high dielectric substrates.

2.3 PCB Material Selection

The four different substrates used in this thesis are shown in Table 2-1. The Rogers substrates were selected due to their uniform ε_r, high quality, and popularity throughout their industry. This is especially true with their RO4003 substrates.

Manufacturer	**Material Name**	**Dielectric Constant**	**Dielectric Tolerance**	**Dielectric Thickness**
Taconic	RF-60A	6.15	+/- 0.25	60 mil
Taconic	CER-10	10	+/- 0.50	62 mil
Rogers	6010.2LM	10.2	+/- 0.25	50 mil
Rogers	RO4003C	3.55	+/- 0.05	60 mil

Table 2-1 - PCB Substrate Parameters

The CER-10 and 6010.2LM substrates are used to illustrate the differences in substrate thickness while keeping a relatively similar dielectric constant. The RF-60A and RO4003C substrates are designed specifically for controlled impedance designs such as filters and high frequency applications [5] [6]. These two substrates are contrasted to determine how low of a dielectric constant is really needed for accurate impedance-controlled designs. These four substrates give a good mix of dielectric constant and thickness for comparison purposes.

In order to compare different materials successfully, a constant filter response was needed across all materials. For this a 5^{th} order 50 Ω bandpass filter centered around 2.45 GHz with a bandwidth of 300 MHz, a Q of 8.16, and passband ripple 0.1 dB was used. These values

were chosen to decrease measurement error and allow it to be used as the transmit and receive filters for the RF link. The low ripple aids in accurately measuring the 3 dB point and corner frequencies by providing a flatter response in the passband. The large bandwidth allows for variations in corner frequencies to not have a large overall effect on the performance of the filter and still operate in the indented 2.4 GHz ISM band. Taking into consideration the choices made in sections 3.1 and 2.3, four different substrates and four different distributed element filter subtypes were used for a total of 16 different filters.

To highlight the effect that the dielectric constant and substrate thickness has, each of the PCB substrates parameters were used to find the ideal trace width required to implement a 50 Ω trace using equations 2 and 3. This is shown in Table 2-2. RF-60A and RO4003C used the wide trace equation and CER-10 and 6010.2LM used the narrow trace equation.

Substrate and Dielectric Constant	**RF-60A** ε_r **= 6.15** **60 mils thick**	**CER-10** ε_r **= 10** **62 mils thick**	**6010.2LM** ε_r **= 10.2** **50 mils thick**	**RO4003C** ε_r **= 3.55** **60 mils thick**
50 Ω Trace Width	88 mils	59 mils	46 mils	140 mils

Table 2-2 - Substrate 50 Ω Trace Widths

2.4 Genesys Investigation

Keysight Genesys, a RF and microwave synthesis and simulation software package, was heavily used in the creation and optimization of each of the filters present in this investigation. The decision to use Genesys was initially due to its availability as a piece of software currently licensed to GVSU and would not require any expensive software licenses. As the software package was explored further it showed several beneficial features such as filter optimization, component transformations, layout and schematic support, and EM simulations. More information pertaining to Genesys and a full list of its features can be found on Keysight's website [7]. A working knowledge of Genesys was first put together by evaluating the different

filter tools and tutorials included out of the box. These tutorials were found on the Genesys YouTube channel [8]. There are three standard filter synthesis tools present in Genesys: Passive Filter, Microwave Filter, and S/Filter.

For lumped element LC filters the Passive Filter synthesis is ideal as it is geared around using different filter subtypes. There isn't an optimization tool integrated into the Passive Filter tool but instead it has an order estimation calculator [9]. A frequency and desired attenuation can be entered in, and based on the filter settings, a recommended filter order is given to help meet those attenuation requirements.

The Microwave Filter synthesis tool was found to be the best option in Genesys for designing distributed element filters. Unlike Passive Filter, Microwave Filter takes into account the manufacturing process and substrate properties and then uses that information to calculate a more accurate frequency response [10]. Microwave Filter was used as the main synthesis tool for all the distributed element filters designed during this investigation. S/Filter was not explored as its features were more advanced and outside of the scope of this project.

Once the optimized filter response is found, further analysis should be done to account for full wave (EM) effects. This is ran in Genesys by using Keysight's Momentum EM solver to perform an FE mesh analysis. While Momentum provides a significantly more accurate model by considering the substrate, layout, and signal coupling, it can take longer to complete. While this would be considered a very quick calculation to run, it can drastically increase optimization time when the Momentum results are used as the goal parameters as the Momentum solver is ran in between each optimization step. It was discovered that this long simulation time could be circumvented by finding the offset between the standard simulation and Momentum results and applying it as a frequency offset to the filter design. For example, if the Momentum results

showed an overall downward shift of 60 MHz from the center frequency, the bandpass filter would be reentered as 2240 to 2540 MHz from the original values of 2300 to 2600 MHz. This would dramatically reduce simulation time by manually compensating for the transition between the standard simulation and the mesh analysis via Momentum. From here the Momentum results would be used as the optimization parameters and total run time was cut from roughly 5 hours down to 30 minutes.

Chapter 3: Distributed Element Filter Circuits

3.1 Filter Topology Choices

A wide range of distributed element filter subtypes with different topologies exist and consist of innovative combinations of open-circuited and short-circuited stubs to achieve their desired filter responses. During this investigation four different subtypes were investigated to determine their strengths and draw backs. These subtypes were stepped impedance, edge-coupled, hairpin, and elliptic. While these filter subtypes might be numerically equivalent, it is important to understand the realized performance once fabricated.

A stepped impedance design use sections of alternating high and low characteristic impedance elements [2]. This makes them easier to visualize when compared to their lumped element counterpart as there are very few transformations that take place. Inductance is added with thin traces, and capacitance is added by the significantly thicker traces, see Figure 3-1.

Figure 3-1 - Stepped Impedance Distributed Element Filter Topology Example

Both edge-coupled and hairpin subtypes are variants of parallel-coupled line filters [4]. Parallel-coupled line filters in their simplest form are constructed from roughly half-wavelength transmission lines that overlap with each other for a quarter-wavelength per element, see Figure 3-2 [11]. The hairpin expands on this by folding each element back onto itself to create a “U” shape that reduces the overall footprint of the filter, see Figure 3-3.

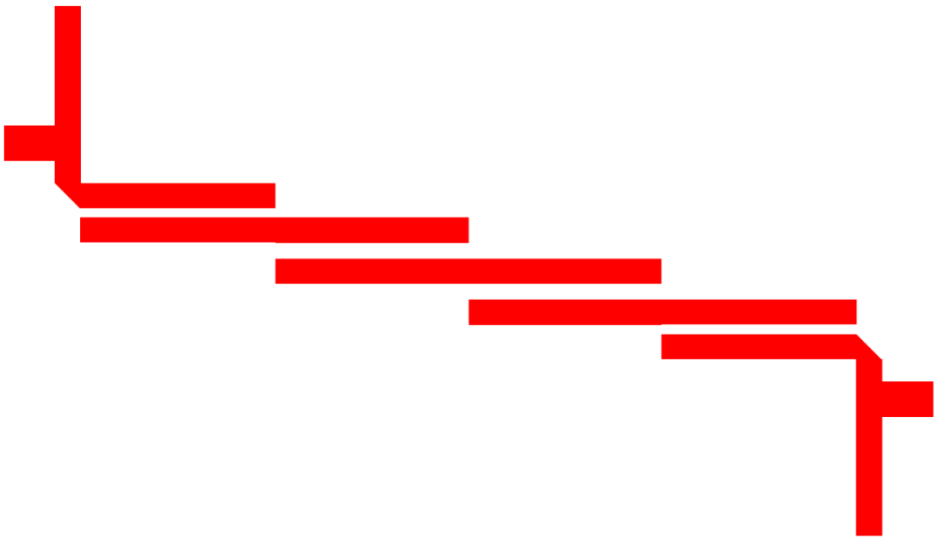


Figure 3-2 – Edge-coupled Distributed Element Filter Topology Example

Figure 3-3 - Hairpin Distributed Element Filter Topology Example

The distributed element elliptic filter uses filter elements present in both the stepped impedance and parallel-coupled line filters to create an Cauer filter response. However, the sharper filter response requires significantly closer filter elements which can make fabricating the filter unrealistic [12] See Figure 3-4 for the small vertical traces that are present.

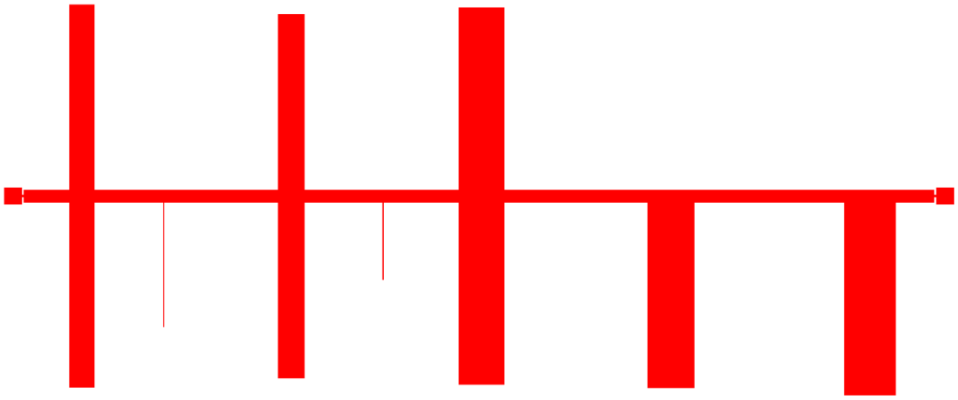
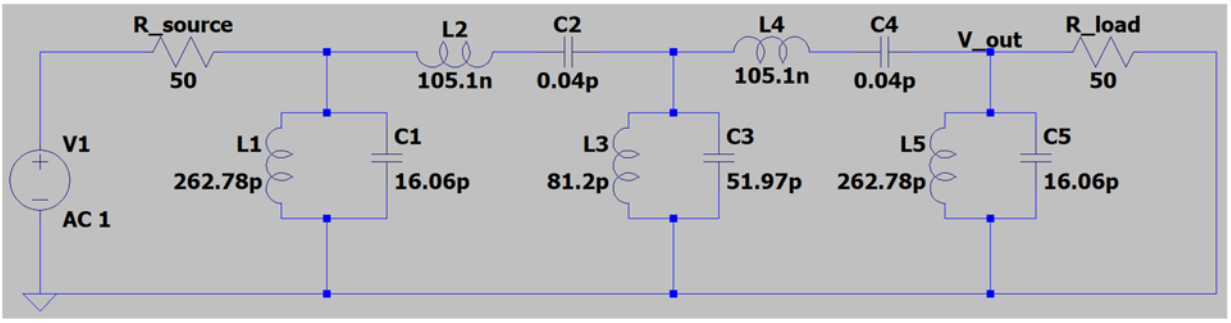


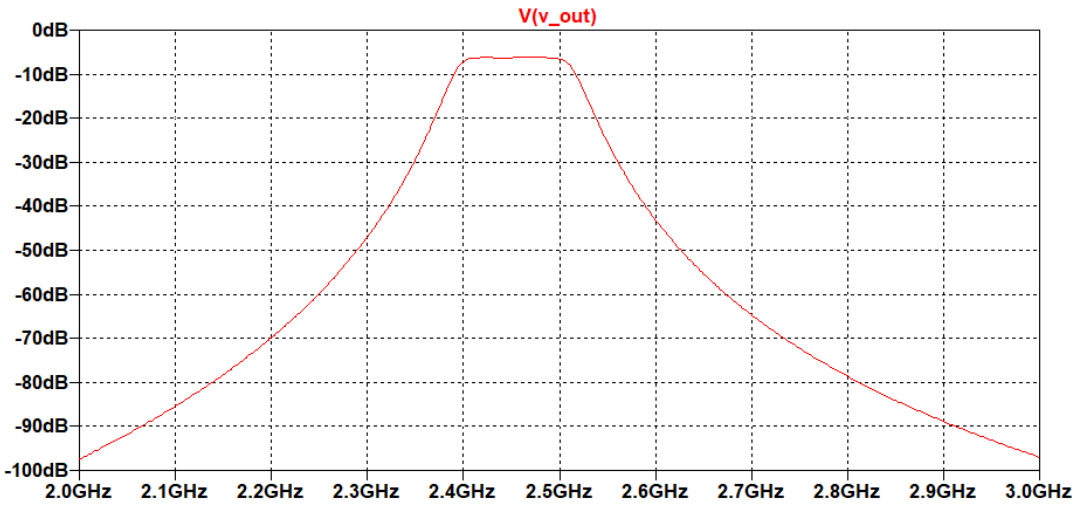
Figure 3-4 - Elliptic Distributed Element Filter Topology Example

3.2 Insertion Loss Investigation

The initial filter experiment's purpose was to compare lumped element and distributed element filters by designing a bandpass filter using the insertion method and then compare them to an equivalent distributed element filter. The maximally flat prototype values were used to synthesize a 50 Ω, 5th order, max flat, 100 MHz wide, 2.45 GHz bandpass filter [2]. The ideal simulated response and component values are shown Figure 3-5.



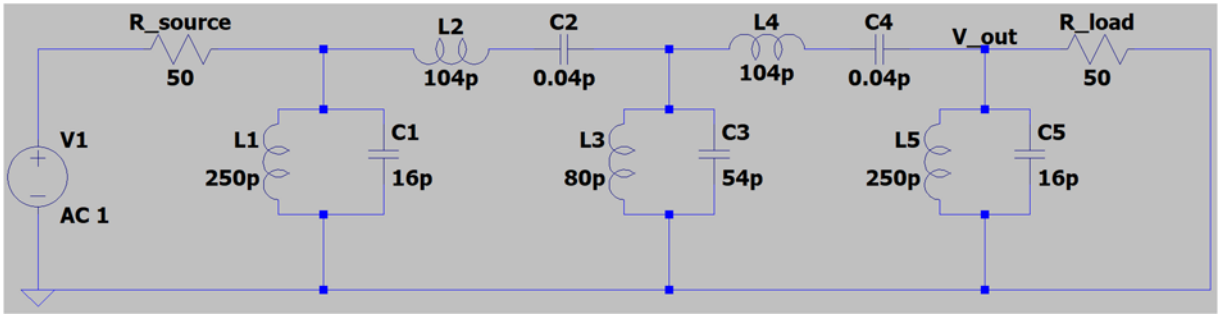
Ideal Values Found Using the Insertion Loss Method



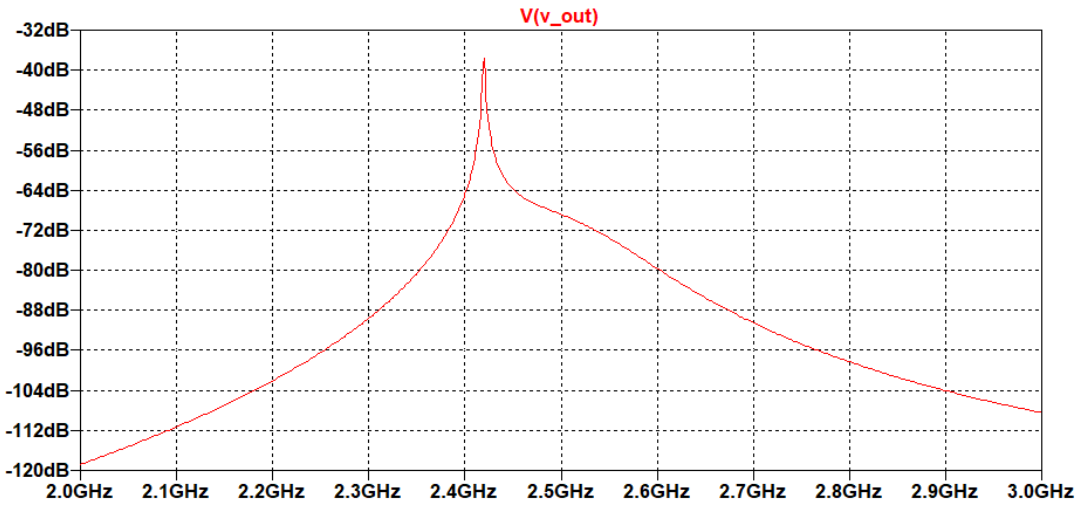
Ideal Simulated S_{21} Response

Figure 3-5 - Ideal Values Found using the Insertion Loss Method

However, when real and available component values were used to simulate the filter's response the S_{21} response was altered drastically. In addition, this simulation did not take into account parasitics, part tolerancing, or radiation/coupling effects which would have reduced its performance further. These response and component values are shown in Figure 3-6.



Nearest Component Values Found Using the Insertion Loss Method



Nearest Component Simulated S_{21} Response

Figure 3-6 - Nearest Component Values to the Insertion Loss Method

Based on the results as shown in Figure 3-5 and Figure 3-6, it was determined to not pursue the insertion loss experiments any further at this time as it was not within the original scope of the investigation and was not yielding a viable option. As such, no transforms to move from lumped element to distributed element designs were investigated either. This activity could potentially be used as a research project for an undergraduate engineering student or spread out over multiple labs. These values, while not very practical for a lumped element design, did serve as an exploratory effort into what might be a realistic specification for the distributed element filters used in the RF system.

For future investigations of fabricating equivalent lumped and distributed element filters, a few required changes have already become apparent. A lower quality filter with a greater bandwidth, would likely be more tolerant to smaller shifts in component values. This would help alleviate the problems caused by the differences between the calculated and actual component values. Shifting the center frequency down between 600 to 1000 MHz would make it easier to find useable components and would assist in limiting the contributions of parasitics and RF

effects. Such effects could cause complications with the distributed element filter as the geometry might be unrealizable at these frequencies.

3.3 Distributed Element Filter Simulation

Each of the four distributed element filter subtypes discussed above in section 3.1 were designed for each of the four substrate choices. Keysight Genesys 2015 was used to synthesize and optimize each filter. First, an accurate representation of each substrate's relevant physical properties needed to be imported into Genesys. These properties are shown below in Table 3-1. Each substrate was entered as part of a library to minimize the risk of a data entry error between the multiple variants. This information was taken from each substrate's data sheet.

Substrate	**Relative Permittivity (ε_r)**	**Relative Permeability (μ_r)**	**Loss Tangent**	**Resistivity (ρ)**	**Copper Thickness**	**Dielectric Thickness**
RF-60A	6.15	1	0.0023	1	1.42 mil	60 mil
CER-10	10	1	0.0035	1	1.42 mil	62 mil
6010.2LM	10.2	1	0.0023	1	1.42 mil	50 mil
RO4003C	3.55	1	0.0021	1	1.42 mil	60 mil

Table 3-1 - Genesys Substrate Properties Used

The settings present in Table 3-2 were used as the standard design criteria for the stepped, edge-coupled, hairpin, and elliptic distributed element filters.

Input/output Impedance (Ω)	**Passband Ripple (dB)**	**Attenuation at Cutoff (dB)**	**Order**	**Low Freq Cutoff (MHz)**	**High Freq Cutoff (MHz)**
50	0.1	3	5	2300	2600

Table 3-2 - Standard Genesys Filter Settings

All 16 filters were designed and optimized against the same criteria. Genesys' built in optimization tools were used to complete this task. The criteria used to optimize each filter is shown below in Table 3-3.

Measurement	Target	Frequency Start	Frequency End
S_{21}	-30 dB	2300 MHz	2600 MHz
S_{21}	-30 dB	2075 MHz	2187.5 MHz
S_{11}	-30 dB	2712.5 MHz	2825 MHz

Table 3-3 - Genesys Optimization Criteria

The simulated minimum insertion loss, lower corner frequency, upper corner frequency, and center frequency of each of the filters are shown below in Table 3-4. The CER-10 edge coupled filters simulated S_{21} and S_{11} parameters are shown below in Figure 3-7 as example typical and expected results. The complete set of S_{21} and S_{11} Simulations and layout for each filter and substrate is shown in Appendix A – Genesys Simulation Results.

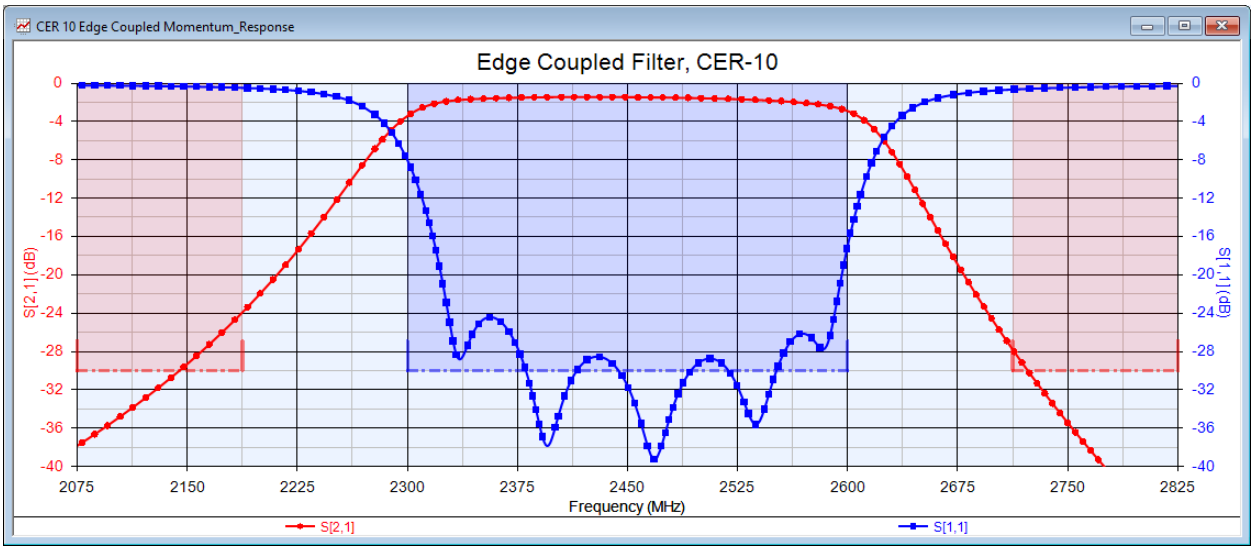


Figure 3-7 - Example Genesys S21 and S11 Filter Response

Substrate	Filter Subtype	Minimum Insertion Loss (dB)	Lower Corner Frequency (MHz)	Upper Corner Frequency (MHz)	Center Frequency (MHz)
RF-60A	Stepped	-2.59	2273.1	2596.7	2434.9
CER-10	Stepped	-5.17	2281.8	2597.7	2439.7
6010.2LM	Stepped	-5.70	2202.4	2636.9	2419.6
RO4003C	Stepped	-1.50	2271.8	2623.8	2447.8
RF-60A	Edge-coupled	-0.90	2263.3	2624.2	2443.8
CER-10	Edge-coupled	-1.44	2291.7	2616.3	2454.0
6010.2LM	Edge-coupled	-1.25	2274.0	2627.0	2450.5
RO4003C	Edge-coupled	-0.43	2283.0	2629.1	2456.0
RF-60A	Hairpin	-0.95	2270.8	2624.2	2447.5
CER-10	Hairpin	-1.39	2270.8	2616.1	2443.5
6010.2LM	Hairpin	-1.38	2281.3	2621.0	2451.1
RO4003C	Hairpin	-0.84	2294.3	2625.8	2460.0
RF-60A	Elliptic	-1.41	2322.9	2506.6	2414.7
CER-10	Elliptic	-9.53	2218.8	2385.4	2302.1
6010.2LM	Elliptic	-10.46	2213.5	2590.3	2401.9
RO4003C	Elliptic	-1.04	2284.7	2504.6	2394.7

Table 3-4 - Genesys Filter Simulation Overview

The simulation results were used to decide which designs would possibly yield comparable results when fabricated. To make this decision, two different factors were considered: (1) was the frequency response acceptable and (2), was the design manufacturable. The smallest trace width present in any portion of a filter layout is shown in Table 3-5.

Substrate	Filter Subtype	Smallest Trace Width (mil)
RF-60A	Stepped	7.6
CER-10	Stepped	2.6
6010.2LM	Stepped	1.5
RO4003C	Stepped	18.4
RF-60A	Edge-coupled	55.9
CER-10	Edge-coupled	35.5
6010.2LM	Edge-coupled	26.2
RO4003C	Edge-coupled	92.6
RF-60A	Hairpin	57.9
CER-10	Hairpin	35.7
6010.2LM	Hairpin	26.3
RO4003C	Hairpin	92.9
RF-60A	Elliptic	0.013
CER-10	Elliptic	0.021
6010.2LM	Elliptic	0.001
RO4003C	Elliptic	0.126

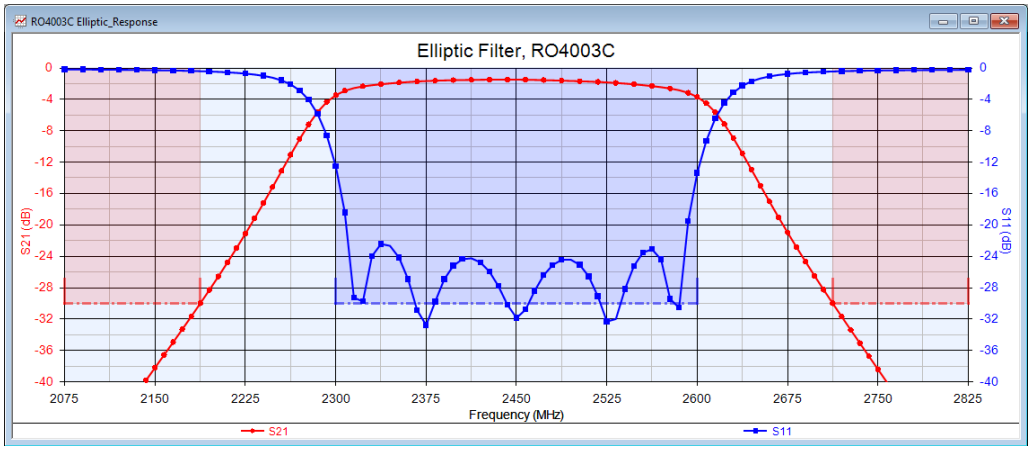
Table 3-5 – Genesys Filter Layout Smallest Dimension

Out of the four stepped filter designs, three had traces that were under 8 mils wide. Depending on where and who is fabricating a PCBs, 8 mils is generally where issues with manufacturability as well as price increases can start to play a role. However, the CER-10 and 6010.2LM substrates had traces at 2.6 and 1.5 mils respectively which would be too small for reliable fabrication. Even though all of the stepped filters had acceptable frequency responses, three of the four substrates could not be manufactured with any confidence and as such were not candidates to be built. Based on this information, a substrate with an ε_r of roughly 6 or less would have been a suitable option for a stepped impedance filter for this bandpass design.

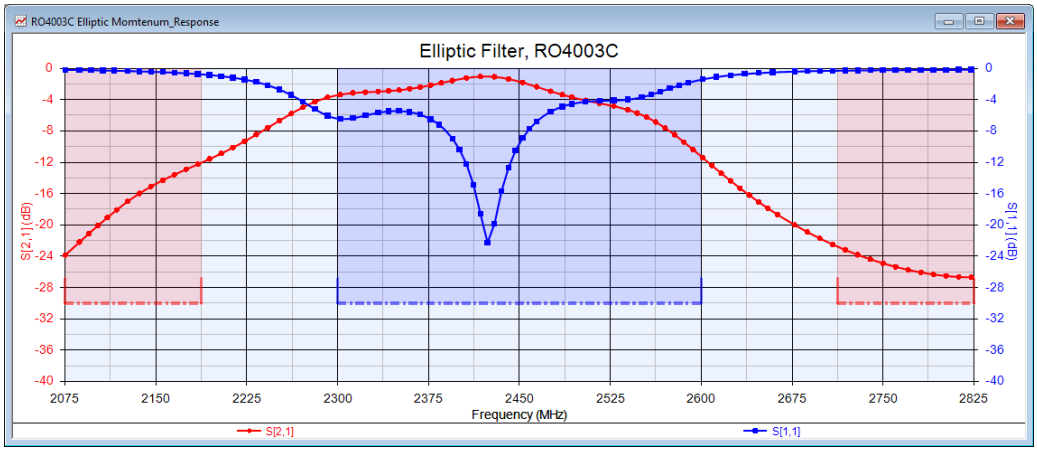
Similarly to the stepped filters, the elliptic filters had unreasonably small trace widths in their layouts that ranged from 0.001 to 0.126 mils. These values were completely unrealistic and indicate that this filter subtype is a less than ideal choice for this investigation. This is further reinforced by the fact that none of the optimization criteria could be met for the EM simulation.

Some of the stepped impedance and elliptic filters designs had insertion losses that ranged from -2.59 to -10.46 dB and were significantly higher than the edge-coupled and hairpin designs of -0.43 to -1.44 dB. These higher values were found on the higher dielectric substrates where there were some excessively small filter elements. Since these two filter designs were not going to get built the cause of the higher insertion loss was not investigated further, but it would make sense that these designs also had additional unwanted filter performance.

A comparison of the standard Genesys simulation and the Momentum simulation for the RO4003C substrate is shown below in Figure 3-8 to further illustrate this difference.



Standard Genesys Simulation Results



Momentum simulation Results

Figure 3-8 – RO4003C Elliptic Filter Simulation Comparison

At the basic level it appears that when metal edge-effects are taken into consideration a drastically different frequency response is found. However, the poor frequency response of the Momentum simulation could be caused by the unrealistically thin open circuit stubs. These elements may have been too small to have any significant contributions during the mesh analysis as the default layout mesh resolution of Genesys is 1 μm or 0.0394 mils. This is larger than the smallest trace width present in the RF-60A, CER-10, and 6010.2LM designs. To see what effect the mesh resolution had on the outcome, the Momentum simulations were reran with the mesh resolution reduced to 1 nm. No difference in the Momentum simulation results were observed for either of the RF-60A, CER-10, or 6010.2LM substrates, while the RO4003C results were slightly different, but not improved in any significant way.

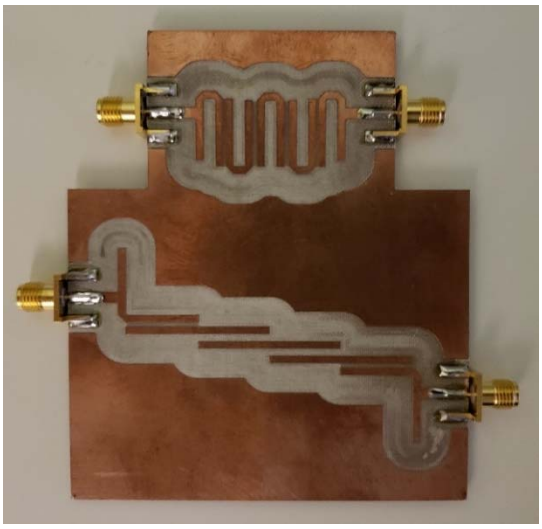
3.4 Distributed Element Filter Fabrication

Based on the results of Table 3-4 and Table 3-5, and the data shown in Appendix A – Genesys Simulation Results, PCBs were developed for all four substrates implementing the hairpin and edge-coupled designs. These filters were built with the intent to compare how close their measured results were to their simulated results. This was to verify the accuracy of the Genesys models.

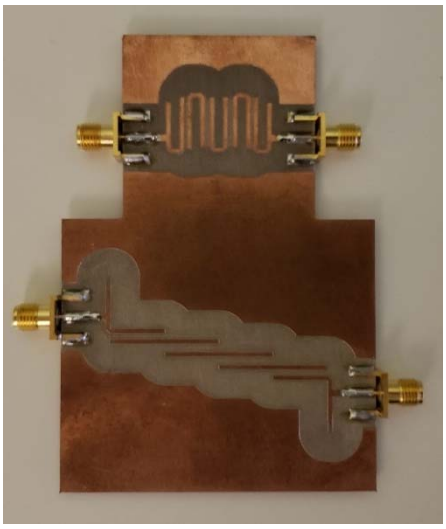
To start this process, each of the layouts generated in Genesys was exported as a DWG files and imported into Altium 2015 and turned into component footprints. Doing this preserved the geometry of each filter and prevented any accidental modifications to the copper. Both the hairpin and edge-coupled filters were implemented together on the same PCB and in such a way to minimize traces lengths between the filter and the SMA connectors.

A separation distance between the ground pour on the top layer and the filter elements and SMA connectors of three times the substrate thickness was incorporated into each of the

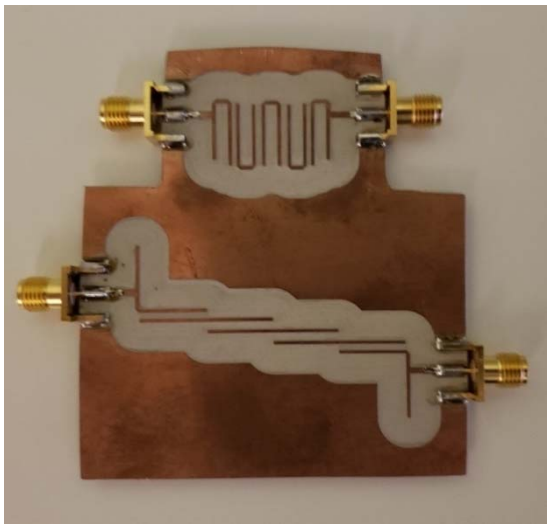
eight filter designs. This was added to help insure that the majority of the coupling was taking place between the top and bottom layers and not between the filter elements and the adjacent copper on the top layer. Photographs of the fabricated PCBs are shown below in Figure 3-9. All fabrication for the distributed element filters was performed using an LPKF ProtoMat S103 circuit board plotter.



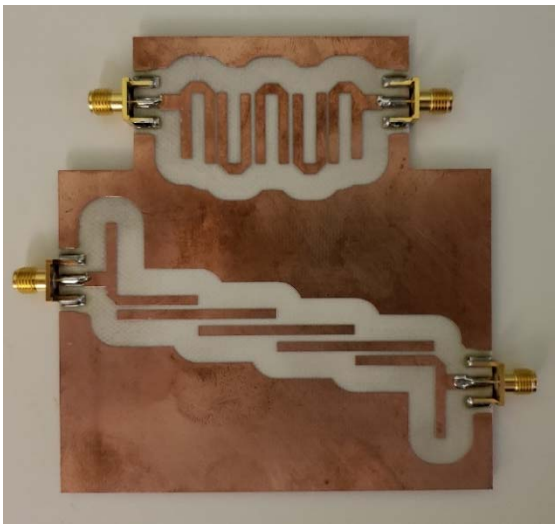
RF-60A Filters (3.186” by 3.750”)



CER-10 Filters (2.689” by 3.875”)



6010.2LM Filters (2.625” by 2.935”)



RO4003C Filters (3.938” by 4.125”)

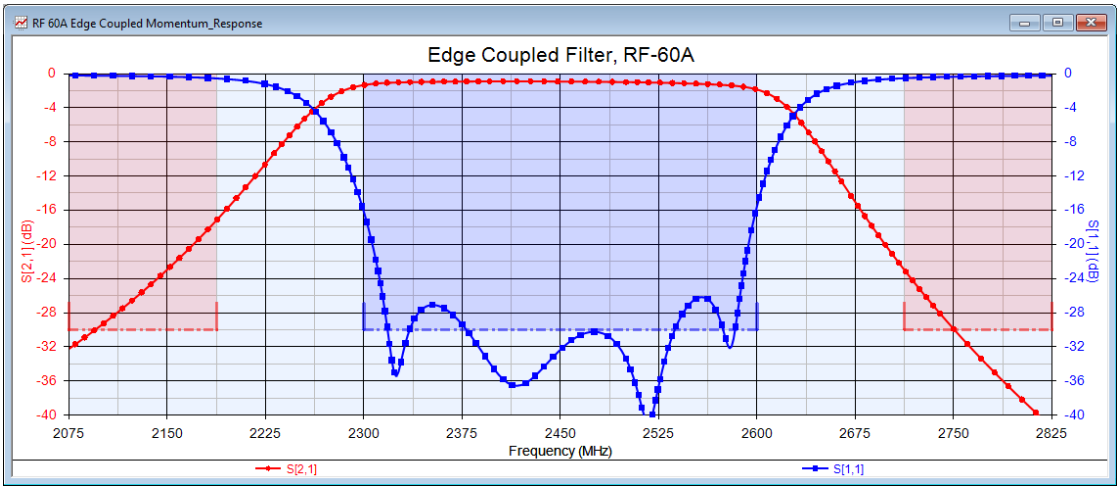
Figure 3-9 - Fabricated Distributed Element Filters

As expected, the largest sized filter corresponds to the widest 50 Ω traces as calculated in Table 2-2. Both the fabricated filters and 50 Ω traces had the RO4003C substrate as the largest. The traces and filters from largest to smallest were, RO4003C, RF-60A, CER-10, and 6010.2LM.

3.5 Distributed Element Filter Measurements

Once all four of the filter PCBs were fabricated and the edge mount SMA connectors were soldered on, they were measured using a Rohde & Schwarz ZNB 20 Vector Network Analyzer (VNA) with a Maury Microwave type N SOLT calibration kit and phase stable cables. The S_{21} and S_{11} parameters of each filter was measured from 1 MHz to 8 GHz, in 500 kHz steps, and at a level of -10 dBm. The data taken from the VNA was saved as a .csv file for easy post-processing with MATLAB. While this investigation primarily focused on the S_{21} response of each filter to simplify the overall scope and work balance, the S_{11} was recorded as well as it can be used to further compare the performance of each of the filters if required.

Each of the .csv files were imported in MATLAB to generate graphs and to automate finding each of the 3 dB corner frequencies. No manipulation of the data was done in MATLAB. Each filter was graphed similarly in format and scale to the Genesys simulation results to assist with comparisons. This data is shown in Appendix B – Fabricated Filter Measurements. For comparison, the simulated results and measured results of the RF-60A edge-coupled filter is shown in Figure 3-10.



RF-60A Edge-coupled Genesys Simulation

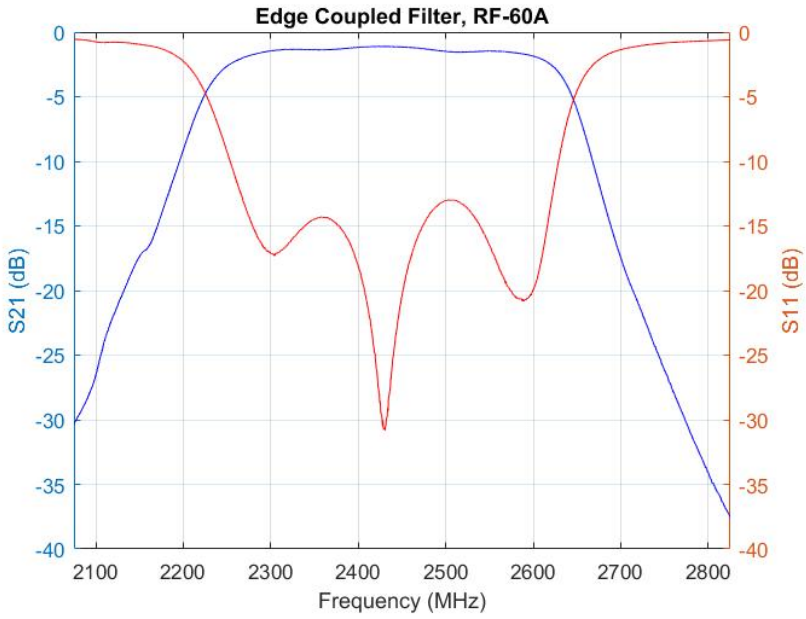


Figure 3-10 - RF-60A Edge-coupled Measurement

The minimum insertion loss of each filter was found by searching for the highest S_{21} value within the graphed window of 2075 to 2825 MHz. This window was selected as it contained the designed passband of 2300 to 2600 MHz and matched the Genesys simulation range. The lower and upper corner frequencies were found by finding the closest frequency in

each direction that was at least 3 dB lower than the insertion loss value. For example, using the RF-60A edge coupled filter data, the minimum loss in the passband was found to be -1.1073 dB at 2429.0 MHz. Based on that information a 3 dB point amplitude of -4.1073 dB was used to find the lower and upper corner frequencies. This yielded a lower corner frequency of 2230.0 MHz with a S_{21} magnitude of -4.1758 dB and an upper corner frequency of 2638.5 MHz with a S_{21} magnitude of -4.1380 dB. The insertion loss in the pass band, corner frequencies, and calculated center frequency for all eight filters is shown below in Table 3-6.

Substrate	Filter Subtype	Minimum Insertion Loss (dB)	Lower Corner Frequency (MHz)	Upper Corner Frequency (MHz)	Center Frequency (MHz)
RF-60A	Edge-coupled	-1.11	2230.0	2638.5	2434.3
CER-10	Edge-coupled	-1.45	2295.5	2618.5	2457.0
6010.2LM	Edge-coupled	-1.45	2348.0	2682.0	2515.0
RO4003C	Edge-coupled	-1.10	2265.5	2644.0	2454.8
RF-60A	Hairpin	-1.08	2286.5	2699.5	2493.0
CER-10	Hairpin	-3.59	2320.0	2759.0	2539.5
6010.2LM	Hairpin	-1.53	2387.5	2735.0	2561.3
RO4003C	Hairpin	-1.26	2293.0	2701.5	2497.3

Table 3-6 - Distributed Element Filter Measurements

3.6 Filter Measurement Observations

Each of the filters behaved similarly with a few exceptions. The CER-10 hairpin filter had a ~3 dB ripple in the passband as shown in Figure 3-11, while all other filters were almost completely flat.

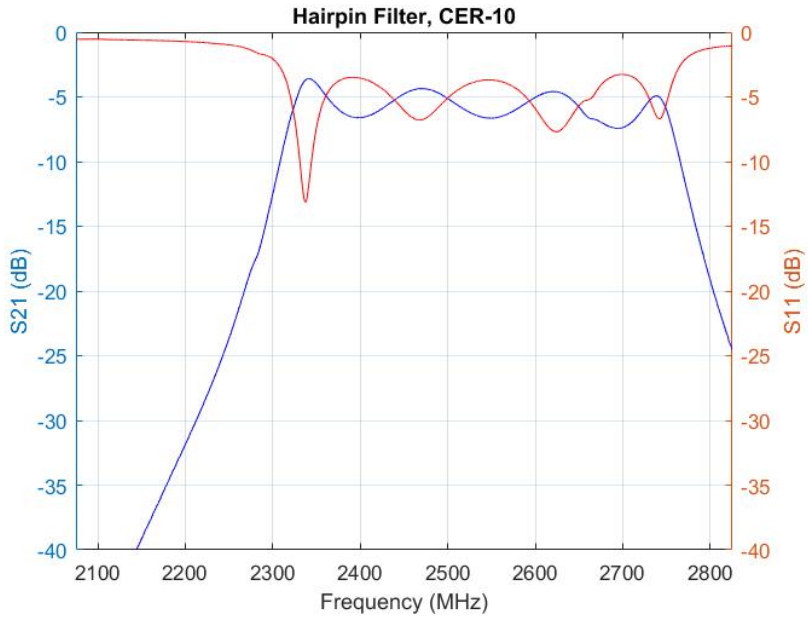


Figure 3-11 - CER-10 Hairpin Measurement

This ripple was still present after the VNA was recalibrated and the SMA connectors on the PCB were replaced. The ripple was deemed inherent to the filter itself and could have been caused by a manufacturing mistake, error in the Genesys model parameters, or a defect with the substrate itself.

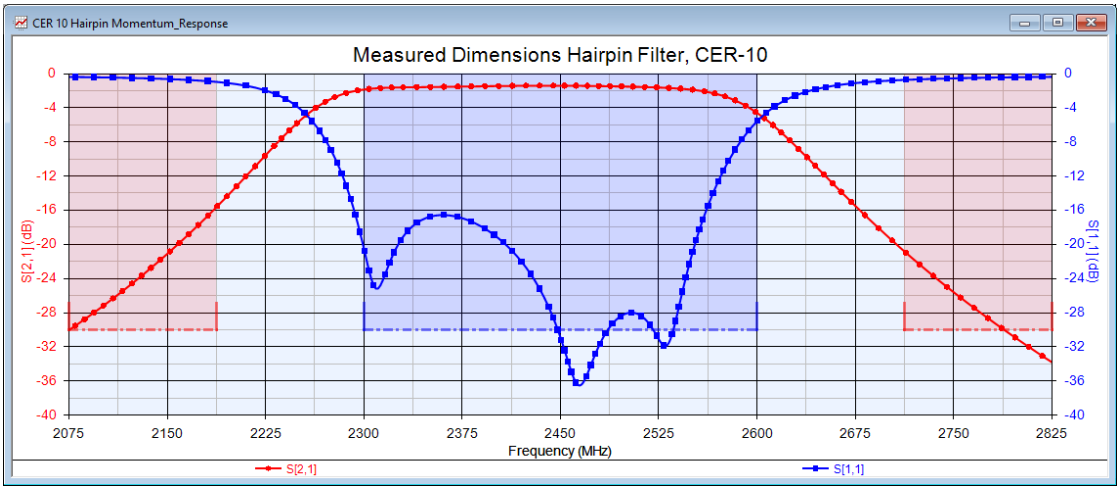


Figure 3-12 - CER-10 Hairpin Filter Simulation From Measured Dimensions

Another observed trend was that both of the 6010.2LM filters had the largest shift in center frequency when compared to the simulated results. The edge-coupled design shifted up in frequency by 64.5 MHz and the hairpin design shifted up by 110.2 MHz. This stood out as the other three edge-coupled filters only showed a shift in the center frequency by 1.3 to 9.5 MHz. This substrate proved to be challenging to mill out. During the milling process of the 6010.2LM PCB, the substrate proved to be very gummy and ended up being melted by the cutting tool instead of shaved away. This substrate is a ceramic-PTFE composite and was fabricated based on the guidelines provided by Rogers [13]. The hairpin filters overall had a much larger shift up in center frequency with a range of 37.2 MHz to 96.0 MHz, with the 6010.2LM hairpin filter excluded from this list.

Based on the simulation and measured data, a dielectric constant of 6 or less is recommended for distributed element filters as the RO4003C and RF-60A substrates had the least shift between the simulated and measured results overall. While the CER-10 and 6010.2LM substrates had the largest shift between the simulated and measured results, their frequency response was still mostly acceptable relative to the system they were designed for. Using a bandwidth of 300 MHz allowed for some of the shift between simulated and measured response to be tolerable. For tighter designs were minimal frequency shift between the simulated and measure results are needed, higher dielectric constant substrates should be avoided.

Chapter 4: Additional RF Circuits and Systems

4.1 System Overview and Requirements

The requirements of the RF circuits were intentionally left vague and open ended. This was to allow for the design to be flexible as the various circuits were built and measured. However, there were some basic requirements put forward to help guide the investigation. Those initial requirements are shown below.

- All power inputs shall have reverse voltage protections
- SMA connector types shall be used for input and output connectors
- All major circuit blocks shall be contained on their own PCB and are able to be operated fully independently of adjacent inputs or outputs
- No SPI, I^2C, or similar communications shall be used
- All components must be able to be soldered by hand

While these requirements did not provide much in terms of initial direction they were able to setup a defined work space and scope of the RF circuit investigation, with the main focus being to produce a working RF system that can be used as part of an engineering laboratory. Altium 2015 was used for all schematic capture and circuit layout. The schematic, layout, BOM, and cost of each of the RF system circuits are shown in Appendix C – Schematic, Layout, and BOM Detail. Pictures of the built circuits and of the measurement setups are shown in Appendix D – Constructed Circuits and Measurement Pictures. A block diagram of the complete system is shown in Figure 4-1.

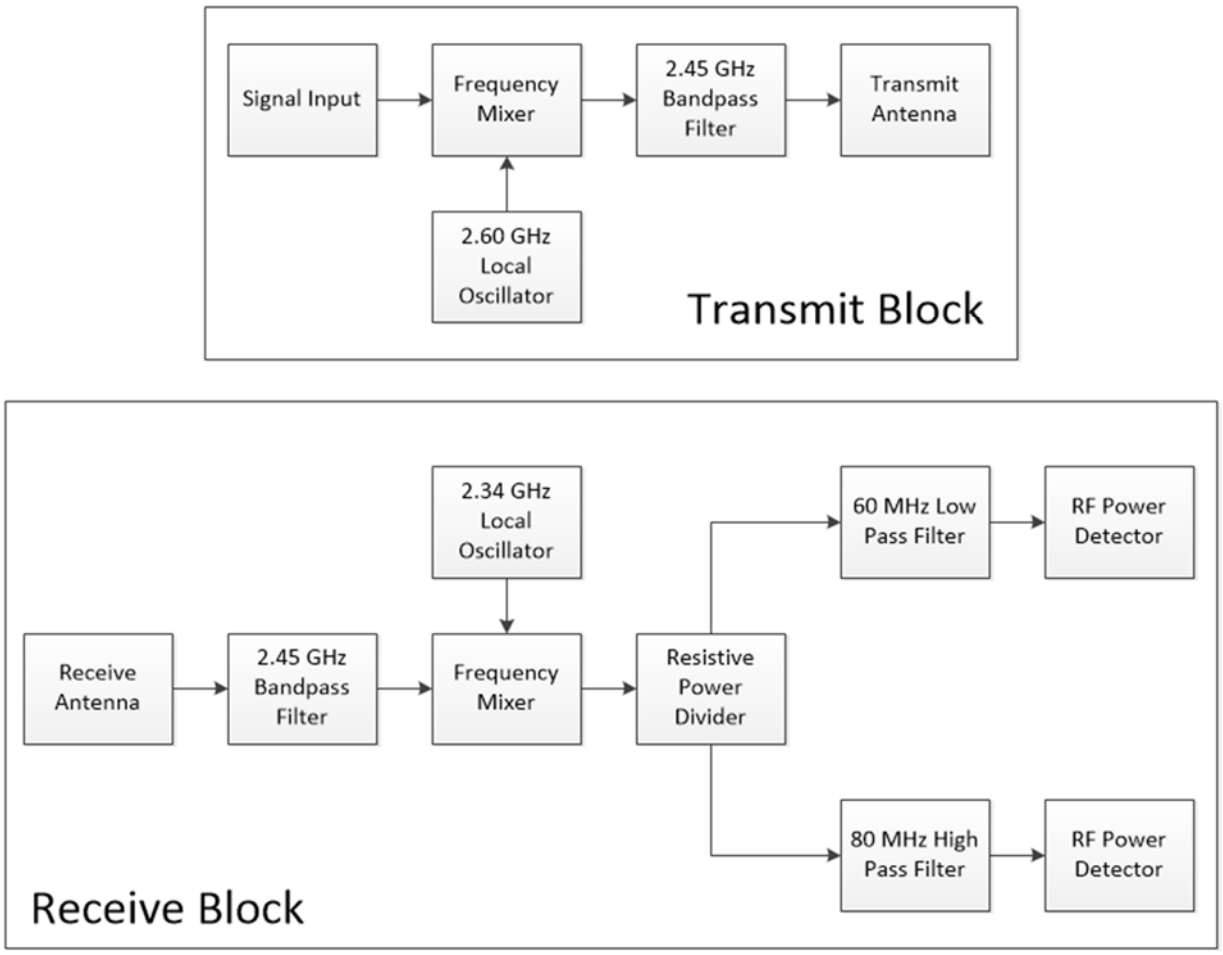


Figure 4-1 - RF Link Block Diagram

4.2 Power Supplies

The power supply and front-end protection were initially designed for the receive circuit and then copied over to the transmit and detector circuits once it was proven successful. Based on initial component selection research, a 5 V supply was identified as the best option. To achieve this a 5 V LDO, TLE4274-2D V50, was selected [14]. Further specifics about the device can be found in its datasheet. Using a switched-mode-power-supply (SMPS) would have been excessive and needlessly complicated. The voltage regulator that was selected also meets the reverse protection and input range requirement as it can tolerate an input of ±40 V and has an

operating range of 5.5 to 40 V while supplying up to 400 mA. The loading requirement of this supply was not fully known so extra headroom was factored into the component selection as this IC was used to power multiple different circuits. The power supply schematic used for the transmit PCB is show below in Figure 4-2.

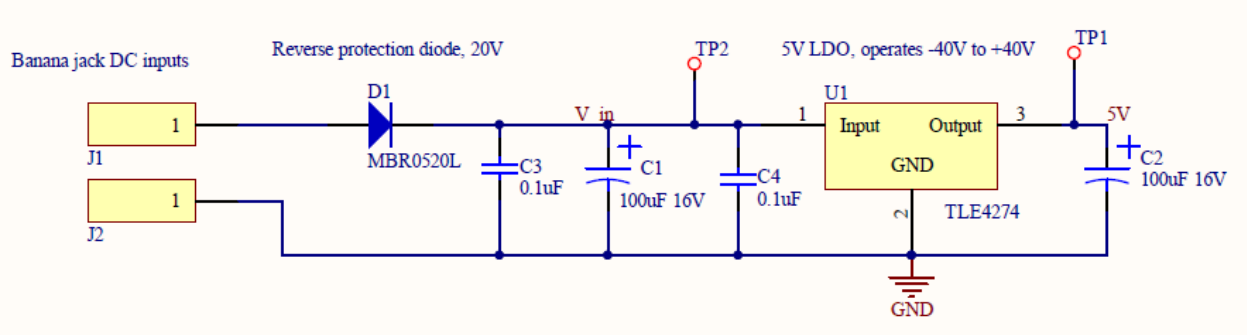


Figure 4-2 - Power Supply Circuit

The capacitor values used on the input and output of the regulator are the recommended components as suggested by the TLE4274's data sheet. One of these capacitors, C1, is an electrolytic capacitor and vulnerable to damage caused by reverse polarity. To add further reverse polarity protection, a 20 V Schottky diode, with a 0.385 V nominal forward voltage, was added as the first series element in the power supply circuit [15]. This component selections give the power supply circuit a safe operation input voltage of 6 to 15 V.

4.3 Local Oscillator and Voltage Tuning

Both the transmit and receive circuits were broken down into two separate elements, the mixing frequency generation and the up-down converter that would perform the mixing. A VCO was selected to provide the LO mixing frequency generation. Much like the power supply circuit, the VCO would be used for both the transmit and receive PCB. To meet this, the MAX2750 from Maxim was selected. This VCO has a supply input range of 2.7 to 5.5 V and

can generate a frequency of ~2200 to 2600 MHz at -3 dBm based on a control voltage input of 0 V to 3 V [16]. Further specifics about the device can be found in its datasheet. The VCO and its supporting components are shown below in Figure 4-3. This circuit was used for both the transmit and receive designs as it meets the requirements for both.

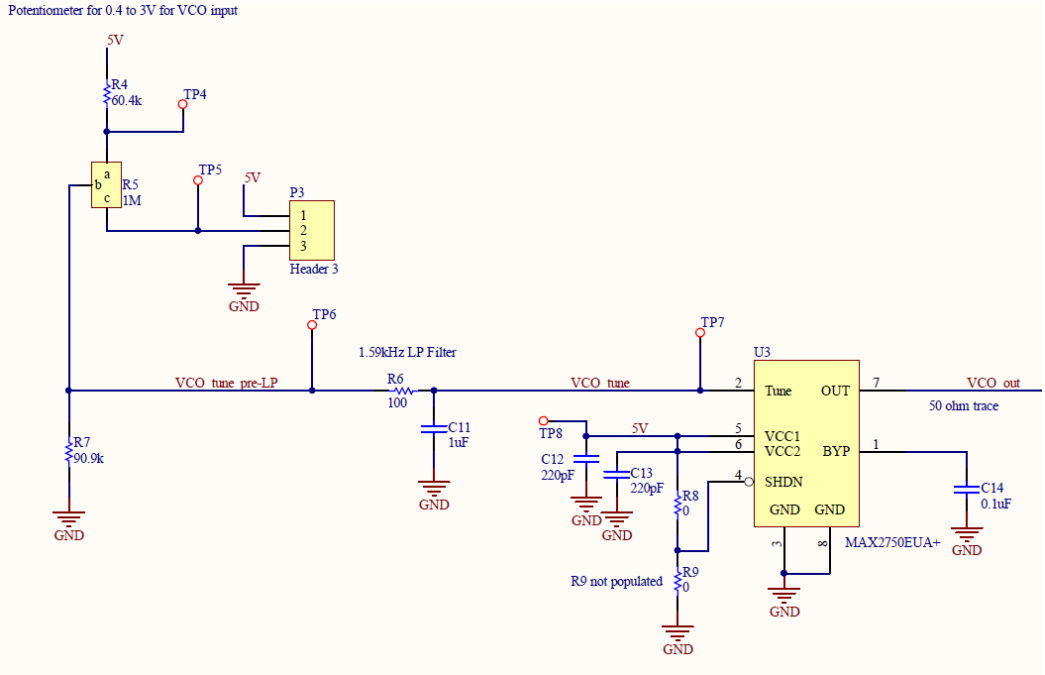


Figure 4-3 - VCO and Tuning Circuit

To create the tuning voltage, a voltage divider was implemented using a 21 turn 1 MΩ trimmer resistor. This provided a slow and smooth change in the tuning voltage to the VCO through a 1.59 kHz lowpass filter. The trimmer resistor was used over a more accurate phase-locked loop (PLL) for several reasons. The most obvious reasons are that cost was reduced, less components are needed, and there is a smaller footprint on the PCB. The trimmer resistor is also less complex than a PLL since all the operations can be directly controlled by the end user without the use of a digital interface. While the PLL would have provided a more accurate output from the VCO, programming the registers of a PLL would have worked against the

tunability and ease of measurement requirements. It was determined that the lack of closed loop feedback from the use of a simple trimmer resistor was acceptable as the purpose of the RF system is to educate students on its functionality and not create a high-performance design. The values for C12, C13, and C14 were the suggested values given in the MAX2750 datasheet.

Once the transmit circuit was fully built, the operational frequency range of the VCO was measured with a nearfield probe. The IF input and RF output of the mixer were terminated with 50 Ω loads. It was verified that the MAX2750 was able to output a LO frequency range of roughly 2314 - 2608 MHz with an input range of 0.390 to 3.010 V, as designed. The stability of the VCO was characterized by how much the output frequency would drift by applying freeze spray and a heat gun to the VCO IC and taking a rough temperature measurement with a thermal couple. Applying 5 seconds of freeze spray to approximately cool the board to 0°F caused the VCO to drift roughly 13 MHz, see Figure 4-4.

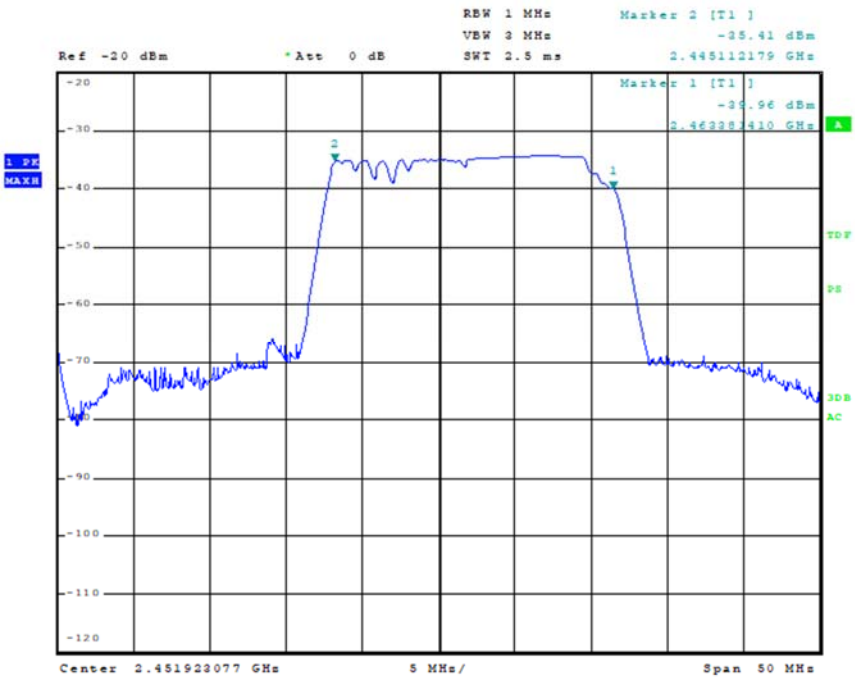


Figure 4-4 - VCO Frequency Drift - Cold

Applying 5 seconds of heat to increase the temperature to roughly 250 °F caused the VCO to drift by roughly 10 MHz, see Figure 4-5

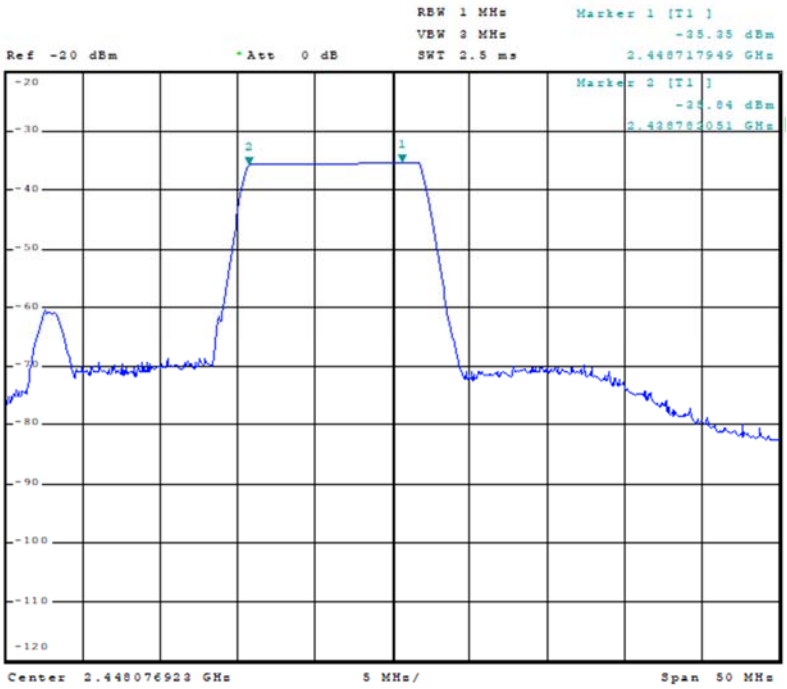


Figure 4-5 - VCO Frequency Drift - Hot

4.4 Transmit Circuit

For the RF generation of the transmit circuit an up-down converter was selected to provide the mixing. A MAX2671 was identified as an IC that would meet the requirements of the design. This up-down converter has an IF input range of 40 to 500 MHz with a maximum input power of +10 dBm, has a LO input range of ~600 to 2500 MHz with a maximum input power of +10 dBm, an RF output range of ~400-2500 MHz, offers LO to RF port isolation of -36.8 dBm, and operates off a DC input voltage of 2.7 to 5.5 V [17]. Further specifics can be found in the device's data sheet. The upconverter circuit is shown below in Figure 4-6. Values for L1, L2, C6, C7, and C15 were selected with guidance from the data sheet based on the

desired frequency of operation to assist with impedance matching. R2 was populated with a zero-ohm jumper and R3 was skipped. All RF traces were kept as short as possible and kept at a characteristic impedance of 50 Ω. This was to minimize unwanted reflections and RF coupling from internal or external sources. The PCB used had a nominal thickness of 62 mil, 4 layers with internal ground and 5V power planes on FR-4 material.

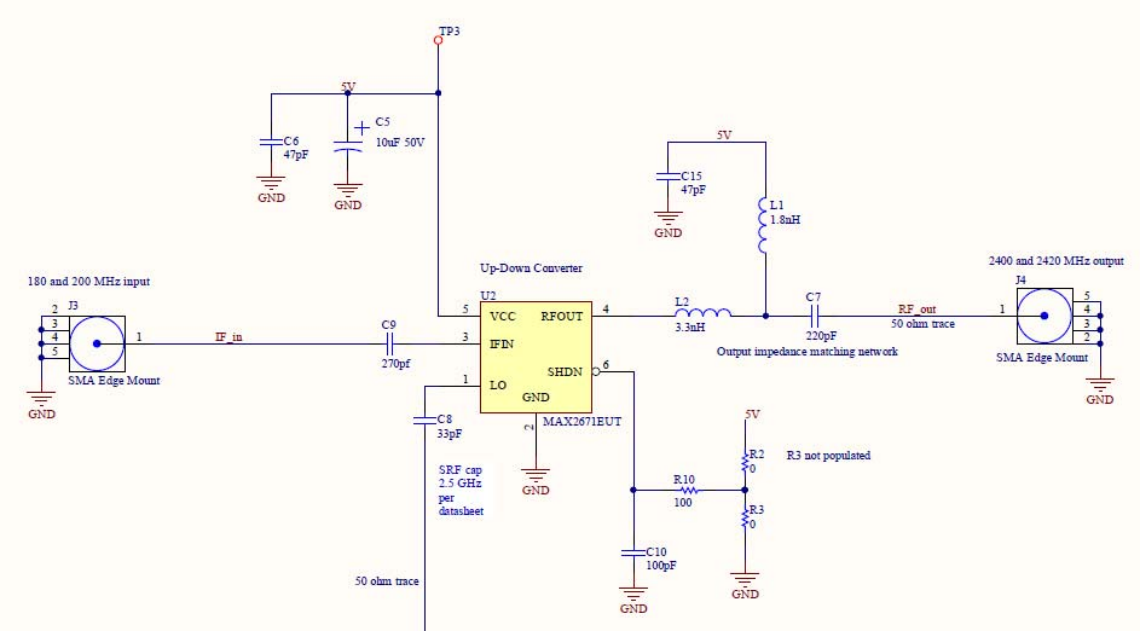


Figure 4-6 - Transmit PCB Upconverter Circuit

The MAX2671 has an IF port that is able to operate with an input power range of -50 dBm to +10 dBm [17]. This allows a for wide range of drive strength options to investigate how well the system operates, isolates other RF sources, and how quickly different devices can go into compression. The MAX2671 has an LO power input range of -35 to +10 dBm which allowed for any unexpected or unaccounted for losses in the VCO output power. Given the nominal VCO output of -3 dBm, the MAX2671 will be operating with a linear conversion gain [17].

The transmit circuit was designed to take either 200 or 180 MHz IF and mix it with a LO of 2600 MHz to provide an RF output at 2400 or 2420 MHz, respectfully. These requirements were verified through measurements of the transmit circuit. Given a -25 dBm input at 200 and 180 MHz the measurements in Table 4-1 were taken.

IF Frequency	**LO Frequency**	**LO Tuning Voltage**	**RF Output Frequency**	**RF Output Amplitude**	**LO on RF Amplitude**	**IF on RF Amplitude**
200 MHz	2600 MHz	2.898 V	2.399 GHz	-28.47 dBm	-35.95 dBm	-61.71 dBm
180 MHz	2600 MHz	2.898 V	2.420 GHz	-29.45 dBm	-35.91 dBm	-63.19 dBm

Table 4-1 - Transmit Circuit Measurements

4.5 Receive Circuit

The majority of the receive circuit design is copied and pasted directly from the transmit portion. As stated in sections 4.2 and 4.3, both the power supply and VCO circuits were designed with the intent to be used in both the transmit and receive designs. To this same extent, a very similar up-down converter IC was selected for the receive circuit, the MAX2682 from Maxim. This downconverter functions very similarly to the MAX2671 upconverter. Beyond the functional inversion, one key difference is that the RF pin and IF pin positions are swapped.

The MAX2682 downconverter has an RF input of 400 to 2500 MHz with a maximum input power of +10 dBm, a LO input range of 400 to 2500 MHz with a maximum input power of +10 dBm, an IF output range of 10 to 500 MHz, LO to IF port isolation of approximately 20 dBm, and operates off a DC input voltage of 2.7 to 5.5 V [18]. Further specifics can be found in the device's data sheet. The downconverter circuit is shown in Figure 4-7. Values for L1, L2, C7, and C9 were selected with guidance from the data sheet based on the desired frequency of operation in order to assist with impedance matching. In addition to this, R10 and R11 were added as precaution if additional filtering or impedance matching was required. R10 was populated with a zero-ohm jumper and R11 was skipped. All RF traces were kept as short as

possible and kept at a characteristic impedance of 50 Ω. This was to minimize unwanted reflections and RF coupling from internal or external sources. The PCB used had a nominal thickness of 62 mil, 4 layers with internal ground and 5V power planes on FR-4 material.

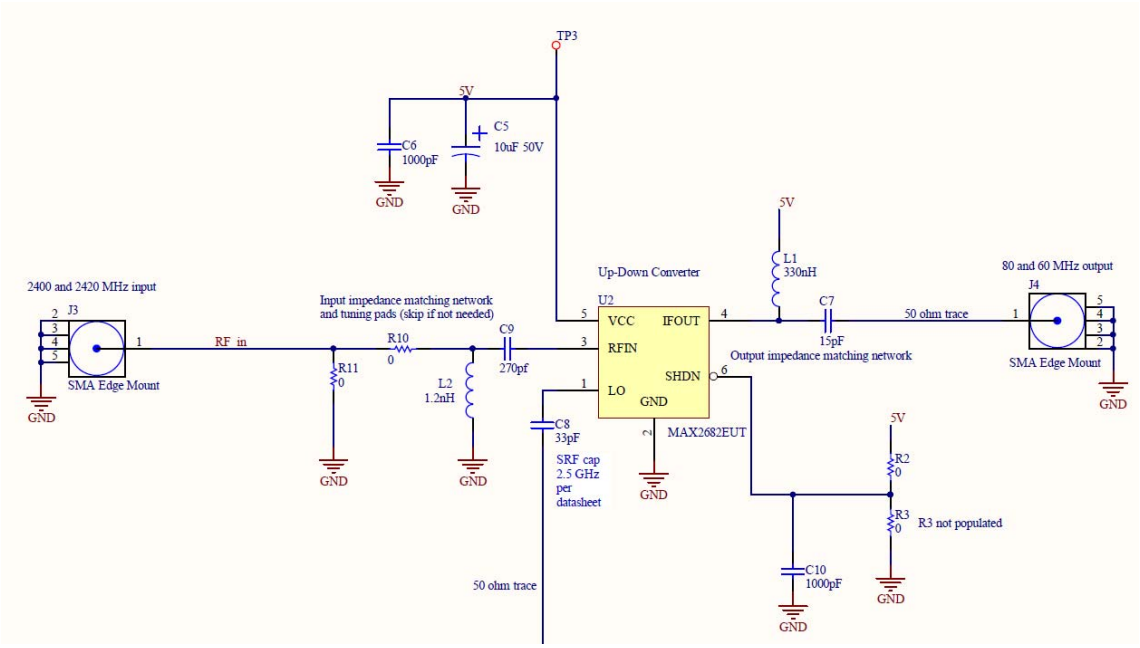


Figure 4-7 - Receive PCB Downconverter Circuit

No sensitivity floor for RF input power was provided in the datasheet, however several measurements stated in the datasheet mention they were performed with a RF input of -25 dBm [18]. Realistically, the low end of the MAX2682's RF input is mostly likely comparable to that of the MAX2671's IF input of -50 dBm. With this taken into consideration, no amplification was planned for in either the transmit or receive circuits as both devices had enough sensitivity per their data sheets.

The receive circuit was designed to take an 2400 and 2420 MHz RF signal and mix it with an LO of 2340 MHz and provide an IF output of 60 and 80 MHz. Given an RF input of -25 dBm at 2400 and 2420 MHz the measurements in Table 4-2 were taken.

RF Frequency	LO Frequency	LO Tuning Voltage	IF Output Frequency	IF Output Amplitude	LO on IF Amplitude	RF on IF Amplitude
2400 MHz	2340 MHz	0.456 V	60.53 MHz	-30.45 dBm	-22.47 dBm	-42.39 dBm
2420 MHz	2340 MHz	0.456 V	80.63 MHz	-28.75 dBm	-22.42 dBm	-41.22 dBm

Table 4-2 - Receive Circuit Measurements

4.6 Power Divider

To split the IF output of the receive circuit, a signal splitter was required. A lossy 3-port resistive divider was used to split the input into two outputs signals that were 6 dB below the input power [2]. The circuit for the resistive power divider is shown in Figure 4-8.

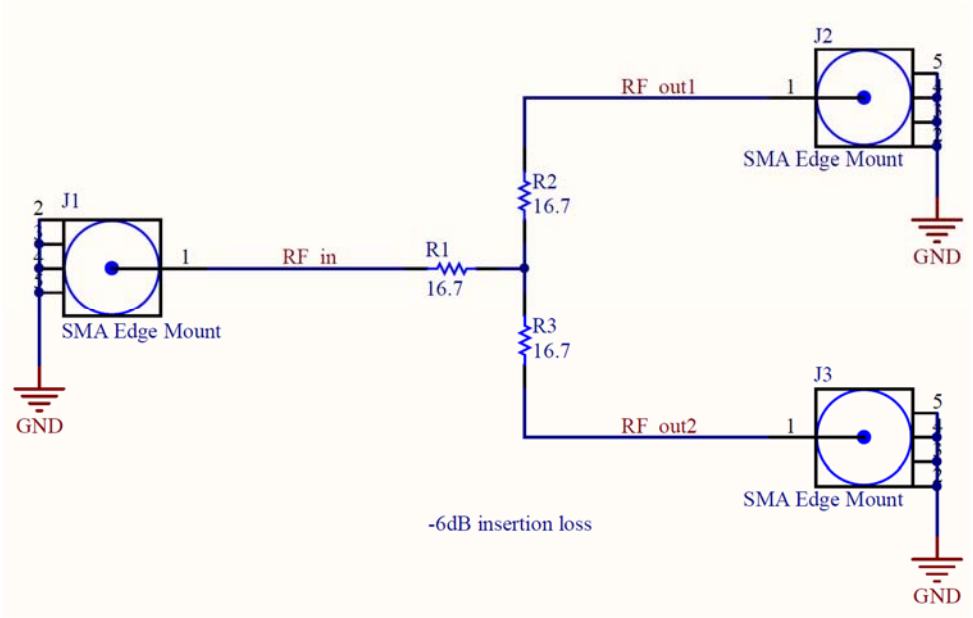


Figure 4-8 - Resistive Divider Circuit

This PCB was built on an RO4003C substrate as it was an impedance sensitive design. This also had the benefit of the board being able to be built on the LPKF ProtoMat S103 circuit board plotter. The resistive splitter is a simple design that did not require multiple layers or vias. When measured the design was found to have an insertion loss (input to output) of ~6 dB across

the frequency range of 1 to 1000 MHz. The output to output isolation was found to be the same as the insertion loss which was expected due to the design.

4.7 Filters

Four different filters are used in the RF system; an 2400 MHz bandpass transmit filter, an 2400 MHz bandpass receive filter, an 60 MHz low pass detector filter, and an 80 MHz high-pass detector filter. For the transmit and receive bandpass filters, the edge-coupled RO4003C filter as selected due to this filter having the least deviation between the simulated and measured results even though all eight of fabricated filters performed similarly in the 2.4 GHz ISM band. For more information on the distributed element filters, refer to sections 3.3, 3.4, and 3.5 where they were originally discussed.

The 60 and 80 MHz filters are used to sort the 60 MHz low bits and the 80 MHz high bits between the individual detector circuits. The filters were designed using the Passive Filter tool within Genesys. Both filters were designed using the same parameters except for the difference of one being a low pass filter and the other being a high-pass filter. The filter simulation settings used are shown below in Table 4-3.

Input/output Impedance (Ω)	**Passband Ripple (dB)**	**Attenuation at Cutoff (dB)**	**Order**	**Cutoff Frequency (MHz)**
50	0.25	0.25	11	70

Table 4-3 - Genesys Detector Filter Settings

Unfortunately, the detector filter PCB was designed and ordered before the full RF signal path was able to be built and measured. This means the minimum attenuation in the stop bands that was needed to prevent any false triggers or cross talk between channels was unknown. To compensate for this, an 11^{th} order filter was used to provide at least 30 dB of attenuation between the two channels. This coupled with the 6 dB loss from the power divider and roughly 4 dB of

loss from the receive circuit means that approximately 40 dB of isolation will be achieved between the 60 MHz low channel and the 80 MHz high channel.

The PCB used had a nominal thickness of 62 mil, was 2 layers, and used FR-4 material. The simulated and measured results of each filter are shown below in Table 4-4. The measured response for each filter is shown below in Figure 4-9 and Figure 4-10.

	60 MHz Low pass			80 MHz High-pass		
Measurement Source	**Attenuation at 60 MHz**	**Attenuation at 80 MHz**	**Corner Frequency**	**Attenuation at 60 MHz**	**Attenuation at 80 MHz**	**Corner Frequency**
Simulated	-0.689 dB	-30.063 dB	72.7 MHz	-39.193 dB	-0.143 dB	68.7 MHz
Measured	-3.450 dB	-38.550 dB	71.3 MHz	-36.400 dB	-2.530 dB	63.8 MHz

Table 4-4 - Detector Filter Simulated and Measured Results

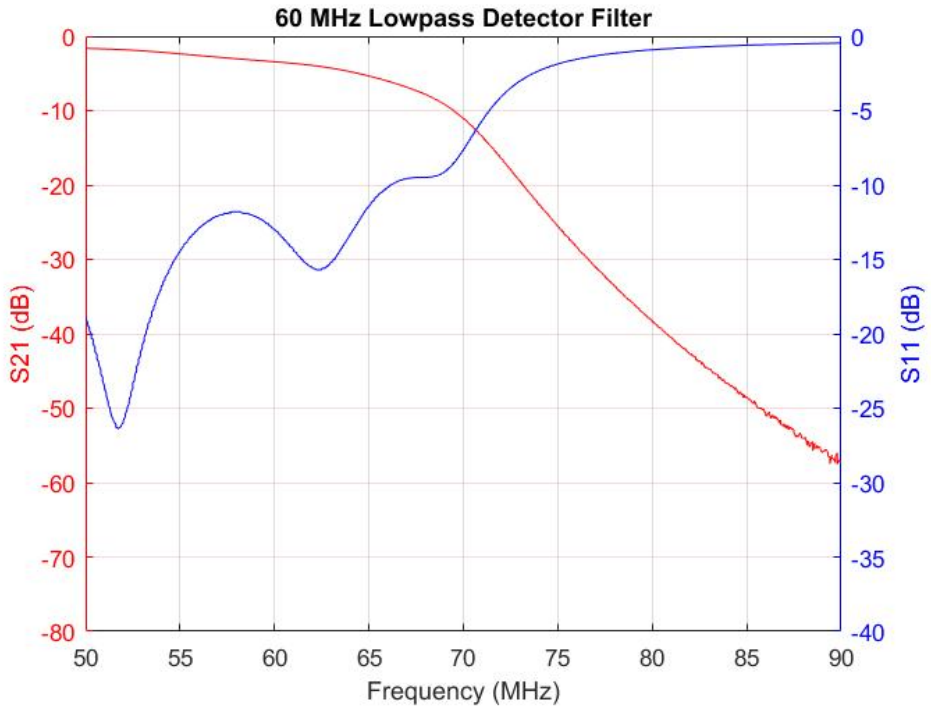


Figure 4-9 - 60 MHz Low Pass Filter Measured Response

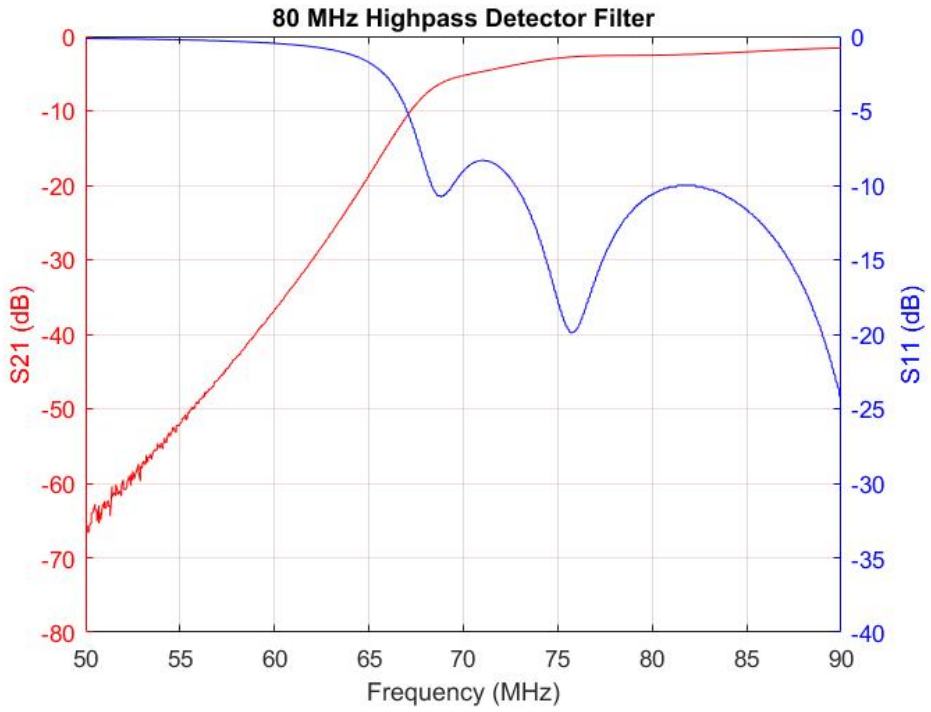


Figure 4-10 - 80 MHz High-pass Filter Measured Response

Both filters had slightly more loss than expected at their intended frequency of operation, with the 60 MHz low pass filter down an additional 2.761 dB to -3.450 dB and the 80 MHz high-pass filter down 2.387 dB to -2.530. This could have been caused in part by using cheaper, lower quality components with higher ESR and ESL or simply due to incomplete information in the simulated results such as the Q or parasitics of the components. Cheaper components were used instead of higher quality RF components in effort to keep costs down as the highest intended signal is 80 MHz. However, the insertion loss, roll off, and corner frequency of each of the filters was found to be acceptable as no unwanted performance was measured and was not investigated further.

4.8 Detector Circuit

Since the RF system did not have an advanced modulation scheme, and instead only transmitted a continuous wave (CW) signal, a simpler detector circuit could be used. The main function of the detector circuit was to turn on an LED when an 60 MHz or 80 MHz signal was present, depending on which "bit" the detector was responsible for. With one detector attached to each filter, only one would be active at a time. To detect when RF was present, independent of frequency, a MAX2014 logarithmic amplifier was selected. This device accepts an RF signal between 50 and 1000 MHz and converts it into a DC voltage that is proportional to the RF power at its input and scales from roughly 0.7 to 1.8 VDC given an RF input range of -65 to +5 dBm [19]. Further specifics can be found in the devices data sheet. Once the RF is scaled to a DC voltage, an MCP6545 op-amp comparator was selected as a trigger to turn on an LED indicator [20]. The trigger voltage reference level is set by the voltage divider network created via a 500 kΩ trimmer resistor on the MCP6545's inverting input. In order for the MCP6545 to trigger off of the full range of the MAX2014s 0.7 to 1.8 VDC output, the trimmer resistor needed to be set somewhere between 430 kΩ and 320 kΩ when measured between the wiper and ground. The log amplifier and comparator circuits used along with components as suggested by their data sheets are shown below in Figure 4-11. No components are present to assist with impedance matching due to the low frequency of operation and electrically short trace length. The PCB used had a nominal thickness of 62 mil, was 2 layers, and was implemented on FR-4 material. Due to the separation between the top and bottom layers a 50 Ω trace was not used for the RF input at the SMA connector as the width required to reach that impedance was close to 140 mils. This was deemed a very low risk as the total distance between J3 and the RF input into U2 was less than 1.5 cm, which is less than 1/100th of a wavelength at 100 MHz.

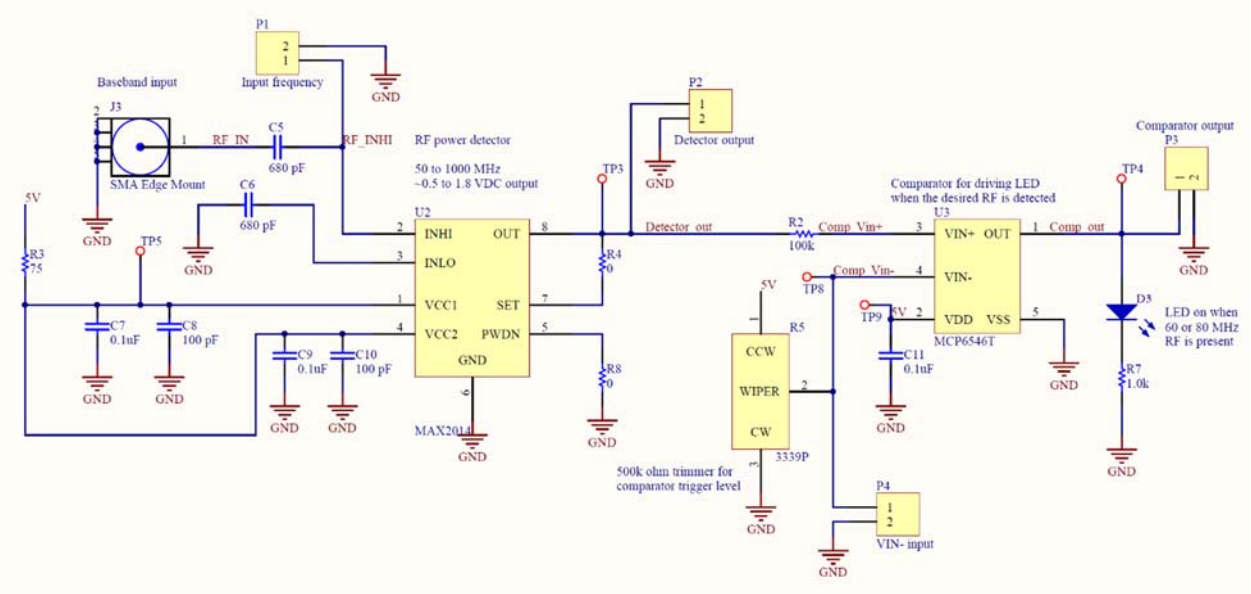


Figure 4-11 - Detector Circuit

However, when the design was built up, a current draw of more than 0.70 A was observed with the source of this issue traced back the incorrect assumption that the MCP6546 was an open-drain device. The initial schematic as shown in Figure 4-11, is based off the assumption that the MCP6546 is supplying current and that no additional components were needed. To correct for this, R7 was move into a pull-up configuration and two more resistors were added to hard set the voltage at the inverting input of the MCP6546 to 1.02 V. These changes were done as hand modifications. The updated schematic for the comparator portion is shown in Figure 4-12.

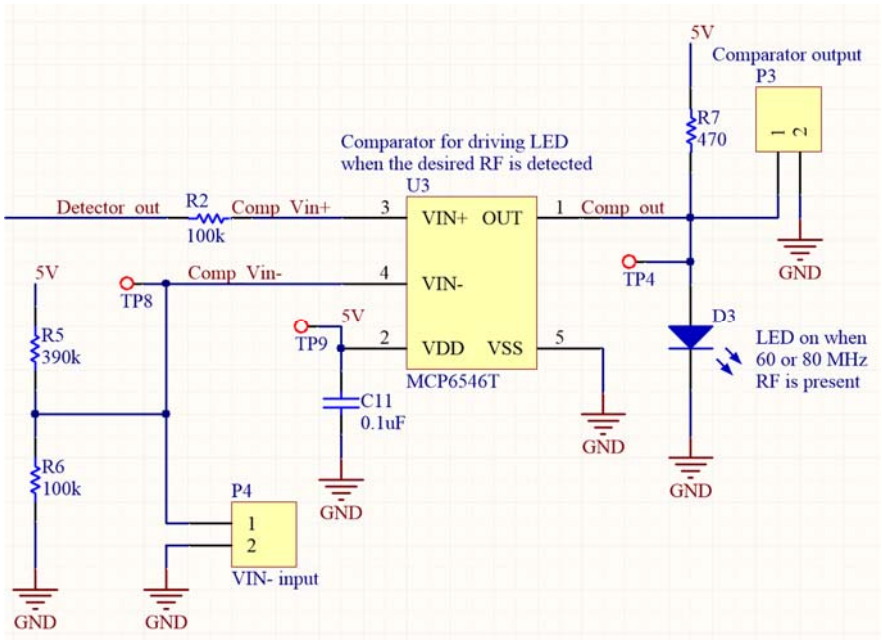


Figure 4-12 - MCP6546 Hand Modification Schematic Updates

However, even with these hand modifications to the board the excessive current draw was still present, and the board was not operational. Removing the MCP6546 from PCB stopped the excessive current draw and allowed the components that were still populated to function as designed. Removing the MCP6546 limited the functionality of the detector circuit by removing the LED indicator and the ability to set the trigger level. To compensate for this reduced functionality, the presence of RF was instead evaluated by measuring the output voltage of the MAX2014 with a digital multimeter (DMM) at P2. The output voltage of the MAX2014 was measured with a 50 Ω load and across an input range of -65 to -5 dBm and recorded in Table 4-5. The 50 Ω load measurement represents the minimum DC output the detector circuit is capable of.

Detector Input Power	50 Ω load	-65 dBm	-55 dBm	-45 dBm	-35 dBm	-25 dBm	-15 dBm	-5 dBm
DC Output Voltage	0.457 V	0.626 V	0.817 V	1.015 V	1.206 V	1.401 V	1.591 V	1.756 V

Table 4-5 - Detector Circuit Trigger Levels

To help quantify the system performance, the RF environment that the RF link was operating in needed to be evaluated by finding the noise floor of the detectors. This was performed by measuring the detector's DC voltage output with the system fully configured but with the transmit circuit unpowered. A value of 0.526 V for the 60 MHz channel and 0.898 V for the 80 MHz channel was measured and was used as the noise floor of the system and acted as the minimum sensitivity for each detector channel. The presence of an RF signal sent by the transmit circuit would be indicated by a voltage above the noise floor measurement. Conversely, any detector output voltage at the noise floor while the transmit circuit was active indicated poor or inadequate reception at the receive circuit.

The 80 MHz channel had a much higher noise floor of 0.898 V when compared to the 60 MHz channel of 0.526 V. The source of this additional RF power was found to be caused by the 2.4 GHz Wi-Fi present at the time of these measurements. The 60 MHz channel transmitted at 2.4 GHz which is on the outskirts of the 2.4 GHz Wi-Fi band were little to no activity was present. This coupled with the lowpass filter meant less of the Wi-Fi signal was making its way to the detector circuit. However, the 80 MHz channel transmitted at 2.42 GHz which is well within the various Wi-Fi channels at this frequency. The majority of the Wi-Fi present was then mixed down and passed through the highpass filter to the detector. The 80 MHz channel detector circuit then translated both the intended 80 MHz BFSK signal and all the present Wi-Fi into a DC voltage. A measurement of the RF spectrum from 2350 to 2550 MHz that was present

during testing is shown in Figure 4-13. The RF spectrum of the receiver IF output has the same noise envelope, see Figure 4-14, and is contributing to the reduced sensitivity of the detector circuit.

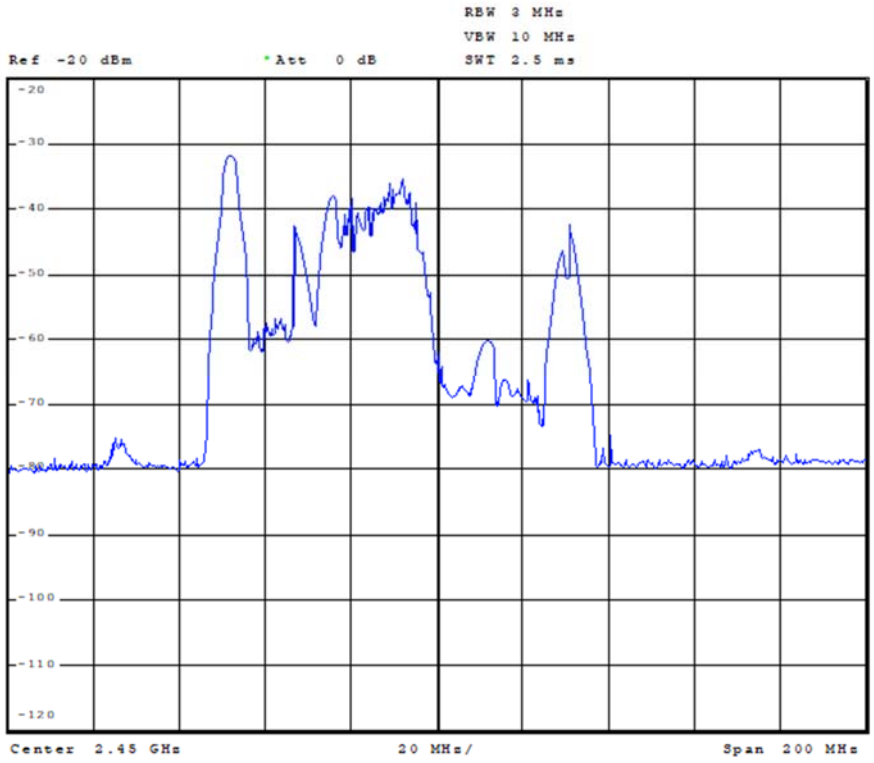


Figure 4-13 - RF Noise Spectrum

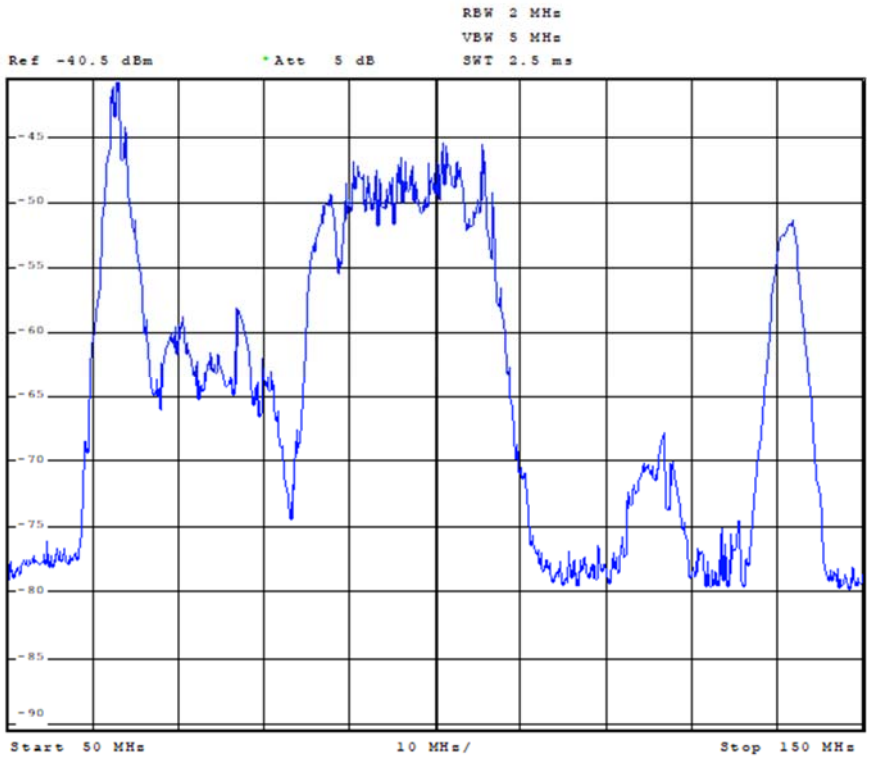


Figure 4-14 - Noise Spectrum On Detector Input

4.9 Overall System Performance

Once all the different PCBs were fabricated and assembled, the entire RF link system was tested to evaluate its overall performance using the edge-coupled RO4003C filters.

A signal generator was used to supply a 0 dB signal at 200 MHz and 180 MHz for the input signal to the transmit circuit. A DMM was used to measure the DC voltage generated by the detector circuit. All PCBs were powered with 10 VDC with separate supplies for the transmit and receive circuits. SMA cables and SMA barrels were used to interface each of the different circuits together with N type adapters used were needed to connect to RF test equipment. A stepped spectrum analyzer was used to make sure that the RF link system was configured correctly and operating as intended. This test setup was used to find the maximum distance the system would operate at. These measurements are shown in Table 4-6.

Separation		Contact		4 cm	5 cm	60 cm	65 cm
Applied Signal	**Noise Floor**	**60 MHz Signal**	**80 MHz Signal**	**80 MHz Signal**	**80 MHz Signal**	**60 MHz Signal**	**60 MHz Signal**
60 MHz Detector Output	0.526 V	1.346 V	0.554 V	0.533 V	0.531 V	0.599 V	0.527 V
80 MHz Detector Output	0.898 V	0.898 V	1.121 V	0.909 V	0.898 V	0.898 V	0.898 V

Table 4-6 - Transmit Distance Measurements

While the 80 MHz signal was lost at a separation of 5 cm between the transmit and receive antennas, the presence of the 60 MHz signal was able to be measured up to a separation of 60 cm. These measurements were taken using the edge-coupled RO4003C filter.

The entire system gain for each of the different signal paths was measured as well. This measurement is shown below in Table 4-7 and Table 4-8. It was found that the transmit signal path had roughly 4.5 dB of loss between the signal input and the input of the antenna. These loses are attributed to the upconverter and the transmit filter. Due to the similar insertion losses present in all of the distributed filters, this measurement was only taken with the edge-coupled RO4003C filter. The receive signal path was slightly more lossy with -11.4 dB for the 60 MHz channel and -7.92 dB for the 80 MHz channel. The higher loss compared to the transmit circuit is caused by the resistive splitter and detector filters that are not present in the transmit circuit. The isolation between the two detector channels was measured at approximately 42 dB.

Input Signal	Transmit Circuit Output	System Gain
-25 dBm at 200 MHz	-29.70 dBm at 2.40 GHz	-4.70 dB
-25 dBm at 180 MHz	-29.57 dBm at 2.42 GHz	-4.57 dB

Table 4-7 - Transmit Circuit System Gain Measurements

Input Signal	60 MHz Filter Output	System Gain	80 MHz Filter Output	System Gain
-25 dBm at 2.40 GHz	-36.40 dBm at 60 MHz	-11.40 dB	-67.31 dBm at 80 MHz	-42.31 dB
-25 dBm at 2.42 GHz	-66.25 dBm at 60 MHz	-41.25 dB	-32.92 dBm at 80 MHz	-7.92 dB

Table 4-8 - Receive Circuit System Gain Measurements

While the edge-coupled RO4003C filter was identified as having the smallest difference between the simulated and measured results and was the initial choice for the transmit and receive filters, the performance of the RF system using the other filters needed to be measured. To take this measurement, a constant input signal of 200 MHz at 0 dBm was applied to the transmit circuit while each of the other filter designs were used for the transmit filter. The distance between the transmit and receive antennas was recorded when a detector voltage of 0.6 V was observed. While setting up this measurement it was found that small variations in the setup and the user proximity to either of the antennas could produce a 10 to 20 mV shift in the noise floor. By measuring a detector output above the noise floor at 0.6 V, the repeatability and accuracy of the measurement was found to increase. The maximum transmit distance for each filter design is in Table 4-9. While the RF transmit distance is not a direct function of the distributed element filters, this information was captured for comparison purposes.

Filter Type	Substrate	Maximum Transmit Distance
Edge-coupled	RF-60A	39 cm
Hairpin		44 cm
Edge-coupled	CER-10	51 cm
Hairpin		46 cm
Edge-coupled	6010.2LM	50 cm
Hairpin		45 cm
Edge-coupled	RO4003C	44 cm
Hairpin		59 cm

Table 4-9 - Transmit Filter Comparison Measurements

The measurements in Table 4-9 show a range of 20 cm between the different filter designs. The edge-coupled designs performed the best for the high dielectric substrates while the hairpin designs performed the best for the low dielectric substrates. It was expected that the CER-10 filters would cause the highest reduction in transmit distance due to the high insertion loss and low S_{11} measurement. However, it outperformed RF-60A filters and had similar results to the 6010.2LM filters. The hairpin RO4003C filter was found to have the best performance and operate 15 cm further than the initial edge-coupled RO4003C filter. Taking this information into consideration, the maximum distance that the RF link would operate at was reevaluated using the hairpin RO4003C filters for both the transmit and receive filters. This ended up increasing the maximum transmit distance to 107 cm. This is an improvement of 45 cm over the original 62 cm measured when using the edge-coupled RO4003C filters.

It was expected that the transmit distance would be proportional to the insertion loss and/or the S_{11} measurement of the filter. However, as shown in section 3.5 there is only roughly 0.45 dB of difference in the measured insertion loss between all of the filters, excluding the hairpin CER-10 design. A more likely reason behind the variation in transmit distance among the various filters is the difference in filter PCB geometry. It is possible that the filter PCB had some capacitively loading effects on the electric field and perverted the radiation pattern of the antenna resulting in a transmit distance that wasn't directly proportional to the filters properties. With an antenna length of 46.46 mm and a frequency of 2.4 GHz, a reactive near field distance of 1.76 cm and far field distance of 3.45 cm can be found [21]. The floating top layer pour, bottom ground layer, and non-uniform edges are all within the 1.76 cm radius of the reactive near field and could all contribute to the unintuitive transmission distance measurements. Additional cabling could be used to move the filter outside of the near field region of the

transmit antenna. These activities were not performed as the scope of this project is the RF circuits and functionality, not on the antennas and RF propagation aspects of the design. However, the optimization of the filter PCB layout and antenna separation could be a potential future work for an undergraduate engineering student.

The total cost for the RF system investigation was $349.95 with $206.35 spent on PCBs, $123.66 spent on components, and $19.94 spent for miscellaneous components such as cables and antennas. The total cost of the system could be reduced by combining multiple PCBs and ordering in bulk. This would reduce the number of different boards required as well as cut down on some of the redundant components like the multiple power supply circuits. For any undergraduate engineer labs developed around this system, a balance will have to be found between potential student activities and cost.

Chapter 5: Conclusion

Using Genesys to simulate and optimize the filter designs helped to find which combinations of filter subtype and substrates were practical to pursue further, which was a critical first step. Through these activities it was found that both the stepped impedance and the elliptic subtypes had unmanufacturable aspects of the designs due to excessively small trace widths which were on the order of 2.6 mils or smaller.

Once the edge-coupled and hairpin filters were fabricated, differences in the frequency response between each of the filter subtypes and materials were found. The 6010.2LM substrate ($\varepsilon_r = 10.2$) filters showed the largest shift upwards in the center frequency when compared to the other substrates. When compared to the CER-10 ($\varepsilon_r = 10$) material, the 6010.2LM was shifted 61.5 MHz higher for the edge-coupled design and 14.2 MHz higher for the hairpin design. It was worth noting that both high dielectric substrates experienced issues during routing and unintentionally had additional substrate material removed. Due to the softness of the material, the cutting tool was unable to make clean cuts and ended up removing additional material with each pass. This most likely caused the 3 dB ripple that was present in the passband for the CER-10 hairpin filter and also is a possible explanation for the large difference between the simulated and measured center frequencies for these substrates.

The hairpin filters experienced an overall center frequency shift up compared to the edge-coupled designs. Excluding the 6010.2LM substrate due to possible manufacturing issues, the hairpin filters overall shifted anywhere from 37.2 to 96.0 MHz while the edge-coupled filters at most experienced a shift of 9.5 MHz when comparing the measured to the simulated results. This is likely due to the additional geometry involved in the hairpin design.

No clear difference was found between the various thickness of the high dielectric boards, CER-10 and 6010.2LM. The issues with manufacturing made it difficult to compare the two with any real confidence. However, the lower dielectric substrates, RF-60A and RO4003C, performed significantly closer to the simulated results. The main outcome of the distributed element filter investigation was that the materials with lower dielectric constants were more tolerant of non-standard routing techniques and have measured S_{21} responses that were the closest to the simulated results. It was also found that the edge-coupled and hairpin designs were the most manufacturable. A possible future investigation would be to have all of the distributed element filter designs sent out for fabrication at a reputable manufacturer. This would allow for the production of fabricated products that are closer to their ideal designs and generate a better comparison between the four different substrates.

The RF system was able to successfully transmit a binary on/off BSFK signal at a maximum distance of at least 107 cm in the 2.4 GHz ISM band with a driving strength of 0 dBm. However, the 80 MHz channel was significantly noisier than the 60 MHz and required a stronger signal in order to cut through the noise. When driven at 0 dBm, the 80 MHz channel was able to operate with a separation just under 5 cm between the transmit antenna and the receive antenna. This was all completed with each major circuit block existing on separate and standalone PCBs.

The breakdown of the circuits into separate PCBs allowed each to operate and be measured independently to better showcase their contribution to the system. In order to provide options to help facilitate undergraduate engineering lab activities at GVSU, several tunable aspects were added to better show the various engineering principles that were implemented in each of the designs. The VCOs used for the transmit and receive circuits are tunable to demonstrate the up-down converter's frequency mixing. The trigger level of the detector, while

not functioning in the final design, was designed to be adjusted using a trimmer resistor to set the point at which the comparator turns on.

Future improvements to the RF system could be modifying circuit functionality to better align with course work. Since the system does not incorporate an advanced detector circuit that is mindful of any modulation, one improvement would be to have the system make use of a more noise immune modulation scheme, such as FM, that could possibly remove the need of an amplifier in order to increase the transmission distance. A second future improvement activity could be to add signal splitters to the VCO outputs in order to have a measurement port that could be used to directly understand the frequency it is operating at instead of measuring it through the output of the mixer. This was not implemented during this investigation due to time constraints and the need to design a working complete system without multiple revisions. Another future improvement would be to fully implement the detector circuit as originally designed with a working RF indicator LED and tunable trigger reference. A standard 741 op-amp with feedback to limit hysteresis would be a good option to explore as a replacement for the MCP6546 but would require a new PCB. A MCP6546R comparator would be a suitable option and would potentially not require a board change. A final future improvement would be to use a more directional antenna or a gain block to increase the effective radiated power and ultimately increase the transmit range.

Appendix A – Genesys Simulation Results

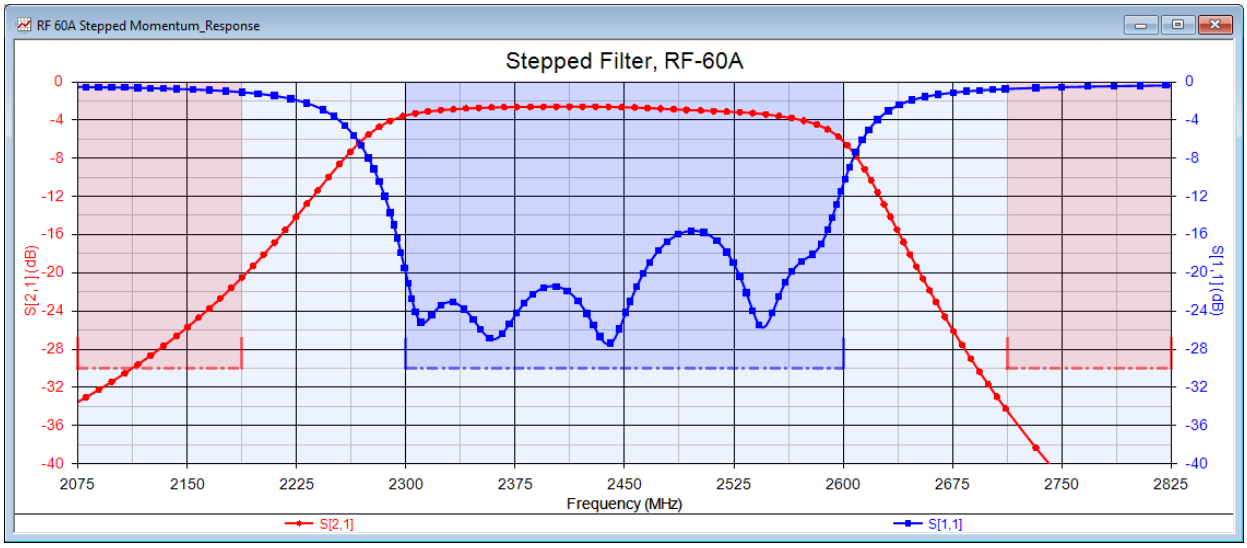


Figure A-1 - RF-60A Stepped Impedance Genesys S_{21} and S_{11} Simulations

Figure A-2 - RF-60A Stepped Impedance Genesys Layout

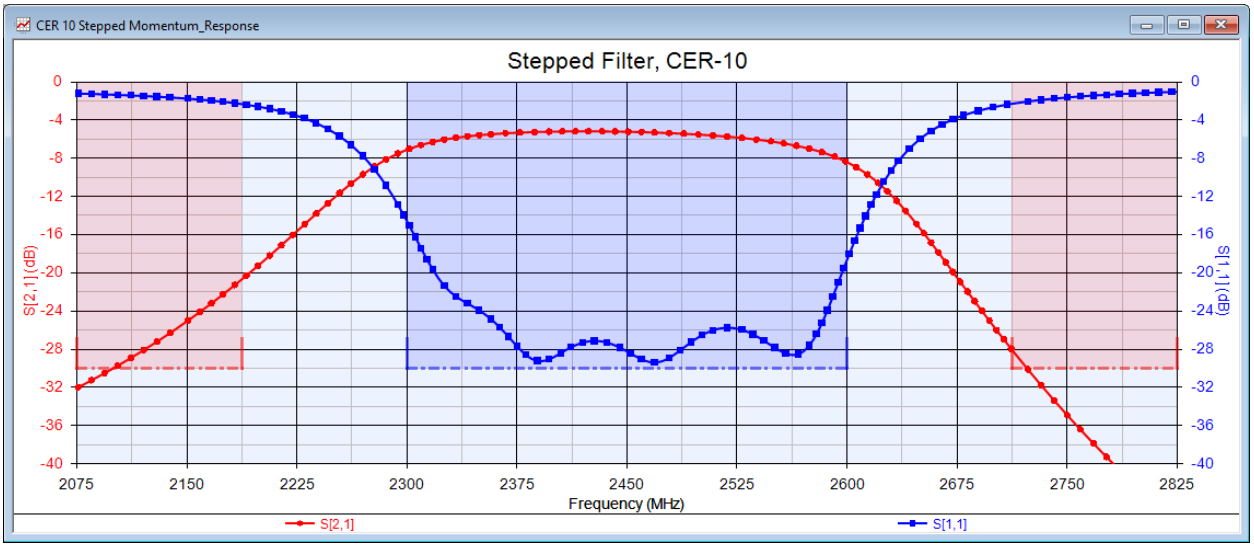


Figure A-3 - CER-10 Stepped Impedance Genesys S_{21} and S_{11} Simulations

Figure A-4 - CER-10 Stepped Impedance Genesys Layout

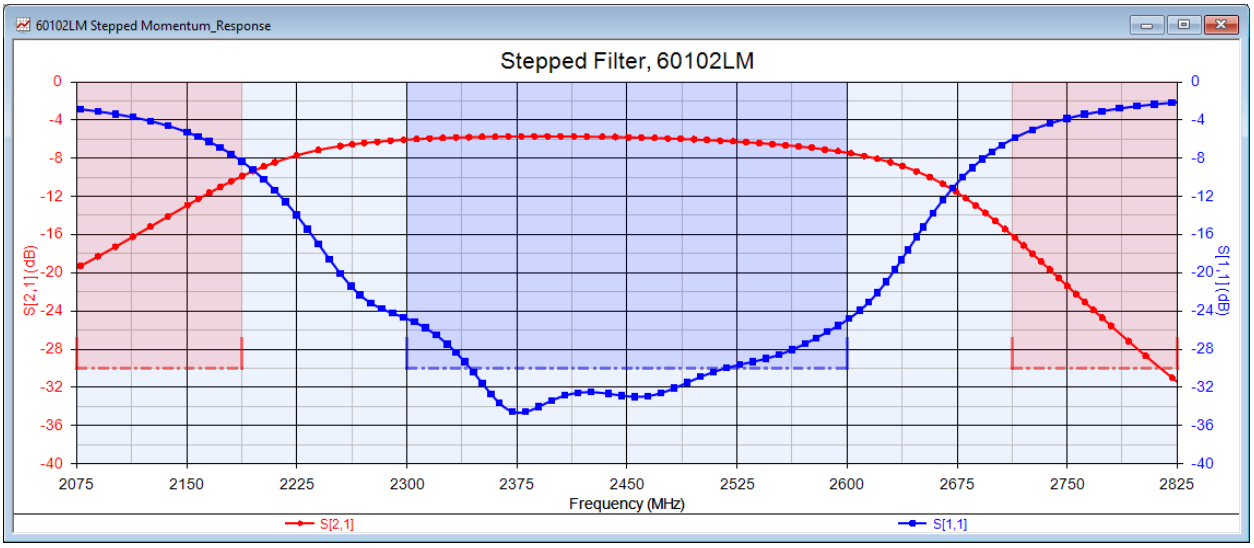


Figure A-5 - 6010.2LM Stepped Impedance Genesys S_{21} and S_{11} Simulations

Figure A-6 - 6010.2LM Stepped Impedance Genesys Layout

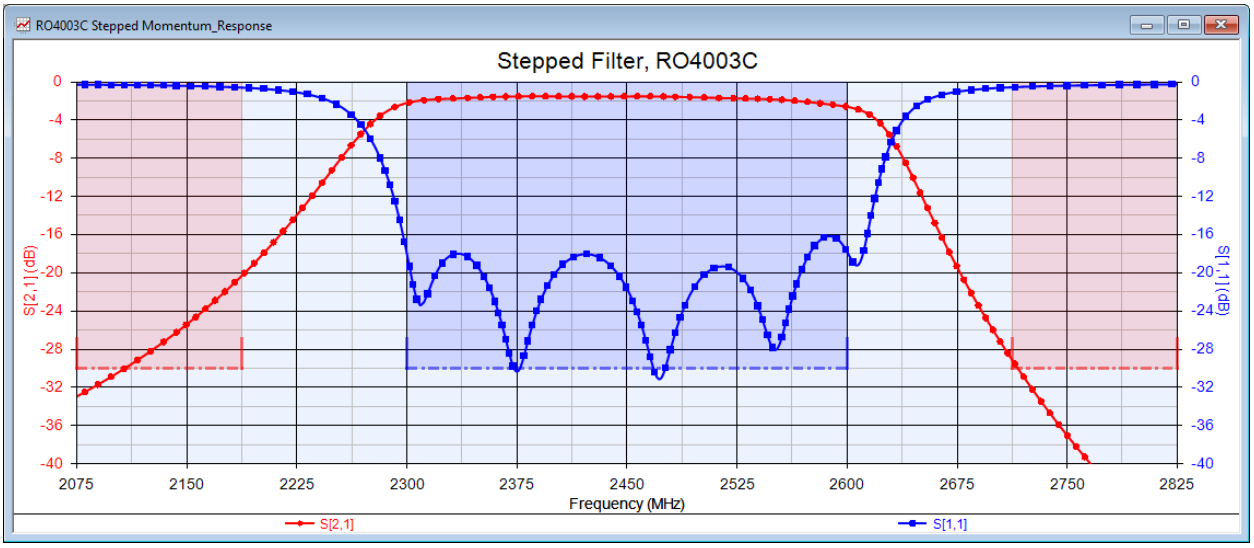


Figure A-7 - RO4003C Stepped Impedance Genesys S_{21} and S_{11} Simulations

Figure A-8 - RO4003C Stepped Impedance Genesys Layout

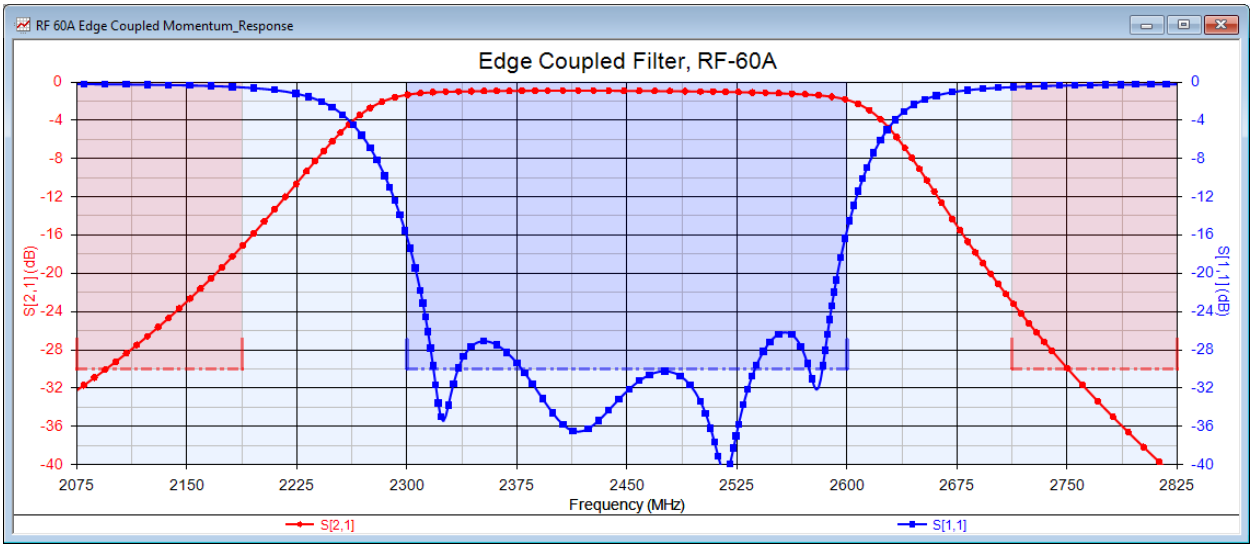


Figure A-9 - RF-60A Edge-coupled Genesys S_{21} and S_{11} Simulations

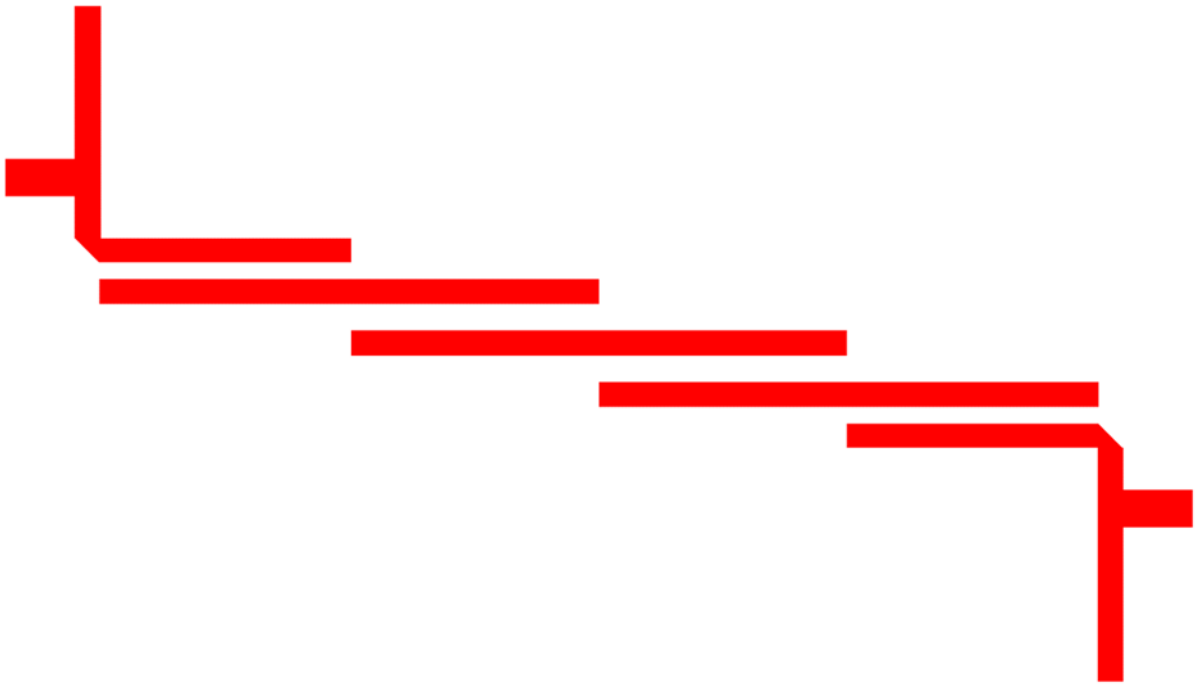


Figure A-10 - RF-60A Edge-coupled Genesys Layout

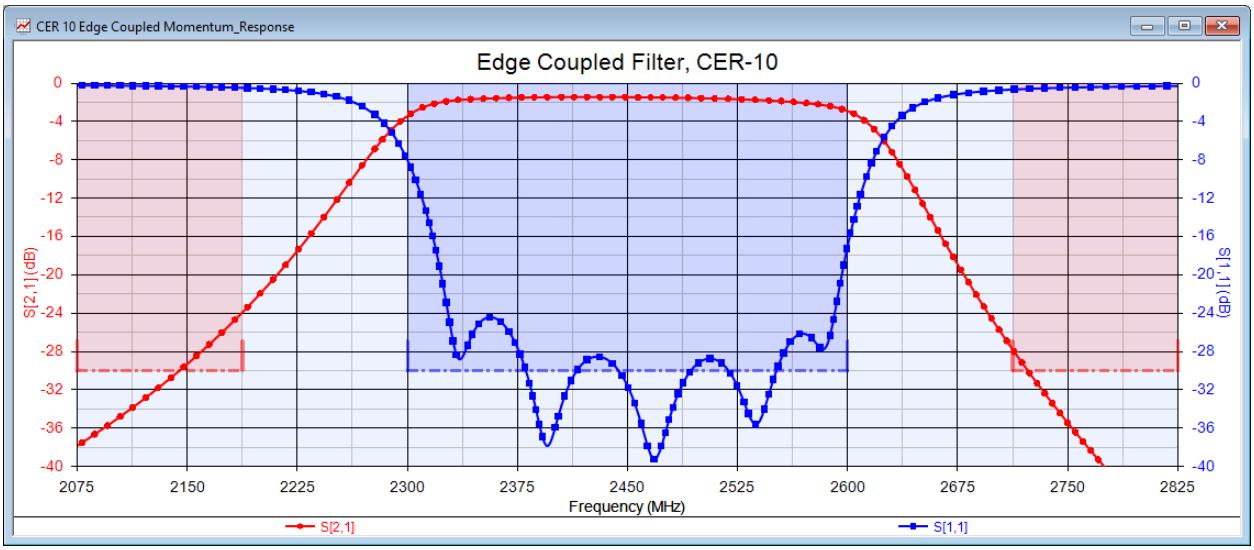


Figure A-11 - CER-10 Edge-coupled Genesys S_{21} and S_{11} Simulations

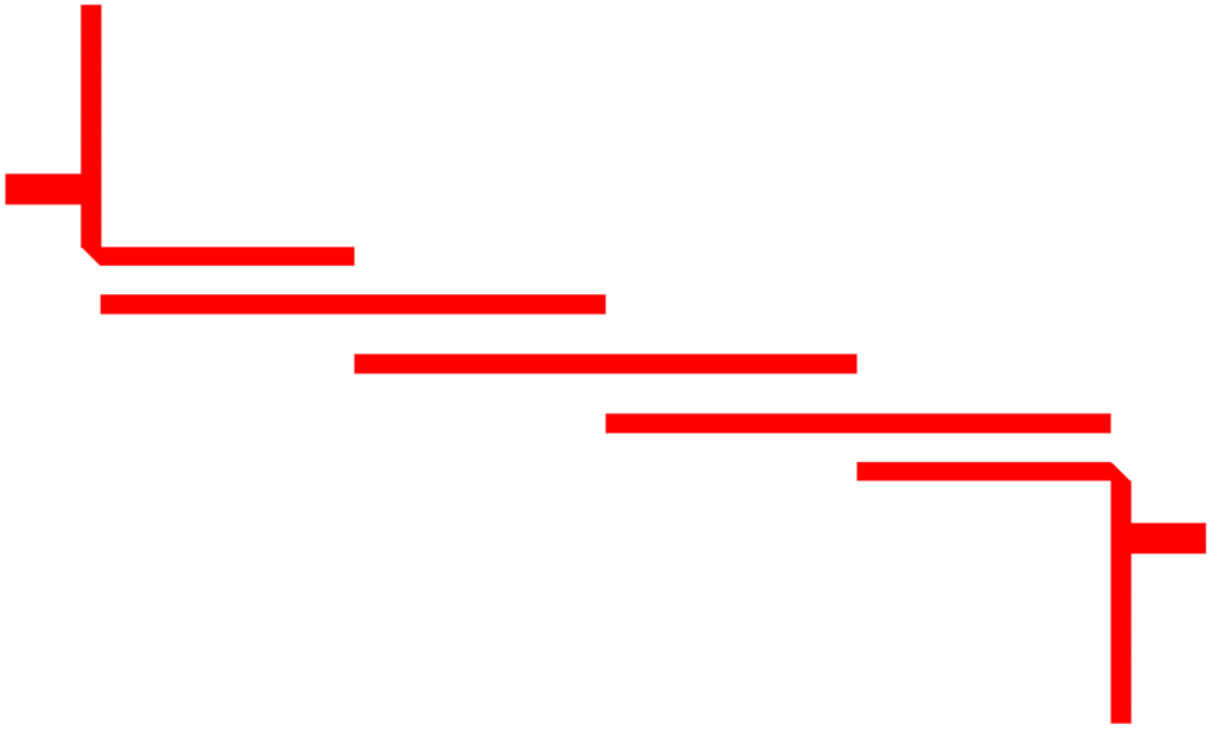


Figure A-12 - CER-10 Edge-coupled Genesys Layout

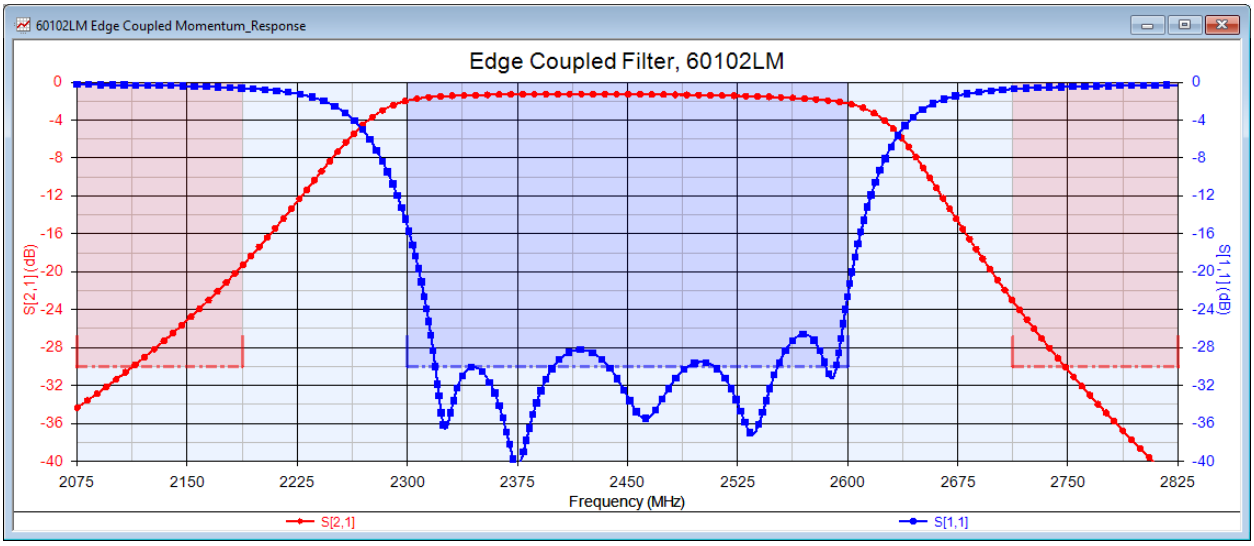


Figure A-13 - 6010.2LM Edge-coupled Genesys S_{21} and S_{11} Simulations

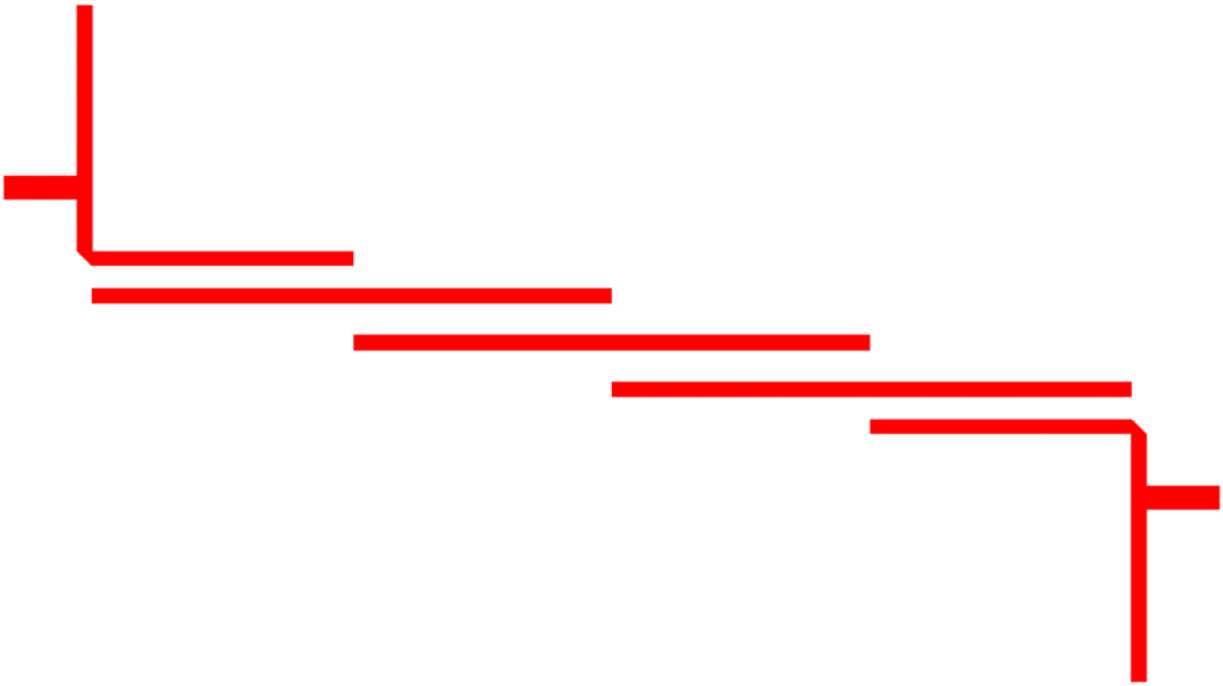


Figure A-14 - 6010.2LM Edge-coupled Genesys Layout

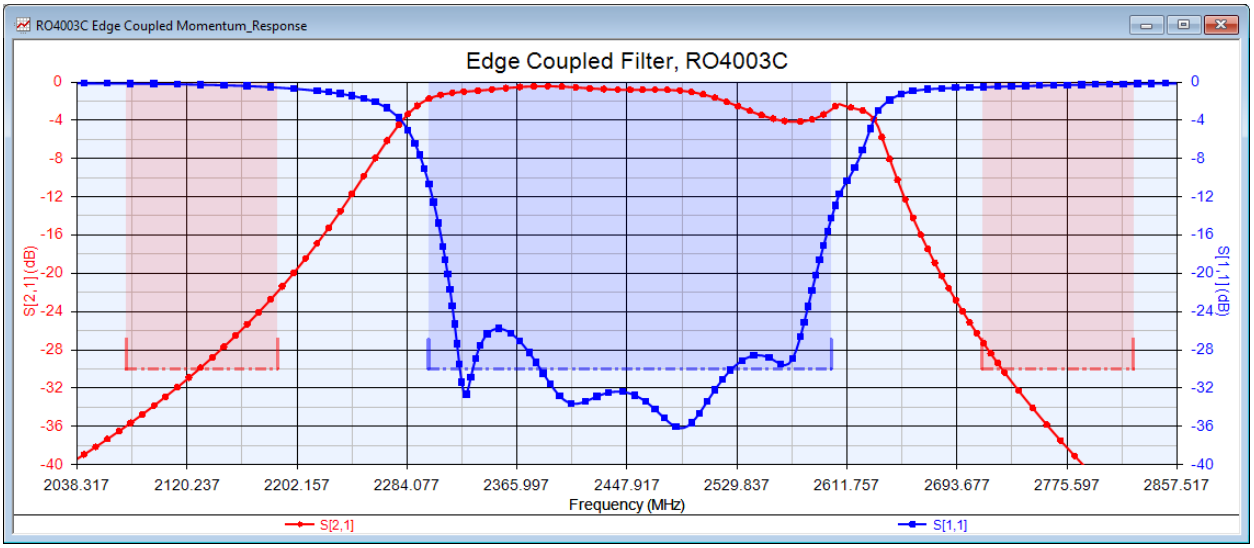


Figure A-15 - RO4003C Edge-coupled Genesys S_{21} and S_{11} Simulations

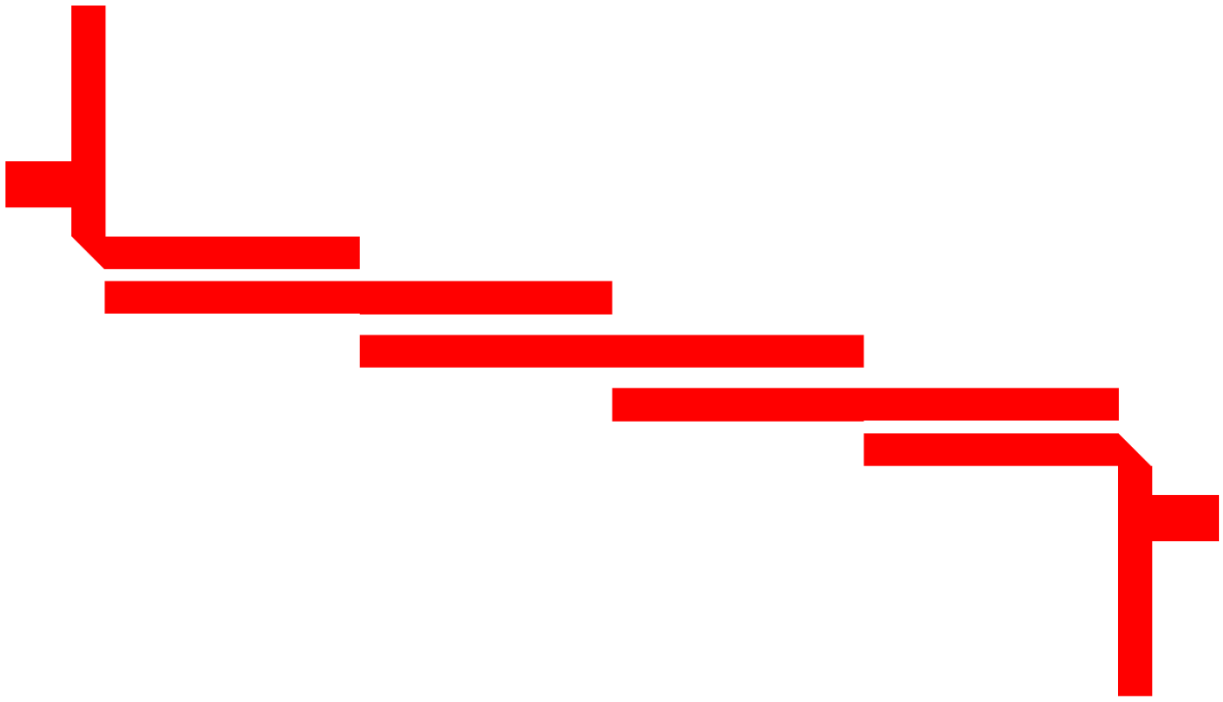


Figure A-16 - RO4003C Edge-coupled Genesys Layout

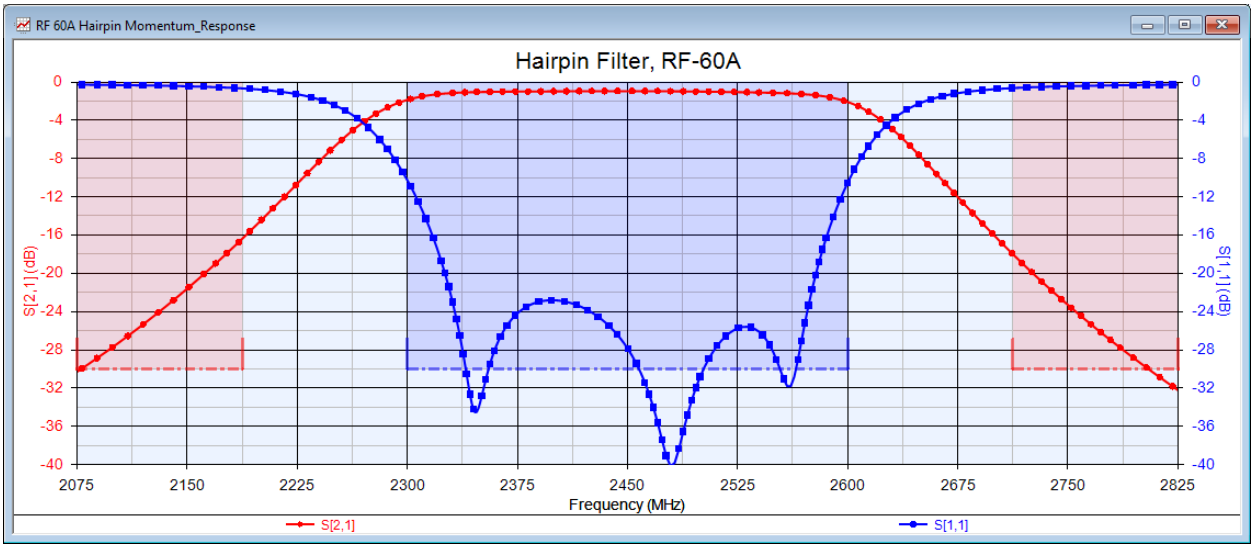


Figure A-17 - RF-60A Hairpin Genesys S_{21} and S_{11} Simulations

Figure A-18 0 RF-60A Hairpin Genesys Layout

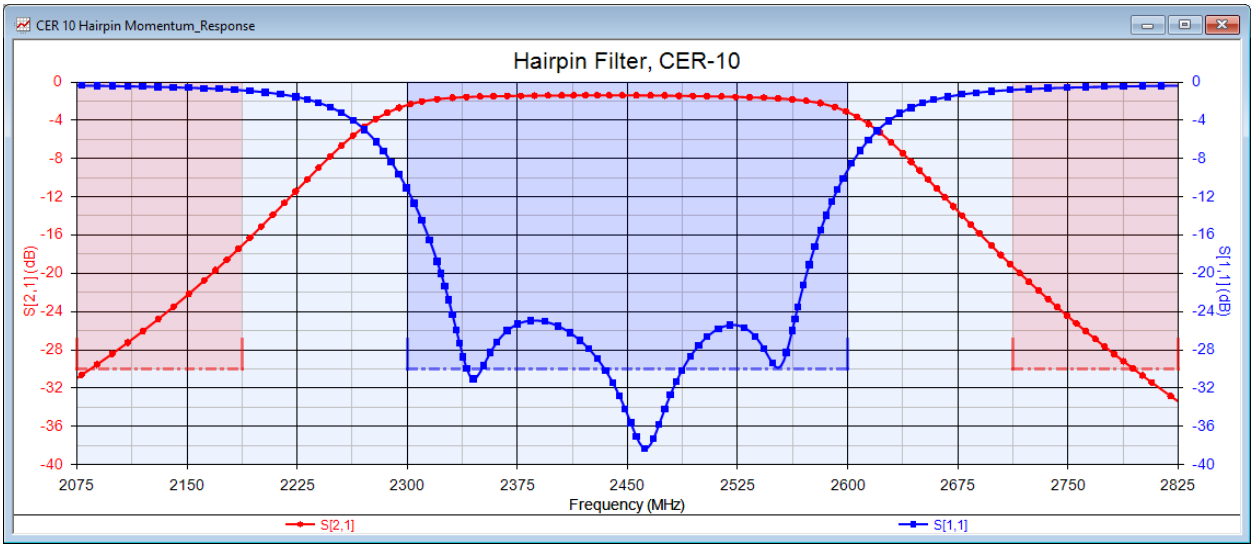


Figure A-19 - CER-10 Hairpin Genesys S_{21} and S_{11} Simulations

Figure A-20 - CER-10 Hairpin Genesys Layout

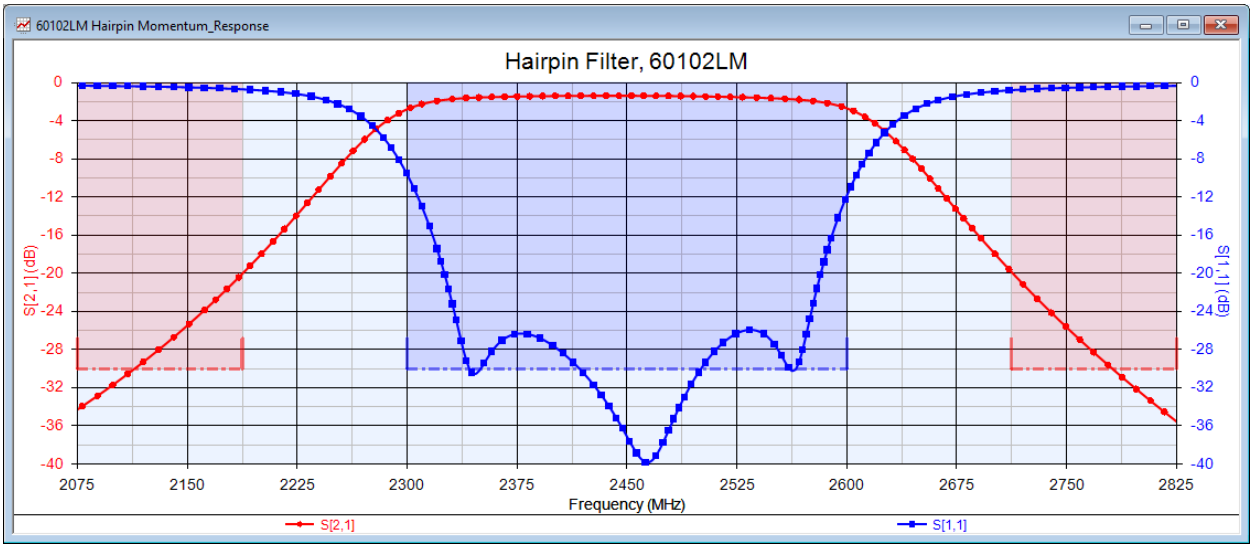


Figure A-21 - 6010.2LM Hairpin Genesys S_{21} and S_{11} Simulations

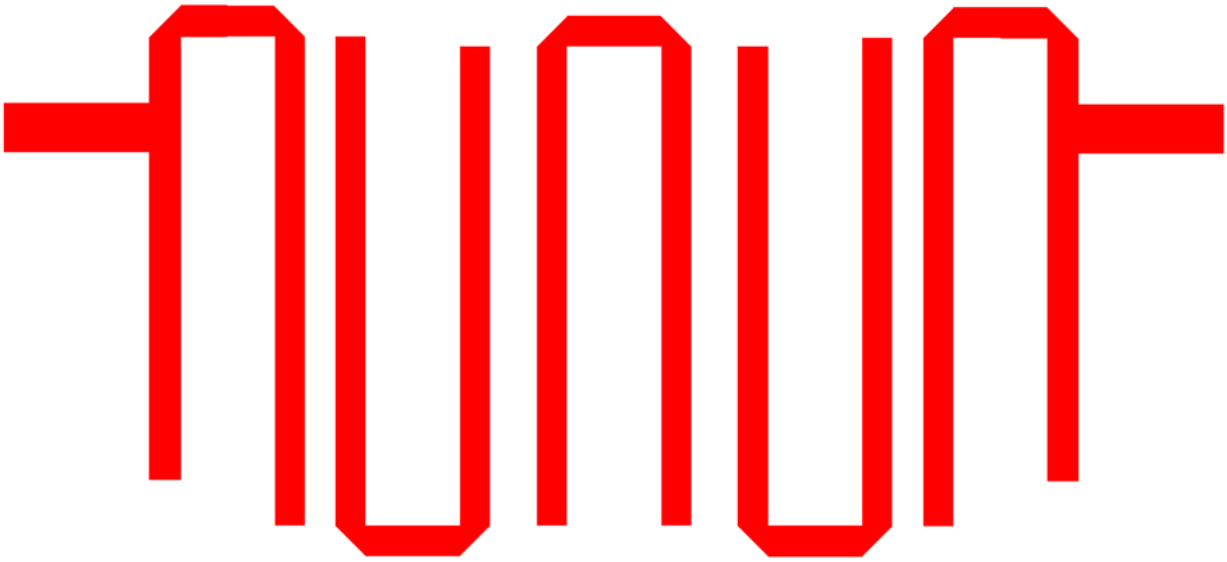


Figure A-22 - 6010.2LM Hairpin Genesys Layout

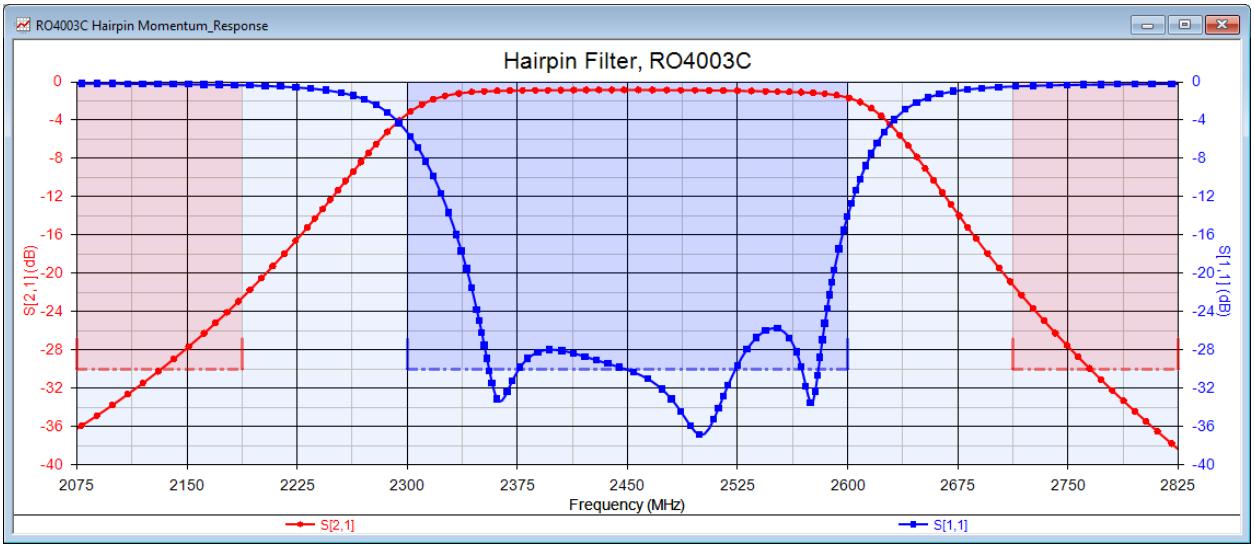


Figure A-23 - RO4003C Hairpin Genesys S_{21} and S_{11} Simulations

Figure A-24 - RO4003C Hairpin Genesys Layout

Figure A-25 - RF-60A Elliptic Genesys S_{21} and S_{11} Simulations

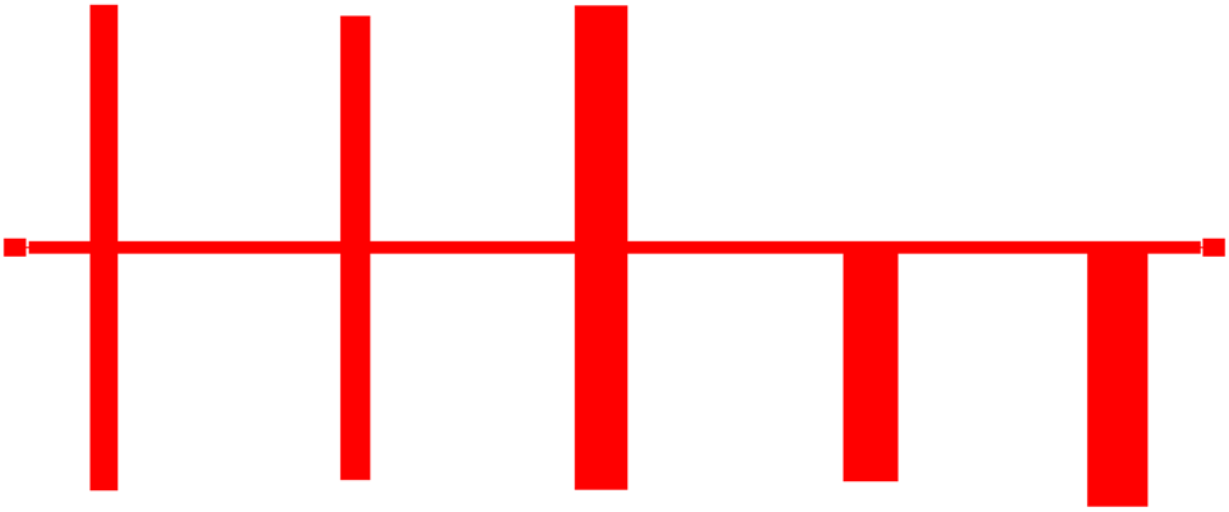


Figure A-26 - RF-60A Elliptic Genesys Layout

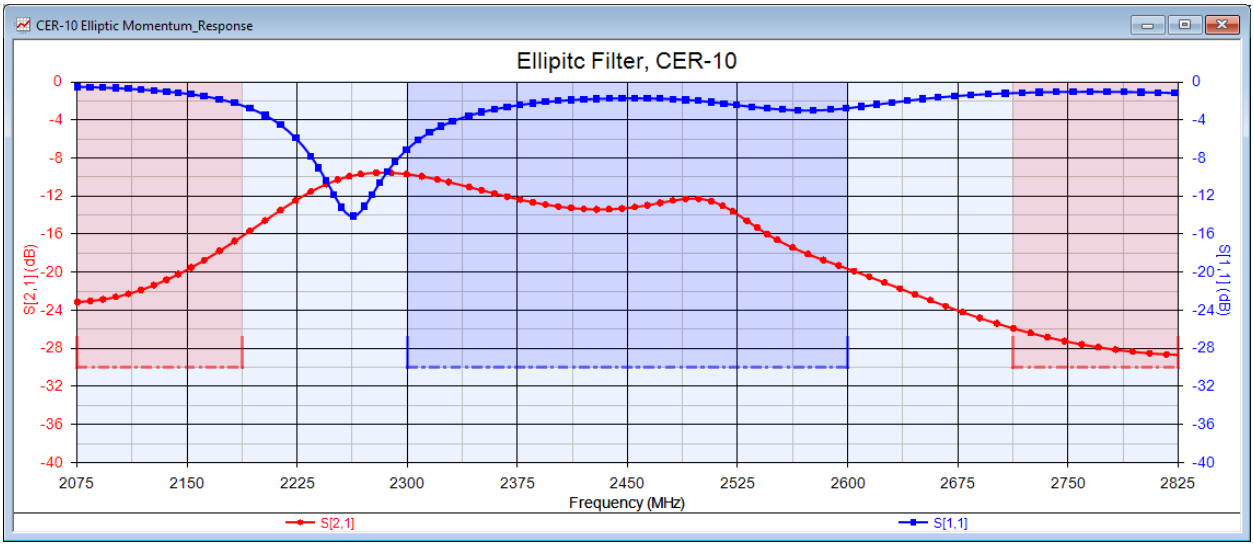


Figure A-27 - CER-10 Elliptic Genesys S_{21} and S_{11} Simulations

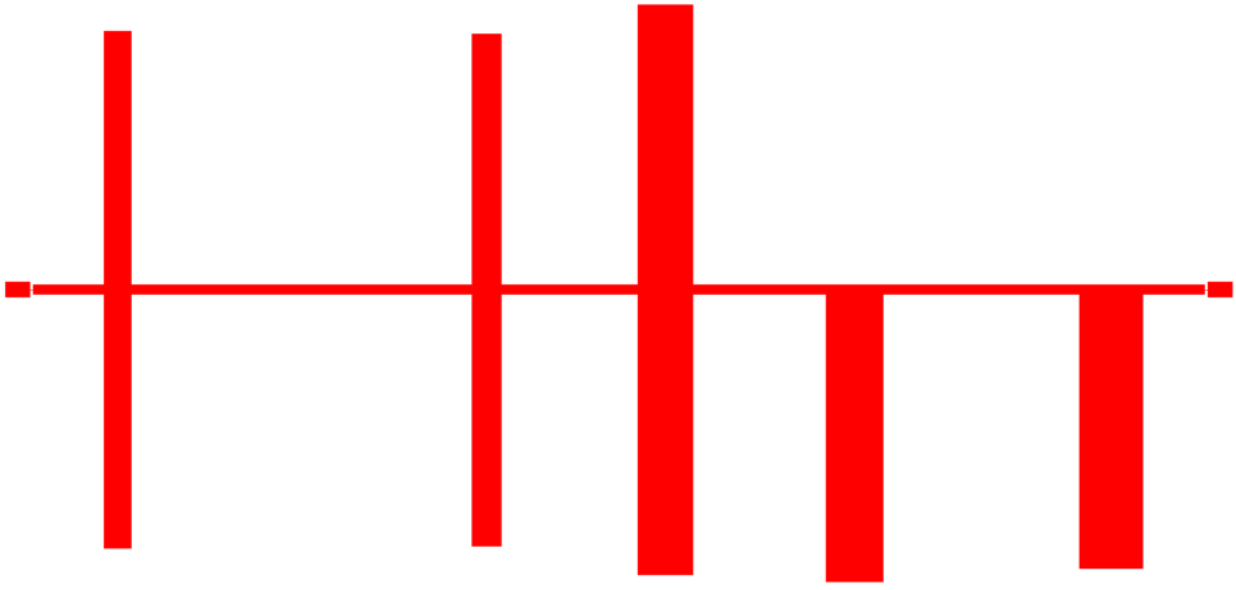


Figure A-28- CER-10 Elliptic Genesys Layout

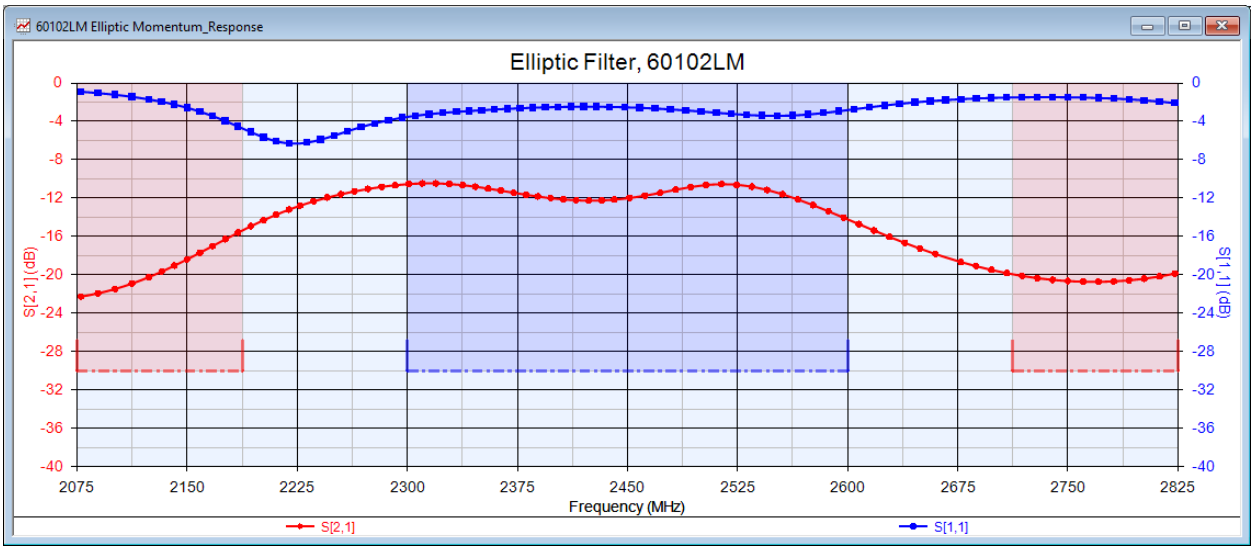


Figure A-29 - 6010.2LM Elliptic Genesys S_{21} and S_{11} Simulations

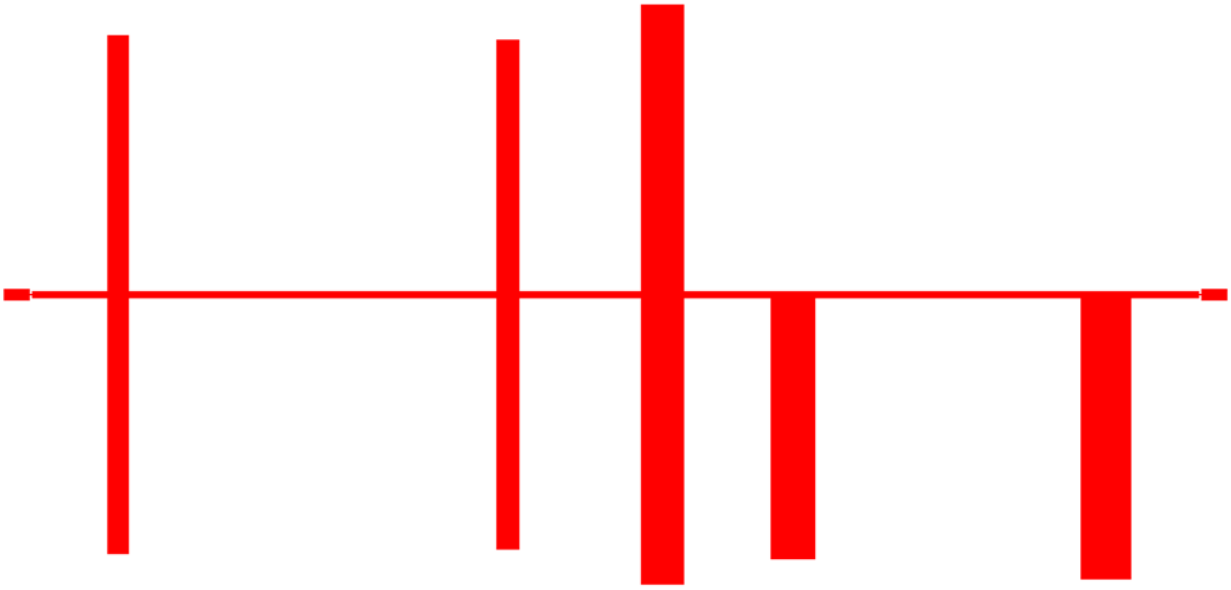


Figure A-30 - 6010.2LM Elliptic Genesys Layout

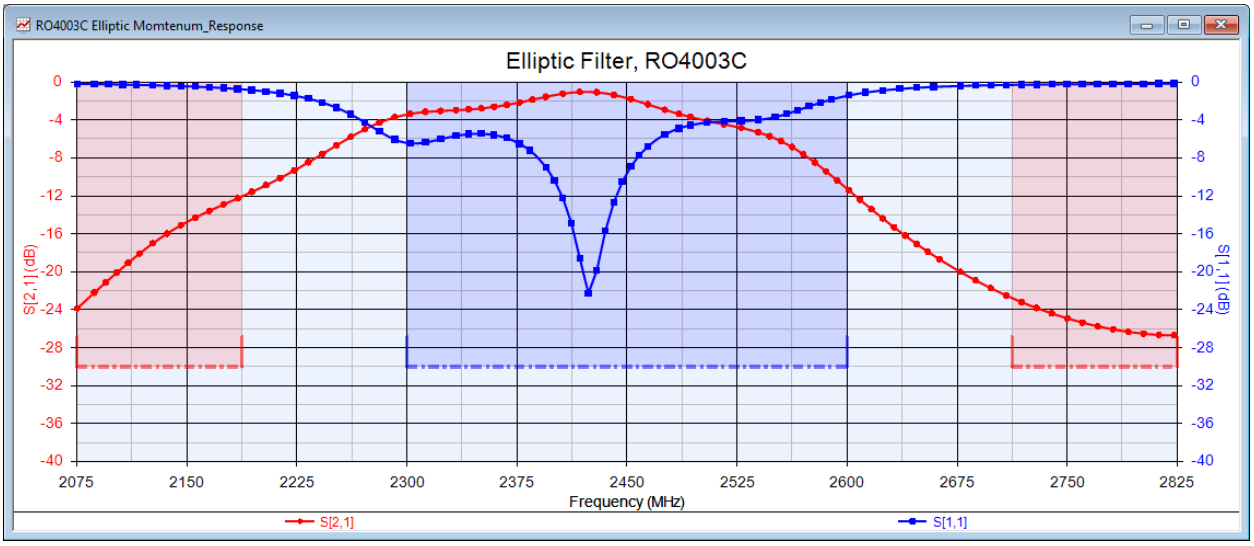


Figure A-31 - RO4003C Elliptic Genesys S_{21} and S_{11} Simulations

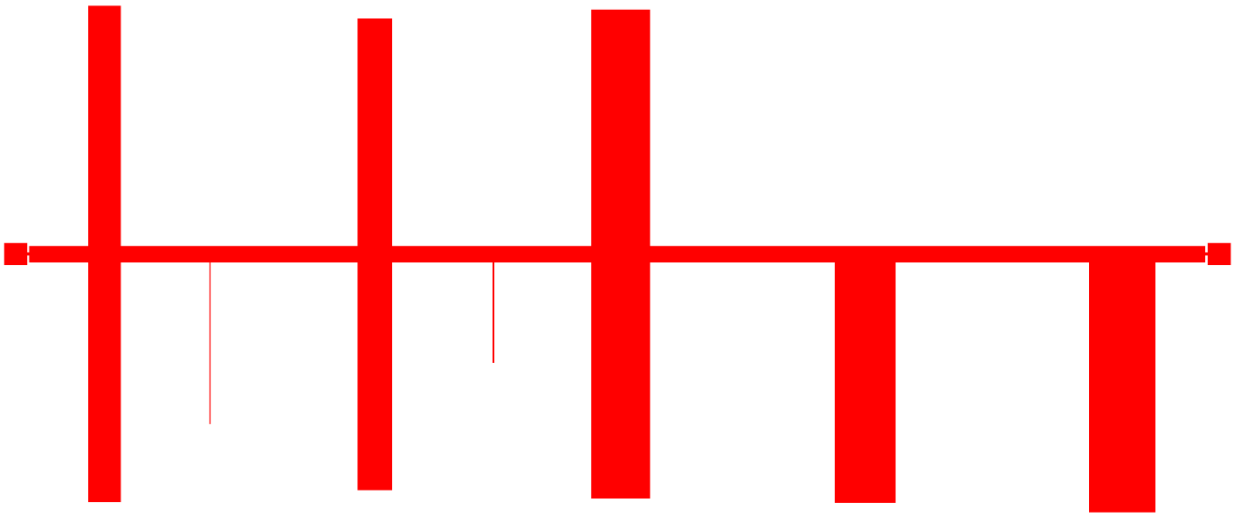


Figure A-32 - RO4003C Elliptic Genesys Layout

Appendix B – Fabricated Filter Measurements

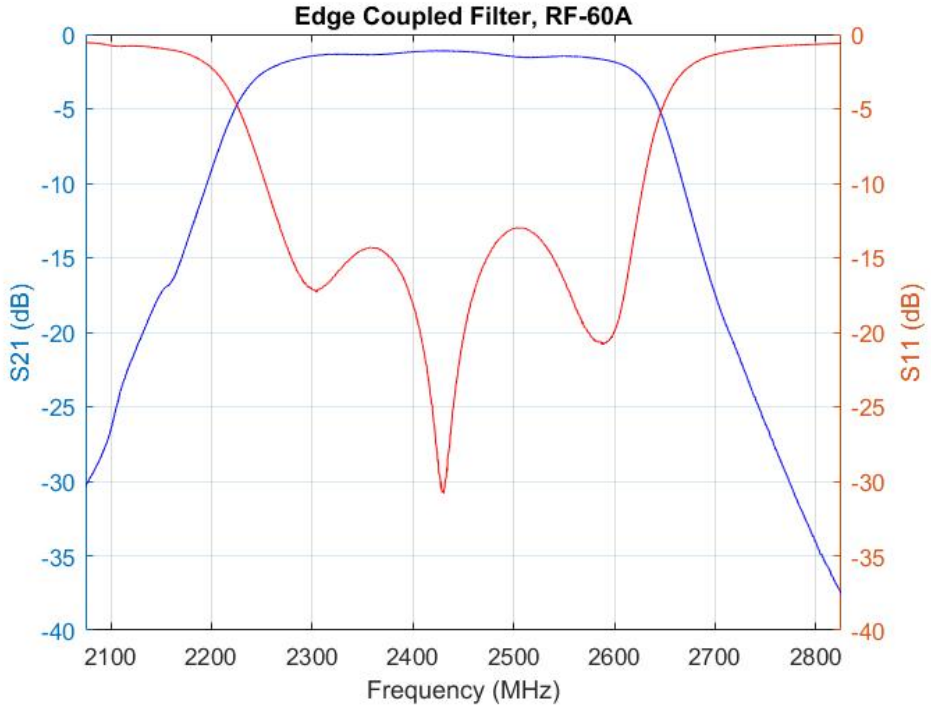


Figure B-1 - RF-60A Edge-coupled Filter Measurements

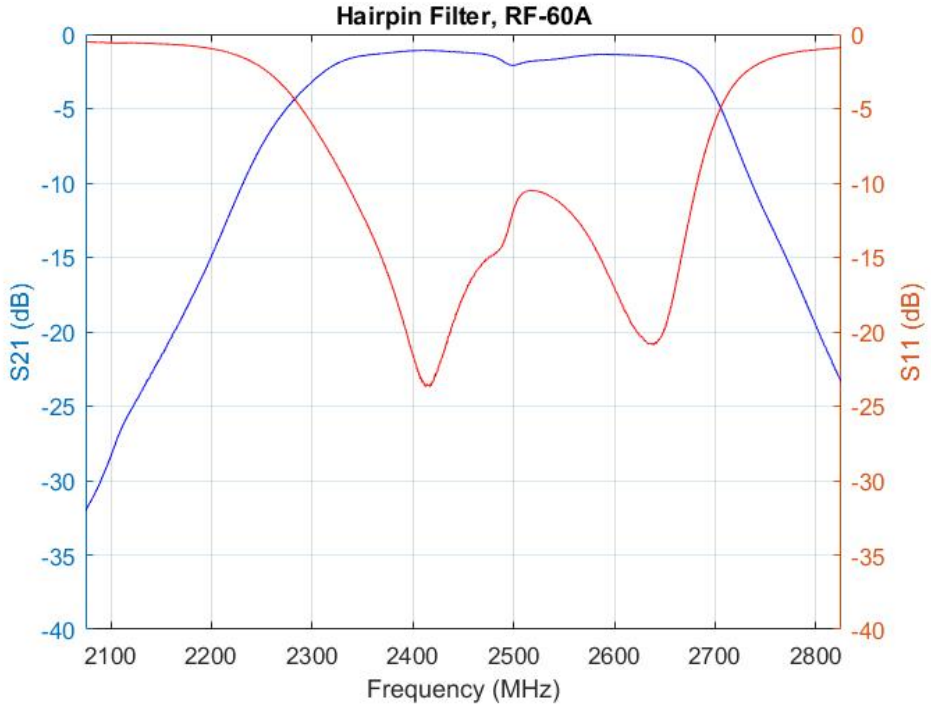


Figure B-2 - RF-60A Hairpin Filter Measurements

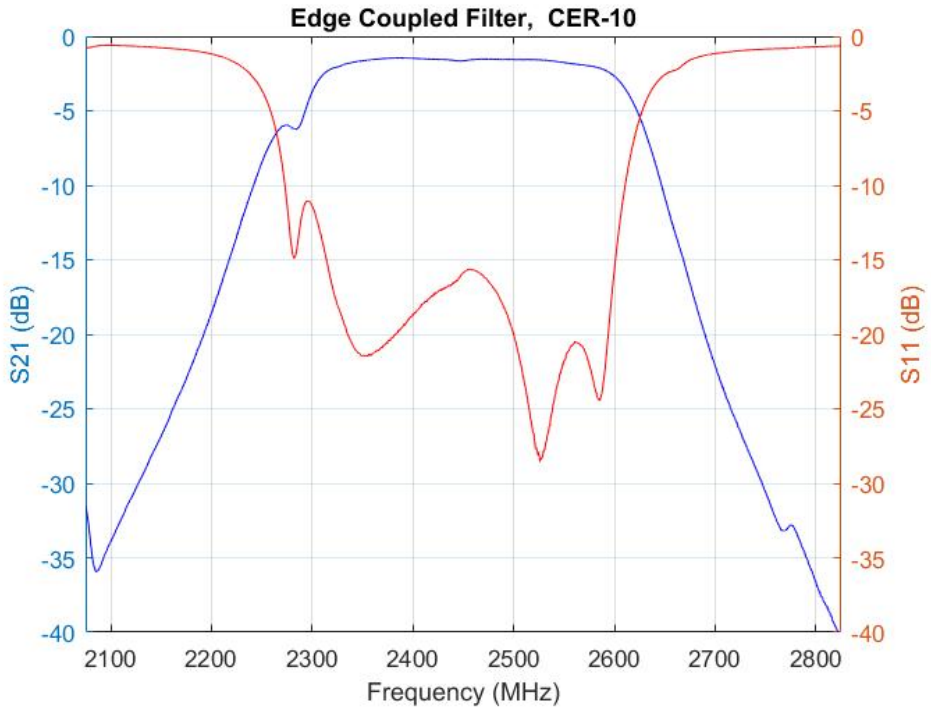


Figure B-3 - CER-10 Edge-coupled Filter Measurements

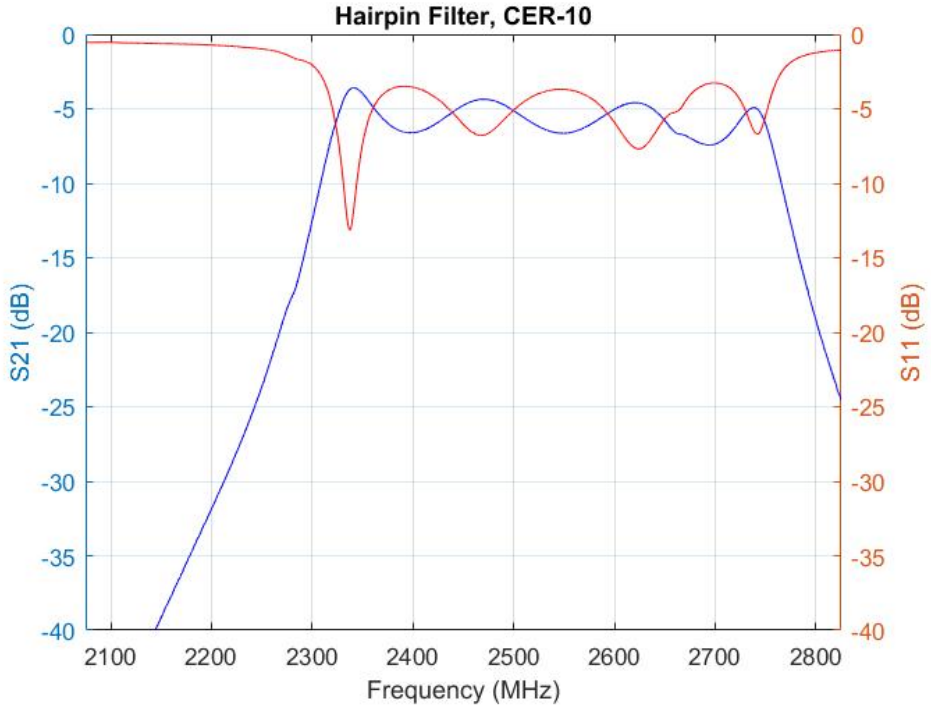


Figure B-4 - CER-10 Hairpin Filter Measurements

Figure B-5 - 6010.2LM Edge-coupled Filter Measurements

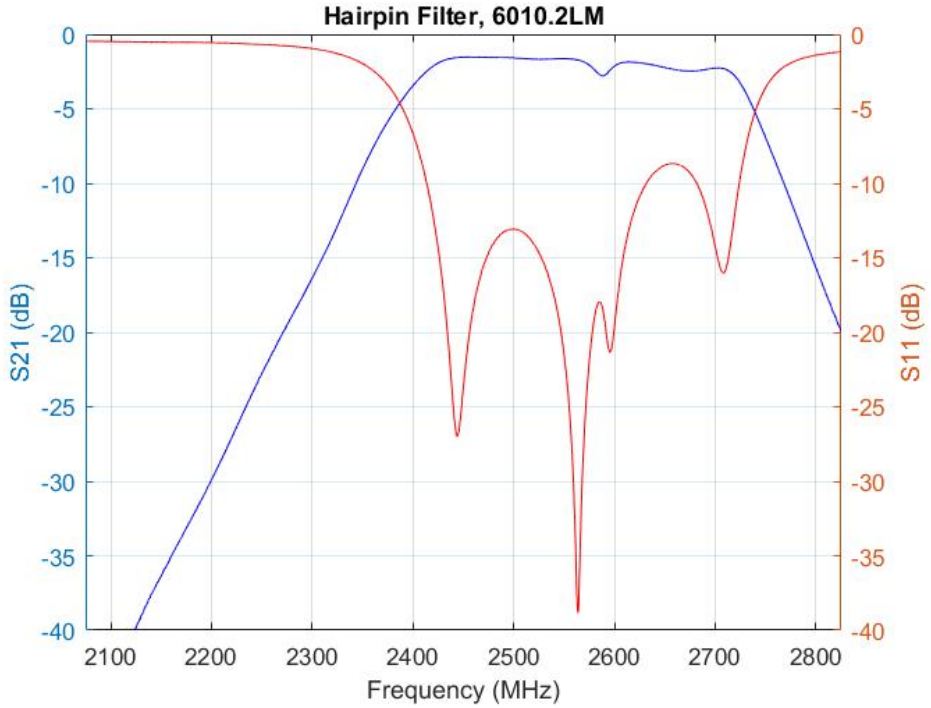


Figure B-6 - 6010.2LM Hairpin Filter Measurements

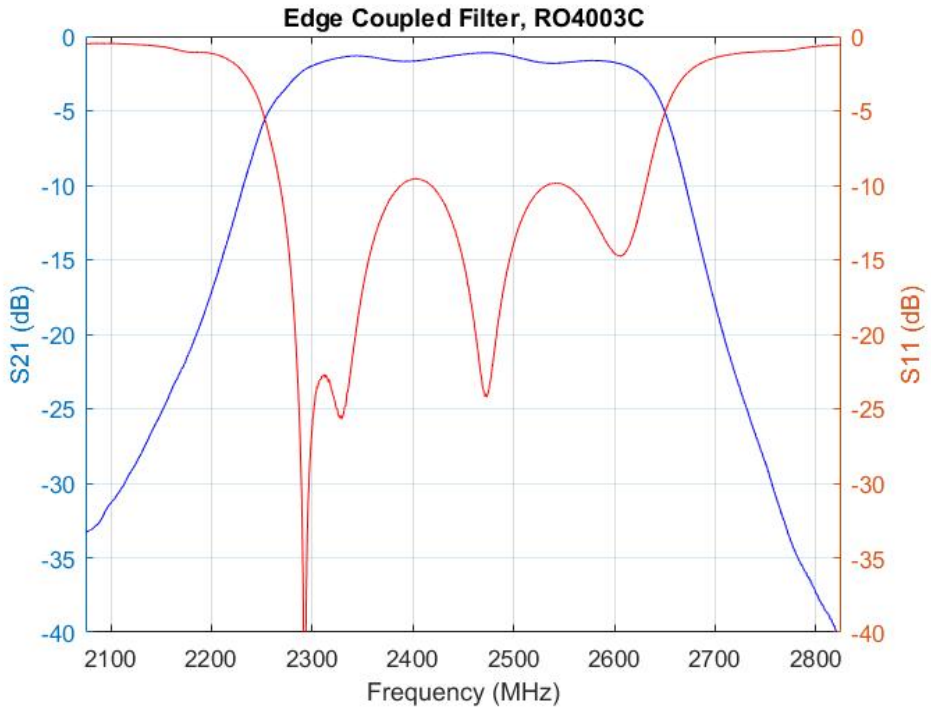


Figure B-7 - RO4003C Edge-coupled Filter Measurements

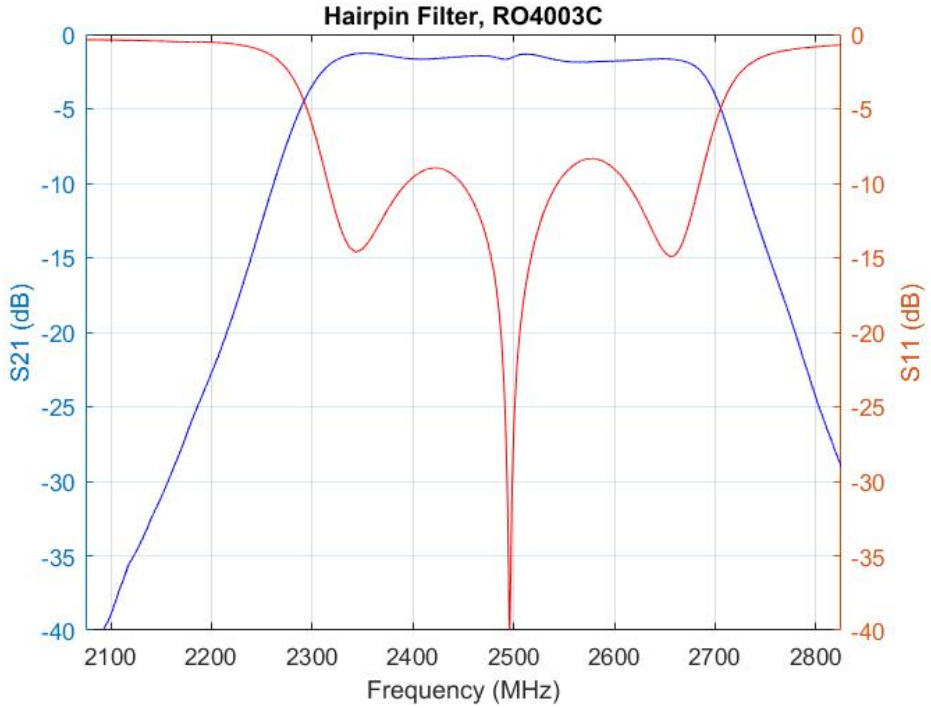
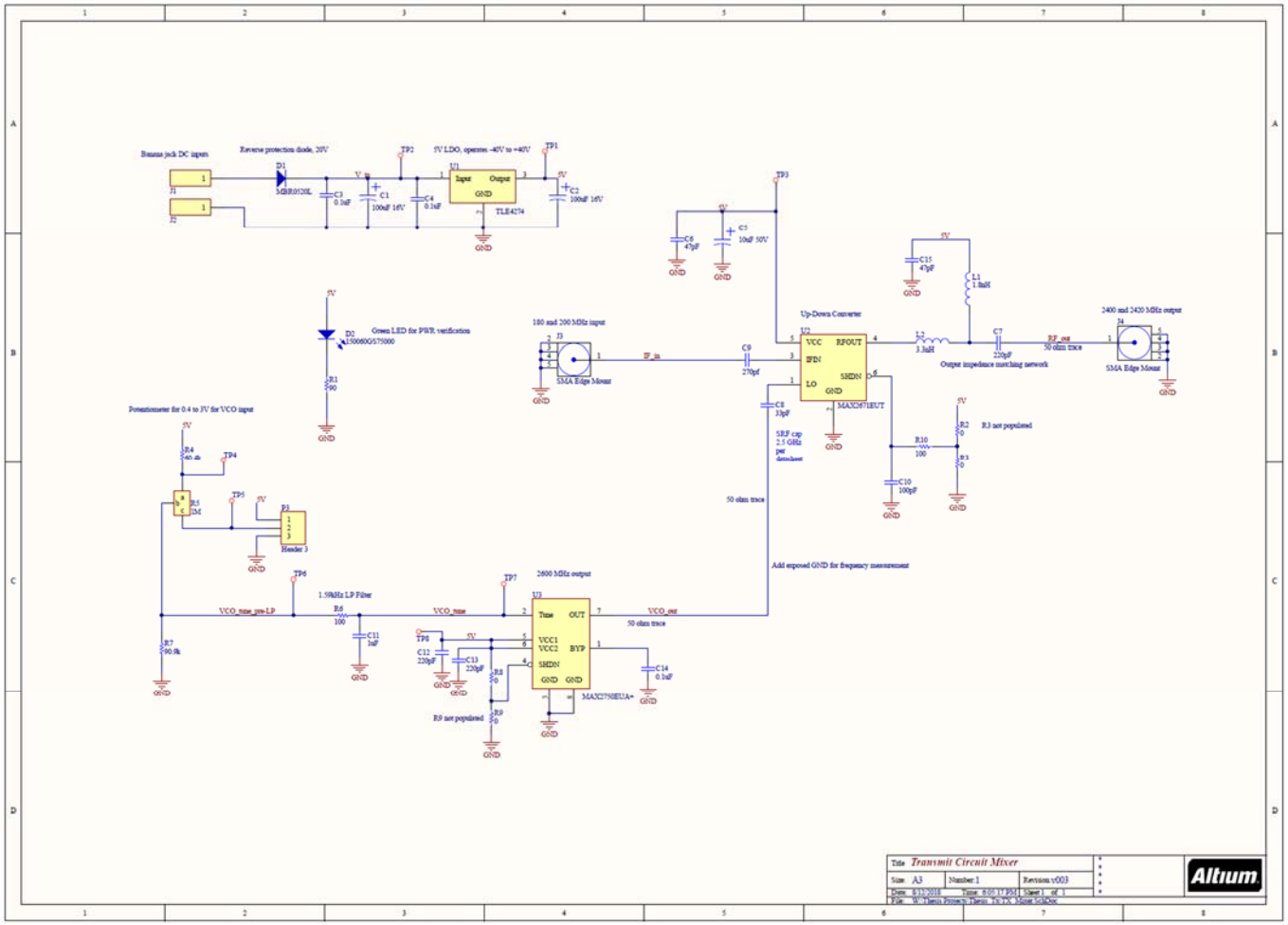
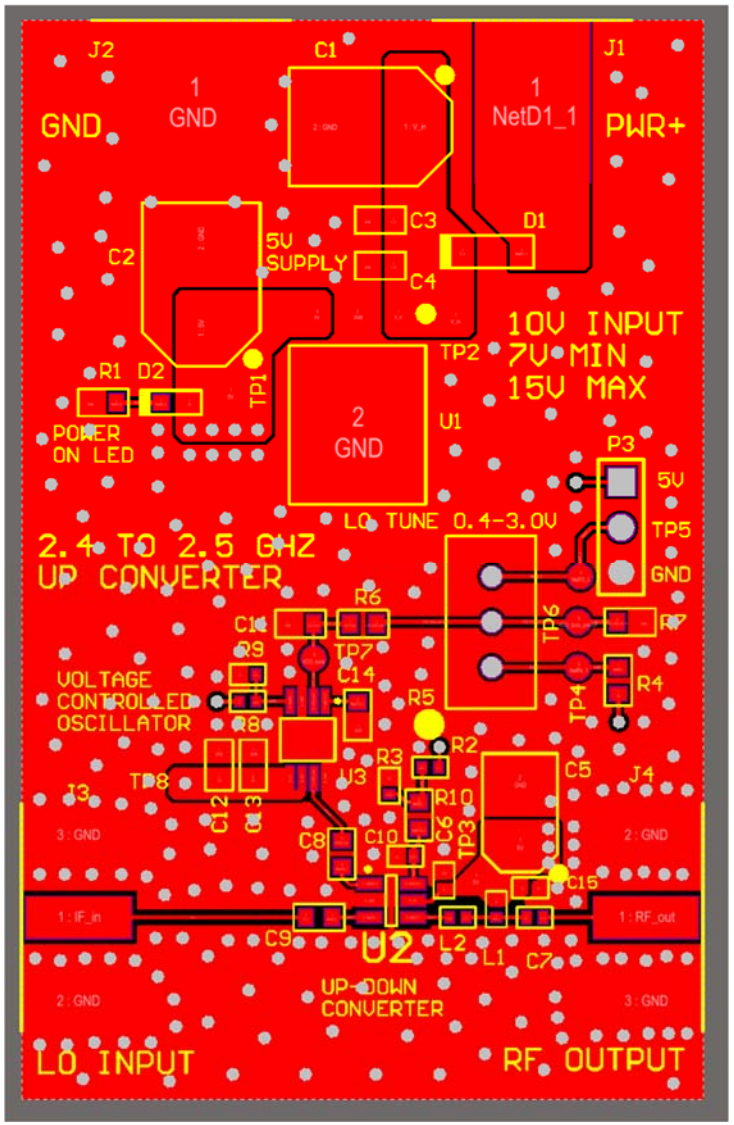


Figure B-8 - RO4003C Hairpin Filter Measurements

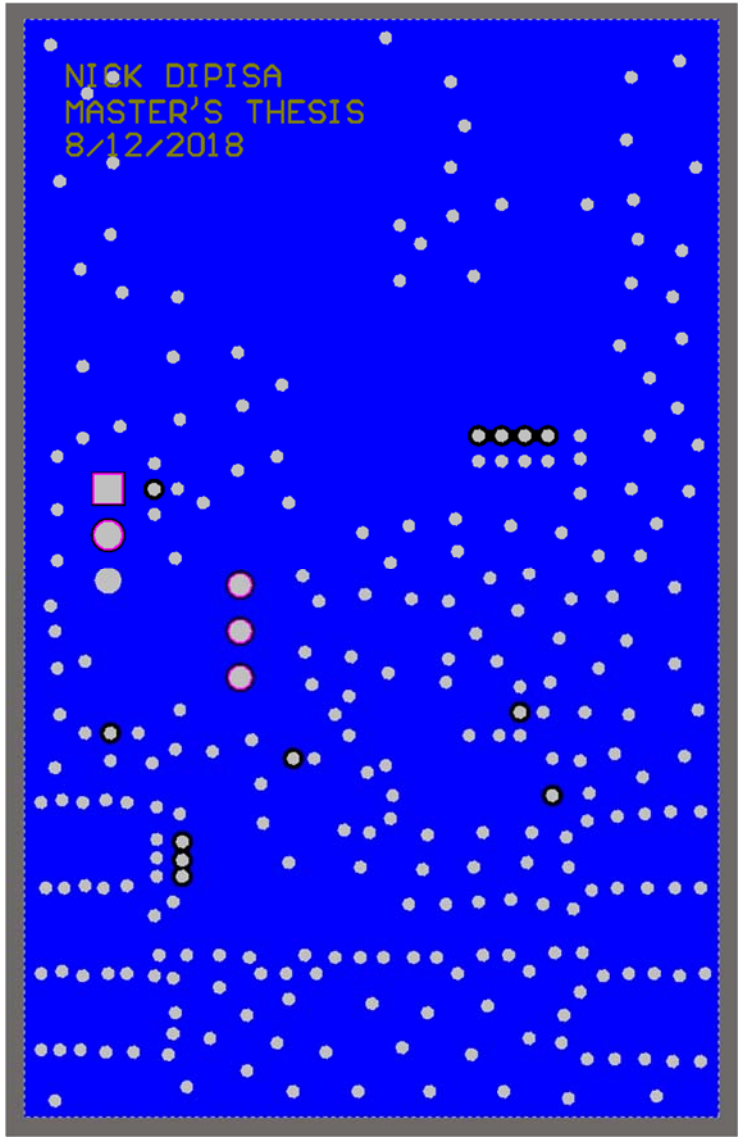
Appendix C – Schematic, Layout, and BOM Detail

C.1 – Transmit Circuit





Top Layer

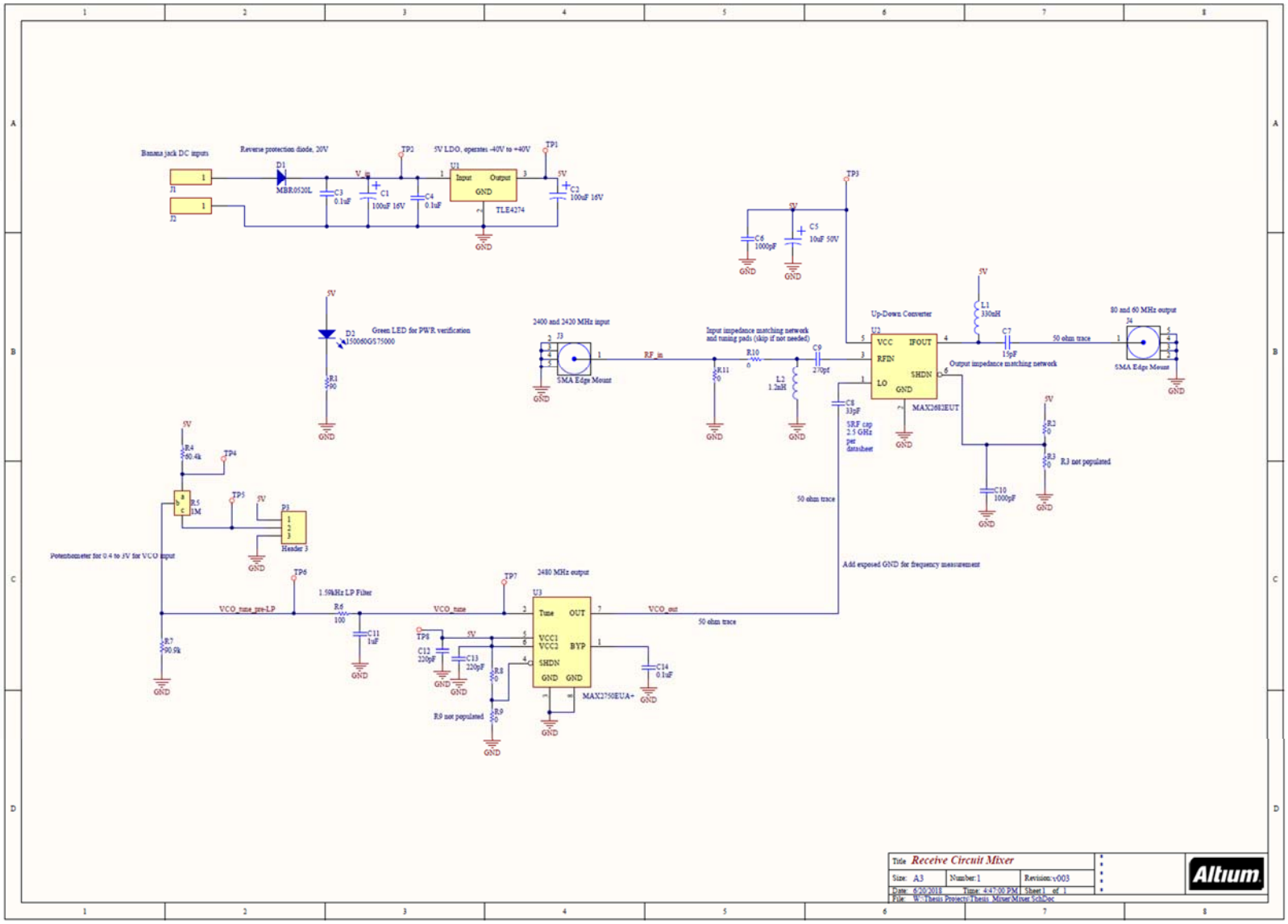


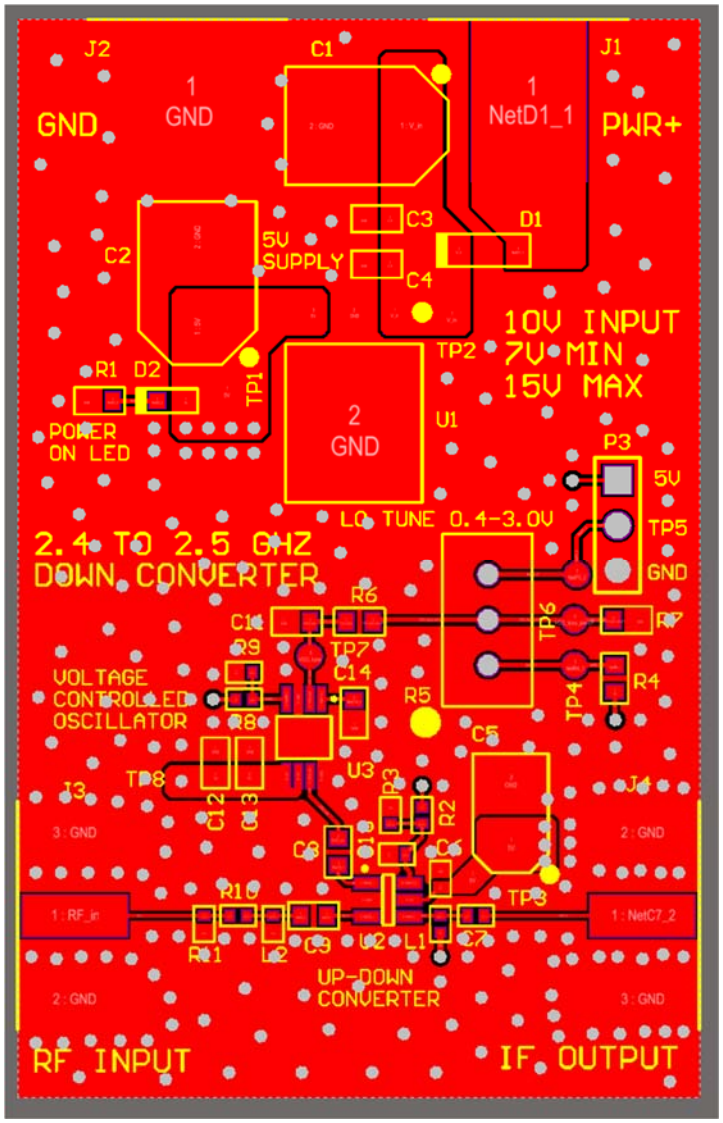
Bottom Layer

Designator	Description	Value	Manufacturer	Manufacturer P/N	Vendor	Vendor P/N	Quantity	Price
C1, C2	Aluminum Electrolytic Capacitors - SMD 16VDC 100uF 20%	100uF	Panasonic	EEE-FK1C101SR	Mouser Electronics	667-EEE-FK1C101SR	2	$ 0.42
C3, C4, C14	Multilayer Ceramic Capacitors MLCC - SMD/SMT RECOMN	0.1uF	Murata Electronics	GRM188R61C104KA01D	Mouser Electronics	81-GRM188R61C104KA1D	3	$ 0.10
C5	Aluminum Electrolytic Capacitors - SMD 50VDC 10uF 20%	10uF	Panasonic	EEE-FK1H100SR	Mouser Electronics	667-EEE-FK1H100SR	1	$ 0.43
C6, C15	Multilayer Ceramic Capacitors MLCC - SMD/SMT 0402 47p	47pF	Vishay/Vitramon	VJ0402A470JXXCW1BC	Mouser Electronics	77-VJ0402A470JXXCBC	2	$ 0.10
C7	Multilayer Ceramic Capacitors MLCC - SMD/SMT WCAP-C	220pF	Wurth Electronics	885012205040	Mouser Electronics	710-885012205040	1	$ 0.10
C8	0603 Ceramic Chip Capacitor - Standard	33pF	American Technical Ceramics (ATC)	600S330JT250XT	Mouser Electronics	581-600S330JT	1	$ 1.09
C9	0603 Ceramic Chip Capacitor - Standard	270pf	Vishay/Vitramon	VJ0603D271KXAAJ	Mouser Electronics	77-VJ0603D271KXAAJ	1	$ 0.16
C10	Multilayer Ceramic Capacitors MLCC - SMD/SMT 0402 100	100pF	Vishay/Vitramon	VJ0402A101JXJCW1BC	Mouser Electronics	77-VJ0402A101JXJCBC	1	$ 0.10
C11	Multilayer Ceramic Capacitors MLCC - SMD/SMT 0603 10V	1uF	TDK	C1608X5R1A105M080AC	Mouser Electronics	810-C1608X5R1A105M	1	$ 0.28
C12, C13	Multilayer Ceramic Capacitors MLCC - SMD/SMT 16volts 2	220pF	KEMET	C0603C221M4RACTU	Mouser Electronics	80-C0603C221M4R	2	$ 0.24
D1	Schottky Diodes & Rectifiers Schottky Power Rect .5a		ON Semiconductor/Fairchild	MBR0520L	Mouser Electronics	512-MBR0520L	1	$ 0.37
D2	Standard LEDs - SMD WL-SMCW SMDMono TpVw Waterc		Wurth Electronics	150060GS75000	Mouser Electronics	710-150060GS75000	1	$ 0.14
J1, J2	Test Plugs & Test Jacks BANANA JACK RED, Test Plugs &		Johnson/Cinich Connectivity Solutions	108-0902-001, 108-0903-001	Mouser Electronics	530-108-0902-1, 530-108-0903-1	2	$ 0.65
J3, J4	CONN SMA RCPT STR 50OHM EDGE MNT		Molex	0732511150	Digi-Key Corp.	WM5534-ND	2	$ 3.33
L1	Fixed Inductors 0402 1.8nH 0.2nH 900mA 0.08ohms 6GHz	1.8nH	Murata Electronics	LQG15HN1N8C02D	Mouser Electronics	81-LQG15HN1N8C02D	1	$ 0.10
L2	Fixed Inductors 0402 3.3nH 0.3nH 900mA 0.08ohms6.0GH	3.3nH	Murata Electronics	LQG15WZ3N3S02D	Mouser Electronics	81-LQG15WZ3N3S02D	1	$ 0.15
P3	SIL VERTICAL PC TAIL PIN HEADER		Harwin Inc.	M20-9990345	Digi-Key Corp.	952-2263-ND	1	$ 0.18
R1	Thick Film Resistors - SMD 1/10Watt 100ohms 1% Comme	90	Vishay	CRCW0603100RFKEAC	Mouser Electronics	71-CRCW0603100RFKEAC	1	$ 0.10
R2, R3, R8, R9	0402 Chip Resistor - Standard	0					N/A	$ -
R4	Thick Film Resistors - SMD 1/10W 60.4Kohms 1% Comme	60.4k	Vishay	CRCW060360K4FKEAC	Mouser Electronics	71-CRCW060360K4FKEAC	1	$ 0.10
R5	Trimmer Resistors - Through Hole 1Mohms 10%		Vishay/Sfernice	T93YB105KT20	Mouser Electronics	72-T93YB-1M	1	$ 1.22
R6, R10	Thick Film Resistors - SMD 1/10Watt 100ohms 1% Comme	100	Vishay	CRCW0603100RFKEAC	Mouser Electronics	71-CRCW0603100RFKEAC	2	$ 0.10
R7	Thick Film Resistors - SMD 1/10W 90.9Kohms 1% Comme	90.9k	Vishay	CRCW060390K9FKEAC	Mouser Electronics	71-CRCW060390K9FKEAC	1	$ 0.10
U1	5V 400mA LDO		Infineon Technologies	TLE4274-2D V50	Mouser Electronics	726-TLE42742DV50	1	$ 1.82
U2	Up-Down Converters 400MHz to 2.5GHz Upconverter		Maxium Integrated	MAX2671EUT+T	Mouser Electronics	700-MAX2671EUTT	1	$ 1.81
U3	VCO Oscillators 2.4-2.5GHz Mono V-Controlled Osc		Maxim Integrated	MAX2750EUA+	Mouser Electronics	700-MAX2750EUA	1	$ 6.05

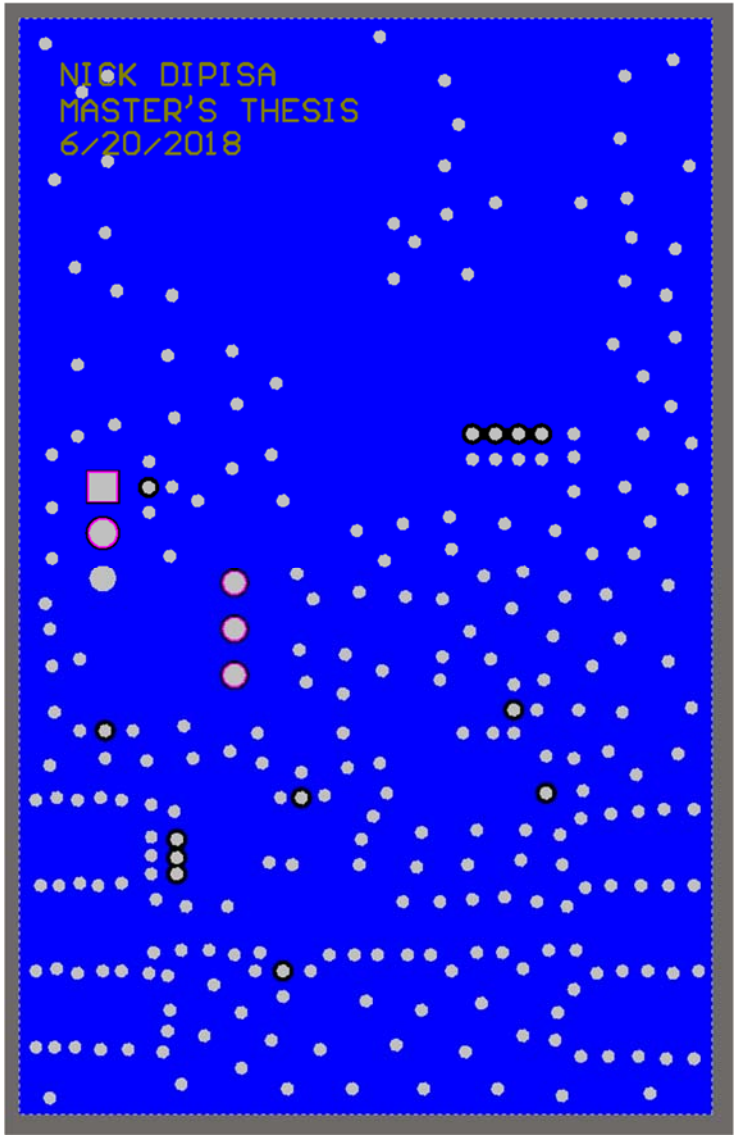
Transmit Circuit	
Total BOM Cost	$24.28
PCB Cost 4-layer 2.375” by 1.500” 0.062” thick FR-4 substrate	$71.00
Total Cost	**$95.28**

C.2 – Receive Circuit





Top Layer

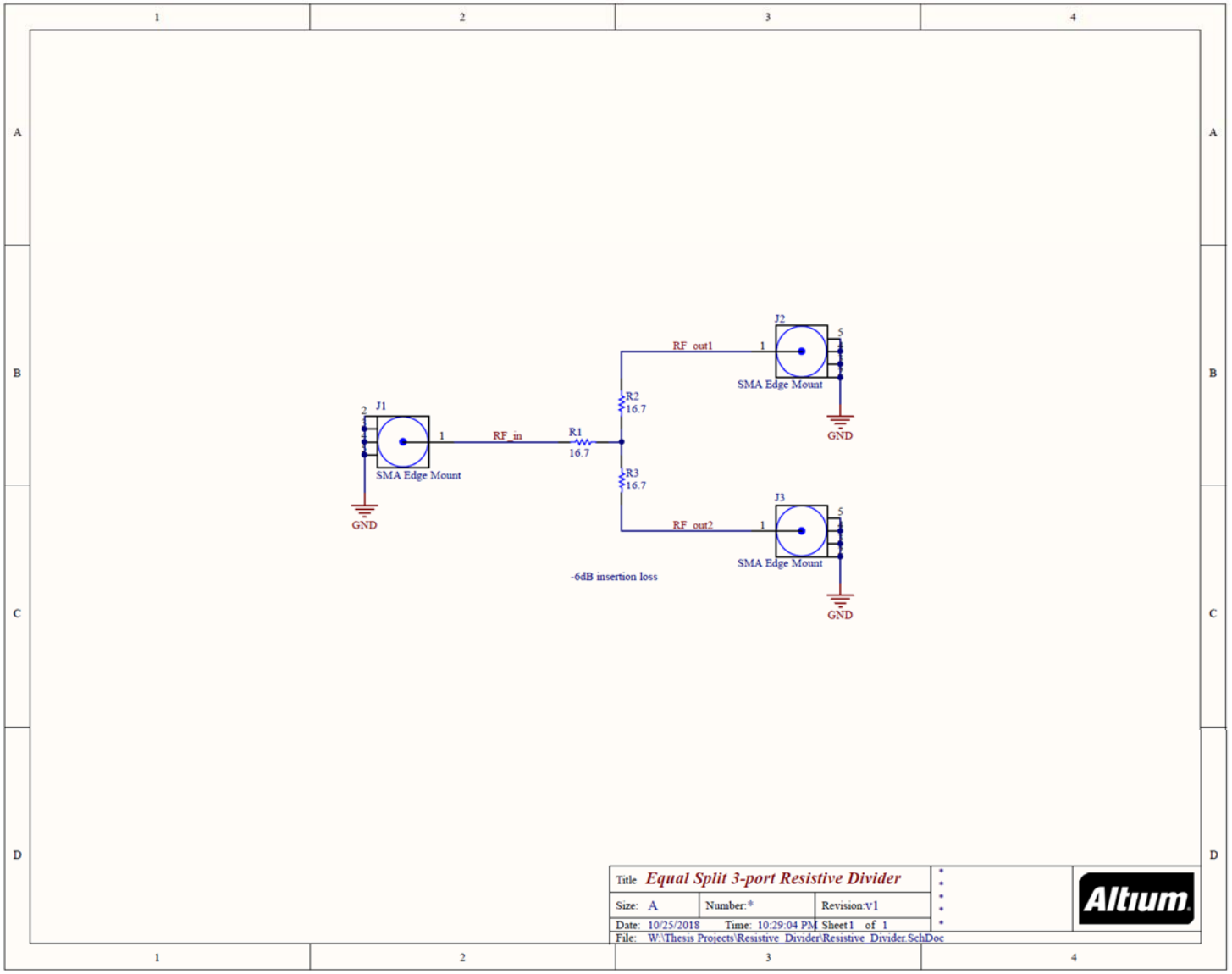


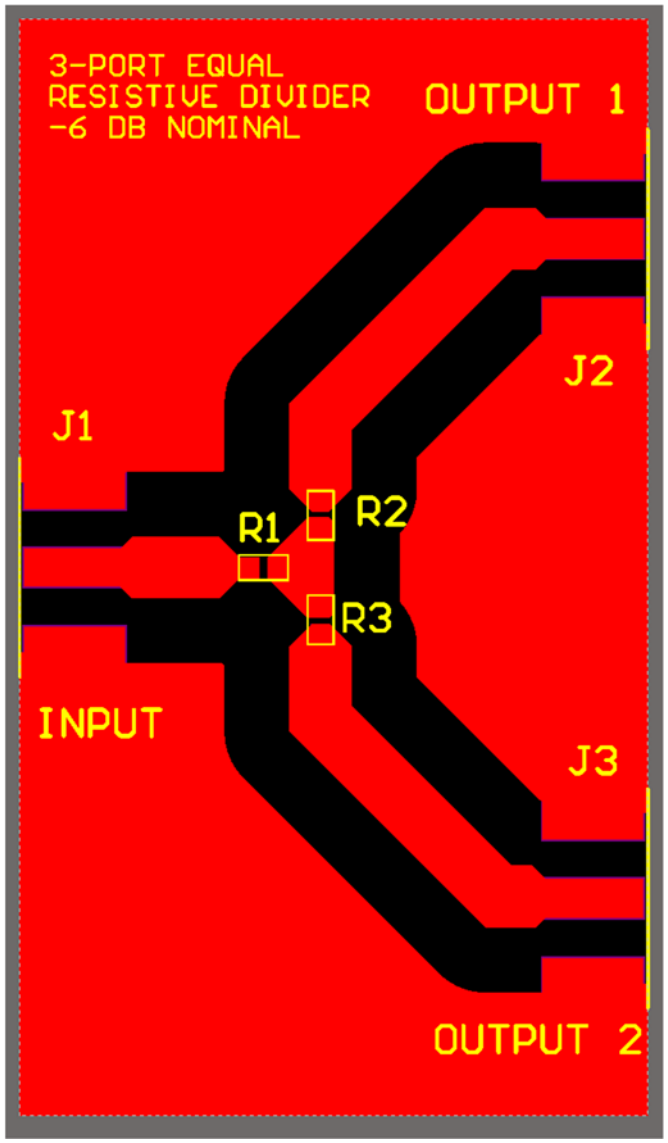
Bottom Layer

Designator	Description	Value	Manufacturer	Manufacturer P/N	Vendor	Vendor P/N	Quantity	Price
C1, C2	Aluminum Electrolytic Capacitors - SMD 16VDC 100uF 20%		Panasonic	EEE-FK1C101SR	Mouser Electronics	667-EEE-FK1C101SR	2	$ 0.42
C3, C4, C14	Multilayer Ceramic Capacitors MLCC - SMD/SMT RECOMM	0.1uF	Murata Electronics	GRM188R61C104KA01D	Mouser Electronics	81-GRM188R61C104KA1D	3	$ 0.10
C5	Aluminum Electrolytic Capacitors - SMD 50VDC 10uF 20%		Panasonic	EEE-FK1H100SR	Mouser Electronics	667-EEE-FK1H100SR	1	$ 0.43
C6, C10	Multilayer Ceramic Capacitors MLCC - SMD/SMT 0402 100	1000pF	Vishay/Vitramon	VJ0402Y102KXJCW1BC	Mouser Electronics	77-VJ0402Y102KXJCBC	2	$ 0.10
C7	0402 Ceramic Chip Capacitor - Standard	15pF	Murata Electronics	GJM1555C1H150FB01D	Mouser Electronics	81-GJM1555C1H150FB1D	1	$ 0.24
C8	0603 Ceramic Chip Capacitor - Standard	33pF	American Technical Ceramics (ATC)	600S330JT250XT	Mouser Electronics	581-600S330JT	1	$ 1.09
C9	0603 Ceramic Chip Capacitor - Standard	270pf	Vishay/Vitramon	VJ0603D271KXAAJ	Mouser Electronics	77-VJ0603D271KXAAJ	1	$ 0.16
C11	Multilayer Ceramic Capacitors MLCC - SMD/SMT 0603 10V	1uF	TDK	C1608X5R1A105M080AC	Mouser Electronics	810-C1608X5R1A105M	1	$ 0.28
C12, C13	Multilayer Ceramic Capacitors MLCC - SMD/SMT 16volts 2	220pF	KEMET	C0603C221M4RACTU	Mouser Electronics	80-C0603C221M4R	2	$ 0.24
D1	Schottky Diodes & Rectifiers Schottky Power Rect .5a		ON Semiconductor/Fairchild	MBR0520L	Mouser Electronics	512-MBR0520L	1	$ 0.37
D2	Standard LEDs - SMD WL-SMCW SMDMono TpVw Waterc		Wurth Electronics	150060GS75000	Mouser Electronics	710-150060GS75000	1	$ 0.14
J1, J2	Test Plugs & Test Jacks BANANA JACK RED, Test Plugs &		Johnson/Cinich Connectivity Solutions	108-0902-001, 108-0903-001	Mouser Electronics	530-108-0902-1, 530-108-0903-1	2	$ 0.65
J3, J4	CONN SMA RCPT STR 50OHM EDGE MNT		Molex	0732511150	Digi-Key Corp.	WM5534-ND	2	$ 3.33
L1	0402 Chip Inductor - Standard	330nH	Murata Electronics	LQB15NNR33M10D	Mouser Electronics	81-LQB15NNR33M10D	1	$ 0.11
L2	0402 Chip Inductor - Standard	1.2nH	TDK	MHQ1005P1N2BT000	Mouser Electronics	810-MHQ1005P1N2BT000	1	$ 0.29
P3	SIL VERTICAL PC TAIL PIN HEADER		Harwin Inc.	M20-9990345	Digi-Key Corp.	952-2263-ND	1	$ 0.18
R1	Thick Film Resistors - SMD 1/10Watt 100ohms 1% Comme	90	Vishay	CRCW0603100RFKEAC	Mouser Electronics	71-CRCW0603100RFKEAC	1	$ 0.10
R2, R3, R8, R9, R10, R11	0402 Chip Resistor - Standard	0					6	$ -
R4	Thick Film Resistors - SMD 1/10W 60.4Kohms 1% Comme	60.4k	Vishay	CRCW060360K4FKEAC	Mouser Electronics	71-CRCW060360K4FKEAC	1	$ 0.10
R5	Trimmer Resistors - Through Hole 1Mohms 10%		Vishay/Sfernice	T93YB105KT20	Mouser Electronics	72-T93YB-1M	1	$ 1.22
R6	Thick Film Resistors - SMD 1/10Watt 100ohms 1% Comme	100	Vishay	CRCW0603100RFKEAC	Mouser Electronics	71-CRCW0603100RFKEAC	1	$ 0.10
R7	Thick Film Resistors - SMD 1/10W 90.9Kohms 1% Comme	90.9k	Vishay	CRCW060390K9FKEAC	Mouser Electronics	71-CRCW060390K9FKEAC	1	$ 0.10
U1	5V 400mA LDO		Infineon Technologies	TLE4274-2D V50	Mouser Electronics	726-TLE42742DV50	1	$ 1.82
U2	Up-Down Converters 400MHz to 2.5GHz Upconverter		Maxium Integrated	MAX2682EUT+T	Mouser Electronics	700-MAX2682EUTT	1	$ 2.49
U3	VCO Oscillators 2.4-2.5GHz Mono V-Controlled Osc		Maxim Integrated	MAX2750EUA+	Mouser Electronics	700-MAX2750EUA	1	$ 6.05

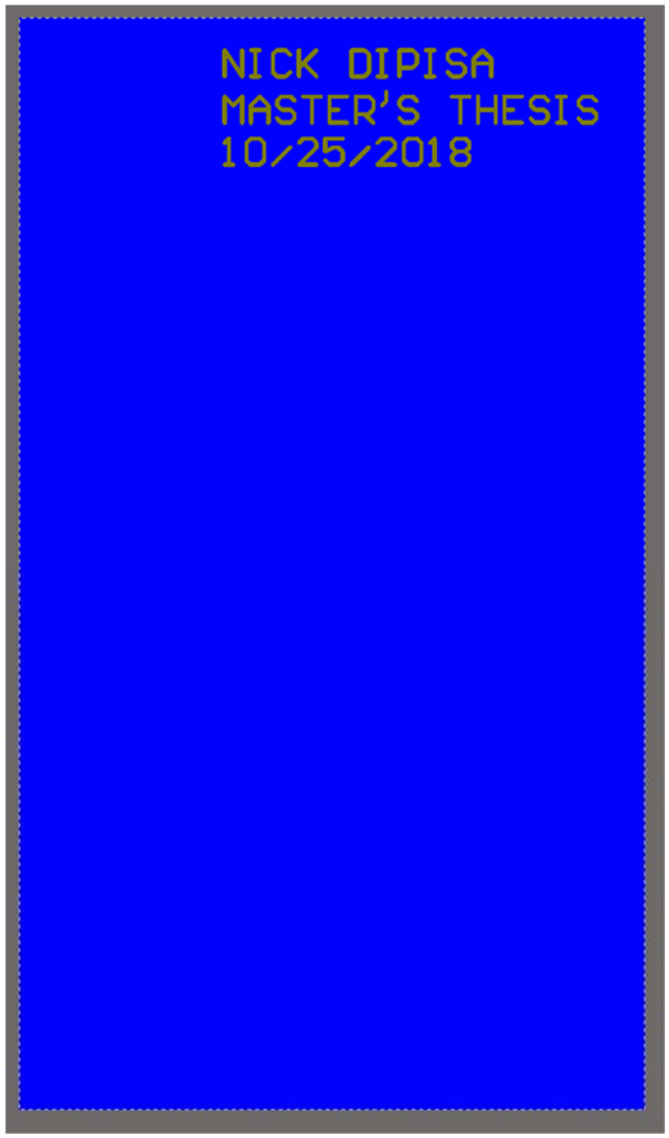
Receive Circuit	
Total BOM Cost	$25.05
PCB Cost 4-layer 2.375” by 1.500” 0.062” thick FR-4 substrate	$71.00
Total Cost	**$96.05**

C.3 – Power Divider Circuit





Top Layer

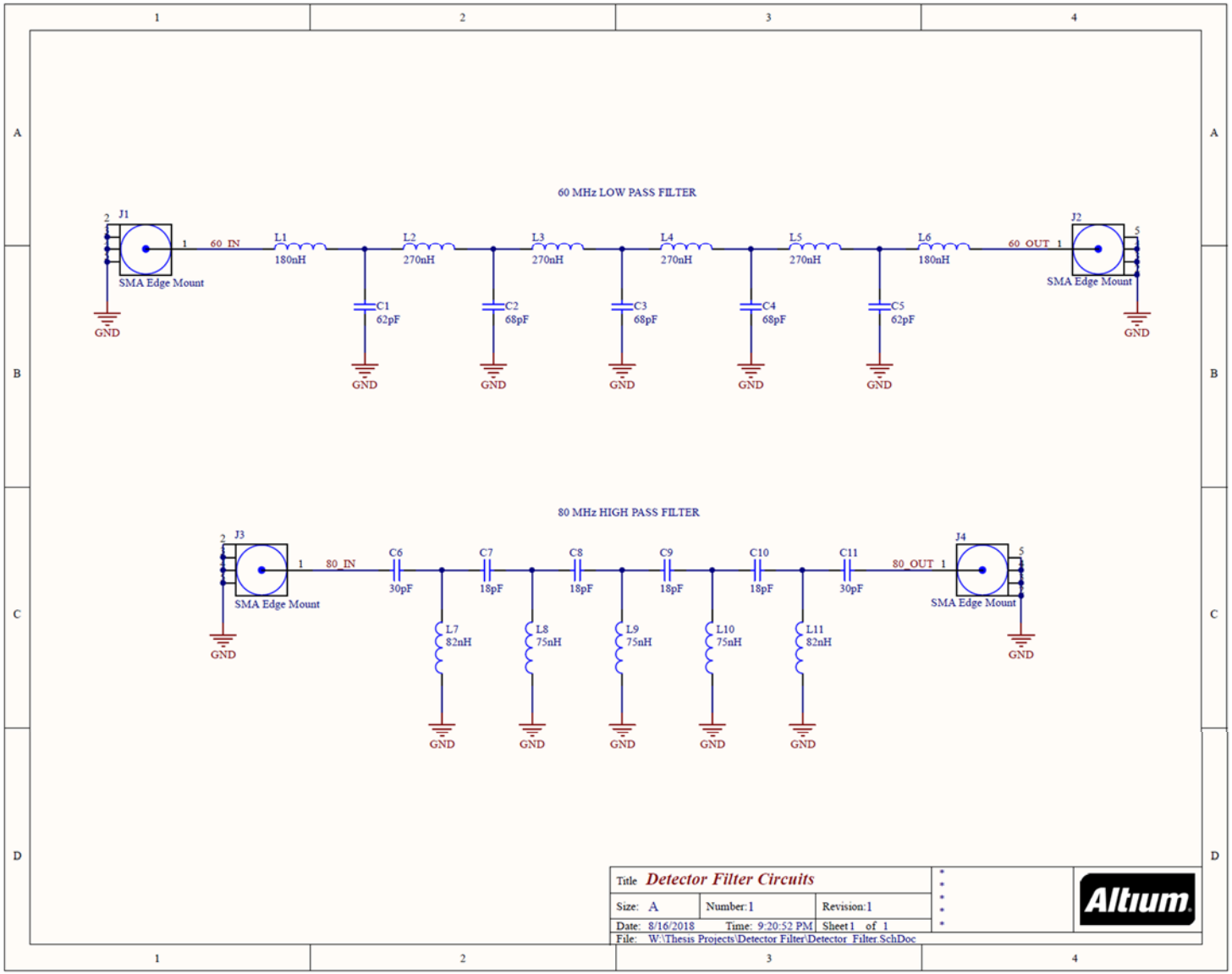


Bottom Layer

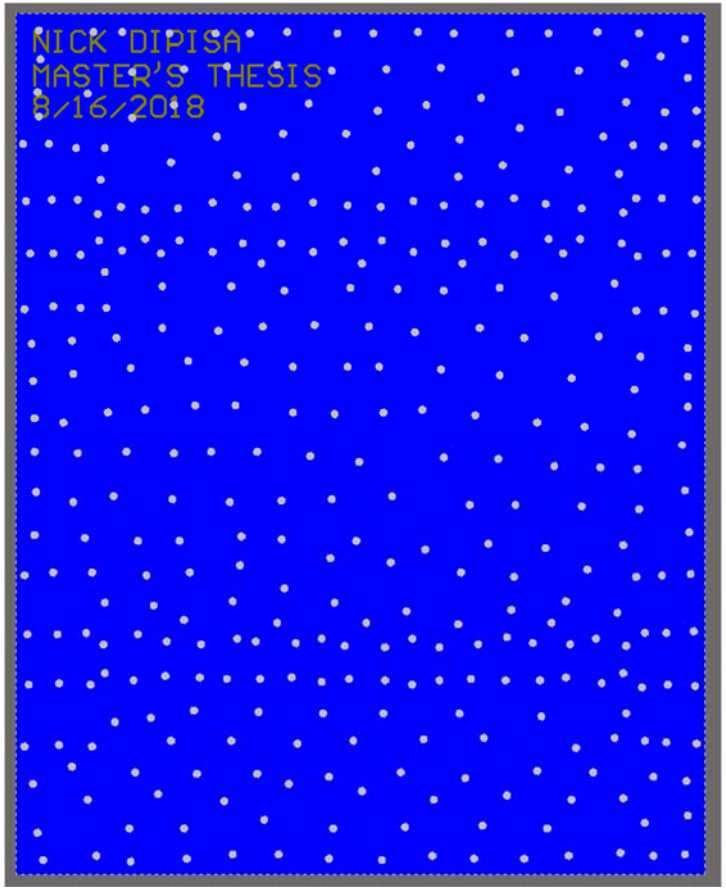
Designator	Description	Value	Manufacturer	Manufacturer P/N	Vendor	Vendor P/N	Quantity	Price
J1, J2, J3	CONN SMA RCPT STR 50OHM EDGE MNT		Molex	0732511150	Digi-Key Corp.	WM5534-ND	3	$ 3.33
R1, R2, R3	Thin Film Resistors - SMD 1/10W 16.7 Ohms 0.1%	16.7	Yageo	RT0603BRD0716R7L	Mouser Electronics	603-RT0603BRD0716R7L	3	$ 0.38

Power Divider Circuit	
Total BOM Cost	$11.13
PCB Cost 2-layer 2.500” by 1.430” 0.062” thick RO4003C substrate Fabricated at Gentex	$0.00
Total Cost	**$11.13**

C.4 – Detector Filter Circuits



Top Layer

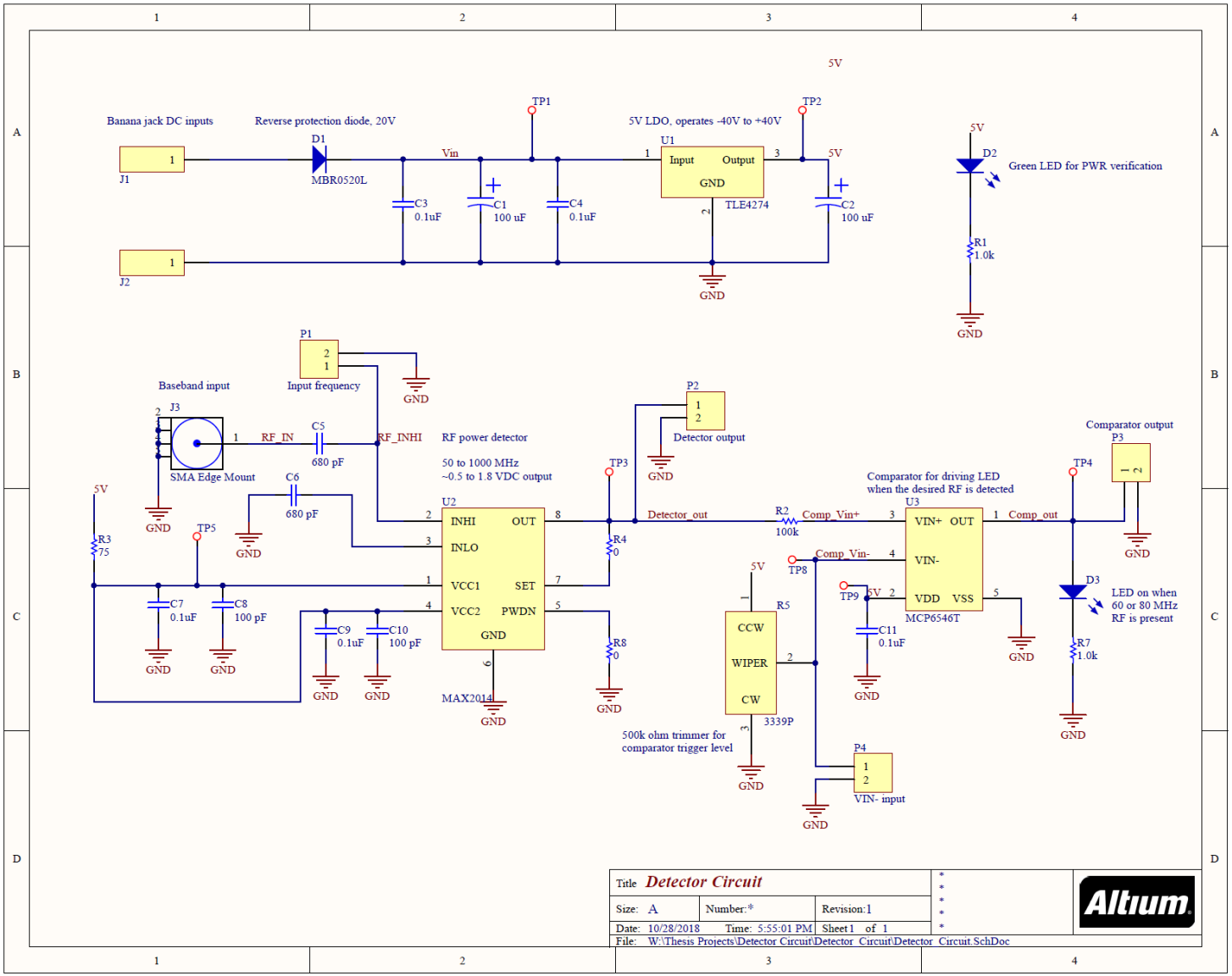


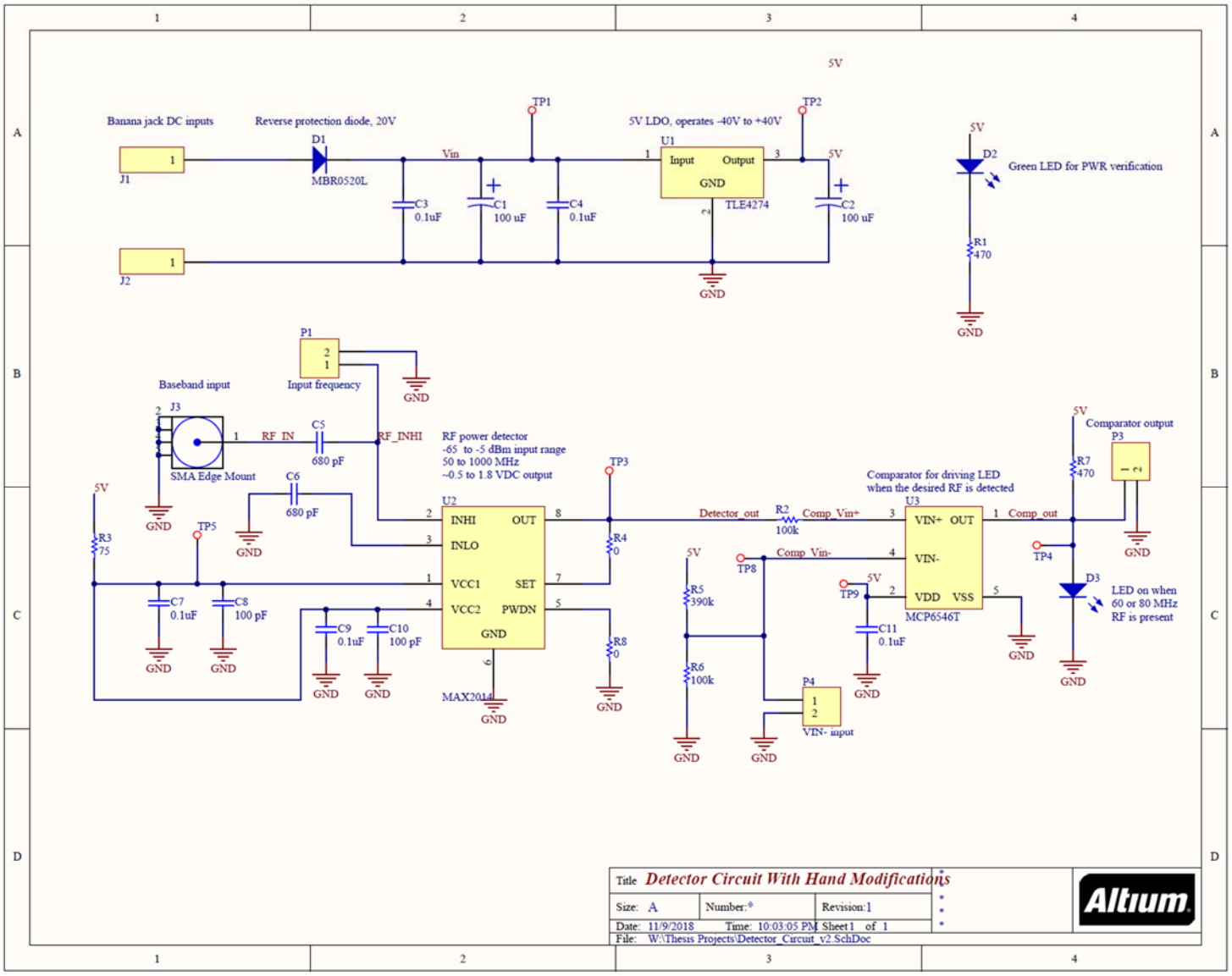
Bottom Layer

Designator	Description	Value	Manufacturer	Manufacturer P/N	Vendor	Vendor P/N	Quantity	Price
C1, C5	Multilayer Ceramic Capacitors MLCC - SMD/SMT 0402 62p	62pF	Murata Electronics	GCM1555C1H620JA16D	Mouser Electronics	81-GCM1555C1H620JA6D	2	$ 0.10
C2, C3, C4	Multilayer Ceramic Capacitors MLCC - SMD/SMT 0603 68p	68pF	Vishay/Vitramon	VJ0603A680GXAPW1BC	Mouser Electronics	77-VJ0603A680GXAPBC	3	$ 0.10
C6, C11	Multilayer Ceramic Capacitors MLCC - SMD/SMT 0603 30p	30pF	Murata Electronics	GRM1885C1H300GA01D	Mouser Electronics	81-GRM185C1H300GA01D	2	$ 0.17
C7, C8, C9, C10	Multilayer Ceramic Capacitors MLCC - SMD/SMT 50V 18pF	18pF	KEMET	C0603C180K5HACAUTO	Mouser Electronics	80-C0603C180K5HAUTO	4	$ 0.10
J1, J2, J3, J4	CONN SMA RCPT STR 50OHM EDGE MNT		Molex	0732511150	Digi-Key Corp.	WM5534-ND	4	$ 3.33
L1, L6	402 180nH Fixed Inductor	180nH	TDK	MLF1005VR18JT000	Mouser Electronics	810-MLF1005VR18JT000	2	$ 0.28
L2, L3, L4, L5	Fixed Inductors 0806 .27uH 273mOhms +/-5%Tol 510mA	270nH	Taiyo Yuden	LBM2016TR27J	Mouser Electronics	963-LBM2016TR27J	4	$ 0.21
L7, L11	82nH Fixed Inductor	82nH	TDK	MLF1608D82NMTA00	Mouser Electronics	810-MLF1608D82NMTA00	2	$ 0.16
L8, L9, L10	Fixed Inductors 0603 78nH 5% 590mA 0.41ohms 2280MH	75nH	Murata Electronics	LQW18AN75NJ8ZD	Mouser Electronics	81-LQW18AN75NJ8ZD	3	$ 0.29

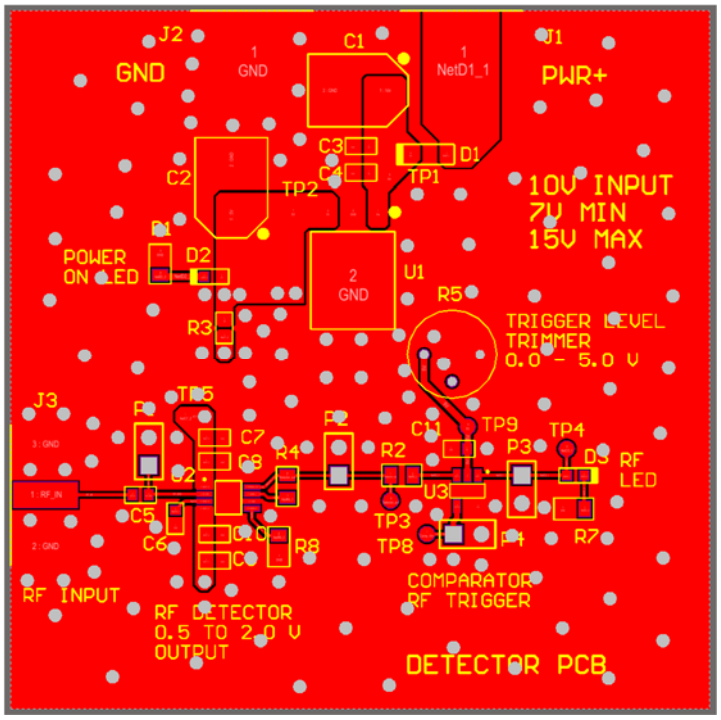
Detector Filter Circuits	
Total BOM Cost	$17.15
PCB Cost 2-layer 3.000” by 2.400” 0.062” thick FR-4 substrate	$26.00
Total Cost	**$43.15**

C.5 – Detector Circuit

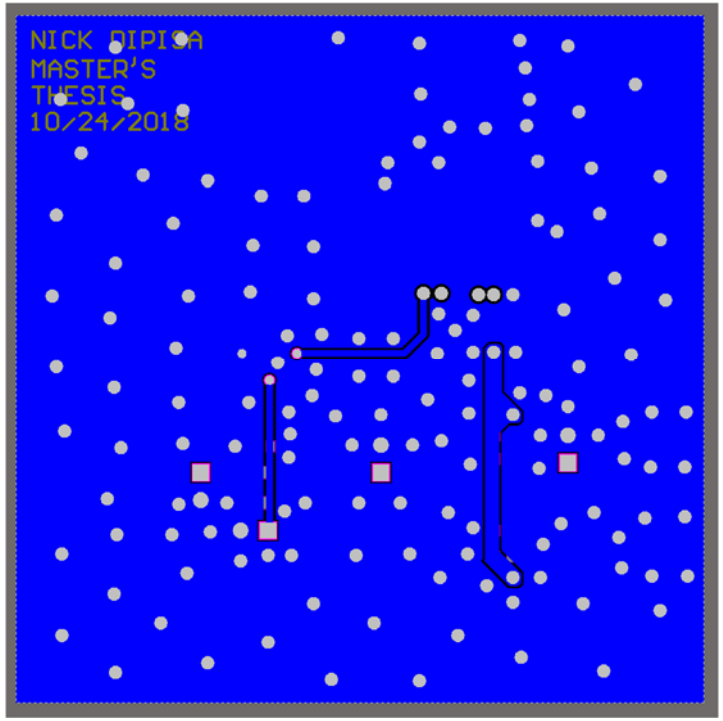




Detector Circuit with Hand Modifications for MCP6546 Troubling Shooting



Top Layer

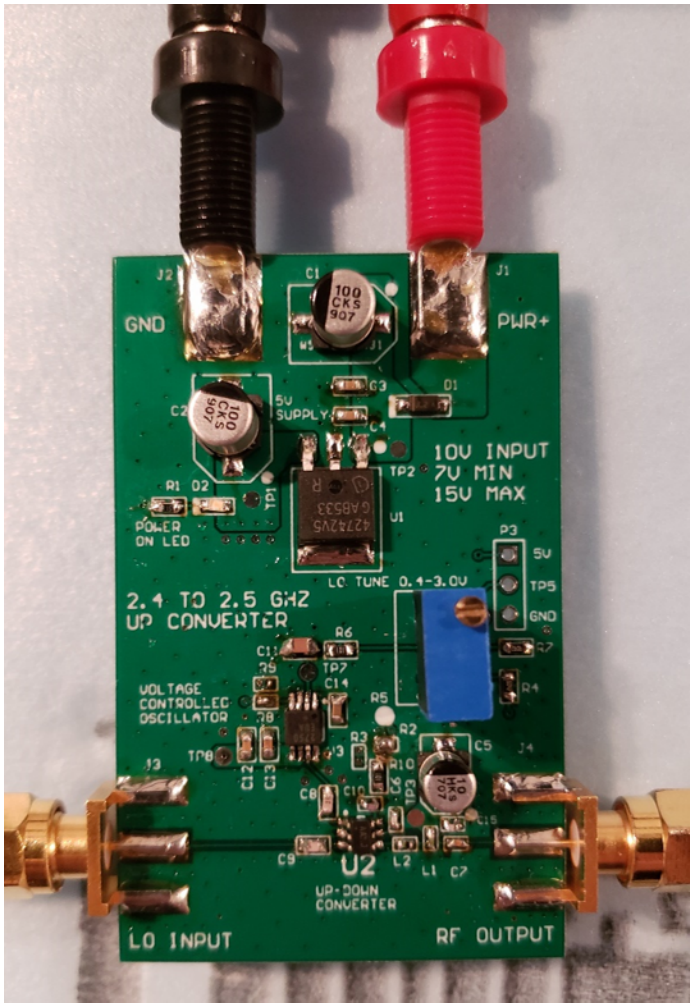


Bottom Layer

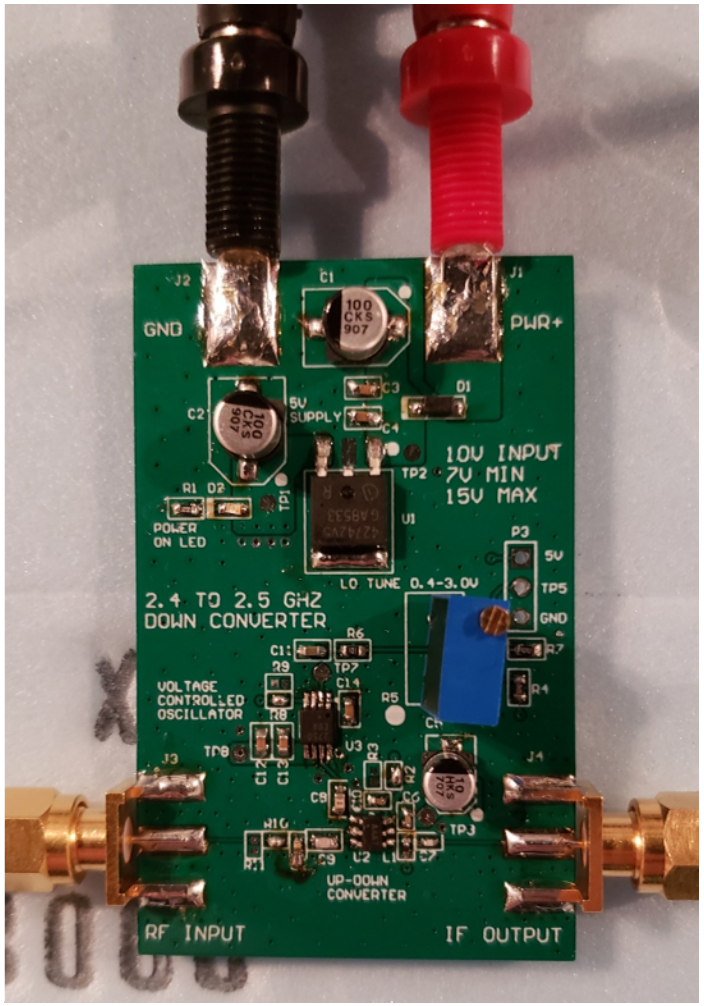
Designator	Description	Value	Manufacturer	Manufacturer P/N	Vendor	Vendor P/N	Quantity	Price
C1, C2	Aluminum Electrolytic Capacitors - SMD 16VDC 100uF 20%	100 uF	Panasonic	EEE-FK1C101SR	Mouser Electronics	667-EEE-FK1C101SR	2	$ 0.42
C3, C4, C7, C9, C11	CAP CER 0.1UF 25V X7R 0603	0.1uF	Wurth Electronics Inc.	885012206071	Digi-Key Electronics	732-7989-1-ND	5	$ 0.10
C5, C6	CAP CER 680PF 100V X7R 0603	680 pF	Wurth Electronics Inc.	885012206107	Digi-Key Electronics	732-12237-1-ND	2	$ 0.10
C8, C10	CAP CER 100PF 25V X7R 0603	100 pF	Wurth Electronics Inc.	885012206053	Digi-Key Electronics	732-7972-1-ND	2	$ 0.10
D1	Schottky Diodes & Rectifiers Schottky Power Rect .5a		ON Semiconductor/Fairchild	MBR0520L	Mouser Electronics	512-MBR0520L	1	$ 0.37
D2, D3	Standard LEDs - SMD WL-SMCW SMDMono TpVw Water		Wurth Electronics	150060GS75000	Mouser Electronics	710-150060GS75000	2	$ 0.14
J1, J2	Test Plugs & Test Jacks BANANA JACK RED		Johnson/Cinich Connectivity Solutions	108-0902-001	Mouser Electronics	530-108-0902-1	2	$ 0.65
J3	CONN SMA RCPT STR 50OHM EDGE MNT		Molex	0732511150	Digi-Key Corp.	WM5534-ND	1	$ 3.33
P1, P2, P3, P4	SIL VERTICAL PC TAIL PIN HEADER		Harwin Inc.	M20-9990246	Digi-Key Corp.	952-2262-ND	4	$ 0.11
R1, R7	RES SMD 1K OHM 5% 0.4W 0805	1.0k	Rohm Semiconductor	ESR10EZPJ102	Rohm Semiconductor	RHM1.0KKCT-ND	2	$ 0.10
R2	RES SMD 100K OHM 0.5% 1/10W 0805	100k	Susumu	RR1220P-104-D	Digi-Key Electronics	RR12P100KDCT-ND	1	$ 0.11
R3	RES SMD 75 OHM 1% 0.4W 0805	75	Rohm Semiconductor	ESR10EZPF75R0	Digi-Key Electronics	RHM75.0AECT-ND	1	$ 0.17
R4, R8	0805 Chip Resistor - Standard	0					2	$ -
R5	TRIMMER 500K OHM 0.5W PC PIN TOP	500k	Bourns Inc.	3339P-1-504LF	Digi-Key Electronics	3339P-504LF-ND	1	$ 5.76
U1	5V 400mA LDO		Infineon Technologies	TLE4274-2D V50	Mouser Electronics	726-TLE42742DV50	1	$ 1.82
U2	IC RF DETECT 50MHZ-1GHZ 8UMAX		Maxim Integrated	MAX2014EUA+	Digi-Key Electronics	MAX2014EUA+-ND	1	$ 6.91
U3	IC COMP SGL OPN DRN 1.6V SOT23-5		Microchip Technology	MCP6546T-I/OT	Digi-Key Electronics	MCP6546T-I/OTCT-ND	1	$ 0.37

Detector Circuit	
Total BOM Cost 2 circuits required	$22.80
PCB Cost 2-layer 2.500” by 2.500” 0.062” thick FR-4 substrate	$38.35
Total Cost	**$83.95**

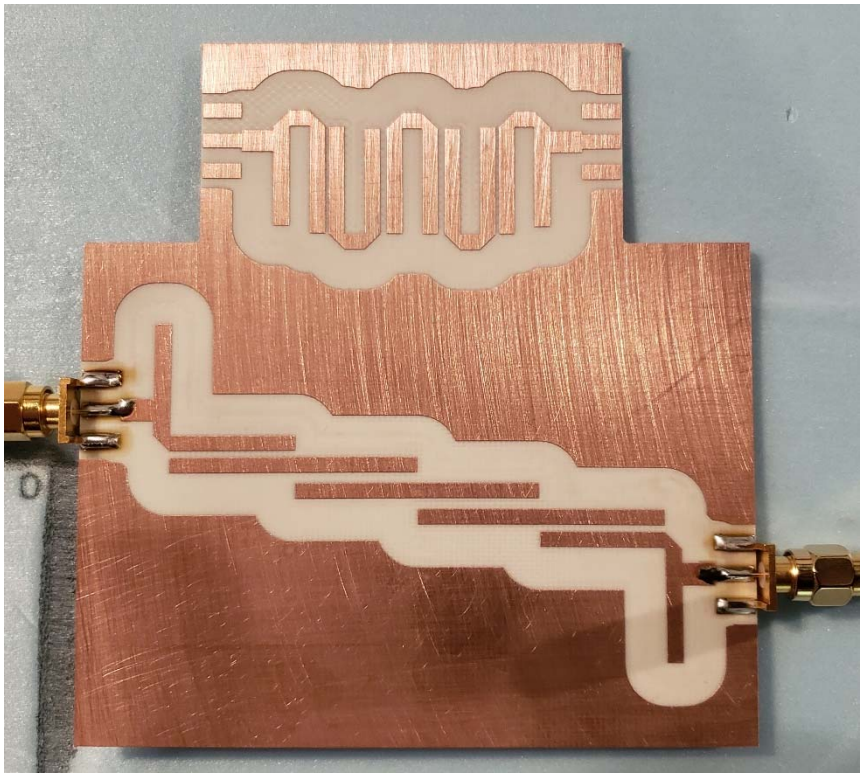
Appendix D – Constructed Circuits and Measurement Pictures



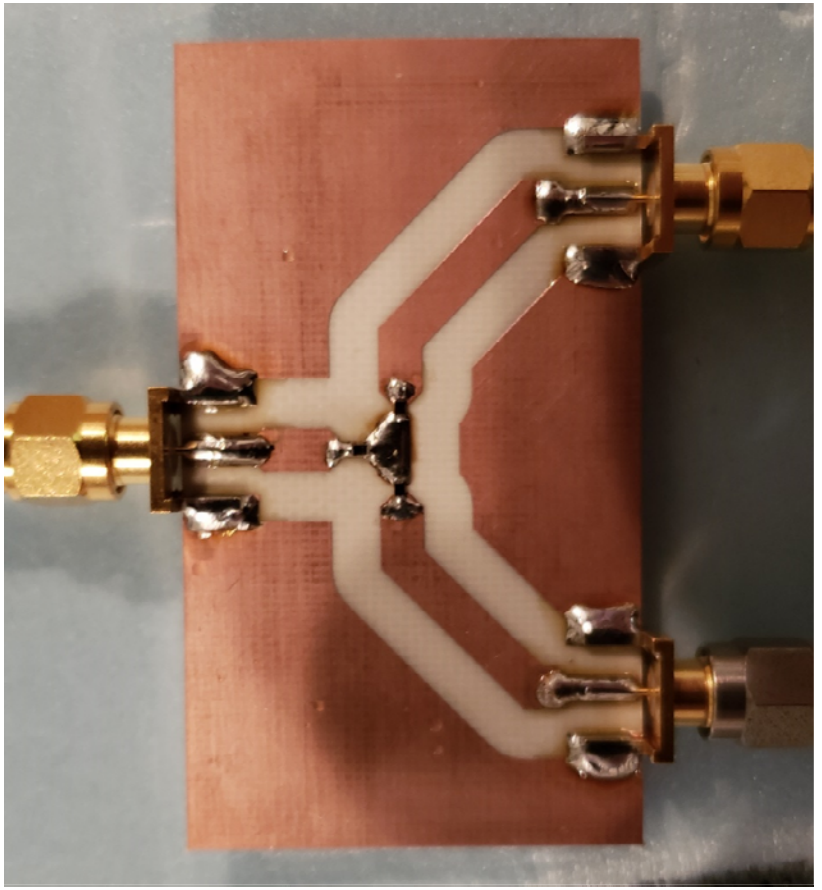
Transmit Circuit PCB



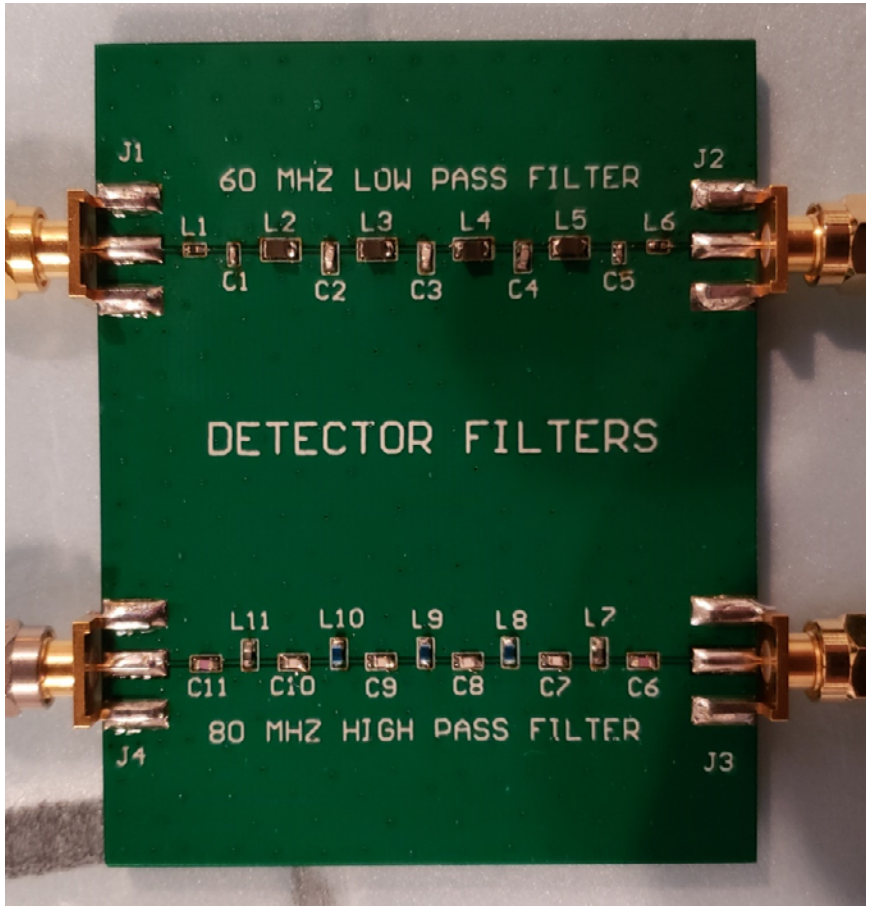
Receive Circuit PCB



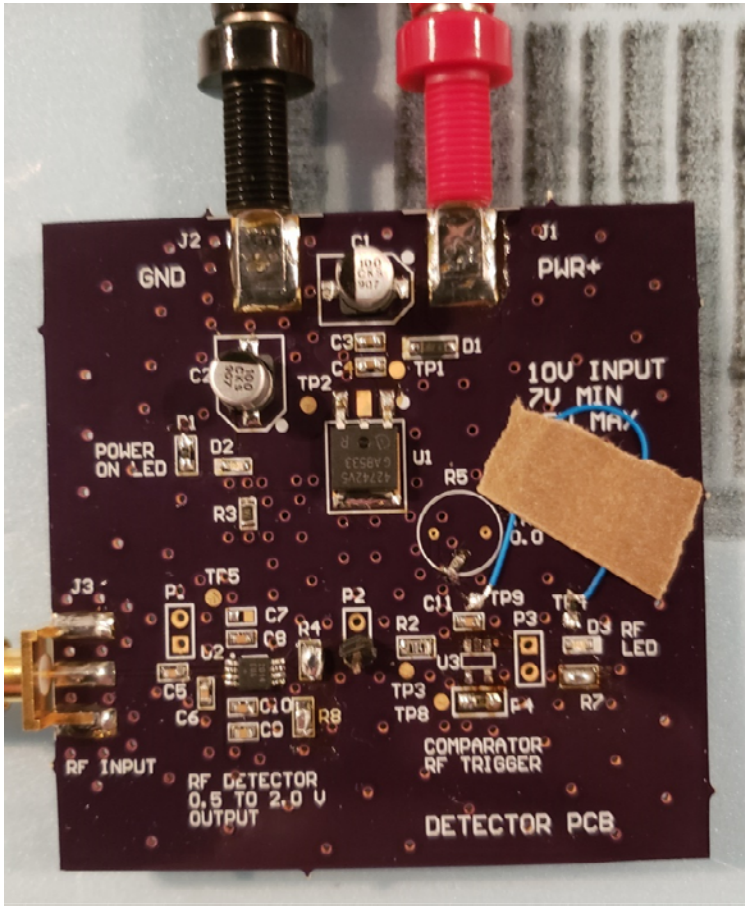
2400 MHz Transmit/Receive Filter PCB



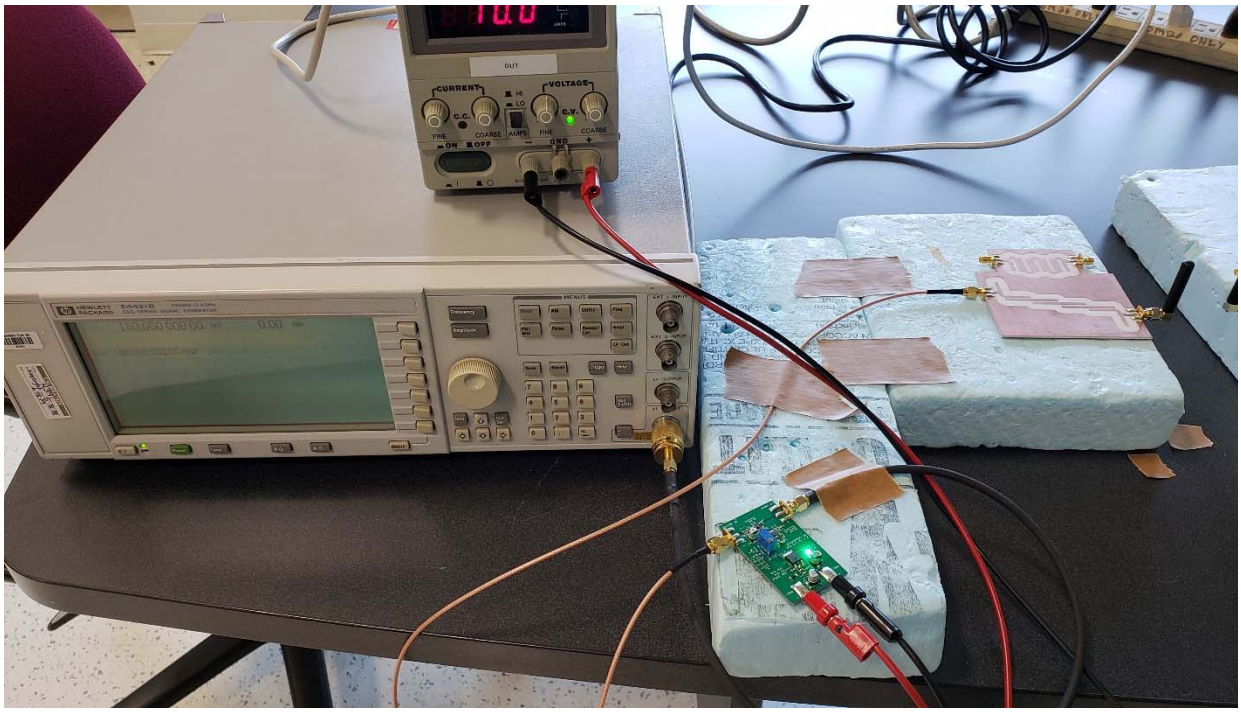
Three-port Resistive Splitter PCB



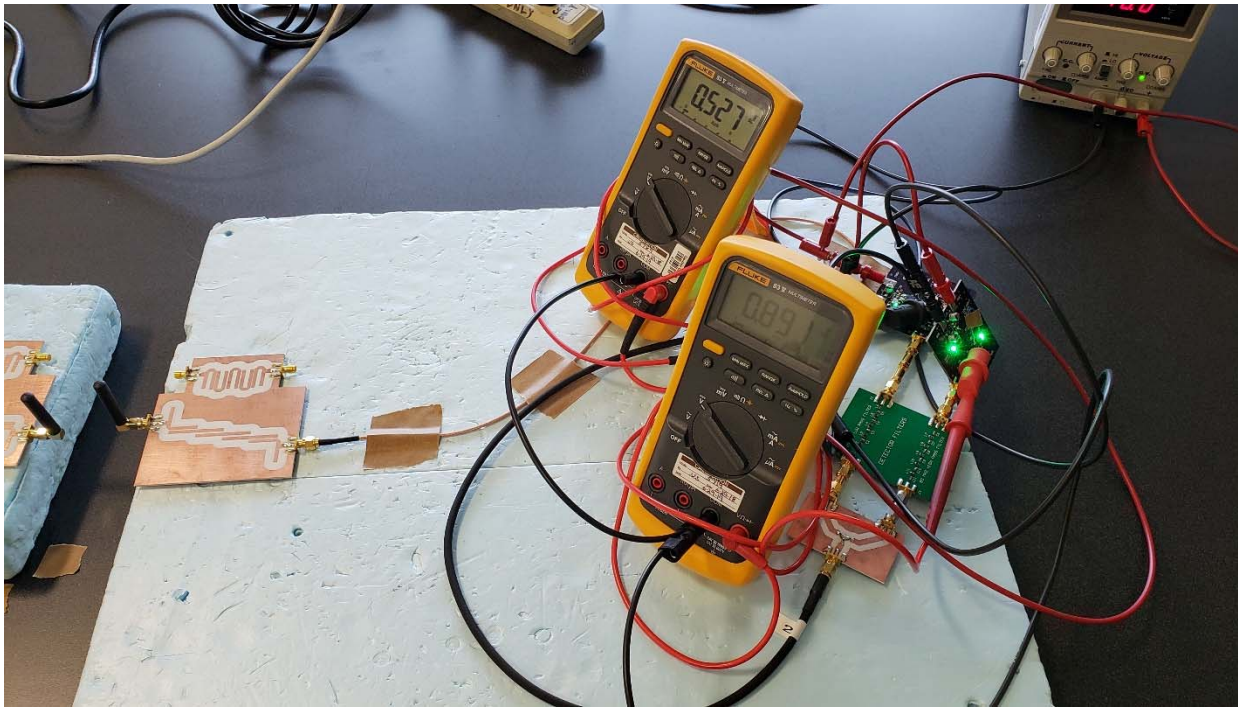
Detector Filter PCB



Detector Circuit PCB with Hand Modifications



Transmit Test Equipment Setup



Receive Test Equipment Setup

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